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Opportunities for Radio Frequency Nanoelectronic Integrated Circuits Using Carbon-Based Technologies

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Diese Dissertation ist meinen Eltern und Anni gewidmet.

This thesis is dedicated to my parents and to Anni.

Abstract

Opportunities for Radio Frequency Nanoelectronic Integrated Circuits Using Carbon-Based Technologies

This thesis presents a body of work on the modeling of and performance predictions for carbon nanotube field-effect transistors (CNFET) and graphene field-effect transistors (GFET). While conventional silicon-based CMOS is expected to reach its ultimate scaling limits during the next decade, these two novel technologies are promising candidates for future high-performance electronics. The main goal of this work is to investigate on the opportunities of using such carbon-based electronics for RF integrated circuits. This thesis addresses 1) the modeling of noise and process variability in CNFETs, 2) RF performance predictions for CNFETs, and 3) an accurate GFET compact model.

This work proposes the first CNFET noise compact model. Noise is of primary importance for RF applications and its description significantly increases the insight gained from simulation studies. Furthermore, a CNFET variability model is presented, which handles tube synthesis and metal tube removal imperfections. These two model extensions have been added to the Stanford CNFET compact model and allow for the variability-aware RF performance assessment of the CNFET technology.

In continuation, comprehensive RF performance projections for CNFETs are provided both on the device and circuit level. The overall set of ITRS RF-CMOS technology requirement FoMs is determined and shows that the CNFET performs excellently in terms of speed, gain, and minimum noise figure. Furthermore, for the first time FoMs are reported for the basic RF building blocks low-noise amplifier and oscillator. In addition, it is shown that CNFET downscaling yields significant performance improvements. Based on these analyses it is confirmed that the CNFET has the potential to outperform Si-CMOS in RF applications.

A third key contribution of this thesis is the development of an accurate GFET compact model. Previous compact models simplify several physical aspects, which can cause erroneous simulation results. Here, an accurate yet simple mathematical description of the GFET's current-voltage relation is proposed and implemented in Verilog-A. Comprehensive error analyses are done in order to highlight the advantages of the new approach. Furthermore, the model is verified against measurement results. The developed GFET model is an important step towards better understanding the characteristics and opportunities of graphene-based analog circuitry.

Acknowledgments

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Abbreviations

AC	**A**lternating **C**urrent
ADC	**A**nalog-**D**igital **C**onverter
BiCMOS	**Bi**polar-**C**omplementary **M**etal-**O**xide-**S**emiconductor
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
CNFET	**C**arbon **N**anotube **F**ield-**E**ffect **T**ransistor
CNT	**C**arbon **N**ano**T**ube
CVD	**C**hemical **V**apor **D**eposition
DAC	**D**igital-**A**nalog **C**onverter
DC	**D**irect **C**urrent
DOS	**D**ensity **O**f **S**tates
EM	**E**lectro**M**agnetic
ERD	**E**merging **R**esearch **D**evice
FET	**F**ield-**E**ffect **T**ransistor
FoM	**F**igure-**o**f-**M**erit
GFET	**G**raphene **F**ield-**E**ffect **T**ransistor
HDL	**H**ardware **D**escription **L**anguage
HEMT	**H**igh-**E**lectron-**M**obility **T**ransistor
IC	**I**ntegrated **C**ircuit
IF	**I**ntermediate **F**requency
ITRS	**I**nternational **T**echnology **R**oadmap for **S**emiconductors
LNA	**L**ow-**N**oise **A**mplifier
LO	**L**ocal **O**scillator
LTE	**L**ong **T**erm **E**volution
mCNT	**m**etallic **C**arbon **N**ano**T**ube
MG	**M**ulti-**G**ate

mmW	**m**illi**m**eter **W**ave
MOS	**M**etal-**O**xide-**S**emiconductor
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield-**E**ffect **T**ransistor
NEMS	**N**ano**E**lectro**M**echanical **S**ystem
NNTB	**N**earest-**N**eighbour **T**ight-**B**inding
PA	**P**ower **A**mplifier
PCSNIM	**P**ower-**C**onstrained **S**imultaneous **N**oise and **I**nput **M**atching
PDF	**P**robability **D**ensity **F**unction
PSD	**P**ower **S**pectral **D**ensity
RF	**R**adio **F**requency
RV	**R**andom **V**ariable
sCNT	**s**emiconducting **C**arbon **N**ano**T**ube
S/D	**S**ource/**D**rain
SiP	**S**ystem-**i**n-**P**ackage
SoC	**S**ystem-**o**n-**C**hip
VCO	**V**oltage-**C**ontrolled **O**scillator
VLSI	**V**ery-**L**arge-**S**cale **I**ntegration

Chapter 1

Introduction

DURING the last decades we have witnessed tremendous performance improvements in the field of electronics, primarily driven by our information society's need for cheap but increasingly complex devices for consumer electronics, medical systems, and many more. This has not only provided us with new tools for our everyday life, but triggered significant advancements in engineering and science and has therefore lead to improvements of the quality of life in large parts of the world. The history of electronics is a success story which is to a great extent due to the continuous evolution of its workhorse, the silicon-based complementary metal-oxide-semiconductor (CMOS) technology. However, with every new technology generation increasingly severe manufacturing issues appear. This is why the scientific community spends enormous research efforts to find a substitute for conventional CMOS that will be based on other materials than silicon. During the last years carbon semiconductors have emerged as an exciting new candidate among them. This thesis is dedicated to give a deeper insight to these novel technologies from an RF engineering point of view. For that purpose, this work treats the modeling of and performance projections for carbon-nanotube field-effect transistors (CNFET) and graphene field-effect transistors (GFET).

This introduction is organized as follows: Sec. 1.1 discusses the miniaturization and limits of Si-based CMOS and presents the spectrum of emerging technologies. Then, Sec. 1.2 describes the trend towards a functional diversification of integrated circuits (IC). Sec. 1.3 gives an introduction to the history and the promising properties of carbon-based semiconductors. Finally, Sec. 1.4 presents the outline of this thesis.

1.1 Moore's law and the end of scaling

The continuous downscaling of the transistor size has been and still is the guiding principle for the improvement of the CMOS technology. The first metal-oxide-semiconductor field-effect-transistor (MOSFET) was manufactured in the year 1960 and had a gate length of 20 µm [1]. Since then, the minimum feature size, at which semiconductor devices can be produced cost-effectively, is shrinking with a factor of about 0.7 every two years. This has already been stated in 1965 as "Moore's Law" [2] and implies an increase of device density by a factor of two for every two years (Fig. 1.1). State-of-the-art technologies for the mass market now have a minimum feature size of 22 nm [3] and have an extraordinarily low cost per function. While in 1962 the average transistor selling price was about 1$, up to today it has dropped to nanodollars [4]. The International Technology Roadmap for Semiconductors (ITRS) [5] predicts a continuation of this scaling trend. In the year 2028, the time horizon of the ITRS 2013 projections, a gate length of 5.1 nm will be required for high-performance logic circuitry.

With continuous device scaling, an increasing number of process integration challenges appear. Among them are the control of short-channel degradation, the growth of high-κ gate dielectrics on high-mobility channel materials with a defect-free interface, source/drain engineering for reduced parasitic resistances, and controlling threshold voltage variability due to lithography limitations and random dopant fluctuations [5]. Addressing these issues will get increasingly difficult and costly, and finally fundamental physical limits for devices at atomic scale will mark the end of decades of CMOS scaling.

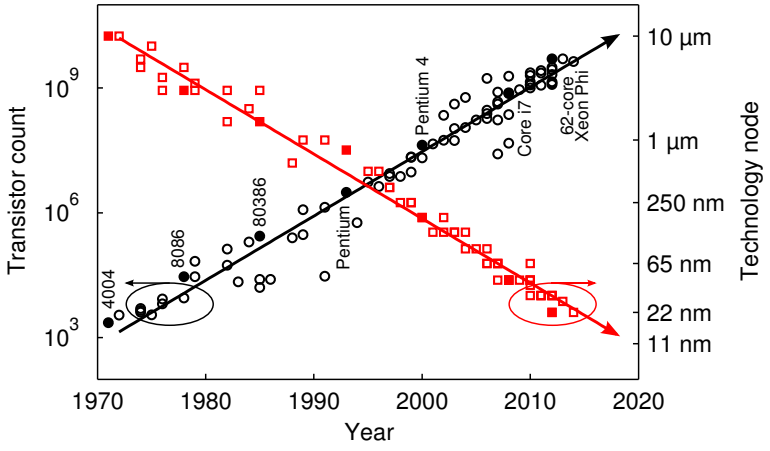

FIGURE 1.1: Transistor count and technology node of Intel, AMD, Motorola, and IBM microprocessors introduced between the years 1971 and 2014, illustrating Moore's law. Several milestone Intel mircoprocessors are indicated.

With this scenario on the horizon, the semiconductor industry currently follows the "More Moore" strategy (Fig. 1.2). It consists of enabling further downscaling by introducing technology enhancements that yet do not alter the functional principle of CMOS. In recent years this has been achieved with strained silicon [6], metal/high-κ gate stacks [7], fully depleted silicon-on-insulator, and three-dimensional channel geometries [8]. The replacement of the silicon channel by better performing semiconductors is forseen as the next step in CMOS evolution, but is still in the prototype phase. Apart from the More Moore concept, there exist further advanced "Beyond CMOS" technologies, that will possibly replace CMOS in the long term. However, they are still in an embryonic state. They will first use charge-based information carriers, but later may be based on completely new information processing paradigms using non-charge-based concepts (*e.g.*, spin waves or magnetic fields).

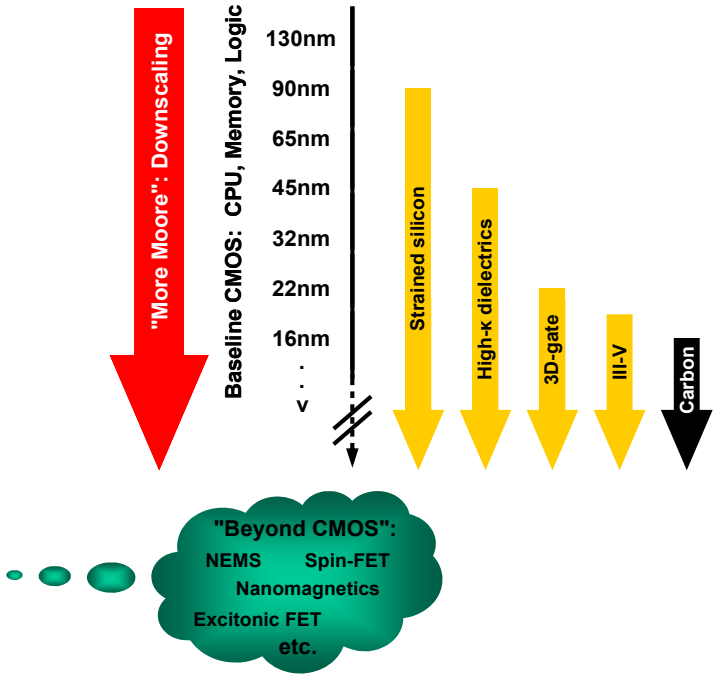

FIGURE 1.2: The "More Moore" concept stands for extending CMOS to the end of the roadmap by downscaling the transistor size, but without altering the transistors' functional principle. Future scaling will likely be enabled by replacing the silicon channel first by III-V compound semiconductors and then by carbon-based materials. In contrast to "More Moore", the "Beyond CMOS" concept stands for future devices that are based on completely new functional principles (from [9], modified).

1.1.1 Emerging research devices

The prototype "More Moore" and "Beyond CMOS" technologies are referred to as emerging research devices (ERD). According to the ITRS they are classified as follows [5]:

- *More Moore: Extending MOSFETs to the end of the roadmap*
  The technically most mature aspirant to substitute conventional Si-based CMOS is a channel replacement by III-V compound semiconductors [10] and germanium [11] grown on a Si substrate. These materials show superior carrier mobility for n- and p-type channels, respectively. Then, devices may evolute towards a nanowire geometry [12], which allows for an efficient gate control over the channel to limit short-channel effects. Finally, ultimate CMOS scaling may be reached by exploiting the extremely high mobility and low-dimensional structure of carbon-based channels, *i.e.*, carbon-nanotubes (CNT) [13] and graphene nanoribbons [14, 15]. In parallel, the tunnel field-effect transistor [16] with its steep sub-threshold slope is handled as an additional promising technology that targets low-power applications.

- *Charge-based Beyond CMOS: Non-conventional field-effect transistors (FET) and other charge-based information carrier devices*
  This class of EMDs involves electron transport, but has a switching functionality that is entirely different from the one of conventional FETs. Among these devices are the spin transistor [17], the impact ionization metal-oxide-semiconductor transistor [18, 19], nanoelectromechanical switches [20], and atomic switches [21].

- *Non-FET, non charge-based Beyond CMOS devices*
  Technologies using information carriers that are not an electronic charge will require the longest period until their possible introduction. A nonexhaustive list includes spin wave devices [22], nanomagnetic logic [23], and the excitonic FET [24].

Traditionally, the investigations on the mentioned CMOS and ERD technologies were driven by information processing, transmission, and storage applications. However, there is a trend towards using these technologies not only in the digital domain, but also for additional non-digital functionalities, as will be discussed in the following section.

1.2 The "More than Moore" concept

In addition to the "More Moore" evolution of digital ICs, there exists a second axis of developmant labeled "More than Moore" [9] (Fig. 1.3). During the last two decades there has been a trend towards a functional diversification of ICs for a better interaction with the analog user environment. Traditionally, CMOS processes were mostly limited to provide logic and memories for information and communication technologies, but particularly since the beginning of the 21st century, More than Moore components such as analog/radio-frequency (RF) building blocks and microelectromechanical systems have been cointegrated with conventional CMOS. This has sparked a revolution in economic segments such as mobile communications, automotive security systems, fast diagnostic medical equipment, and imaging. Indeed, since the year 2000, communication and consumer markets outperform computing markets regarding the revenues for semiconductor companies [25].

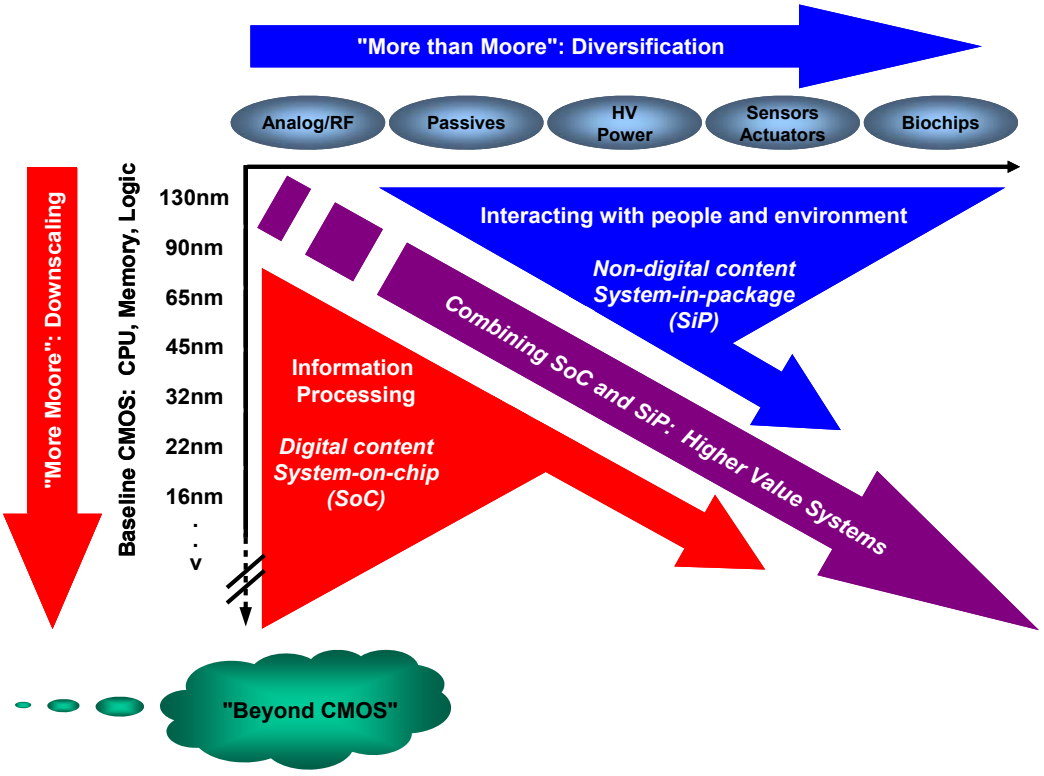

FIGURE 1.3: The "More than Moore"concept stands for the functional diversification of ICs (from [9], modified).

Historically, high-speed analog circuitry was reserved to bipolar technologies and III-V compound semiconductors, which were integrated on separate dies and assembled together with the digital part on a printed circuit board or as a System-in-Package (SiP). In the 1990s, the Bipolar-CMOS (BiCMOS) technology gained importance and allowed the integration of bipolar junction transistors together with CMOS on the same die to realize Systems-on-Chip (SoC) [26]. However, BiCMOS requires many extra process steps and so it is economically less viable than the individual CMOS technology. During the last decade BiCMOS has therefore been displaced to a large extent. Due to the increasing operating frequencies of CMOS transistors it is now possible to realize digital, analog, and even RF functions with conventional CMOS. As a result of to the economy of scale of CMOS, SoCs and with them the More than Moore concept are today applied profitably in wide market segments.

As mentioned in the previous section, III-V compound semiconductors on a Si substrate will likely be the successor of conventional Si-based CMOS in the More Moore domain and this trend will be extended to More than Moore applications. However, according to the 2013 ITRS, in the year 2022 even these III-V materials will fail to satisfy RF device requirements [5]. This is where a rapidly progressing novel technology based on an economic raw material with excellent intrinsic properties enters the stage: carbon electronics.

1.3 The rise of carbon-based technologies

Carbon allotropes are a group of materials that are formed of the chemical element carbon, but which differ in their crystalline structure. Historically, coal and diamond were the first carbon allotropes that have been exploited. Coal is an amorphous form of carbon and is used since centuries as a source of thermal energy [Fig. 1.4.(a)]. Diamond consists of carbon bonded in the form of two overlapping cubic face-centered lattices and is known for its extreme hardness and high thermal conductivity [Fig. 1.4.(b)]. Cutted and polished it is appreciated as a gemstone for jewelry. A third carbon allotrope that is known since long is graphite, which consists of stacked graphene layers, that is, of stacked one-atom-thick layers of carbon atoms arranged in a honeycomb lattice. Graphite has been mined since the 16th century and is for instance used as a material for pencils [Fig. 1.4.(c)].

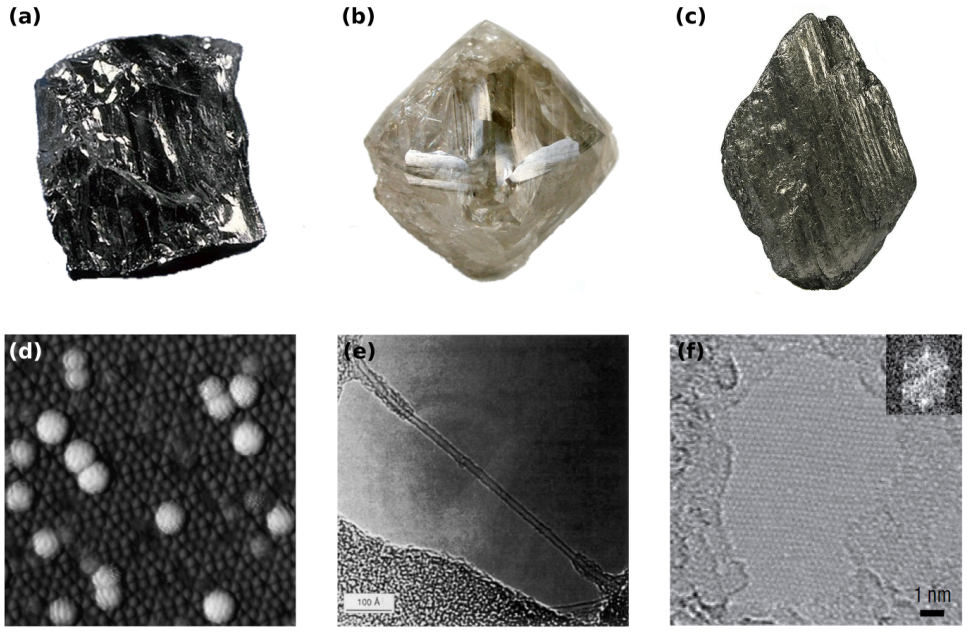

FIGURE 1.4: Carbon-based materials: (a) anthracite coal, the variety of coal with the highest carbon content [27] (b) diamond, carbon atoms in two overlapping cubic face-centered lattices [28] (c) graphite, stacked layers of graphene [28] (d) C_{60}-buckminsterfullerene, a spherical molecule with a truncated icosahedron structure [29] (e) carbon nanotube, a cylindrical structure with its wall formed of graphene [30] (f) graphene, carbon atoms bonded in a hexagonal honeycomb lattice [31].

1.3.1 New carbon allotropes

In recent decades, the family of carbon allotropes has been extended by several new materials (Fig. 1.5) of most interesting physical properties. In the year 1985, Kroto *et al.* experimentally discovered the zero-dimensional buckminsterfullerene [32], which is a spherical carbon molecule with the chemical formula C_{60} [Fig. 1.4.(d)]. The so-called buckyball is a polyhedron with twenty hexagonal and twelve pentagonal surfaces. It resembles a football as well as the geodesic domes of its eponym, the American architect Richard Buckminster Fuller. Since the discovery of C_{60}, a completely new branch of chemistry developed. That is why its discoverers were awarded the 1996 Nobel Price in Chemistry. There have been intents to exploit this material for electronics, but up to now the obtained results are mostly limited to thin-film transistors with a carrier mobility of several $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [33]. C_{60} is therefore not handled as a possible replacement for silicon electronics.

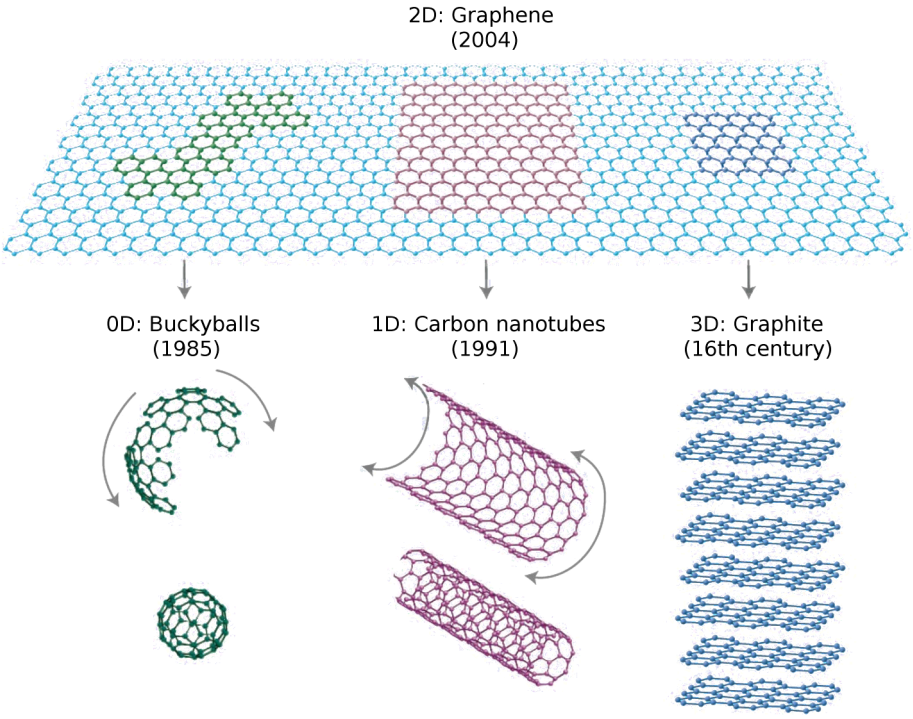

FIGURE 1.5: Carbon allotropes and the year of their discovery. A sheet of graphene can be imagined as being the basis material for buckminsterfullerene, carbon nanotubes and graphite by wrapping it up into a sphere, rolling it into a tube or stacking it, respectively (from [34], modified).

In 1991, the multi-wall CNT [35] has been discovered. Two years later, the single-wall CNT [30] has been intentionally manufactured for the first time and with it a promising candidate for replacing silicon in advanced electronic devices has been found [Fig. 1.4.(e)]. Due to its one-dimensional structure, the CNT shows reduced carrier scattering and near-ballistic transport at room temperature [36]. Furthermore, the CNT has the ability to sustain enormous current densities [37] and has excellent thermal conductance [38] and mechanical strength [39]. In 1998, the first CNFET prototypes based on this material were manufactured [40, 41]. Since then research on CNT-based microelectronics devices has been progressing at a rapid pace and up to today CNFETs have reached an intrinsic cut-off frequency f_T of 153 GHz [42]. Furthermore, the CNT has been proposed as a replacement for Cu in very-large-scale integration (VLSI) interconnects [43] and is handled as a key enabler of More than Moore applications such as nanoelectromechanical systems (NEMS) [44, 45] and biosensors [46].

A second wave of investigations on carbon-based electronics was triggered in the year 2004 by the discovery of the two-dimensional carbon allotrope graphene [Fig. 1.4.(f)],

which was published in a landmark paper of Novoselov, Geim, *et al.* [47]. Although for decades free-standing graphene was believed to be inherently unstable and to decompose to fullerenes and soot, it was possible to isolate this one-atom thick hexagonal lattice of carbon atoms by micromechanical cleavage of bulk graphite. Graphene has soon been recognised as a "wonder material". It has a giant intrinsic charge carrier mobility and shows ballistic transport over several µm [48] as well as an excellent thermal conductivity [49], mechanical strength [50], and current carrying capability [51]. During the last decade, the interest on the physics and applications of graphene has been ever growing [34, 52, 53] and for their ground-breaking experiments Novoselov and Geim have been awarded the 2010 Nobel Prize in Physics. In the field of microelectronics, graphene nanoribbons target future digital circuitry and large-area graphene is a candidate for future RF electronics [54], although it has no bandgap. The fastest GFET is currently reaching an intrinsic f_{T} of 427 GHz [55]. Further possible graphene applications are, amongst others, photonics, sensors, and bioapplications [53].

1.3.2 Technology outlook

It is widely accepted that within this decade the immaturity of carbon-based technologies impedes their viable employment in ICs. Therefore, the industry currently targets less stringent applications such as thin-film electronics on flexible substrates [56, 57] and transparent conductive coatings for touch screens or e-papers [58, 59]. However, recent roadmaps [53, 60] predict that the growth of large-area high-quality graphene and the purification and placement of CNTs may be sufficiently controlled at the beginning of the 2020s to apply these materials in high performance electronics. In particular, analog/RF electronics will likely be the first to benefit from carbon-based materials, as they have the advantage of relaxed manufacturing requirements in comparison to digital circuitry. In addition, these applications can tolerate the always-on behavior of zero-bandgap graphene. This market insertion of CNTs and/or graphene will be just in time to replace III-V high-frequency transistors, for which according to ITRS projections no manufacturable solutions are known from 2022 on to obtain the required cut-off frequency f_{T} and maximum oscillation frequency f_{max} [5].

1.4 Outline of this thesis

The introduction to this thesis has given an overview of the historical development of VLSI and has then discussed emerging technology options. It has identified carbon-based electronics as a serious candidate not only for future digital VLSI, but especially for analog/RF applications in a More than Moore scenario.

The remainder of this thesis is structured as follows: Chapter 2 reviews technological and theoretical fundamentals of this thesis. Subsequently, Chapter 3 defines the thesis's objectives and the applied methodology. Then, from Chapter 4 on, original contributions are presented. Chapter 4 treats CNFET manufacturing process variability and noise modeling. These two model extensions build the basis for further investigations on CNFET figures-of-merit (FoM) on device and circuit level, which are presented in Chapter 5. In continuation, the focus changes over from CNTs to graphene. Chapter 6 proposes a highly accurate GFET compact model, which is provided as a tool for the exploration of GFET-based integrated circuit design. Finally, Chapter 7 is dedicated to the overall conclusions of this thesis.

Chapter 2

Technological and theoretical fundamentals of this thesis

CARBON NANOTUBES and GRAPHENE are promising candidates for RF nanoelectronics in future "More than Moore" ICs. This chapter serves as a groundwork for the following parts of this thesis by reviewing three basic aspects of such carbon-based RF electronics: 1) a general overview of RF electronics, 2) carbon-based electronics in particular, and 3) the electronic structure of these two novel materials.

Sec. 2.1 provides a general introduction to RF electronics with a focus on communication systems. It discusses the need to exploit the technologically challenging THz band (300 GHz - 3 THz) for future ultra-high bandwidth communication systems. Then it reviews the building blocks for such systems on the device and circuit abstraction level, and finally discusses RF transceiver architectures. Subsequently, Sec. 2.2 first reviews the basic physical properties of graphene and CNTs and compares them to conventional materials. Then it gives a practical overview of the state-of-the-art manufacturing capabilities and RF performance of carbon-based devices and circuits. Finally, Sec. 2.3 provides theoretical insight into the electronic structure of graphene and CNTs.

This chapter gives a general introduction to the wide field of carbon-based RF electronics. In the remainder of this thesis, the detailed state-of-the-art of the treated specific areas will be presented in each respective chapter.

2.1 Radio frequency electronics

The following review of important aspects of RF electronics focuses on wireless communication systems and their building blocks (see Fig. 2.1), as these systems are a main driver for the development of integrated analog electronics. First, the trend towards THz communication systems is presented and the need for improved RF devices is justified. Then, in a bottom-up approach, the basic characteristics of RF transistors, common low-level building blocks of RF front-ends (*e.g.*, amplifiers and oscillators), and finally receiver and transmitter architectures for such front-ends are discussed.

2.1.1 Communication systems as drivers for RF electronics

Wireless communication systems show an increasing demand for high data rates. Today the Long Term Evolution (LTE) broadband communication standard for mobile phones marks the speed limit of mass market products with its peak download rate of $300\,\mathrm{Mbit\,s^{-1}}$, but until the beginning of the next decade data rates will have increased to around $10\,\mathrm{Gbit\,s^{-1}}$ (see Fig. 2.2). This will push economically promising applications

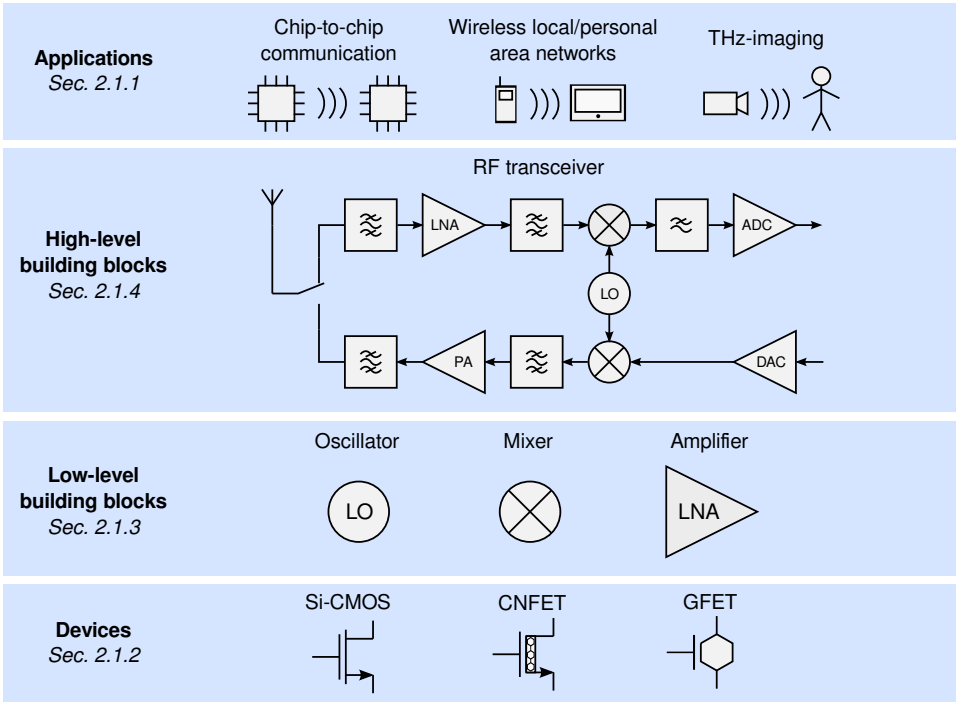

FIGURE 2.1: RF electronics: overview of different abstraction levels.

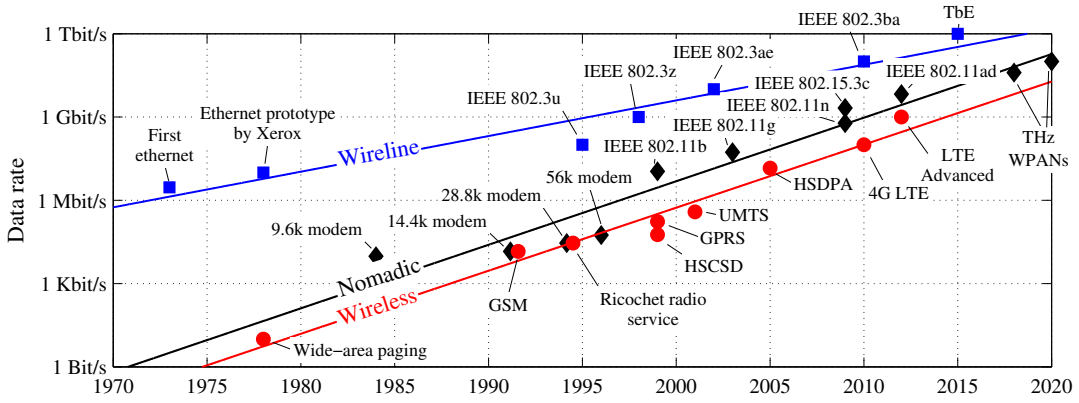

FIGURE 2.2: Chronology of the data rates of wireless, nomadic, and wireline communication standards [61].

such as wireless high-definition video streaming, high-speed wireless local- and personal-area networks, and kiosk download of multimedia content from a stationary transmitter to a small mobile receiver [61]. Edholm's Law of Bandwidth states that this evolution of data rates in wireless systems will approach them to the traditionally much faster wireline communication standards [62].

As discussed in [61], a challenging data rate target such as $10\,\mathrm{Gbit\,s^{-1}}$ requires either a high spectral efficiency of the used modulation scheme, a high bandwidth, or a combination of these two characteristics. In the electromagetic (EM) spectrum the largest globally available RF band can be found at a frequency of around 60 GHz with a bandwidth of 7 GHz. Today this frequency range can readily be explored with Si-CMOS technologies [63]. However, in order to achieve the abovementioned data rate goal, a spectral efficiency of $14\,\mathrm{bit\,s^{-1}\,Hz^{-1}}$ would be required, which is highly challenging. A sufficiently wide frequency band for more realistic modulation schemes of a few $\mathrm{bit\,s^{-1}\,Hz^{-1}}$ can only be found in the THz band from 300 GHz to 3 THz. Fig. 2.3 illustrates that still no services occupy this region and it can therefore provide the required ultra-high bandwidths beyond 20 GHz. Until several years ago the THz band was not covered satisfactorily by any technology, which coined the term "THz gap". Classical microwave electronics could only reach the lower limit of this band and optics could not go below its upper limit. Today a spectrum of up to several hundreds of GHz can at least experimentally be exploited with conventional technologies, but a big step towards cost-effective industrial applications using large parts of the THz band is still pending. Given this need for better-performing technologies, carbon-based devices with their predicted excellent RF performance offer themselves as a promising candidate to conquer the THz spectrum.

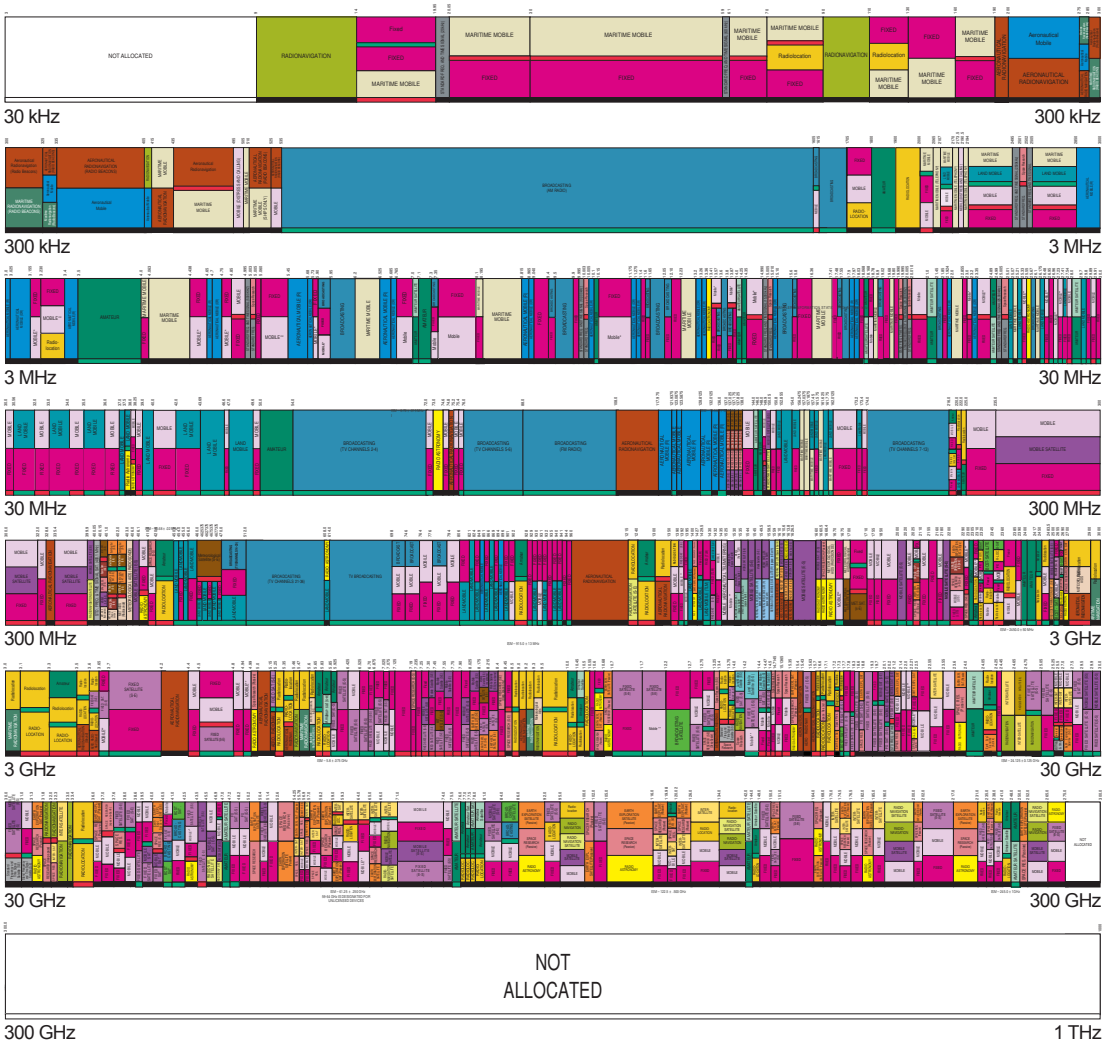

FIGURE 2.3: Electromagnetic spectrum and allocated frequencies [64, 66]. The region from 280 GHz upwards is still not occupied by any service and can therefore be exploited by ultra-high data rate applications.

The possible fields of use of future carbon-based RF electronics are however not limited to communication systems. For instance, a second application being in the starting blocks is THz imaging for biomedical applications, security screening, and material analyses. Furthermore, the Federal Communications Commission Office previews the passive use of these high frequencies for earth exploration satellites and radio astronomy [64] and several space missions already have equipment using this frequency range [65].

2.1.2 Radio frequency transistors

RF systems can be based on vacuum or solid-state devices [67]. Vacuum devices such as klystrons and travelling wave tubes can generate continuous wave signals beyond 100 GHz with a high output power, but they are bulky and their use is limited to special-purpose applications such as satellite communications. Compactness and economic competitiveness clearly point to solid-state electronics for realizing general-purpose RF systems. The use of diodes for the detection and generation of millimeter wave (mmW) signals is already well established and, for instance, Schottky diodes can be used to receive signals beyond 1 THz. However, active elements such as LNAs, PAs, and active mixers rely on transistors. In the remainder of this section the basic characteristics and performance metrics of such RF transistors are discussed. These characteristics are not only valid for conventional FETs, but are also applicable to CNFETs and GFETs.

The large-signal behavior of a transistor is typically decribed by its transfer characteristics [Fig. 2.4.(a)] and output characteristics [Fig. 2.4.(b)], which are plots of the device's drain current I_{D} against its gate-source voltage V_{GS} and drain-source voltage V_{DS}, respectively. Within circuits, DC voltages are applied to the transistor's terminals and drive the device to a certain biasing point. For the insight in the behaviour of linear circuits (*e.g.*, amplifiers) as well as for defining performance metrics it is convenient to linearize the nonlinear large-signal equations around the biasing point. This allows amongst others to obtain a small-signal equivalent circuit such as illustrated in Fig. 2.5, which describes the transistor's behaviour for small input signal variations around a given bias.

An important device-level performance FoM is the transconductance g_{m}, that is, the device's capability of changing the output current I_{D} when changing the input voltage V_{GS}. The output conductance g_0 describes the level of current saturation of a transistor, thus it gives informations about the immunity of I_{D} against V_{DS} variations. While g_{m} should obviously be as high as possible, the ideal g_0 approaches zero, which is yet hard to achieve in short-channel devices. A third basic FoM is the intrinsic gain g_{int}, which is a way to quantify the amplification characteristics of a transistor. The abovementioned three quantities are defined in Eqs. (2.1) to (2.3).

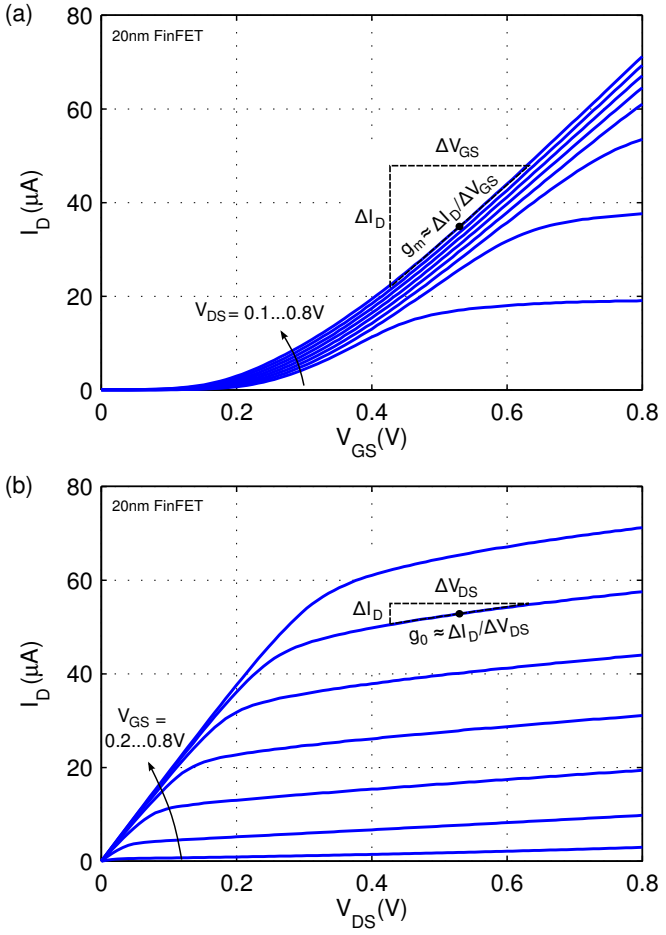

FIGURE 2.4: DC characteristics of a 20 nm FinFET [68]: (a) Transfer characteristics and the definition of the transconductance g_m. (b) Output characteristics and the definition of the output conductance g_0. I_D is the drain current, V_GS the gate-source voltage, and V_DS the drain-source voltage.

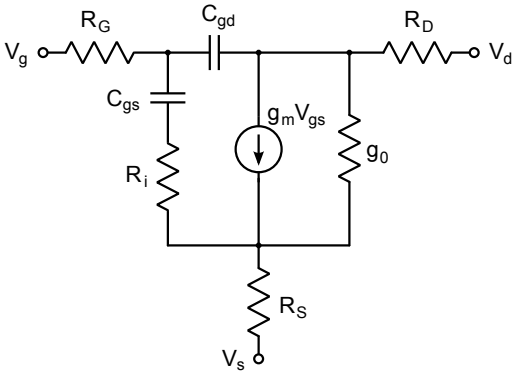

FIGURE 2.5: Small-signal transistor model [69], obtained by linearizing the large-signal behavior around a certain operating point. V_d, V_g, and V_s are small-signal voltages applied at the the drain, gate, and source terminal, respectively. V_gs is $V_\mathrm{g} - V_\mathrm{s}$. g_m is the transconductance and g_0 is the output conductance. C_gd and C_gs are the gate-drain and gate-source capacitances. R_d, R_g, and R_s are parasitic series capacitances at the respective terminals and R_i is the intrinsic gate resistance.

$$g_\mathrm{m} = \frac{\mathrm{d}I_\mathrm{D}}{\mathrm{d}V_\mathrm{GS}} \tag{2.1}$$

$$g_0 = \frac{\mathrm{d}I_\mathrm{D}}{\mathrm{d}V_\mathrm{DS}} \tag{2.2}$$

$$g_\mathrm{int} = \frac{g_\mathrm{m}}{g_0} \tag{2.3}$$

The frequency dependence of a transistor's amplification characteristics is commonly described by the cut-off frequency f_T and the maximum oscillation frequency f_max, which are closely related to the current and power gain, respectively. f_T is the frequency, at which the current gain of a transistor has dropped to unity. Analog to this, f_max is the frequency, at which the unilateral power gain U is unity [69]. An estimate of these two FoMs excluding the effects of extrinsic parasitics can be given as

$$f_\mathrm{T} \approx \frac{g_\mathrm{m}}{2\pi\left(C_\mathrm{gs} + C_\mathrm{gd}\right)} \tag{2.4}$$

$$f_\mathrm{max} \approx \frac{g_\mathrm{m}}{4\pi C_\mathrm{gs}} \cdot \frac{1}{\sqrt{g_0 R_\mathrm{i}}}, \tag{2.5}$$

All used quantities occur in the small-signal model shown in Fig. 2.5. These two equations clearly point out the need for a high g_m and low capacitances. Furthermore, the latter equation indicates that f_max depends on the saturation behaviour of the device.

Finally, the noise figure NF is another performance measure used in the context of RF electronics. It quantifies the degradation of the signal-to-noise ratio caused by the transistor's internal noise sources. Amongst others, NF depends on the degree of matching between the impedance of the signal source Z_Source and the transistor's input impedance for optimum noise Z_opt. By means of a matching circuit, Z_Source can be adapted to Z_opt, which allows to decrease NF to an absolute minimum value NF_min. While NF is given in dB, the noise factor F is its equivalent on a linear scale.

2.1.3 Basic radio frequency building blocks

In the following the basic RF building blocks low-noise amplifier (LNA), power amplifier (PA), oscillator, and mixer are reviewed on the circuit level and common performance FoMs are presented.

2.1.3.1 Low-noise amplifier

The LNA is the first active stage of an RF receiver chain. It is a key element, as its noise directly adds to the overall noise of the chain and therefore crucially influences the sensitivity of the receiver. Commonly, design tradeoffs between noise, gain, linearity, impedance matching, and power dissipation have to be made to achieve amplified but minimally distorted signals for the subsequent receiver stages [70]. In their Mixed-Signal Design Roadmap [71], Brederlow *et al.* provide a performance FoM which covers these tradeoffs:

$$FoM_{\mathrm{LNA}} = \frac{G \cdot IIP_3 \cdot f}{(F-1) \cdot P} \ . \tag{2.6}$$

Here, G is the LNA's gain. The input-referred third-order intercept point $IIP3$ is a measure for the degree of nonlinear distortions and describes the theoretical input power level at which the third order harmonic distortions at the output are as high as the fundamental tone. The noise figure on a linear scale F describes the degradation of the signal-to-noise ratio caused by the LNA's internal noise sources. P is the DC power consumption. By considering the frequency f, the overall FoM is kept frequency-independent.

An example for a typical LNA architecture is the power-constrained simultaneous noise and input matching (PCSNIM) approach [70]. Fig. 2.6 shows the schematic of this architecture. The three passive elements at the gate and source of the FET are dimensioned in such a way that low noise, high gain, and low power consumption can simultaneously be achieved.

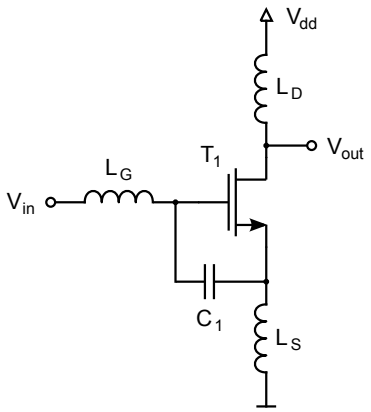

FIGURE 2.6: Low-noise amplifier circuit schematic. This example represents the PCSNIM architecture, which permits simultaneous noise and input matching for a limited transistor size and power consumption by dimensioning the three passives L_{G}, L_{S}, and C_1 [70].

2.1.3.2 Power amplifier

Power amplifiers are a basic element in the transmission chain of RF front-ends (see Fig. 2.7 for a simple class-A PA). They are required to amplify signals with sufficient linearity and particularly in the case of mobile devices they have to work with high efficiency. A FoM describing the performance of PAs is [71]:

$$FoM_{\mathrm{PA}} = P_{\mathrm{out}} \cdot G \cdot PAE \cdot f^2 \ . \tag{2.7}$$

Here, P_{out} is the RF output power and G is the gain. The power-added efficiency is defined as $PAE = 100 \cdot (P_{\mathrm{out}} - P_{\mathrm{in}})/P$, where P_{in} is the PA's RF input power and P is the DC power consumption. The signal frequency f is squared to compensate the high-frequency gain roll-off. The linearity is also an important PA property, as it determines

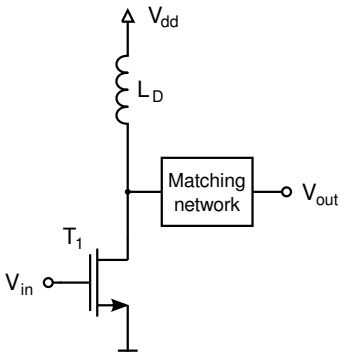

FIGURE 2.7: Power amplifier circuit schematic [72]. This class-A PA stage is simple and linear, but does not perform well in terms of efficiency.

the distortions caused in adjacent frequency bands. However, linearity strongly depends on the amplifier operation class. For the sake of a design-approach-independent FoM it is therefore omitted in Eq. (2.7).

2.1.3.3 Voltage-controlled oscillator

Voltage-controlled oscillators (VCO) are a type of oscillator that permits to tune the oscillation frequency electronically over a certain range. An example for the use of such circuits in RF transceivers are phase-locked loops, which generate a high-frequency local oscillator (LO) signal from a highly stable quartz frequency source that oscillates at lower frequency. Two main design goals for VCOs are to minimize phase noise and power consumption. A suitable performance FoM is [71]:

$$FoM_{\mathrm{VCO}} = \left(\frac{f_0}{\Delta f}\right)^2 \frac{1}{\mathrm{L}\{\Delta f\} \cdot P} \ . \tag{2.8}$$

Here, f_0 is the oscillation frequency. $\mathrm{L}\{\Delta f\}$ is the phase noise power spectral density at a distance Δf from f_0. P is the DC power consumption. This FoM neglects the frequency tuning range, which depends on the respective applications.

Fig. 2.8 shows the circuit schematic of a typical VCO.

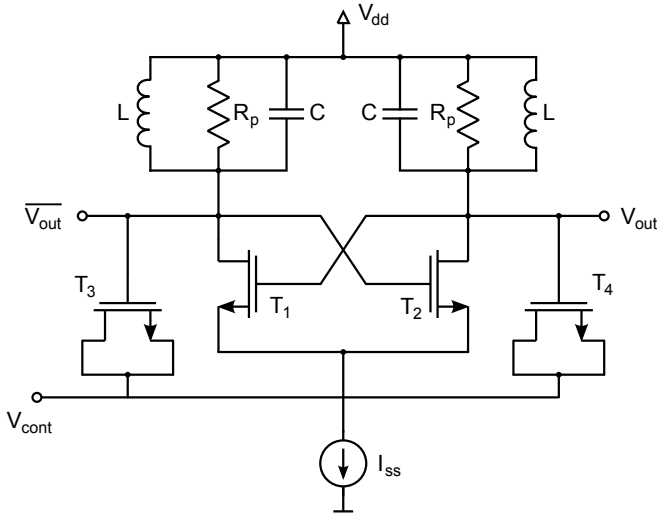

FIGURE 2.8: Voltage-controlled oscillator circuit schematic. The oscillator is realized as a cross-coupled differential pair ($\mathrm{T}_1, \mathrm{T}_2$) with an LC-tank resonator (L, C, and ohmic losses $\mathrm{R_p}$). The frequency range is varied with two metal-oxide-semiconductor (MOS) varactors T_3 and T_4 [72].

2.1.3.4 Mixer

Mixers such as the example given in Fig. 2.9 are analog multipliers that are used to perform frequency translation. The center frequency of the input signal f_{RF} and the local oscillator (LO) frequency f_{LO} yield two output signals with their spectral components centered around $f_{\mathrm{RF}} + f_{\mathrm{LO}}$ and $f_{\mathrm{RF}} - f_{\mathrm{LO}}$. By selecting one of these two output bands by means of a subsequent filter, signal up- or downconversion can be achieved. Mixers should ideally have high gain, low noise, and low power consumption. A performance measure for mixers is (following [73]):

$$FoM_{\mathrm{Mixer}} = \frac{G \cdot IIP_3}{F \cdot P} \ . \tag{2.9}$$

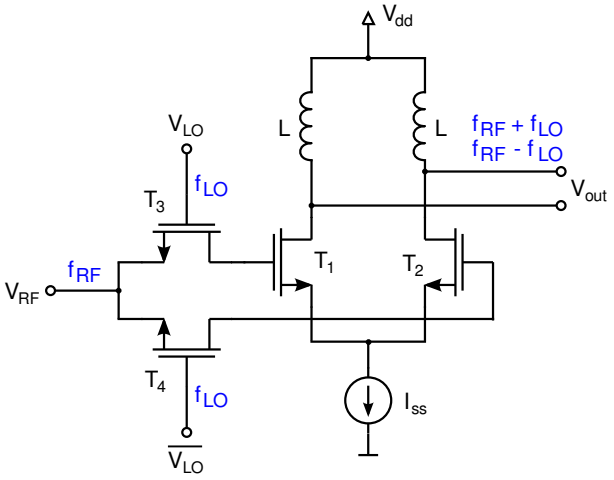

FIGURE 2.9: Mixer circuit schematic. Passive mixer ($\mathrm{T}_3, \mathrm{T}_4$) followed by gain stage ($\mathrm{T}_1, \mathrm{T}_2$) [72]. f_{RF} is the center frequency of the input signal and f_{LO} is the LO frequency. The mixer creates the two output components $f_{\mathrm{RF}} \pm f_{\mathrm{LO}}$.

2.1.4 Transceiver architectures

The term "transceiver" is a portmanteau combining the words transmitter and receiver. RF front-ends, the main high-level building block of RF electronics, usually combine these two elements by means of a duplexer to connect them to a single antenna (see Fig. 2.1). In the following, the basic architectures of RF receiver and transmitter chains are reviewed and classified with respect to their frequency conversion and modulation schemes.

It can be distinguished between two basic receiver classes with distinct frequency conversion schemes [67]. The homodyne receiver [Fig. 2.10.(a)], also referred to as direct-conversion or zero intermediate frequency (IF) architecture, is an architecture with a low complexity and a small number of circuit blocks. From the signal spectrum entering the antenna, a specific signal band around a carrier frequency f_{RF} is selected with bandpass filters and preamplified with an LNA, before the spectrum is directly downconverted to the baseband by mixing it with a LO signal with a frequency of $f_{\mathrm{LO}} = f_{\mathrm{RF}}$. An unwanted image of the spectrum of interest at $2f_{\mathrm{RF}}$ is removed by a final low-pass filter, before the signal is forwarded to the subsequent analog-digital converter (ADC) and digital processing stages. This homodyne architecture has the drawback of a possible DC offset at the mixer output due to LO leakthrough to the RF input of the mixer. Furthermore, a high f_{LO} is required. By contrast, the heterodyne receiver [Fig. 2.10.(b)] initially converts the RF signal to a much lower intermediate frequency $f_{\mathrm{IF}} \ll f_{\mathrm{RF}}$, which can more easily be processed than the RF signal, and then provides the baseband signal after a second downconversion step. This second architecture offers a higher channel selectivity, its LO frequency can be lower, it has less stringent requirements on the quality factor of the channel select filter, and it avoids the DC offset problem inherent to the zero-IF architecture. However, these advantages come at the price of an increased complexity and the need to suppress an image caused by the unwanted downconversion of the spectral components located at $2f_{\mathrm{IF}}$ distance from f_{RF}.

A second characteristic of RF receiver chains is their modulation scheme [67]. While amplitude modulation is simple, its spectral efficiency is low. In comparison, phase-modulated schemes require quadrature mixers such as depicted in Fig. 2.10.(b), but offer higher data rates. Such double mixers are fed by an in-phase LO signal I and a second LO signal Q which is shifted by 90°. Today this quadrature approach is widely used in transceivers.

RF transmitter architectures are similar to the receiver architectures, but perform their operations in reversed order [67]. As an example, Fig. 2.11 shows a homodyne transmitter converting a quadrature baseband signal directly to the RF frequency band. A power amplifier provides the required output power and a subsequent band select filter suppresses possible out-of-band spurious signals caused by the PA's nonlinearity, before the amplified signal is fed to the antenna.

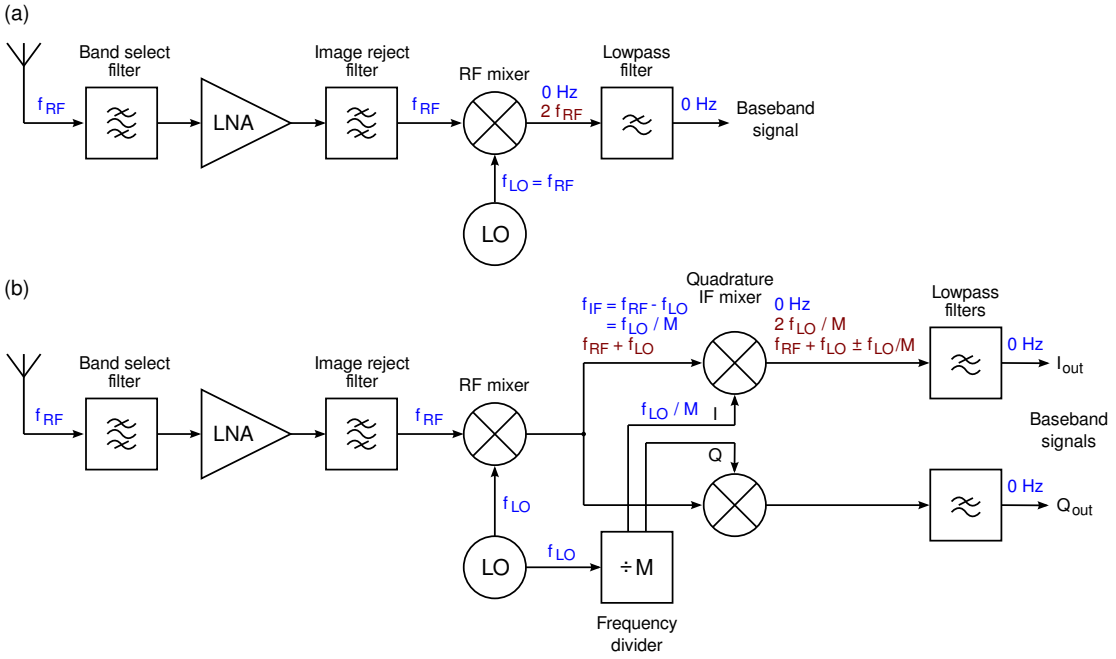

FIGURE 2.10: (a) Homodyne RF receiver architecture. (b) Heterodyne RF receiver architecture with quadrature IF mixer. Wanted and unwanted spectral components are indicated in blue and red, respectively.

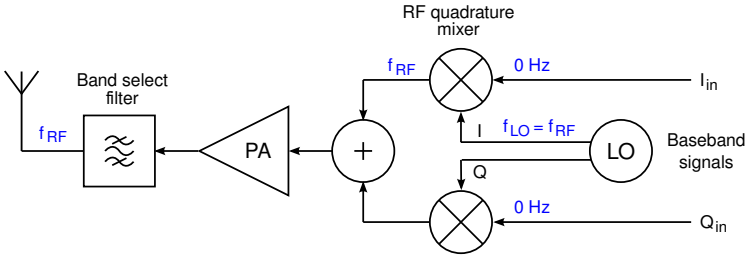

FIGURE 2.11: Homodyne RF transmitter with a quadrature baseband signal.

2.2 Carbon-based electronics

Carbon nanotubes and graphene have sparked significant interest in the scientific community due to their excellent electrical, thermal, and mechanical properties. Only after several years of development, today's CNFETs and GFETs already show remarkable RF performance. Indeed, they have reached the speed of Si-CMOS at equal gate length and approach the fastest III-V devices. Moreover, first proofs-of-concept of carbon-based digital and RF circuits have been reported. The demonstrated prototype devices and circuits are however still far away from their predicted THz-performance. Major manufacturing challenges have to be addressed before being able to exploit the full potential of these technologies and to establish them in high-performance electronics.

2.2.1 Basic physical properties of graphene and carbon nanotubes

Graphene and CNTs show unique bandgap characteristics (Table 2.1). Large-area single-layer graphene is a zero-bandgap semimetal leading to devices with particular new characteristics. A regularly cited possibility to open a gap in graphene for more conventional device behavior is to form narrow graphene nanoribbons to exploit quantum confinement effects [14, 15]. CNTs, the second material for carbon-based electronics, can be semiconducting or metallic depending on their geometry. The bandgap of semiconducting CNTs is indirectly proportional to their tube diameter.

One of the most promising electrical properties of carbon semiconductors is their exceptional carrier mobility μ (Table 2.1). The highest room-temperature mobilities that have been experimentally demonstrated for graphene and CNTs are as high as $200\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [48] and $100\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [76], respectively. These excellent values significantly outperform even the fastest III-V semiconductor InSb, for which an electron mobility of $77\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [79] has been quoted. Furthermore, due to band symmetry it is expected that carbon-based materials have similar electron and hole mobilities μ_e and μ_h, while most conventional semiconductors perform significantly worse in the hole conduction regime. For instance, the $\mu_\mathrm{h}/\mu_\mathrm{e}$ ratio of InSb is 0.014 and of GaAs it is 0.037 [78, 79]. This favorable picture in terms of carrier mobility loses some of its shine when considering that high μ comes at the price of a low bandgap [69]. Large-area graphene, for which excellent mobilities have been reported, has no gap. In contrast,

TABLE 2.1: Electrical properties of graphene and carbon nanotubes and comparison to conventional semiconductors.[1]

Material	Carrier mobility[2,3] μ ($\mathrm{cm^2\,V^{-1}\,s^{-1}}$)	Saturation velocity v_{sat} ($\mathrm{m\,s^{-1}}$)	Bandgap E_{g} (eV)
Graphene[4]	200000	$\approx 6 \times 10^5$	0
CNT	100000	$\approx 5 \times 10^5$	≥ 0
Si	1350 (480)	1.0×10^5	1.11
Ge	3600 (1800)	0.7×10^5	0.66
GaAs	8000 (300)	1.2×10^5	1.43
InSb	77000 (1100)	4.0×10^5	0.17

[1] References: graphene: μ [48], v_{sat} [74], E_{g} [75]; CNT: μ [76], v_{sat} [77], E_{g} [75]; conventional semiconductors: μ [78, 79], v_{sat} [79, 80], E_{g} [78]

[2] Room-temperature conditions apply

[3] Electron and (hole) mobilities given for conventional semiconductors

[4] Large-area graphene, without a quantum-confinement bandgap

TABLE 2.2: Thermal and mechanical properties of graphene and carbon nanotubes and comparison to conventional materials.[1]

Material	Thermal conductivity k_{thermal} ($\mathrm{W\,m^{-1}\,K^{-1}}$)	Young's modulus E_{Young} (TPa)	Tensile strength σ_{ts} (GPa)
Graphene	3000-5000	1.02	130
CNT	3500	1.47	150
Diamond	2320	1.21	60
Electrolytic Cu	390	0.12	0.30
Steel type 304	15	0.195	0.55

[1] References: graphene: k_{thermal} [49], E_{Young} [50], σ_{ts} [50]; CNT: k_{thermal} [38], E_{Young} [81], σ_{ts} [39]; conventional materials: k_{thermal} [82], E_{Young} [82, 83], σ_{ts} [82, 83]

graphene nanoribbons as well as CNTs show μ values that are indirectly proportional to their bandgap.

In strongly downscaled channels μ looses part of its relevance, as under high-field transport in short-channel devices the carrier velocity is strongly determined by the saturation velocity v_{sat} (Table 2.1). For graphene and CNTs v_{sat} is predicted to be in the range of 5 to $6 \times 10^5\,\mathrm{m\,s^{-1}}$ [74,77] and is therefore about five times higher than the v_{sat} of Si [79] and even surpasses the $4 \times 10^5\,\mathrm{m\,s^{-1}}$ of InSb [80].

Graphene and CNTs do not only have unique electrical characteristics, but stand also out due to their thermal and mechanical properties (Table 2.2). With a thermal conductivity k_{thermal} of around 3000 to $5000\,\mathrm{W\,m^{-1}\,K^{-1}}$ [38,49] they are better heat conductors than diamond ($2320\,\mathrm{W\,m^{-1}\,K^{-1}}$) or Cu ($390\,\mathrm{W\,m^{-1}\,K^{-1}}$) [82]. Measurements of the Young's modulus E_{Young} have revealed that both graphene and CNTs are approximately as rigid as diamond [50,81,83]. Furthermore, experimentally determined tensile strengths σ_{ts} for graphene and CNTs are 130 GPa [50] and 150 GPa [39], respectively, which more than duplicates the highest value of 60 GPa reported for diamonds [83].

2.2.2 Radio frequency carbon-nanotube field-effect transistors

RF-CNFETs are commonly realized as planar devices and have a structure similar to conventional Si-based MOSFETs (see Fig. 2.12). A well-performing channel material for CNFETs consists of a highly aligned single-walled CNT array [84]. Such arrays can be grown by CVD [85] or disposed from a CNT solution and oriented by dielectrophoresis [86]. Compared to single-tube channels, arrays allow higher current density and transconductance per unit width and reduce the impact of external parasitic elements.

The fraction of metallic CNTs (mCNT) in the channel array is a crucial factor for device performance, as mCNTs constitute a parasitic resistance in parallel to the useful semiconducting channel. Several methods have been developed to achieve a low amount of mCNTs in tube arrays. Among them are the preferential growth of semiconducting CNTs (sCNT) [87], the removal of mCNTs by selective etching [88] or electrical burning [89], and previous sorting before the deposition of a purified sCNT solution [90].

In addition to avoiding metallic shorts, further manufacturing challenges are synthesizing sCNTs with a better defined bandgap energy, increasing the tube array density to achieve

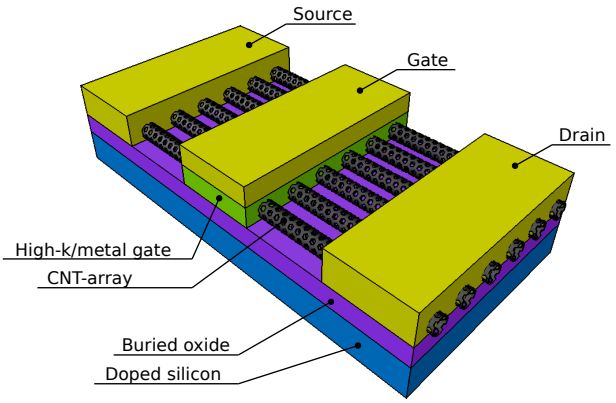

FIGURE 2.12: CNFET geometry.

higher performance, controlled doping, forming lower contact resistances, as well as depositing defect-free high-κ gate dielectrics [5]. The lack of control over these parameter causes large manufacturing process variations.

2.2.2.1 CNFET performance

Fig. 2.13 illustrates that during the last one and a half decades CNT-based technologies have evolved quickly from first experimental transistors to today's impressively fast prototypes. The CNFET device which at the time of writing this thesis holded the record in RF performance was reported in the year 2012 and is based on an array of aligned CNTs disposed from an aqueous solution [42]. After deembedding, the device shows an intrinsic cut-off frequency f_T of 153 GHz and an intrinsic maximum oscillation frequency f_max of 30 GHz. A comparable CNFET manufactured in 2009 and based on a random network of single-walled semiconducting CNTs has an intrinsic f_T of 80 GHz [91]. Fig. 2.14 compares the f_T performance of these CNFETs to competing technologies.

Although CNFETs are handled as excellent RF devices, high parasitic capacitances and contact resistances still severely deteriorate their RF performance. For instance, the device reported in Ref. [42] has an extrinsic f_T and f_max of only 7 GHz and 15 GHz, respectively. Today's experimental results are therefore still in strong contrast with performance projections, which, although considering device nonidealities, predict THz-potential both for f_T and f_max [92–94]. The ultimate limit for the CNFET's f_T-performance has been stated as $f_\mathrm{T,ultimate} = 140\,\mathrm{GHz}\,\mu\mathrm{m}/L_\mathrm{g}$ [95], with L_g as the gate length. Reusing the 100 nm-CNFET reported in [42] as an example shows that this device's intrinsic and extrinsic f_T reach 10.9% and 0.5% of $f_\mathrm{T,ultimate}$, respectively.

Not only high speed, but also current saturation is a crucial requisite for analog technologies. It is amongst others required to obtain high gain and near-ideal current sources. With a tight electrostatic control over the one-dimensional tubes, CNFETs have shown to be scalable down to 9 nm without a significant increase of short channel effects and therefore promise current saturation even for highly scaled devices [97, 98].

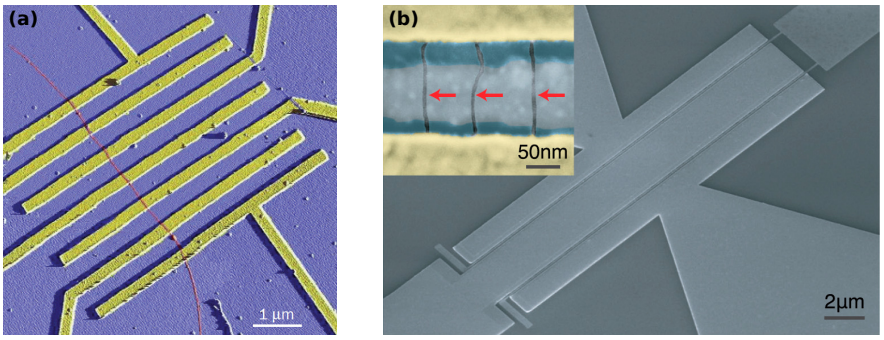

FIGURE 2.13: Evolution of CNFET manufacturing capabilities: (a) Atomic force microscope image of an early CNFET (reported 2000 in [96]). A CNT (red line) is fixed onto several electrodes to measure its conductance. The doped substrate acts as a backgate to vary the charge density of the CNT. (b) Scanning electron microscope image of a recent RF-CNFET with $f_T = 153\,\text{GHz}$ (reported 2012 in [42]). The device channel consists of an array of sCNTs (see inset).

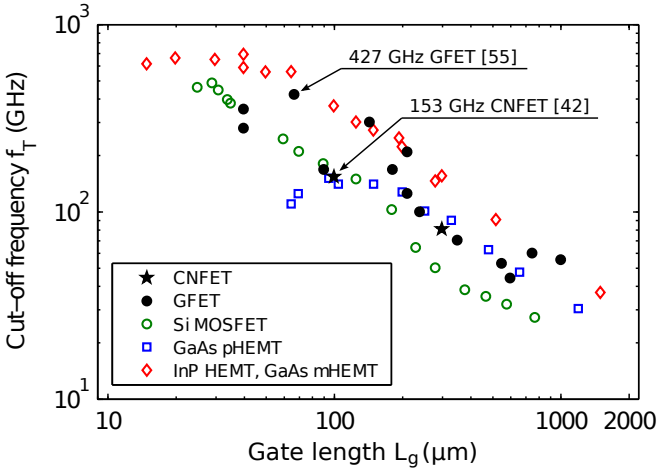

FIGURE 2.14: State-of-the-art of carbon-based RF devices: cut-off frequency f_T vs. gate length L_g for CNFETs and GFETs and comparison to Si- and III-V-technologies (data from a review given in [69]). The best-performing CNFET [42] and GFET [55] have an intrinsic f_T of 153 GHz and 427 GHz, respectively.

2.2.3 Radio frequency graphene field-effect transistors

RF-GFETs are, like RF-CNFETs, manufactured as planar devices (see Fig. 2.15). The graphene channel for GFET prototypes is currently provided in several ways [69]: mechanical exfoliation of graphene flakes from graphite [99], CVD on a metal wafer and transfer to the substrate [100] or epitaxial growth on SiC [101]. The latter two methods are compatible to industrial-scale manufacturing, but with a charge carrier mobility of up to about $10\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [53] they still do not yield the same outstanding mobilities as mechanical exfoliation.

The lack of a bandgap in graphene is a serious issue for digital applications, for which an on/off ratio of at least 10^6 is required [53]. Graphene nanoribbon FETs may be an alternative to overcome this limitation [102], but narrow graphene nanoribbons with a high band gap lack high carrier mobility [69]. RF devices, however, are not as much affected by this restriction as their digital counterparts, as they are not necessarily required to be switched off.

Current manufacturing challenges include controlling the number of grown graphene layers and increasing the crystallite size. Furthermore, the graphene-metal contact resistance has to be better understood and reduced, and defect-free high-κ dielectrics have to be deposited on the inert graphene surface.

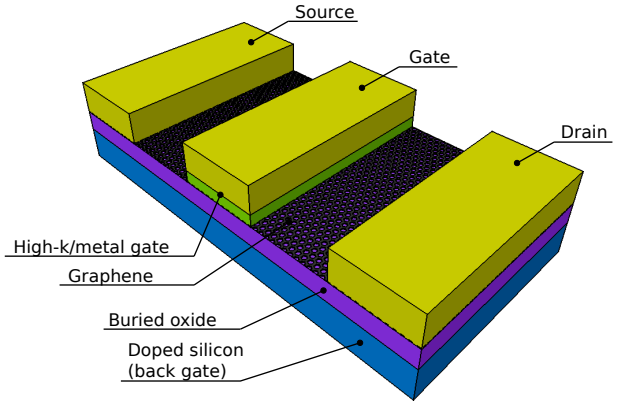

FIGURE 2.15: GFET geometry.

2.2.3.1 GFET performance

Fig. 2.16 illustrates the fast technology evolution from experimental devices focusing on graphene's DC characteristics to today's RF devices. A comparison of the f_T performance of such RF-GFETs to alternative technologies (Fig. 2.14) reveals that they already surpass Si-MOSFETs with equal L_g and that they are even able to compete with InP high-electron-mobility transistors (HEMT) and metamorphic GaAs HEMTs. The up to date best-performing RF-GFETs date back to the year 2012, when Refs. [55] and [104] reported remarkable f_T and f_{max} values of 427 GHz and 44 GHz, respectively. However, these values confirm the trend that the f_{max} of GFETs lags about one decade behind their f_T, which can be attributed to high parasitic gate resistances and to insufficient current saturation [69].

RF-GFETs are predicted to provide THz-performance. However, the GFET has a performance disadvantage in comparison to the CNFET amongst others due to a higher intrinsic gate capacitance. In a case study reported in [92] the maximum intrinsic f_T and f_{max} of GFETs were about 30% and 60% lower than the ones of CNFETs.

Due to the band structure of graphene, current saturation in large-area GFETs is difficult to achieve. Although a prototype showing saturation has early been reported [105], the GFET biasing region where saturation occurs is still very limited. The insufficient quality of saturation in GFETs results in high output conductance, low gain, and the low f_{max} reported for experimental devices.

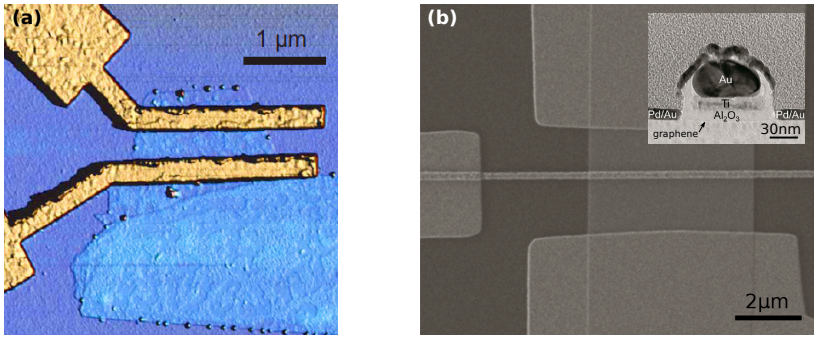

FIGURE 2.16: Evolution of GFET manufacturing capabilities: (a) Atomic force microscope image of an early GFET (reported 2007 in [103]). A graphene flake is transferred to an oxidized substrate and connected by electrodes. The subjacent doped substrate is used as a back-gate. (b) Scanning electron microscope image of a recent RF-GFET with $f_T = 427$ GHz (reported 2012 in [55]). The used process provides self-aligned gates (see inset).

2.2.4 Carbon-based circuits

The research on carbon-based electronics is more and more extended from the device to the circuit level. This section discusses milestone analog and digital circuits based on CNFETs and GFETs which were developed during the last years (Fig. 2.17), in order to illustrate the possibilities of current manufacturing processes. However, although advancements on carbon-based circuits have been made, the required maturity for market-insertion of RF applications will not be reached until the next decade [53].

2.2.4.1 Carbon nanotube-based circuits

Early experimental demonstrations of CNFET circuits were made using single CNTs. In 2006, a 52 MHz-ring oscillator designed out of five CMOS inverter stages aligned on one CNT was reported [106]. A year later, the nonlinear current-voltage characteristics of a single CNT were exploited to demodulate an audio signal that was amplitude-modulated on a carrier frequency of 1 GHz [107]. In 2008, progress in the analog and digital domain was demonstrated with a 500 MHz-ring oscillator using a CNT-array CNFET [108] as well as a 4-bit row decoder made of 88 transistors on flexible substrate and clocked at 1 kHz [109].

More recently, over 10000 CNFETs were manufactured on a single chip using a conventional semiconductor fabrication line [110]. The devices were realized using arrays of individually positioned carbon nanotubes. Then, in 2013 the up to date most complex CNFET circuit was presented [13]. Shulaker *et al.* developed a CNT computer based on highly aligned CNT arrays with more than 99.99 % sCNT obtained by electrical breakdown. The circuit runs an operating system capable of multitasking, supports 20 different instructions, and is operated at a clock frequency of 1 kHz.

2.2.4.2 Graphene-based circuits

Among the first reported GFET circuits were basic analog building blocks such as frequency multipliers and amplifiers, which were built around individual transistors [111–113]. A breakthrough in the wafer-scale integration of graphene circuits has been made in the year 2011 with the integration of GFET mixers using metal inductances

[114]. A further wafer-scale circuit demonstration has been made with a 1.28 GHz-ring oscillator in 2013 [115]. Recently, in January 2014, a radio frequency receiver performing signal amplification has been presented [116]. It is the most complex integrated graphene circuit up to now. Three GFETs as well as capacitors and inductors have been integrated to perform signal amplification, filtering and downconversion with the purpose of receiving digital data modulated on a 4.3 GHz-carrier. The circuit occupies an area of 0.6 mm^2 and has been fabricated with a Si-CMOS-compatible technology on 200 mm-wafers.

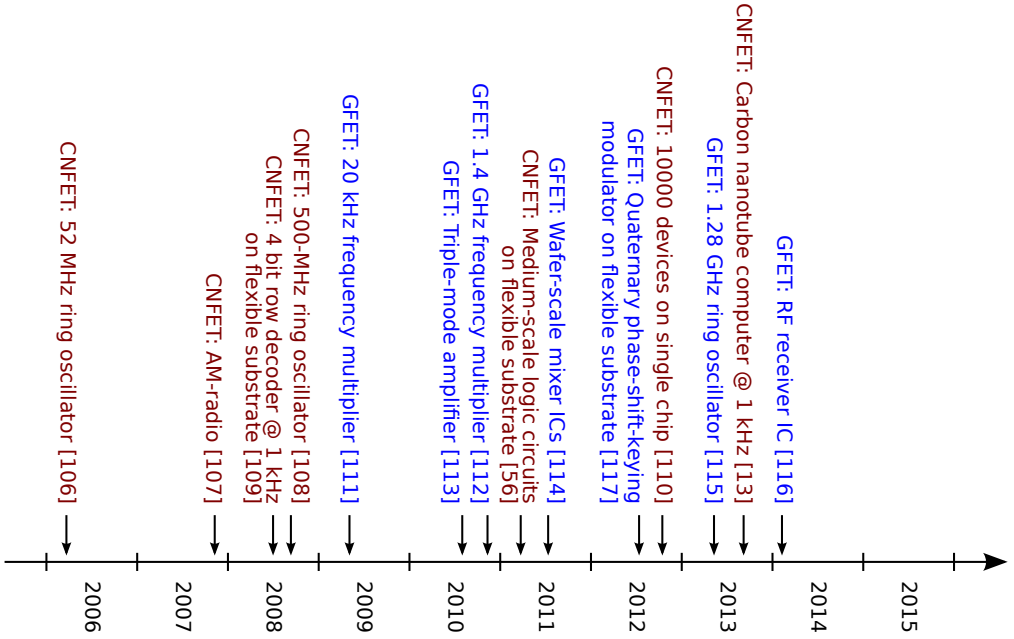

FIGURE 2.17: Timeline of milestone CNFET and GFET circuits [13, 56, 106–117].

2.3 Electronic band structure of graphene and carbon nanotubes

The electronic band structure is a central concept of solid-state physics. It describes the electronic behavior of a material by determining the allowed and forbidden energy states of its electrons and holes. The band structure is an indispensable tool to understand the physical properties of a material (for instance, the occurrence of semiconducting and metallic CNTs) and to gain insight into device physics. This section's discussion of the band models of graphene and CNTs highlights concepts that will be frequently used in the following parts of this thesis that treat device modeling.

2.3.1 Band structure of graphene

The first investigations on the energy dispersion relation of graphene date back to the year 1947 [118] and were made with the purpose to study the properties of graphite. Several decades later, the possibility to manufacture CNTs renewed the scientific community's interest on graphene's electronical properties, as they serve as a starting point to derive the band structure of CNTs. Since then, the band structures of graphene and CNTs have been widely discussed in literature [119–124] and have found their way into textbooks [75]. The following description of graphene's and the CNT's energy dispersion relations (Secs. 2.3.1 and 2.3.2) is based on the excellent review given in [75].

2.3.1.1 Direct and indirect lattice

Graphene is a two-dimensional sheet made of carbon atoms arranged in a honeycomb lattice. Each carbon atom forms strong σ-bonds with it's three neighbouring atoms by sharing three of its valence electrons with them through orbital hybridization. A fourth valence electron is not localized in the graphene plane as the three other ones, but perpendicular to it. This π-bond electron is only weakly bound to the nucleus and the primary responsible for the electrical properties of graphene.

A fundamental crystallographic description of the arrangement of graphene's carbon atoms in space can be made by means of a Bravais lattice and a basis [78]. In such Bravais lattice every lattice point is identically surrounded by neighbouring points. The

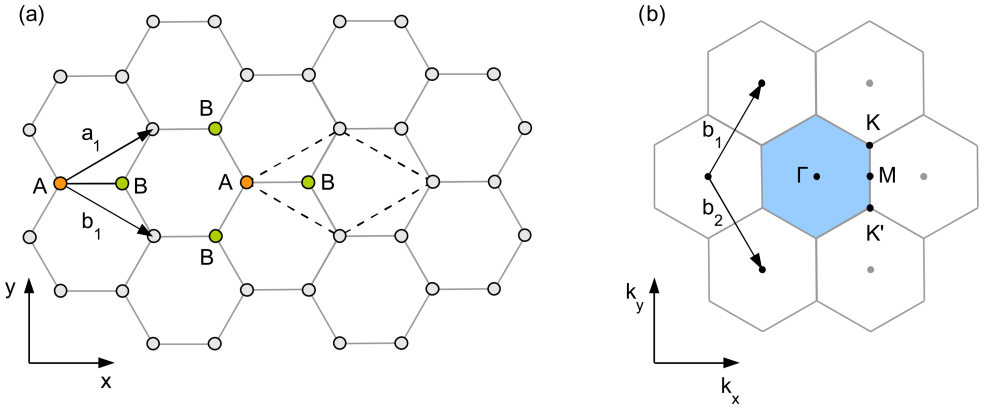

FIGURE 2.18: (a) The direct lattice of graphene shows the arrangement of the carbon atoms in space. The Bravais lattice is rhomboidal (dashed lines) and described by the primitive vectors $\boldsymbol{a}_1$ and $\boldsymbol{a}_2$. A pair of atoms at positions A and B forms the basis of the direct graphene lattice. (b) The reciprocal lattice is described by the vectors $\boldsymbol{b}_1$ and $\boldsymbol{b}_2$. The Brillouin zone of graphene is marked blue. Γ, K, and M are points of high symmetry.

honeycomb lattice itself does not qualify as a Bravais lattice, as can be verified in Fig. 2.18.(a): for instance, the right neighbours of atoms labelled A are not the same as the ones of the B atoms. However, honeycomb lattices can be seen as a rhomboidal Bravais lattice with a combination of an A and a B atom at each lattice point. These two atoms form the so-called basis of the lattice.

Graphene's Bravais lattice is described by two primitive vectors $\boldsymbol{a}_1$ and $\boldsymbol{a}_2$, whose length depends on the lattice constant $a = 2.46\,\text{Å}$.

$$\boldsymbol{a}_1 = \left(\frac{\sqrt{3}a}{2},\ \frac{a}{2}\right);\quad \boldsymbol{a}_2 = \left(\frac{\sqrt{3}a}{2},\ -\frac{a}{2}\right) \tag{2.10}$$

The reciprocal graphene lattice is obtained by the discrete Fourier transform of the above mentioned direct graphene lattice and is a description of the crystal structure in reciprocal space, also referred to as k-space, where k stands for the wave vector. The reciprocal lattice of graphene is a honeycomb lattice similar to the direct lattice, but rotated by 90° as shown in Fig. 2.18.(b). The primitive vectors of the reciprocal lattice $\boldsymbol{b}_1$ and $\boldsymbol{b}_2$ are given as:

$$\boldsymbol{b}_1 = \left(\frac{2\pi}{\sqrt{3}a},\ \frac{2\pi}{a}\right);\quad \boldsymbol{b}_2 = \left(\frac{2\pi}{\sqrt{3}a},\ -\frac{2\pi}{a}\right)\ . \tag{2.11}$$

Fig. 2.18.(b) illustrates the hexagonal first Brillouin zone of graphene. Due to symmetry, knowing the energy dispersion relation in this zone is sufficient to describe the relation in the whole k-space.

2.3.1.2 Nearest-neighbour tight-binding energy dispersion

Solving the time-independent Schrödinger equation

$$-\frac{\hbar^2}{2m_0}\nabla^2\Psi\left(\mathbf{r}\right)+U_c\left(\mathbf{r}\right)\Psi\left(\mathbf{r}\right)=E\Psi\left(\mathbf{r}\right) \tag{2.12}$$

for a given system leads to its allowed energy states. The wave function $\Psi\left(\mathbf{r}\right)$ is describing the electron cloud at position $\mathbf{r}$. m_0 is the electron rest mass and $U_c\left(\mathbf{r}\right)$ stands for the graphene crystal potential stemming from the attractive force of the positively charged carbon nuclei. The allowed energy states of the system are described by E. ∇^2 is the Laplace operator.

Some assumptions are made to achieve a closed form solution for the graphene problem. Electrons are assumed as tightly bound to the nuclei and electron wavefunctions only overlap with the ones of the three nearest neighbour atoms, giving this approach the name nearest-neighbour tight-binding (NNTB) approximation. After an extended derivation, the Schrödinger equation yields graphene's energy dispersion relation

$$E\left(\boldsymbol{k}\right)^{\pm}=\pm\gamma\sqrt{1+4\cos\left(\frac{\sqrt{3}a}{2}k_{\mathrm{x}}\right)\cos\left(\frac{a}{2}k_{\mathrm{y}}\right)+4\cos^2\left(\frac{a}{2}k_{\mathrm{y}}\right)}\quad, \tag{2.13}$$

where the nearest-neighbour overlap energy $\gamma\approx 3.1\,\mathrm{eV}$ is a fitting parameter.

The conductance band and valence band obtained with the NNTB approximation are shown in Fig. 2.19. They touch at zero energy at the 6 distinctive K- or Dirac-points, which implies that graphene is a zero-bandgap semiconductor. Graphene's energy relation is of a highly symmetric nature, resulting in similar electron and hole properties.

Conventional semiconductors have an approximately parabolic dispersion, so in a defect-free lattice their electrons behave like free electrons with reduced electron mass. By

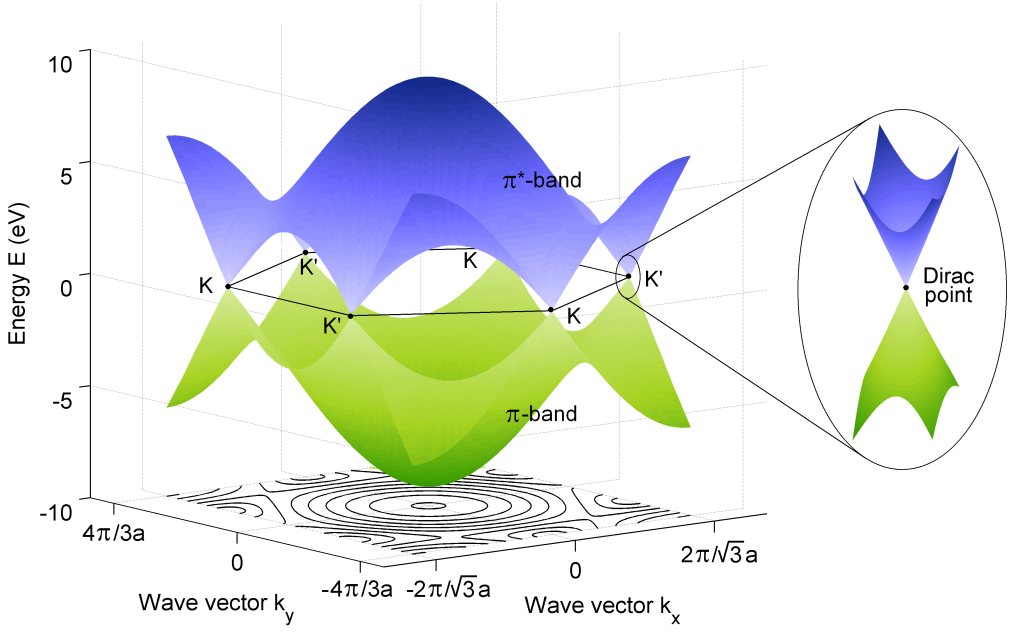

FIGURE 2.19: Graphene NNTB energy dispersion relation $E(\boldsymbol{k})$. Conductance and valence bands are indicated as π^*- and π-bands, respectively. The K- or Dirac points mark the boundary of the hexagonal first Brillouin zone. The inset shows a Dirac cone that illustrates the linear energy dispersion relation in the vicinity of the Dirac points.

contrary, graphene's energy dispersion in the vicinity of the Dirac points is approximately linear (see inset Fig. 2.19):

$$E(\boldsymbol{k})^{\pm}_{\text{linear}} = \pm\hbar v_{\text{F}} |\boldsymbol{k}| \ , \tag{2.14}$$

where $\hbar$ is the reduced Planck constant and v_{F} the Fermi velocity.

In consequence, graphene's electrons at low energy ($E \ll \gamma$) can be described as massless Dirac fermions, that is, as relativistic particles with zero rest mass which move at an effective "speed of light" of $v_{\text{F}} \approx 1 \times 10^6\,\text{m}\,\text{s}^{-1}$. For that reason graphene exhibits exotic quantum electrodynamics phenomena such as the anomalous integer quantum hall effect occurring at half-integer filling factors [125] or Klein tunneling allowing the unimpeded penetration of particles through high and wide potential barriers [126].

For completeness, graphene's density of states (DOS), derivable from the energy dispersion relation, is given as:

$$D\left(E\right) = \frac{2}{\pi}\left|k\frac{\mathrm{d}k}{\mathrm{d}E}\right| = \frac{2}{\pi\left(\hbar v_F\right)^2}\left|E\right| \ . \tag{2.15}$$

It vanishes at zero Fermi energy, making graphene a material that combines the zero-bandgap property of metals and the zero-DOS property of semiconductors.

Finally, it should be reminded that the NNTB method is based on approximations. These are not required for *ab initio* calculations. With a significantly higher computational effort and without closed-form solutions, *ab initio* calculations give more exact results and lead to slightly different forms of the conduction and valence band at high energies [122]. However, for most electronic applications the error of the NNTB results is negligible [75].

This section's band structure discussion is only valid for single-layer graphene. Stacking several layers to bi- or multilayer graphene alters the energy dispersion relation [127]. For instance, bilayer graphene has a parabolic-like and not a linear low-energy dispersion relation.

2.3.2 Band structure of carbon nanotubes

2.3.2.1 Chirality

A CNT can be imagined as a ribbon of graphene cut out of a graphene sheet and rolled into a tube (see Figs. 2.20 and 2.21). Depending on the cutting direction and the width of the ribbon, one obtains CNTs with different lattice orientations and diameters. The concept of chirality is used to describe this physical form of the CNTs. Possible configurations are i) achiral CNTs, which exist in the two flavours zigzag-CNT and armchair-CNT, and ii) chiral CNTs, which represent all other possible tube configurations. The chiral vector $\boldsymbol{C}_\mathrm{h}$ exactly defines the geometry of a CNT. As illustrated in Fig. 2.20, it represents the linear combination $\boldsymbol{C}_\mathrm{h} = n_1 \cdot \boldsymbol{a}_1 + n_2 \cdot \boldsymbol{a}_2$ of the two primitive

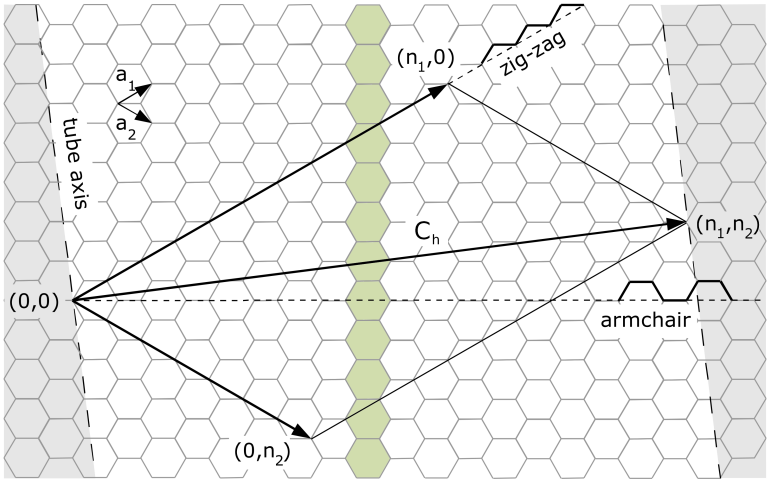

FIGURE 2.20: A CNT can be imagined as created out of a ribbon of graphene (diagram following [75]). The chirality vector $\boldsymbol{C}_\mathrm{h}$ exactly defines its geometry. $(n_1, 0)$-zigzag-, (n_1, n_1)-armchair-, or in this example a chiral $(11, 7)$-CNT may be formed.

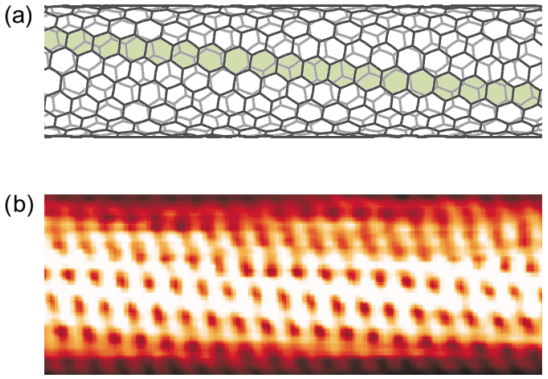

FIGURE 2.21: (a) Structure of a chiral $(11, 7)$-CNT related to the graphene ribbon depicted in Fig. 2.20 (created with CoNTub [128]). (b) Atomically resolved scanning tunneling microscopy image of an $(11, 7)$-CNT (from [129]).

lattice vectors $\boldsymbol{a}_1$ and $\boldsymbol{a}_2$. The resulting tubes are referred to as (n_1, n_2)-CNTs.[1] CNT diameters d are commonly in the range of 0.5 to 5 nm and are directly related to the tube chirality:

$$d = \frac{|\boldsymbol{C}_\mathrm{h}|}{\pi} = \frac{a \cdot \sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \ . \tag{2.16}$$

2.3.2.2 Zone-folding approximation

The energy dispersion relation of CNTs can be derived from the discussed NNTB band structure of graphene. Due to the tubular form of CNTs, quantum confinement in the circumferential tube direction occurs. As a result, the band structure of CNTs is a subset of the energy spectrum $E(\boldsymbol{k})$ of graphene:

$$E\left(\boldsymbol{k}_\parallel + \boldsymbol{k}_\perp\right) \subset E\left(\boldsymbol{k}\right) \ , \tag{2.17}$$

where $\boldsymbol{k}_\parallel$ is a continuous wave vector describing the electron movement along the tube axis and $\boldsymbol{k}_\perp$ is a discrete wave vector in perpendicular direction.

The quantization of $\boldsymbol{k}_\perp$ can be obtained by introducing a circumferential boundary condition, which implies periodicity of the electron wave function:

$$\Psi\left(\boldsymbol{0}\right) = \Psi\left(\boldsymbol{C}_\mathrm{h}\right) = e^{i|\boldsymbol{k}_\perp| \cdot |\boldsymbol{C}_\mathrm{h}|} \Psi\left(\boldsymbol{0}\right) \ . \tag{2.18}$$

[1] This thesis follows the (n_1, n_2) notation of Saito *et al.* [119] in order to avoid confusion with the energy substate m (see Eq. (2.19) and Sec. 4.3.1.1), while other work (*e.g.*, [75]) follows the (n, m) notation.

This condition is fulfilled for all

$$|\boldsymbol{k}_\perp| = \frac{2\pi}{|\boldsymbol{C}_\mathrm{h}|} m, \quad m = 0, 1, \ldots, N-1 \quad . \tag{2.19}$$

Here, $N = \left(2|\boldsymbol{C}_\mathrm{h}|^2\right) / \left(a^2 \gcd\left(2n_1 + n_2, 2n_2 + n_1\right)\right)$ is the number of hexagons per lattice unit cell. $\gcd(\cdot)$ stands for the greatest common divider. m is an integer number related to the energy subbands due to circumferential confinement.

It is sufficient to consider an interval of

$$|\boldsymbol{k}_\parallel| = (-1, 1) \cdot \frac{\pi}{|\boldsymbol{T}|} \ , \tag{2.20}$$

with $|\boldsymbol{T}| = \sqrt{3}|\boldsymbol{C}_\mathrm{h}| / \gcd\left(2n_1 + n_2, 2n_2 + n_1\right)$ being the length of the translational vector, in order to cover the overall first Brillouin zone of CNTs. The energy subbands of this zone can be mapped back into the first Brillouin zone of graphene (Fig. 2.22), which is why the method described in this section is named zone-folding approximation.

2.3.2.3 Semiconducting and metallic behavior

The geometry of a (n_1, n_2)-CNT is directly related to its energy dispersion relation and in particular to its bandgap. As illustrated in Figs. 2.22 and 2.23, depending on tube chirality, energy subbands may cross the zero-bandgap K-points of graphene's band structure, leading to mCNTs. Otherwise, sCNTs are obtained.

In the case of sCNTs, the bandgap E_g is indirectly proportional to the tube diameter:

$$E_g \approx 2\gamma \frac{a}{d} \approx \frac{0.9\,\mathrm{eV\,nm^{-1}}}{d} \ . \tag{2.21}$$

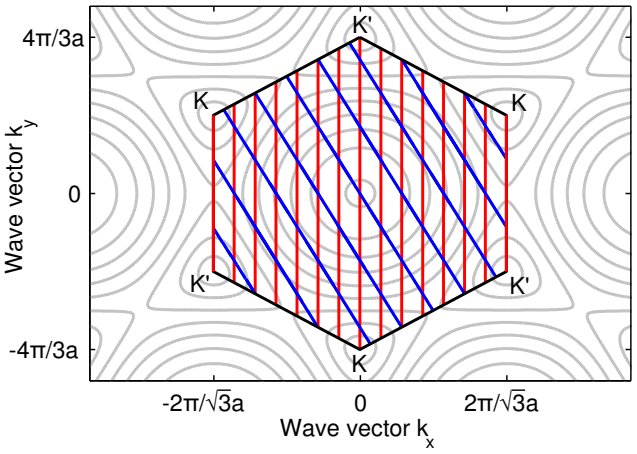

FIGURE 2.22: Zone-folding approximation: subbands of an armchair $(7,7)$-mCNT (red lines) and a zigzag $(7,0)$-sCNT (blue lines) in graphene's first Brillouin zone. The contour plot symbolizes graphene's energy dispersion relation. Several subbands of the armchair CNT cross K-points, leading to metallic behavior (diagram following [75]).

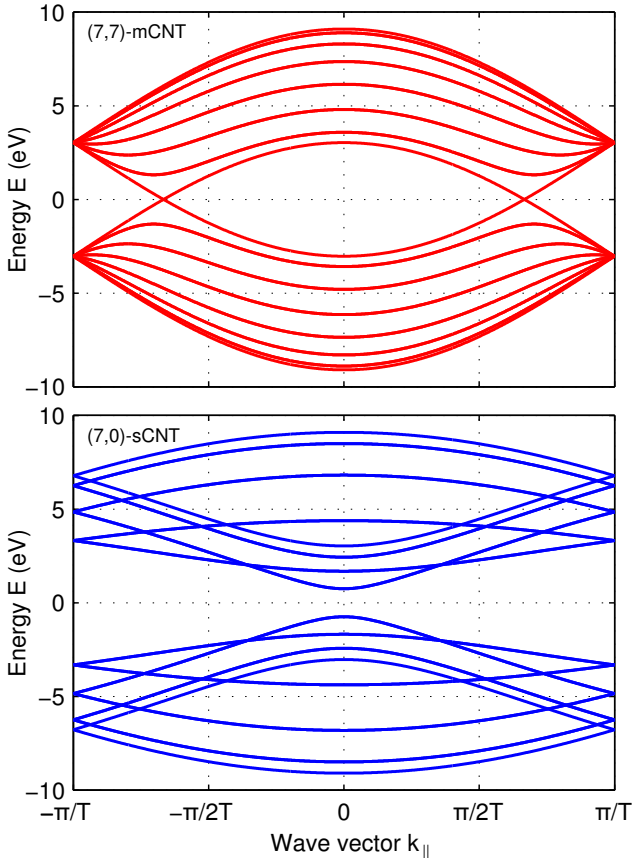

FIGURE 2.23: Band structures of a (7,7)-mCNT and a (7,0)-sCNT. The subbands can be imagined as cross-sections of graphene's energy dispersion relation.

(n_1, n_2)-CNTs fulfilling the condition

$$\mathrm{mod}\left(\frac{n_1 - n_2}{3}\right) = 0 \ , \tag{2.22}$$

where $\mathrm{mod}\,(\cdot)$ is the modulo operator, fall into the category of mCNTs and have no bandgap. This equation indicates that statistically one third of the grown CNTs are metallic, when a nonselective tube synthesis process is employed. This leads to important restrictions for the use of CNTs in microelectronics.

The zone folding approximation is most accurate for tubes with high diameters $d > 1\,\mathrm{nm}$, as it does not take into account curvature effects occurring in small nanotubes. Moreover, it underlies the same limitations as the NNTB-band structure of graphene, which is most accurate at low energies.

Chapter 3

Thesis objectives and methodology

THE DISCOVERER of carbon nanotubes, Sumio Iijima, humorously quoted Michael Faraday in a speech at the Royal Institution to illustrate the possible large impact of CNTs [75]: "One day, sir, you may tax it." Faraday gave this response 1850 to the British minister of finance when being asked for the practical value of electricity. In a similar manner, one of the discoverers of graphene, the Nobel laureate Andre Geim, stated [130]: "Graphene opened up a material world we didn't even know existed."

These two comments confirm that graphene and CNTs have the potential to significantly impact wide fields of science[1]. In this exciting context, this thesis aims to advance the state-of-the-art in the field of CNT- and graphene-based RF electronics. In particular, it gives new insights in device modeling, provides comprehensive performance projections for CNFETs, and proposes a model for accurate GFET circuit design.

This chapter is organized as follows. Sec. 3.1 defines the specific objectives of this work. In continuation, Sec. 3.2 discusses the methodology applied to achieve these objectives. Finally, Sec. 3.3 mentions the organizational framework in which this work has been elaborated.

[1]One of the two Flagship projects recently started by the European Union exclusively treats the research on graphene. One of the project's numerous work packages is dedicated to graphene-based high-frequency electronics [131].

3.1 Thesis objectives

The main objective of this thesis is

to investigate on the opportunities of using carbon-based devices for future RF integrated circuits.

This objective has been divided into several specific subtasks, which are summarized by the following points:

- **Identify promising research fields to advance the state-of-the-art of carbon-based RF electronics.**
- **Provide improved models for carbon-based devices.**
- **Provide performance projections by determining RF-FoMs of carbon-based devices and circuits.**

In the following, the methodology that was applied to achieve these goals is exposed.

3.2 Methodology

This thesis on carbon-based electronics can be split into two main parts: the work on CNT-based and the work on graphene-based technologies (see Fig. 3.1). The overall workload was distributed as approximately 2/3 for investigations on CNT electronics and 1/3 for investigations on the graphene part.

Both lines of research have in common that they have been initiated by an extensive review of the state-of-the-art of the respective device physics, compact models, device and circuit manufacturing capabilities, and possible applications. This has allowed to identify promising research fields. Notably, it has been recognized the need to improve the existing device models and extend them with additional functionality to allow more realistic and comprehensive RF performance projections and to provide circuit designers with more powerful tools.

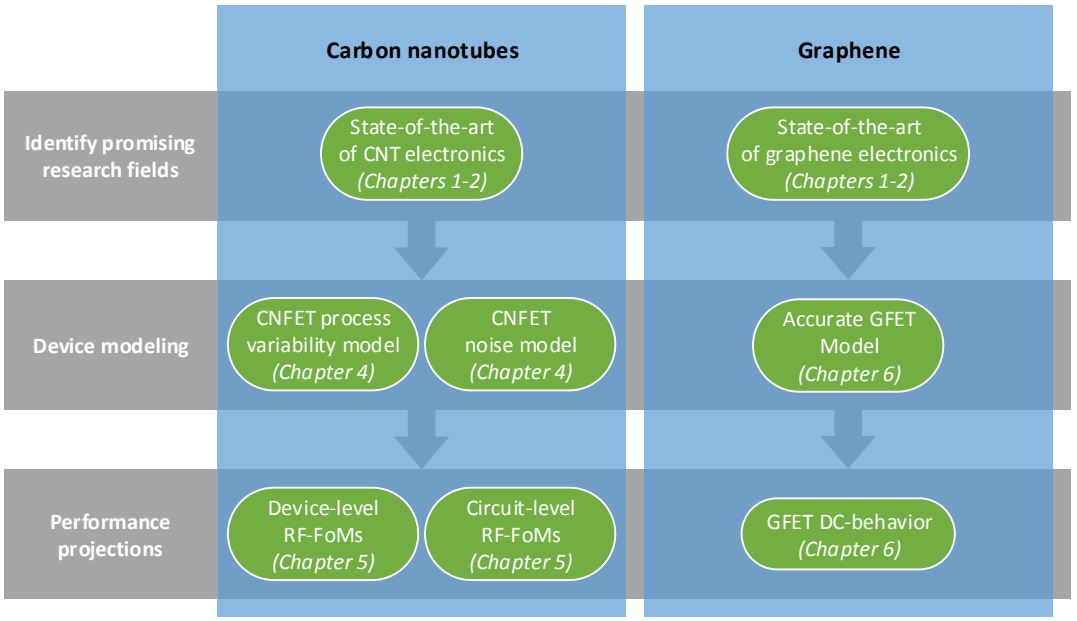

FIGURE 3.1: Methodology applied in this thesis and treated work packages.

The Stanford CNFET Compact Model [132–135] has been a main tool for this work's investigations on carbon-based electronics. This model has been available from its authors in the form of a Verilog-A implementation. A main result of this thesis is the extension of this tool by a noise compact model and a manufacturing process variability model. This extended model has been used to determine a comprehensive set of RF-FoMs on device and circuit level, which stand out due to fact that they systematically consider the effects of noise. The Virtuoso Analog Design Environment [136] of Cadence Design Systems with its included Verilog-A compiler and its wide spectrum of simulation tools has been used both for the development of the additional model functionalities as well as for the performed circuit simulations.

The work on graphene electronics is based on a compact model [137, 138] developed by David Jiménez at the Universitat Autònoma de Barcelona, Spain. In early simulations it has been seen that this class of GFET models yields unrealistic results amongst others for the GFET's saturation behavior. This occurred under several biasing conditions like low-voltage biasing and approximations made in the derivation of the model equations were identified as the cause for this behaviour. This motivated the work on a more accurate GFET compact model, which was developed with the numerical computing environment MATLAB [139] and then implemented in Verilog-A. It is compatible with circuit simulators such as the Virtuoso Analog Design Environment and can therefore

easily be employed for the exploration of graphene-based circuits. However, as there still does not exist any suitable GFET noise compact model, the investigations on RF-FoMs performed for the CNFET technology were not repeated for the GFET technology.

3.3 Organizational framework

The author of this thesis, Gerhard Martin Landauer, has developed his work at the High Performance Integrated Circuits and Systems Design (HIPICS) group of the Electronics Engineering Department of the Universitat Politècnica de Catalunya, Barcelona, Spain. His thesis was mainly funded by a competitive FI-DGR grant of the Catalan Government. Within the scope of the thesis he participated at the Design And Test Principles For Terascale Integrated Systems (TEC2008-01856) project of the Spanish Ministry of Science and Innovation and the Terascale Reliable Adaptive Memory Systems (FP7 248789) project of the European Union.

The director of this thesis, Dr. José Luis González, was formerly Associate Professor at the Electronics Engineering Department of the Universitat Politècnica de Catalunya, Barcelona, Spain, where he was amongst others responsible for the Electronics Engineering Ph.D. programme. Since 2011 he works as a Senior Research Engineer at the Laboratoire d'Architectures Intégrées Radiofréquences (LAIR) at CEA-Leti, Grenoble, France, from where he continued the supervision of this thesis. During his absence from the Universitat Politècnica de Catalunya, Dr. Antonio Rubio, head of the HIPICS group, was the administrative responsible of the author.

A part of this thesis was elaborated during a 4-month foreign stay between September 2012 and January 2013 at the LAIR laboratory at CEA-Leti, Grenoble, France.

The parts of this thesis treating graphene electronics were made in cooperation with Dr. David Jiménez, Associate Professor at the Escola d'Enginyeria of the Departament d'Enginyeria Electrònica of the Universitat Autònoma de Barcelona, Bellaterra, Spain.

Chapter 4

A process variability and noise model for carbon nanotube field-effect transistors

IN ORDER to investigate systematically on the CNFET's RF performance, a suitable RF compact model is required. Such a model has to include noise, as this phenomenon is crucial for RF applications. Efforts have been made in recent years by characterizing specific device samples [140, 141], but noise in CNFETs has not been described in a general way before this thesis. Apart from noise, an RF-CNFET compact model must also take into account sources of manufacturing process variability in order to guarantee realistic simulation results. Among these sources are CNT diameter and dopant variations, the impact of mCNTs, and mCNT removal imperfections [142].

In this chapter extensions to the Stanford CNFET compact model [132–135] are presented, which complete it with noise and variability modeling. They are implemented in Verilog-A and compatible with commercial circuit simulators. Sec. 4.1 provides a brief introduction to the extended CNFET model, which includes the assumed device geometry, the model's input parameters, and the physical properties of the model. Then, Secs. 4.2 and 4.3 describe the variability and the noise model, respectively. Sec. 4.4 illustrates the model's behavior by presenting typical CNFET characteristics. Finally, in Sec. 4.5 conclusions about this work are drawn.

This chapter serves as a basis for the following Chapter 5, where the developed model will be employed for a detailed analysis of the CNFET's RF performance. Appendix B provides the Verilog-A source code of the model extensions.

4.1 Basic characteristics of the CNFET model

4.1.1 RF-CNFET structure

The device modeled here is a quasi-ballistic n-type MOSFET-like RF-CNFET. Its channel consists of an array of aligned CNTs (device geometry shown in Fig. 4.1), as required for high-performance RF applications [84]. The CNT array density D is in the following simulations assumed as $100\,\mu m^{-1}$, if not otherwise indicated. Multiple gate fingers and S/D contacts are used to reduce parasitic contact and access resistances. The intrinsic channel is embedded in a high-κ dielectric (assumed as 4 nm HfO_2, relative permittivity $\kappa = 16$) and covered by a metal gate. The gate length L_g can be chosen within a range from 22 to 65 nm. While the intrinsic CNTs are undoped, the extrinsic S/D extensions with lengths L_{sd} equal to L_g are heavily doped to reduce the performance-degrading Schottky barriers between the CNTs and S/D metal electrodes.

4.1.2 Model input parameters

Table 4.1 lists the extended CNFET model's input parameters and the values typically chosen for this work's simulations. The model allows to vary basic device characteristics such as the channel and tube extension length, the CNT-array pitch, the gate oxide height and permittivity, and the number of gate fingers and CNTs. The parameters affecting process variability and noise are discussed in detail in the following Secs. 4.2 and 4.3.

The configuration files `parameters.vams` (see Appendices B.1 and B.2) give extended control over the CNFET behavior in addition to the parameters mentioned in Table 4.1. They allow to modify advanced properties of the Stanford CNFET model such as the carrier scattering mean-free path or the extrinsic parasitic capacitances.

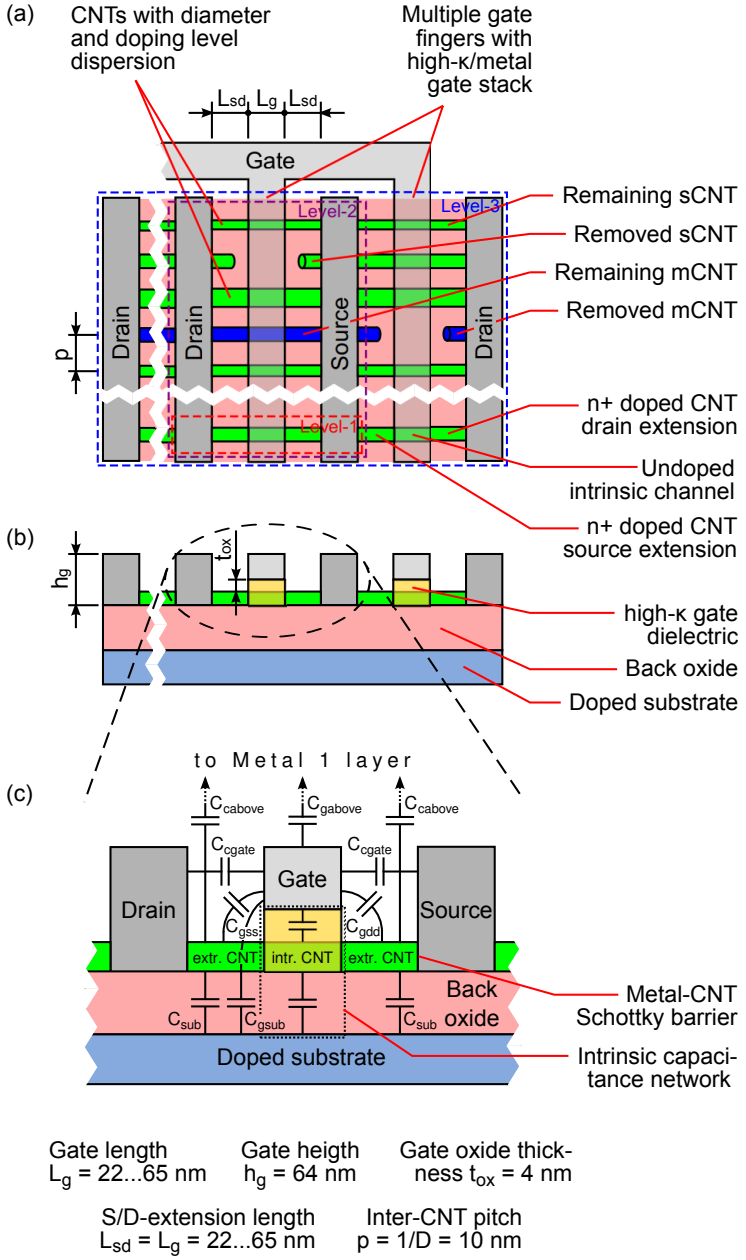

FIGURE 4.1: (a) Top view of the CNFET device under investigation, including manufacturing imperfections. The Level-1 (single tube), Level-2 (single finger), and Level-3 (whole device) CNFET models are indicated. (b) Cross-section of the CNFET. (c) Detailed view of the cross-section of a single-tube CNFET element, including the considered extrinsic capacitances [134, 135]: C_{gsub} is the gate-to-substrate fringe capacitance; C_{gabove} is the local interconnect to Metal 1 coupling capacitance; C_{cgate} is the gate to S/D-electrode coupling capacitance, valid for $L_{\mathrm{sd}} = L_{\mathrm{g}} = 22 \ldots 65\,\mathrm{nm}$; C_{sub} is the CNT-to-substrate capacitance (10 µm-thick SiO_2 back oxide); C_{cabove} is the CNT-Metal 1 coupling capacitance; C_{gss} and C_{gdd} are the gate-CNT extension inner-fringe capacitances. The intrinsic capacitance network is described in detail in [132].

TABLE 4.1: Input parameters for the extended CNFET model.

Input parameter	Description	Typical value
`Lg`	Gate length L_g and S/D extension length L_{sd}	32 nm (from 22 to 65 nm)
`pitch`	CNT pitch p	10 nm
`Kgate`	Gate oxide relative permittivity κ	16
`Tox`	Gate oxide height h_g	4 nm
`dist_type`	Diameter distribution $f_X(d_{Tube})$	0 for Process A 1 for Process B
`dia_mean`[1]	CNT diameter mean value $\mu(d_{Tube})$	1.5 nm
`dia_stddev`[1]	CNT diameter standard deviation $\sigma(d_{Tube})$	0.2 nm
`Efi_mean`	Doped CNT Fermi level mean value	0.66 eV ($\mu(f_{Doping}) = 1\%$)
`Efi_stddev`	Doped CNT Fermi level standard deviation	0.03 eV ($\sigma(f_{Doping}) = 0.1\%$)
`psemi`	Probability of growth of sCNT p_{Semi}	100% (from 0% to 100%)
`premsemi`	Probability of removal of sCNT $p_{RemSemi}$	0% (from 0% to 100%)
`premmet`	Probability of removal of mCNT p_{RemMet}	0% (from 0% to 100%)
`numtubes`	Number of CNTs in aligned tube array	10 (from 1 to 10)
`numfingers`	Number of gate fingers	10 (from 1 to 10)
`pos_tran`	Transistor number, to set inter-transistor variability correlations	0
`alpha_h`	Hooge's flicker noise constant α_H	10^{-4}

[1] Value ignored for diameter distribution according to Process B.

4.1.3 Model hierarchy

Fig. 4.1.(a) indicates the hierarchical structure of the extended CNFET model. The Level-1 model (Appendix B.1) describes the intrinsic mechanisms and extrinsic parasitics of a single-tube element. It is based on the Stanford CNFET compact model [132–135], which has been extended in this work by noise and variability mechanisms. The Level-2 model (Appendix B.2) instantiates Level-1 single-tube devices to form a CNT-array controlled by a single gate finger. The Level-3 model (Appendix B.3) instantiates in the same manner multiple Level-2 elements in order to create the overall device.

4.1.4 CNFET model physics

As mentioned above, the individual 1-tube elements building up the overall RF-CNFET structure are instantiations of the Stanford CNFET compact model [132–135]. This model provides a comprehensive description of the electrical behavior of the intrinsic CNT and additional extrinsic elements. It covers relevant physical aspects such as an intrinsic transcapacitance network, carrier scattering, and extrinsic parasitics.

Extrinsic resistances are caused by the CNT-metal Schottky interface and the resistance of the doped tube extensions. A detailed view of the extrinsic capacitance network is given in Fig. 4.1.(c). The intrinsic model is based on a quantized band structure. It considers the first two subbands due to circumferential quantization and the first ten substates due to axial quantization. In addition, quantum capacitance and quantum inductance effects as well as inter-CNT charge screening are included.

In the intrinsic channel the carriers move with the energy-dependent Fermi velocity v_{F}. Assuming a 1.5 nm-CNT, electrons at the lowest possible conduction band energy move with $v_{\mathrm{F}} = 4.04 \times 10^5\,\mathrm{m\,s^{-1}}$ and asymptotically reach $9.95 \times 10^5\,\mathrm{m\,s^{-1}}$ for high energy. v_{F} determines the theoretical cut-off frequency limit $f_{\mathrm{T,lim}} = v_{\mathrm{F}}/2\pi L_{\mathrm{g}}$ [95]. For instance, an intrinsic CNFET with diameter $d_{\mathrm{Tube}} = 1.5\,\mathrm{nm}$ and $L_{\mathrm{g}} = 32\,\mathrm{nm}$ reaches 77% of $f_{\mathrm{T,lim}}$.

Inelastic scattering on acoustical and optical phonons as well as elastic scattering reduce the injected carriers' transmission probability from source to drain from unity (*i.e.*, ballistic transport) to slightly below unity (*i.e.*, quasi-ballistic transport) with still a high percentage of ballistic electrons. In the previous example of the 1.5 nm x 32 nm CNT, 99.5% of the electrons at the lowest conduction band energy move ballistically.

4.2 A manufacturing process variability model for carbon-nanotube field effect transistors

Today's CNFET fabrication technologies are still adversely affected by several shortcomings. It is not possible to provide exact control over CNT diameter and doping, or the removal of tubes with metallic behaviour [142].

Among these sources of variability, tube diameter dispersion has a major impact on device behavior, as the diameter d_{Tube} of a CNT defines its electrical behavior. In this work two tube growth processes with distinct diameter distributions are assumed (Fig. 4.2): Process A represents a desirable distribution of Gaussian nature with an average of $\mu = 1.5\,\mathrm{nm}$ and a small standard deviation of $\sigma = 0.2\,\mathrm{nm}$ [142]. Its diameter probability density function (PDF) is

$$f_{\mathrm{A}}(d_{\mathrm{Tube}}|\,\mu,\sigma) = \frac{1}{\sigma\sqrt{2\pi}} \cdot \exp\left(-\frac{(d_{\mathrm{Tube}}-\mu)^2}{2\sigma^2}\right) . \tag{4.1}$$

In contrast, Process B reflects the statistical properties of a real growth process as reported in literature [143]. It has a diameter range from 0.4 to 3.5 nm with a mean value of 1.17 nm and is empirically fitted by a shifted log-normal PDF:

$$f_{\mathrm{B}}(d_{\mathrm{Tube}}|\,\mu,\sigma) = \frac{1}{(d_{\mathrm{Tube}}-d_0)\sigma\sqrt{2\pi}} \cdot \exp\left(-\frac{(\ln(d_{\mathrm{Tube}}-d_0)-\mu)^2}{2\sigma^2}\right) . \tag{4.2}$$

$d_0 = 0.346\,\mathrm{nm}$, $\mu = -0.485\,\mathrm{nm}$, and $\sigma = 0.837\,\mathrm{nm}$ are parameters obtained by least-square fitting to measurement data [143].

The diameter of a CNT defines its band gap and therefore the conduction type, *i.e.*, semiconducting or metallic. As one third of the possible CNT geometries give a band structure lacking a band gap, diameter variability leads to a growth-process dependent fraction of mCNTs forming part of the channel array and reducing the fraction p_{Semi} of sCNTs. Typical values range from p_{Semi} equal to 67% for a tube synthesis without preference for any conduction type up to about 96% for highly selective growth processes [87]. The mCNTs act as performance-degrading shunt resistances in parallel to the sCNTs. By applying an optional mCNT removal step, e.g. electrical burning [89], a large part of the mCNTs can be removed. However, this step also unintentionally destroys

some of the useful semiconducting tubes. The probabilities of mCNT- and sCNT-removal are assumed as $p_{\mathrm{RemMet}} = 0 \ldots 100\%$ and $p_{\mathrm{RemSemi}} = 0 \ldots 10\%$, respectively.

Apart from diameter dispersion and tube removal uncertainty, chemical n-type doping in the source and drain regions is assumed as a third source of variability. The doping level molar fraction f_{Doping} shows a Gaussian distribution with 1% mean and 0.1% standard deviation (following [142]).

See Table 4.2 for a summary of the considered process variability sources.

TABLE 4.2: Variable process parameters assumed for the simulations performed in this work.

CNT growth and doping	
d_{Tube}	Process A: $\mu = 1.5\,\mathrm{nm}$, $\sigma = 0.2\,\mathrm{nm}$ (Gauss.)
	Process B: 0.4 to 3.5 nm (measured)
f_{Doping}	$\mu = 1\%$, $\sigma = 0.1\%$ (Gauss.)
p_{Semi}	$67 \ldots 100\%$
mCNT removal	
p_{RemMet}	$0 \ldots 100\%$
p_{RemSemi}	$0 \ldots 10\%$

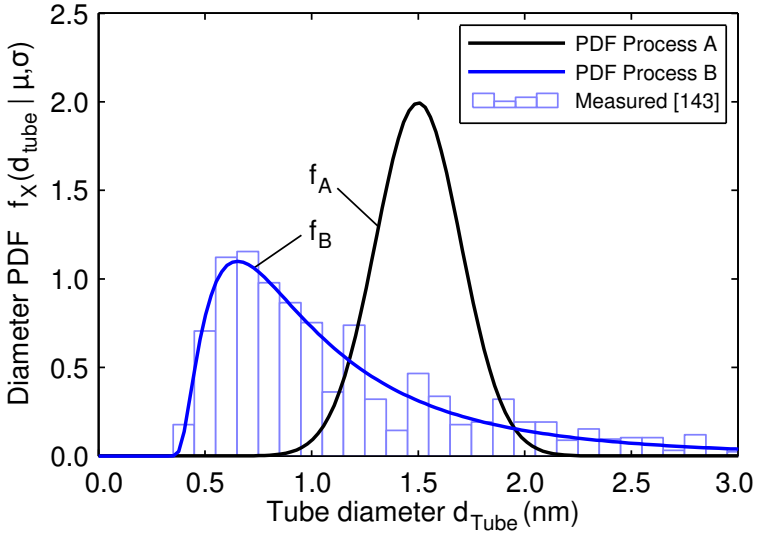

FIGURE 4.2: Probability density functions of the tube diameters d_{Tube} of Processes A and B. f_{A} is a Gaussian PDF, f_{B} is a shifted log-normal PDF fitted to measurement data reported in [143].

4.2.1 Implementation of the CNFET variability model in Verilog-A

Verilog-A offers functions to generate random numbers with uniform and normal (Gaussian) distribution patterns:

```
$rdist_uniform(seed, min, max);
$rdist_normal(seed, mean, stddev);
```

The seed variable is used to initialize the pseudo-random generators behind these functions. It provides a starting point for computing the number sequences. Given identical seed and statistical input parameters, the same sequence can be repeatedly generated.

Each Level-1 single-tube CNFET instantiation individually evaluates the random variables (RV) Fermi level shift in the doped extrinsic region `Efi`, tube removal `tube` (1 if CNT exists, 0 if CNT has been removed), conduction type `condtype` (1 if sCNT, 0 if mCNT), and tube diameter `diameter`. For the doping level and the tube removal probability there is no correlation between neighbouring Level-1 devices. In contrast, d_{Tube} and the conduction type must not change for the Level-1 devices arranged along an individual CNT. These correlations of the latter two RVs have been achieved with the seed generation structure shown in Fig. 4.3.

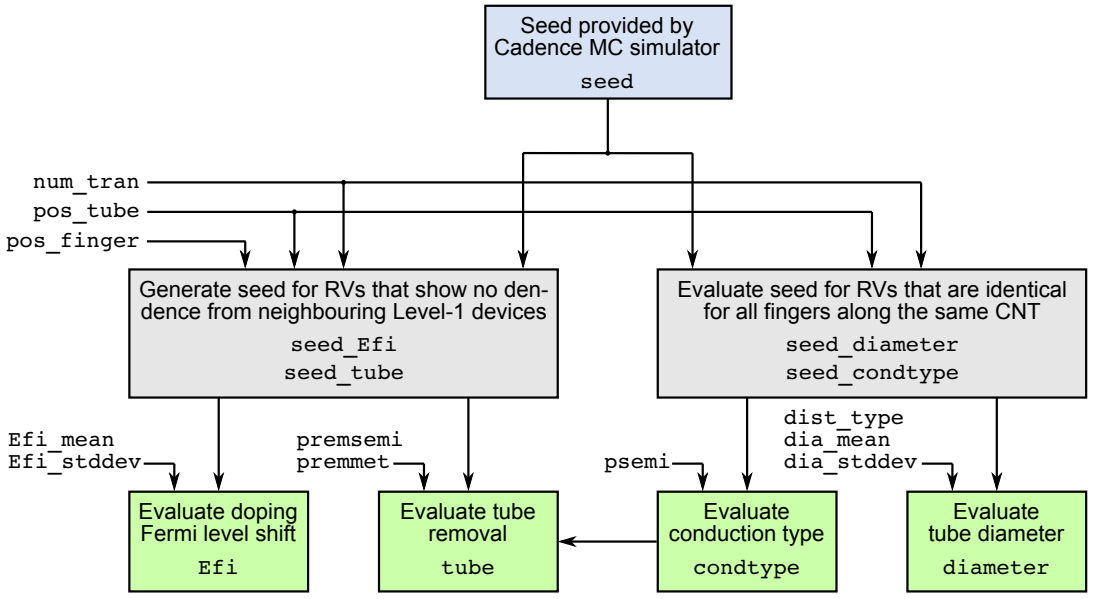

FIGURE 4.3: Implementation of the CNFET variability model.

Each of the single-tube devices in the `numtubes` x `numfingers` field of Level-1 elements is assigned a tube position `pos_tube` and finger position `pos_finger`. This allows the Level-1 instantiations to know their position in the overall array. Based on these two coordinates and on an initial random number `seed` provided by the Cadence Monte-Carlo simulator, each Level-1 element computes four additional seeds. While `seed_Efi` and `seed_tube` do not depend on neighbouring devices, `seed_diameter` and `seed_condtype` and therefore the RVs `diameter` and `condtype` are constant along a single CNT. In addition, in order to investigate on the effects of process mismatch between overall CNFETs, to each Level-3 device a transistor number `num_trans` is assigned. For CNFETs with identical `num_trans` the same characteristics are generated.

In continuation, two examples illustrate the generation of the RVs. Depending on the distribution type `dist_type`, diameter dispersions according to Process A or B are computed as follows:

```
if (dist_type==0) begin // Gaussian distribution
  diameter = $rdist_normal(seed_diameter, dia_mean, dia_stddev);
end else begin // Shifted log-normal distr., fitted to measurements
  diameter = exp($rdist_normal(seed_diameter,-0.4853,0.8366))+0.3463;
  diameter = diameter*1e-9; // in nm
end
```

The following structure is employed to determine the conduction type of the CNTs. In a similar form it is also used to determine if a CNT has been removed from a single-tube device.

```
if ($rdist_uniform(seed_condtype, 0, 1)<=psemi) begin
  condtype=1; // growth of sCNT
end else begin
  condtype=0; // growth of mCNT
end
```

The overall source code of the CNFET process variability model can be found in Appendix B.

4.3 A compact noise model for carbon-nanotube field effect transistors

Noise current sources corresponding to various noise generation mechanisms contribute to the CNFET's overall noise. Fig. 4.4 shows an equivalent circuit including the noise sources described in this section. The calculation of their power spectral densities (PSD) and the sources themselves have been added to the original Verilog-A code of the Stanford CNFET compact model [132–134] (see Appendix B.1).

4.3.1 CNFET noise sources

4.3.1.1 Suppressed channel shot noise

Conventional noise theory for long-channel devices [144] underestimates the drain noise in short channels, because it neglects shot noise effects occurring in the ballistic and quasi-ballistic transport regime [145]. In strongly downscaled transistors like the CNFET the main obstacle to carrier flow is not scattering, but a potential barrier near the source end of the channel. In case of low carrier density in the channel such as in the deep subthreshold regime, the hopping of carriers over this barrier follows Poissonian statistics

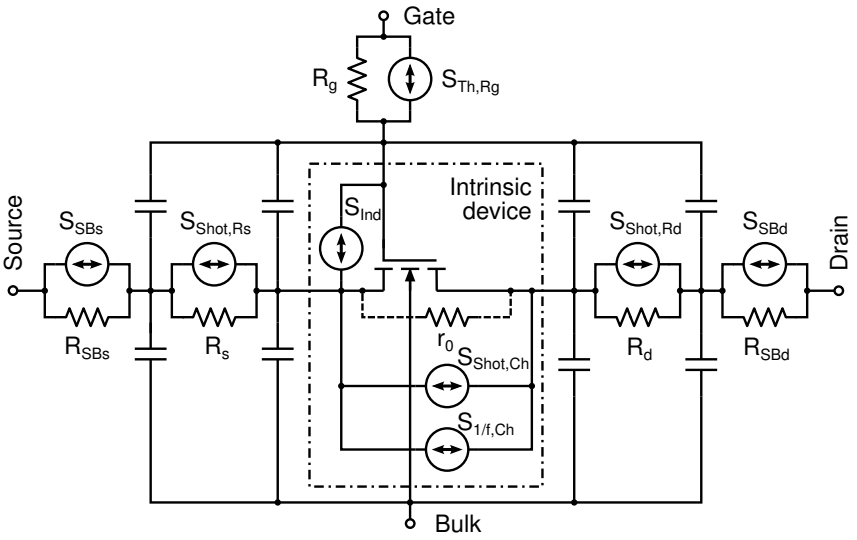

FIGURE 4.4: CNFET equivalent circuit [132], including noise current sources for the intrinsic channel's suppressed shot noise and flicker noise ($S_{\mathrm{Shot,Ch}}$, $S_{1/\mathrm{f,Ch}}$), suppressed shot noise at the S/D extensions ($S_{\mathrm{Shot,Rs}}$, $S_{\mathrm{Shot,Rd}}$), at the S/D contact Schottky barriers (S_{SBs}, S_{SBd}), the parasitic gate resistance ($S_{\mathrm{Th,Rg}}$), as well as channel-induced gate noise (S_{Ind}).

and results in the well-known full shot noise PSD $S_{\mathrm{Shot,full}} = 2qI_{\mathrm{D}}$, where q is the elementary charge and I_{D} the drain current. With increasing electron density, the Pauli exclusion principle as well as long-range Coulomb interactions between the electrons begin to play a significant role. They introduce correlations between subsequent carrier injections, which reduces the noise PSD below the mentioned full shot noise level.

Iannaccone *et al.* developed an analytical framework for suppressed shot noise in ballistic nanoscale MOSFETs [146, 147]. They express the PSD of suppressed shot noise as:

$$S_{\mathrm{Shot,Ch}} = 2q^2 \int_{E=0}^{\infty} vD \left[\left(1 - \frac{\tilde{v} C_{\mathrm{qs}}}{C_{\mathrm{g}} + C_{\mathrm{qs}}} \frac{1}{v} \right)^2 f_{\mathrm{s}} \left(1 - f_{\mathrm{s}} \right) \right] \mathrm{d}E \ . \tag{4.3}$$

The components responsible for Pauli and Coulomb suppression can be easily identified as the factor $(1 - f_{\mathrm{s}})$ and the squared term between round parentheses, respectively. Pauli suppression depends on the Fermi-Dirac occupation factor f_{s} at the source end of the channel. Carriers injected at the drain end are not considered, as far-from-equilibrium conditions are assumed. Coulomb suppression depends on the geometrical gate capacitance C_{g}, the quantum capacitance C_{qs} due to carriers injected from the source end, the longitudinal electron velocity v, and a weighted longitudinal electron velocity $\tilde{v}$, which is addressed in detail in [146]. Further expressions required to evaluate Eq. (4.3) are the elementary charge q and the density of states D. The integration variable E represents energy.

This solution has been adapted to be easily computable with the Stanford CNFET model. Notably, the particular band structure of short CNTs is considered [132]. The allowed energy states $E_{(\mathrm{m,l})}$ of CNTs are obtained by applying Born-von Karman boundary conditions to graphene's energy dispersion relation. Each value $E_{(\mathrm{m,l})}$ corresponds to a circumferential wave number k_{m} and an axial wave number k_{l}. Here, m and l denote the mth subband due to quantization in the circumferential direction of the CNT and the lth substate due to axial quantization. The integral over E in Eq. (4.3) is replaced by a double sum over these two wavenumbers, which is equivalent to summing over $E_{(\mathrm{m,l})}$ states and facilitates computational evaluation. Only the lowest two subbands and the first several substates in axial direction are significantly occupied by charge carriers, limiting these two sums to reasonable lengths. D is unity at energies equal to $E_{(\mathrm{m,l})}$,

and zero otherwise. Its normalization to channel length is considered by $1/L_\mathrm{g}$. With two-fold subband and spin degeneracy, we finally obtain Eq. (4.4).

$$S_\mathrm{Shot,Ch} = \frac{8q^2}{L_\mathrm{g}} \sum_{k_\mathrm{m}} \sum_{k_\mathrm{l}} \left[v \left(1 - \frac{\tilde{v} C_\mathrm{qs}}{C_\mathrm{g} + C_\mathrm{qs}} \frac{1}{v} \right)^2 f_\mathrm{s} \left(1 - f_\mathrm{s} \right) \right] \tag{4.4}$$

Fig. 4.5 shows the shot noise suppression behavior of a typical CNFET, obtained by evaluating Eq. (4.4). It is expressed by the Fano factor $F_\mathrm{Shot} = S_\mathrm{Shot,Ch}/S_\mathrm{Shot,full}$, which is unity for Poissonian shot noise and smaller than unity in the case of suppression. For usual drain bias currents, the impact of both Pauli exclusion and Coulomb interaction is pronounced and reduces noise to just a few percent of full Poissonian noise.

This work does not consider the effect of shot noise enhancement due to hole injection from the drain to bound states in the intrinsic channel [147], which occurs in low band-gap CNTs under certain biasing conditions. This effect is only relevant in the sub-threshold regime and therefore of minor importance for common RF applications.

The developed description for suppressed channel shot noise in CNFETs is only valid for sCNT channels. In the case of ballistic mCNTs the Fano factor approaches zero [148].

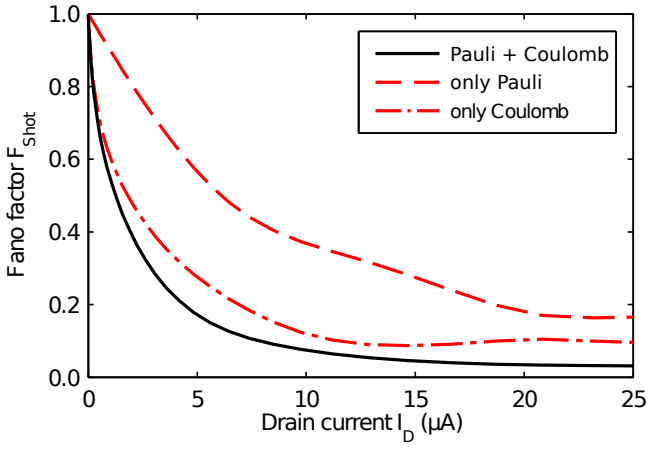

FIGURE 4.5: Fano factor F_Shot vs. drain current I_D, indicating shot noise suppression in a 32 nm node CNFET with a single-tube channel ($d_\mathrm{Tube} = 1.5\,\mathrm{nm}$), biased with a drain-source voltage $V_\mathrm{DS} = 0.9\,\mathrm{V}$. Room temperature conditions apply. The effects only due to Pauli exclusion or Coulomb interaction as well as their overall impact are shown.

4.3.1.2 Channel flicker noise

High flicker noise in CNFETs has been reported in literature [140]. It is inversely proportional to frequency f and it's PSD follows in first order Hooge's empirical law

$$S_{1/\mathrm{f,Ch}} = \frac{\alpha_{\mathrm{H}}}{n} \cdot \frac{I_{\mathrm{D}}^2}{f} \ , \tag{4.5}$$

where α_{H} is the technology-dependent Hooge's constant and n the number of charge carriers in the conductor. In this work the pessimistic assumption of $\alpha_{\mathrm{H}} = 10^{-4}$ is made, as usual for unoptimized manufacturing technologies [149].

4.3.1.3 Channel-induced gate noise

Due to the lack of theoretical treatment of this type of noise for ballistic CNFETs, it is assumed that van der Ziel's description of channel-induced gate noise [144] is valid to estimate this noise source's impact. Van der Ziel stated the channel noise PSD as

$$S_{\mathrm{Ch,vdZ}} = 4k_{\mathrm{B}}T\gamma g_{\mathrm{d0}} \tag{4.6}$$

and the channel-induced gate noise PSD as

$$S_{\mathrm{Ind,vdZ}} = 4k_{\mathrm{B}}T\delta\frac{\omega^2 C_{\mathrm{GS}}^2}{5g_{\mathrm{d0}}} \ . \tag{4.7}$$

In these equations, k_{B} the Boltzmann constant, T the absolute temperature, $\gamma = 2/3$ is the white noise gamma factor, g_{d0} is the drain-source conductance of the completely open channel, $\delta = 4/3$ is the gate noise coefficient, $\omega = 2\pi f$ the angular frequency, and C_{GS} the gate-source capacitance. $S_{\mathrm{Ch,vdZ}}$ and $S_{\mathrm{Ind,vdZ}}$ are partially correlated with a correlation factor of $0.395j$.

A bias-dependent equivalent g_{d0} is obtained by equating Eq. (4.6) with Eq. (4.4). This step yields this model's channel-induced gate noise PSD:

$$S_{\mathrm{Ind}} = \frac{128}{45}\left(k_{\mathrm{B}}T\omega C_{\mathrm{GS}}\right)^2 \frac{1}{S_{\mathrm{Shot,Ch}}} \ . \tag{4.8}$$

4.3.1.4 Thermal gate noise

The ohmic gate resistance generates thermal noise and is approximated as a lumped element per gate finger [94]. Each element has a resistance of

$$R_{\mathrm{g}} = \frac{1}{3}\frac{W_{\mathrm{g}}}{L_{\mathrm{g}}}\frac{\rho_{\mathrm{g}}}{t_{\mathrm{g}}} \ , \tag{4.9}$$

where L_{g} and W_{g} are the gate length and width, respectively. $t_{\mathrm{g}} = 64\,\mathrm{nm}$ is the height of the gate finger. ρ_{g} is the specific resistance of the gate material. Following [94], a tungsten film with $\rho_{\mathrm{g}} = 2 \times 10^{-7}\,\Omega\,\mathrm{m}$ is assumed.

4.3.1.5 Suppressed shot noise in S/D extensions

Dopant ions in the S/D extensions increase the Fermi level up to the conduction band and let the extensions act as metal-like always-on conductors. However, they reduce the mean-free path $L_{\mathrm{MFP,sd}}$ between subsequent scattering events to an estimated value of 15 nm [133]. As $L_{\mathrm{MFP,sd}}$ is in the range of L_{sd}, transport in the extension regions is not ballistic, but has a strong diffusive component. The Fano suppression factor of one-dimensional metallic conductors with diffusive transport ($L_{\mathrm{MFP,sd}} \ll L_{\mathrm{sd}}$) due to elastic scattering is universally given as $F_{\mathrm{Shot}} = 1/3$. In the case of ballistic transport ($L_{\mathrm{MFP,sd}} \gg L_{\mathrm{sd}}$) it approaches zero. This transition from the diffusive to the ballistic regime is described by [148]

$$S_{\mathrm{Shot,Rs/d}} = \frac{2}{3}\left(1 - \frac{1}{\left(1 + L_{\mathrm{sd}}/L_{\mathrm{MFP,sd}}\right)^3}\right) qI_{\mathrm{D}} \ . \tag{4.10}$$

4.3.1.6 Flicker noise in S/D extensions

α_H is virtually not influenced by carrier scattering at ionized impurities introduced by doping [140], so it is assumed to be constant over the whole CNT, *i.e.* along the intrinsic channel and doped S/D extensions. In the doped regions with diffusive transport regime the carriers suffer higher scattering and are slower compared to the channel, which implies higher n and therefore lower flicker noise [Eq. (4.5)]. Thus, flicker noise in the

source and drain extensions is in the first approximation negligible compared to the high channel flicker noise.

4.3.1.7 Noise at the CNT-metal contact Schottky barrier

The Schottky barriers at the contacts between the tube extensions and the S/D metal electrodes are nearly transparent, as the barrier thickness is strongly reduced by heavy CNT doping [133]. Carrier transmission is mainly due to tunneling through the barrier, and not due to thermoionic emission over it. The noise in tunneling junctions, with only the lowest sub-band significantly contributing to carrier transport, and double subband and spin degeneracy can be expressed as [148]

$$S_{\mathrm{SBs/d}} = \frac{4q^2}{h}\left(4k_{\mathrm{B}}TT_{\mathrm{n}}^2 + 2T_{\mathrm{n}}\left(1-T_{\mathrm{n}}\right)qV\coth\left(\frac{qV}{2k_{\mathrm{B}}T}\right)\right) \ . \tag{4.11}$$

The term $4q^2/h$, with h being the Planck constant, is the inverse of the CNT quantum resistance of $6.45\,\mathrm{k\Omega}$. T_{n} is the carrier transmission probability and V the voltage drop over the tunneling junction. This equation yields a bias-dependent sum of thermal and shot noise.

With this final noise source all sources required for the overall CNFET compact noise model illustrated in Fig. 4.4 have been described.

4.3.2 Implementation of the noise sources in Verilog-A

Verilog-A provides a set of functions to support the modeling of noise for small-signal simulations. This has allowed to implement the CNFET noise sources presented in the previous section.

Thermal gate noise $S_{\mathrm{Th,Rg}}$, suppressed shot noise in S/D extensions $S_{\mathrm{Shot,Rs/d}}$, and noise at the CNT-metal contact Schottky barrier $S_{\mathrm{SBs/d}}$ are white noise sources (*i.e.*, frequency-independent). They have been described using the command

```
I(Node1, Node2) <+ white_noise(S);
```

which adds a frequency-independent noise current with a power spectral density `S` between two nodes `Node1` and `Node2` of the circuit.

Similarly, the frequency-dependent flicker noise $S_{1/\mathrm{f,Ch}}$ has been implemented with the command

```
I(Node1, Node2) <+ flicker_noise(S,a);
```

which creates a current noise source with a frequency-dependent PSD of $S \propto f^{-a}$. The factor `a` has been set to 1.0.

However, while Verilog-A provides these two straightforward solutions for the implementation of white and flicker noise, additional steps have to be taken in the case of correlated noise. In this model, the suppressed channel shot noise $S_{\mathrm{Shot,Ch}}$ and the channel-induced gate noise S_{Ind} have been implemented following the method reported in [150]:

In order to create correlated noise sources, first an auxiliary node `Noise` has been introduced. It sinks a noise current with the PSD `Sch` that is equal to the one of the suppressed channel shot noise $S_{\mathrm{Shot,Ch}}$.

```
I(Noise)  <+ V(Noise)*1.0;
I(Noise)  <+ white_noise(Sch);
```

Subsequently, the channel's noise has been divided into a to the gate noise uncorrelated part

```
I(Drain, Source) <+ white_noise((1.0-noise_corr*noise_corr)*Sch);
```

and a correlated part

```
I(Drain, Source) <+ noise_corr*V(Noise);
```

Here, `noise_corr` is equal to the absolute value $|0.395j|$ of the correlation constant. Finally, the channel-induced gate noise current has been added with the command

```
I(Gate, Source) <+ ddt(V(Noise)*sqrt(noise_ratio));
```

The time derivative operator `ddt( )` yields the frequency dependence $S_{\mathrm{Ind}} \propto \omega^2$ as well as the 90° phase shift due to the complex correlation constant. `sqrt( )` is the square-root function and `noise_ratio` is the ratio $S_{\mathrm{Ind}}/S_{\mathrm{Shot,Ch}}$ for $\omega = 1$.

With the above presented three methods to create white, flicker, and correlated noise, all types of noise required for this work have been modeled. For completeness, Appendix B.1 gives the Verilog-A code of the overall implementation of the noise model.

4.4 Typical CNFET behavior

In this section the developed extended model is used to derive basic CNFET characteristics. An $L_{\mathrm{g}} = 32\,\mathrm{nm}$ device sample with 10 CNTs and 10 gate fingers is assumed. Three of the tubes are metallic, as is probable for a conventional tube growth process with $p_{\mathrm{Semi}} = 67\%$.

Fig. 4.6 shows the DC behavior of the device. The impact of the shunt resistance due to the parallel mCNTs is clearly visible both in the transfer and the output characteristics. The metallic tubes impede the device to turn off for low V_{GS} [Fig. 4.6.(a)] and cause a significant output conductance g_0 in the saturation region [Fig. 4.6.(b)]. The linear dependence of the drain current I_{D} on the gate-source voltage V_{GS} in saturation indicates that the device is operated in the velocity saturation regime.

Fig. 4.7 gives insight into the I_{D}-dependence of the transconductance g_{m}, the cut-off frequency f_{T}, and the minimum noise figure NF_{min} for several drain-source voltage biasing points. Comparison shows that peaks in g_{m} are related to maximums of f_{T} and minimums of NF_{min}. The highest achievable f_{T} value of the CNFET under investigation is approximately 675 MHz for high V_{DS} biasing. The lowest NF_{min} values at such biasing are in the range of 1.10 to 1.23 dB.

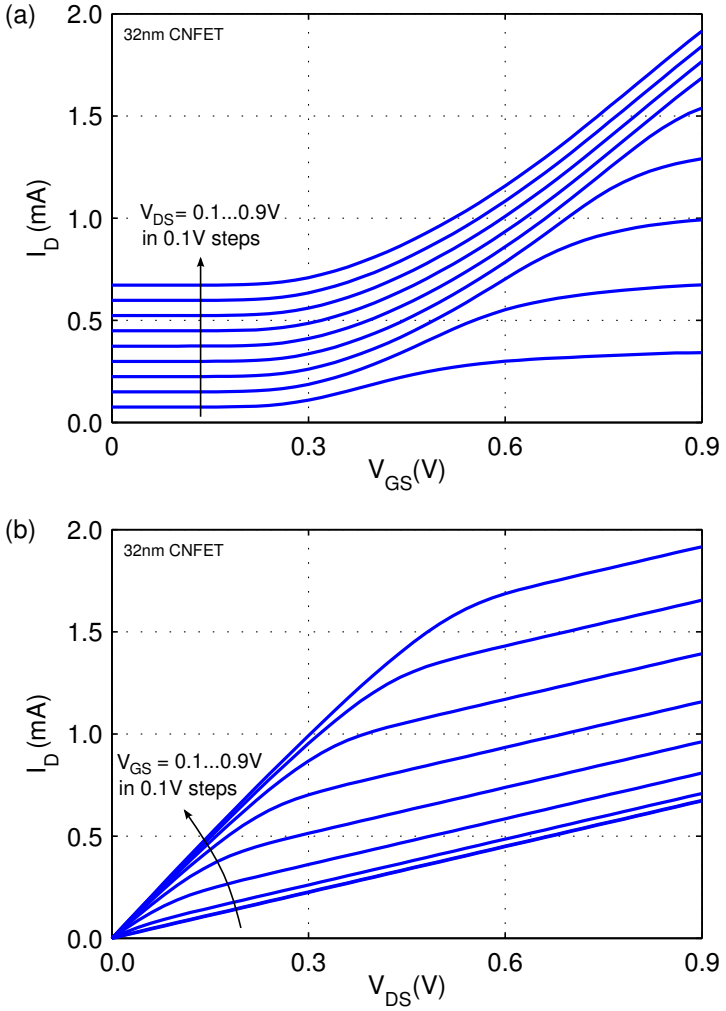

FIGURE 4.6: (a) Transfer characteristics: drain current I_D vs. gate-source voltage V_{GS} for varying drain-source voltage V_{DS}. (b) Output characteristics: drain current I_D vs. drain-source voltage V_{DS} for varying gate-source voltage V_{GS}. The CNFET with a channel length of 32 nm has 10 gate fingers and consists of a tube array with 7 sCNTs and 3 mCNTs.

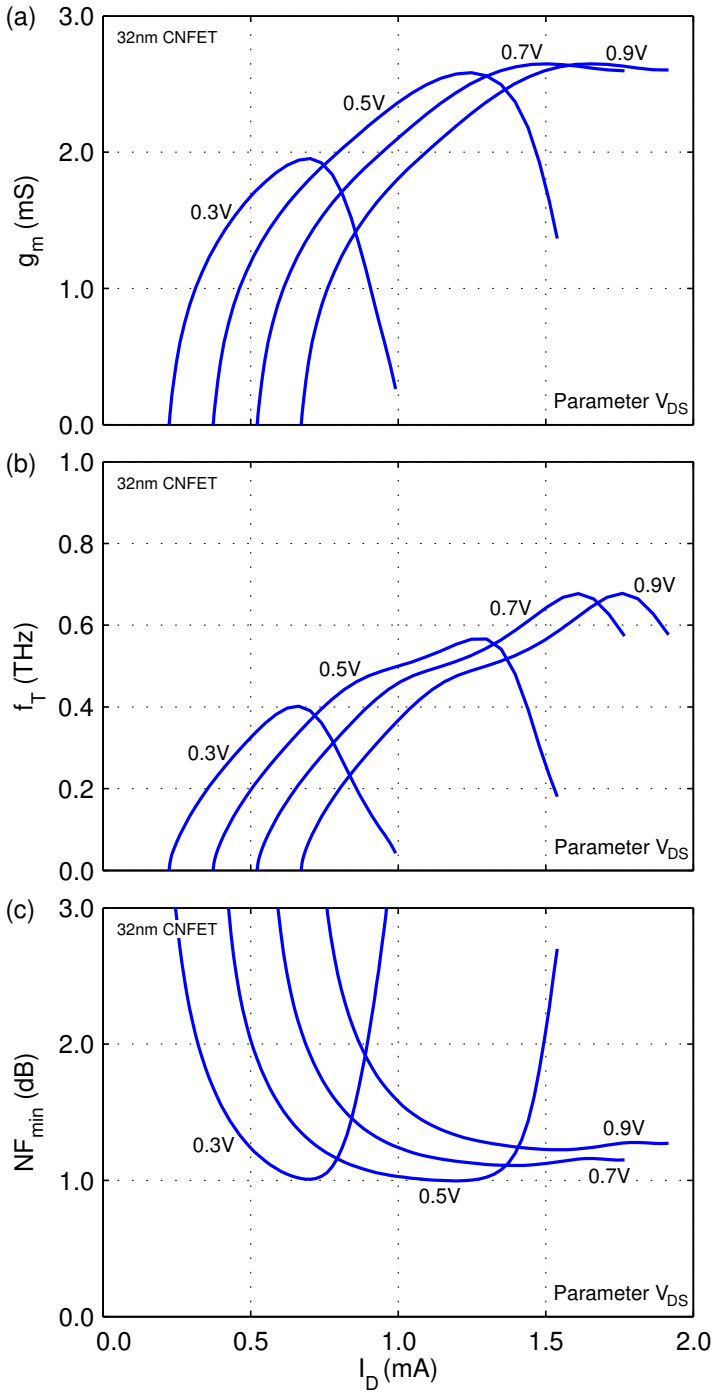

FIGURE 4.7: (a) Transconductance g_{m} vs. drain current I_{D}. (b) Cut-off frequency f_{T} vs. I_{D}. (c) Minimum noise figure NF_{min} vs. I_{D}. The drain-source voltage for V_{DS} is varied from 0.3 to 0.9 V in 0.2 V-steps. Device properties are chosen such as in Fig. 4.6.

4.5 Conclusion

In this chapter models for the manufacturing process variability and for noise in CNFETs have been developed. First, an overview of the assumed device geometry, a brief discussion of the underlying device physics, and the extended model's input parameters have been given. Subsequently, a summary of variability mechanisms, their statistical description, and a discussion of their implementation has been provided. Then, analytical formulas for the PSDs of the quasi-ballistic CNFET's internal noise sources as well as their implementation have been discussed. These two extensions have been coded in Verilog-A (see Appendix B) and are compatible with conventional circuit simulators. They have been added to the Stanford CNFET compact model, which originally was developed for digital design and has in that way been prepared for variability-aware RF simulations.

The proposed manufacturing process variability model includes tube diameter variation and doping variation. It furthermore considers mCNT shunts in parallel to the useful channel and is able to handle imperfect tube removal processes.

Within the development of the CNFET noise model, emphasis has been put on the description of suppressed channel shot noise. Van der Ziel's classical description of MOSFET channel noise breaks down for short-channel devices with quasi-ballistic transport. In such highly downscaled devices the random injection of charge carriers over the channel's potential barrier causes shot noise and the correlation between subsequent injection events leads to a partial noise suppression. Further considered noise sources are channel flicker noise, channel-induced and thermal gate noise, suppressed shot noise and flicker noise in the S/D extensions, as well as noise at the CNT-metal Schottky barrier.

Finally, basic characteristics of a typical CNFET configuration with metallic shorts in the tube array have been presented in order to provide an application example for the developed extended CNFET model.

The work presented in this chapter is a basis for the following Chapter 5, where the extended model will be used for comprehensive analyses of the CNFET device behavior and for RF-CNFET performance projections on the device and circuit level.

Chapter 5

Radio frequency performance of carbon nanotube field-effect transistors on the device and circuit level

IN SPITE of intense investigations on the CNFET's digital behavior [151], studies on its RF properties are still in an early stage and mostly limited to treat the achievable cut-off frequency f_{T} [95, 152]. Ref. [92] addresses a wider field of properties by determining f_{T}, the maximum oscillation frequency f_{max}, and the intrinsic gain g_{m}/g_0 (*i.e.*, the ratio of transconductance g_{m} and output conductance g_0) of RF-CNFETs considering manufacturing process variability. In a similar work [93, 94], RF-FoMs of the CNFET are compared to more conventional technologies. There is yet a need for more detailed investigations on the RF performance of this novel technology, not only at device but also at circuit level, and notably including noise.

This chapter is dedicated to such investigations. It presents a two-part simulation study that aims to determine the capability of the CNFET technology to replace conventional silicon in future RF applications. The corresponding simulations have been performed using the Cadence Virtuoso Spectre Circuit Simulator of Cadence Design Systems, Inc. [153], and are based on a Verilog-A implementation of the process variability and noise extensions presented in Chapter 4. Firstly, a global overview on device properties is

addressed in Sec. 5.1. It includes the optimum biasing point, the influence of the CNT density on performance, the CNFET's noise behaviour, the impact of process variations, and the derivation of a set of RF-CMOS technology requirement FoMs as stated in the ITRS [5]. Secondly, the analysis is extended in Sec. 5.2 from the device level to circuit-level performance for basic RF circuits. Notably, FoMs of LNAs and oscillators operating in the sub-mmW range are reported. Such RF building blocks are chosen because of their ubiquity in RF systems. Both on the device and on the circuit level, the CNFET performance is compared to conventional Si-CMOS and technology scaling trends are analysed. Conclusions are drawn in Sec. 5.3.

5.1 CNFET device level performance

In the following the device level behavior of the CNFET technology defined in Sec. 4.1 is discussed. The considered device is a 10-finger CNFET in common-source configuration. The gate length L_g is 32 nm, unless otherwise specified, and the gate width is 100 nm. The drain-source biasing voltage is $V_\mathrm{DS} = 0.9\,\mathrm{V}$. Room temperature ($T = 300\,\mathrm{K}$) applies.

5.1.1 Optimum biasing point

Before investigating in more detail on device performance, the biasing current for simultaneous high-speed and low-noise operation is determined. For that purpose the analog FoMs f_T and minimum noise figure NF_min are studied in function of the mean bias current per tube I_D. Fig. 5.1 shows that, given a CNT array with a well-behaving diameter distribution such as the one of Process A (Table 4.2), excellent RF performance can be obtained (peak cut-off frequency $f_\mathrm{T,peak} = 1.25\,\mathrm{THz}$, min. $NF_\mathrm{min} = 0.687\,\mathrm{dB}$ at 300 GHz). In contrast, these values cannot be reached when using Process B (peak cut-off frequency $f_\mathrm{T,peak} = 0.45\,\mathrm{THz}$, min. $NF_\mathrm{min} = 1.51\,\mathrm{dB}$ at 300 GHz). The CNFET based on Process A has the desirable property of having the optimum biasing currents for peak f_T and minimum NF_min close together like it is the case for conventional silicon MOSFETs [154]. In fact, $I_\mathrm{D,NFmin} = 15.4\,\mu\mathrm{A/tube}$ for low noise lies slightly below $I_\mathrm{D,fT} = 16.5\,\mu\mathrm{A/tube}$ for highest device speed. For the subsequent device simulations the CNFETs are biased with their optimum biasing currents $I_\mathrm{D} = I_\mathrm{D,fT}$, which provides $f_\mathrm{T,peak}$ and yet keeps noise acceptably low.

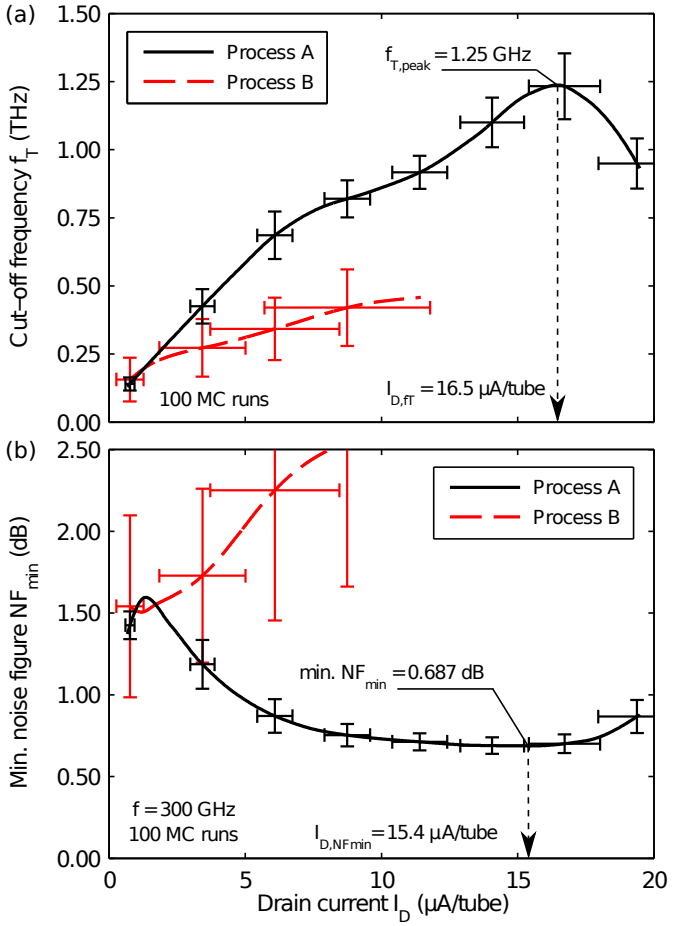

FIGURE 5.1: (a) Cut-off frequency f_T and (b) minimum noise figure NF_{min} at 300 GHz vs. mean biasing current I_D per tube. V_{DS} is fixed to 0.9 V. Varying I_D is obtained by sweeping V_{GS} from 0.4 to 0.9 V. Values are given for 32 nm CNFETs based on Processes A and B with p_{Semi} = 100%. Results are based on 100 Monte-Carlo runs, error bars show standard deviations. Peak f_T and minimum NF_{min} are indicated together with the corresponding optimum biasing currents $I_{D,fT}$ and $I_{D,NFmin}$, respectively.

5.1.2 Influence of CNT array density

This work's technology predictions are made for the CNT array density $D = 100\,\mu m^{-1}$, which is in the same order of magnitude as the recently published target of $125\,\mu m^{-1}$ for processes in the year 2020 [60], but higher than today's maximum demonstrated density of $10\,\mu m^{-1}$ for arrays with controlled pitch [60]. To study the effect of D on device performance, the focus is again on the FoMs f_T and NF_{min}.

Fig. 5.2 shows that D has a significant impact on device speed. As already seen, the chosen density of $100\,\mu m^{-1}$ yields $f_T = 1.25$ THz. This is close to the maximum point of $f_T = 1.48$ THz at $D = 166\,\mu m^{-1}$ for a 68% higher overall drain current. Above this density, the onset of inter-CNT screening negatively affects the gate control over the

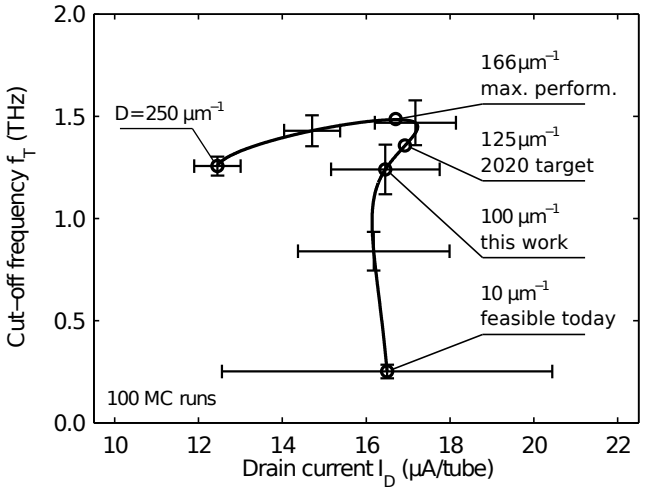

FIGURE 5.2: Cut-off frequency f_T vs. mean biasing current I_D for varying CNT array density D. Results are given for 32 nm CNFETs based on Process A with $p_\mathrm{Semi} = 100\%$, biased with $I_\mathrm{D,fT}$ and $V_\mathrm{DS} = 0.9\,\mathrm{V}$. Results are obtained from 100 Monte-Carlo runs, error bars show standard deviations at the points $D = [10\ 50\ 100\ 150\ 200\ 250]\ \mu\mathrm{m}^{-1}$.

channel. Therefore, a further increase of D would not be beneficial. Fig. 5.2 also reveals that today's processes cannot exploit the high-speed potential of CNFETs, because of a high penalty due to parasitic capacitances.

In contrast to f_T, NF_min is virtually not influenced by D and stays nearly constant at approximately 0.69 dB. This can be expected from the fact that the number of transistors in parallel connection does not alter the NF_min of an overall device. However, the changing parasitic load at the input affects the optimum input impedance required to obtain such NF_min.

5.1.3 Diameter and doping variability

The impact of the diameter distribution on device performance is huge. *E.g.*, CNFETs can already approach a respectable $f_\mathrm{T,peak}$ of 0.45 THz when growing CNTs with a diameter dispersion according to Process B. However, highest RF performance cannot be achieved, as the band gap of most of the grown CNTs is too high to be able to bias them efficiently. Only a small part of CNTs with large diameter carries the highest part of the overall drain current, while the other tubes are nearly or completely switched off. This results in a high parasitic capacitances with respect to the device's transconductance and a comparatively low performance. In contrast, synthesising CNTs according to Process A yields a large fraction of CNTs with significantly lower band gap, resulting

in a boost in performance. $f_{\mathrm{T,peak}}$ is increased by a factor of 2.78 up to 1.25 THz. Minimum NF_{min} at 300 GHz is behaving similarly. While with Process B it is higher than 1.51 dB, with Process A this value is reduced by a factor of 2.20 to only 0.687 dB. Error bars in Fig. 5.1 show the combined effect of diameter and doping level dispersion on the abovementioned FoMs and on the biasing current. Such dispersion is significant particularly in the case of Process B, but can be mitigated by increasing the device width and therefore the number of CNTs in the channel.

This analysis highlights the need for a tighter control of the CNT growth process. The CNT mean diameter has to be sufficiently high to avoid tubes that remain in the off-state during operation. Process A with its $\mu(d_{\mathrm{Tube}}) = 1.5\,\mathrm{nm}$ has shown to fulfil this requirement. In addition, diameter dispersion should be lower than what can be achieved with today's growth processes in order to avoid large variations of the CNFET's performance characteristics.

5.1.4 Metal tube removal and conduction type variability

mCNTs are a major obstacle for high performance, which is why a metal tube removal step has to be considered for high-performance CNFET manufacturing. Fig. 5.3 depicts a set of analog FoMs and their dependence on the efficiency of such a step.

High purity manufacturing processes (*e.g.* with the probability of sCNT growth $p_{\mathrm{Semi}} = 96\%$) yield a maximum f_{T} of 1.21 THz. With an increasing fraction of mCNTs, f_{T} decreases approximately linearly [inset Fig. 5.3.(a)]. For conventional tube growth processes (*e.g.* $p_{\mathrm{Semi}} = 67\%$) f_{T} is already degraded to 0.70 THz. A mCNT-removal step is not required for high-purity processes, but it has positive impact on the f_{T} of devices with lower p_{Semi} [Fig. 5.3.(a)]. However, even if all mCNTs grown by a conventional low-purity tube growth process are successfully removed, the performance of high-purity processes cannot be achieved, as the resulting inactive areas in the tube array lead to a higher parasitic capacitance per active tube. Unintentional removal of sCNTs degrades performance due to the same mechanism. E.g., assuming $p_{\mathrm{Semi}} = 96\%$ and inactivating 10% of the sCNTs leads to a reduction of f_{T} of about 6%.

The relation between p_{Semi} and NF_{min} is nearly linear [inset Fig. 5.3.(b)]. If a low-purity tube growth process is used, mCNT removal post-processing is required for optimized

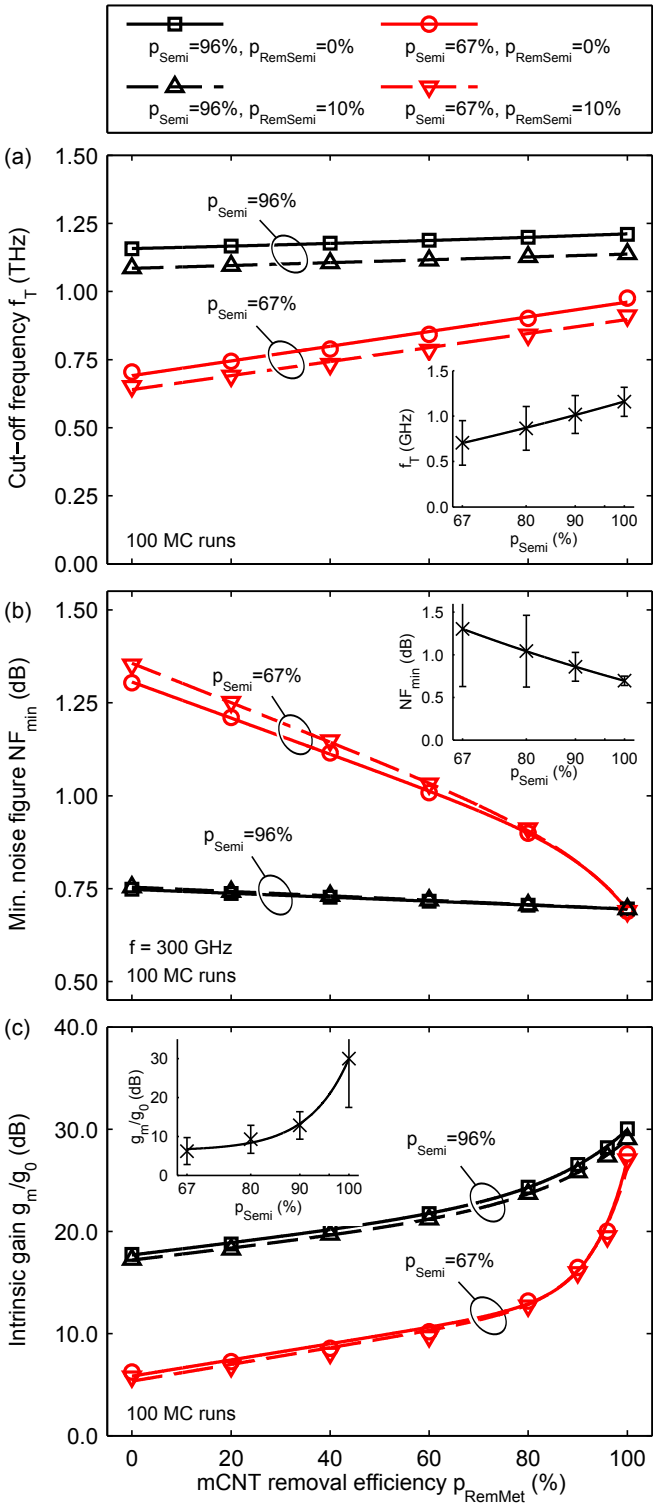

FIGURE 5.3: Impact of the efficiency of an mCNT removal process (p_{RemMet}), unintentionally also removing sCNTs (p_{RemSemi}), on (a) cut-off frequency f_{T}, (b) intrinsic gain g_{m}/g_0, and (c) minimum noise figure NF_{min}. Values are given for 32 nm CNFETs based on Process A with a varying amount of grown sCNTs (p_{Semi}). The insets show the effect of p_{Semi} on f_{T}, g_{m}/g_0 and NF_{min}, with error bars indicating standard deviation. Results are based on 100 Monte-Carlo runs. $I_{\mathrm{D}} = I_{\mathrm{D,fT}}$ and $V_{\mathrm{DS}} = 0.9\,\mathrm{V}$.

low-noise behavior [Fig. 5.3.(b)]. sCNT-removal has a negative impact on $NF_{\min}$ and is more pronounced for lower p_{Semi}.

The intrinsic gain g_{m}/g_0 is strongly affected by mCNT shunt resistances, as they substantially increase the intrinsically low g_0 of the CNFET with its tight electrostatic gate control over the 1-D channel. Therefore, an efficient metal tube removal process with the probability of mCNT removal p_{RemMet} approaching 100% is required in order to not only obtain speed, but also sufficient gain.

5.1.5 Noise behavior

To identify the noise sources with highest impact, the contributions of the individual noise sources to the overall output noise of a single-tube Level-1 CNFET have been analyzed (Fig. 5.4). Channel shot noise is dominant at low I_{D} per tube. With increasing I_{D} its importance decreases due to suppression and for $I_{\mathrm{D}} = 1.16\,\mu\mathrm{A}$ it is replaced by shot noise in the source extension region as the strongest noise source. Another noise mechanism of major importance is flicker noise. The number of charge carriers n in the channel of ballistic devices is very low and according to Eq. (4.5) this yields a high noise PSD. This is not a unique feature of the CNFET, but common to highly downscaled devices [155]. Even though for the CNFET under investigation the flicker noise has decayed to a low level at the frequency of interest of 300 GHz, the corner frequency

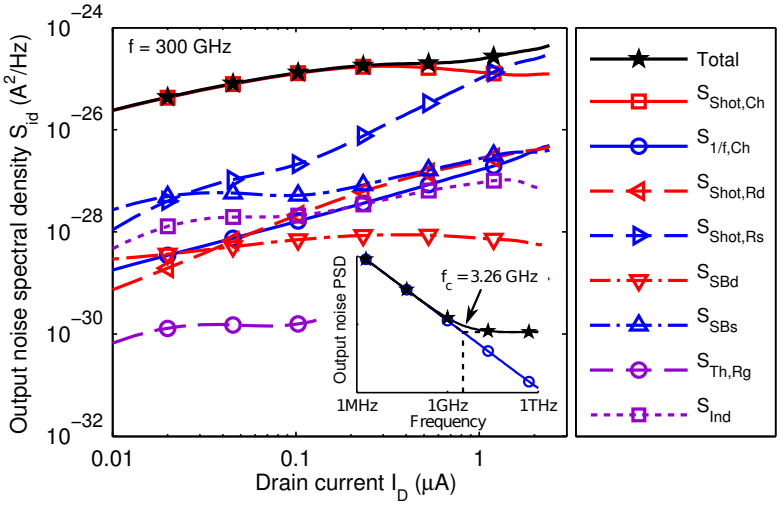

FIGURE 5.4: Contribution of the different noise sources to the total output noise PSD S_{id} of a 32 nm single-tube CNFET. Nominal process parameters apply. Biasing conditions are $I_{\mathrm{D}} = I_{\mathrm{D,fT}}$ and $V_{\mathrm{DS}} = 0.9\,\mathrm{V}$.

f_c, where contribution of flicker to overall noise is 50%, is as high as 3.26 GHz (inset Fig. 5.4). For amplifier circuits this may not be problematic, as they are likely to be operated significantly above f_c. However, circuits with noise up-conversion such as oscillators or mixers suffer performance degradation. Channel-induced gate noise plays a secondary role in terms of the total output noise PSD S_{id}. However, due to its partially uncorrelated nature with respect to the channel noise, it influences NF_{min}. Noise at the S/D Schottky barriers and thermal gate noise have a minor impact.

5.1.6 Global device performance overview

Table 5.1 lists a set of FoMs as mentioned in the ITRS RF-CMOS technology requirements [5], determined for the CNFET [CNTs based on Process A, $p_{Semi} = 100\%$, probability of sCNT removal $p_{RemSemi} = 0\%$; tube diameter variability ($\mu(d_{Tube}) = 1.5\,nm$, $\sigma(d_{Tube}) = 0.2\,nm$) and doping level molar fraction variability ($\mu(f_{Doping}) = 1\%$, $\sigma(f_{Doping}) = 0.1\%$) as indicated in Table 4.2]. The given results provide a global overview over the analog performance of this work's CNFET. The 32 nm CNFET technology node is taken as an example and its performance is contrasted with the predictions for multi-gate (MG) Si-CMOS for the year 2018. Furthermore, for every benchmark category the respective year is indicated when conventional MG Si-CMOS will outperform the 32 nm CNFET. This allows us to show the clear advantage of this novel technology in all benchmarked categories save flicker noise and intrinsic gain.

MG Si-CMOS will not reach the 32 nm CNFET's outstanding f_T before the year 2021. Peak f_{max} is extraordinarily high (as reported in [94]) and even outside the timeframe of ITRS predictions, which end in 2026. This high f_{max} performance is particularly due to the CNFET's low g_0. The maximum stable gain at 60 GHz MSG_{60} also performs well. Even though CNT diameter control is immature, threshold voltage matching shows good results. However, g_m/g_0 is low compared to the results presented in Fig. 5.3, as following ITRS definitions it is determined in the linear regime at 10% of the drain saturation current. Finally, noise shows a disparate picture. While NF_{min} is excellent, flicker noise is high and has to be taken into account when designing circuits with noise up-conversion.

Device downscaling yields performance improvements in all benchmark categories except flicker noise.

TABLE 5.1: CNFET device performance overview[1].

	f_T (GHz)	f_{max} (GHz)	NF_{min} (dB) @ 60 GHz	MSG_{60} (dB) @ 60 GHz
CNFET technology node				
22 nm	1704 (299)	9902 (643)	0.089 (0.005)	21.83 (0.361)
32 nm	1249 (117)	7672 (448)	0.141 (0.010)	20.66 (0.239)
45 nm	862 (50)	5838 (334)	0.254 (0.021)	19.46 (0.285)
65 nm	621 (38)	4008 (247)	0.484 (0.041)	17.81 (0.289)
Comparison Si-CNT				
MG Si-CMOS in 2018	890	755	0.55	16.9
MG Si-CMOS equality with 32 nm CNFET (year)	2021	>2026	>2026	>2026

	g_m/g_0 (-)	$1/f$ noise ($\mu V^2\,\mu m^2\,Hz^{-1}$)	σV_{th} match (mV µm)
CNFET technology node			
22 nm	28.59 (21.23)	115.5 (4.48)	1.72
32 nm	24.56 (16.97)	114.8 (3.00)	1.86
45 nm	23.04 (15.14)	114.3 (2.77)	2.21
65 nm	23.03 (15.78)	113.4 (2.50)	2.69
Comparison Si-CNT			
MG Si-CMOS in 2018	65	46.7	0.61
MG Si-CMOS equality with 32 nm CNFET (year)	<2011	<2011	2017

[1] Results are given as mean values (standard deviations between parantheses).

5.2 Performance of CNFET-based RF circuits

The RF performance study of the CNFET technology is in this section extended from the device level to basic RF circuits, using the same circuit simulation environment as in Sec. 5.1. This analysis focuses on two major analog building blocks: the LNA and the oscillator (Figs. 5.5 and 5.9), both indispensable for RF integrated circuits. Due to their different natures - externally driven amplifier versus autonomous circuit with noise up-conversion - their analysis covers wide aspects of the CNFET's high-speed analog behavior.

5.2.1 Low-noise amplifier

The task of a low-noise amplifier is to provide an amplified yet not distorted signal to subsequent signal processing blocks. Thus, notably noise, but also nonlinearities, have to be kept low. As wireless applications are a main system driver of today's SoCs, power consumption also has to be limited. According to the mixed-signal design roadmap [71] employed in the ITRS, a FoM covering these requirements can be stated as $FoM_{\mathrm{LNA}} = G \cdot IIP_3 \cdot f/((F-1)P)$ [71] (see Sec. 2.1.3.1). Here, G is the power gain, IIP_3 the input-referenced third-order intercept point, f the frequency, F the linear-scale noise figure, and P the power consumption. $G \cdot IIP_3$ can also be expressed as the output-referenced third-order intercept point OIP_3.

5.2.1.1 Low-noise amplifier circuit design

The LNA under investigation is a RF-CNFET in common-source configuration with an input matching network and power supply decoupling (Fig. 5.5). The CNFET's noise behavior is distinct to well known long-channel Si-CMOS [144], so commonly known LNA design flows [70], which simultaneously optimize gain, noise, and power, cannot straightforwardly be extended to the CNFET. For instance, the inductively degenerated LNA design method requires that the real part of the device's optimum impedance Z_{opt} needed for NF_{min} does not significantly change when varying the size of the source inductor, and the CNFET does not fulfil this condition. For that reason, the basic method of matching the input for NF_{min} to exploit the CNFET's excellent low-noise behavior has been applied in this work.

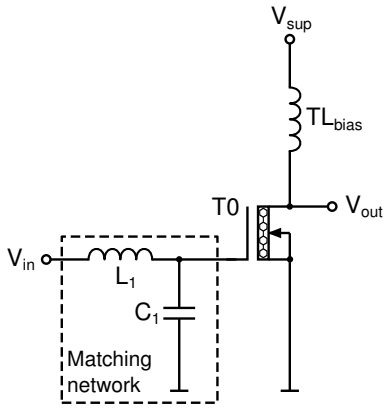

FIGURE 5.5: LNA with input matching network and a drain bias decoupling transmission line TL_{bias}, gate biasing is not shown. T0 is biased by $I_{D,fT}$ at a supply voltage of $V_{sup} = 0.9\,V$. It consists of 100 single-tube CNFETs (10 aligned CNTs based on Process A, $p_{Semi} = 100\%$ and $p_{RemSemi} = 0\%$; 10 gate fingers). In- and output voltages are indicated by V_{in} and V_{out}, respectively.

The design procedure can be summarized as follows:

1. For the investigations on the LNA's FoMs the maximum CNFET size allowed by the extended CNFET model has been chosen. The number of gate fingers N_{finger} and the number of tubes per CNFET N_{tube} have both been set to 10.

2. The device has been biased with $I_{D,fT}$ (see Table 5.2) to obtain the highest possible cut-off frequency $f_{T,peak}$.

3. An input matching circuit consisting of an ideal parallel matching capacitance C_1 and an ideal series matching inductance L_1 have been added to the input of the CNFET. Parametric analyses for several technology nodes and the two operation frequencies 300 and 600 GHz have been performed in order to determine the matching values, for which the required source impedance of Z_{opt} is presented to the input of the CNFET (see Table 5.2).

4. The circuit stability at the operating frequency has been guaranteed with source- and load-stability-circle analyses.

As an example for the behavior of a noise-matched CNFET-LNA, Fig. 5.6 shows the noise figure NF and the forward voltage gain $|S_{21}|$ of an LNA based on a 32 nm-CNFET. NF reaches a minimum value of 0.59 dB at the operating frequency $f = 300\,GHz$, while $|S_{21}|$ has a peak value of 7.43 dB close to this frequency. At 300 GHz, the circuit has input and output impedances of $|Z_{11}| = 11.3\,\Omega$ and $|Z_{22}| = 214\,\Omega$, respectively.

TABLE 5.2: Input matching circuit design for the CNFET-based LNAs.

Technology node (nm)	$I_{D,fT}$ (µA/tube)	C_1 (aF)	L_1 (pH)
Operating frequency $f = 300$ GHz:			
22	13.45	1535	153
32	17.48	1450	146
45	18.48	1480	138
65	15.60	1635	126
Operating frequency $f = 600$ GHz:			
22	13.45	1000	52.9
32	17.48	895	50.5
45	18.48	885	48.4
65	15.60	970	44.5

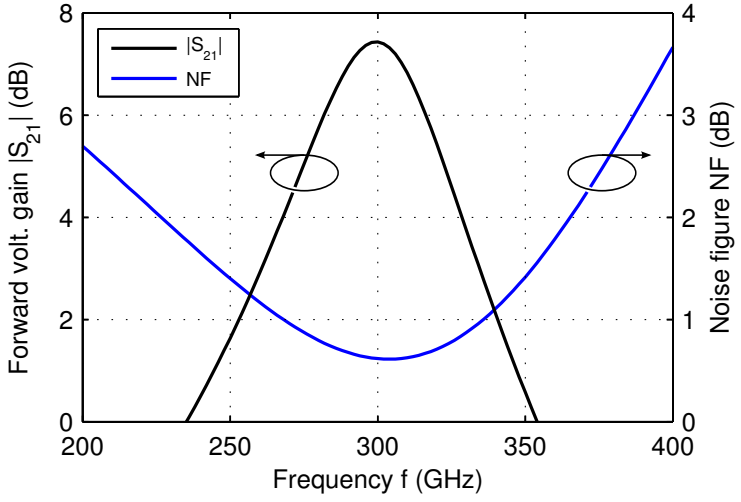

FIGURE 5.6: Forward voltage gain $|S_{21}|$ and noise figure NF vs. frequency f for the designed 300 GHz-LNA based on a nominal 32 nm-CNFET.

5.2.1.2 Low-noise amplifier performance analysis

FoM_{LNA} has been determined for a number of technology nodes at the operating frequencies 300 and 600 GHz (see Tables 5.3 and 5.4 for nominal and Monte-Carlo results, respectively). Fig. 5.7 shows the LNA performance as a function of f. Although the CNFET-based LNA has a simple circuit topology, its performance in terms of FoM_{LNA} lies in the region of the most advanced Si-CMOS LNAs. Furthermore, with CNFETs good performance values can be achieved for much higher operating frequencies f than with Si-CMOS, which today hardly exceeds about 100 GHz. *E.g.*, a CNFET-based LNA at the 32 nm node used at 300 GHz shows mean values of $G = 17.93\,\mathrm{dB}$, $NF = 0.713\,\mathrm{dB}$, $P = 1.46\,\mathrm{mW}$, and $OIP_3 = -10.10\,\mathrm{dBm}$, yielding $FoM_{\mathrm{LNA}} = 119.7\,\mathrm{GHz}$.

Fig. 5.8 depicts the scaling trend of LNAs based on CNFETs. A shrinkage from the 65 to the 22 nm node multiplies FoM_{LNA} by a factor of 7.5. However, at smaller technology nodes the improvements of the noise behaviour and gain are partially compensated by an onset of more nonlinearity.

CNT diameter variability has a strong impact on LNA performance, amongst others due to the sensibility of the CNFET's noise figure for input mismatching, as the input matching network is optimized for nominal process values. Monte-Carlo simulations show, that process variations reduce the mean FoM_{LNA} by about 13%. Furthermore, regarding the standard deviations of FoM_{LNA} in Figs. 5.7 and 5.8 shows the uncertainty in performance of individual CNFET-based LNA samples.

TABLE 5.3: Performance of the CNFET-based LNAs (nominal process parameters).

Technology node (nm)	NF (dB)	G (dB)	OIP_3 (dBm)	P (mW)	FoM_{LNA} (GHz)
Operating frequency $f = 300\,\mathrm{GHz}$:					
22	0.395	22.92	-14.33	1.213	95.84
32	0.590	21.67	-10.35	1.576	120.69
45	1.055	14.25	-8.652	1.665	89.38
65	1.942	8.646	-8.510	1.406	53.33
Operating frequency $f = 600\,\mathrm{GHz}$:					
22	0.777	13.59	-15.89	1.213	65.05
32	1.170	12.86	-12.07	1.576	76.45
45	1.985	7.771	-11.15	1.665	47.72
65	3.385	3.165	-7.632	1.406	62.37

TABLE 5.4: Performance of the CNFET-based LNAs (Monte-Carlo results)[1].

Technology node (nm)	NF (dB)	G (dB)	OIP_3 (dBm)	P (mW)	FoM_{LNA} (GHz)
Operating frequency $f = 300\,\mathrm{GHz}$:					
22	0.476 (0.069)	21.60 (1.752)	-11.63 (1.853)	1.153 (0.098)	169.8 (88.21)
32	0.713 (0.063)	17.93 (1.440)	-10.10 (1.247)	1.460 (0.113)	119.7 (50.06)
45	1.263 (0.093)	11.95 (0.783)	-8.784 (1.040)	1.555 (0.117)	80.68 (39.49)
65	2.208 (0.143)	6.802 (0.753)	-13.18 (1.860)	1.306 (0.100)	18.84 (11.05)
Operating frequency $f = 600\,\mathrm{GHz}$:					
22	0.920 (0.120)	12.77 (0.901)	-12.82 (1.848)	1.153 (0.098)	126.2 (58.45)
32	1.372 (0.107)	10.53 (0.993)	-10.87 (2.311)	1.482 (0.117)	97.34 (34.53)
45	2.333 (0.156)	5.878 (0.664)	-10.57 (5.811)	1.555 (0.117)	68.19 (45.43)
65	3.816 (0.222)	1.600 (0.636)	-12.50 (1.766)	1.306 (0.100)	20.72 (14.53)

[1] Results are given as mean values (standard deviations between parantheses).

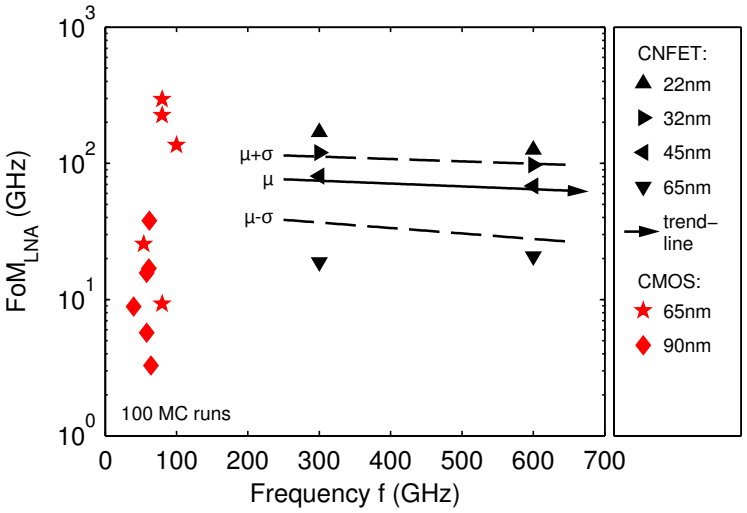

FIGURE 5.7: LNA performance FoM_{LNA} mean value vs. frequency f. This work's CNFET technology is compared to Si-CMOS LNAs (reported in [156–158] and referenced in [156,158]). The trendline shows the frequency scaling behavior of the CNFET technology. Process variations are indicated by trendline fitting for FoM_{LNA} mean values (μ) and mean values ± standard deviations ($\mu \pm \sigma$). Results are based on 100 Monte-Carlo runs.

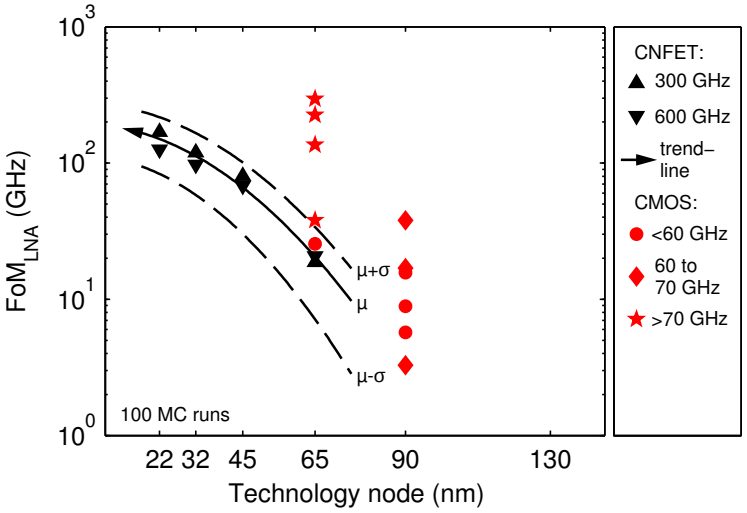

FIGURE 5.8: LNA performance FoM_{LNA} vs. technology node. This work's CNFET technology is compared Si-CMOS LNAs (references as above). The trendline shows the technology node scaling of the CNFET technology. Process variations are indicated as above.

5.2.2 Oscillator

The key performance issue of a voltage-controlled oscillator (VCO) is to provide stable oscillations, *i.e.*, with low phase noise. A common way of characterizing such performance is the VCO-FoM reported in [71]: $FoM_{\mathrm{VCO}} = (f_0/\Delta f)^2/(\mathrm{L}\{\Delta f\}\,P)$, where f_0 is the oscillation frequency and $\mathrm{L}\{\Delta f\}$ the phase noise PSD in a 1 Hz band at the frequency offset Δf. P is the power consumption in mW (see Sec. 2.1.3.3).

5.2.2.1 Oscillator circuit design

The topology under investigation is a differential LC-tank oscillator [72] (Fig. 5.9). The quality factor of the resonator is a crucial parameter for an oscillator as it affects phase noise and determines the losses to be compensated by the transistor pair. In order to guarantee realistic simulations, the tank inductance L_{tank} has been implemented using microstrip transmission lines provided by a commercial 65 nm CMOS technology (see Fig. 5.10).

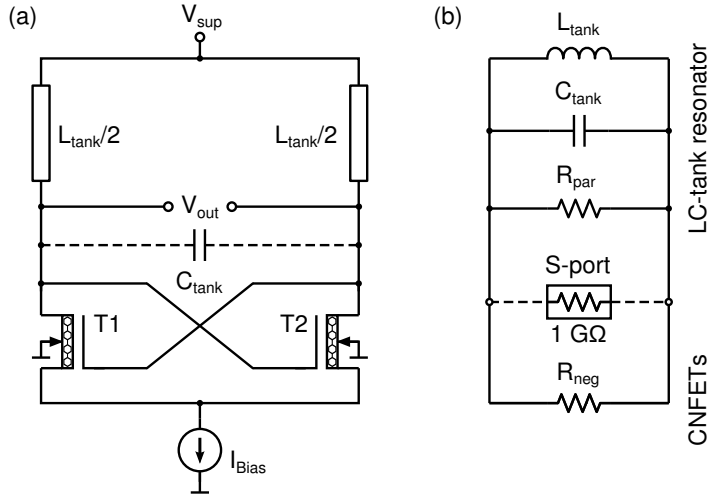

FIGURE 5.9: (a) Differential LC-tank oscillator with microstrip transmission lines $L_{\mathrm{tank}}/2$ and the CNFETs' capacitances (summarized as C_{tank}) forming the resonator. The supply voltage is $V_{\mathrm{sup}} = 0.9\,\mathrm{V}$. T1 and T2 are based on Process A and their size is chosen to compensate ohmic losses. The output voltage is indicated by V_{out}. (b) Equivalent circuit of the LC-tank resonator with an equivalent parallel resistance R_{par} representing ohmic losses, which are compensated by a negative resistance R_{neg} generated by the differential pair. Also shown is a high-impedance S-parameter port to measure the circuit's overall parallel resistance R_{tot}.

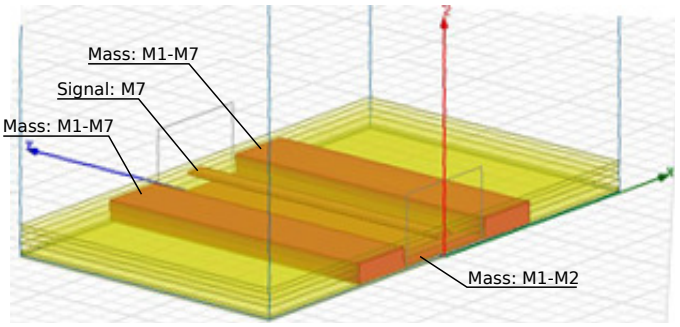

FIGURE 5.10: View of the microstrip transmission line used for the oscillator's tank inductance. The strip is 5 µm wide and realized at metal layer M7. It is localized between two mass walls, that are both at 7 µm distance and span from M1 to M7. The metal layers M1 and M2 form a mass plane.

The lossy LC-tank can be represented by a parallel resonance circuit that includes an equivalent parallel resistance R_{par} [Fig. 5.9.(b)]. Its resonance frequency is approximately

$$f_0 \approx \frac{1}{2\pi\sqrt{L_{\mathrm{tank}}C_{\mathrm{tank}}}} \,. \tag{5.1}$$

In order to generate oscillations, the CNFETs of the differential pair have to generate a negative resistance

$$R_{\mathrm{neg}} = -\frac{2}{g_{\mathrm{m}}} \,, \tag{5.2}$$

which must be sufficiently low to fulfil the oscillation condition $R_{\mathrm{par}}/|R_{\mathrm{neg}}| \geq 1$. In order to secure the start-up of the oscillator, this condition has been tightened to

$$\frac{R_{\mathrm{par}}}{|R_{\mathrm{neg}}|} \geq A \,, \tag{5.3}$$

with the start-up factor $A = 2$.

Combining Eqs. (5.2) and (5.3) with the overall parallel resistance at resonance $R_{\mathrm{tot}} = 1/(1/R_{\mathrm{par}} + 1/R_{\mathrm{neg}})$ yields an equation that allows to evaluate the start-up factor when knowing g_{m} and R_{tot}:

$$A = \frac{g_{\mathrm{m}}}{2} \cdot \frac{1}{\frac{g_{\mathrm{m}}}{2} + \frac{1}{R_{\mathrm{tot}}}} \,. \tag{5.4}$$

With the aid of this expression, the following algorithm to design the oscillator circuit has been applied (see Fig. 5.11):

1. The biasing current per tube $I_{\mathrm{gm,opt}}$ for the CNFET's maximum transconductance per tube $g_{\mathrm{m,opt}}$ is determined and the biasing current source is set to $I_{\mathrm{Bias}} = 2N_{\mathrm{finger}}N_{\mathrm{tube}}I_{\mathrm{gm,opt}}$.

2. The microstrip length is chosen such that yields the desired f_0.

3. The start-up factor A is determined by evaluating Eq. (5.4). For that purpose, the transconductance is given as $g_{\mathrm{m}} = N_{\mathrm{finger}}N_{\mathrm{tube}}g_{\mathrm{m,opt}}$ and R_{tot} is measured with a high-impedance S-parameter probe. If A is sufficiently close to 2, the circuit design process is completed.

4. If $A \neq 2$, the CNFET size is increased/decreased by varying N_{finger} and N_{tube} to correct a too low/high A . I_{Bias} is then adapted to the new size.
   A change of the microstrip length influences R_{par}, which requires to alter the transistor size in order to provide $A = 2$. However, the transistor size influences C_{tank} and requires a readaptation of the microstrip length in order to obtain the desired f_0. Therefore, steps 2) to 4) have to be repeated to iteratively approach A and f_0 to the desired values.

Tables 5.5 and 5.6 show the results of this design process for the analyzed technology nodes and oscillation frequencies. For instance, 32 nm-CNFETs used for a 300.0 GHz-oscillator show a $g_{\mathrm{m,opt}} = 43.55\,\mu\mathrm{S/tube}$ for a biasing current $I_{\mathrm{gm,opt}} = 15.74\,\mu\mathrm{A/tube}$. It has been determined that 25 single-tube elements ($N_{\mathrm{finger}} = 5$, $N_{\mathrm{tube}} = 5$) in combination with microstrips with a length of 108.7 µm yield both the desired oscillation frequency $f_0 = 300\,\mathrm{GHz}$ and a sufficiently high start-up factor A. The given CNFETs provide the

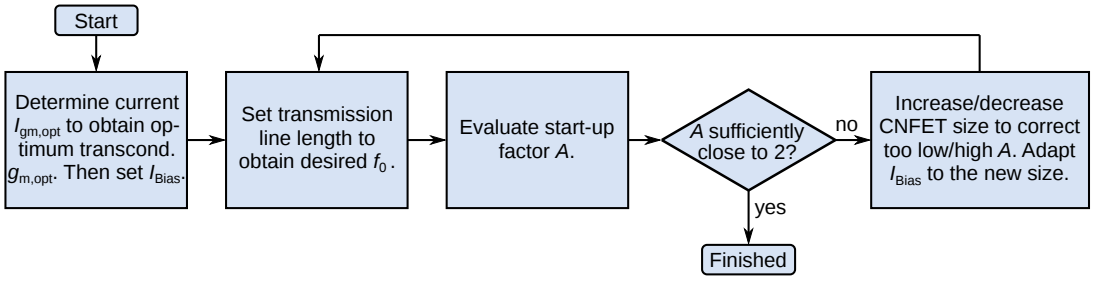

FIGURE 5.11: Oscillator design algorithm.

negative resistance $R_{\mathrm{neg}} = -2/(N_{\mathrm{finger}} N_{\mathrm{tube}} g_{\mathrm{m,opt}}) = -1837\,\Omega$, which with the measured total parallel resistance $R_{\mathrm{tot}} = -3839\,\Omega$ gives a parasitic resistance $R_{\mathrm{par}} = 3523\,\Omega$, resulting in $A = R_{\mathrm{par}}/|R_{\mathrm{neg}}| = 1.92 \approx 2$.

TABLE 5.5: CNFET-based oscillator design - Transistor characteristics.

Technology node (nm)	N_{finger}	N_{tube}	$g_{\mathrm{m,opt}}$ (µS/tube)	$I_{\mathrm{gm,opt}}$ (µA/tube)	f_{T} (GHz) @ $I_{\mathrm{gm,opt}}$	f_{max} (GHz) @ $I_{\mathrm{gm,opt}}$
Target oscillation frequency $f_0 = 300\,\mathrm{GHz}$:						
22	4	5	53.56	21.00	1799	2971
32	5	5	43.55	15.74	1342	2907
45	5	6	38.50	18.66	973	1755
65	7	7	31.92	16.10	671	948
Target oscillation frequency $f_0 = 600\,\mathrm{GHz}$:						
22	3	4	53.56	21.00	1799	3016
32	4	4	43.55	15.74	1342	2974
45	5	6	38.50	18.66	973	1755
65	10	10	31.92	16.10	671	891

TABLE 5.6: CNFET-based oscillator design - Microstrip characteristics, oscillation frequency, and compensation of the parasitic tank resistance.

Technology node (nm)	L_{line} (µm)	W_{line} (µm)	f_0 (GHz)	R_{tot} (Ω) @ f_0	A (-)
Target oscillation frequency $f_0 = 300\,\mathrm{GHz}$:					
22	109.0	5.0	300.2	-3721	2.01
32	108.7	5.0	300.0	-3839	1.92
45	107.7	5.0	299.9	-3601	1.93
65	104.0	5.0	299.9	-2739	1.88
Target oscillation frequency $f_0 = 600\,\mathrm{GHz}$:					
22	54.3	5.0	600.3	-5874	2.13
32	54.1	5.0	599.7	-5553	2.07
45	52.3	5.0	599.7	-3338	2.08
65	44.0	5.0	-	-4000	1.19

5.2.2.2 Oscillator performance analysis

The performance of the eight designed CNFET-based oscillators has been determined (see Table 5.7). They show superior performance in terms of FoM_{VCO} when compared to Si-CMOS (Figs. 5.12 and 5.13). This is partly due to the CNFET-oscillators' high f_0, achievable even with the employed simple circuit topology working at the fundamental wave. In addition, the oscillators have low phase noise and a low power consumption. *E.g.*, a 300 GHz oscillator realized with a 32 nm CNFET-technology has an $\mathrm{L}\{100\,\mathrm{MHz}\} = -129\,\mathrm{dBc}$ for $P = 10.5\,\mathrm{mW}$. However, flicker noise up-conversion increases the phase noise in the proximity of f_0 up to a corner-frequency of about 10 MHz.

The CNFET-based oscillator scales positively with f_0, while using Si-CMOS it gets challenging to achieve good performance at high frequency. Furthermore, to achieve an f_0 of several hundred GHz, Si-CMOS-based VCOs already rely on advanced circuit topologies such as the push-push and triple-push oscillator working at the second or third harmonic, respectively.

Mostly because of noise reduction, CNFET scaling yields good results at least down to the 22 nm node. In contrast, Si-CMOS scaling decreases performance (Fig. 5.13).

Table 5.7: Performance of the CNFET-based oscillators.

Technology node (nm)	f_0 (GHz)	P (mW)	$\mathrm{L}\{100\,\mathrm{MHz}\}$ (dBc)	FoM_{VCO} (dB)
Target oscillation frequency $f_0 = 300\,\mathrm{GHz}$:				
22	300.2	13.90	-130.9	189.1
32	300.0	10.51	-129.3	188.6
45	299.9	12.69	-125.9	184.4
65	299.9	8.33	-119.6	179.9
Target oscillation frequency $f_0 = 600\,\mathrm{GHz}$:				
22	600.3	14.16	-127.9	192.0
32	599.7	9.43	-124.2	190.0
45	599.7	7.52	-117.6	184.4
65	-	-	-	-

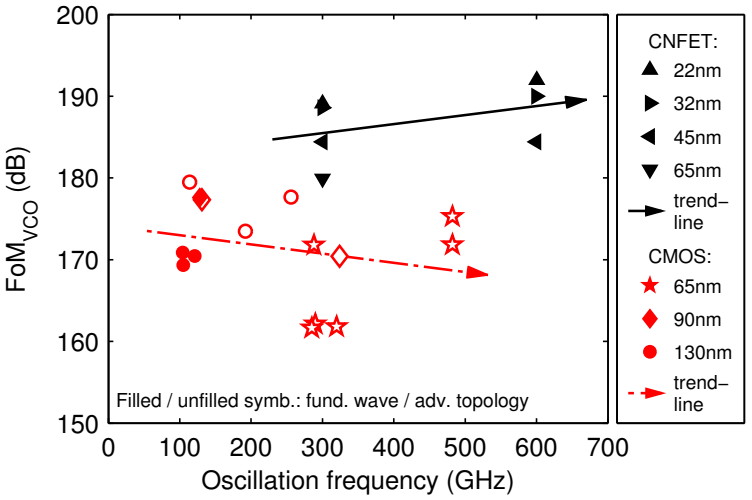

FIGURE 5.12: Oscillator performance FoM_{VCO} vs. oscillation frequency f_0. Values are given for this work's CNFET technology and Si-CMOS VCOs (reported in [159–164] and referenced in [159]). Nominal process parameters apply. Si-CMOS references are classified in circuit topologies working with the fundamental wave (filled symbols) and harmonics (unfilled symbols). Trendlines indicate the frequency scaling behavior of the technologies.

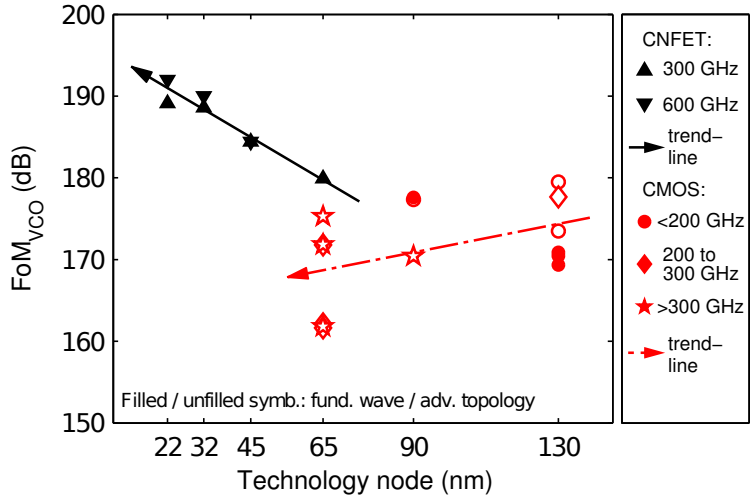

FIGURE 5.13: Oscillator performance FoM_{VCO} vs. technology node. As above, values are given for this work's CNFET technology and Si-CMOS VCOs (references as above). Nominal process parameters apply. Si-CMOS references are classified in circuit topologies as above. Trendlines indicate the technology node scaling of the technologies.

5.3 Conclusion

In this chapter a detailed simulation study of the CNFET technology's RF behaviour has been provided both at the device and circuit level. The performed simulations have been based on the variability and noise models presented in Chapter 4.

It has been shown that the assumed CNFET technology can outperform MG Si-CMOS in most ITRS RF-CMOS benchmark categories (*i.e.* f_{T}, f_{max}, NF_{min}, MSG_{60}, σV_{th} match). For these device-level FoMs the CNFET technology has years of performance advantage over Si-CMOS, and good scalability shows promise for maintaining this advantage once having arrived at the market. One weak point is high flicker noise, which yet is inherent to highly scaled devices with a low number of charge carriers in the channel. It indicates the need for optimized manufacturing methods with a low Hooge's constant α_{H}.

The design of CNFET-based LNAs and oscillators has been discussed. In continuation, circuit-level FoMs for these RF building blocks have been determined and allow the following insights: 1) Simple CNFET-based LNA topologies are already competitive with the most advanced CMOS designs in terms of FoM_{LNA}. 2) CNFET oscillators clearly outperform their silicon counterparts regarding FoM_{VCO}. 3) By using CNFETs very high operating frequencies can easily be achieved.

These promising results rely on a tube growth process with a well-behaving CNT diameter distribution, a sufficiently high CNT array density, and a diminishing percentage of mCNTs, while unoptimized growth processes result in performance penalties.

In summary, the CNFET is predicted to outperform Si-CMOS in RF applications, a field which has become a main driving force for the semiconductors industry. This encourages the improvement of today's CNFET manufacturing technologies up to market insertion, as carbon nanotubes may enable a future high-performance low-cost SoC scenario.

Chapter 6

An accurate and Verilog-A compatible compact model for graphene field-effect transistors

THE GROWING INTEREST in graphene electronics results in a demand for accurate GFET compact models, but a challenge in model development is to combine the opposed requirements of 1) predicting device properties with high accuracy in all operation regions and 2) a sufficiently simple mathematical description that allows a model's implementation in existing circuit design environments using hardware description languages (HDL) such as Verilog-A. This chapter is dedicated to the development of such an accurate nonetheless easily implementable GFET compact model.

Pioneering work in analytical GFET modeling has been done by Meric *et al.* [105]. Further research yielded not only deeper insight into physics-based modeling methods [165,166], but also a number of closed-form analytical descriptions [137,138,167–172] that can readily be implemented as compact models. Moreover, a model for hand-calculation-based circuit design has been reported [173]. However, these models depend to varying extent on simplifications of several physical elements: i) quantum capacitance, ii) charge carrier density, iii) electrostatics of the capacitive gate voltage divider, and iv) saturation velocity. This yields inaccuracy particularly in the vicinity of the Dirac point, *i.e.*, for a small absolute value $|V_c|$ of the channel potential. As a consequence, under certain

biasing conditions analog properties such as the drain current I_{D}, transconductance g_{m}, or output conductance g_0 are altered, which can severely affect the outcome of graphene circuit design.

In this chapter, first the characteristics of the four abovementioned common simplifications in GFET modeling are discussed (Sec. 6.1). Then, a GFET model with high accuracy also for small $|V_{\mathrm{c}}|$ is developed, which nonetheless can be implemented using HDLs. The proposed drain-source current model is for single-layer zero-bandgap graphene and a horizontal double-gate structure. It assumes drift-diffusion transport and features the following physical parameters: oxide capacitance, quantum capacitance, carrier mobility, velocity saturation due to optical phonon scattering, and additional mobile charges due to electron-hole puddles (Sec. 6.2). A complete Verilog-A version is available in Appendix C. Subsequently, the accuracy of this work's model is compared with a representative model available in literature [137,138,165,171]. In continuation, a comprehensive error analysis of both model types is provided (Sec. 6.3). The model developed in this chapter is then validated by comparing it to experimental results [174–176] (Sec. 6.4). As an application example, the DC characteristics of the GFET are analyzed (Sec. 6.5). Finally, conclusions are drawn (Sec. 6.6).

6.1 Modeling aspects affecting accuracy

This work's approach to obtain a highly accurate GFET drain current equation consists on minimizing the simplifications of the graphene quantum capacitance, the charge density relevant for drain-current calculations, the charge stored in voltage-dependent capacitors, and the channel-potential-dependency of the graphene saturation velocity, while at the same time keeping in mind that the analytical formulation has to be compatible with HDLs. The four abovementioned modeling aspects are described in the next subsections.

6.1.1 Quantum capacitance

The quantum capacitance C_{q} describes the intrinsic charge storage of a material excited by a small-signal electric potential [75]. C_{q} is in series with the geometric gate capacitance and as in graphene C_{q} is low, its high reactance has a significant impact on the

overall gate capacitance.

C_q depends on the channel potential V_c, which is defined as the difference between the potential V at the quasi-Fermi level[1] $E_\mathrm{F} = -qV$ and the potential $V - V_\mathrm{c}$ at the Dirac point[2] energy $E_\mathrm{DP} = -q(V - V_\mathrm{c})$ [Fig. 6.1.(a)]. The band diagram of the intrinsic device [Fig. 6.1.(b)] illustrates the quasi-Fermi level and the Dirac point energy as a function of the horizontal space coordinate [177]. The relation between C_q and V_c is shown in Fig. 6.2.(a). It is beneficial to assume C_q as being proportional to $|V_\mathrm{c}|$, as this considerably simplifies gate electrostatics. This absolute-value approximation of C_q has been frequently used in previous work [137, 138, 165–167, 171], but is only valid for $q|V_\mathrm{c}| \gg k_\mathrm{B}T$, where q is the elementary charge, k_B the Boltzmann constant, and T the absolute temperature. In order to guarantee high accuracy, at room temperature conditions $|V_\mathrm{c}|$ must be significantly higher than 25.8 mV.

In the vicinity of the Dirac point (*i.e.*, for $q|V_\mathrm{c}| \ll k_\mathrm{B}T$) the abovementioned condition does not hold true, resulting in considerable modeling error. Parrish *et al.* [169] have shown that significant accuracy improvements can be achieved in this operation region

[1] In a semiconductor in equilibrium, the probability that an electron occupies an energy state E is given by the Fermi function $\mathrm{f}_0(E_\mathrm{F}) = 1/[1 + \exp((E - E_\mathrm{F})/(k_\mathrm{B}T))]$, where E_F is the Fermi level, k_B the Boltzmann constant, and T the absolute temperature. E_F marks the energy level, whose available states are occupied to 50%. E_F can be influenced by external electrostatic fields such as introduced by a gate electrode. If the semiconductor is in non-equilibrium (*i.e.*, an external voltage/current source causes a potential drop and electrons flow), E_F changes along the length of the semiconductor. The E_F at a certain point is then called quasi-Fermi level.

[2] The Dirac point is the energy level of graphene's energy dispersion relation, where the conduction and valence band touch (see Sec. 2.3.1.2). Around the Dirac point the energy dispersion can be approximated as linear [see Figs. 2.19 and 6.1.(a)].

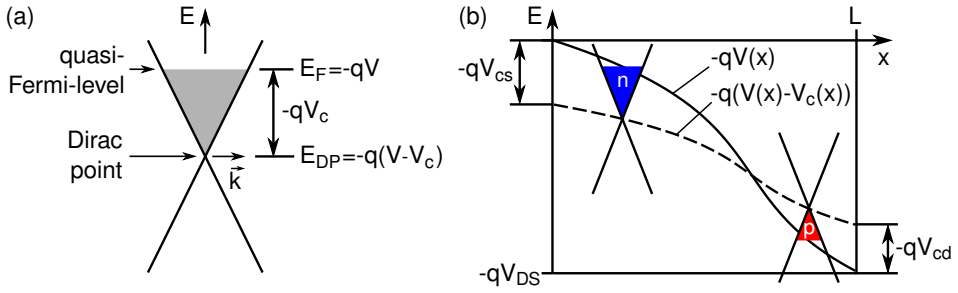

FIGURE 6.1: (a) E-$\vec{k}$ energy-dispersion relation of graphene, showing the potential definitions employed in this work. $E_\mathrm{F} = -qV$ is the quasi-Fermi-level energy, $E_\mathrm{DP} = -q(V - V_\mathrm{c})$ is the energy at the Dirac point [177]. (b) Schematical band-diagram of the intrinsic device [177]: Energy E vs. position x. The quasi-Fermi-level $-qV(x)$ and the energy at the Dirac point $-q(V(x) - V_\mathrm{c}(x))$ are shown. V is the voltage drop in the channel, V_c the channel potential, and V_cd and V_cs are the channel potentials at the drain and source side, respectively, and q is the elementary charge. Two Dirac cones illustrate the mixed n/p-type channel of this example.

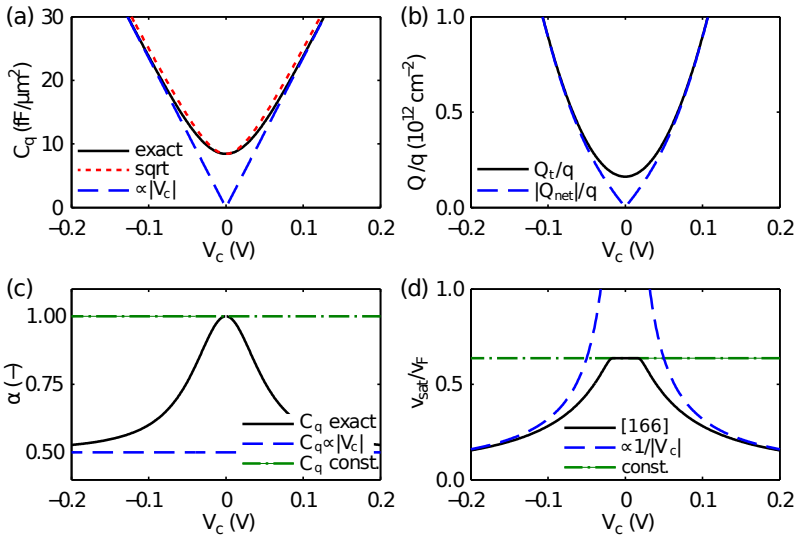

FIGURE 6.2: Modeling aspects affecting accuracy: (a) Quantum capacitance C_q vs. channel potential V_c: exact C_q, square root-approximation, and absolute value approximation $C_\mathrm{q} \propto |V_\mathrm{c}|$ (b) Transport sheet carrier density Q_t/q and absolute value of the net mobile sheet carrier density $|Q_\mathrm{net}|/q$ vs. V_c (c) Capacitance weighting factor α vs. V_c, given for the exact C_q description, $C_\mathrm{q} \propto |V_\mathrm{c}|$, and a constant C_q (d) Ratio of saturation velocity to Fermi velocity $v_\mathrm{sat}/v_\mathrm{F}$ vs. V_c: as in [166], for $v_\mathrm{sat} \propto |V_\mathrm{c}^{-1}|$, and constant.

with a C_q approximation based on a square-root function $C_\mathrm{q} \propto \sqrt{1 + c_\mathrm{c}^2 V_\mathrm{c}^2}$, where c_c is a constant.

Within this work gate electrostatics are based on the exact description of C_q, whereas the low-field drain current expressions are derived using the accurate, but not exact square-root approximation.

6.1.2 Charge density relevant for transport

Gate electrostatics are usually evaluated by comparing the charge density at the gate electrode to the net mobile sheet charge density $Q_\mathrm{net} = q(p - n)$, which expresses the difference between the hole and electron densities p and n induced in the graphene channel. The use of Q_net is frequently extended from gate electrostatics to drain current calculations [137,138,165,171,172] by describing the drain current density as $J_\mathrm{D} = Q_\mathrm{net} v$, with v being the carrier velocity. However, this approach gives satifying results only for $q|V_\mathrm{c}| \gg k_\mathrm{B}T$, as the charge carrier density due to thermal excitation is underestimated close to the Dirac point [Fig. 6.2.(b)].

This drawback can be overcome by using the transport sheet charge density $Q_\mathrm{t} = q\,(p+n)$ for drain current calculations [166, 169, 177, 178], following the fact that in the zero-bandgap material graphene the holes and electrons additively contribute to the overall current. Q_t shows a residual charge density for small $|V_\mathrm{c}|$ and converges to Q_net for $q|V_\mathrm{c}| \gg k_\mathrm{B}T$ [Fig. 6.2.(b)].

This work follows the approach of employing Q_net for calculations on gate electrostatics and Q_t for deriving the drain current equations.

6.1.3 Charge-voltage relation of voltage-dependent capacitors

The charge stored in a voltage-dependent capacitor $C(\tilde{V})$ is described as $Q = \int C(\tilde{V})\mathrm{d}\tilde{V}$. Only for the trivial case of constant C, this relation reduces to $Q = C\tilde{V}$. For a more general voltage-dependency such as in the case of graphene's C_q, the charge-voltage relation can be evaluated by introducing a capacitance weighting factor $\alpha(\tilde{V})$, yielding $Q = \alpha C\tilde{V}$. Neglecting this factor overestimates C_q's impact on gate electrostatics. For the frequently used absolute-value approximation $C_\mathrm{q} \propto |V_\mathrm{c}|$ the weighting is $\alpha = 1/2$ [137, 138, 165, 166, 171, 172]. In the case of constant C it is $\alpha = 1$.

In this work a transition from $\alpha = 1$ for $q|V_\mathrm{c}| \ll k_\mathrm{B}T$ to $\alpha = 1/2$ for $q|V_\mathrm{c}| \gg k_\mathrm{B}T$ is implemented [Fig. 6.2.(c)], which corresponds to the exact C_q-vs.-V_c relation.

6.1.4 Saturation velocity model

Fig. 6.2.(d) shows common models of the V_c-dependent graphene saturation velocity v_sat. Close to the Dirac point v_sat can be approximated as constant. For higher V_c it has been found to follow the relation $v_\mathrm{sat} \propto |V_\mathrm{c}^{-1}|$ [105]. However, this latter description is not valid around the Dirac point, as at zero V_c it has a singularity. In this operation region the model of [105] is therefore in contradiction with the physical limit of the carrier velocity in graphene, which is the Fermi velocity[3] v_F. Ref. [166] presents an alternative v_sat description, which is used in this work and covers the whole V_c range by splitting it into a constant and an energy-dependent region.

[3]The Fermi velocity is defined as $v_\mathrm{F} = (1/\hbar) \cdot (\mathrm{d}E/\mathrm{d}k)$ evaluated at the Fermi level [75]. $\hbar$ is the reduced Planck constant, E is the energy, and k the wave vector. In graphene, v_F is approximately $1 \times 10^6\,\mathrm{m\,s^{-1}}$.

TABLE 6.1: Overview of approximations affecting the accuracy of existing compact models and comparison to this work.

GFET model	C_q-approx. electro-stat./transp.	Distinction Q_{net}, Q_t	Electrostat. incl. α	v_{sat} model
[165]	$\propto \lvert V_c \rvert$	no	yes	$\propto \lvert V_c^{-1} \rvert$
[166]	$\propto \lvert V_c \rvert$	yes	yes	2 regions
[137]	$\propto \lvert V_c \rvert$	no	yes	constant
[138]	$\propto \lvert V_c \rvert$	no	yes	$\propto \lvert V_c^{-1} \rvert$
[167]	$\propto \lvert V_c \rvert$	-	-	$\propto \lvert V_c^{-1} \rvert$
[168]	-	-	-	$\propto \lvert V_c^{-1} \rvert$
[169]	$\propto \sqrt{1 + c_c^2 V_c^2}$	yes	no	-
[170]	-	-	-	$\propto \lvert V_c^{-1} \rvert$
[171]	$\propto \lvert V_c \rvert$	no	yes	$\propto \lvert V_c^{-1} \rvert$
[172]	$\propto \lvert V_c \rvert + const.$	no	yes	$\propto \lvert V_c^{-1} \rvert$
This work	C_q exact and $\propto \sqrt{1 + c_c^2 V_c^2}$	yes	yes	2 regions

As a summary of this section, the various GFET models found in literature and a comparison with the approach used in this work are provided in Table 6.1.

6.2 An accurate GFET drain-current model

In this section an accurate drain-current model for intrinsic GFET devices is presented (Fig. 6.3), following the specifications summarized at the bottom of Table 6.1. First a HDL-implementable solution for the channel potential V_c is proposed. Then, closed-form analytical expressions for the drain-current and the impact of velocity saturation are derived.

6.2.1 Electrostatics

6.2.1.1 Implicit channel potential equation

In the following the equivalent capacitive circuit shown in Fig. 6.4 is evaluated to obtain the channel potential V_c. The net voltages at the top- and back-gate are represented as $V'_{GS} = V_{GS} - V_{GS,0}$ and $V'_{BS} = V_{BS} - V_{BS,0}$, respectively [165]. V_{GS} and V_{BS} are the gate

voltages applied at the intrinsic terminals, $V_{\mathrm{GS},0}$ and $V_{\mathrm{BS},0}$ are constants representing the gate voltages at the point of minimum drain current. These constants account for the metal-graphene workfunction difference, possible interface states at the graphene-oxide interface, as well as optional doping of the graphene.

V'_{GS} and V'_{BS} induce a net mobile sheet charge density $Q_{\mathrm{net}} = q\,(p-n)$ in the channel:

$$Q_{\mathrm{net}} = \frac{2q\,(k_{\mathrm{B}}T)^2}{\pi\,(\hbar v_{\mathrm{F}})^2}\left(\mathfrak{F}_1\left(\frac{qV_{\mathrm{c}}}{k_{\mathrm{B}}T}\right) - \mathfrak{F}_1\left(-\frac{qV_{\mathrm{c}}}{k_{\mathrm{B}}T}\right)\right)\ . \tag{6.1}$$

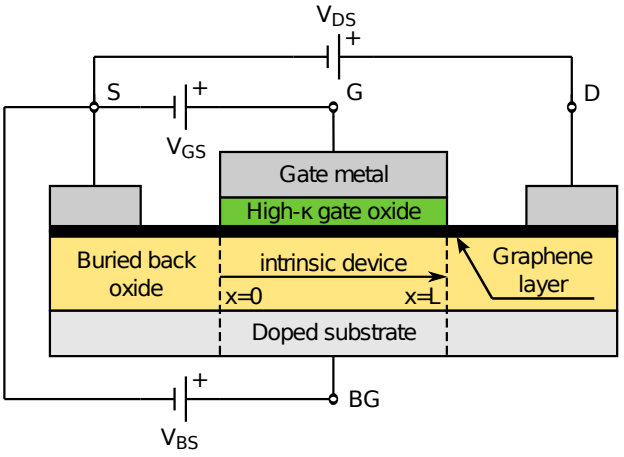

FIGURE 6.3: Cross-section of the modeled dual-gate GFET, with drain (D), gate (G), source (S), and back-gate (BG) contacts. The channel material is single-layer zero-bandgap graphene. The device has a high-κ/metal top-gate and its back-gate is formed by a buried oxide layer and the doped substrate. The device is biased by the top-gate-, back-gate-, and drain-source voltages V_{GS}, V_{BS}, and V_{DS}, respectively. The intrinsic device is indicated.

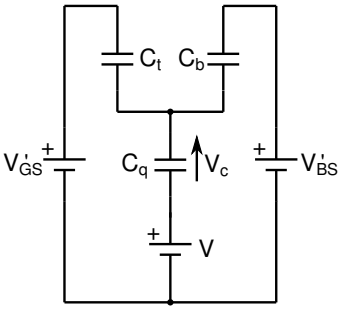

FIGURE 6.4: Equivalent circuit of a capacitive voltage divider representing GFET gate electrostatics [165].C_{q} is the quantum capacitance, C_{t} and C_{b} are the top- and back-gate oxide capacitances. V'_{GS} and V'_{BS} represent the net top- and back-gate voltages. V is the voltage drop in the channel, and V_{c} the channel potential.

p and n are evaluated using Fermi-Dirac integrals of first order[4] $\mathfrak{F}_1(\cdot)$. $\hbar$ is the reduced Planck constant.

Q_{net} is stored in the quantum capacitance, which is defined as $C_{\mathrm{q}} = \mathrm{d}Q_{\mathrm{net}}/\mathrm{d}V_{\mathrm{c}}$ [177]. Within this work, the exact solution of this derivative is referred to as the exact quantum capacitance:

$$C_{\mathrm{q}} = \frac{2q^2 k_{\mathrm{B}} T}{\pi(\hbar v_{\mathrm{F}})^2} \ln\left[2\left(1+\cosh\left(\frac{qV_{\mathrm{c}}}{k_{\mathrm{B}}T}\right)\right)\right] \ . \tag{6.2}$$

Now the capacitance weighting factor α is introduced in order to correctly consider the charge-voltage relation of voltage-dependent capacitors $Q_{\mathrm{net}} = \int_0^{V_{\mathrm{c}}} C_{\mathrm{q}}(\tilde{V})\mathrm{d}\tilde{V} = \alpha(V_{\mathrm{c}})C_{\mathrm{q}}(V_{\mathrm{c}})V_{\mathrm{c}}$. Its application to the exact C_{q} description gives

$$\alpha = \frac{Q_{\mathrm{net}}}{C_{\mathrm{q}}V_{\mathrm{c}}} = \frac{k_{\mathrm{B}}T}{qV_{\mathrm{c}}} \cdot \frac{\mathfrak{F}_1\left(\frac{qV_{\mathrm{c}}}{k_{\mathrm{B}}T}\right) - \mathfrak{F}_1\left(-\frac{qV_{\mathrm{c}}}{k_{\mathrm{B}}T}\right)}{\ln\left(2\left(1+\cosh\left(\frac{qV_{\mathrm{c}}}{k_{\mathrm{B}}T}\right)\right)\right)} \ . \tag{6.3}$$

Subsequently, the channel potential is expressed by equating the charges stored in C_{q} and the parallel connection of the two gate capacitances C_{t} and C_{b}, which yields a modified form of the usual implicit expression [165] for V_{c}:

$$V_{\mathrm{c}} = -\frac{(V'_{\mathrm{GS}} - V)\cdot C_{\mathrm{t}} + (V'_{\mathrm{BS}} - V)\cdot C_{\mathrm{b}}}{C_{\mathrm{t}} + C_{\mathrm{b}} + \alpha(V_{\mathrm{c}})C_{\mathrm{q}}(V_{\mathrm{c}})} \ . \tag{6.4}$$

6.2.1.2 Iterative Verilog-A algorithm to obtain the channel potential

Because of the complexity of Eq. 6.4, it is not possible to express V_{c} explicitely. However, here a construct in Verilog-A (Fig. 6.5) is used to let the circuit simulator iteratively solve this equation during run-time [132]. In continuation, the evaluation of V_{cd} is described, but V_{cs} is computed similarly.

First, a circuit node `nodeVcd` is instantiated. After the iterative solving process, the potential at this node will be equal to V_{cd}. However, at the beginning the node's potential is still different from the desired value. This first guess is assigned to the variable `Vcd`:

[4] The Fermi-Dirac integral of of first order is defined as $\mathfrak{F}_1(\eta) = (1/2)\int_0^{\infty}(\epsilon \mathrm{d}\epsilon)/(1+\exp(\epsilon-\eta))$. Here, η is the normalized Fermi level $\eta = (E_{\mathrm{F}} - E_{\mathrm{DP}})/(k_{\mathrm{B}}T)$. $E_{\mathrm{F}} = -qV$ is the Fermi level, $E_{\mathrm{DP}} = -q(V - V_{\mathrm{c}})$ is the Dirac point energy.

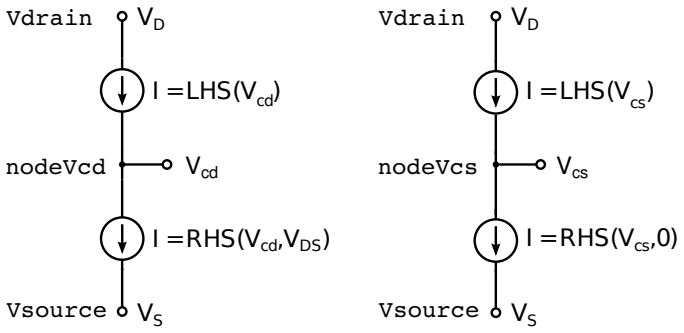

FIGURE 6.5: Verilog-A construct [132] to obtain the channel potentials at the drain and source end of the channel V_{cd} and V_{cs} by iteratively evaluating Eq. (6.4).

```
Vcd = V(nodeVcd);
```

`Vcd` is used to evaluate the left-hand side $LHS(V_{\mathrm{cd}})$ and right-hand side $RHS(V_{\mathrm{cd}}, V_{\mathrm{DS}})$, which gives the results `LHSd` and `RHSd`. These values are assigned to a series connection of two current sources (see left side of Fig. 6.5):

```
I(VDrain,nodeVcd)  <+ LHSd;
I(nodeVcd,VSource) <+ RHSd;
```

This series connection requires `LHSd` and `RHSd` to be equal. The simulator is iteratively changing the potential at the node `nodeVcd` until this goal is achieved and the solution converges. V_{cd} can then obtained by reading out the value of `Vcd`. Therefore, this iterative evaluation provides an accurate description of V_{cd}, which is also valid in the vicinity of the Dirac point.

During the procedure described above, the Fermi-Dirac integral of first order, for which no closed-form solution exists, is approximated with a maximum relative error of 1.79×10^{-6} using elementary mathematical functions [179, 180]. The complete source code of the iterative equation solver is available in Appendix C.

6.2.2 Low-field drain current

The next step is to derive an analytical equation for the GFET drain current I_{D}. First, under the condition of symmetrical electron and hole mobilities [169], the transport sheet charge density $Q_{\mathrm{t}} = q(p + n)$ is expressed as a quadratic polynomial:

$$Q_\mathrm{t} = \frac{2q\left(k_\mathrm{B}T\right)^2}{\pi\left(\hbar v_\mathrm{F}\right)^2}\left(\mathfrak{F}_1\left(\frac{qV_\mathrm{c}}{k_\mathrm{B}T}\right)+\mathfrak{F}_1\left(-\frac{qV_\mathrm{c}}{k_\mathrm{B}T}\right)\right) = \frac{q\pi\left(k_\mathrm{B}T\right)^2}{3\left(\hbar v_\mathrm{F}\right)^2}+\frac{q^3V_\mathrm{c}^2}{\pi\left(\hbar v_\mathrm{F}\right)^2}\ . \tag{6.5}$$

The polynomial's constant term represents the thermal charge density at the Dirac point. A second residual charge density to be taken into account is the spatial inhomogeneity due to electron and hole puddles [181], which are equally probable electron- and hole-rich regions distributed on the pristine graphene sheet and caused by disorders such as ripples and charge-induced inhomogeneities. The carrier density due to these puddles can be expressed as $n_\mathrm{pud} = \frac{\Delta^2}{\pi\hbar^2 v_\mathrm{F}}$, with Δ being the maximum inhomogeneity of the electrostatic potential. This additional component leads to the total transport sheet carrier density

$$Q_\mathrm{tot} = Q_\mathrm{t} + qn_\mathrm{pud}\ . \tag{6.6}$$

Using a soft-saturation model, the carrier velocity can be expressed as $v = \mu E/(1+\mu E/v_\mathrm{sat})$, with μ as the low-field carrier mobility and E the horizontal electrical field strength. It has been shown elsewhere [137] that by combining the soft-saturation approach with the relation $I_\mathrm{D} = W_\mathrm{g}Q_\mathrm{tot}(x)v(x)$, a useful representation of the drain current can be obtained:

$$I_\mathrm{D} = \frac{\mu W_\mathrm{g}\int_0^{V_\mathrm{DS}} Q_\mathrm{tot}\mathrm{d}V}{L_\mathrm{g}+\mu\left|\int_0^{V_\mathrm{DS}}\frac{1}{v_\mathrm{sat}}\mathrm{d}V\right|}\ . \tag{6.7}$$

Here, W_g is the channel width and L_g is the channel length. As Q_tot is given as a function of V_c, solving the integral in the numerator of the abovementioned equation requires a variable substitution of V by V_c for the non-constant parts of the integrand, implying the replacement of $\mathrm{d}V$ by $\frac{\mathrm{d}V}{\mathrm{d}V_\mathrm{c}}\mathrm{d}V_\mathrm{c}$. By deriving Eq. (6.4) with respect to V_c, we obtain

$$\frac{\mathrm{d}V}{\mathrm{d}V_\mathrm{c}} = 1+\frac{C_\mathrm{q}}{C_\mathrm{t}+C_\mathrm{b}}\ . \tag{6.8}$$

Now, the accurate square-root-based approximation [169]

$$C_\mathrm{q} \approx \frac{2q^2 k_\mathrm{B} T \ln(4)}{\pi(\hbar v_\mathrm{F})^2} \cdot \sqrt{1 + \left(\frac{qV_\mathrm{c}}{k_\mathrm{B} T \ln(4)}\right)^2} \tag{6.9}$$

with a maximum relative error of 7.97% allows expressing the numerator integral of Eq. (6.7) as

$$\begin{aligned} &\int_{V_\mathrm{cs}}^{V_\mathrm{cd}} \left(c_\mathrm{a} V_\mathrm{c}^2 + c_\mathrm{b} V_\mathrm{c}^2 \sqrt{1 + c_\mathrm{c}^2 V_\mathrm{c}^2}\right) \mathrm{d}V_\mathrm{c} + \int_0^{V_\mathrm{DS}} q\left(n_0 + n_\mathrm{pud}\right) \mathrm{d}V \\ &= \frac{c_\mathrm{a}}{3} V_\mathrm{c}^3 - \frac{c_\mathrm{b}}{8c_\mathrm{c}^3} \mathrm{asinh}(c_\mathrm{c} V_\mathrm{c}) + \sqrt{1 + c_\mathrm{c}^2 V_\mathrm{c}^2} \left(\frac{c_\mathrm{b}}{8c_\mathrm{c}^2} V_\mathrm{c} + \frac{c_\mathrm{b}}{4} V_\mathrm{c}^3\right)\Big|_{V_\mathrm{cs}}^{V_\mathrm{cd}} + q\left(n_0 + n_\mathrm{pud}\right) V_\mathrm{DS} \end{aligned} \tag{6.10}$$

with the constants $c_\mathrm{a} = \frac{q^3}{\pi(\hbar v_\mathrm{F})^2}$, $c_\mathrm{b} = \frac{1}{C_\mathrm{t}+C_\mathrm{b}} \cdot \frac{2q^5 k_\mathrm{B} T \ln(4)}{\pi^2(\hbar v_\mathrm{F})^4}$, $c_\mathrm{c} = \frac{q}{k_\mathrm{B} T \ln(4)}$, and $n_0 = \frac{\pi(k_\mathrm{B}T)^2}{3(\hbar v_\mathrm{F})^2}$.

It has therefore already been obtained an analytical solution for I_D for the case of low E, where velocity-saturation effects still have not been taken into account.

6.2.3 Velocity saturation

Now the integral in the denominator of Eq. (6.7) is solved to add velocity-saturation effects to the drain current description. The employed velocity-saturation model [166] predicts constant v_sat below the critical carrier density ρ_crit and carrier density-dependent v_sat above this threshold (see Fig. 6.6):

$$\rho_\mathrm{crit} = \frac{1}{2\pi}\left(\frac{\Omega}{v_\mathrm{F}}\right)^2 \tag{6.11}$$

$$v_\mathrm{sat} = \begin{cases} \frac{2v_\mathrm{F}}{\pi}, & \text{if } |Q_\mathrm{net}| \le q\,|\rho_\mathrm{crit}| \\ \frac{2q\Omega}{\pi^2 \hbar v_\mathrm{F} |Q_\mathrm{net}|} & \\ \cdot\sqrt{\frac{\pi(\hbar v_\mathrm{F})^2 |Q_\mathrm{net}|}{q} - \left(\frac{\hbar\Omega}{2}\right)^2}, & \text{if } |Q_\mathrm{net}| > q\,|\rho_\mathrm{crit}| \end{cases} \tag{6.12}$$

Here, $\hbar\Omega$ is the effective energy at which a substrate optical phonon[5] is emitted.

[5]Phonons are quasi-particles that represent periodic excitations of a crystal. They exist in quantized form and can be emitted by a collision of an electron with the semiconductor crystal. Such a collision reduces the kinetic energy of the electron, which is added to the thermal energy of the crystal. Phonons can be classified into acoustic and optical phonons. The latter ones have higher energies and often oscillation frequencies that are in the range of infrared or visible light.

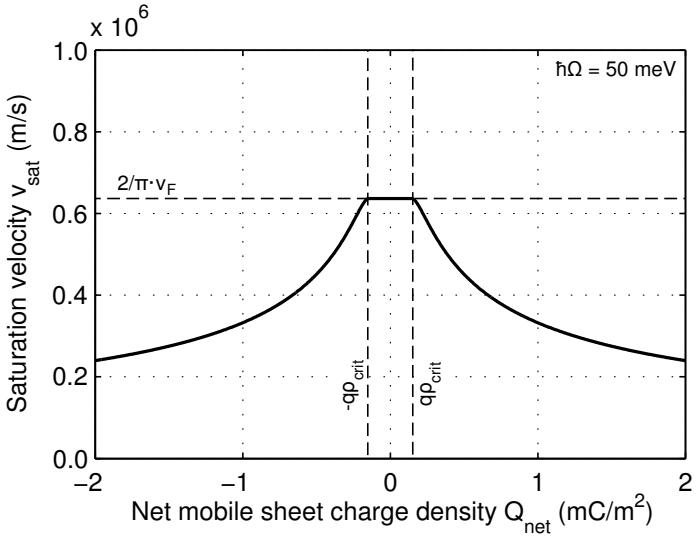

FIGURE 6.6: Graphene saturation velocity v_{sat} vs. net mobile sheet charge density Q_{net} [166]. The optical phonon energy $\hbar\Omega$ is set to 50 meV.

The v_{sat}-model in [166] is based on the absolute-value approximation $C_{\mathrm{q}} \propto |V_{\mathrm{c}}|$, which is inaccurate close to the Dirac point. However, in this region v_{sat} is constant and so the $C_{\mathrm{q}} \propto |V_{\mathrm{c}}|$ approximation has no impact on its accuracy.

As v_{sat} is given as a function of Q_{net}, a double variable substitution to replace $\mathrm{d}V$ by $\frac{\mathrm{d}V}{\mathrm{d}V_{\mathrm{c}}}\frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}Q_{\mathrm{net}}}\mathrm{d}Q_{\mathrm{net}}$ is advantageous. Based on the approximations $C_{\mathrm{q}} = 2q^3|V_{\mathrm{c}}|/(\pi(\hbar v_{\mathrm{F}})^2)$ and $Q_{\mathrm{net}} = C_{\mathrm{q}}V_{\mathrm{c}}/2$, we obtain the required derivatives

$$\frac{\mathrm{d}V}{\mathrm{d}V_{\mathrm{c}}}(Q_{\mathrm{net}}) = 1 + \frac{1}{C_{\mathrm{t}} + C_{\mathrm{b}}} \cdot \sqrt{\frac{4q^3\,|Q_{\mathrm{net}}|}{\pi(\hbar v_{\mathrm{F}})^2}}\ , \tag{6.13}$$

$$\frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}Q_{\mathrm{net}}}(Q_{\mathrm{net}}) = \sqrt{\frac{\pi(\hbar v_{\mathrm{F}})^2}{4q^3\,|Q_{\mathrm{net}}|}}\ . \tag{6.14}$$

This allows to express the denominator integral of Eq. 6.7 as

$$\int_{Q_{\mathrm{net,s}}}^{Q_{\mathrm{net,d}}} \frac{1}{v_{\mathrm{sat}}}\frac{\mathrm{d}V}{\mathrm{d}V_{\mathrm{c}}}\frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}Q_{\mathrm{net}}}\mathrm{d}Q_{\mathrm{net}} = \begin{cases} A|_{Q_{\mathrm{net,s}}}^{Q_{\mathrm{net,d}}}\ , & \text{if } |Q_{\mathrm{net}}| \le q\,|\rho_{\mathrm{crit}}| \\ B|_{Q_{\mathrm{net,s}}}^{Q_{\mathrm{net,d}}}\ , & \text{if } |Q_{\mathrm{net}}| > q\,|\rho_{\mathrm{crit}}| \end{cases} \tag{6.15a}$$

$$A = a\sqrt{bc}d \cdot Q_{\mathrm{net}} + 2\sqrt{c}d \cdot \mathrm{sgn}(Q_{\mathrm{net}})\sqrt{|Q_{\mathrm{net}}|} \tag{6.15b}$$

$$B = \frac{\sqrt{c}e}{6\sqrt{b}f^2} \cdot \Bigg[\operatorname{sgn}(Q_{\mathrm{net}}) \cdot 2\sqrt{f\,|Q_{\mathrm{net}}| - g} \cdot \Big(2abf\,|Q_{\mathrm{net}}| + 3f\sqrt{b\,|Q_{\mathrm{net}}|} + 4abg\Big) + 3\sqrt{bfg^2} \cdot \ln\Big(2b\sqrt{f\,|Q_{\mathrm{net}}|}\sqrt{f\,|Q_{\mathrm{net}}| - g} + 2bfQ_{\mathrm{net}} - \operatorname{sgn}(Q_{\mathrm{net}}) \cdot bg\Big)\Bigg] \tag{6.15c}$$

with the constants $a = \frac{1}{C_{\mathrm{t}}+C_{\mathrm{b}}} \cdot \frac{2q^3}{\pi(\hbar v_{\mathrm{F}})^2}$, $b = \frac{\pi(\hbar v_{\mathrm{F}})^2}{q^3}$, $c = \frac{\pi(\hbar v_{\mathrm{F}})^2}{4q^3}$, $d = \frac{\pi}{2v_{\mathrm{F}}}$, $e = \frac{\pi^2\hbar v_{\mathrm{F}}}{2q\Omega}$, $f = \frac{\pi(\hbar v_{\mathrm{F}})^2}{q}$, and $g = \left(\frac{\hbar\Omega}{2}\right)^2$. The integration domain is limited by the net mobile sheet charge densities $Q_{\mathrm{net,d}}$ and $Q_{\mathrm{net,s}}$ at the drain and source end of the channel, respectively. $\operatorname{sgn}(\cdot)$ is the sign function.

Now, with the antiderivatives expressed in Eqs. (6.10) and (6.15), an accurate analytical solution to the overall drain-current description Eq. (6.7) including velocity saturation effects has been found.

6.3 Accuracy improvements in the vicinity of the Dirac point

In this section the accuracy of the developed drain current model is analyzed using the numerical computing environment MATLAB [139]. It is shown that improvements in the vicinity of the Dirac point are obtained, while at the same time good performance in other regions is preserved.

6.3.1 Comparative study of the drain current model

6.3.1.1 Current-voltage characteristics and derived parameters

The accuracy improvements introduced by this work are illustrated by predicting the characteristics of the 3 µm-GFET reported in [176]. This work's model and a representative model configuration from previous literature [137, 138, 165, 171], which in the following is referred to as "previous model", are compared to the ideal drain current model that does not depend on any of the approximations listed in Sec. 6.1. In order to put emphasis on the importance of C_{q} and Q_{t} modeling, velocity saturation is not taken into account until the following section. Table 6.2 gives an overview of the properties of the two simplified variants and the ideal model.

TABLE 6.2: Model variants for the evaluation of the low-field drain current equation. The "previous" model configuration is following Refs. [137,138,165,171], the "ideal" model is avoiding the approximations listed in Sec. 6.1.

GFET model	Electrostatics		Transport	
	Approx. of C_q	Fermi-Dirac Integrals	Approx. of C_q	Sheet charge density
this work	exact	approx.	$\propto\sqrt{1+c_\mathrm{c}^2V_\mathrm{c}^2}$	Q_t
previous	$\propto\lvert V_\mathrm{c}\rvert$	-	$\propto\lvert V_\mathrm{c}\rvert$	Q_net
ideal	exact	exact	exact	Q_t

Fig. 6.7.(a) shows the transfer characteristics of the modeled GFET. Close to the point of minimum current there is a pronounced deviation from the ideal behavior when using the previous model. For instance, at the operating point of $V_\mathrm{DS}=-0.5\mathrm{V}$ and $V_\mathrm{GS}=-0.25\mathrm{V}$, the relative error of the drain current is $\mathrm{relerr}(I_\mathrm{D})=-32.8\%$ when using the previous modeling approach, but is improved to 4.85% with this work's method. In the same way, the relative error in g_m-modeling is reduced from $\mathrm{relerr}(g_\mathrm{m})=9.32\%$ to 5.10% [Fig. 6.7.(b)]. The reason for the observed difficulties using the previous model at the mentioned operating point is revealed in Fig. 6.7.(c). The ideal channel potentials V_cd and V_cs are simultaneously close to the Dirac point. Although the two potentials still do not fulfil the condition $q\lvert V_\mathrm{c}\rvert < k_\mathrm{B}T$ [introduced in Sec. 6.1.1 and indicated as a gray band in Fig. 6.7.(c)], using the previous model the errors due to the C_q and Q_t approximations can already be noticed. The saturation region is particularly sensible to these approximations. Fig. 6.8.(a) illustrates the previous model's overestimation of the GFET's level of current saturation. For instance, at the operating point $V_\mathrm{DS}=V_\mathrm{GS}=0.25\,\mathrm{V}$ with the disadvantageous condition $\lvert V_\mathrm{cd}\rvert=0\,\mathrm{V}$ [Fig. 6.8.(c)], the previous model predicts total saturation and therefore underestimates the output conductance with an error of $\mathrm{relerr}(g_0)=-100\%$ [Fig. 6.8.(b)]. As a consequence, in the GFET's saturation region the intrinsic gain g_m/g_0 is predicted too optimistically (Fig. 6.9). Furthermore, as a FET's intrinsic maximum oscillation frequency f_max is in first order proportional to $1/\sqrt{g_0}$, using the previous model f_max is overestimated in the saturation region. In contrast, this work avoids erroneous modeling of g_0 at such operating point.

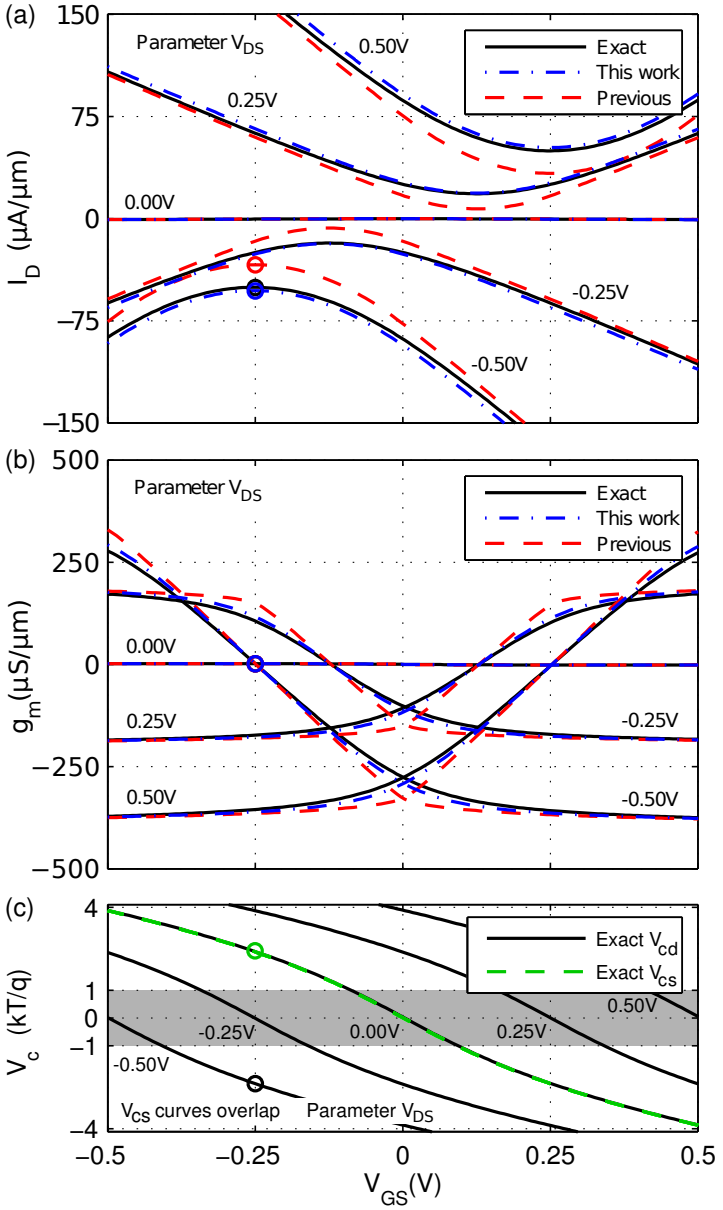

FIGURE 6.7: (a) Transfer (I_{D}-vs.-V_{GS}) and (b) transconductance (g_{m}-vs.-V_{GS}) characteristics of a 3 µm-GFET. This work's model, a previous model, and an ideal model are compared (see Table 6.2 for model configurations). (c) Channel potential (V_{c}-vs.-V_{GS}) characteristics of the ideal model. The condition $q|V_{\mathrm{c}}| < k_{\mathrm{B}}T$ is indicated as a gray band. The $V_{\mathrm{DS}} = -0.5$ V, $V_{\mathrm{GS}} = -0.25$ V operating point is indicated with markers. Device parameters are following Ref. [176]: $L = 3$ µm, $t_{\mathrm{oxb}} = 8.5$ nm, $\kappa_{\mathrm{b}} = 3.5$, $\mu = 7000\,\mathrm{cm}^2/\mathrm{Vs}$, $T = 300$ K. Further assumptions are: $\Delta = 0$ meV, $R_{\mathrm{D/S}} = 0\,\Omega$µm, no velocity saturation.

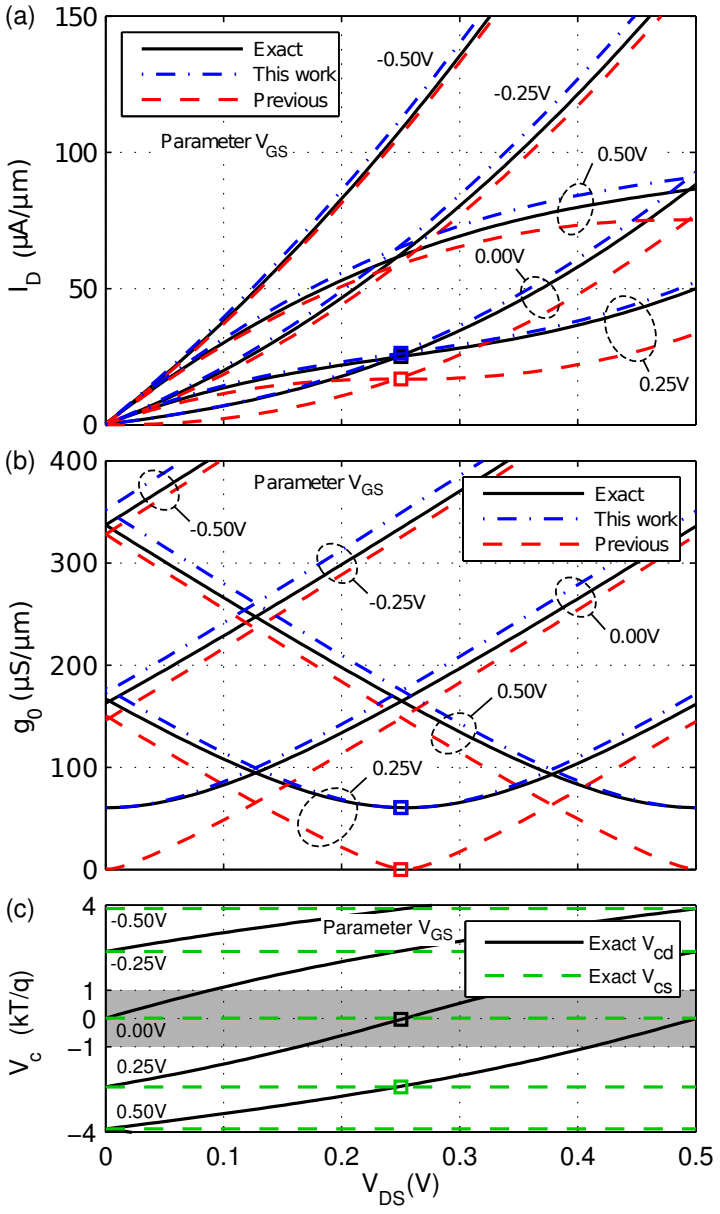

FIGURE 6.8: (a) Output (I_D-vs.-V_{DS}), (b) output conductance (g_0-vs.-V_{DS}), and (c) channel potential (V_c-vs.-V_{DS}) characteristics of a 3µm-GFET. The condition $q|V_c| < kT$ is indicated as a gray band. The $V_{DS} = 0.25$V, $V_{GS} = 0.25$V operating point is indicated with markers. Model configurations and device parameters are as in Fig. 6.7.

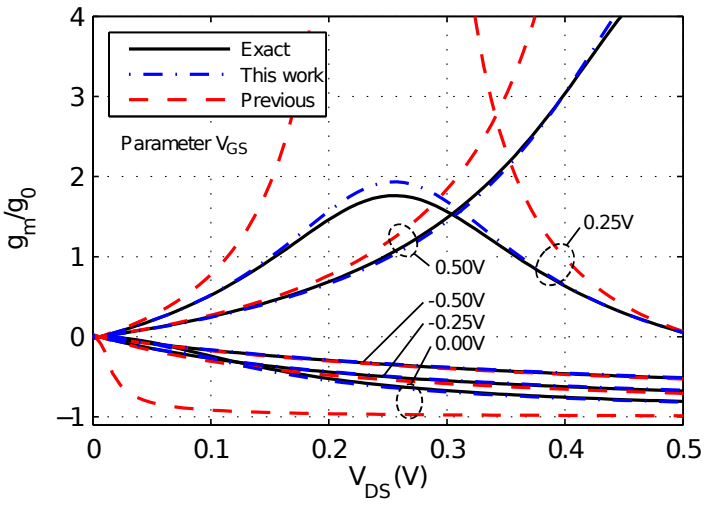

FIGURE 6.9: Intrinsic gain (g_m/g_0-vs.-V_{DS}) characteristics of a 3 µm-GFET. Model configurations and device parameters are as in Fig. 6.7.

6.3.1.2 Evaluation of the relative modeling error

Fig. 6.10 shows a comparative benchmark of this work and the previous model and indicates their relative errors with respect to the ideal behavior. This analysis provides a global accuracy overview, as V_{DS} and V_{GS} continuously span a biasing range from -1 to 1 V. The model configurations are as in the previous section (see Table 6.2) and the already discussed operating points are indicated by markers.

With this work's approach, gate electrostatics are evaluated with negligible error even in the case of low V_c, yielding an accurate mapping of V_c to the biasing voltages V_{GS} and V_{DS} (Fig. 6.10.(a), left side; peak relative error $\text{relerr}_{\text{peak}}(V_{cd}) = -0.0023\%$). In contrast, with the previous model V_c is overestimated close to the Dirac point. For V_{cs} and V_{cd} that occurs at $V_{GS} \approx 0$ V and $V_{GS} \approx V_{DS}$, respectively. The V_{cd}-case is depicted on the right side of Fig. 6.10.(a), where $\text{relerr}_{\text{peak}}(V_{cd}) \to \infty$ can be seen as a diagonal band at $V_{GS} \approx V_{ds}$. Furthermore, this work avoids the significant error in C_q modeling close to the Dirac point and improves $\text{relerr}_{\text{peak}}(C_q)$ from -100% to -2.24×10^{-5} % [Fig. 6.10.(b)]. The error in drain current modeling $\text{relerr}_{\text{peak}}(I_D)$ is also strongly decreased from -100% to 6.35% in the vicinity of zero biasing, *i.e.*, at $V_{GS} \approx 0$ V and $V_{DS} \approx 0$ V [Fig. 6.10.(c)]. Due to the square-root-based approximation of C_q, the error is yet not zero. The trend is similar when regarding the I_D-derived property g_m [Fig. 6.10.(d)]. When using this work's model, $\text{relerr}_{\text{peak}}(g_m)$ is 23.8% close to zero biasing, while it approaches ∞ with the previous model. Finally, $\text{relerr}_{\text{peak}}(g_0)$ is limited to 6.35% with this work, but is sensible to errors when V_{cd} is poorly modeled [Fig. 6.10.(e)].

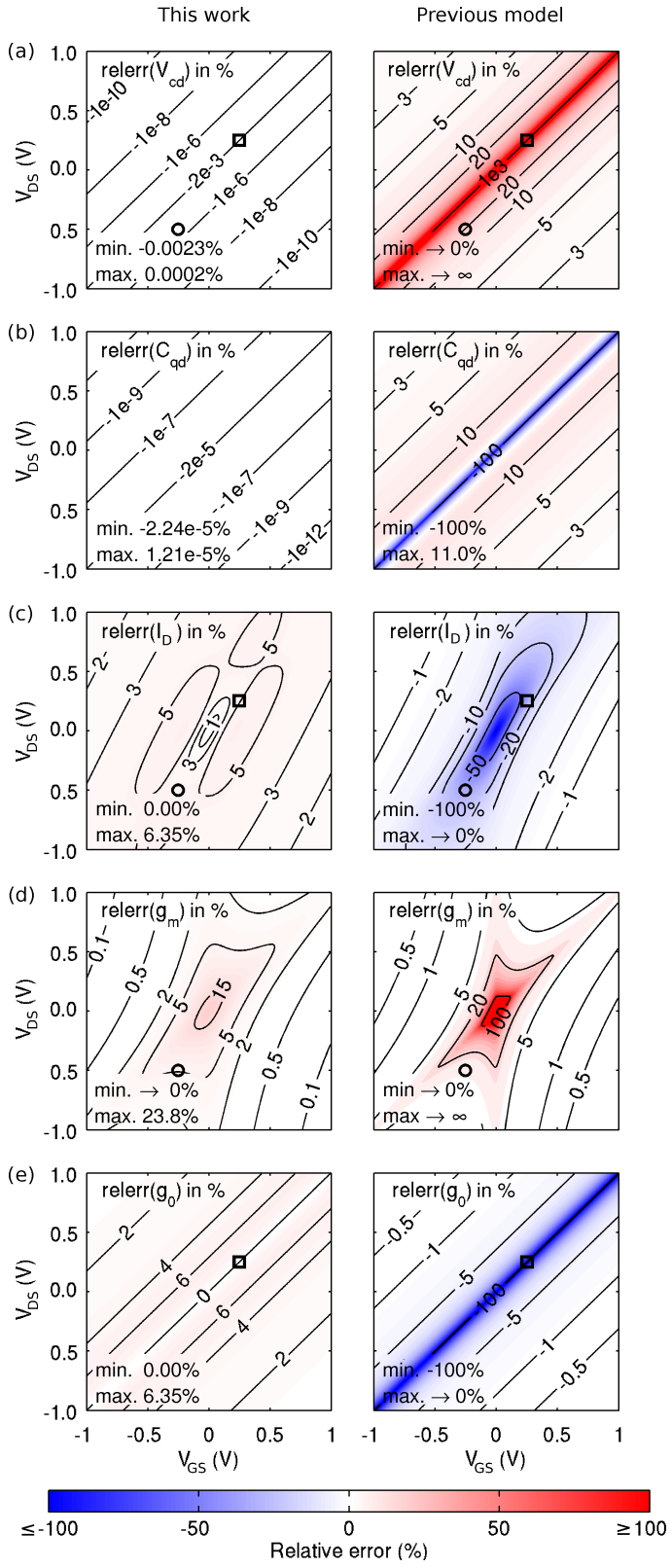

FIGURE 6.10: Comparison of the relative errors of this work's drain current equation (left column) and a previous modeling approach (right column) with the ideal model (see Table 6.2 for model configurations). The errors are given for: (a) channel potential at the drain end V_{cd} (b) Quantum capacitance at the drain end C_{qd} (c) drain current I_{D} (d) transconductance g_{m} (e) output conductance g_0. Model configurations and device parameters are as in Fig. 6.7. The operating points indicated in Figs. 6.7 (round markers) and 6.8 (square markers) are shown. All plots are identically scaled.

6.3.2 Evaluation of the two-region velocity saturation model

After investigating on the accuracy of this work's GFET model under low-field conditions, the advantage of the used two-region velocity saturation model [166] with respect to the $v_{\mathrm{sat}} \propto |V_{\mathrm{c}}^{-1}|$ approach [105] is discussed [see Fig. 6.11]. Overestimating v_{sat} close to the Dirac point [Fig. 6.2.(d)] leads to significant errors. In a biasing range such as the one used in the previous section (V_{GS} and V_{DS} ranging from -1 to 1 V), using the simpler approach leads to a $\mathrm{relerr}_{\mathrm{peak}}(I_{\mathrm{D}})$ of 11.5% with respect to this work's 2-region model. The modeling error of g_{m} is of the same order of magnitude with $\mathrm{relerr}_{\mathrm{peak}}(g_{\mathrm{m}}) = -8.83\%$. In addition, for small V_{cd} the $v_{\mathrm{sat}} \propto |V_{\mathrm{c}}^{-1}|$ model wrongly estimates current saturation. In this operation region $\mathrm{relerr}_{\mathrm{peak}}(g_0)$ is approaching $\pm\infty$.

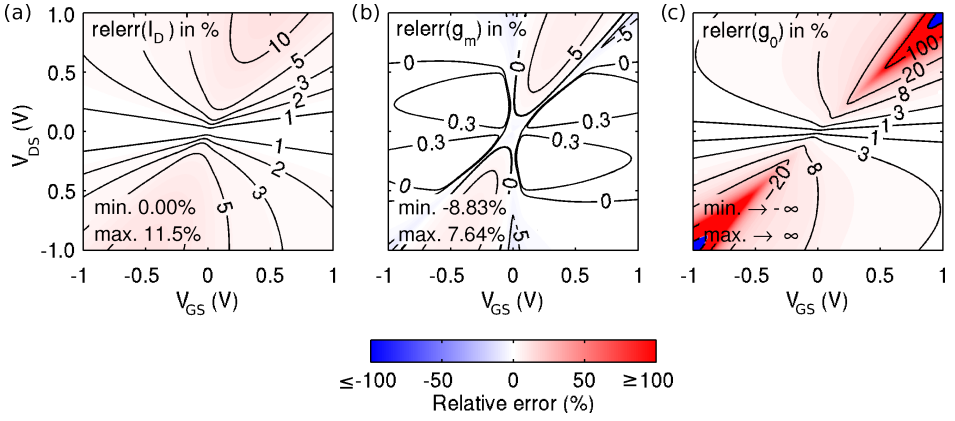

FIGURE 6.11: Relative error of the $v_{\mathrm{sat}} \propto \left|V_{\mathrm{c}}^{-1}\right|$ model compared to the two-region velocity saturation model [166] used in this work. The error is given for: (a) drain current I_{D} (b) transconductance g_{m} (c) output conductance g_0. Velocity saturation is considered with $\hbar\Omega = 50$ meV. Model configurations and all other device parameters are as in Fig. 6.7. All plots are identically scaled.

6.4 Model validation

The GFET drain current model presented in this work is now verified by comparing it to experimental data. In a two-step study, first, the new model's advantages are highlighted by using it in a situation that provokes very low $|V_{\mathrm{c}}|$. The second part demonstrates the model's sound behavior in conventional biasing regions.

For this study, the model has been implemented in Verilog-A (source code available in Appendix C) and simulations have been performed using the Cadence Virtuoso Spectre

Circuit Simulator[6] [153]. An overview of the model's input parameters is given in Table 6.3. Fig. 6.12 shows the test bench used to perform this section's DC simulations.

[6] As the GFET's extrinsic D/S resistances are considered, the extrinsic terminal voltages are not equal to the for the model equations required intrinsic voltages. Therefore, simulations cannot be performed with MATLAB like in Sec. 6.3, but require a circuit simulator.

TABLE 6.3: Input parameters for the accurate GFET Verilog-A model.

Input parameter	Description	Typical value
`Lg`	Gate length L_g	5 µm
`Wg`	Gate width W_g	1 µm
`tox_top`	Top-gate oxide thickness t_oxt	15 nm
`tox_back`	Back-gate oxide thickness t_oxb	300 nm
`kappa_top`	Top-gate oxide permittivity κ_t	8.9
`kappa_back`	Back-gate oxide permittivity κ_b	3.9
`Vgs0`	Top-gate voltage for minimum drain current $V_\mathrm{GS,0}$	1.24 V
`Vbs0`	Back-gate voltage for minimum drain current $V_\mathrm{BS,0}$	11.0 V
`Rd`	Extrinsic drain resistance R_D	170 Ω µm
`Rs`	Extrinsic source resistance R_S	170 Ω µm
`mucm2Vs`	Carrier mobility μ in $\mathrm{cm^2\,V^{-1}\,s^{-1}}$	1150 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$
`Delta`	Spatial potential inhomogeneity Δ due to electron-hole puddles	100 meV
`hbarOmega`	Optical phonon energy $\hbar\Omega$	75 meV

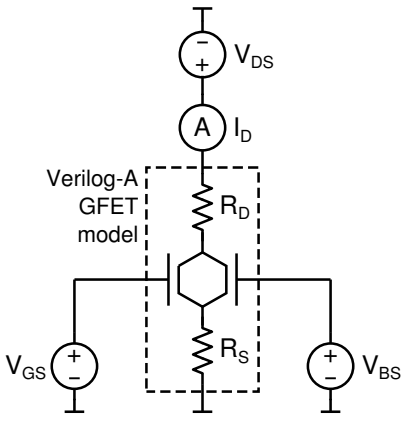

FIGURE 6.12: Test bench for the simulation of the GFET's DC characteristics. The Verilog-A model includes the extrinsic drain and source resistances R_D and R_S.

6.4.1 Operation in the vicinity of the Dirac point

Low V_{ds} biasing leads to $V_{\mathrm{cs}} \approx V_{\mathrm{cd}}$, and in the vicinity of the point of minimum drain current then both potentials simultaneously fulfill $q\,|V_{\mathrm{c}}| \ll k_{\mathrm{B}}T$. Under this condition, with the previous model the currents injected at the drain and source side of the GFET are erroneous at the same time, yielding a significant underestimation of the overall drain current.

Chen and Appenzeller [174] provide a scenario that allows to evaluate both this work's results and the previous modelling approach at low biasing, as they have reported measurement data for the transfer characteristics of GFETs biased at $V_{\mathrm{DS}} = 10\,\mathrm{mV}$. These GFETs are based on graphene flakes located on an oxidized silicon wafer (Fig 6.13). The devices' drain and source contacts have been realized with top-electrodes. The heavily-doped silicon substrate acts as a back-gate, and a 300 nm-thick layer of SiO_2 is the back-gate oxide. Devices of several gate lengths and widths have been reported.

In continuation, the behavior of a 2.8 µm-GFET is predicted. The used modeling parameters are listed in Table 6.4, which also includes the parameters mentioned in [174]. Fig. 6.14.(a) shows that this work's model correctly describes I_{D} in the vicinity of the point of minimum current while the previous model does not. However, compared to the analysis in Sec. 6.3, relerr(I_{D}) is reduced due to electron-hole puddles, which introduce an additional linear term in the I_{D}-vs.-V_{DS} characteristics [see Eq. (6.10)]. This yields a parallel conductance that avoids a drain current close to zero when using the previous model. Fig. 6.14.(b) depicts that with this work's model g_{m} is also modelled with good accuracy to the measurement, contrary to what happens with the previous model.

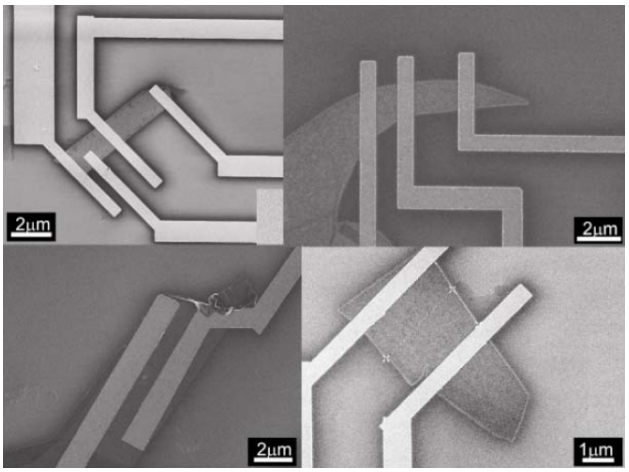

FIGURE 6.13: Scanning electron microscopy images of back-gated GFETs reported by Chen and Appenzeller (from [174]). Devices of various channel lengths and widths were fabricated.

TABLE 6.4: Model parameters for the prediction of the DC behavior of the 2.8 µm-GFET reported in [174].

Input parameter	Model value	Value given in [174]
`Lg`	2.8 µm	2.8 µm
`Wg`[1]	1 µm	-
`tox_top`[2]	1 m	-
`tox_back`	300 nm	300 nm
`kappa_top`[2]	1.0	-
`kappa_back`	3.9	(SiO_2)
`Vgs0`[2]	0.0 V	-
`Vbs0`	11.86 V	-
`Rd`	150 Ω µm	$R_S + R_D = 300\,\Omega\,\mu m$
`Rs`	150 Ω µm	
`mucm2Vs`	3800 $cm^2\,V^{-1}\,s^{-1}$	3750 $cm^2\,V^{-1}\,s^{-1}$
`Delta`[3]	70.0 meV / 74.5 meV	-
`hbarOmega`[2]	1 eV	-

[1] W_g is set to 1 µm, as results are given per µm device width.

[2] Model parameters are chosen such that they have a negligible influence on the device behavior.

[3] Values are given for this work's model / the previous model.

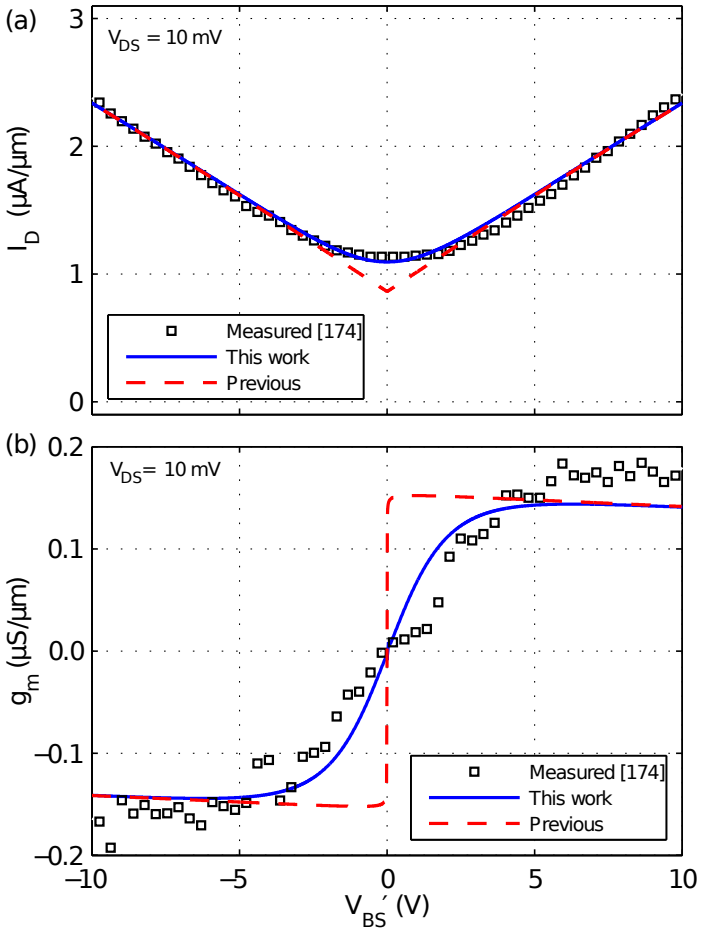

FIGURE 6.14: Comparison of this work's GFET model and a previous model (see Table 6.2 for model configurations) to low-bias measurements at $V_{\mathrm{DS}} = 10\,\mathrm{mV}$ of the transfer characteristics of a 2.8 µm-GFET reported in [174]. (a) Drain current I_{D} and (b) Transconductance g_{m} vs. net back-gate voltage V'_{BS}. The chosen device parameters are listed in Table 6.4. Room temperature $T = 300\,\mathrm{K}$ applies.

6.4.2 Operation under conventional biasing conditions

Now, the usability of this work's model under conventional biasing conditions of up to several volts is demonstrated by reproducing the transfer and output characteristics of a 5 µm [175] and a 3 µm [176] GFET device.

The 5 µm-GFET reported by Wang *et al.* [175] is based on large-area CVD graphene, which has been grown on a Cu substrate and has then been transferred onto polished Si wafers covered with a 300 nm-thick layer of SiO_2. The device's top-gate dielectric consists of 15 nm of Al_2O_3 and is covered by a metal gate. The D/S electrodes form ohmic contacts with the graphene layer. The other device, a 3 µm-GFET reported by Meric *et al.* [176] (Fig. 6.15), is based on exfoliated graphene as the channel material and exfoliated hexagonal boron nitride h-BN as the gate dielectric. The isolating h-BN has been located on a back-gate metal electrode and then been covered by a graphene layer, which has been connected by ohmic contacts. The back-gate structure of Meric's device avoids the performance-degrading deposition of a top-gate dielectric on the sensible graphene surface and therefore yields higher carrier mobility.

The accurate model developed in this section has been used to reproduce the transfer characteristics of the 5 µm-GFET and the output characteristics of the 3 µm-GFET. Figs. 6.16 and 6.17 show the results of these DC simulations and demonstrate that both scenarios are modeled accurately. Tables 6.5 and 6.6 give the respective model parameters, which are close to the values reported in the publications [175, 176] corresponding to the devices.

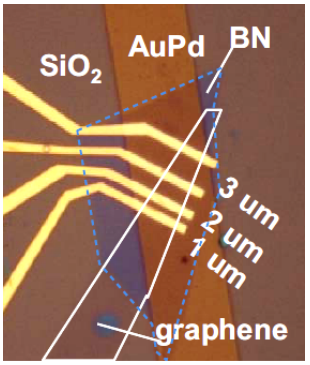

FIGURE 6.15: Optical micrograph of the 3 µm-GFET reported by Meric *et al.* (from [176]). The back-gate device is based on exfoliated h-BN and graphene as the gate dielectric and channel material, respectively.

TABLE 6.5: Model parameters for the prediction of the DC behavior of the 5.0 µm-GFET reported in [175].

Input parameter	Model value	Value given in [175]
`Lg`	5.0 µm	5.0 µm
`Wg`[1]	1 µm	25 µm
`tox_top`	15 nm	15 nm
`tox_back`	300 nm	300 nm
`kappa_top`	8.9	(Al_2O_3)
`kappa_back`	3.9	(SiO_2)
`Vgs0`	1.24 V	1.24 V
`Vbs0`	11.0 V	11.0 V
`Rd`	3.5 kΩ µm	2.5 . . . 4.2 kΩ µm
`Rs`	3.5 kΩ µm	2.5 . . . 4.2 kΩ µm
`mucm2Vs`	1150 $cm^2\,V^{-1}\,s^{-1}$	1500 $cm^2\,V^{-1}\,s^{-1}$
`Delta`	100 meV	-
`hbarOmega`	75 eV	-

[1] W_g is set to 1 µm, as results are given per µm device width.

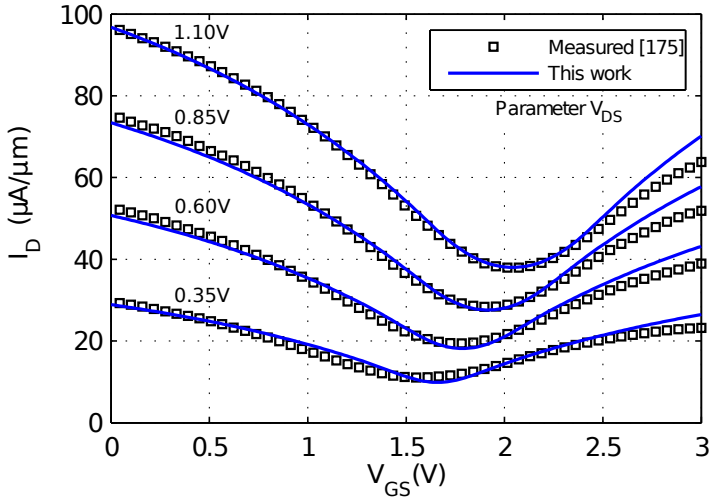

FIGURE 6.16: Comparison of this work's GFET model to the transfer characteristics of a 5 µm-GFET reported in [175]. Shown is the drain current I_D vs. gate-source voltage V_{GS} for varying drain-source voltage V_{DS}. The chosen device parameters are listed in Table 6.5. Room temperature $T = 300$ K applies.

TABLE 6.6: Model parameters for the prediction of the DC behavior of the 3.0 µm-GFET reported in [176].

Input parameter	Model value	Value given in [176]
`Lg`	3.0 µm	3.0 µm
`Wg`[1]	1 µm	-
`tox_top`[2]	1 m	-
`tox_back`	8.5 nm	8.5 nm
`kappa_top`[2]	1.0	-
`kappa_back`	3.5	(h-BN)
`Vgs0`	0.0 V	-
`Vbs0`	0.0 V	-
`Rd`	170 Ω µm	-
`Rs`	170 Ω µm	-
`mucm2Vs`	7000 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$	$\mu_\mathrm{e} = 8579\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ $\mu_\mathrm{h} = 10\,713\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$
`Delta`	65 meV	-
`hbarOmega`	75 eV	40 eV

[1] W_g is set to 1 µm, as results are given per µm device width.
[2] Model parameters are chosen such that they have a negligible influence on the device behavior.

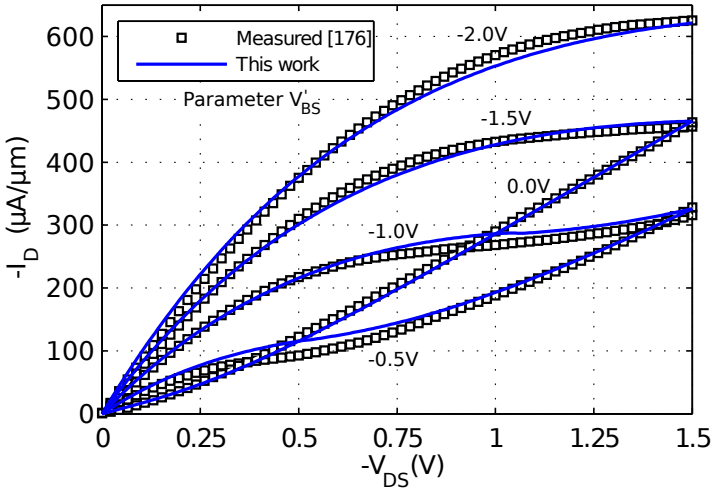

FIGURE 6.17: Comparison of this work's GFET model to the output characteristics a 3 µm-GFET reported in [176]. Shown is the drain current I_D vs. drain-source voltage V_DS for varying net back-gate voltage V'_BS. The chosen device parameters are listed in Table 6.6. Room temperature $T = 300$ K applies.

6.5 DC behavior of the GFET

Finally, an application example for the developed and verified accurate GFET model is presented. The DC characteristics of the state-of-the-art GFET reported by Meric *et al.* [176] are compared to performance predictions for an optimized GFET. The latter device has the same channel dimensions, but the following improvements are assumed: the BN gate dielectric thickness is reduced to 4 nm, the carrier mobility is $40\,000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ such as has readily been reported for graphene on BN [182], and the contact resistance is reduced to $50\,\Omega\,\mu\mathrm{m}$, which is comparable to typical values for Si-MOSFETs [183] (see Table 6.7).

Fig. 6.18.(a) shows a comparison of the I_D vs. biasing voltage relations of the conventional and the optimized GFET. By introducing the abovementioned improvements, the current drive capability of the GFET can roughly be doubled. Fig. 6.18.(b) depicts that a similar increase can be obtained for the transconductance g_m. Furthermore, the g_m of the optimized device is approximately constant in a wide biasing range. This linear dependence of I_D on V_GS indicates operation close to velocity saturation and is particularly promising in terms of device linearity. The output conductance behavior is shown in Fig. 6.18.(c). g_0 is high in a wide biasing region, although the optimized device shows larger zones of the desired low g_0. Due to a strong impact of velocity saturation, g_0 can even turn to negative values for high V_DS. Fig. 6.18.(d) depicts that in both analyzed cases g_int is even lower than unity in wide biasing zones. However, the optimized GFET maintains a performance advantage in terms of this FoM. A final observation is that

Table 6.7: Parameters for the performance comparison between a conventional and an optimized GFET.

Device parameter	Conventional GFET [176]	Optimized GFET
L_g	3.0 µm	3.0 µm
t_ox	**8.5 nm**	**4 nm**
κ	3.5 (BN)	3.5 (BN)
$R_\mathrm{d},\ R_\mathrm{s}$	$\mathbf{170\,\Omega\,\mu m}$	$\mathbf{50\,\Omega\,\mu m}$
μ	$\mathbf{7000\,cm^2\,V^{-1}\,s^{-1}}$	$\mathbf{40\,000\,cm^2\,V^{-1}\,s^{-1}}$
Δ	65 meV	65 meV
$\hbar\Omega$	75 eV	75 eV

the mentioned negative g_0 regions cause negative g_{int} regions. This and the fact that the change in sign of these two FoMs happens at the zones of maximum gain may add additional constraints to GFET circuit design.

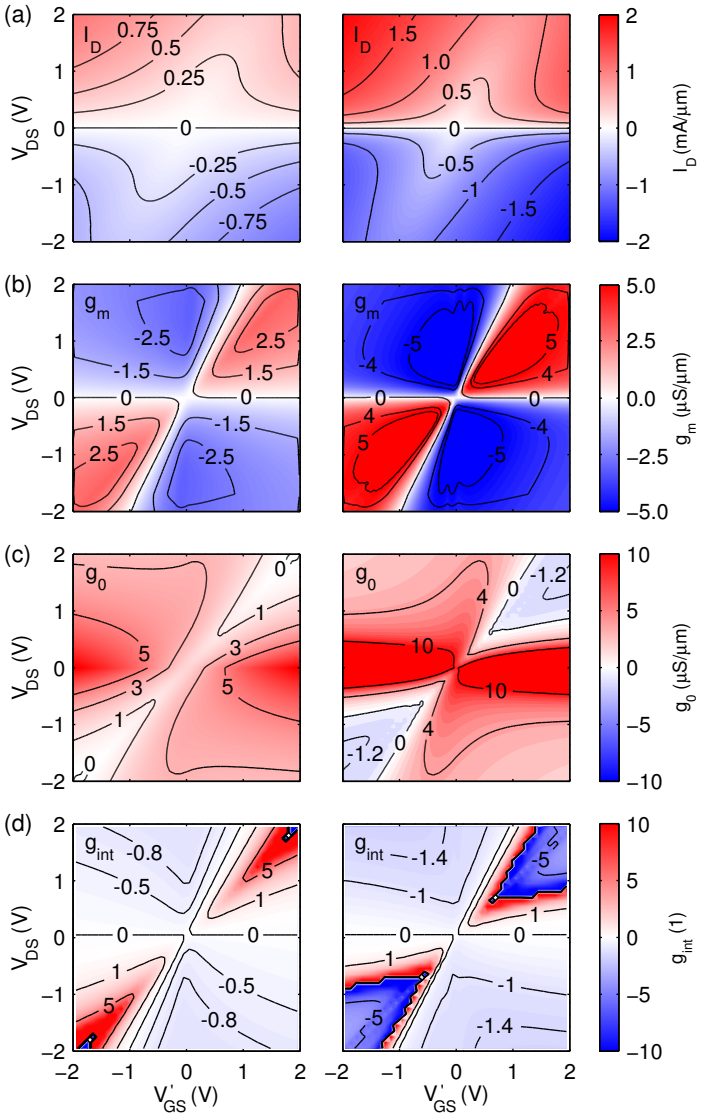

FIGURE 6.18: Comparison of the DC behavior of a conventional (left column) and an optimized (right column) GFET (see Table 6.7 for model configurations). Shown are (a) the drain current I_{D}, (b) the transconductance g_{m}, (c) the output conductance g_0, and (d) the intrinsic gain g_{int} vs. the drain-source and gate-source biasing voltages V_{DS} and V'_{GS}, respectively. The V_{DS} and V'_{GS} scales are identical for all plots.

6.6 Conclusion

Accurate models are an essential prerequisite for successful performance analyses and circuit design. However, in previously published GFET models several simplifications cause inaccurate results especially when the quasi-Fermi-level at the source or drain side of the channel is close to the Dirac point.

In this chapter it has been developed an intrinsic GFET compact model with high accuracy independently of the quasi-Fermi-level's distance to the Dirac point. First, an overview of the problematic modeling aspects quantum capacitance, charge density relevant for transport, charge-voltage relation of voltage-dependent capacitors, and saturation velocity has been given. Then, an HDL-implementable GFET drain current solution has been proposed that mitigates the approximations of these aspects (Verilog-A version available in Appendix C). Subsequently, the improvements in accuracy for device parameters such as I_{D}, g_{m}, and g_0 have been highlighted by comparing this work's model with a previously published model configuration. The exact prediction of these parameters impacts figures-of-merit such as the intrinsic gain or f_{max} and is of major interest for GFET performance projections and circuit design.

The developed model has been validated by showing good agreement to experimental data both in the case of low-voltage operation and conventional biasing conditions. As an application example, it has finally been used to confirm an enhancement of DC performance FoMs when increasing the GFET's carrier mobility and decreasing its gate dielectric thickness and contact resistance.

Chapter 7

Final conclusions

THIS THESIS presents a body of work on the modeling of and performance predictions for carbon nanotube and graphene field-effect transistors, which are two promising candidate technologies for future high-performance electronics. The main objective of this work has been to investigate on the opportunities of using these carbon-based technologies for RF integrated circuits. For that purpose, the following key issues have been addressed: the modeling of manufacturing process variability and noise in CNFETs, RF performance predictions for CNFETs on device and circuit level, and providing an accurate GFET compact model.

A key contribution of this thesis comes from the proposal of the first CNFET noise compact model. Noise is a phenomenon that is of primary importance for the performance of RF circuits, and the capability of describing its dependence on the device parameters and operating point allows to significantly increase the insights gained from simulation studies. This work has methodically introduced the most significant contributors to CNFET RF-noise and has provided an analytical description for each of them. Special focus has been put on channel shot noise suppression caused by Coulomb interactions and Pauli exclusion. A second contribution of this thesis is the proposal of a CNFET manufacturing process variability model. The synthesis of carbon nanotubes entails significant process variations, which causes uncertainty of the tubes' electrical properties such as the bandgap or dopant concentration. The imperfect removal of metallic tubes adds additional process variability. The model covers such CNT growth and removal variations in order to enable more realistic performance projections. Both the CNFET

noise and the variability model have been implemented in the hardware description language Verilog-A and added as extensions to the Stanford CNFET compact model. This extended compact model allows for the variability-aware RF performance assessment of the CNFET technology using conventional circuit design environments.

A significant part of this thesis focuses on comprehensive RF performance projections for the CNFET —both on the device and on the circuit level —with the aim of highlighting the opportunities of using this novel technology in comparison to conventional silicon-based RF-CMOS. In the first part of a two-step study, a detailed device performance overview has been provided by determining the overall set of ITRS RF-CMOS technology requirement FoMs for several CNFET technology nodes. With respect to multi-gate Si-CMOS, the CNFET is found to have a significant performance advantage in terms of device speed, gain, and the minimum noise figure. It has been shown that the CNFET positively responds to device downscaling in most benchmark categories, which would allow to keep his performance advantage until well beyond the year 2026 time horizon of the ITRS. The second part of the study has extended the state-of-the art of CNFET circuit-level performance projections by designing the two basic RF building blocks low-noise amplifier and oscillator and reporting FoMs for them. This has been made possible by considering the impact of noise. This latter analysis accounts for the following insights: 1) simple CNFET-based LNAs are already competitive with the most advanced CMOS designs, 2) CNFET oscillators clearly outperform their silicon counterparts, and 3) with CNFETs very high operating frequencies can easily be achieved. In summary, these promising results confirm that the CNFET has the potential to outperform Si-CMOS in RF applications. This novel technology can be a key enabler for future low-cost high-performance RF electronics, which encourages to improve today's still immature manufacturing capabilities and make real the CNFET's performance potential.

A third main contribution of this thesis is the development of an accurate physics-based compact model for single-layer GFETs. Most of today's models of that kind rely on simplifications of certain physical properties. This can cause wrong simulation results such as an erroneous prediction of the GFET's current saturation, which critically impacts the outcome of graphene-based circuit design. Given this background, this thesis proposes a GFET compact model with improved accuracy. It combines the two opposed requirements of 1) simple enough model equations to allow their implementation with

conventional hardware description languages and 2) sufficiently complex equations to obtain accurate results. For that purpose, a new description of the accuracy-affecting modeling aspects has been proposed and the GFET's current-voltage relation has been derived. In continuation, the obtained improvements have been systematically studied. The novel modeling approach gives significantly better results for the drain current, transconductance, output conductance, and intrinsic gain. Also, the new model has been validated by comparing it to reported measurements for GFET prototypes under several biasing conditions. Finally, it has been used to investigate on the positive impact of several manufacturing process improvements on the GFET's DC performance. The proposed model has been implemented in Verilog-A and is compatible to conventional circuit simulators, which facilitates its dissemination in the graphene circuit design community. The availability of such an accurate GFET compact model is an important step towards better understanding the characteristics and opportunities of graphene-based analog circuitry.

7.1 Summary of thesis contributions

The contributions of this thesis can be summarized as follows:

- The first CNFET noise compact model has been proposed. For that purpose, the CNFET's main noise sources have been mathematically described and implemented in Verilog-A. As noise is crucial in RF applications, this contribution increases the insights from CNFET circuit simulations.
- A CNFET variability model has been proposed and implemented in Verilog-A. It considers typical manufacturing process imperfections and allows variability-aware CNFET circuit simulations.
- The RF performance of the CNFET technology has been analyzed on the device level. The overall set of ITRS RF-CMOS technology requirement FoMs has been determined.
- The performance analysis of the CNFET technology has been extended to the circuit level. For the first time, FoMs for the basic RF building blocks LNA and oscillator have been determined.

- Several modeling aspects of previous GFET compact models have been identified to cause inaccurate simulation results under certain conditions. A more accurate description of the GFET's current-voltage relation has been proposed and its advantage compared to previous work has been highlighted.
- The proposed GFET drain current equations have been implemented in Verilog-A as an accurate GFET compact model. It has been validated against measurements and is provided as a useful tool for the exploration of graphene-based analog circuits.

7.2 Future work

The following list shows several promising research fields to further extend the state-of-the-art of carbon-based electronics:

- A description of channel-induced gate noise specifically for ballistic RF-CNFETs would allow further insight into this noise source's impact on that novel technology.
- Up to today no comprehensive noise compact model for the channel noise or even the channel-induced gate noise of graphene FETs has been reported. This strongly limits RF simulations for graphene-based circuits. For instance, FoMs for basic RF building blocks cannot be determined for GFETs such as it has been done in this work for the CNFET technology.
- An experimental validation of the proposed CNFET noise model and further experimental validation of the proposed accurate GFET compact model would give new insights to further develop and improve these models.

Appendix A

Publications

A.1 Journal papers

- G. M. Landauer and J. L. González, "Radio-frequency performance of carbon nanotube-based devices and circuits considering noise and process variation," *IEEE Trans. Nanotechnol.*, vol. 13, no. 2, pp. 228-237, Mar. 2014.
- G. M. Landauer, D. Jiménez, and J. L. González, "An accurate and Verilog-A compatible compact model for graphene field-effect transistors," *IEEE Trans. Nanotechnol.*, in press.

A.2 Conference papers

- G. M. Landauer, D. Jiménez, and J. L. González, "Compact modeling of external parasitics of graphene field-effect transistors," *Graphene 2014*, Toulouse, France, May 2014.
- G. M. Landauer and J. L. González, "A compact noise model for carbon nanotube FETs," *2012 Int. Semiconductor Conf. Dresden-Grenoble (ISCDG)*, Grenoble, France, Sep. 2012, pp. 53-56.
- G. M. Landauer and J. L. González, "Carbon nanotube FET process variability and noise model for radiofrequency investigations," *2012 12th IEEE Conf. Nanotech. (IEEE-NANO)*, Birmingham, UK, Aug. 2012, pp. 1-5.

- G. M. Landauer and J. L. González, "Impact of process variability and noise on the radiofrequency performance of carbon-nanotube field-effect transistors," *Nanospain 2012*, Santander, Spain, Feb. 2012.

- G. M. Landauer and J. L. González, "Radiofrequency Performance of Carbon Nanotube FETs in comparison to classical CMOS technology," *41st European Solid-State Device Research Conf. (ESSDERC), fringe poster session*, Helsinki, Finland, Sep. 2011.

Appendix B

Verilog-A implementation of the CNFET process variability and noise model

B.1 CNFET model - Level 1

The following Level 1 source code is a modified version of the code provided with the original Stanford CNFET compact model [132–135]. It contains the noise model and parts of the process variability model developed in this work.

The source code includes some parts of the original code (modified versions of the interfaces, the electrical nodes, and the voltage/current assignments to the nodes). However, the core of the original model —responsible for the charge, drain current, and capacitance calculations —has been removed. It is available at the web site of the Stanford Nanoelectronics Lab [135].

veriloga.va

```
1
2 `include "disciplines.vams"
3 `include "parameters.vams"
4
5 module NCNFET_L1(Drain, Gate, Source, Sub);
6
7 /*************************************************************
8 ********************** Electrical nodes ***********************
9 *************************************************************/
```

```
10
11 inout Drain, Gate, Source, Sub;
12
13 electrical Drain, Gate, Source, Sub, Drain_int, Source_int, Drain_b,
       Drain_ch, Source_b, Drain_lk, Source_lk;
14 electrical CoupleNode, Vgate, mid2, Vsource_int, Vdrain_int, VsubM, phib,
        Noise;
15
16
17 /*****************************************************************
18 ********************** Input parameters ************************
19 *****************************************************************/
20
21 parameter real Lg=32.0e-9;           // CNFET channel/gate length
22 parameter real pitch=10.0e-9;        // Tube pitch
23 parameter real Kgate=16.0;           // High-k gate dielectric constant
24 parameter real Tox=4.0e-9;           // Gate oxide thickness
25 parameter integer dist_type = 0;     // Diameter distribution: Gaussian =
       0, shifted log-normal = 1
26 parameter real dia_mean = 1.5e-9;    // Tube diameter
27 parameter real dia_stddev = 0.0e-9; // ...and its standard deviation
28 parameter real Efi_mean = 0.66;      // The n+ doped CNT fermi level (eV),
        0.66eV for 1% doping level, 0.6eV for 0.8% doping level
29 parameter real Efi_stddev = 0.00;    // ...and its standard deviation
30 parameter real psemi = 1.0;          // Probability of growth of sCNT
31 parameter real premsemi = 0.0;       // Probability of removal of sCNT
32 parameter real premmet = 0.0;        // Probability of removal of mCNT
33 parameter integer pos_tube = 0;      // Tube position, for variab. model
34 parameter integer pos_finger = 0;    // Finger position, for variab. model
35 parameter integer num_tran = 0;      // Transistor pos., for variab. model
36 parameter real alpha_h=1.0e-4;       // Hooge's Flicker noise constant
37
38 (*cds_inherited_parameter*) parameter real seed = 0; // Seed variable,
       passed from Cadence Monte-Carlo simulator
39
40 /*****************************************************************
41 ********************** Variable declarations *******************
42 *****************************************************************/
```

```
188 // Kinetic inductance
189 real Lk;
190
191
192 //*************************** Noise model ************************
193
194 // Auxiliary variables for suppressed channel shot noise
195 real cqs;      // Source-related quantum capacitance
196 real fano_channel;  // Fano factor for suppressed channel shot noise
197
198 // Auxiliary variables for flicker noise
199 real ncarr;    // Number of carriers in the channel
200
201 // Auxiliary variables for channel-induced gate noise
202 real rd0equ, noise_gamma, noise_delta, noise_corr, noise_ratio;
203
204 // Auxiliary variables for noise at Schottky barrier
205 real Tnd, Tns, Vsbd, Vsbs;
206
207 // Power spectral densities
208 real Sch;    // PSD of suppressed channel shot noise
209 real S1f;    // PSD of flicker noise
210 real SshotRd;    // PSD of noise in doped D tube end
211 real SshotRs;    // PSD of noise in doped S tube end
212 real Ssbd;     // Thermal/shot noise at D Schottky barrier
213 real Ssbs;     // Thermal/shot noise at S Schottky barrier
214
215
216 //********************** Variability model ***********************
217
218 // Tube existing (1) or removed (0)
```

```
219 real tube;
220
221 // Conduction type semiconducting (1) or metallic (0)
222 real condtype;
223
224 // Doping level in tube extensions
225 real Efi;
226
227 // Chirality vector
228 real n1, n2;
229
230
231 /*************************************************************
232 ********************** User-defined functions *****************
233 *************************************************************/
```

```
296 /*************************************************************
297 ************* Implementation of the CNFET model equations *********
298 *************************************************************/
299
300 analog begin
301
302   /*************************************************************
303   ********************** Variability model *********************
304   *************************************************************/
305
306   @(initial_step)
307     begin : probabilities
308
309     //******** Auxiliary variables for variability model **********
310
311     // Auxiliary seed variables
312     integer seed_temp0, seed_temp1, seed_temp2, seed_offs;
313     // Main seed variables
314     integer seed_diameter, seed_condtype, seed_Efi, seed_tube;
315     // Random variables
316     real diameter, nchir, mchir;
317     // Auxiliary variable
318     integer i;
319
320
321     //******************** Calculate seeds ***********************
322
323     // Seed offset
324     seed_temp0 = seed;
325     for (i = 0; i <= 10; i = i+1) begin
326       seed_offs = $rdist_uniform(seed_temp0,100,1000000);
327     end
328
329     // seeds for random variables dependent on tube and transistor
      position
330     seed_temp1 = seed_temp0+num_tran*seed_offs+pos_tube*seed_offs*
      seed_offs;
331     seed_diameter = $rdist_uniform(seed_temp1, 1, 10000000);
332     seed_condtype = $rdist_uniform(seed_temp1, 1, 10000000);
333
334     // seeds for random variables dependent on tube and finger and
      transistor position
335     seed_temp2 = seed_temp0+num_tran*seed_offs+pos_tube*seed_offs*
      seed_offs+pos_finger*seed_offs*seed_offs*seed_offs+seed_offs*seed_offs
      *seed_offs*seed_offs;
336     seed_Efi = $rdist_uniform(seed_temp2, 1, 10000000);
337     seed_tube = $rdist_uniform(seed_temp2, 1, 10000000);
338
339
340     //*************** Evaluate chirality vector ******************
341
342     if (dist_type==0) begin // Gaussian
343       diameter = $rdist_normal(seed_diameter, dia_mean, dia_stddev);
344     end else begin // Shifted log-normal
```

```
345       diameter = exp($rdist_normal(seed_diameter, -0.4853, 0.8366))
      +0.3463;
346       diameter = diameter*1.0e-9;
347     end
348     diameter = max(diameter,0.4e-9); // limit diameters to reasonable
      values
349     diameter = min(diameter,3.5e-9);
350
351     nchir = `pi/`a*diameter;
352     mchir = 0.0;
353
354
355     //**************** Evaluate conduction type ******************
356
357     if ($rdist_uniform(seed_condtype, 0, 1)<=psemi) begin
358       condtype=1; // sCNT
359     end else begin
360       condtype=0; // mCNT
361     end
362
363
364     //****************** Evaluate doping level *******************
365
366     Efi = $rdist_normal(seed_Efi, Efi_mean, Efi_stddev);
367
368
369     //****************** Evaluate tube removal *******************
370
371     if (condtype==1) begin // if sCNT
372       if ($rdist_uniform(seed_tube, 0, 1)<=premsemi) begin
373         tube=0.0*1e-100; // Tube removed
374       end else begin
375         tube=1; // Tube stays
376       end
377     end else begin // if mCNT
378       if ($rdist_uniform(seed_tube, 0, 1)<=premmet) begin
379         tube=0.0*1e-100; // Tube removed
380       end else begin
381         tube=1; // Tube stays
382       end
383     end
384
385     // Chirality vectors to be passed to intrinsic CNFET model
386     if (tube==1) begin // Tube chirality, in case that tube exists
387       n1=nchir;
388       n2=mchir;
389     end else begin // Dummy chirality, in case that tube removed
390       n1=19.0;
391       n2=0.0;
392     end
393   end
394
395
396   /*************************************************************
397   ********** Assign basic parameters for intrinsic model **********
398   *************************************************************/
```

```
517   /*************************************************************
518   ******************** Get bias conditions ***********************
519   *************************************************************/
```

```
541   /*************************************************************
542   ******************** Evaluate sCNT current **********************
543   *************************************************************/
```

```
966   /*************************************************************
967   ******************** Evaluate mCNT current **********************
968   *************************************************************/
969
```

```
970   begin : evaluate_GMETAL
971     real Tmetal;
972
973     Tmetal = (`lambda_ap*`lambda_op)/(`lambda_ap*`lambda_op+(`lambda_ap+
        `lambda_op)*Lg);
974     GMETAL = (1.0-condtype)*4.0*hsppow(`q,2)/`h*1.0e20*Tmetal*(v_vd-v_vs)
        ;
975
976   end // End : evaluate_GMETAL
977
978   /*****************************************************************
979   ******************** Evaluate Vg_to_phib  ***********************
980   *****************************************************************/
```

```
1033  /*****************************************************************
1034  ********************** Evaluate charge_vds ***********************
1035  *****************************************************************/
```

```
1082  /*****************************************************************
1083  ***************** Evaluate intrinsic capacitances ***************
1084  *****************************************************************/
```

```
1115  /*****************************************************************
1116  ************** Charge induced by the electrodes *****************
1117  *****************************************************************/
```

```
1136  /*****************************************************************
1137  ************** Total charge induced on the sCNT surface *********
1138  *****************************************************************/
```

```
1184  /*****************************************************************
1185  ************ Assign basic parameters for extrinsic model  ********
1186  *****************************************************************/
```

```
1226  /*****************************************************************
1227  ***************** Metal-CNT coupling capacitance  ***************
1228  *****************************************************************/
```

```
1237  /*****************************************************************
1238  ************ Quantum resistance of the doped tube ends  **********
1239  *****************************************************************/
```

```
1274  /*****************************************************************
1275  ******************* Schottky barrier resistance  ****************
1276  *****************************************************************/
```

```
1371  /*****************************************************************
1372  ************************ Elastic scattering **********************
1373  *****************************************************************/
```

```
1379  /*****************************************************************
1380  *************** Gate-to-interconnect capacitance ****************
1381  *****************************************************************/
1382
1383  begin : interconnect_cap
1384    real Ctot, Cc_gate;
1385
1386    // Coupling capacitance between gates
1387    Cc_gate = `Coeff0_Cc_gate + `Coeff1_Cc_gate*Lg + `Coeff2_Cc_gate*Lg*
       Lg + `Coeff3_Cc_gate*Lg*Lg*Lg;
1388
1389    // total coupling capacitance for gate region
1390    Ctot = `Cgsub+`Cgabove+Cc_gate+Cc_gate;
1391    Cgpar = Ctot*pitch;
```

```
1392
1393    end
1394
1395
1396    /*************************************************************
1397    ********************** Kinetic inductance **********************
1398    *************************************************************/
1399
1400    Lk = 4.0e-3*Lg; // 4 nF/um
1401
1402
1403    /*************************************************************
1404    ***********************  Evaluate Fano factor ******************
1405    *************************************************************/
1406
1407    begin : evaluate_fano_factor
1408      // Evaluate the Fano factor describing the degree of shot noise
          suppression due to Coulomb and Fermi interactions
1409      // The applied method follows G. Iannaccone, J. Comp. Electronics,
          vol.3, pp.199-202, 2004.
1410
1411      // Drain and source voltage
1412      real vvd, vvs;
1413
1414      // Surface potential shift
1415      real delta_phib;
1416
1417      // Source-related quantum capacitance
1418      real cqs_1, cqs_2;
1419      real cqs_sub10, cqs_sub11, cqs_sub12, cqs_sub13, cqs_sub14, cqs_sub15
          , cqs_sub16, cqs_sub17, cqs_sub18, cqs_sub19;
1420      real cqs_sub20, cqs_sub21, cqs_sub22, cqs_sub23, cqs_sub24, cqs_sub25
          , cqs_sub26, cqs_sub27, cqs_sub28, cqs_sub29;
1421
1422      // Fermi velocity
1423      real coeff_vF;
1424      real vF_sub10, vF_sub11, vF_sub12, vF_sub13, vF_sub14, vF_sub15,
          vF_sub16, vF_sub17, vF_sub18, vF_sub19;
1425      real vF_sub20, vF_sub21, vF_sub22, vF_sub23, vF_sub24, vF_sub25,
          vF_sub26, vF_sub27, vF_sub28, vF_sub29;
1426
1427      // Weighted quantum capacitance
1428      real vs_cqs;
1429      real vs_cqs_1, vs_cqs_2;
1430      real vs_cqs_sub10, vs_cqs_sub11, vs_cqs_sub12, vs_cqs_sub13,
          vs_cqs_sub14, vs_cqs_sub15, vs_cqs_sub16, vs_cqs_sub17, vs_cqs_sub18,
          vs_cqs_sub19;
1431      real vs_cqs_sub20, vs_cqs_sub21, vs_cqs_sub22, vs_cqs_sub23,
          vs_cqs_sub24, vs_cqs_sub25, vs_cqs_sub26, vs_cqs_sub27, vs_cqs_sub28,
          vs_cqs_sub29;
1432
1433      // Fermi occupation level
1434      real fermi_s10, fermi_s11, fermi_s12, fermi_s13, fermi_s14, fermi_s15
          , fermi_s16, fermi_s17, fermi_s18, fermi_s19;
1435      real fermi_s20, fermi_s21, fermi_s22, fermi_s23, fermi_s24, fermi_s25
          , fermi_s26, fermi_s27, fermi_s28, fermi_s29;
1436
1437      // Fano factor
1438      real fano_A;
1439      real fano_A_1, fano_A_2;
1440      real fano_A_sub11, fano_A_sub12, fano_A_sub13, fano_A_sub14,
          fano_A_sub15, fano_A_sub16, fano_A_sub17, fano_A_sub18, fano_A_sub19;
1441      real fano_A_sub21, fano_A_sub22, fano_A_sub23, fano_A_sub24,
          fano_A_sub25, fano_A_sub26, fano_A_sub27, fano_A_sub28, fano_A_sub29;
1442      real fano_B;
1443      real fano_B_1, fano_B_2;
1444      real fano_B_sub11, fano_B_sub12, fano_B_sub13, fano_B_sub14,
          fano_B_sub15, fano_B_sub16, fano_B_sub17, fano_B_sub18, fano_B_sub19;
1445      real fano_B_sub21, fano_B_sub22, fano_B_sub23, fano_B_sub24,
          fano_B_sub25, fano_B_sub26, fano_B_sub27, fano_B_sub28, fano_B_sub29;
1446
```

```
1447      // Parameters passing along
1448      vvd = v_vd;
1449      vvs = v_vs;
1450      delta_phib = v_phib - v_sub;
1451
1452      // Evaluate the source-related quantum capacitance
1453      cqs_sub10=exp((E1-delta_phib)/`kT)/hsppow(1.0+exp((E1-delta_phib)/`kT
          ),2);
1454      cqs_sub11=exp((E11-delta_phib)/`kT)/hsppow(1.0+exp((E11-delta_phib)/
          `kT),2);
1455      cqs_sub12=exp((E12-delta_phib)/`kT)/hsppow(1.0+exp((E12-delta_phib)/
          `kT),2);
1456      cqs_sub13=exp((E13-delta_phib)/`kT)/hsppow(1.0+exp((E13-delta_phib)/
          `kT),2);
1457      cqs_sub14=exp((E14-delta_phib)/`kT)/hsppow(1.0+exp((E14-delta_phib)/
          `kT),2);
1458      cqs_sub15=exp((E15-delta_phib)/`kT)/hsppow(1.0+exp((E15-delta_phib)/
          `kT),2);
1459      cqs_sub16=exp((E16-delta_phib)/`kT)/hsppow(1.0+exp((E16-delta_phib)/
          `kT),2);
1460      cqs_sub17=exp((E17-delta_phib)/`kT)/hsppow(1.0+exp((E17-delta_phib)/
          `kT),2);
1461      cqs_sub18=exp((E18-delta_phib)/`kT)/hsppow(1.0+exp((E18-delta_phib)/
          `kT),2);
1462      cqs_sub19=exp((E19-delta_phib)/`kT)/hsppow(1.0+exp((E19-delta_phib)/
          `kT),2);
1463
1464      cqs_sub20=exp((E2-delta_phib)/`kT)/hsppow(1.0+exp((E2-delta_phib)/`kT
          ),2);
1465      cqs_sub21=exp((E21-delta_phib)/`kT)/hsppow(1.0+exp((E21-delta_phib)/
          `kT),2);
1466      cqs_sub22=exp((E22-delta_phib)/`kT)/hsppow(1.0+exp((E22-delta_phib)/
          `kT),2);
1467      cqs_sub23=exp((E23-delta_phib)/`kT)/hsppow(1.0+exp((E23-delta_phib)/
          `kT),2);
1468      cqs_sub24=exp((E24-delta_phib)/`kT)/hsppow(1.0+exp((E24-delta_phib)/
          `kT),2);
1469      cqs_sub25=exp((E25-delta_phib)/`kT)/hsppow(1.0+exp((E25-delta_phib)/
          `kT),2);
1470      cqs_sub26=exp((E26-delta_phib)/`kT)/hsppow(1.0+exp((E26-delta_phib)/
          `kT),2);
1471      cqs_sub27=exp((E27-delta_phib)/`kT)/hsppow(1.0+exp((E27-delta_phib)/
          `kT),2);
1472      cqs_sub28=exp((E28-delta_phib)/`kT)/hsppow(1.0+exp((E28-delta_phib)/
          `kT),2);
1473      cqs_sub29=exp((E29-delta_phib)/`kT)/hsppow(1.0+exp((E29-delta_phib)/
          `kT),2);
1474
1475      cqs_1 = cqs_sub10 + cqs_sub11 + cqs_sub12 + cqs_sub13 + cqs_sub14 +
          cqs_sub15 + cqs_sub16 + cqs_sub17 + cqs_sub18 + cqs_sub19;
1476      cqs_2 = cqs_sub20 + cqs_sub21 + cqs_sub22 + cqs_sub23 + cqs_sub24 +
          cqs_sub25 + cqs_sub26 + cqs_sub27 + cqs_sub28 + cqs_sub29;
1477
1478      cqs = `de_fac*`q/(Lgate*`kT)*(cqs_1+cqs_2);
1479
1480      // Evaluate the energy-dependent fermi-velocity vF
1481      coeff_vF = 2*`pi*hspsqrt(3.0)*`a*`Vpi*`q/`h*1e20;
1482
1483      vF_sub10 = coeff_vF*0.0/hspsqrt(hsppow(K1,2)+hsppow(0.0,2));
1484      vF_sub11 = coeff_vF*Kp1/hspsqrt(hsppow(K1,2)+hsppow(Kp1,2));
1485      vF_sub12 = coeff_vF*Kp2/hspsqrt(hsppow(K1,2)+hsppow(Kp2,2));
1486      vF_sub13 = coeff_vF*Kp3/hspsqrt(hsppow(K1,2)+hsppow(Kp3,2));
1487      vF_sub14 = coeff_vF*Kp4/hspsqrt(hsppow(K1,2)+hsppow(Kp4,2));
1488      vF_sub15 = coeff_vF*Kp5/hspsqrt(hsppow(K1,2)+hsppow(Kp5,2));
1489      vF_sub16 = coeff_vF*Kp6/hspsqrt(hsppow(K1,2)+hsppow(Kp6,2));
1490      vF_sub17 = coeff_vF*Kp7/hspsqrt(hsppow(K1,2)+hsppow(Kp7,2));
1491      vF_sub18 = coeff_vF*Kp8/hspsqrt(hsppow(K1,2)+hsppow(Kp8,2));
1492      vF_sub19 = coeff_vF*Kp9/hspsqrt(hsppow(K1,2)+hsppow(Kp9,2));
1493
1494      vF_sub20 = coeff_vF*0.0/hspsqrt(hsppow(K2,2)+hsppow(0.0,2));
1495      vF_sub21 = coeff_vF*Kp1/hspsqrt(hsppow(K2,2)+hsppow(Kp1,2));
```

```
1496      vF_sub22 = coeff_vF*Kp2/hspsqrt(hsppow(K2,2)+hsppow(Kp2,2));
1497      vF_sub23 = coeff_vF*Kp3/hspsqrt(hsppow(K2,2)+hsppow(Kp3,2));
1498      vF_sub24 = coeff_vF*Kp4/hspsqrt(hsppow(K2,2)+hsppow(Kp4,2));
1499      vF_sub25 = coeff_vF*Kp5/hspsqrt(hsppow(K2,2)+hsppow(Kp5,2));
1500      vF_sub26 = coeff_vF*Kp6/hspsqrt(hsppow(K2,2)+hsppow(Kp6,2));
1501      vF_sub27 = coeff_vF*Kp7/hspsqrt(hsppow(K2,2)+hsppow(Kp7,2));
1502      vF_sub28 = coeff_vF*Kp8/hspsqrt(hsppow(K2,2)+hsppow(Kp8,2));
1503      vF_sub29 = coeff_vF*Kp9/hspsqrt(hsppow(K2,2)+hsppow(Kp9,2));
1504
1505      // Evaluate the weighted average vS*CQS
1506      vs_cqs_sub10=vF_sub10*exp((E1-delta_phib)/`kT)/hsppow(1.0+exp((E1-
         delta_phib)/`kT),2);
1507      vs_cqs_sub11=vF_sub11*exp((E11-delta_phib)/`kT)/hsppow(1.0+exp((E11-
         delta_phib)/`kT),2);
1508      vs_cqs_sub12=vF_sub12*exp((E12-delta_phib)/`kT)/hsppow(1.0+exp((E12-
         delta_phib)/`kT),2);
1509      vs_cqs_sub13=vF_sub13*exp((E13-delta_phib)/`kT)/hsppow(1.0+exp((E13-
         delta_phib)/`kT),2);
1510      vs_cqs_sub14=vF_sub14*exp((E14-delta_phib)/`kT)/hsppow(1.0+exp((E14-
         delta_phib)/`kT),2);
1511      vs_cqs_sub15=vF_sub15*exp((E15-delta_phib)/`kT)/hsppow(1.0+exp((E15-
         delta_phib)/`kT),2);
1512      vs_cqs_sub16=vF_sub16*exp((E16-delta_phib)/`kT)/hsppow(1.0+exp((E16-
         delta_phib)/`kT),2);
1513      vs_cqs_sub17=vF_sub17*exp((E17-delta_phib)/`kT)/hsppow(1.0+exp((E17-
         delta_phib)/`kT),2);
1514      vs_cqs_sub18=vF_sub18*exp((E18-delta_phib)/`kT)/hsppow(1.0+exp((E18-
         delta_phib)/`kT),2);
1515      vs_cqs_sub19=vF_sub19*exp((E19-delta_phib)/`kT)/hsppow(1.0+exp((E19-
         delta_phib)/`kT),2);
1516
1517      vs_cqs_sub20=vF_sub20*exp((E2-delta_phib)/`kT)/hsppow(1.0+exp((E2-
         delta_phib)/`kT),2);
1518      vs_cqs_sub21=vF_sub21*exp((E21-delta_phib)/`kT)/hsppow(1.0+exp((E21-
         delta_phib)/`kT),2);
1519      vs_cqs_sub22=vF_sub22*exp((E22-delta_phib)/`kT)/hsppow(1.0+exp((E22-
         delta_phib)/`kT),2);
1520      vs_cqs_sub23=vF_sub23*exp((E23-delta_phib)/`kT)/hsppow(1.0+exp((E23-
         delta_phib)/`kT),2);
1521      vs_cqs_sub24=vF_sub24*exp((E24-delta_phib)/`kT)/hsppow(1.0+exp((E24-
         delta_phib)/`kT),2);
1522      vs_cqs_sub25=vF_sub25*exp((E25-delta_phib)/`kT)/hsppow(1.0+exp((E25-
         delta_phib)/`kT),2);
1523      vs_cqs_sub26=vF_sub26*exp((E26-delta_phib)/`kT)/hsppow(1.0+exp((E26-
         delta_phib)/`kT),2);
1524      vs_cqs_sub27=vF_sub27*exp((E27-delta_phib)/`kT)/hsppow(1.0+exp((E27-
         delta_phib)/`kT),2);
1525      vs_cqs_sub28=vF_sub28*exp((E28-delta_phib)/`kT)/hsppow(1.0+exp((E28-
         delta_phib)/`kT),2);
1526      vs_cqs_sub29=vF_sub29*exp((E29-delta_phib)/`kT)/hsppow(1.0+exp((E29-
         delta_phib)/`kT),2);
1527
1528      vs_cqs_1 = vs_cqs_sub10 + vs_cqs_sub11 + vs_cqs_sub12 + vs_cqs_sub13
         + vs_cqs_sub14 + vs_cqs_sub15 + vs_cqs_sub16 + vs_cqs_sub17 +
         vs_cqs_sub18 + vs_cqs_sub19;
1529      vs_cqs_2 = vs_cqs_sub20 + vs_cqs_sub21 + vs_cqs_sub22 + vs_cqs_sub23
         + vs_cqs_sub24 + vs_cqs_sub25 + vs_cqs_sub26 + vs_cqs_sub27 +
         vs_cqs_sub28 + vs_cqs_sub29;
1530
1531      vs_cqs = +1.0*`de_fac*`q/(Lgate*`kT)*(vs_cqs_1+vs_cqs_2);
1532
1533      // Fermi occupation levels for all substates
1534      fermi_s10 = 1.0/(1.0+exp((E1-delta_phib)/`kT));
1535      fermi_s11 = 1.0/(1.0+exp((E11-delta_phib)/`kT));
1536      fermi_s12 = 1.0/(1.0+exp((E12-delta_phib)/`kT));
1537      fermi_s13 = 1.0/(1.0+exp((E13-delta_phib)/`kT));
1538      fermi_s14 = 1.0/(1.0+exp((E14-delta_phib)/`kT));
1539      fermi_s15 = 1.0/(1.0+exp((E15-delta_phib)/`kT));
1540      fermi_s16 = 1.0/(1.0+exp((E16-delta_phib)/`kT));
1541      fermi_s17 = 1.0/(1.0+exp((E17-delta_phib)/`kT));
1542      fermi_s18 = 1.0/(1.0+exp((E18-delta_phib)/`kT));
```

```
1543      fermi_s19 = 1.0/(1.0+exp((E19-delta_phib)/`kT));
1544
1545      fermi_s20 = 1.0/(1.0+exp((E2-delta_phib)/`kT));
1546      fermi_s21 = 1.0/(1.0+exp((E21-delta_phib)/`kT));
1547      fermi_s22 = 1.0/(1.0+exp((E22-delta_phib)/`kT));
1548      fermi_s23 = 1.0/(1.0+exp((E23-delta_phib)/`kT));
1549      fermi_s24 = 1.0/(1.0+exp((E24-delta_phib)/`kT));
1550      fermi_s25 = 1.0/(1.0+exp((E25-delta_phib)/`kT));
1551      fermi_s26 = 1.0/(1.0+exp((E26-delta_phib)/`kT));
1552      fermi_s27 = 1.0/(1.0+exp((E27-delta_phib)/`kT));
1553      fermi_s28 = 1.0/(1.0+exp((E28-delta_phib)/`kT));
1554      fermi_s29 = 1.0/(1.0+exp((E29-delta_phib)/`kT));
1555
1556      // Evaluate Fano factor
1557      fano_A_sub11 = (vF_sub11*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub11),2)*
          fermi_s11*(1-fermi_s11));
1558      fano_A_sub12 = (vF_sub12*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub12),2)*
          fermi_s12*(1-fermi_s12));
1559      fano_A_sub13 = (vF_sub13*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub13),2)*
          fermi_s13*(1-fermi_s13));
1560      fano_A_sub14 = (vF_sub14*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub14),2)*
          fermi_s14*(1-fermi_s14));
1561      fano_A_sub15 = (vF_sub15*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub15),2)*
          fermi_s15*(1-fermi_s15));
1562      fano_A_sub16 = (vF_sub16*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub16),2)*
          fermi_s16*(1-fermi_s16));
1563      fano_A_sub17 = (vF_sub17*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub17),2)*
          fermi_s17*(1-fermi_s17));
1564      fano_A_sub18 = (vF_sub18*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub18),2)*
          fermi_s18*(1-fermi_s18));
1565      fano_A_sub19 = (vF_sub19*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub19),2)*
          fermi_s19*(1-fermi_s19));
1566
1567      fano_A_sub21 = (vF_sub21*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub21),2)*
          fermi_s21*(1-fermi_s21));
1568      fano_A_sub22 = (vF_sub22*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub22),2)*
          fermi_s22*(1-fermi_s22));
1569      fano_A_sub23 = (vF_sub23*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub23),2)*
          fermi_s23*(1-fermi_s23));
1570      fano_A_sub24 = (vF_sub24*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub24),2)*
          fermi_s24*(1-fermi_s24));
1571      fano_A_sub25 = (vF_sub25*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub25),2)*
          fermi_s25*(1-fermi_s25));
1572      fano_A_sub26 = (vF_sub26*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub26),2)*
          fermi_s26*(1-fermi_s26));
1573      fano_A_sub27 = (vF_sub27*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub27),2)*
          fermi_s27*(1-fermi_s27));
1574      fano_A_sub28 = (vF_sub28*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub28),2)*
          fermi_s28*(1-fermi_s28));
1575      fano_A_sub29 = (vF_sub29*hsppow(1-vs_cqs/((cqs+Ci)*vF_sub29),2)*
          fermi_s29*(1-fermi_s29));
1576
1577      fano_A_1 = fano_A_sub11 + fano_A_sub12 + fano_A_sub13 + fano_A_sub14
          + fano_A_sub15 + fano_A_sub16 + fano_A_sub17 + fano_A_sub18 +
          fano_A_sub19;
1578      fano_A_2 = fano_A_sub21 + fano_A_sub22 + fano_A_sub23 + fano_A_sub24
          + fano_A_sub25 + fano_A_sub26 + fano_A_sub27 + fano_A_sub28 +
          fano_A_sub29;
1579
1580      fano_A = `de_fac/Lgate*(fano_A_1+fano_A_2);
1581
1582      fano_B_sub11 = vF_sub11*fermi_s11;
1583      fano_B_sub12 = vF_sub12*fermi_s12;
1584      fano_B_sub13 = vF_sub13*fermi_s13;
1585      fano_B_sub14 = vF_sub14*fermi_s14;
1586      fano_B_sub15 = vF_sub15*fermi_s15;
1587      fano_B_sub16 = vF_sub16*fermi_s16;
1588      fano_B_sub17 = vF_sub17*fermi_s17;
1589      fano_B_sub18 = vF_sub18*fermi_s18;
1590      fano_B_sub19 = vF_sub19*fermi_s19;
1591
```

```
1592      fano_B_sub21 = vF_sub21*fermi_s21;
1593      fano_B_sub22 = vF_sub22*fermi_s22;
1594      fano_B_sub23 = vF_sub23*fermi_s23;
1595      fano_B_sub24 = vF_sub24*fermi_s24;
1596      fano_B_sub25 = vF_sub25*fermi_s25;
1597      fano_B_sub26 = vF_sub26*fermi_s26;
1598      fano_B_sub27 = vF_sub27*fermi_s27;
1599      fano_B_sub28 = vF_sub28*fermi_s28;
1600      fano_B_sub29 = vF_sub29*fermi_s29;
1601
1602      fano_B_1 = fano_B_sub11 + fano_B_sub12 + fano_B_sub13 + fano_B_sub14
          + fano_B_sub15 + fano_B_sub16 + fano_B_sub17 + fano_B_sub18 +
          fano_B_sub19;
1603      fano_B_2 = fano_B_sub21 + fano_B_sub22 + fano_B_sub23 + fano_B_sub24
          + fano_B_sub25 + fano_B_sub26 + fano_B_sub27 + fano_B_sub28 +
          fano_B_sub29;
1604
1605      fano_B = `de_fac/Lgate*(fano_B_1+fano_B_2);
1606
1607      // Overall Fano factor for the suppressed channel shot noise
1608      fano_channel = fano_A/fano_B;
1609
1610    end // End: evaluate_fano_factor
1611
1612
1613    /*************************************************************
1614    ******************** Evaluate noise sources ******************
1615    *************************************************************/
1616
1617    // Evaluate noise PSDs of the different noise sources
1618    begin : evaluate_noisepow
1619
1620      real Ichannel; // Channel current
1621      real vF;       // Fermi velocity of mCNTs
1622      real fano_end; // Fano factor of diffusive metallic wire
1623
1624
1625      //****** Assign basic parameters for noise calculations *******
1626
1627      // Channel current, valid both for sCNTs and mCNTs
1628      Ichannel = GCNT+GMETAL;
1629
1630      // Fermi velocity of mCNTs approximated as 10^6 m/s
1631      vF = 1.0e6;
1632
1633
1634      //************ Suppressed channel shot noise PSD **************
1635
1636      if (condtype==1) begin
1637        // sCNT: suppressed channel shot noise
1638        Sch = 2*`q*Ichannel*fano_channel;
1639      end else begin
1640        // mCNT: ballistic channel without shot noise
1641        Sch = 0;
1642      end
1643
1644
1645      //***************** Channel flicker noise PSD *****************
1646
1647      // Number of carriers in the channel for flicker noise evaluation
1648      if (condtype==1) begin // sCNT
1649        ncarr = G_Qchannel/`q*Lg;
1650      end else begin // mCNT
1651        ncarr = Ichannel/(`q*vF)*Lg;
1652      end
1653
1654      // Flicker noise PSD
1655      S1f = alpha_h/ncarr*hsppow(Ichannel,2);
1656
1657
1658      //************ Shot noise PSD for doped tube ends *************
```

```
1659
1660      // Noise at doped D/S tube ends (diffusive metallic wire with elastic
           scattering)
1661      fano_end = 1.0/3.0*(1.0-1.0/hsppow(1+Lss/`Leff,3));
1662      SshotRd = 2*`q*I(Drain_b,Drain_lk)*fano_end;
1663      SshotRs = 2*`q*I(Source_lk,Source_b)*fano_end;
1664
1665      // Thermal/shot noise at D/S Schottky barrier
1666      Vsbd = V(Drain,Drain_b);
1667      Vsbs = V(Source_b,Source);
1668      Ssbd = 4*hsppow(`q,2)/(`h*1e-20)*(4*`k*`q*(`TEMP+273)*hsppow(Tnd,2)
          +2*Tnd*(1-Tnd)*`q*Vsbd*((exp((`q*Vsbd)/(2*`k*`q*(`TEMP+273)))+exp((-`q
          *Vsbd)/(2*`k*`q*(`TEMP+273))))/(exp((`q*Vsbd)/(2*`k*`q*(`TEMP+273)))-
          exp((-`q*Vsbd)/(2*`k*`q*(`TEMP+273))))))*tube;
1669      Ssbs = 4*hsppow(`q,2)/(`h*1e-20)*(4*`k*`q*(`TEMP+273)*hsppow(Tns,2)
          +2*Tns*(1-Tns)*`q*Vsbs*((exp((`q*Vsbs)/(2*`k*`q*(`TEMP+273)))+exp((-`q
          *Vsbs)/(2*`k*`q*(`TEMP+273))))/(exp((`q*Vsbs)/(2*`k*`q*(`TEMP+273)))-
          exp((-`q*Vsbs)/(2*`k*`q*(`TEMP+273))))))*tube;
1670
1671      // Constants for channel-induced gate noise, following van der Ziel
1672      noise_corr = 0.395;
1673      noise_gamma = 2.0/3.0;
1674      noise_delta = 4.0/3.0;
1675
1676      // Equivalent rd0 resistance
1677      rd0equ = 4.0*`k*`q*(`TEMP+273)*noise_gamma/(Sch);
1678
1679      // Noise ratio Sig/Sid at omega=1
1680      noise_ratio = 2.0/5.0*hsppow(Cgs,2.0)*hsppow(rd0equ,2.0)*condtype;
1681
1682   end // End : evaluate_noisepow
1683
1684
1685   /*************************************************************
1686   ********************** Place components **********************
1687   *************************************************************/
1688
1689   // Generate correlated channel/gate noise
1690   I(Noise) <+ V(Noise)*1.0; // Auxiliary node for correlated noise
1691   I(Noise) <+ white_noise(Sch*tube, "Corr");
1692   // Placing components
1693   // Voltage Controlled channel current source
1694   I(Drain_int,Source_int)  <+ (GCNT+GMETAL)*tube;
1695   // Channel and gate-induced noise
1696   I(Drain_int, Source_int) <+ white_noise((1.0-noise_corr*noise_corr)*Sch
        *tube, "Uncorr"); // Uncorr. channel noise
1697   I(Drain_int, Source_int) <+ noise_corr*V(Noise); // Corr. channel noise
1698   I(Gate, Source_int)      <+ ddt(V(Noise)*sqrt(noise_ratio)*tube); //
        Gate noise
1699
1700   // Flicker noise
1701   I(Drain_int,Source_int)  <+ flicker_noise(S1f*tube,1.0,"S1f");
1702
1703   // Intrinsic gate to Source/Drain/Sub capacitance
1704   I(Source_int,Vgate) <+ ddt(Csg*V(Source_int,Vgate)*tube);
1705   I(Drain_int,Vgate)  <+ ddt(Cdg*V(Drain_int,Vgate)*tube);
1706   I(Gate,mid2)        <+ ddt(Cbg*V(Gate,mid2)*tube);
1707   I(Gate,Vsource_int) <+ ddt(Cgs*V(Gate,Vsource_int)*tube);
1708   I(Gate,Vdrain_int)  <+ ddt(Cgd*V(Gate,Vdrain_int)*tube);
1709   I(Source_int,VsubM) <+ ddt(Csb*V(Source_int,VsubM)*tube);
1710   I(Drain_int,VsubM)  <+ ddt(Cdb*V(Drain_int,VsubM)*tube);
1711
1712   // Coupling cap. between metal Gate stack and doped D/S CNT
1713   I(Gate,Source_int)  <+ ddt(Cgss*V(Gate,Source_int)*tube);
1714   I(Gate,Drain_int)   <+ ddt(Cgdd*V(Gate,Drain_int)*tube);
1715
1716   // Substrate resistance
1717   V(mid2,Sub)         <+ `Rsub*I(mid2,Sub);
1718
1719   // delta_phib
1720   I(Vdrain_int,phib)  <+ G_Qtotal;
```

```
1721   I(phib,Sub)          <+ G_Qchannel;
1722
1723   // The dummy controlled voltage source to get vds and delta_phi
1724   V(Vdrain_int,Sub)    <+ 1.0*V(Drain_int,Sub);
1725   V(Vgate,Sub)         <+ 1.0*V(Gate,Sub);
1726   V(Vsource_int,Sub)   <+ 1.0*V(Source_int,Sub);
1727   V(VsubM)             <+ 1.0*V(Sub);
1728
1729   // The coupling caps between CNTs, CNT and below/above plane
1730   I(Drain_b,Sub)    <+ ddt(Cd1*V(Drain_b,Sub)*tube);
1731   I(Drain_lk,Sub)   <+ ddt(Cd2*V(Drain_lk,Sub)*tube);
1732   I(Source_b,Sub)   <+ ddt(Cs1*V(Source_b,Sub)*tube);
1733   I(Source_lk,Sub)  <+ ddt(Cs2*V(Source_lk,Sub)*tube);
1734
1735   // Gate-interconnect coupling capacitance
1736   I(Gate,Sub)       <+ ddt(Cgpar*V(Gate,Sub));
1737
1738   // Extrinsic resistors
1739   I(Drain,Drain_b)         <+ (1.0/Rsbd)*V(Drain,Drain_b)+white_noise(Ssbd
        *tube,"Ssbd"); // The Schottky Barrier at drain side
1740   I(Drain_b,Drain_lk)      <+ (1.0/Rd)*V(Drain_b,Drain_lk)+white_noise(
        SshotRd*tube,"SshotRd"); // The res. at doped tube at drain side
1741   I(Source_lk,Source_b)    <+ (1.0/Rs)*V(Source_lk,Source_b)+white_noise(
        SshotRs*tube,"SshotRs"); // The resistance at doped tube at source
        side
1742   I(Source_b,Source)       <+ (1.0/Rsbs)*V(Source_b,Source)+white_noise(
        Ssbs*tube,"Ssbs"); // The Schottky Barrier at source side
1743
1744   // Voltage Controlled source for elastic scattering in channel
1745   V(Drain_ch,Drain_int)    <+ 1.0*EDDin;
1746
1747   // Kinetic inductance
1748   V(Drain_lk,Drain_ch)     <+ 0.5*Lk*ddt(I(Drain_lk,Drain_ch)*tube); //
        Part of kinetic inductance assigned to drain side
1749   V(Source_int,Source_lk) <+ 0.5*Lk*ddt(I(Source_int,Source_lk)*tube); //
         Part of kinetic inductance assigned to source side
1750
1751   // Required to include coupling effects of potentials at D/S electrodes
         on intrinsic channel
1752   V(CoupleNode,Sub)        <+ V(Drain_int,Sub);
1753
1754   end // End: analog begin
1755
1756 endmodule
```

The following `parameters.vams` source code is a modified version of the source code provided with the original Stanford CNFET compact model [135].

parameters.vams

```
1  // ---- Temperature
2  `define TEMP  27.0           // Room temperature
3
4  // ---- Natural constants ----
5  `define q 1.60e-19           // Electronic charge
6  `define Vpi 3.033            // Carbon pi-pi bond energy
7  `define d 0.144e-9           // Carbon pi-pi bond distance
8  `define a 0.2495e-9          // Carbon lattice constant
9  `define pi 3.1416            // Pi constant
10 `define h 6.63e-14           // Planck constant, x1e20
11 `define h_ba 1.0552e-14      // Red. Planck constant, x1e20
12 `define k 8.617e-5           // Boltzmann constant divided by q
```

```
13 `define epso 8.85e-12         // Dielectric constant in vacuum
14 `define kT (`k*(`TEMP+273.0))// The kT constant divided by q, at 300K
15
16 // ---- Model parameters ----
17
18 // Carrier scattering
19 `define Lgeff 200.0e-9      // Estimated MFP in intrinsic CNT
20 `define Leff 15.0e-9        // Estimated MFP in p+/n+ doped CNT
21 `define lambda_op 15.0e-9   // Optical phonon backscattering MFP with mCNT
22 `define lambda_ap 500.0e-9 // Acoustic phonon backscatt. MFP with mCNT
23 `define photon 0.16         // Photon energy, typical value
24
25 // Work functions and flat-band voltage
26 `define phi_M 4.5 // Metal workfunction
27 `define phi_S 4.5 // CNT workfunction
28 `define Vfbn 0.0  // Flat-band voltage
29
30 // Capacitances
31 `define Ksub 3.9                    // Dielectric constant of SiO2
32 `define Cgsub 30e-12                // Metal gate to substrate fringe
      capacitance per unit length, approximated as 30af/um, with 10um SiO2
33 `define Cgabove 27e-12              // Local interconnect to M1 coupling
      capacitance, 500nm apart, infinite large plane
34 `define Ccabove 15e-12              // Coupling capacitance between CNT
      and the above M1 layer, 500nm apart
35 `define Coeff0_Cc_gate 3.17372e-10  // Polynomial fit of capacitance
      between gates, valid for Lg=Ls=Ld in a range between 16 and 64nm, Hg
      =64nm, k=3.9
36 `define Coeff1_Cc_gate -0.0119797   // ...
37 `define Coeff2_Cc_gate 2.17192e+05  // ...
38 `define Coeff3_Cc_gate -1.39439e+12 // ...
39 `define Coeff1_Cgsd 20.55e-12       // Slope for Cg_sd vs. Lsd, H=64nm, K
      =3.9, contact spacing 32nm, valid for 10nm<Lsd<100nm
40 `define Coeff2_Cgsd 0.55e-18        // The intersection of Cg_sd vs. Lsd,
       H=64nm, K=3.9, contact spacing 32nm, valid for 10nm<Lsd<100nm
41 `define Coeff_Cc (`pi*3.9*`epso)    // The coefficient of the coupling
      capacitance between adjacent CNTs
42 `define Csub 20.0e-12               // Csub is CNT to Substrate
      capacitance per unit length,approximated as 20af/um with 10um thick
      SiO2
43 `define Ccsd 0.0e-13                // Coupling capacitance between
      channel region and source/drain islands
44 `define CoupleRatio 0.5             // Percentage of coupling capacitance
       between channel and drain out of the total fringe capacitance Ccsd
45 `define GF 1.0                      // Consider (1) or not (0) the impact
       of the gate-tube end region parasitic capacitance
46
47 // Other constants
48 `define Rsub 0.0       // Substrate resistance, set to zero for the ideal
       case
49 `define Lgmax 100.0e-9 // Maximum channel length to calculate current for
       short channel device
50
51 // Do not change
52 `define coeffj (4*`q/`h*`q/1e-20) // Coefficient of current component, 4
      is due to both spin degeneracy and mode degeneracy
53 `define de_fac 4.0                // Factor to calculate the number of
      electrons in CNT
54 `define CNTPos 0.0                // Position in the middle of the array
      if CNTPos=0, edge position if CNTPos=1
55 `define Dout 0.0                 // 1 if connected to doped tube, 0 if
      connected to metal electrode
56 `define Sout 0.0                 // 1 if connected to doped tube, 0 if
      connected to metal electrode
```

B.2 CNFET model - Level 2

veriloga.va

```
1  `include "disciplines.vams"
2  `include "parameters.vams"
3
4  module NCNFET_L2(Drain, Gate, Source, Sub);
5
6  /*************************************************************
7  ********************* Electrical nodes ***********************
8  *************************************************************/
9
10 inout Drain, Gate, Source, Sub;
11
12 electrical Drain, Gate, Gate_res, Source, Sub;
13
14 electrical Drain_int_0, Drain_int_1, Drain_int_2, Drain_int_3,
       Drain_int_4, Drain_int_5, Drain_int_6, Drain_int_7, Drain_int_8,
       Drain_int_9;
15 electrical Gate_res_int_0, Gate_res_int_1, Gate_res_int_2, Gate_res_int_3
       , Gate_res_int_4, Gate_res_int_5, Gate_res_int_6, Gate_res_int_7,
       Gate_res_int_8, Gate_res_int_9;
16 electrical Source_int_0, Source_int_1, Source_int_2, Source_int_3,
       Source_int_4, Source_int_5, Source_int_6, Source_int_7, Source_int_8,
       Source_int_9;
17 electrical Sub_int_0, Sub_int_1, Sub_int_2, Sub_int_3, Sub_int_4,
       Sub_int_5, Sub_int_6, Sub_int_7, Sub_int_8, Sub_int_9;
18
19 electrical Drain_vir_0, Drain_vir_1, Drain_vir_2, Drain_vir_3,
       Drain_vir_4, Drain_vir_5, Drain_vir_6, Drain_vir_7, Drain_vir_8,
       Drain_vir_9;
20 electrical Gate_res_vir_0, Gate_res_vir_1, Gate_res_vir_2, Gate_res_vir_3
       , Gate_res_vir_4, Gate_res_vir_5, Gate_res_vir_6, Gate_res_vir_7,
       Gate_res_vir_8, Gate_res_vir_9;
21 electrical Source_vir_0, Source_vir_1, Source_vir_2, Source_vir_3,
       Source_vir_4, Source_vir_5, Source_vir_6, Source_vir_7, Source_vir_8,
       Source_vir_9;
22 electrical Sub_vir_0, Sub_vir_1, Sub_vir_2, Sub_vir_3, Sub_vir_4,
       Sub_vir_5, Sub_vir_6, Sub_vir_7, Sub_vir_8, Sub_vir_9;
23
24
25 /*************************************************************
26 ********************* Input parameters ***********************
27 *************************************************************/
28
29 parameter real Lg=32.0e-9;          // CNFET channel/gate length
30 parameter real pitch=10.0e-9;       // Tube pitch
31 parameter real Kgate=16.0;          // High-k gate dielectric constant
32 parameter real Tox=4.0e-9;          // Gate oxide thickness
33 parameter integer dist_type = 0;    // Diameter distribution: Gaussian =
       0, shifted log-normal = 1
34 parameter real dia_mean = 1.5e-9;   // Tube diameter
35 parameter real dia_stddev = 0.0e-9; // ...and its standard deviation
36 parameter real Efi_mean = 0.66;     // The n+ doped CNT fermi level (eV),
        0.66eV for 1% doping level, 0.6eV for 0.8% doping level
37 parameter real Efi_stddev = 0.00;   // ...and its standard deviation
38 parameter real psemi = 1.0;         // Probability of growth of sCNT
39 parameter real premsemi = 0.0;      // Probability of removal of sCNT
40 parameter real premmet = 0.0;       // Probability of removal of mCNT
41 parameter integer numtubes = 1 from [1:10]; // Number of tubes
42 parameter integer pos_finger = 0;   // Finger position, for variab. model
43 parameter integer num_tran = 0;     // Transistor pos., for variab. model
44 parameter real alpha_h=1.0e-4;      // Hooge's Flicker noise constant
45
46
47 /*************************************************************
48 ********* Instantiate Level 1 models (single tubes) **********
```

```
49 ************************************************************/
50
51 NCNFET_L1 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       pos_tube(0.0),.pos_finger(pos_finger),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET00 (Drain_int_0, Gate_res_int_0,
       Source_int_0, Sub_int_0);
52 NCNFET_L1 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       pos_tube(1.0),.pos_finger(pos_finger),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET01 (Drain_int_1, Gate_res_int_1,
       Source_int_1, Sub_int_1);
53 NCNFET_L1 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       pos_tube(2.0),.pos_finger(pos_finger),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET02 (Drain_int_2, Gate_res_int_2,
       Source_int_2, Sub_int_2);
54 NCNFET_L1 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       pos_tube(3.0),.pos_finger(pos_finger),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET03 (Drain_int_3, Gate_res_int_3,
       Source_int_3, Sub_int_3);
55 NCNFET_L1 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       pos_tube(4.0),.pos_finger(pos_finger),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET04 (Drain_int_4, Gate_res_int_4,
       Source_int_4, Sub_int_4);
56 NCNFET_L1 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       pos_tube(5.0),.pos_finger(pos_finger),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET05 (Drain_int_5, Gate_res_int_5,
       Source_int_5, Sub_int_5);
57 NCNFET_L1 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       pos_tube(6.0),.pos_finger(pos_finger),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET06 (Drain_int_6, Gate_res_int_6,
       Source_int_6, Sub_int_6);
58 NCNFET_L1 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       pos_tube(7.0),.pos_finger(pos_finger),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET07 (Drain_int_7, Gate_res_int_7,
       Source_int_7, Sub_int_7);
59 NCNFET_L1 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       pos_tube(8.0),.pos_finger(pos_finger),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET08 (Drain_int_8, Gate_res_int_8,
       Source_int_8, Sub_int_8);
60 NCNFET_L1 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       pos_tube(9.0),.pos_finger(pos_finger),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET09 (Drain_int_9, Gate_res_int_9,
       Source_int_9, Sub_int_9);
61
62
63 /************************************************************
64 ****************** Level 2 implementation ******************
65 ************************************************************/
66
67 analog begin : model_L2
68
69   real Rgate;
```

```
70   real R0, R1, R2, R3, R4, R5, R6, R7, R8, R9;
71   real R0vir, R1vir, R2vir, R3vir, R4vir, R5vir, R6vir, R7vir, R8vir,
       R9vir;
72
73
74   //********* Evaluate parasitic gate finger resistance **********
75
76   begin : gate_resistance
77     Rgate = (`rho_g/`tg)*(pitch/Lg)*1.0/3.0;
78   end
79
80
81   //************** Evaluate shunt resistance values **************
82
83   begin : connectors
84
85     if (numtubes >= 1) begin
86       R0 = 1.00e-6;
87       R0vir = 1.0e12;
88     end else begin
89       R0 = 1.0e12;
90       R0vir = 1.00e-6;
91     end
92     if (numtubes >= 2) begin
93       R1 = 1.00e-6;
94       R1vir = 1.0e12;
95     end else begin
96       R1 = 1.0e12;
97       R1vir = 1.00e-6;
98     end
99     if (numtubes >= 3) begin
100      R2 = 1.00e-6;
101      R2vir = 1.0e12;
102    end else begin
103      R2 = 1.0e12;
104      R2vir = 1.00e-6;
105    end
106    if (numtubes >= 4) begin
107      R3 = 1.00e-6;
108      R3vir = 1.0e12;
109    end else begin
110      R3 = 1.0e12;
111      R3vir = 1.00e-6;
112    end
113    if (numtubes >= 5) begin
114      R4 = 1.00e-6;
115      R4vir = 1.0e12;
116    end else begin
117      R4 = 1.0e12;
118      R4vir = 1.00e-6;
119    end
120    if (numtubes >= 6) begin
121      R5 = 1.00e-6;
122      R5vir = 1.0e12;
123    end else begin
124      R5 = 1.0e12;
125      R5vir = 1.00e-6;
126    end
127    if (numtubes >= 7) begin
128      R6 = 1.00e-6;
129      R6vir = 1.0e12;
130    end else begin
131      R6 = 1.0e12;
132      R6vir = 1.00e-6;
133    end
134    if (numtubes >= 8) begin
135      R7 = 1.00e-6;
136      R7vir = 1.0e12;
137    end else begin
138      R7 = 1.0e12;
139      R7vir = 1.00e-6;
```

```
140     end
141     if (numtubes >= 9) begin
142       R8 = 1.00e-6;
143       R8vir = 1.0e12;
144     end else begin
145       R8 = 1.0e12;
146       R8vir = 1.00e-6;
147     end
148     if (numtubes >= 10) begin
149       R9 = 1.00e-6;
150       R9vir = 1.0e12;
151     end else begin
152       R9 = 1.0e12;
153       R9vir = 1.00e-6;
154     end
155
156   end
157
158
159   /*************************************************************
160   ********************** Place components **********************
161   *************************************************************/
162
163   //************** Parasitic gate resistance *********************
164
165   V(Gate,Gate_res) <+ Rgate*I(Gate,Gate_res)+ white_noise(4*`k*`q*(`TEMP
        +273)/Rgate,"gate_therm");
166
167
168   //**** Connection of Level 1 devices to ext. Level 2 nodes *****
169
170   V(Drain_int_0,Drain) <+ R0*I(Drain_int_0,Drain);
171   V(Drain_int_1,Drain) <+ R1*I(Drain_int_1,Drain);
172   V(Drain_int_2,Drain) <+ R2*I(Drain_int_2,Drain);
173   V(Drain_int_3,Drain) <+ R3*I(Drain_int_3,Drain);
174   V(Drain_int_4,Drain) <+ R4*I(Drain_int_4,Drain);
175   V(Drain_int_5,Drain) <+ R5*I(Drain_int_5,Drain);
176   V(Drain_int_6,Drain) <+ R6*I(Drain_int_6,Drain);
177   V(Drain_int_7,Drain) <+ R7*I(Drain_int_7,Drain);
178   V(Drain_int_8,Drain) <+ R8*I(Drain_int_8,Drain);
179   V(Drain_int_9,Drain) <+ R9*I(Drain_int_9,Drain);
180
181   V(Gate_res_int_0,Gate_res) <+ R0*I(Gate_res_int_0,Gate_res);
182   V(Gate_res_int_1,Gate_res) <+ R1*I(Gate_res_int_1,Gate_res);
183   V(Gate_res_int_2,Gate_res) <+ R2*I(Gate_res_int_2,Gate_res);
184   V(Gate_res_int_3,Gate_res) <+ R3*I(Gate_res_int_3,Gate_res);
185   V(Gate_res_int_4,Gate_res) <+ R4*I(Gate_res_int_4,Gate_res);
186   V(Gate_res_int_5,Gate_res) <+ R5*I(Gate_res_int_5,Gate_res);
187   V(Gate_res_int_6,Gate_res) <+ R6*I(Gate_res_int_6,Gate_res);
188   V(Gate_res_int_7,Gate_res) <+ R7*I(Gate_res_int_7,Gate_res);
189   V(Gate_res_int_8,Gate_res) <+ R8*I(Gate_res_int_8,Gate_res);
190   V(Gate_res_int_9,Gate_res) <+ R9*I(Gate_res_int_9,Gate_res);
191
192   V(Source_int_0,Source) <+ R0*I(Source_int_0,Source);
193   V(Source_int_1,Source) <+ R1*I(Source_int_1,Source);
194   V(Source_int_2,Source) <+ R2*I(Source_int_2,Source);
195   V(Source_int_3,Source) <+ R3*I(Source_int_3,Source);
196   V(Source_int_4,Source) <+ R4*I(Source_int_4,Source);
197   V(Source_int_5,Source) <+ R5*I(Source_int_5,Source);
198   V(Source_int_6,Source) <+ R6*I(Source_int_6,Source);
199   V(Source_int_7,Source) <+ R7*I(Source_int_7,Source);
200   V(Source_int_8,Source) <+ R8*I(Source_int_8,Source);
201   V(Source_int_9,Source) <+ R9*I(Source_int_9,Source);
202
203   V(Sub_int_0,Sub) <+ R0*I(Sub_int_0,Sub);
204   V(Sub_int_1,Sub) <+ R1*I(Sub_int_1,Sub);
205   V(Sub_int_2,Sub) <+ R2*I(Sub_int_2,Sub);
206   V(Sub_int_3,Sub) <+ R3*I(Sub_int_3,Sub);
207   V(Sub_int_4,Sub) <+ R4*I(Sub_int_4,Sub);
208   V(Sub_int_5,Sub) <+ R5*I(Sub_int_5,Sub);
209   V(Sub_int_6,Sub) <+ R6*I(Sub_int_6,Sub);
```

```
210   V(Sub_int_7,Sub) <+ R7*I(Sub_int_7,Sub);
211   V(Sub_int_8,Sub) <+ R8*I(Sub_int_8,Sub);
212   V(Sub_int_9,Sub) <+ R9*I(Sub_int_9,Sub);
213
214
215   //******* Connection of Level 1 devices to dummy nodes *******
216
217   V(Drain_int_0,Drain_vir_0) <+ R0vir*I(Drain_int_0,Drain_vir_0);
218   V(Drain_int_1,Drain_vir_1) <+ R1vir*I(Drain_int_1,Drain_vir_1);
219   V(Drain_int_2,Drain_vir_2) <+ R2vir*I(Drain_int_2,Drain_vir_2);
220   V(Drain_int_3,Drain_vir_3) <+ R3vir*I(Drain_int_3,Drain_vir_3);
221   V(Drain_int_4,Drain_vir_4) <+ R4vir*I(Drain_int_4,Drain_vir_4);
222   V(Drain_int_5,Drain_vir_5) <+ R5vir*I(Drain_int_5,Drain_vir_5);
223   V(Drain_int_6,Drain_vir_6) <+ R6vir*I(Drain_int_6,Drain_vir_6);
224   V(Drain_int_7,Drain_vir_7) <+ R7vir*I(Drain_int_7,Drain_vir_7);
225   V(Drain_int_8,Drain_vir_8) <+ R8vir*I(Drain_int_8,Drain_vir_8);
226   V(Drain_int_9,Drain_vir_9) <+ R9vir*I(Drain_int_9,Drain_vir_9);
227
228   V(Gate_res_int_0,Gate_res_vir_0) <+ R0vir*I(Gate_res_int_0,
        Gate_res_vir_0);
229   V(Gate_res_int_1,Gate_res_vir_1) <+ R1vir*I(Gate_res_int_1,
        Gate_res_vir_1);
230   V(Gate_res_int_2,Gate_res_vir_2) <+ R2vir*I(Gate_res_int_2,
        Gate_res_vir_2);
231   V(Gate_res_int_3,Gate_res_vir_3) <+ R3vir*I(Gate_res_int_3,
        Gate_res_vir_3);
232   V(Gate_res_int_4,Gate_res_vir_4) <+ R4vir*I(Gate_res_int_4,
        Gate_res_vir_4);
233   V(Gate_res_int_5,Gate_res_vir_5) <+ R5vir*I(Gate_res_int_5,
        Gate_res_vir_5);
234   V(Gate_res_int_6,Gate_res_vir_6) <+ R6vir*I(Gate_res_int_6,
        Gate_res_vir_6);
235   V(Gate_res_int_7,Gate_res_vir_7) <+ R7vir*I(Gate_res_int_7,
        Gate_res_vir_7);
236   V(Gate_res_int_8,Gate_res_vir_8) <+ R8vir*I(Gate_res_int_8,
        Gate_res_vir_8);
237   V(Gate_res_int_9,Gate_res_vir_9) <+ R9vir*I(Gate_res_int_9,
        Gate_res_vir_9);
238
239   V(Source_int_0,Source_vir_0) <+ R0vir*I(Source_int_0,Source_vir_0);
240   V(Source_int_1,Source_vir_1) <+ R1vir*I(Source_int_1,Source_vir_1);
241   V(Source_int_2,Source_vir_2) <+ R2vir*I(Source_int_2,Source_vir_2);
242   V(Source_int_3,Source_vir_3) <+ R3vir*I(Source_int_3,Source_vir_3);
243   V(Source_int_4,Source_vir_4) <+ R4vir*I(Source_int_4,Source_vir_4);
244   V(Source_int_5,Source_vir_5) <+ R5vir*I(Source_int_5,Source_vir_5);
245   V(Source_int_6,Source_vir_6) <+ R6vir*I(Source_int_6,Source_vir_6);
246   V(Source_int_7,Source_vir_7) <+ R7vir*I(Source_int_7,Source_vir_7);
247   V(Source_int_8,Source_vir_8) <+ R8vir*I(Source_int_8,Source_vir_8);
248   V(Source_int_9,Source_vir_9) <+ R9vir*I(Source_int_9,Source_vir_9);
249
250   V(Sub_int_0,Sub_vir_0) <+ R0vir*I(Sub_int_0,Sub_vir_0);
251   V(Sub_int_1,Sub_vir_1) <+ R1vir*I(Sub_int_1,Sub_vir_1);
252   V(Sub_int_2,Sub_vir_2) <+ R2vir*I(Sub_int_2,Sub_vir_2);
253   V(Sub_int_3,Sub_vir_3) <+ R3vir*I(Sub_int_3,Sub_vir_3);
254   V(Sub_int_4,Sub_vir_4) <+ R4vir*I(Sub_int_4,Sub_vir_4);
255   V(Sub_int_5,Sub_vir_5) <+ R5vir*I(Sub_int_5,Sub_vir_5);
256   V(Sub_int_6,Sub_vir_6) <+ R6vir*I(Sub_int_6,Sub_vir_6);
257   V(Sub_int_7,Sub_vir_7) <+ R7vir*I(Sub_int_7,Sub_vir_7);
258   V(Sub_int_8,Sub_vir_8) <+ R8vir*I(Sub_int_8,Sub_vir_8);
259   V(Sub_int_9,Sub_vir_9) <+ R9vir*I(Sub_int_9,Sub_vir_9);
260
261
262   //*************** VCV-Sources for dummy nodes ***************
263
264   V(Drain_vir_0) <+ V(Drain);
265   V(Drain_vir_1) <+ V(Drain);
266   V(Drain_vir_2) <+ V(Drain);
267   V(Drain_vir_3) <+ V(Drain);
268   V(Drain_vir_4) <+ V(Drain);
269   V(Drain_vir_5) <+ V(Drain);
270   V(Drain_vir_6) <+ V(Drain);
```

```
271   V(Drain_vir_7) <+ V(Drain);
272   V(Drain_vir_8) <+ V(Drain);
273   V(Drain_vir_9) <+ V(Drain);
274
275   V(Gate_res_vir_0) <+ V(Gate_res);
276   V(Gate_res_vir_1) <+ V(Gate_res);
277   V(Gate_res_vir_2) <+ V(Gate_res);
278   V(Gate_res_vir_3) <+ V(Gate_res);
279   V(Gate_res_vir_4) <+ V(Gate_res);
280   V(Gate_res_vir_5) <+ V(Gate_res);
281   V(Gate_res_vir_6) <+ V(Gate_res);
282   V(Gate_res_vir_7) <+ V(Gate_res);
283   V(Gate_res_vir_8) <+ V(Gate_res);
284   V(Gate_res_vir_9) <+ V(Gate_res);
285
286   V(Source_vir_0) <+ V(Source);
287   V(Source_vir_1) <+ V(Source);
288   V(Source_vir_2) <+ V(Source);
289   V(Source_vir_3) <+ V(Source);
290   V(Source_vir_4) <+ V(Source);
291   V(Source_vir_5) <+ V(Source);
292   V(Source_vir_6) <+ V(Source);
293   V(Source_vir_7) <+ V(Source);
294   V(Source_vir_8) <+ V(Source);
295   V(Source_vir_9) <+ V(Source);
296
297   V(Sub_vir_0) <+ V(Sub);
298   V(Sub_vir_1) <+ V(Sub);
299   V(Sub_vir_2) <+ V(Sub);
300   V(Sub_vir_3) <+ V(Sub);
301   V(Sub_vir_4) <+ V(Sub);
302   V(Sub_vir_5) <+ V(Sub);
303   V(Sub_vir_6) <+ V(Sub);
304   V(Sub_vir_7) <+ V(Sub);
305   V(Sub_vir_8) <+ V(Sub);
306   V(Sub_vir_9) <+ V(Sub);
307
308 end
309
310 endmodule
```

parameters.vams

```
1  // ---- Temperature
2  `define TEMP 27.0   // Temperature of operation
3
4  // ---- Natural constants ----
5  `define q 1.60e-19  // Electronic charge
6  `define k 8.617e-5  // Boltzmann constant devided by q
7
8  // ---- Model parameters ----
9  `define rho_g 20e-8 // Specific resistance of tungsten gate
10 `define tg 64e-9      // Gate heigth
```

B.3 CNFET model - Level 3

veriloga.va

```
1  `include "disciplines.vams"
2
3  module NCNFET_L3 (Drain, Gate, Source, Sub);
4
5  /*************************************************************
6  ********************* Electrical nodes ***********************
7  *************************************************************/
8
9  inout Drain, Gate, Source, Sub;
10 electrical Drain, Gate, Source, Sub;
11
12 electrical Drain_int_0, Drain_int_1, Drain_int_2, Drain_int_3,
       Drain_int_4, Drain_int_5, Drain_int_6, Drain_int_7, Drain_int_8,
       Drain_int_9;
13 electrical Gate_int_0, Gate_int_1, Gate_int_2, Gate_int_3, Gate_int_4,
       Gate_int_5, Gate_int_6, Gate_int_7, Gate_int_8, Gate_int_9;
14 electrical Source_int_0, Source_int_1, Source_int_2, Source_int_3,
       Source_int_4, Source_int_5, Source_int_6, Source_int_7, Source_int_8,
       Source_int_9;
15 electrical Sub_int_0, Sub_int_1, Sub_int_2, Sub_int_3, Sub_int_4,
       Sub_int_5, Sub_int_6, Sub_int_7, Sub_int_8, Sub_int_9;
16
17 electrical Drain_vir_0, Drain_vir_1, Drain_vir_2, Drain_vir_3,
       Drain_vir_4, Drain_vir_5, Drain_vir_6, Drain_vir_7, Drain_vir_8,
       Drain_vir_9;
18 electrical Gate_vir_0, Gate_vir_1, Gate_vir_2, Gate_vir_3, Gate_vir_4,
       Gate_vir_5, Gate_vir_6, Gate_vir_7, Gate_vir_8, Gate_vir_9;
19 electrical Source_vir_0, Source_vir_1, Source_vir_2, Source_vir_3,
       Source_vir_4, Source_vir_5, Source_vir_6, Source_vir_7, Source_vir_8,
       Source_vir_9;
20 electrical Sub_vir_0, Sub_vir_1, Sub_vir_2, Sub_vir_3, Sub_vir_4,
       Sub_vir_5, Sub_vir_6, Sub_vir_7, Sub_vir_8, Sub_vir_9;
21
22
23 /*************************************************************
24 ********************* Input parameters ***********************
25 *************************************************************/
26
27 parameter real Lg=32.0e-9;          // CNFET channel/gate length
28 parameter real pitch=10.0e-9;       // Tube pitch
29 parameter real Kgate=16.0;          // High-k gate dielectric constant
30 parameter real Tox=4.0e-9;          // Gate oxide thickness
31 parameter integer dist_type = 0;    // Diameter distribution: Gaussian =
       0, shifted log-normal = 1
32 parameter real dia_mean = 1.5e-9;   // Tube diameter
33 parameter real dia_stddev = 0.0e-9; // ...and its standard deviation
34 parameter real Efi_mean = 0.66;     // The n+ doped CNT fermi level (eV),
       0.66eV for 1% doping level, 0.6eV for 0.8% doping level
35 parameter real Efi_stddev = 0.00;   // ...and its standard deviation
36 parameter real psemi = 1.0;         // Probability of growth of sCNT
37 parameter real premsemi = 0.0;      // Probability of removal of sCNT
38 parameter real premmet = 0.0;       // Probability of removal of mCNT
39 parameter integer numtubes = 1 from [1:10];  // Number of tubes
40 parameter integer numfingers = 1 from [1:10]; // Number of gate fingers
41 parameter integer num_tran = 0;     // Transistor pos., for variab. model
42 parameter real alpha_h=1.0e-4;      // Hooge's Flicker noise constant
43
44
45 /*************************************************************
46 ********** Instantiate Level 2 models (gate fingers) *************
47 *************************************************************/
48
```

```
49 NCNFET_L2 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       numtubes(numtubes),.pos_finger(0.0),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET00 (Drain_int_0, Gate_int_0,
       Source_int_0, Sub_int_0);
50 NCNFET_L2 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       numtubes(numtubes),.pos_finger(1.0),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET01 (Drain_int_1, Gate_int_1,
       Source_int_1, Sub_int_1);
51 NCNFET_L2 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       numtubes(numtubes),.pos_finger(2.0),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET02 (Drain_int_2, Gate_int_2,
       Source_int_2, Sub_int_2);
52 NCNFET_L2 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       numtubes(numtubes),.pos_finger(3.0),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET03 (Drain_int_3, Gate_int_3,
       Source_int_3, Sub_int_3);
53 NCNFET_L2 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       numtubes(numtubes),.pos_finger(4.0),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET04 (Drain_int_4, Gate_int_4,
       Source_int_4, Sub_int_4);
54 NCNFET_L2 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       numtubes(numtubes),.pos_finger(5.0),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET05 (Drain_int_5, Gate_int_5,
       Source_int_5, Sub_int_5);
55 NCNFET_L2 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       numtubes(numtubes),.pos_finger(6.0),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET06 (Drain_int_6, Gate_int_6,
       Source_int_6, Sub_int_6);
56 NCNFET_L2 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       numtubes(numtubes),.pos_finger(7.0),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET07 (Drain_int_7, Gate_int_7,
       Source_int_7, Sub_int_7);
57 NCNFET_L2 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       numtubes(numtubes),.pos_finger(8.0),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET08 (Drain_int_8, Gate_int_8,
       Source_int_8, Sub_int_8);
58 NCNFET_L2 #(.Lg(Lg),.pitch(pitch),.Kgate(Kgate),.Tox(Tox),.dia_mean(
       dia_mean),.dia_stddev(dia_stddev),.Efi_mean(Efi_mean),.Efi_stddev(
       Efi_stddev),.psemi(psemi),.premsemi(premsemi),.premmet(premmet),.
       numtubes(numtubes),.pos_finger(9.0),.num_tran(num_tran),.dist_type(
       dist_type),.alpha_h(alpha_h)) FET09 (Drain_int_9, Gate_int_9,
       Source_int_9, Sub_int_9);
59
60
61 /*****************************************************************
62 ********************** L3 implementation **********************
63 *****************************************************************/
64
65 analog begin : model_L3
66
67   real R0, R1, R2, R3, R4, R5, R6, R7, R8, R9;
68   real R0vir, R1vir, R2vir, R3vir, R4vir, R5vir, R6vir, R7vir, R8vir,
       R9vir;
```

```
69
70
71  //************* Evaluate shunt resistance values ***************
72
73  begin : connectors
74
75    if (numfingers >= 1) begin
76      R0 = 0.00e-6;
77      R0vir = 1.0e12;
78    end else begin
79      R0 = 1.0e12;
80      R0vir = 0.00e-6;
81    end
82    if (numfingers >= 2) begin
83      R1 = 0.00e-6;
84      R1vir = 1.0e12;
85    end else begin
86      R1 = 1.0e12;
87      R1vir = 0.00e-6;
88    end
89    if (numfingers >= 3) begin
90      R2 = 0.00e-6;
91      R2vir = 1.0e12;
92    end else begin
93      R2 = 1.0e12;
94      R2vir = 0.00e-6;
95    end
96    if (numfingers >= 4) begin
97      R3 = 0.00e-6;
98      R3vir = 1.0e12;
99    end else begin
100     R3 = 1.0e12;
101     R3vir = 0.00e-6;
102   end
103   if (numfingers >= 5) begin
104     R4 = 0.00e-6;
105     R4vir = 1.0e12;
106   end else begin
107     R4 = 1.0e12;
108     R4vir = 0.00e-6;
109   end
110   if (numfingers >= 6) begin
111     R5 = 0.00e-6;
112     R5vir = 1.0e12;
113   end else begin
114     R5 = 1.0e12;
115     R5vir = 0.00e-6;
116   end
117   if (numfingers >= 7) begin
118     R6 = 0.00e-6;
119     R6vir = 1.0e12;
120   end else begin
121     R6 = 1.0e12;
122     R6vir = 0.00e-6;
123   end
124   if (numfingers >= 8) begin
125     R7 = 0.00e-6;
126     R7vir = 1.0e12;
127   end else begin
128     R7 = 1.0e12;
129     R7vir = 0.00e-6;
130   end
131   if (numfingers >= 9) begin
132     R8 = 0.00e-6;
133     R8vir = 1.0e12;
134   end else begin
135     R8 = 1.0e12;
136     R8vir = 0.00e-6;
137   end
138   if (numfingers >= 10) begin
139     R9 = 0.00e-6;
```

```
140       R9vir = 1.0e12;
141     end else begin
142       R9 = 1.0e12;
143       R9vir = 0.00e-6;
144     end
145
146   end
147
148
149   /*************************************************************
150   ********************** Place components **********************
151   *************************************************************/
152
153   //**** Connection of Level 2 devices to ext. Level 3 nodes *****
154
155   V(Drain_int_0,Drain) <+ R0*I(Drain_int_0,Drain);
156   V(Drain_int_1,Drain) <+ R1*I(Drain_int_1,Drain);
157   V(Drain_int_2,Drain) <+ R2*I(Drain_int_2,Drain);
158   V(Drain_int_3,Drain) <+ R3*I(Drain_int_3,Drain);
159   V(Drain_int_4,Drain) <+ R4*I(Drain_int_4,Drain);
160   V(Drain_int_5,Drain) <+ R5*I(Drain_int_5,Drain);
161   V(Drain_int_6,Drain) <+ R6*I(Drain_int_6,Drain);
162   V(Drain_int_7,Drain) <+ R7*I(Drain_int_7,Drain);
163   V(Drain_int_8,Drain) <+ R8*I(Drain_int_8,Drain);
164   V(Drain_int_9,Drain) <+ R9*I(Drain_int_9,Drain);
165
166   V(Gate_int_0,Gate) <+ R0*I(Gate_int_0,Gate);
167   V(Gate_int_1,Gate) <+ R1*I(Gate_int_1,Gate);
168   V(Gate_int_2,Gate) <+ R2*I(Gate_int_2,Gate);
169   V(Gate_int_3,Gate) <+ R3*I(Gate_int_3,Gate);
170   V(Gate_int_4,Gate) <+ R4*I(Gate_int_4,Gate);
171   V(Gate_int_5,Gate) <+ R5*I(Gate_int_5,Gate);
172   V(Gate_int_6,Gate) <+ R6*I(Gate_int_6,Gate);
173   V(Gate_int_7,Gate) <+ R7*I(Gate_int_7,Gate);
174   V(Gate_int_8,Gate) <+ R8*I(Gate_int_8,Gate);
175   V(Gate_int_9,Gate) <+ R9*I(Gate_int_9,Gate);
176
177   V(Source_int_0,Source) <+ R0*I(Source_int_0,Source);
178   V(Source_int_1,Source) <+ R1*I(Source_int_1,Source);
179   V(Source_int_2,Source) <+ R2*I(Source_int_2,Source);
180   V(Source_int_3,Source) <+ R3*I(Source_int_3,Source);
181   V(Source_int_4,Source) <+ R4*I(Source_int_4,Source);
182   V(Source_int_5,Source) <+ R5*I(Source_int_5,Source);
183   V(Source_int_6,Source) <+ R6*I(Source_int_6,Source);
184   V(Source_int_7,Source) <+ R7*I(Source_int_7,Source);
185   V(Source_int_8,Source) <+ R8*I(Source_int_8,Source);
186   V(Source_int_9,Source) <+ R9*I(Source_int_9,Source);
187
188   V(Sub_int_0,Sub) <+ R0*I(Sub_int_0,Sub);
189   V(Sub_int_1,Sub) <+ R1*I(Sub_int_1,Sub);
190   V(Sub_int_2,Sub) <+ R2*I(Sub_int_2,Sub);
191   V(Sub_int_3,Sub) <+ R3*I(Sub_int_3,Sub);
192   V(Sub_int_4,Sub) <+ R4*I(Sub_int_4,Sub);
193   V(Sub_int_5,Sub) <+ R5*I(Sub_int_5,Sub);
194   V(Sub_int_6,Sub) <+ R6*I(Sub_int_6,Sub);
195   V(Sub_int_7,Sub) <+ R7*I(Sub_int_7,Sub);
196   V(Sub_int_8,Sub) <+ R8*I(Sub_int_8,Sub);
197   V(Sub_int_9,Sub) <+ R9*I(Sub_int_9,Sub);
198
199
200   //********* Connection of Level 2 devices to dummy nodes *******
201
202   V(Drain_int_0,Drain_vir_0) <+ R0vir*I(Drain_int_0,Drain_vir_0);
203   V(Drain_int_1,Drain_vir_1) <+ R1vir*I(Drain_int_1,Drain_vir_1);
204   V(Drain_int_2,Drain_vir_2) <+ R2vir*I(Drain_int_2,Drain_vir_2);
205   V(Drain_int_3,Drain_vir_3) <+ R3vir*I(Drain_int_3,Drain_vir_3);
206   V(Drain_int_4,Drain_vir_4) <+ R4vir*I(Drain_int_4,Drain_vir_4);
207   V(Drain_int_5,Drain_vir_5) <+ R5vir*I(Drain_int_5,Drain_vir_5);
208   V(Drain_int_6,Drain_vir_6) <+ R6vir*I(Drain_int_6,Drain_vir_6);
209   V(Drain_int_7,Drain_vir_7) <+ R7vir*I(Drain_int_7,Drain_vir_7);
210   V(Drain_int_8,Drain_vir_8) <+ R8vir*I(Drain_int_8,Drain_vir_8);
```

```
211   V(Drain_int_9,Drain_vir_9) <+ R9vir*I(Drain_int_9,Drain_vir_9);
212
213   V(Gate_int_0,Gate_vir_0) <+ R0vir*I(Gate_int_0,Gate_vir_0);
214   V(Gate_int_1,Gate_vir_1) <+ R1vir*I(Gate_int_1,Gate_vir_1);
215   V(Gate_int_2,Gate_vir_2) <+ R2vir*I(Gate_int_2,Gate_vir_2);
216   V(Gate_int_3,Gate_vir_3) <+ R3vir*I(Gate_int_3,Gate_vir_3);
217   V(Gate_int_4,Gate_vir_4) <+ R4vir*I(Gate_int_4,Gate_vir_4);
218   V(Gate_int_5,Gate_vir_5) <+ R5vir*I(Gate_int_5,Gate_vir_5);
219   V(Gate_int_6,Gate_vir_6) <+ R6vir*I(Gate_int_6,Gate_vir_6);
220   V(Gate_int_7,Gate_vir_7) <+ R7vir*I(Gate_int_7,Gate_vir_7);
221   V(Gate_int_8,Gate_vir_8) <+ R8vir*I(Gate_int_8,Gate_vir_8);
222   V(Gate_int_9,Gate_vir_9) <+ R9vir*I(Gate_int_9,Gate_vir_9);
223
224   V(Source_int_0,Source_vir_0) <+ R0vir*I(Source_int_0,Source_vir_0);
225   V(Source_int_1,Source_vir_1) <+ R1vir*I(Source_int_1,Source_vir_1);
226   V(Source_int_2,Source_vir_2) <+ R2vir*I(Source_int_2,Source_vir_2);
227   V(Source_int_3,Source_vir_3) <+ R3vir*I(Source_int_3,Source_vir_3);
228   V(Source_int_4,Source_vir_4) <+ R4vir*I(Source_int_4,Source_vir_4);
229   V(Source_int_5,Source_vir_5) <+ R5vir*I(Source_int_5,Source_vir_5);
230   V(Source_int_6,Source_vir_6) <+ R6vir*I(Source_int_6,Source_vir_6);
231   V(Source_int_7,Source_vir_7) <+ R7vir*I(Source_int_7,Source_vir_7);
232   V(Source_int_8,Source_vir_8) <+ R8vir*I(Source_int_8,Source_vir_8);
233   V(Source_int_9,Source_vir_9) <+ R9vir*I(Source_int_9,Source_vir_9);
234
235   V(Sub_int_0,Sub_vir_0) <+ R0vir*I(Sub_int_0,Sub_vir_0);
236   V(Sub_int_1,Sub_vir_1) <+ R1vir*I(Sub_int_1,Sub_vir_1);
237   V(Sub_int_2,Sub_vir_2) <+ R2vir*I(Sub_int_2,Sub_vir_2);
238   V(Sub_int_3,Sub_vir_3) <+ R3vir*I(Sub_int_3,Sub_vir_3);
239   V(Sub_int_4,Sub_vir_4) <+ R4vir*I(Sub_int_4,Sub_vir_4);
240   V(Sub_int_5,Sub_vir_5) <+ R5vir*I(Sub_int_5,Sub_vir_5);
241   V(Sub_int_6,Sub_vir_6) <+ R6vir*I(Sub_int_6,Sub_vir_6);
242   V(Sub_int_7,Sub_vir_7) <+ R7vir*I(Sub_int_7,Sub_vir_7);
243   V(Sub_int_8,Sub_vir_8) <+ R8vir*I(Sub_int_8,Sub_vir_8);
244   V(Sub_int_9,Sub_vir_9) <+ R9vir*I(Sub_int_9,Sub_vir_9);
245
246
247   //**************** VCV-Sources for dummy nodes *****************
248
249   V(Drain_vir_0) <+ V(Drain);
250   V(Drain_vir_1) <+ V(Drain);
251   V(Drain_vir_2) <+ V(Drain);
252   V(Drain_vir_3) <+ V(Drain);
253   V(Drain_vir_4) <+ V(Drain);
254   V(Drain_vir_5) <+ V(Drain);
255   V(Drain_vir_6) <+ V(Drain);
256   V(Drain_vir_7) <+ V(Drain);
257   V(Drain_vir_8) <+ V(Drain);
258   V(Drain_vir_9) <+ V(Drain);
259
260   V(Gate_vir_0) <+ V(Gate);
261   V(Gate_vir_1) <+ V(Gate);
262   V(Gate_vir_2) <+ V(Gate);
263   V(Gate_vir_3) <+ V(Gate);
264   V(Gate_vir_4) <+ V(Gate);
265   V(Gate_vir_5) <+ V(Gate);
266   V(Gate_vir_6) <+ V(Gate);
267   V(Gate_vir_7) <+ V(Gate);
268   V(Gate_vir_8) <+ V(Gate);
269   V(Gate_vir_9) <+ V(Gate);
270
271   V(Source_vir_0) <+ V(Source);
272   V(Source_vir_1) <+ V(Source);
273   V(Source_vir_2) <+ V(Source);
274   V(Source_vir_3) <+ V(Source);
275   V(Source_vir_4) <+ V(Source);
276   V(Source_vir_5) <+ V(Source);
277   V(Source_vir_6) <+ V(Source);
278   V(Source_vir_7) <+ V(Source);
279   V(Source_vir_8) <+ V(Source);
280   V(Source_vir_9) <+ V(Source);
281
```

```
282   V(Sub_vir_0) <+ V(Sub);
283   V(Sub_vir_1) <+ V(Sub);
284   V(Sub_vir_2) <+ V(Sub);
285   V(Sub_vir_3) <+ V(Sub);
286   V(Sub_vir_4) <+ V(Sub);
287   V(Sub_vir_5) <+ V(Sub);
288   V(Sub_vir_6) <+ V(Sub);
289   V(Sub_vir_7) <+ V(Sub);
290   V(Sub_vir_8) <+ V(Sub);
291   V(Sub_vir_9) <+ V(Sub);
292
293 end
294
295 endmodule
```

Appendix C

Verilog-A implementation of the accurate GFET compact model

veriloga.va

```
1  `include "disciplines.vams"
2  `include "phys_constants.vams"
3
4  module GFET(Drain, Gate, Source, BackGate);
5
6  /*****************************************
7    Input parameters and global variables
8  *****************************************/
9
10   // Input parameters
11   parameter real Lg = 5.0e-6;          // Gate length (m)
12   parameter real Wg = 1.0e-6;          // Gate width (m)
13   parameter real tox_top = 15.0e-9;    // Top-oxide thickness (m)
14   parameter real tox_back = 300.0e-9; // Back-oxide thickness (m)
15   parameter real kappa_top = 8.9;      // Rel. permittivity top-oxide (1)
16   parameter real kappa_back = 3.9;     // Rel. permittivity back-oxide (1)
17   parameter real Vgso = 1.24;          // Flatband voltage top-gate (V)
18   parameter real Vbso = 11.0;          // Flatband voltage back-gate (V)
19   parameter real Rd = 170e-6;          // Drain resistance (Ohm m)
20   parameter real Rs = 170e-6;          // Source resistance (Ohm m)
21   parameter real mucm2Vs = 1150.0;     // Low-field mobility (cm2/Vs)
22   parameter real Delta = 0.1;          // Potential inhomogeneity (eV)
23   parameter real hbarOmega = 0.075;    // Phonon energy hbar*omega (eV)
24
25   // Electrical connections
26   inout Drain, Gate, Source, BackGate;
27   electrical Drain, DrainInt, Gate, Source, SourceInt, BackGate,
       VDrainInt, VGate, VSourceInt, VBackGate, nodeVcd, nodeVcs;
28
29   // Global variables
30   real mu;
31   real Vd, Vs, Vg, Vb;
32   real Vcd, Vcs;
33   real LHSs, RHSs, LHSd, RHSd;
34   real Ids;
35   real Ct, Cb;
36   real Leff;
37   real Qnetd, Qnets;
38
```

```
39
40 /*****************************************
41   Auxiliary functions
42 *****************************************/
43
44   // Signum function
45   analog function real sgn;
46   input x;
47   real x;
48
49   begin
50     if (x>0.0)
51     begin
52       sgn=1.0;
53     end
54     else if (x<0.0)
55     begin
56       sgn=-1.0;
57     end
58     else
59     begin
60       sgn=0.0;
61     end
62     end
63
64   endfunction // Signum function
65
66   // Approximation of the Fermi-Dirac integral of first order
67   // Based on Halen and Pulfrey:
68   // J. Appl. Phys. 57 (12) (1985) 5271-5274
69   // J. Appl. Phys. 59 (6)  (1986) 2264
70   analog function real FDint;
71     input eta;
72
73     real eta;
74     real a1, a2, a3, a4, a5, a6, a7, b1, b2;
75
76     begin
77       a1 = 1.000000;
78       a2 = 0.250052;
79       a3 = 0.111747;
80       a4 = 0.064557;
81       a5 = 0.040754;
82       a6 = 0.020532;
83       a7 = 0.005108;
84
85       b1 = 1.644934066848226;
86       b2 = 0.500000000000000;
87
88       if (eta<=0)
89         FDint = a1*exp(1.0*eta)-a2*exp(2.0*eta)+a3*exp(3.0*eta)-a4*exp
     (4.0*eta)+a5*exp(5.0*eta)-a6*exp(6.0*eta)+a7*exp(7.0*eta);
90       else
91         FDint = -a1*exp(-1.0*eta)+a2*exp(-2.0*eta)-a3*exp(-3.0*eta)+a4*
     exp(-4.0*eta)-a5*exp(-5.0*eta)+a6*exp(-6.0*eta)-a7*exp(-7.0*eta)+b2*
     pow(eta,2.0)+b1;
92
93     end
94
95   endfunction // Fermi-Dirac Integral
96
97
98 /*****************************************
99   Velocity saturation antiderivatives
100 *****************************************/
101
102   analog function real intA; // constant saturation velocity
103     input Q, Ct, Cb, omega;
104     real Q, Ct, Cb, omega;
105     real a,b,c,d;
106
```

```
107     begin
108       a = 2.0/(Ct+Cb)*pow(`q,3.0)/(`pi*pow(`hbar*`vf,2.0));
109       b = `pi*pow(`hbar*`vf,2.0)/pow(`q,3.0);
110       c = `pi*pow(`hbar*`vf,2.0)/(4.0*pow(`q,3.0));
111       d = `pi/(2.0*`vf);
112
113       intA = sgn(Q)*(2.0+a*sqrt(b*sgn(Q)*Q))*sqrt(c)*d*sqrt(sgn(Q)*Q);
114     end
115
116   endfunction // intA
117
118   analog function real intB; // inversely proportional saturation
        velocity
119     input Q, Ct, Cb, omega;
120     real Q, Ct, Cb, omega;
121     real a,b,c,e,f,g;
122
123     begin
124       a = 2.0/(Ct+Cb)*pow(`q,3.0)/(`pi*pow(`hbar*`vf,2.0));
125       b = `pi*pow(`hbar*`vf,2.0)/pow(`q,3.0);
126       c = `pi*pow(`hbar*`vf,2.0)/(4.0*pow(`q,3.0));
127       e = pow(`pi,2.0)*`hbar*`vf/(2.0*`q*omega);
128       f = `pi*pow(`hbar*`vf,2.0)/`q;
129       g = pow(`hbar*omega/2.0,2.0);
130
131       intB = sqrt(c)*e/(6.0*sqrt(b)*pow(f,2.0))*(2.0*sqrt(f*sgn(Q)*Q-g)
      *(2.0*a*b*f*Q+sgn(Q)*3.0*f*sqrt(b*sgn(Q)*Q)+sgn(Q)*4.0*a*b*g)+3.0*sqrt
      (b*f)*g*ln(2.0*b*sqrt(f*sgn(Q)*Q)*sqrt(f*sgn(Q)*Q-g)+2.0*b*f*Q-sgn(Q)*
      b*g));
132
133     end
134
135   endfunction // intB
136
137
138 /*****************************************
139   Main code
140 *****************************************/
141
142   analog begin
143
144     // Normalize mobility parameter
145     mu = mucm2Vs/1.0e4; // (m^2/Vs)
146
147     // Normalized top- and back-gate capacitance
148     Ct = `epso*kappa_top/tox_top; //   (F/m^2)
149     Cb = `epso*kappa_back/tox_back; // (F/m^2)
150
151     begin // Bias conditions
152       Vd = V(VDrainInt);
153       Vs = V(VSourceInt);
154       Vg = V(VGate);
155       Vb = V(VBackGate);
156
157       Vcd = V(nodeVcd);
158       Vcs = V(nodeVcs);
159     end // Bias conditions
160
161     // Evaluate LHS of gate electrostatics equation
162     begin : eval_LHS
163
164       real VVcs, VVcd;
165
166       VVcd = Vcd;
167       VVcs = Vcs;
168
169       Qnetd = `q*2.0/`pi*pow(`kT/(`vf*`hbar),2.0)*(FDint(VVcd*`qkT)-FDint
      (-VVcd*`qkT));
170       Qnets = `q*2.0/`pi*pow(`kT/(`vf*`hbar),2.0)*(FDint(VVcs*`qkT)-FDint
      (-VVcs*`qkT));
171
```

```
172       LHSd = VVcd*(Ct+Cb)+Qnetd;
173       LHSs = VVcs*(Ct+Cb)+Qnets;
174
175     end // eval_LHS
176
177     // Evaluate RHS of gate electrostatics equation
178     begin : eval_RHS
179
180       real VVd, VVs, VVg, VVb, VVcs, VVcd;
181
182       VVd = Vd;
183       VVg = Vg;
184       VVb = Vb;
185       VVs = Vs;
186
187       VVcd = Vcd;
188       VVcs = Vcs;
189
190       RHSd = -(VVg-Vgso-VVd)*Ct - (VVb-Vbso-VVd)*Cb;
191       RHSs = -(VVg-Vgso-VVs)*Ct - (VVb-Vbso-VVs)*Cb;
192     end // eval_RHS
193
194     // Effective channel length due to velocity saturation
195     begin : eval_effective_length
196       real omega, rhocrit;
197       real integ;
198       real Qs, Qd, QnetsV, QnetdV;
199       real VCd, VCs, Vchs, Vchd, k;
200       real VVd, VVs, VVg, VVb;
201
202       VVd = Vd;
203       VVg = Vg;
204       VVb = Vb;
205       VVs = Vs;
206
207       omega = hbarOmega*`q/`hbar;
208       rhocrit = 1.0/(2.0*`pi)*pow(omega/`vf,2.0);
209
210       k = (2.0*pow(`q,2)/`pi) * (`q/pow(`hbar*`vf,2));
211       VCd = (VVg-Vgso-VVd)*Ct + (VVb-Vbso-VVd)*Cb;
212       VCs = (VVg-Vgso-VVs)*Ct + (VVb-Vbso-VVs)*Cb;
213       Vchd = sgn(VCd)*(-(Ct+Cb)+sqrt(pow(Ct+Cb,2)+sgn(VCd)*2.0*k*VCd))/k;
214       Vchs = sgn(VCs)*(-(Ct+Cb)+sqrt(pow(Ct+Cb,2)+sgn(VCs)*2.0*k*VCs))/k;
215
216       QnetdV = -pow(`q,3.0)/(`pi*pow(`hbar*`vf,2.0))*pow(Vchd,2.0)*sgn(
    Vchd);
217       QnetsV = -pow(`q,3.0)/(`pi*pow(`hbar*`vf,2.0))*pow(Vchs,2.0)*sgn(
    Vchs);
218
219       if (QnetsV<= QnetdV)
220       begin
221         Qs = QnetsV;
222         Qd = QnetdV;
223       end
224       else
225       begin
226         Qs = QnetdV;
227         Qd = QnetsV;
228       end
229
230       if (Qs<=-rhocrit*`q)
231       begin
232         if (Qd<=-rhocrit*`q)
233         begin
234           integ = intB(Qd,Ct,Cb,omega)-intB(Qs,Ct,Cb,omega);
235         end
236         else if (Qd <= rhocrit*`q)
237         begin
238           integ = intA(Qd,Ct,Cb,omega)-intA(-rhocrit*`q,Ct,Cb,omega)+intB
    (-rhocrit*`q,Ct,Cb,omega)-intB(Qs,Ct,Cb,omega);
239         end
```

```
240         else //(Qd > rhocrit*`q)
241         begin
242           integ = intB(Qd,Ct,Cb,omega)-intB(rhocrit*`q,Ct,Cb,omega)+intA(
        rhocrit*`q,Ct,Cb,omega)-intA(-rhocrit*`q,Ct,Cb,omega)+intB(-rhocrit*`q
        ,Ct,Cb,omega)-intB(Qs,Ct,Cb,omega);
243         end
244       end
245       else if (Qs <= rhocrit*`q)
246       begin
247         if (Qd <= rhocrit*`q)
248         begin
249           integ = intA(Qd,Ct,Cb,omega)-intA(Qs,Ct,Cb,omega);
250         end
251         else //(Qd > rhocrit*`q)
252         begin
253           integ = intB(Qd,Ct,Cb,omega)-intB(rhocrit*`q,Ct,Cb,omega)+intA(
        rhocrit*`q,Ct,Cb,omega)-intA(Qs,Ct,Cb,omega);
254         end
255       end
256       else //(Qs > rhocrit*`q)
257       begin //(Qd > rhocrit*`q)
258         integ = intB(Qd,Ct,Cb,omega)-intB(Qs,Ct,Cb,omega);
259       end
260
261       Leff = Lg+mu*abs(integ);
262
263     end // eval_effective_length
264
265     // Evaluate overall Drain current equation
266     begin : eval_Drain_current
267
268       real VVcd, VVcs;
269       real Intd, Ints;
270       real ca, cb, cc, n0;
271       real Npuddle;
272       real VVds;
273
274       VVds = Vd-Vs;
275
276       VVcd = Vcd;
277       VVcs = Vcs;
278
279       ca = pow(`q,3.0)/(`pi*pow(`hbar*`vf,2.0));
280       cb = 1.0/(Ct+Cb)*2.0*pow(`q,5.0)*`kT*ln(4)/(pow(`pi,2.0)*pow(`hbar*
        `vf,4.0));
281       cc = `qkT/ln(4);
282       n0 = `pi*pow(`kT,2.0)/(3.0*pow(`hbar*`vf,2.0));
283
284       Intd = ca*pow(VVcd,3.0)/3.0-cb/(8.0*pow(cc,3.0))*asinh(cc*VVcd)+
        sqrt(1.0+pow(cc*VVcd,2.0))*(cb*VVcd/(8.0*pow(cc,2.0))+cb*pow(VVcd,3.0)
        /4.0);
285       Ints = ca*pow(VVcs,3.0)/3.0-cb/(8.0*pow(cc,3.0))*asinh(cc*VVcs)+
        sqrt(1.0+pow(cc*VVcs,2.0))*(cb*VVcs/(8.0*pow(cc,2.0))+cb*pow(VVcs,3.0)
        /4.0);
286
287       Npuddle = pow(Delta*`q,2.0)/(`pi*pow(`vf*`hbar,2.0));
288
289       Ids = mu*Wg*((Intd-Ints) + `q*(Npuddle+n0)*VVds)/Leff;
290
291     end // eval_Drain_current
292
293     // Place components
294
295     // Construct to obtain Vcd, Vcs
296     I(VDrainInt,nodeVcd)   <+ LHSd;
297     I(nodeVcd,VSourceInt)  <+ RHSd;
298     I(VDrainInt,nodeVcs)   <+ LHSs;
299     I(nodeVcs,VSourceInt)  <+ RHSs;
300     V(VDrainInt)           <+ 1.0*V(DrainInt);
301     V(VSourceInt)          <+ 1.0*V(SourceInt);
302     V(VGate)               <+ 1.0*V(Gate);
```

```
303     V(VBackGate)           <+ 1.0*V(BackGate);
304
305     // Drain current
306     I(DrainInt,SourceInt) <+ Ids;
307
308     // Parasitic resistances
309     V(Drain,DrainInt)      <+ Rs/Wg*I(Drain,DrainInt);
310     V(SourceInt,Source)    <+ Rd/Wg*I(SourceInt,Source);
311
312   end // Analog begin
313
314 endmodule
```

phys_constants.vams

```
1  /*****************************************
2    Physical constants
3  *****************************************/
4
5  `define q 1.60218e-19       // Elementary charge (C)
6  `define pi 3.1415926535898 // Pi
7  `define hbar 1.05458e-34    // Reduced Planck constant (Js)
8  `define epso 8.85418e-12    // Vacuum permittivity (F/m)
9  `define kT 4.14195e-21      // kB*T constant (J) for T = 300 K
10 `define qkT 38.68173        // q/(kB*T) constant (1/V) for T = 300 K
11
12 /*****************************************
13   More constants
14 *****************************************/
15
16 `define vf 1.0e6            // Fermi velocity of graphene (m/s)
```

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