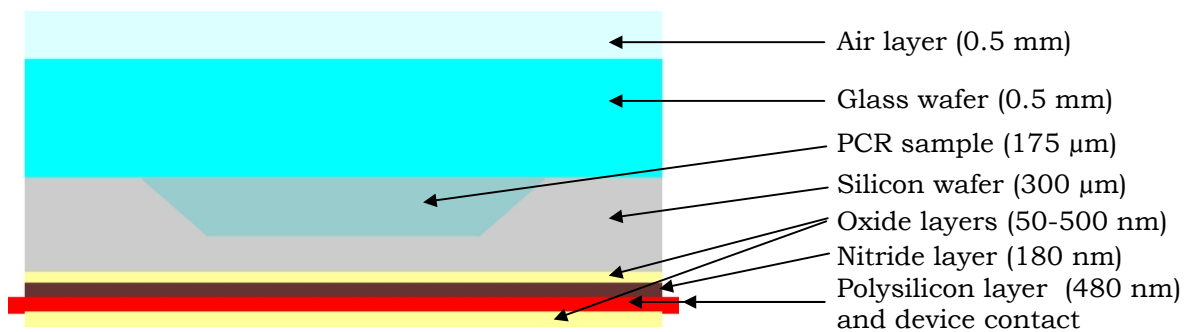## 5.3.1. SIMULATION SETUP

Simulations were carried out using DESSIS-ISE (*Integrated Systems Engineering*) software running on Unix-based SunRay (*Sun Microsystems*) workstations. The advantage of DESSIS-ISE over other, more complex simulation packages like ANSYS, is that, although it does not offer 3D simulation capabilities, it is capable of integrating the simulation of material and device physical properties with SPICE generated circuit net lists. This allows the user to create a material specified, drawn device and to simulate its effect as a device in an external circuit, which was, ultimately, the goal of the simulations required for polysilicon layer analysis as a heater element.

Air layer (0.5 mm)
Glass wafer (0.5 mm)
PCR sample (175 μm)
Silicon wafer (300 μm)
Oxide layers (50-500 nm)
Nitride layer (180 nm)
Polysilicon layer (480 nm)
and device contact

Figure 117 - Schematic cross-section (across the chip width) 2D view of the simulated device. Layer thickness is not up to scale. Simulator meshing was scaled to layer thickness to provide more accurate simulations. Thermal simulation top and bottom forced ambient nodes were situated, respectively, immediately above and below the air layer and the bottom silicon oxide layer. The simulated polysilicon layer was a 480 nm standard doped layer with $1.74 \cdot 10^{20}$ cm^{-3} boron impurities and the underlying silicon wafer was a P-type silicon wafer with its estimated standard 10^{16} cm^{-3} boron impurity level. The PCR sample was simulated as water (see *Materials and Methods*, p.314), but without acknowledging convection effects due to simulator limitations.

Hence, the basic simulation elements were a *drawn* description of the expected device (see Figure 117) and the corresponding stimulator circuit (see Figure 118). For further details on simulation parameters and flow, see *Materials and Methods*, p.314.

With these elements, 2D simulations on a transversal (width) section of the PCR chip could be simulated, using linear current densities (A/μm) and linear resistances (Ω·μm), and these results could then be extrapolated to the real 3D element by multiplying/dividing by the known resistor width.

(b)
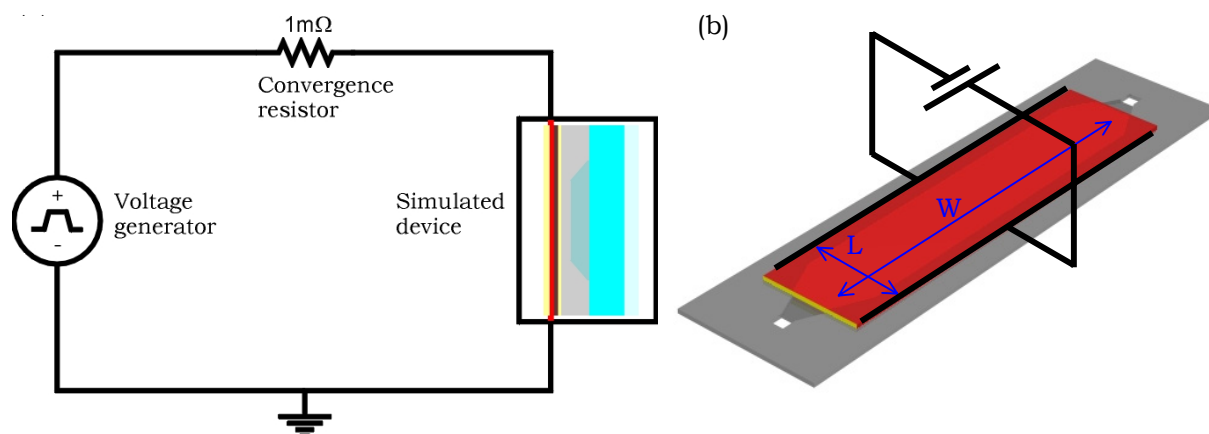
Figure 118 - Schematic diagram of the simulation circuit (a). The 1 mΩ resistor was added to avoid convergence errors in the simulation. Schematic view (b) of the 2D simulated region (yellow) in reference to the PCR-chip (gray), the extended 3D resistor (red) and the electrical connection (black).

## 5.3.2. EVALUATION OF TRANSIENT BEHAVIOR

The first objective of the simulations was to assess the maximum resistance length that would allow fast transient responses for the system. For a fixed resistance width (here assumed as the whole length of the PCR chamber, ~24 mm) the dissipated power for a certain voltage pulse can be obtained by:

$$P = \frac{V^2}{R} = \frac{V^2}{R_S x \dfrac{L}{W}}$$

Equation 6 - Dissipated power in a planar resistor. R_S is the square resistance of the material, while L and W represent the resistor length and width respectively.

Evidently, shorter resistances will allow a higher current flow and thus dissipate more power, generating higher temperatures faster. On the other hand, too long resistances will excessively impede current flow, yielding lower dissipation and, thus, lower temperatures. This fact was validated by simulating the thermal response of a set of different length resistors to a 0.85 s voltage pulse. Due to the inability of the program to simulate liquid convection effects, which produced unrealistic results in the sample (see *Materials and Methods*, p.314), the measurements here shown were taken at the silicon-sample interface. Results, shown in Figure 119, clearly

indicated that the upper limit on resistor length, if PCR-like temperatures were to be achieved in a reasonable way, lay in the 5-6 mm range.
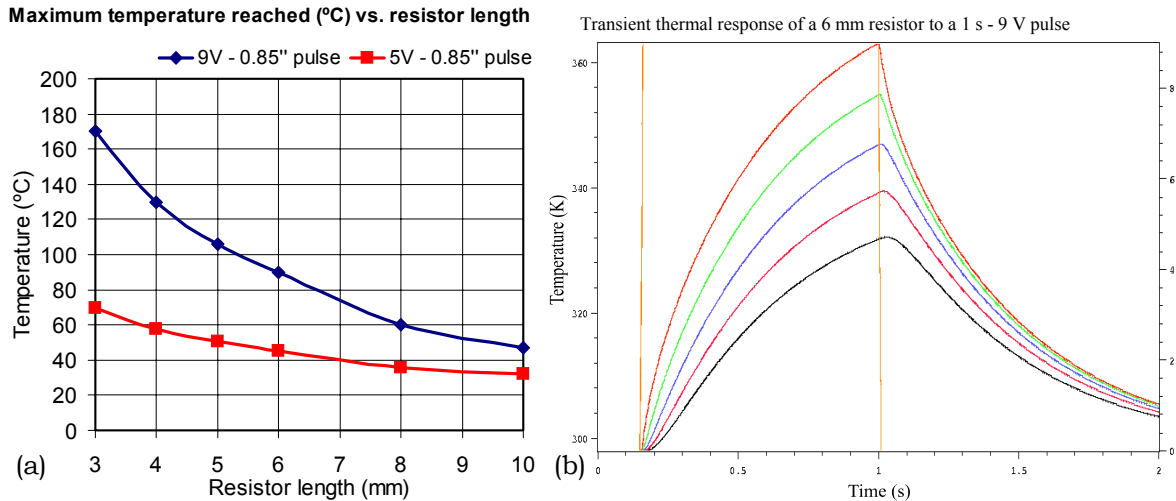
Figure 119 - (a) Maximum temperatures reached by different length resistors after a 0.85 s - 9/5 V pulse and (b) transient thermal response of a 6 mm resistor to a 1 s - 9 V pulse at different depths: orange equals zero depth (sample-silicon interface), while black represents the sample-glass interface. As mentioned above, the simulation of only conduction (and not convection) effects in the liquid sample produced unrealistic results and, thus, only zero-depth values were used to estimate the correlation in (a).

5.3.3. STUDY OF RESISTANCE CHARACTERISTICS

Using the same set of simulations, an electrical characterization of the polysilicon resistances was carried out. Firstly, their J/V curve was obtained from simulated data, as shown in Figure 120.
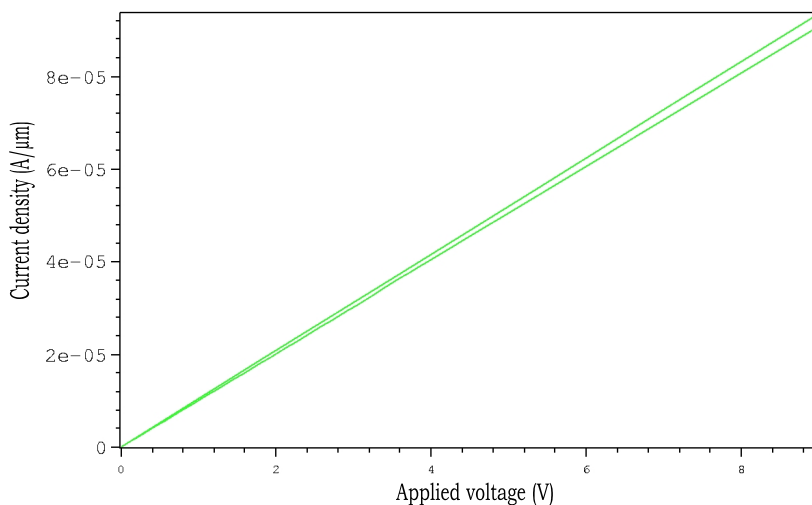
Figure 120 - J/V relation for a 6 mm resistance under a 9 V - 0.85 pulse.

The diverging J/V relations correspond to the rising and falling voltage levels, a fact that would be later taken into account when trying to use the resistor simultaneously as a heater and sensor. From this data, square resistance and current for a given square (see Table 15) could be easily deduced from Equation 7:

$$R_S = \frac{V}{J \cdot L} \qquad (\forall i\, L_i < W_i \quad \Rightarrow L = W)$$

Equation 7 - Square resistance (R_S) as a product of linear current density and square width (W). Since, for all designs $L<W$, $W=L$ can be assumed, and the current passing through the $L \cdot W$ (sc. $L \cdot L$) square will be determined by the voltage falling across L (i.e. V).

Resistance length (mm)	Current density (A/μ)		Intensity (A)		Square resistance (Ω)	
	rise	fall	rise	fall	rise	fall
3	1.86680e-4	1.78096e-4	0.5600	0.5343	16.07	16.84
4	1.40171e-4	1.34795e-4	0.5607	0.5392	16.05	16.69
5	1.12206e-4	1.08533e-4	0.5610	0.5427	16.04	16.58
6	9.3537e-5	9.0875e-5	0.5612	0.5453	16.04	16.51
8	7.0178e-5	6.8966e-5	0.5614	0.5517	16.03	16.31

Table 15 - Derived intensity and square resistance for different length resistors.

Square-resistance values agreed with current CNM-IMB process datasheets for 480 nm / $1.74 \cdot 10^{20}$ cm^{-3} boron impurities polysilicon layers. It is worth noting that square resistance did not vary greatly in rise data, but did differ substantially in fall data. This is due to the fact that on rise time, all resistors were still nearly at ambient temperature, while on fall time they had already achieved the maximum temperatures reported in Figure 119a. Therefore, combining both sets of data, the temperature coefficient of resistivity (TCR) of the resistances could be inferred, following Equation 8, and is shown in Table 16.

$$TCR = \frac{R_T - R_0}{R_0 \cdot (T - T_0)} = \frac{\Delta R}{\Delta T \cdot R_0}$$

Equation 8 - Temperature coefficient of resistivity (TCR) as a relation of the increase/decrease in measured resistance relative to the temperature differential. R_T and R_0 are the measured resistance values at temperatures T and T_0 (ambient temperature in this case, 25 °C).

Resistance length (mm)	TCR (°C^{-1})
5	0.00041781
6	0.00045066

Table 16 - Estimated TCR for the 5 and 6 mm length resistances applying Equation 8. Mean value: $4.34 \cdot 10^{-4}$ °C^{-1}.

Although smaller than that of copper (4.29·10⁻³) or platinum (3.93·10⁻³) the estimated TCR of doped polysilicon (4.34·10⁻⁴) was considered still large enough to provide sensitive thermal sensing. To obtain the estimated temperature from the measured resistance, Equation 8 can be untwined as Equation 9:

$$T = T_0 + \frac{1}{TCR}\left[\frac{R_T}{R_0} - 1\right] \quad \rightarrow \quad T = T_0 + 2304{,}14 \cdot \left[\frac{R_T}{R_0} - 1\right]$$

**Equation 9** - Temperature estimated from measured resistance using the thermal coefficient of resistivity (TCR).

5.3.4. EVALUATION OF HEAT DISTRIBUTION

A final part of the simulation analysis was centered on the distribution of heat across the chip surface and its relation to resistor length. Although, as previously explained, the non-use of liquid convection simulation at the sample yielded unrealistic results, the results on heat distribution considering the silicon-sample and sample-glass interfaces were still significant, since they provided information on the uniformity of temperature distribution over the silicon chip, an uniformity that was also to be expected (acknowledging convection factors) at the sample.

Minimal resistor length

Simulations of temperature distribution along the chip width were run for different resistor lengths. Simulation results (see Figure 121) revealed that the temperature distribution at the sample-glass interface lost homogeneity at lower resistor lengths. The results for a 6 mm resistor (black line in Figure 121) were evenly homogenous at the chamber region and only shot up at the extremes, in which silicon is in direct contact with glass. However, results for the 4 mm resistor (red line in Figure 121) revealed mounting temperature non-homogeneity in the reservoir zone (which increased further with 3 mm resistors), indicating that heat was not radiating efficiently enough across the sample. Even though such an effect could, and would undoubtedly, be alleviated by the non-simulated liquid convection effects that were to take place in the sample, it was decided, as a safety measure, to stick only to designs above the 4.5 mm range in order to avoid peak temperature non-homogeneities in the sample.
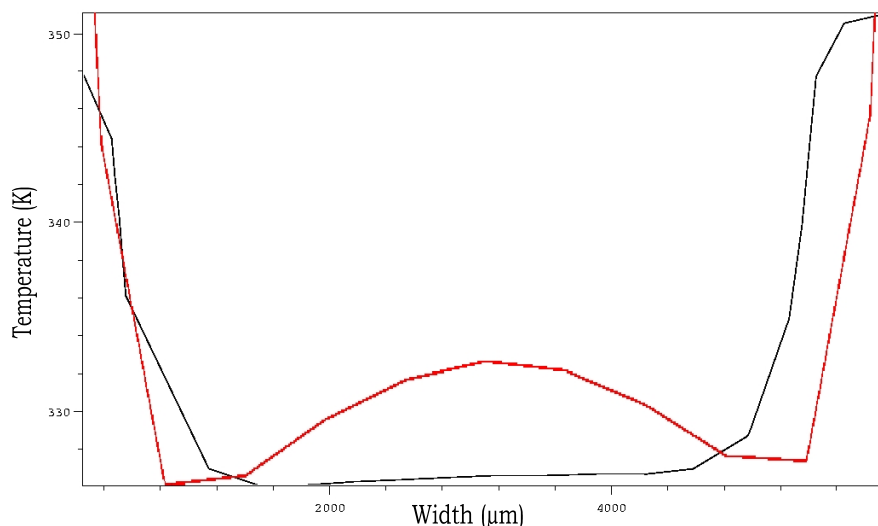
Figure 121 - Temperature distribution across the cross-section (width) of the PCR chip. The temperature was measured at the sample-glass interface, at T=1 s and for a 9 V pulse. The black line corresponds to the temperature distribution of a 6 mm resistor, while the red line corresponds to that of a 4 mm resistor.

Bi-dimensional homogeneity

Once the resistor length had been restricted to the 5-6 mm range due to transient requirements (see p.218) and temperature homogeneity ones (see above), a final bi-dimensional simulation of the temperature distribution across a full cross-section of the PCR-chip for 5 mm long resistor was conducted by linear interpolation of one-dimensional simulations.
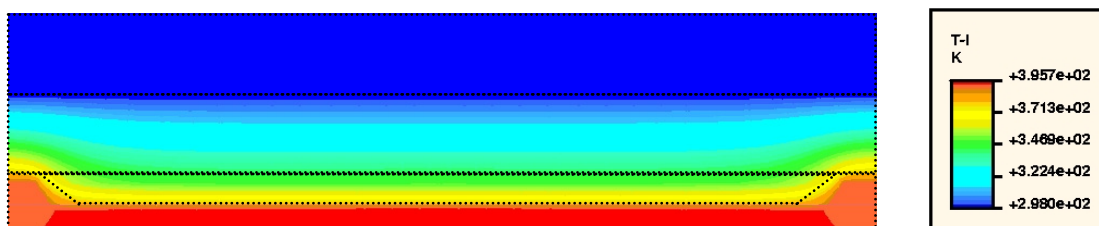
Figure 122 - Bi-dimensional plot of temperature distribution over the cross-section (width) of the PCR-chip. Data was taken from simulations for a 5 mm resistor, at T=1 s and under a 9 V pulse. The underlying device structure (see Figure 117, p.217) is illustrated by dotted lines.

Bi-dimensional simulation results confirmed the uniformity of temperature distribution using 5 mm resistors over the whole PCR-chamber. The substantial vertical thermal gradient observed in the PCR chamber, together with the slight lateral one, were supposed to be artifacts of the non-simulation of thermal liquid convection.

5.3.5. DETERMINATION OF DESIGN PARAMETERS

Continuous resistor design

After the extensive simulation work done, enough quantitative data was available to undertake the design of polysilicon resistors. But, even thought the bi-dimensional simulation had been accomplished by interpolation of adjacent linear resistances, it was clear that the same approach could not be followed in the implementation of a real resistor. That is, if the resistor were to cover the whole PCR chamber area, it ought to be a resistor over 24 mm wide, far much wider than long, since resistor length had been restricted by simulation results to below 6 mm. In such a planar resistor, many undesired effects would occur due to its awkward shape. For instance, lateral current and Joule effects would most probably induce temperature non-homogeneities on the resistor surface, and the application of abrupt current flows could even provoke electro-migration effects that would lower device efficiency and induce other aberrant phenomena.

Parallel resistor array

In view of the problems that the creation of a continuous resistor conveyed, it was decided to adopt a compromise solution by creating a parallel array of rectangular resistors. Since, therefore, the presence of a gap between each segment would be unavoidable, the global efficiency of the parallel array would be lower than that of the continuous resistor estimated in simulations. As a result, the upper limit on resistor length had to be shortened from 6 down to 5 mm in order to compensate for the loss of efficiency the inter-digitized gaps would impose.
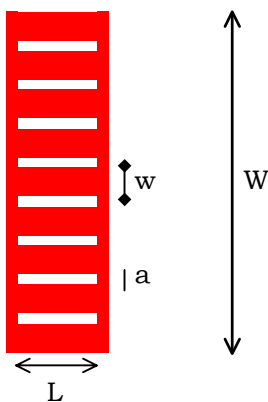
Figure 123 - Basic design of the parallel resistor array. *W* is the global width, while *w* and *L* correspond to each of the segments width and length. The inter-digitized gap width is represented by *a*.

Design parameters

The design parameters for the parallel resistor array can be seen in Figure 123. With this basic design, and supposing that all segments have an equal width (w), the total resistance for the array can be derived as:

$$R_A = \frac{R_i}{n}; \qquad \left[R_i = R_S \frac{L}{w} \right] \quad \Rightarrow \quad R_A = R_S \frac{L}{n \cdot w}$$

Equation 10 - Total array resistance in terms of segment resistance (R_i) and segment number (n). R_S is the square resistance of the polysilicon layer.

Basic design

Considering all the design restrictions imposed by simulation results, layer material and passive chip design, a basic design was proposed to see if it could be driven by the current Peltier driving system. Simulation results had limited segment length to the (4, 6) mm range, and thus the standard length for the basic design was set to 5 mm. Since the minimum width (W) to cover the whole PCR chamber was 24 mm, the remaining decision was to select the values of both segment and gap width (w and a).

Eventually, it was decided to use 1 mm wide segments, which was deemed a safe width for the current flows used, and the minimum possible (100 μm due to mask limitations, see p.126) gap width, leading to a 26.4x5 mm² device. Since the square resistance of the polysilicon layer used had been determined (both by simulation and empirical measure, see p.220) to be in the whereabouts of 15.8 Ω, the total resistance for the basic design would be about 10.401 Ω. To attain fast transient times in PCR operation, simulations had shown that 9 V (or higher) voltages were necessary. Taking into account the expected resistance of the basic design, this would mean a power consumption of 7.78W, well below the upper limit of the operational amplifier used in the Peltier driver circuitry (80W, see p.154), and this meant that the previous circuitry could be reused for the initial characterization of polysilicon resistors.