## 5.4. FABRICATION

### 5.4.1. IMPLEMENTED DESIGNS

The basic design detailed in the previous section was diversely adapted in the design masks of the prototype resistor wafers, yielding a set of different resistors with varying *W*, *w*, *L* and *a* parameters. Furthermore, longitudinal (that is, along the length axis of the PCR chamber) and serpentine-like resistor designs were also included in mask designs, to yield more information on the temperature sensing capabilities of polysilicon resistors and to be on the safe side (having available higher and intermediate resistance resistors), in case simulations had somehow run amok. Figure 124 is a sketchy illustration of the various different designs implemented.

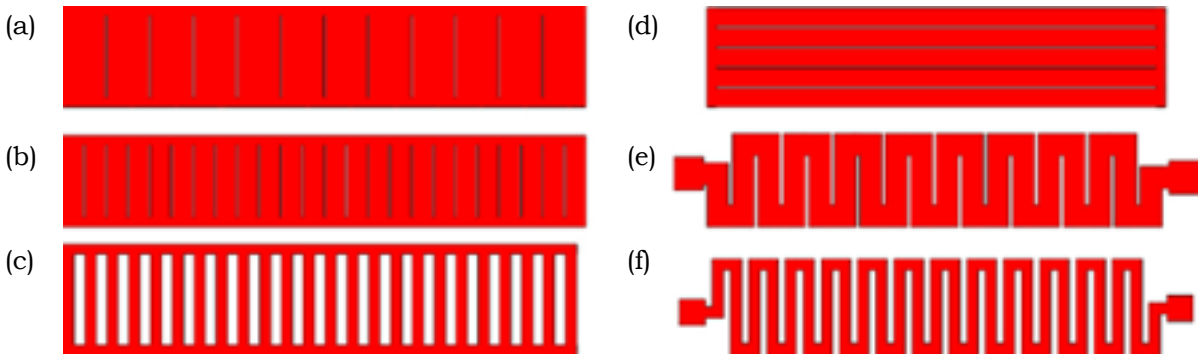


**Figure 124 -** Standard (left) and longitudinal/serpentine-like designs for polysilicon resistors: (a) W=28.6 mm, L=4 mm, w=1 mm, a=100 μm, $E_R$=2.9 Ω; (b) W=28.6 mm, L=4.5 mm, w=2.3 mm, a=100 μm, $E_R$=2.6 Ω; (c) W=28.2 mm, L=5 mm, w= 600 μm, a=500 μm, $E_R$=5.4 Ω; (d) W=5.3 mm, L=24.2 mm, w=1 mm, a=100 μm, $E_R$=35.8 Ω; (e) L=4.5 mm, w=1.2 mm, $E_R$=1.3 kΩ; (f) L=4.5 mm, w=600 μm, $E_R$=1.9 kΩ. $E_R$ is the expected resistance.

### 5.4.2. TECHNOLOGICAL PROCESS

Although the technological process for the fabrication of prototype polysilicon resistors was relatively simple, since it only implied one side processing and three photolithographic steps, care was taken in its design to ensure that it presented full compatibility with previous passive PCR-chip and CMOS processes. Compatibility with prior processes was analyzed mainly in terms of passivation layers and processes, and a full theoretical integrated process was developed in parallel to assess that none of the newly introduced technological steps precluded integration with the

previous process. Similarly, CMOS compatibility was also sought, but here with a twofold goal. On the one hand, compatibility with standard CMOS processes, which had been preserved in passive PCR-chips, would ensure that further circuitry integration was feasible and relatively straightforward. On the other hand, the use of thoroughly tested CMOS processes for polysilicon deposition and doping guaranteed that the emerging resistors would present behaviors according to simulations. Even so, and to assess whether more heavily doped polysilicon layers would result in better transient response heaters, an additional set of wafers was processed using non-standard deposition and doping processes as detailed below.

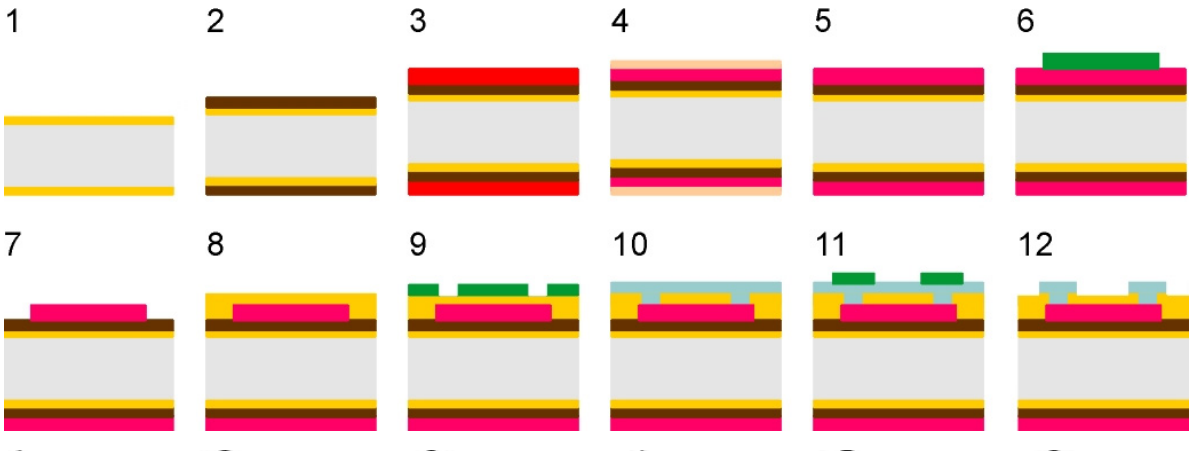


**Figure 125** - Schematic version of the technological process for production of polysilicon resistor prototypes. Layer thickness is not up to scale.

As mentioned before, the technological process for polysilicon resistor prototypes (see Figure 125) is relatively straightforward. Already standard 300 μm double-side polished <100> silicon wafers were initially passivated with a 500 Å dry oxide layer to accommodate later nitride thermal stresses (1). A 1800 Å silicon nitride was then deposited to act as an homogenous thermal distributor for the polysilicon resistors (2) and a standard 4800 Å polysilicon layer (a 6000 Å layer in the non CMOS-standard version) was deposited on top of it (3). Thereafter, the polysilicon layer was doped in standard and non-standard $O_2$+$POCl_3$ conditions, leading to the growth (4) of estimated 700 and 2000 Å thick parasitic PSG oxide layers (see *Materials and Methods*, p.286). These phosphorous-doped low-temperature oxide layers were then removed by standard HF wet chemical etching, leaving approximately 4500 and 5100 Å doped polysilicon layers (5) that were patterned into the desired resistor shapes by standard and semi-standard

photolithography (6) and RIE-etch (7) processes. The resulting resistors were then insulated (8) with a 5000 Å pyrox oxide layer (see *Materials and Methods*, p.287) into which contact holes were patterned and bored (9) by standard wet chemical etch. Subsequently, a 1 μm thick aluminum (AlSiCu) layer (see *Materials and Methods*, p.286) was deposited to completely fill the contact holes and cover the wafer (10). The aluminum layer was finally patterned by standard photolithography (11) and wet etching (12), producing contact pads for the buried polysilicon resistors.

## 5.5. DEVICE TEST AND CHARACTERIZATION

Fabricated devices were tested and characterized in a three-step approach. Polysilicon resistor values were first estimated by direct measurement on the uncut wafers. Thereafter, polysilicon chips were cut and wire-bonded to a custom printed circuit board (PCB), and their behavior as actuators (heaters) and temperature sensors was functionally characterized.

### 5.5.1. CHARACTERIZATION OF FABRICATION PARAMETERS

A first resistance value for each of the designed resistors was gauged by direct measurement on the uncut wafers with a 86H3 Graphical multi-meter (*Fluke*). Measurements were repeated thrice and averaged at different pad positions to account for irregularities in the probe-pad interface. These results (see Table 17) were important since they indicated the offset and deviation of fabricated resistors with respect to simulation and theoretical estimates, thus giving clues for the prediction of real resistor values in further fabrication processes.

Standard doping

| $E_R$ (Ω) | R wafer#1 (Ω) | R wafer #2 (Ω) |
|---|---|---|
| 2.469 | 4.1 ±0.1 | 4.0 ±0.1 |
| 2.514 | 3.8 ±0.1 | 3.7 ±0.1 |
| 2.693 | 4.1 ±0.1 | 4.0 ±0.1 |
| 2.962 | 4.5 ±0.1 | 4.3 ±0.1 |
| 5.486 | 7.3 ±0.1 | 7.1 ±0.1 |
| 1350.9 | 974 ±1 | 992 ±1 |
| 1990.8 | 3337 ±1 | 3358 ±1 |

Non-standard doping

| $E_R$ (Ω) | R wafer#3 (Ω) | R wafer#4 (Ω) |
|---|---|---|
| 1.177 | 2.4 ±0.1 | 2.3 ±0.1 |
| 2.569 | 4.1 ±0.1 | 4.1 ±0.1 |
| 35.816 | 41.4 ±0.1 | 40.7 ±0.1 |
| 44.77 | 51.8 ±0.1 | 50.6 ±0.1 |
| 632.7 | 502 ±1 | 498 ±1 |
| 932.4 | 1698 ±1 | 1680 ±1 |

**Table 17 -** Predicted ($E_R$) and wafer-measured resistances for different polysilicon resistor designs.

### 5.5.2. EXPERIMENTAL SETUP

To experimentally characterize the behavior of polysilicon resistors, chips were mounted and glued with thermo-curable epoxy resin on a custom PCB support (see *Materials and Methods*, p.303) and then wire-bonded to PCB contact pads using a Ø381 μm wire capable of delivering up to 5 A currents. Initial PCB systems (see Figure 126a) were simple rectangular boards onto which the chip was directly mounted. Later custom PCB designs (see Figure 126b) had a central rectangular hole for chip ventilation and four machined cylindrical holes into which long Ø6 mm screws were inserted to act as pedestals. Using two sets of nuts and washers, a 1.1W-12 V electric fan (*Sunon*) was attached to the base of the system to provide air-driven heat dissipation. For temperature monitoring, the in-board Pt100 sensor was then placed on the side of the chip opposite to the polysilicon resistors over a 340 heat-sink compound layer (*Dow Corning*) and held into place with 25 mm heat resistant acrylic tape (*Kapton*). The Labview control software was modified to generate passive 0 V thrust (instead of the negative thrust used in Peltier driven systems) for cooling.

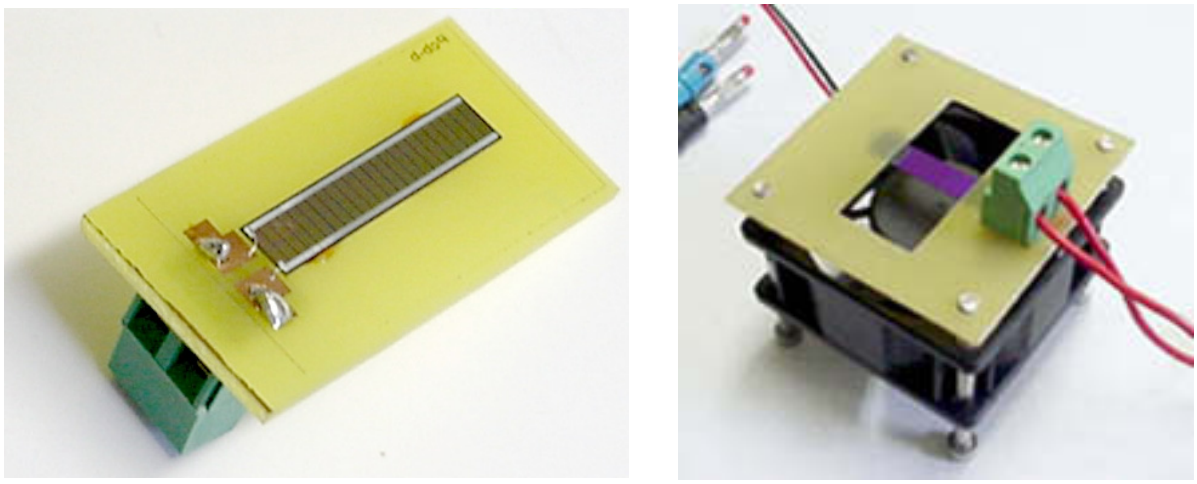

**Figure 126 -** Initial, less efficient chip-holder PCB design (a) and the later optimized design with the attached cooling fan (b).

### 5.5.3. ACTUATOR CHARACTERIZATION

Using the aforementioned initial setup, the heating performance of different kinds of polysilicon resistors was tested. As expected, high-resistance (kΩ) configurations did not yield any temperature change whatsoever and medium-resistance (longitudinal ~50 Ω) ones generated only very slow temperature gradients reaching, at full thrust, temperature differentials

always below the 20-25 ºC range. However, for those resistors designed according to simulation results (2-10 Ω), the experimental yields were very satisfactory. Figure 127 illustrates a non fine-tuned temperature cycling operation with 2.4 and 7.2 Ω resistors. Even though, due to stability problems, the driver thrust was software-limited to 1.5 V (meaning peak 3 A/5 V and 1.5 A/10 V intensity/voltage pairs respectively), 15 ºC/s heating and 4 ºC/s cooling rates were easily attained with the initial PCB configuration.

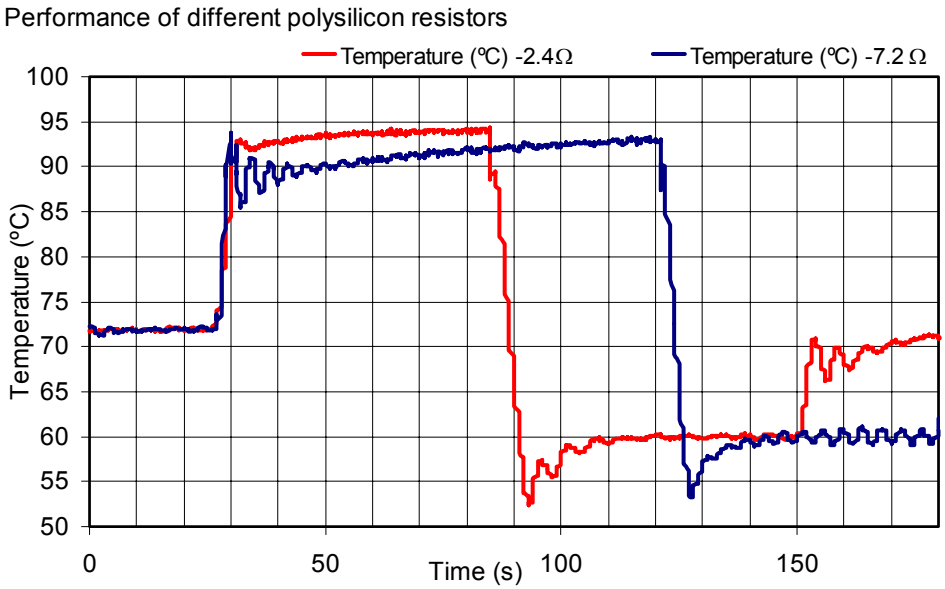


**Figure 127** - Initial, non fine-tuned polysilicon resistor PCR cycling experiments for 7.2 and 2.4 Ω resistors. Heat rates are very similar for both resistors due to driver thrust capping at 15W.

## Comparison with Peltier driven systems

After some tinkering with the temperature control system parameters to provide more stability, new experiments were done with the improved PCB setup and the results were compared with existing data for Peltier driven systems. As expected, polysilicon resistor results for heating far surpassed those obtained with Peltier systems. Without the additional thermal load of the subjacent plastic board, the polysilicon resistor could now easily deliver 25 ºC/s heating rates and in a more stable way. Clearly, higher heating rates were available (Figure 128 experiments were limited to 10W thrust, while the driver nominal output power was 80W), but they became excessively unstable and, in conventional PCR operation (with maximal temperature differential of about 40 ºC), they were not much useful. With

the improved ventilation, polysilicon resistor cooling yields were also remarkable, nearly rivaling those of Peltier driven systems (5 ºC/s).

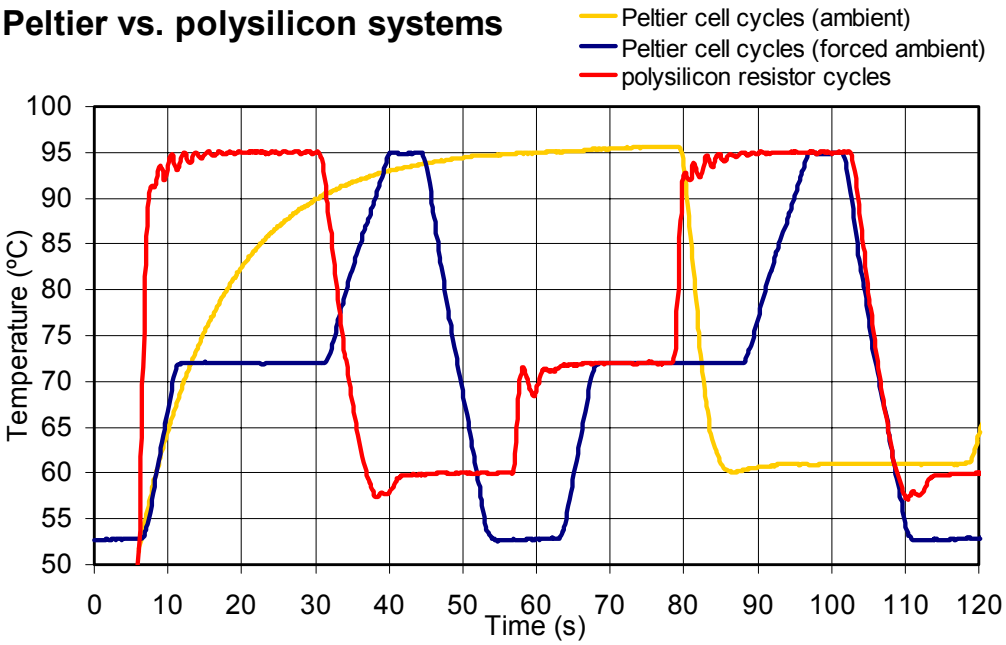


**Figure 128** - Performance comparison for all used driving systems: room-ambient (see p.168) and forced-ambient (see p.169) Peltier systems and a 7.5 Ω polysilicon resistor limited at 10W.

But perhaps the most outstanding advantage of polysilicon systems was their low power consumption (about 2W for the average PCR cycle) when compared with Peltier systems (about 18W for the average PCR cycle at standard ambient temperature). These results are summarized in Table 18.

| Heating system | Heating rate (ºC/s) | Cooling rate (ºC/s) | Power consumption (W) | | | | |
|---|---|---|---|---|---|---|---|
| | | | Average | Heat ramp (peak/av.) | Cool ramp (peak/av.) | 95 ºC hold (av.) | 61 ºC hold (av.) |
| **Polysilicon heater*** | 25 | 5.2 | 2.0 | 11/7 | 0/0 | 2.8 | 1.4 |
| **Forced-ambient Peltier**** | 3.2 | 5.2 | 6.4 | 30/25 | 36/30 | 7.5 | 0.2 |
| **Standard ambient Peltier** | 0.9 | 7.2 | 18.5 | 27/23 | 38/28 | 21.4 | 7.4 |

* Fan power consumption not taken into account
** Hot-plate power consumption not taken into account

**Table 18** - Comparison between assayed Peltier and polysilicon heating systems.

### *Thin-film vs. Peltier systems*

Although, in the light of the previous results, polysilicon resistors stood a far better option than Peltier cells for driving chip PCR systems, this might

not be the general case. The disparity of results between polysilicon resistors and Peltier cells stems mainly from the extra thermal mass that Peltier cells add to the system, and not from a better intrinsic heating performance of resistors over Peltier cells. Therefore, if PCR-chips are shrunk down to the pico-liter volume (millimeter size, [Murakami2000]) and smaller Peltier cells can be used, the performance difference between both kinds of device should progressively even out. The same net effect, or even a better performance of Peltier cells over thin-film resistors, could be attained if high-throughput Peltier devices could be integrated somehow on the silicon chip.

### 5.5.4. SENSOR CHARACTERIZATION

After having characterized the actuator properties of the fabricated polysilicon resistors, an analysis of their sensing properties was conducted. Experiments were done with the highest-resistance (7.5 Ω) resistor capable of providing fast transient responses as an actuator. The aim was to first evaluate the resistor TCR and its feasibility as a temperature-sensing element. If they were sound, then its dual (simultaneous) sensor-actuator feasibility would be evaluated.

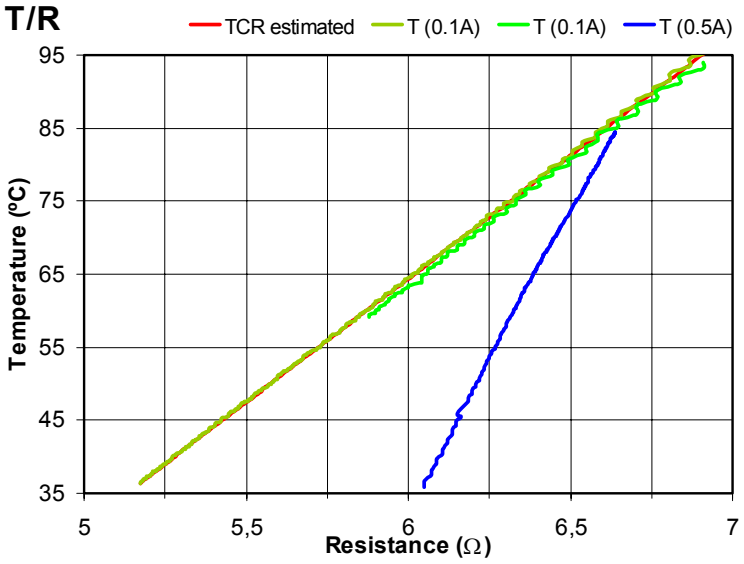


**Figure 129** - Evaluation of a 7.2 Ω polysilicon resistor temperature-sensing capabilities. Green lines show cooling (0.1 A) resistance measures, while the blue line corresponds to an active heating (0.5 A) set of measures. The subjacent red line is the resistance linear-extrapolated temperature value according to the measured TCR ($5.7 \cdot 10^{-3}$ $ºC^{-1}$).

Sensor characterization of polysilicon resistors (see Figure 129) bore various positive results. On the one hand, the measured TCR was tenfold greater

than that predicted by simulations (about $5.7 \cdot 10^{-3}$ °C$^{-1}$) and close to that of common temperature sensing materials (e.g. platinum, chrome, etc.). Although such an enlarged TCR could be the side effect of measurements with resistor values (4-6 Ω) close in range to predicted resistance differentials, what seemed conclusive was that the theoretically predicted TCR was somewhat smaller than the measured one. This meant that temperature variations would yield larger resistance differentials, resulting in more accurate temperature readings. On the other hand, the thermal-resistive response of polysilicon was found to be extremely linear in the desired temperature range (30-100 °C), as shown by the almost-exact linear fit of TCR-extrapolated temperature values (see red line in Figure 129). The different T/R slope (blue line in Figure 129) for actively heated measures (with a 0.5 A current flow across the resistance) was interpreted not as a varying TCR, but as the effect of a linear thermal gradient between the actively heated polysilicon layer and the measuring Pt100 probe. This phenomenon would not be observed in cooling (0.1 A) measurements, since both the polysilicon resistor and the measuring probe would be at roughly the same (device average) temperature, but its occurrence was quite plausible during heating measurements, in which the resistor temperature could rise substantially faster than the overall device (measured) temperature. Nevertheless, if the polysilicon layer was to be used both as sensor and actuator, current-induced effects on the measured temperature had to be carefully assessed and, hence, a new set of measurements was carried out to evaluate the nature of these effects.

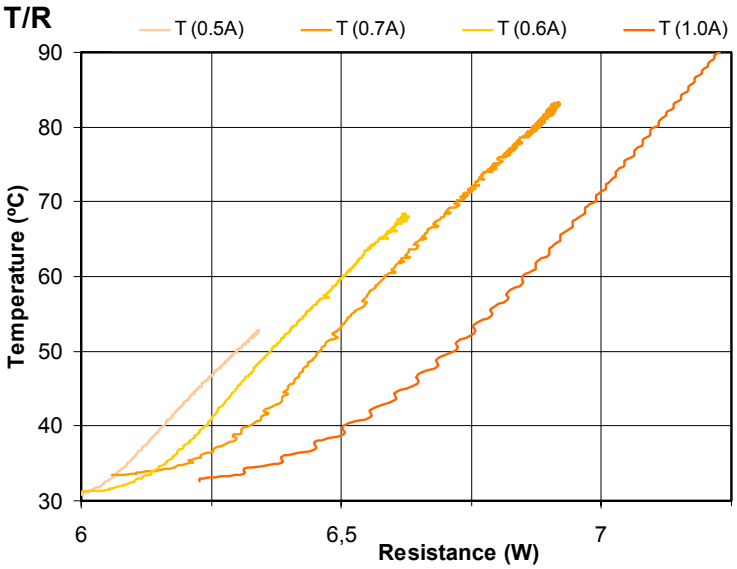


**Figure 130** - Resistance variation with temperature for a 7.2 Ω polysilicon resistor at increasing heating currents (0.5-1.0 A).

Results for this last set of measurements (see Figure 130) indicated that there existed a correlation between increased currents and an offset in the measured resistance. Furthermore, even though all data sets tended to stabilize at the same T/R slope, there was a transitory period before stabilization did take place. All these facts suggested the involvement of classical Joule effects in the heated polysilicon resistors. Hence, even if the correlation between increasing currents and resistances was linear or could be easily modeled, the apparition of Joule-induced transitory periods introduced an excessive uncertainty for coupling both sensor and actuator capabilities in a same polysilicon resistor.

## 5.6. INTEGRATED ACTIVE PCR CHIPS

The successful work done on bare polysilicon resistor chips and the experience gained from passive PCR-chip experimentation were used as the main guide-lines for the integration of active heat-driving circuitry in PCR-chips; that is, the development of standard passive PCR-chips with integrated polysilicon resistors capable of both temperature driving and sensing. Although at times intermingled, this converging work between passive PCR-chip and polysilicon resistor experimentation can be divided into two main areas: technological integration and system design.

### 5.6.1. SYSTEM DESIGN

Even though the system behavior might have benefited from some design changes (as a scaling down of the chip), it was decided to stick to the current passive PCR-chip design in the first stage of technological integration. The reasons for this decision are many. On the one hand, all the previous experimental work with passive PCR-chips had been conducted in 25-30 μl $SiO_2$-coated glass-bonded chips, and all the experimental setup (methacrilate devices, etc.) had also been tailored to these chips. On the other hand, although polysilicon resistor parameters could be extrapolated to other magnitudes, experimental assays had only been conducted with passive PCR-chip size resistors. Overlying it all, there was the hard-acknowledged fact that PCR can be an extremely capricious reaction and thus, it was deemed safer to first carry out the integration process under known conditions and then, if feasible, conduct the anticipated scaling down or any other design changes that might seem fit.

Therefore, the design of integrated devices was bound by several constrains arising from all the previous work done with passive PCR and polysilicon resistor chips.

## Design constraints

### *Size and reservoir design constraints*

In order to fit into the already developed experimental setup, active PCR-chips had to present the same external shape to methacrilate devices and other systems (like Peltier cells). Making the designs compatible with previous passive PCR-chips did not only avert the introduction of new unforeseen effects, but also allowed to conduct experimental results using the same chip and the two kinds of temperature control systems. Therefore, design was restricted to the already developed 40x10 $mm^2$ area chips and, since polysilicon resistor integration also implied double-side processing, to 300 μm-thick wafers. Regarding reservoir design, it was decided to stay with the insofar-successful rhomboidal geometry, although some serpentine-like designs were also included to make, if possible, a quantitative efficiency comparison between both kinds of systems.

### *Sensor/actuator constraints*

Concerning the design of the active circuitry of the chips, the conclusions drawn from the previous simulation and experimentation with polysilicon resistors were acknowledged in a variety of ways. For instance, experimental results indicated that, due to Joule effects in heating resistors (see p.231), it was much safer to implement separate sensor and actuator resistors, and this was the trend adopted here. Regarding their design, simulation and experimentation results had strongly hinted at a parallel resistor grid covering the whole PCR reservoir area as the most suitable design for actuators. A similar reasoning could also be derived for sensors, creating not a single point sensor that could hinder system efficiency with false reads (due, for instance, to the presence of an air bubble over the sensor area [Zhan2000]), but a parallel resistor grid that also covered the whole reaction area and delivered an average temperature reading.

Finally, concerning the resistance value of polysilicon resistors, different estimates were made for sensor and actuator resistors. On the one hand, previous experimentation suggested that the best actuator design was one

with the highest resistance capable of providing fast transients (~6-10 Ω). The main reason for this inference was that low-resistance actuators tended to saturate the driver more easily (drawing more current) and were more difficult to control and stabilize. On the other hand, intuition and experimental results hinted at a far greater increase in the resistance value for sensor resistors. The advantage of large resistance (>50 Ω) sensors was twofold. Firstly, for a given reading voltage, they would admit smaller current flows and thus present lower self-heating, which also implied less non-linear Joule effects. Secondly, greater resistances would also imply larger, more readable, measured voltage changes when a fixed current flow was passed through them. Nevertheless, too large a resistance would imply too small currents of difficult handling and, therefore, taking into account the experimentally measured TCR for polysilicon layers, a resistance value close to that of standard Pt100 RTD sensors (~50-100 Ω) was chosen.

### Implemented design

Hence, the overall design for integrated PCR-chips was almost fully dictated by the design constraints of previous research. The final basic design (see Figure 131) incorporated a rhomboidal 24x5 mm² reservoir and sensor and actuator polysilicon inter-digitized resistor grids with a global resistance value of 55.3 Ω and 4.38 Ω, respectively (estimated from a 15.8 Ω theoretical square resistance value). Contact pads were placed at the inlet/outlet hole adjacent region, taking into account the space required for clamping toric joints.

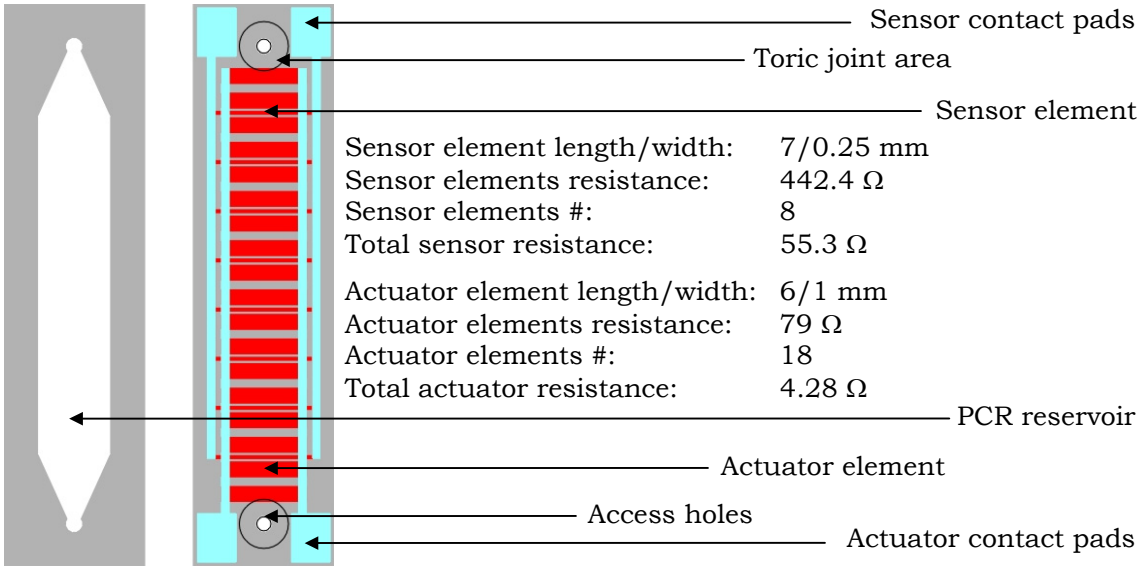


**Figure 131** - Basic design of the integrated active PCR-chips

### *Design discussion*

In the abovementioned scheme, there are several design issues open to discussion. The inter-digitized sensor/actuator design, for instance, was the only possible design option for covering the whole reservoir region with sensors and actuators using a single polysilicon layer. The possibility of introducing a second polysilicon layer and the effects of cross-talk between sensor and actuator elements in the inter-digitized scheme were considered at depth, but it was decided that, due to several reasons, sticking at a single-layer design was the best worst option. On the one hand, including a second polysilicon (or platinum) layer for sensing would require the inclusion of a passivation layer, a new set of contact holes and, in general, it would further complicate a technological process that was already complex. On the other hand, even though two-level perpendicular arrays would minimize cross-talk between sensor and actuator grids, the separation distance between parallel sensor and actuator grid elements (300 μm) in the chosen design was considered safe enough and much larger than the one that could be obtained using an intermediate layer. When taking into account the resistivity of air as compared to that of a dry oxide layer and the difference in layer thickness for both cases, it was considered that the use of parallel inter-digitized arrays was a sensible enough approach for minimizing process complexity. Moreover, the use of a single polysilicon and aluminum layer left the way open for a quite straightforward CMOS process integration. The final total resistance for the sensor (55.3 Ω) was obtained as a settlement between the thinnest possible sensor elements (100 μm with the type of masks here used, see p.126) and a sensible number of elements to make an average read. Although, for the same number of sensor elements, resistance could have been boosted up to ~100 Ω using 150 μm thick (instead of 250 μm thick) sensor elements, this thickness value was deemed too close to the resolution limit, and the advantage that it offered in terms of lower self-heating effects was sacrificed for design reliability. Similarly, the location and size of contact pads was a compromise solution between a possible increase in noise coupling factors and a large enough area to effectively make contact with the resistors. Since the ultimate shape and nature of the holding/clamping device for active PCR-chips had not been determined at this design stage, it was decided to use the largest possible area pads to forestall any unforeseen

clamping/contact problems. Finally, as it has already been partially discussed (see p.234), there is the size of rhomboidal reservoirs. Even though chips had to fit the available mechanical setup, it could have been possible to build some smaller volume reservoirs by thinning the rhomboidal shape. Nevertheless, since previous fabrication runs had resulted in several wafers broken during the production process, it was considered a priority to incorporate the maximum number of identical designs per wafer, in order to end with enough testable chips for conducting reproducible experimentation. Therefore, only some serpentine-like ~20 µl chips (see Figure 132) were included for comparison and all the rhomboidal chips were designed with the same reservoir volume (approximately 30.6 µl for a 175 µm etch; see *Materials and Methods*, p.285 for the complete mask set).

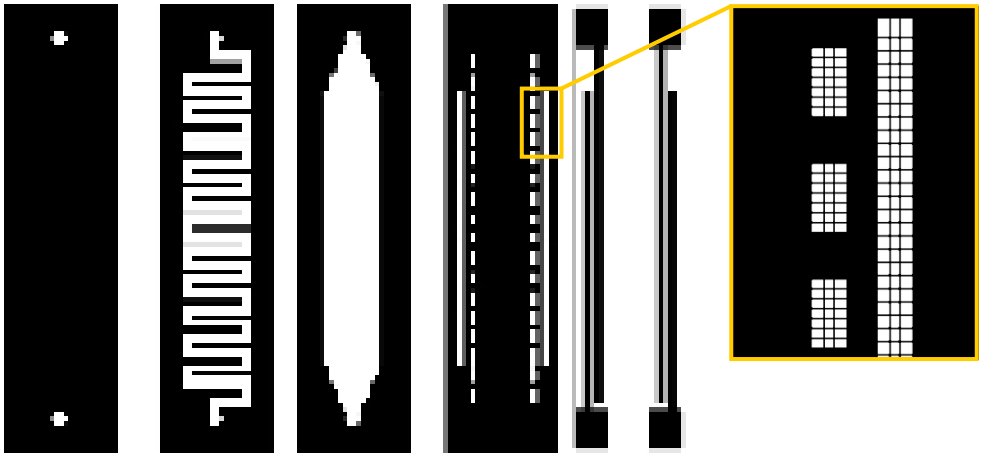

**Figure 132** - Basic mask-set for serpentine and rhomboidal integrated active PCR-chips. A detail section of contact holes, divided into sub-array patterns to maximize electrical conductivity, is shown at right. All masks, except for the aluminum (rightmost) layer mask, are dark-field sets.

### 5.6.2. TECHNOLOGICAL PROCESS INTEGRATION

Since passive PCR-chips had already been produced by double-side processing techniques to obtain silicon-etched back access holes (see p.120), the integration of passive PCR-chips and polysilicon resistors technological processes was relatively straightforward. The major challenge was to find a seamless way to integrate passive PCR-chip micro-machining and passivation processes with back-side polysilicon and aluminum deposition and patterning, and to somehow adapt these layers to the astringent conditions required for opening access holes by deep silicon

micro-machining on the backside. Therefore, much of the process design work was based on the swapping of technological steps and the nature of the passivation layers used, since a dry oxide passivation layer, like the one previously used in passive PCR-chips, was desired on the reservoir to minimize any differences with previous experiments. The final technological process that was agreed upon after long and enlightening discussions with clean room personnel, is only one of the theoretically possible and is sketchily depicted in Figure 133 (see *Materials and Methods*, p.281 for a detailed account).

In essence, the process starts with the basic setup for polysilicon resistor processing (1). Double-side polished, 300 µm P-type <100> silicon wafers are first dry oxidized (500 Å) to accommodate nitride stress and then $Si_3N_4$ and polysilicon layers (1800 and 4800 Å respectively) are deposited on both sides of the wafer (see *Materials and Methods*, p.286). The polysilicon layer is then doped with phosphorous impurities and the ensuing PSG layer removed by wet etching (2).

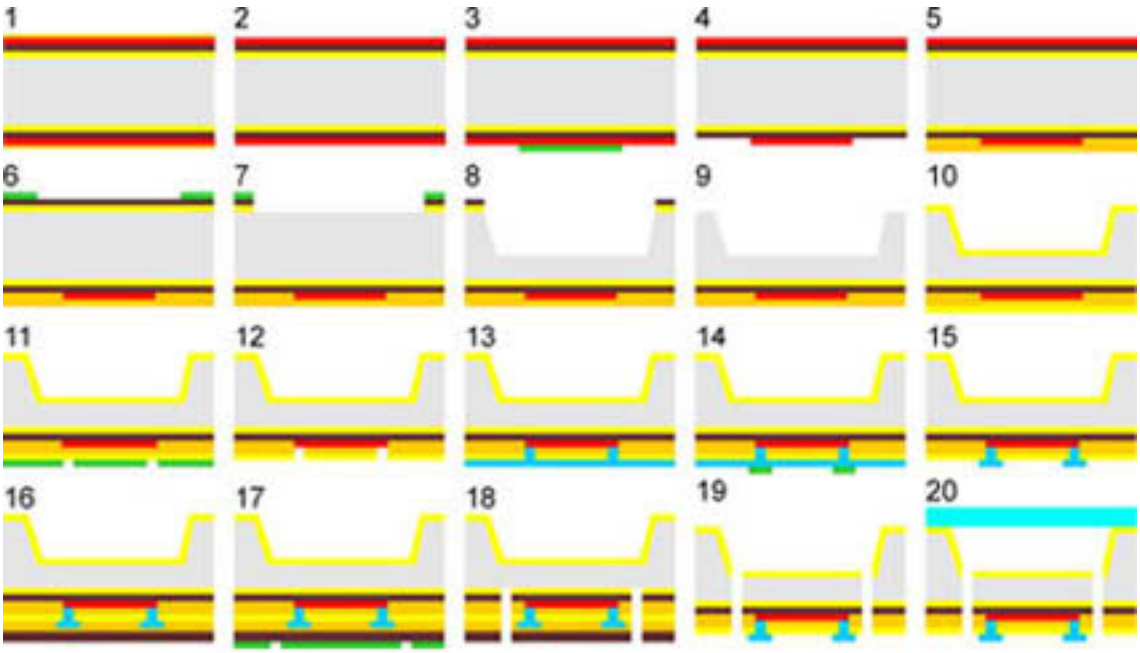


**Figure 133** - Simplified scheme of the complete technological process for integrated active PCR-chips. Layer thickness is not up to scale.

Back-side polysilicon is then patterned with a photo-curable resist (3) and RIE-etched to produce resistor outlines (4). Finally (5), the back-side polysilicon layer is passivated with a thick layer of Pyrox deposited oxide (5500 Å). The process for etching of the PCR reservoirs begins thereafter.

The front-side polysilicon layer is removed by wet chemical etching and the underlying nitride patterned by standard photolithography (6) and etched away, together with the oxide layer below, by RIE-etch (7). The resulting window (8) is then used for a deep TMAH silicon etch (175 μm), with the backside mechanically protected (see *Materials and Methods*, p.293). The window layers (nitride and thermal oxide) are removed again by RIE-etch (9) and the whole wafer is dry oxidized anew (500 Å) to provide the PCR-friendly passivation layer on the front side (10). After the front side process has been completed, the process switches again to the backside. The double-oxide passivation layer is patterned (11) and etched away with RIE-etch to open contact holes with the polysilicon resistors (12). Aluminum (AlSiCu, 1 μm) is then deposited on the backside (13), patterned (14) and wet etched (15) to define the contact pads. Then, the whole backside structure is heavily passivated (16) with a standard CMOS sandwich layer ($SiO_2$-$Si_3N_4$, 4000-7000 Å) to withstand the deep silicon hole etch. The new passivation layer is patterned (17) and etched (18), together with the underlying oxide and nitride layers, by successive RIE-etch attacks, until the core silicon is exposed. Finally (19), a RIE-etch (it was intended to be a TMAH etch, but it presented aluminum liftoff problems, see Figure 134) is carried out to deep etch (125 μm) the silicon layer and then the minimal front-side passivation layer (500 Å). To prevent membrane breakage during perforation due to differential air pressure in the RIE-chamber, the front-side was initially protected with a thick (8 μm) layer of positive photo-resist (see *Materials and Methods*, p.288). After the deep RIE-etch, front-side positive photo-resist was removed and the wafers underwent anodic bonding (20) with a 0.5 mm-thick glass wafer (see *Materials and Methods*, p.294).

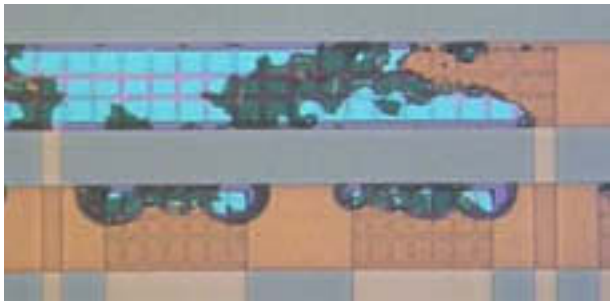

**Figure 134** - Degraded (blue) aluminum tracks (brown) due to liftoff processes during TMAH backside etch.