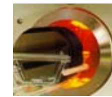


walls and the wafer tray. This causes the reactor to be periodically disassembled and cleaned.

In a cold wall reactor (also known as an adiabatic wall reactor) the substrate to be coated is heated directly either by induction or by radiant heating. It has to be taken into account that most CVD reactions are endothermic. Thence, deposition takes place where the temperature is the highest, while at the coldest zones, as in this case are the walls, remain uncoated, being unnecessary to be disassembled as often as the hot walls reactor.

When comparing the previous CVD deposition techniques, it is observed that LPCVD provides with layers having much higher quality and uniformity. Thus, LPCVD silicon nitride layers are the most suitable for the first cladding layer in the ARROW-A configuration, with thicknesses of 0.13µm (at first antiresonant condition) or 0.38µm (at second antiresonant condition). For obtaining the core of the ARROW-A structure, a deposition technique that permits having thick layers with the selected refractive index is required. This system is also required not only for obtaining the core of the ARROW-B structure, but also for its antiresonant layers. Unfortunately, these layers cannot be obtained either by thermal oxidation or LPCVD processes, since no large modification on the refractive index is possible. Thence, a complementary technique, the Plasma Enhanced CVD has to be used.

Plasma Enhanced CVD

In the thermal CVD processes just reviewed, the reaction was activated by thermal energy transferred to the system. There are compounds that decompose when temperature is raised above certain value. Then, an alternative energy transfer method should be selected.

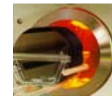
When a gas is progressively heated, it is gradually dissociated so that the reactive species obtained are atomic or molecular fractions. Obtaining complete gas ionization, that is, only having reactive species at atomic level would require a huge amount of energy (T>5000ºC) which obviously is a non-feasible temperature for deposition processes. An alternative way to achieve this energy is by using a low frequency discharge. Under such conditions, both ions and electrons are able to follow

the constantly changing field direction and progressively acquire energy, raising equally their temperature. Then the plasma is said to be in equilibrium (isothermal). Generally, these plasmas are generated at relatively high pressure (10-100KPa), which represents an important reduction of the mean free path, causing collisions to be much more frequent and a fast heating of the ionized precursors. Moreover, such plasmas require a large amount of power and are extremely hot. Due to this fact, they are rarely used except in the diamond deposition.

If, instead of a low frequency, a high frequency field is applied under lower pressures, as is the example shown in table 3.5, the precursors are also ionized. Electrons, which are much lighter than atoms or radicals, are quickly accelerated under the applied electromagnetic field, until energetic levels corresponding to 5000ºC. Since their mass is low, it does not cause a significant overall temperature raise. Ions, however, are so massive that cannot respond to the applied field and thence its contribution to the temperature is negligible. When a highly energetic electron collide with the gas molecules, the latter are dissociated, generating the reactive chemical species which, since the system works under low pressure, fastly diffuse through the boundary layer, reaching the substrate surface and starting the previously described chemical vapor deposition mechanism.

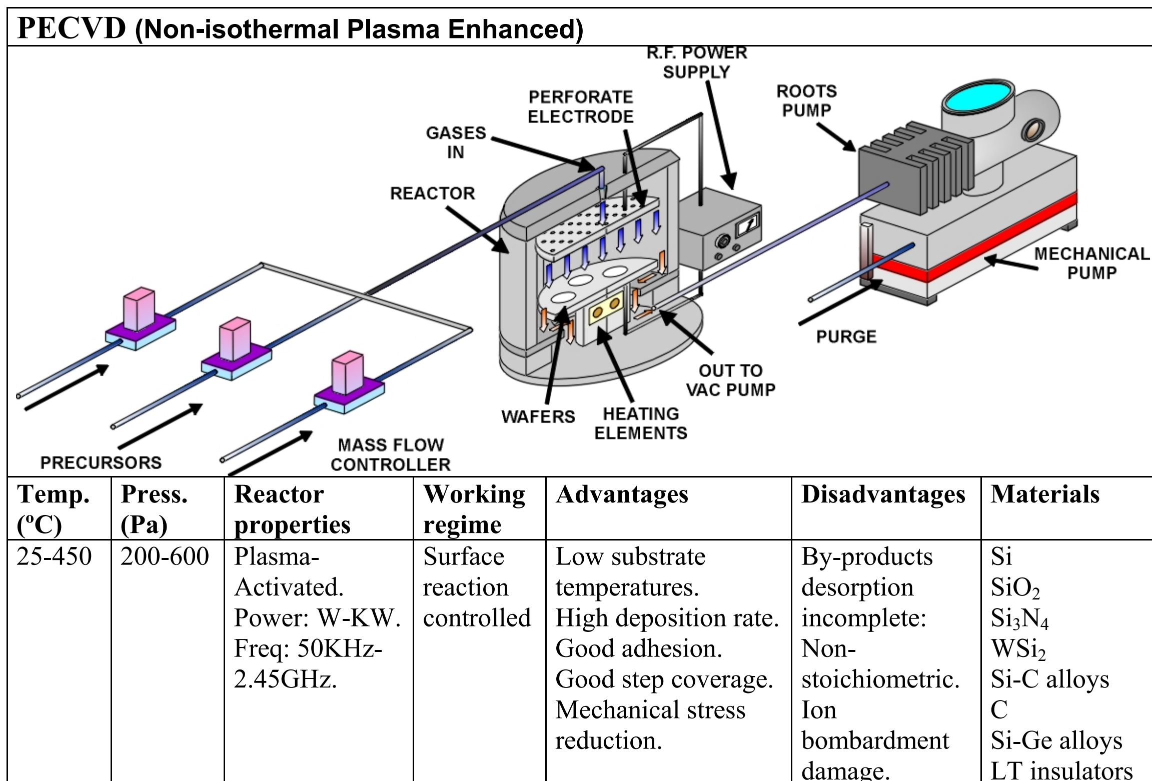
As compared to Thermal CVD systems, PECVD offers several advantages. The most noteworthy of them is the availability of working at temperatures where no CVD processes (excepting MOCVD) would obtain a deposited layer. It allows coating low-temperature materials as could be aluminum or organic polymers. Less critical at low temperatures, but crucial for microelectronics, is the fact that dopant species, such as boron or phosphorus, fastly diffuse between buried layers if the substrate temperature exceeds 800ºC, resulting in irreversible changes in the device properties. With PECVD these substrates can be coated without causing dopant diffusion.

Deposition rate in a PE system working at low pressure still is surface-reaction limited, then, layers are quite homogeneous and uniform, with higher speed growth as compared to an equivalent LPCVD system. Moreover, the low temperature allows



obtaining layers which, due to the mismatch between the layer and the substrate mechanical constants, will surely crack during reactor heating/cooling.

PECVD (Non-isothermal Plasma Enhanced)



Temp. (ºC)	Press. (Pa)	Reactor properties	Working regime	Advantages	Disadvantages	Materials
25-450	200-600	Plasma-Activated. Power: W-KW. Freq: 50KHz-2.45GHz.	Surface reaction controlled	Low substrate temperatures. High deposition rate. Good adhesion. Good step coverage. Mechanical stress reduction.	By-products desorption incomplete: Non-stoichiometric. Ion bombardment damage.	Si SiO_2 Si_3N_4 WSi_2 Si-C alloys C Si-Ge alloys LT insulators

Table 3.5: Standard configuration and general properties of a PECVD system.

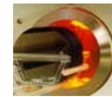
The main drawbacks of plasma deposited layers are due to the inherent impurity presence on the deposited layers: desorption of by-products and carrier gases (if any) is incomplete because of the low temperature and these gases remain included in the growth layer. PECVD films mostly are non-stoichiometric because the deposition reactions vary widely depending on the working conditions. Moreover, particle bombardment during growth continuously increases its defect number. Although layer properties depend on each system, some generalizations can be done according to the reactor parameter settings: **Working pressure:** Obviously, the mean free path increases as the pressure decreases. Consequently, ions can have more energy before the impact and the effect of ion bombardment is more pronounced at lower pressures. Generally, microstructure, stress, density and other film properties show marked response to ion bombardment. **RF power effects:** An increase of the RF power leads to more intense

ion bombardment, increasing the growth rate but worsening the uniformity. Thence, it must be reached an agreement between both parameters. **Growth temperature:** Temperature has a strong influence on the film structure. At low temperature and pressure, the diffusion at the surface is low as compared to the precursors arrival rate. In this situation, the adsorbed precursor molecules are likely to interact between them before it can find its nucleation point, forming an amorphous layer. At high temperatures, the surface diffusion is fast, nucleation points can be found by precursors and crystalline materials can be obtained.

As far as deposition parameters are concerned, low pressure, balanced RF power/growth ratio and temperature according to the desired layer crystalline phase would provide with the best quality available layers. For integrated optics applications, this technique is essential since simply by varying the reactant ratio, it is possible to vary the refractive index of the layers. Then, it would allow obtaining the core for the ARROW-A and the whole ARROW-B structure at low deposition temperatures (300ºC).

3.3 Photolithography

The integrated optical device manufacture consists on a sequence of steps, at which films could be grown, deposited, etched or doped. Technology would be severely limited if the previously mentioned steps could only be done at wafer level, since the key point, not only in integrated optics, but also in any integrated circuit, is the possibility to modify a concrete zone of the wafer, keeping the rest unaltered. This is achieved via the photolithography. Essentially, this process consists on the transference of two-dimensional patterns placed on the mask to an organic polymer, the photoresist. After being developed, it has an exact copy of the mask patterns. At this point, any technological step will only be done at the photoresist-free zones. An entire photolithographic process is schematically presented in fig. 3.4, together with a mask aligner similar to the one employed for obtaining integrated optics devices.



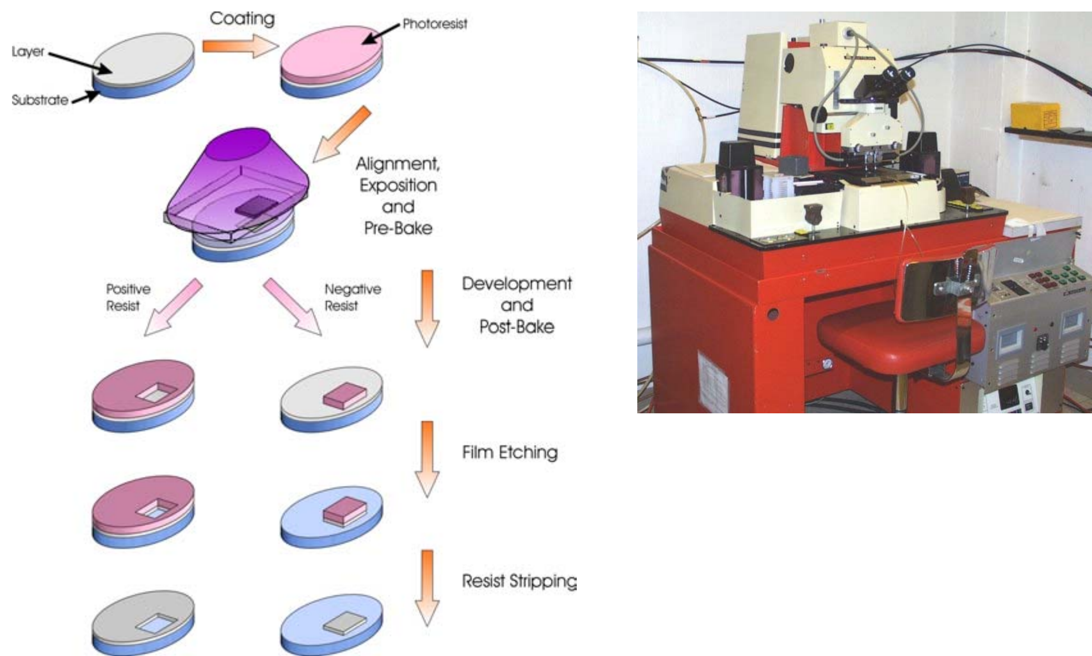


Fig. 3.4 Standard Photolithographic process steps and Karl-Suss MJB Mask Aligner.

3.3.1 Photoresist

As the first step in the photolithography process, a thin film of UV-sensitive photoresist is deposited on the surface of the layer to be patterned. The photoresist is dispensed from a viscous solution onto the wafer placed in a resist spinner. It clearly is one example of the liquid phase chemical processes briefly explained in section 3.2. A vacuum chuck holds the wafer in its position. The wafer is then spun at a high speed that varies depending on the polymer viscosity and the required thickness. At the selected velocity, the centrifugal forces cause the solution to flow towards the edges, covering the entire wafer.

Photoresist are called positive (or positive tone) when the photochemical reaction during its exposure causes an increase of the solubility in developing solutions. They are mainly formed by three basic components: a photoactivator, a low molecular weight polymer and a solvent. Polymer acts as a mere support for the photoactive component and UV-exposition does not modify its structure. The photoactive component becomes soluble after the exposition, weakening the polymer structure by rupture or scission of their polymer chains and enhancing the dissolution of the resist in

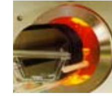
the developer. The solvent acts as a viscosity controller in order to easy the spinning conditions.

The principal components of negative photoresists (also negative tone) are a low molecular weight polymer (base resin), a sensitizer, and a casting solvent. The polymer changes its structure if exposed to radiation. The solvent allows the previously mentioned spinning and formation of thin layers on the substrate surface. Sensitizers are responsible to control the chemical reactions in the polymeric phase. UV radiation strengthen the polymer by random polymer chains cross-linkage (photo-polymerization) that causes an increase of its molecular weight, becoming less soluble. Sensitizes enhances the photo-polymerization reaction and decreases the necessary exposure time.

A comparison between both types of photoresists are presented in table 3.6. The choice between them depends on a large variety of considerations, as could be cost, speed, resolution or equipment. It will even depend on the specific intended pattern. For example, an isolated single line (a waveguide) most easily resolves in a negative resist (higher resolution line), whereas an isolated trench is most easily defined in a positive resist. However, due to equipment simplicity and handling easiness, we will always work with positive resists, except when the contrary is specified.

Properties	**Positive Resist**	**Negative Resist**
Adhesion to Si	Fair	Excellent
Available Compositions	Many	Vast
Contrast/Resolution	High	Low
Cost	Expensive	Cheap
Developer	Aqueous-based	Organic Solvent
Developer process window	Small	Wide, insensitive to overdeveloping
Image width to resist thickness	1:1	3:1
Influence of Oxygen	No	Yes
Lift-Off	Yes	Unusual
Minimum feature	$< 0.5\mu m$	$1\mu m$
Opaque dirt on clear mask effect	Not much effect	Pinhole printing
Pinhole count	Higher	Lower
Pinholes in mask	Higher	Lower
Proximity effect	Prints isolated trenches better	Print isolates lines better
Residue after development	Mostly $<1\mu m$	Often a problem
Step Coverage	Good	Fair
Swelling in developer	No	Yes
Thermal stability	Good	Fair
Wet chemical resistance	Fair	Excellent
Easy to handle	Good	Fair

Table 3.6. Comparison of Positive and Negative Photoresists.



After the deposition and before the exposition, wafers normally have a thermal treatment that eliminates the solvent contained in the photoresist and enhances adhesion to the substrate. This stage, called pre-bake affects significantly resulting properties of the photoresist, as could be photosensitivity and chemical resistance.

3.3.2 Mask

Two-dimensional geometric patterns are designed for each specific layer in the so-called photomask (or mask, for abbreviation). It is a nearly flat optical glass (transparent to near UV) or quartz plate (transparent to deep UV) with a metal (typically, a 800Å thick chromium layer) where the patterns are drawn using an electron beam. For obtaining any device, it could be necessary to use one or more different masks, depending on its complexity. The final device is obtained step by step transferring sequentially the patterns of each mask to the wafer level and subsequent layer processing.

In a standard fabrication process, the lithography step takes place as many times as the number of masks needed. It certainly is one of the most important steps in the fabrication, and often the number of mask levels is a direct measure of the technological complexity when different runs are compared.

As shown in fig. 3.5, polarity mask can be chosen to be light field or dark field. Obviously, depending on the photoresist type, opposite patterns will be obtained. As an example, using the mask of figure 3.5a will provide with a MZI configuration if negative resists are used and a *MZI-shaped* trench with positive resists. Thence, the choose between both polarities is based on the type of resists employed. Finally, an entire dark field mask can be observed in fig 3.5c.

Most of the technological processes require more than one mask, or even use them more than once. It is essential that there exists an alignment between the used mask and the previously patterns done at the wafer. This operation is extremely critical, since a small misalignment between them could cause the device to fail. It is done by ways of the on-wafer alignment patterns; the position and structure of which are shown in Table 3.7.

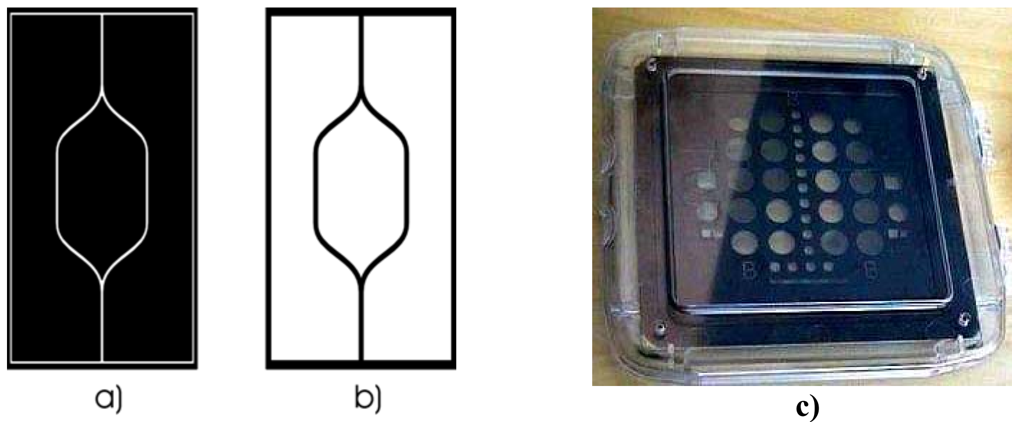
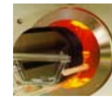


Fig. 3.5. Mask polarities for a Mach-Zehnder Interferometer a) With dark field. b) Using light field. c) Example of a dark field mask.

	Dark Field	Light Field	Light Field	Dark Field	Final Result

Table 3.7. On-wafer alignment patterns relative position on wafer and different shapes for mask polarities.

The position of these alignment patterns depends on each mask aligner. Normally, they have to be in the middle of the mask and the distance between the centers of both patterns cannot exceed a certain size. As it can be seen, in table 3.7, depending if masks are light or dark field, its pattern is the opposite. This due to the fact that, on aligning a mask over a previously patterned layer, it is expected to modify a different part of the film that is yet unaltered. Hence, mask must align consecutively



over unperturbed parts of the layer. There is no problem on using light and dark field masks on the same process, as long as the alignment patterns were done accordingly.

Another safety pattern, shown in table 3.8, is introduced on the masks, concretely on each chip, in order to verify that the alignment is correct in all wafer. Although it could also work as a pattern aligner, they are commonly used to verify that the photolithographic steps have provided with the expected result.

Negative Resist	Positive Resist	Positive resist	Negative Resist	Final Result

Table 3.8. On-chip alignment patterns for both mask polarities.

3.3.3 Exposition

Once the mask and the wafer are appropriately aligned, the exposure process can be carried out. In order to achieve a better resolution of the image, the mask can be placed in physical contact with the substrate (also known as hard contact or contact exposure). Unfortunately, this principle, however effective, causes a faster mask degradation as do non-contact, proximity masks, which are slightly above the wafer (10-20µm). This latter method enlarges the mask lifetime but reduces the resolution of the resulting pattern. Since the separation causes a shadowing effect that increases as the light incidence is less orthogonal (i.e, chips placed at the mask edges are suitable to suffer changes in its dimensions). Resolution with proximity masks is around 2µm.

Problems with this resolution arise on some integrated optics devices, as can be seen in fig. 3.6, branches in a Y-junction are underetched, delaying and rounding the expected sharp edge between waveguides as compared to mask patterns. The blunted vertex has a diameter equal to the photolithographic resolution. This undesired effect causes an increase of the losses in these devices that only can be avoided by varying the Y-junction geometries (as it will be discussed in the next section) or by using another photolithographic processes

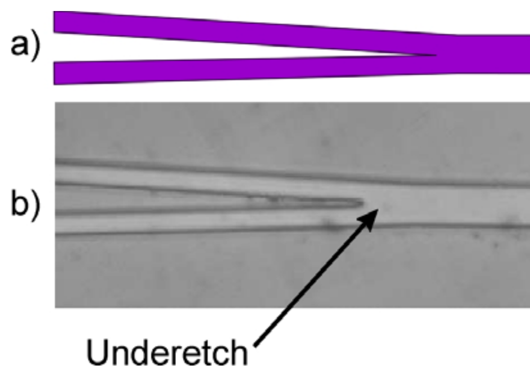


Fig. 3.6. Variation between the layout (a) and the final structure obtained (b) of a Y-junction. Rounding and delaying of the edge is observed.

There exists more sophisticated exposition techniques giving resolution below 1μm, as could be X-Ray, electron beam lithography or these based on laser reduction (resolution depends on the wavelength: the lower the wavelength, the higher the resolution is). Among these based on laser reduction, the most known are the *Steppers*. Masks used in steppers only have the patterns of a single chip (as opposite to the standard photolithographic masks, that had all the wafer chips already written) enlarged by a factor of 10. This image is reduced and projected, via a complex lens system, over the wafer surface. After the single chip irradiation, wafer is moved a given distance and new irradiation is produced. Since light is always orthogonal to the wafer and dimensions are much lower, the shadowing effects are minimized.

After development and previous to the etching process, a thermal treatment, similar to the pre-bake, is carried out to increase the etching resistance of the resist and its adhesion to the substrate. Moreover, this thermal treatment eliminates water residues coming form the developer and causes photoresist to be modified, becoming more resistant when used as a protective mask in the etching processes.