



At this point, photoresist is baked since it may have weakened during the etching process. Then, a deep silicon etching process provides with the accelerometers nearly finished, as shown in Table 5.17 and in the pictures shown in fig. 5.29. At this point, the only steps that remain are the diaphragm liberation (since it is still linked to the frame by ways of the underneath silicon oxide) and the anodic bonding to a glass wafer.

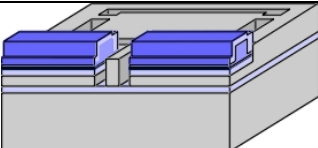
Micromechanization (front side)	
	Wafer with the accelerometer properly defined after the deep RIE Si etching (15 μ m) with SF ₆ . Only remains the liberation of the diaphragm from the underneath silicon oxide

Table 5.17: Accelerometer fabrication status after silicon micromechanization.

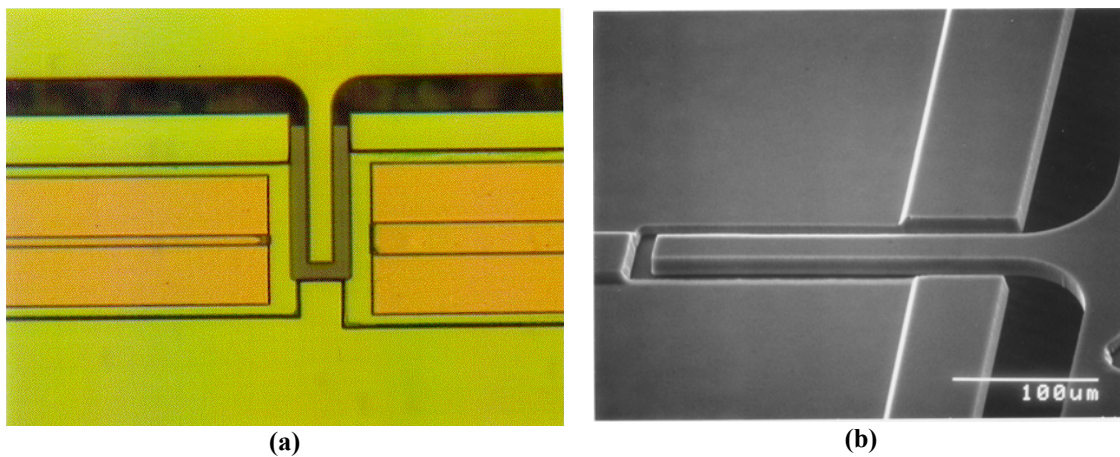


Fig. 5. 29: a) Top view of the sensing regions, where it can be seen that the diaphragm has been properly defined. b) SEM microphotograph of the same region, but in a sample without waveguides.

To etch the buried silicon oxide, HF at 49% is used. A drawback arises from the fact that waveguides have also been done with silicon oxide and if they are not protected, they will be removed during the buried SiO₂ etching. Moreover, it has to be taken into account that the silicon oxide that form the waveguides has been obtained by plasma, which has much poorer quality as compared to thermal silicon oxide. Thus, its etching speed is much faster with the same HF concentration.

The first step tried on the waveguide protection was the spinning of a thick photoresist (μ m). Although previous experimental results have shown that this resist was able to stand up to 45 minutes in HF at 49% without significant degradation (the



necessary time to liberate the diaphragm was approximately 25 minutes), after 3 minutes the photoresist lift from the wafer, causing the waveguide etching. Actually, the photoresist itself did not suffer from any damage, but due to the device morphology, the wet etching caused the photoresist removal. Another possibility that should be considered is the fact that the adherence either to silicon or to high step morphologies probably is not as good as it is for flat silicon wafers. In any case, an alternative protection should be chosen, since photoresist is unable to provide with the expected protection.

From a logical point of view, perhaps silicon nitride is the best option in order to prevent the waveguide removal, since its etching speed is much lower in HF and moreover, it has a good step coverage. With a 0.2 μm thick layer of LPCVD-deposited silicon nitride, waveguides were fastly etched during its submerging in HF. However, when a thicker (0.3 μm) Si_3N_4 was used, it seemed that the waveguides have stood the etching step. However, during the silicon nitride removal with H_3PO_4 waveguides were peeled-off. Two main factors may explain this result: Excessive mechanical stresses on the structure could lead to microfractures of the silicon nitride layer, through which HF etches the underneath waveguide. An alternative explanation would be that, although the silicon nitride is conformal, the deposition on the vertical walls is normally worse, being significantly thinner as compared to flat regions. Thus, when submerging in HF, these regions are unable to stand long etching processes. This latter assumption is confirmed by the fact that as the silicon nitride gets thicker, waveguides seem to resist better the etching process, as can be observed in fig. 5.30. Unfortunately, it is not possible to obtain thicker silicon nitride layers without suffering cracking due to mechanical stresses.

Polysilicon was also considered as a possible layer for protecting silicon oxide waveguides during the etching of buried silicon oxide. For this purpose, a 0.35 μm LPCVD polysilicon layer was deposited on the wafers and, after the photolithographic step, they were submerged in HF at different times. In fig. 5.31 it can be observed that the polysilicon step coverage is poorer as compared to silicon nitride, that causes the waveguide faces not to be properly protected. As can be seen in fig. 5.31 from a to d, as



etching time increases, waveguides are progressively etched underneath the polysilicon layer.

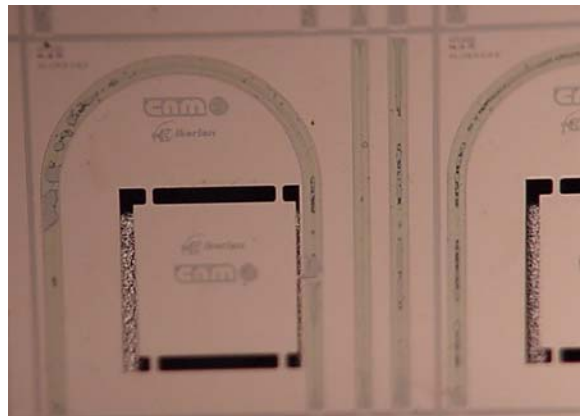


Fig. 5.30: Devices after the silicon nitride wet etching in H_3PO_4 . It can be observed that waveguides have nearly disappeared from the accelerometer.

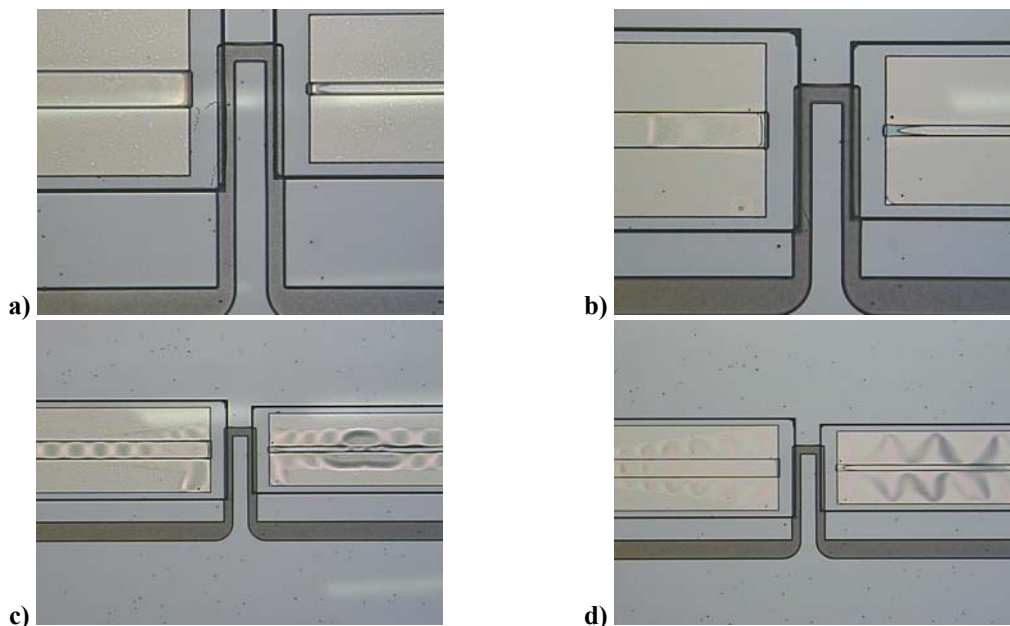


Fig. 5.31: Sensing region during the HF etching. a) As deposited, b) After 5 minutes, b) after 10 minutes, c) After 15 minutes.

Thus, all three technological steps for liberating the diaphragm failed in its purpose. According to the results obtained, and taking into account that the structure has a very high mechanical stress. Hence, what would be most appropriate for protection purposes would be a thick resist that was able to cover the high steps obtained.



Unfortunately, at the end of the project in which optical accelerometers were obtained, no such photoresist was available at IMB facilities.

5.9 Misalignment Uniaxial Optical Accelerometer

Although the results with the optical accelerometer were discouraging, the fact that misalignment accelerometer does not require etching of the buried silicon oxide layer is its main advantage. Fabrication process did not start with etching the wafer surface, as it happened with the previous accelerometer, since in this design waveguides are headed at 0g. The standard ARROW-A layers are grown in the front surface. As it was done with the previous design, the 2µm SiO₂ on the back side has been removed and replaced by a 0.1µm silicon oxide and a Boron implantation is done at the LPCVD silicon nitride located at the back side of the wafer so as to minimize mechanical stress. As shown in table 5.18, after these steps core waveguides are 3.5µm etched RIE and a 2µm PECVD silicon oxide passivation layer was deposited.

<p>ARROW-A waveguides & Unnecessary layer removal</p>	<p>BESOI substrate. Double-side polished, 4" diameter, 450µm thick. 2µm buried SiO₂. 15µm upper silicon layer 2nd cladding: 2µm wet thermal silicon dioxide. n=1.46 Removed from back by wet etching. 0.1µm re-growth 1st cladding: 0.38µm LPCVD silicon nitride. n=2.00 Boron implantation at the back Core: 4µm PECVD silicon oxide. n=1.48</p>		
	<p>CNM-135 M2: Rib Definition</p> <table border="1" data-bbox="644 1491 1377 1727"> <tr> <td data-bbox="644 1491 874 1704"> </td> <td data-bbox="874 1491 1377 1727"> <p>Mask: Width: 14/30/50µm Distance: 24µm</p> <p>Steps: Positive photoresist 2µm thick 3.5µm SiO₂ RIE etching with CHF₃</p> </td> </tr> </table>		<p>Mask: Width: 14/30/50µm Distance: 24µm</p> <p>Steps: Positive photoresist 2µm thick 3.5µm SiO₂ RIE etching with CHF₃</p>
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	<p>Passivation: 2µm PECVD silicon oxide. n=1.46</p>		



	CNM-135 M3: Stress-free regions	
		<p>Mask: Width: 250μm Distance: 120μm</p> <p>Step: 2μm sputtered aluminium 2μm positive photoresist</p>

Table 5.18: Technological steps that allows obtaining ARROW-A segmented structure for misalignment accelerometers.

Identically as the previous accelerometer, the micromechanical structure has been defined in two steps (table 5.19): firstly, an anisotropic etch by the back side has provided with the three-dimensional structure. Secondly, an RIE etching by the front side has liberated the seismic mass from the buried silicon oxide. Differences with the latter accelerometer appear at this point. Since there is no diaphragm to be protected, either silicon and buried silicon oxide layers can be etched by RIE, without affecting the waveguides.

Micromechanization	
	<p style="text-align: center;">CNM-135 M4: Stress-free regions</p> <p>Mask: Square 4015x4015μm “T” convex corner compensation. 1200μm</p> <p>Steps: Positive photoresist 2μm thick RIE Si₃N₄ etching with SF₆+He RIE SiO₂ etching with CHF₃</p>
	Wafer after the etching the protection layers at the back side
	Wafer after the anisotropic silicon etching
	0.3 μ m LPCVD silicon nitride deposition for protection



	<p>CNM-135 M2: Accelerometer front side</p>
	<p>Mask: As defined in chapter 4</p>
	<p>Steps: Thick positive photoresist (6μm) RIE Si₃N₄ etching with SF₆+He Deep RIE Si etching (15μm) with SF₆ RIE SiO₂ etching with CHF₃ Wet Si₃N₄ etching in H₃PO₄</p>
	<p>Wafer status after RIE etching by the front side</p>

Table 5.19: Anisotropic technological steps for defining the accelerometer seismic mass.

The appearance of the wafer and the accelerometers after the previously explained technological steps can be seen in fig. 5.32. As can be observed, it is not a single waveguide on top of the seismic mass, but there are three of them. This configuration was designed to be biaxial optical accelerometer. As explained in [8], two different output signals could be obtained from all three waveguides: If z -acceleration is produced, all three waveguides on the seismic mass will be misaligned with those of the frame. On the contrary, if the acceleration is in the y axis, although the lateral waveguides suffer from misalignment, the waveguide placed at the middle of the seismic mass does not suffer from significant changes, since the mass has a null movement at that point. Unfortunately, overetching on the convex corners of the seismic mass caused the edges to bend, being impossible to couple light between the lateral waveguides. Nevertheless, using only the central waveguide, uniaxial optical accelerometers were obtained.

Although the accelerometer fabrication could be considered as finished at this point, the devices are extremely fragile and easily crack. For this reason a wafer glass (Pyrex #7740) is bonded on the backside of the silicon wafer. However, to permit the free mass movement, previous glass mechanization has to be done. The most important steps are shown in table 5.20. For glass etching, a silicon mask is generally used. Firstly, in a silicon oxide wafer a 2 μ m thermal oxide is grown, in which the windows where the mass should be located are opened by wet etching (HF at 49%). Then, wafers



are firstly etched with TMAH by the side of the window. When etching height has reached half of the wafer thickness, setup is changed so as to allow etching by both sides of the wafer. Then, although thinner silicon wafers are obtained, the patterns at the back side of the silicon wafer have closer dimensions as compared to these of the layout. By anodic bonding, silicon wafer is bonded to a glass wafer and this latter is etched, though the holes opened in the silicon wafer, using HF at 49%. Once the expected step in glass has been obtained, silicon mask is completely etched using TMAH. Finally, the accelerometer wafer is anodically bonded to the micromechanized glass wafer.

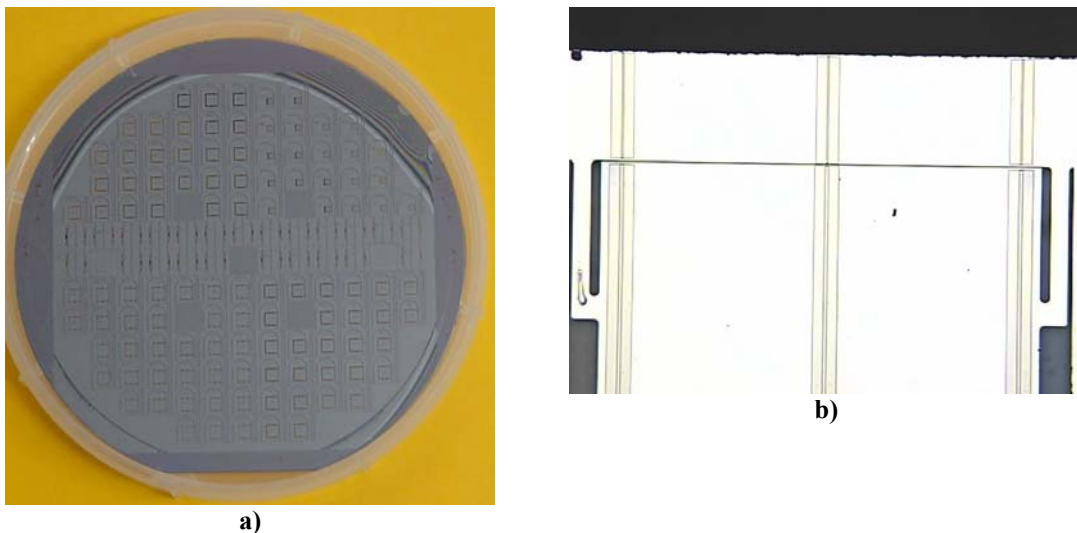


Fig. 5.32: a) BESOI Wafer with uniaxial optical accelerometers after the clean room technological steps. b) Detailed picture of half misalignment accelerometer, where it can be observed the three waveguides in the seismic mass, and two beams anchored to the frame, where the input waveguides are located. Output waveguides are placed on the other side of the seismic mass (not shown in this picture).

Before testing the devices, each accelerometer must be separated from the rest of the wafer (table 5.21). This is achieved using a diamond blade with a water stream, which could cause mechanical parts to be broken if the stream hits directly to the accelerometer. For that reason, the accelerometers have been protected with a highly diluted photoresist layer. After cutting the wafers, the edges have a high roughness and polishing is required in order to minimize insertion losses. Due to the glass wafer, polishing became extremely large and difficult, however possible. Generally, this process requires a first pre-polishing with SIC, that provides with a roughness of about



0.9 μm and then a Al_2O_3 fine polishing enables to reduce the roughness to below the working wavelength.

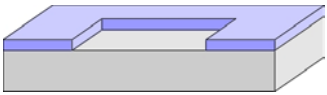



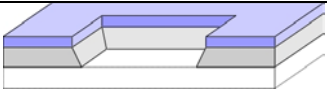
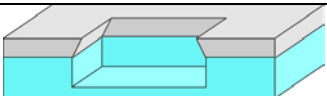
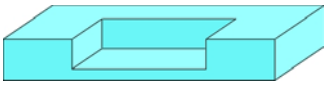
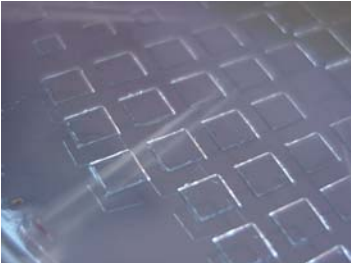
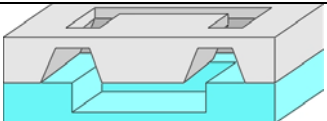
Glass Micromechanization			
	CNM-135 M2: Opening of the windows in glass		
	<table border="1"> <tr> <td></td> <td> Mask: 120% of the seismic mass dimensions Steps: 2μm thermal oxide growth SiO₂ etching with HF in the back side 2μm positive photoresist </td> </tr> </table>		Mask: 120% of the seismic mass dimensions Steps: 2 μm thermal oxide growth SiO ₂ etching with HF in the back side 2 μm positive photoresist
	Mask: 120% of the seismic mass dimensions Steps: 2 μm thermal oxide growth SiO ₂ etching with HF in the back side 2 μm positive photoresist		
	Two-step TMAH silicon etching : Only through the window until half wafer thickness By both sides until having the hole with the expected dimensions		
	Anodic bonding of the silicon mask previously done with a glass mask Etching with HF 49% of the glass wafer through the holes		
	Removal of the Si mask with TMAH		
			
	Anodic bonding of the accelerometers wafer with the micromechanized glass wafer		

Table 5.20: Glass wafer mechanization by anodic bonding and silicon mask.

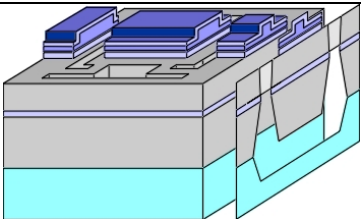
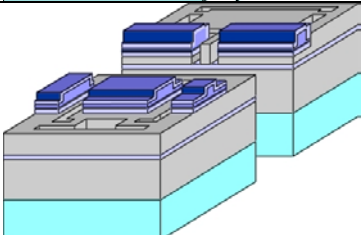
Post process:	
	Situation of the wafer after glass anodic bonding
	Cutting by a diamond blade Polishing with SIC (0.9 μm) + Al_2O_3 (0.3 μm)

Table 5.21: Cutting and polishing of the accelerometers.