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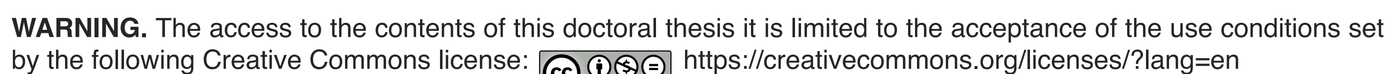
WARNING. The access to the contents of this doctoral thesis it is limited to the acceptance of the use conditions set by the following Creative Commons license:  https://creativecommons.org/licenses/?lang=en

Focused ion beam implantation as a tool for the fabrication of nano electromechanical devices

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Universitat Autònoma de Barcelona (UAB) 2016

Focused ion beam implantation as a tool for the fabrication of nano electromechanical devices

Memoria presentada per optar al títol de
Doctor en Ciència de Materials
Departament de Física de la
Universitat Autònoma de Barcelona

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Memòria presentada per aspirar al Grau de Doctor per Jordi Llobet Sixto.
Vist i plau dels Directors Dr. Francesc Pérez Murano, Dr. Xavier Borrisé Nogué, i tutor Dr. Jordi Sort Viñas.

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Bellaterra, 26 de gener de 2016

Moltes Gràcies!
Thank you!

En primer lloc voldria agrair el suport, ajuda i direcció al Prof. Francesc Pérez-Murano i al Dr. Xavier Borrisé Nogué. A en Xevi voldria agrair-li la confiança que sempre m'ha mostrat des de que es va decidir crear l'àrea de Nanolitografia de la Sala Blanca del IMB-CNM allà l'any 2006. Amb ell sempre he treballat molt a gust i sempre he pogut comptar amb el seu suport quan s'han presentat dificultats o reptes, i sota la seva direcció vaig poder realitzar el PFC d'Enginyeria de Materials (2007) i el treball de Màster de Nanotecnologia (2011). Amb en Francesc i el seu grup també m'he trobat molt a gust i en un gran ambient de treball on he pogut aprendre moltes coses. També voldria agrair-li al Francesc el fet d' "acollir-me" al 2013 per poder realitzar aquesta tesis que tenia tantes ganes de fer. Han sigut uns anys molt bonics i estimulants.

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Guardo un especial record i "good vibes" de tota la gent del grup NanoNEMS, tan els que ara hi sou i els que ja han aixecat el vol. Tots vosaltres heu estat uns companys magnífics. Un plaer haver compartit vivències (i també experiments) amb la Laura Evangelio, la Marta Fernández, l'Ana Conde, en Joan Bausells, en Matteo Lorenzoni, l'Albert Alcacer, l'Angelos Streklas, l'Steven Gottlieb; així com també ho va ser amb l'Álvaro San Paulo, la Nerea Alayo, la Lorea Oria, la Irene Fernández, l'Iñigo Martín, l'Yigezu Mulugeta, en Giordano Tosolini, en Nil Fontanals, la Sophie Verhaeghe, l'Alex Chuquitarqui i en Dani Ruso.

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De vital importància és el fet de menjar. I si a sobre pots fer-ho en un ambient distès i de bon rollo encara millor. Agraeixo molt les converses que hem tingut, i també el saber escoltar, de la Marta Duch, la Núria Torras, l'Alberto Moreno, en Carlos Seisdedos, en Xavi Mas, la Nuria Torres, la Neus Sabaté, en Juan Pablo Agusil i l'Ana Sánchez.

Ha estat un plaer haver compartit tot aquest temps amb els companys de sala blanca. No vull oblidar-me de ningú! Tota la gent involucrada a les etapes, processos, manteniment,... tot el que feu te una gran complexitat tècnica i permet que els projectes avancin. He tingut la sort d'interactuar més a prop durant aquest temps amb la Marta Gerbolés, la Marta Duch, la Libertad Solé, l'Ana Sánchez, l'Alberto Moreno, la María Sánchez, en Jose Calvo, en Josep Montserrat, en Miquel Zabala, la Oihane Beldarrain, la Roser Mas, en Carles Mateu, en Josep Mª Cirera, en Javi Sánchez, en Sergi Sánchez, en Josep Tarradas, en Xavi Mas, en Roger Cot, en Roger Llopis, en José Rus, en José Arias, l'Antonio García Simon, en Joan Cussó, l'Antonio Garzón, l'Antonio Sáenz, en David Muñoz, en Marcos Lechón, la Isabel Montero, la Nieves Alonso, la Carme Girbello, la Julia Pérez,... Moltes gràcies a tots!

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de moment ;) Als meus pares Jordi i Paloma, al meu germà Albert, als meus avis, tiets, cosins, família política i als amics. A tots ells, als que hi son, als que son lluny i als que ja han marxat. Moltes gràcies per tot.

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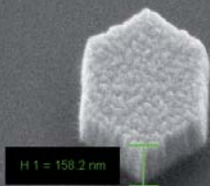
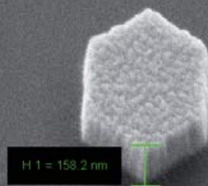
Júlia, que vols que et llegeixi un conte? Aquest va de nanotecnologia.





RESUM

La tesi doctoral titulada “Focused ion beam implantation as a tool for the fabrication of nano electromechanical devices” aborda el repte de la fabricació de ressonadors nano-mètrics des d’una nova òptica basada en la implantació iònica mitjançant un feix de ions focalitzat (FIB). Aquest nou mètode permet fabricar nano-dispositius suspesos funcionals, des del punt de vista elèctric i mecànic, sense necessitat d’utilitzar resina d’una forma i) ràpida i simple, només son necessàries tres etapes de fabricació; ii) flexible, permet definir dispositius amb gran llibertat geomètrica; iii) alta resolució, es demostra la fabricació de dispositius suspesos de 4 μm de longitud per 10 nm de diàmetre; iv) reproduïble i v) compatible amb la tecnologia CMOS.

Partint d’un xip de silici o SOI (silici - diòxid de silici - silici), el mètode de fabricació comença amb un procés d’implantació FIB on es defineixen les estructures i les connexions elèctriques del dispositiu. El segon pas consisteix en el gravat humit del silici, on s’ataca el silici que no està protegit per la implantació FIB, permetent la suspensió o alliberació dels dispositius. En aquest estadi, on les estructures ja estan definides, el silici és amorf, conté gal·li i no és elèctricament funcional (ρ ~1 Ω·m). El darrer pas consisteix en un tractament tèrmic a alta temperatura fins a 1000ºC, en ambient de nitrogen i amb un precursor sòlid de bor on es propicia la recristal·lització del silici formant nano-cristalls, dopar el silici amb bor (tipus p) i eliminar el gal·li. Aquest tractament a alta temperatura, on les estructures no son oxidades, permet obtenir dispositius elèctricament funcionals (ρ ~10^{-4} Ω·m).

Els principals resultats obtinguts es poden classificar en tres àmbits:

- **Investigació de l’efecte de la implantació amb ions gal·li en el silici**, pel que fa tant a aspectes de processament com de propietats nanoelectromecàniques del material.

En aquest treball hem caracteritzat l'estructura del material en les diferents etapes de fabricació i hem caracteritzat elèctrica i electromecànicament els dispositius finals obtinguts pel mètode descrit.

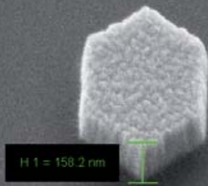
- **Desenvolupament i optimització del procés de fabricació**, especialment pel que respecte al control de dimensions i a la combinació amb altres processos

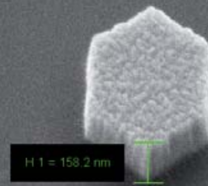
  Es mostra el treball realitzat en la optimització dels diferents paràmetres de fabricació, des de la posta a punt de la dosi d'ions fins a la selectivitat del gravat. A través del disseny de les estructures es pot establir estratègies per controlar i minimitzar els efectes d'"under-etching" en el silici, a través de la definició d'estructures de compensació, i també evitar el col·lapse de les estructures més llargues, degut a les tensions superficials que es produeixen durant els processos de gravat humit, fabricant pilars per sostenir les estructures.

  Aquest mètode de fabricació permet obtenir dispositius a mida convertint-lo en una eina versàtil de prototipatge i de fabricació petites quantitats, que permet aconseguir dispositius de dimensions nano-mètriques per a l'experimentació acadèmica i científica.

- **Investigació de les propietats electròniques, mecàniques i electromecàniques dels dispositius**, i concretament en el cas de nanofils de silici suspesos que es poden aplicar com a ressonadors mecànics d'altra freqüència o transistors d'un sol forat.

  Hem pogut fabricar ressonadors de diferents geometries que ens ha permès estudiar i demostrar la relació que existeix entre la simetria/asimetria dels dispositius i el senyal piezoresistiu mesurat durant la transducció electromecànica. Hem investigat i fabricat transistors d'efecte camp ultra-fins (10 ~ 15 nm) i transistors suspesos on les característiques elèctriques a baixa temperatura mostren efectes de "Coulomb blockade" gracies als nano-cristalls que es formen, dins dels nano-fils de silici suspesos, durant l'etapa de tractament tèrmic.





SUMMARY

The thesis entitled “Focused ion beam implantation as a tool for the fabrication of nano electromechanical devices” aboard the challenge of the fabrication of nanometric resonators from a new approach based on ion implantation by a focused ion beam (FIB) . This new method allows the fabrication of functional suspended nanodevices, from the electrical and mechanical point of view, without using any resist. This method is i) fast and simple, where only three steps are needed; ii) flexible, it is feasible the definition of structures of different shape; iii) high resolution, it is demonstrated the fabrication of 4 μm length and 10 nm diameter suspended devices; iv) reproducible and v) CMOS compatible.

The starting point is a silicon or SOI (silicon – silicon dioxide – silicon) chip. The fabrication approach starts with a FIB implantation process where the structures and the electrical connections of the device are defined. The second step consists on silicon wet etching, where silicon that is not protected by the FIB implantation is etched, allowing the release of the devices. The defined structures are made of amorphous silicon, they contains gallium and they are not functional electrically (ρ ~1 $\Omega \cdot$m). The last step consists on diffusive boron doping at high temperature (up to 1000ºC) in a boron environment, where it is promoted the recrystallization of silicon forming nanocrystals, the boron doping (p type) of silicon and the removal of gallium. In this last step at high temperature the structures are not oxidized obtaining electrically functional devices (ρ ~10^{-4} $\Omega \cdot$m).

The principal results can be classified in three areas:

- **Investigation of the effect of gallium ion implantation onto silicon** from the process and nanoelectromechanical material properties point of view.

  In this work the material structure in the different fabrication steps has been characterized, as well as the electrical and electromechanical properties of the final devices obtained by the described method.

- **Development and optimization of the fabrication process**, especially controlling the dimensions and the combination with other fabrication processes.

  The work done in the optimization of the different fabrication parameters are shown, from the tuning of the ion dosage to the etching selectivity. It is possible to stablish design strategies to control and minimize the under-etching effects onto silicon, as well as to avoid the collapse of long structures, that are the result of the superficial sticking produced during the wet etching processes, by the fabrication of sustaining posts.

  That method permits to obtain customized devices. It is a versatile prototyping method that allows the fabrication of small batches of devices of nanometric dimensions that can be employed for the scientific and academic experimentation.

- **Investigation of the electronical, mechanical and electromechanical properties of the devices**, specifically suspended silicon nanowires that can be employed as high frequency mechanical resonators or single hole transistors.

  We fabricated resonators of different geometries for the study and demonstration of the relation between the geometrical symmetry/asymmetry of the devices and the piezoresistive signal measured during the electromechanical transduction. We investigated and fabricated ultra-thin field effect transistors (10 ~ 15 nm) and suspended transistors that exhibits Coulomb blockade electrical characteristics at low temperature thanks to the nanocrystals that are grown during the high temperature fabrication step.

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Thesis Presentation

1.1 Framework of the thesis

*The thesis entitled **"Focused ion beam implantation as a tool for the fabrication of nano electromechanical devices"** has been realized in the NanoNEMS group of the Institut de Microelectrònica de Barcelona – Centre Nacional de Microelectrònica (IMB – CNM), that belongs to Consejo Superior de Investigaciones Científicas (CSIC), and it is located in the UAB campus (Universitat Autònoma de Barcelona). This thesis has been supervised by Prof. Francesc Pérez-Murano and Dr. Xavier Borrisé Nogué.*

I started towards research in July 2006. At that time my activities were oriented to the development and applicability of technological solutions in a research environment by the use of a Focused Ion Beam (FIB) work station Crossbeam (1560 XB, Zeiss) with some at demand add-ons that are described in chapter 2. As it is explained in more detail in this thesis, the Crossbeam can be understood as a nano-laboratory and it allows to develop oriented solutions for a wide range of investigation requirements. It was acquired by the ICN to support the nanofabrication activities of the research groups of the UAB campus and it was located in the Cleanroom of the IMB-CNM that has been enlarged to update the nanofabrication capabilities.

During that period, I worked as FIB engineer and my activity was oriented to the technological service in order to find and execute specific solutions for different research and technological activities. We worked for different research and technological institutions, public and private, national and international. Some of the services were performed in the framework of the GICSERV program that was founded directly by the Spanish Government through the Ministry in charge of the research activities at those moments. Furthermore, I have been involved in several teaching actions, called "autoservicio cualificado", oriented to train researchers to the use of the Scanning Electron Microscopy (SEM) and the FIB by their own. All these activities have been integrated in the Nanolithography area of the ICTS Clean Room by the management of Dr. Xavier Borrisé, head of the area.

Also during this first phase of my career, I was involved in some research projects. In the context of the Charged Particle Nanotech (CHARPAN) FP6 EU project I had the opportunity to collaborate with Dr. Gemma Rius, Dr. Xavier Borrisé and Prof. Francesc Pérez-Murano. The objective of the CHARPAN project was the development of a new nanofabrication tool based on multiple ion beams. The project was focused on the industrial needs to find new technological approaches for the fabrication of nanometric two and three dimensional devices. The participation of our group was focused in the viability to integrate the FIB technology for the fabrication of NEMS combined with a transistor fabricated by CMOS technology. We developed some new FIB related approaches with the objective of increasing the fabrication throughput of this technology for CMOS-compatible[1] nanostructures. We explore the possibility to pattern a mask for a subsequent silicon etching[2,3] with (i) FIB induced deposition of SiO_2, (ii) FIB milling of a thin layer of aluminum placed on top of a silicon chip, (iii) FIB implantation performed directly on top of a silicon substrate. Figure 1 shows four SEM pictures at different angles of silicon membranes fabricated by FIB implantation and Reactive Ion Etching (RIE). All these results have been presented in[1–3] and they can be considered as the starting point for the present thesis.

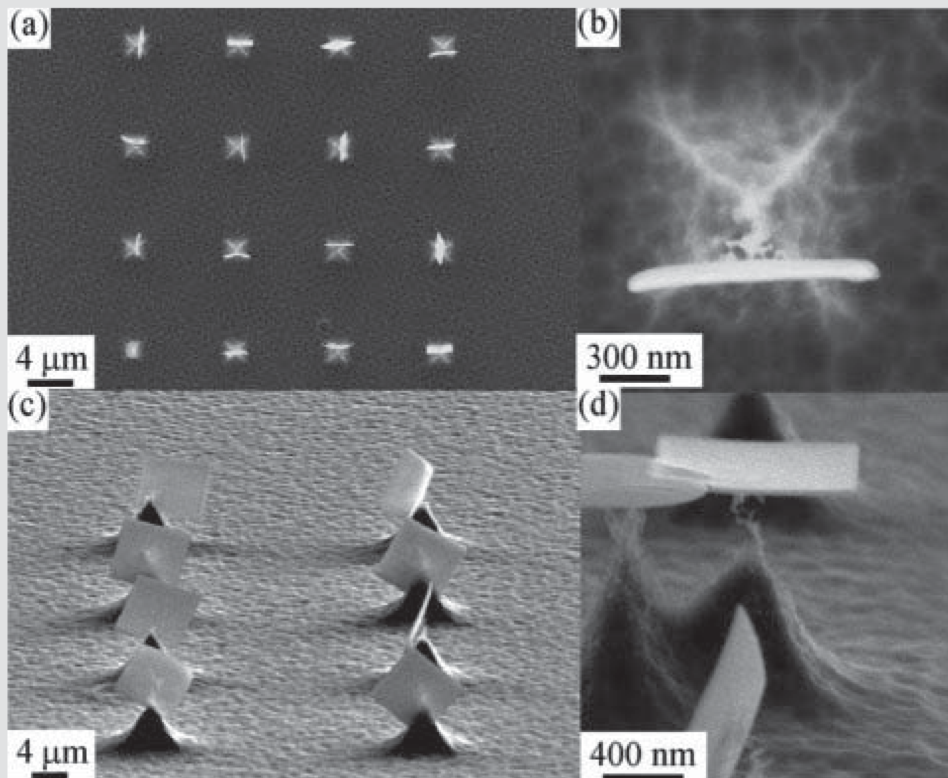

Figure 1. [(a) and (b)] Top-view and [(c) and (d)] tilted view SEM images with nanostructures made of silicon after local FIB exposure of squared areas. The RIE was carried out under conditions to obtain an isotropic etching.[2]

Since Januray 2013 I am working in the NanoNEMS group. The NanoNEMS group is involved on research projects about Nanofabrication and NEMS. The general objective is research on electronic and electromechanical properties of nanostructures, with potential to provide new or enhanced functions to nanodevices and nanosystems, as well as advanced methods for nanofabrication. During the last years, the NanoNEMS group has implemented some experimental setups based on the electrostatic actuation of suspended silicon nanowires.

From the beginning of 2013 until now, the Single Nanometer Manufacturing for beyond CMOS devices (SNM) FP7 EU project is giving us the opportunity to go further in the investigation of novel nanofabrication methods applied to nanoelectronic devices, including the study of the piezoresistive transduction mechanism.[4] The contributions that conform this thesis [5–8] correspond to the work performed in the design and fabrication of nanometric devices obtained by this innovative approach, the characterization of the material and the devices produced by this method, the electrical and electromechanical measurements and the discussion of the obtained results.

Much of the work presented here has been performed in the Clean Room facilities of the IMB-CNM (CSIC). The IMB-CNM Clean Room is a large scale open access facility devoted to innovative technologies, with special attention to the integration of microelectronics together with nanotechnologies. To work in this environment gives the opportunity to use a large number of different equipments and technologies. Among the available equipments, the following technologies can be found: FIB, EBL (Electron Beam Lithography), NIL (Nano Imprint Lithography), AFM (Atomic Force Microscopy), SEM, Optical Lithography (laser, Aligner and stepper), ICP-RIE (Inductively Coupled Plasma – Reactive Ion Etching), Sputtering and Thermal Evaporation, CVD (Chemical Vapor Deposition), furnaces and RTA (Rapid Thermal Processing), Ion Implantation, ALD (Atomic Layer Deposition) and areas designed to work with chemical products as wet etching (anisotropic or isotropic), lift-off and cleaning processes. All these technologies are necessary for the nano-metric development of devices and materials.

For the realization of this thesis the author employed some of the equipment installed in the Clean Room as well as other tools that are located in other laboratories. In the following paragraphs there are described some of them.

As it has been mentioned, the Crossbeam equipment could be understood as a laboratory to fabricate, characterize and interact with matter at the nanoscale. Figure 2 is a photography of the Crossbeam located in the Nanolithography area of the Clean Room of the IMB-CNM (CSIC). The labeled photography demonstrates that the Crossbeam can be used as a tool for electrical characterization thanks to their connectivity with other elements. Apart of the

FIB column it could be observed:

- A SEM column (Gemini, Zeiss) that is mounted in the CrossBeam platform. The SEM could be used for inspection, for real time imaging during the ion processing or electrical characterization, for EBID (Electron Beam Induced Deposition) or for EBL.
- A pattern generator extension (Elphy Quantum, Raith) that permits to design patterns, to control the ion or the electron exposure and the blind navigation through the different patterns of the sample.
- Controllers of the three nanomanipulators (Klendiek) installed inside the vacuum chamber. They are commonly used to contact electrically samples or devices or to manipulate them.
- A semiconductor analyzer (Agilent B1500A) that is connected to the manipulators by a feedthrough. It permits to measure the electrical performance of the fabricated devices.

Figure 2. Photography of the Crossbeam used for the fabrication and characterization of the devices presented in this thesis. In the photography it is also observed some attachments connected to the Crossbeam, as the Elphy Quantum lithographic capabilities (Raith), three manipulators (Kleindiek) and a semiconductor analyzer (Agilent).

Besides the Crossbeam, for the fabrication of the devices there are needed additional technologies. The etching of the devices is performed in the Microsystems laboratory located in the Clean Room. In collaboration with the engineer Marta Gerbolés the structures are released by wet etching. Figure 3 corresponds to the photography of the chemical bench employed to release the devices presented in this thesis. More details of

the anisotropic wet etching are included in chapter 3.

Figure 3. Photography of the chemical bench located in the Microsystems area of the ICTS Clean Room where the wet etching processes have been performed.

For the recrystallization and doping of the devices it is used a CVD furnace (figure 4). In that equipment it is performed a high temperature annealing process in a boron environment. In chapter 3 it are included the details and working conditions used where the fabricated devices are (i) doped with boron, (ii) interstitial gallium atoms are removed from the fabricated structures, (iii) silicon dioxide is not grown and (iv) it is promoted the nanocrystalline arrangement of amorphous silicon. All these effects contribute to enhance the electrical conductivity of the fabricated devices.

Figure 4. Photography of the CVD furnace (located in the Furnace area of the ICTS Clean Room) used to perform the high temperature diffusive boron doping of the devices.

The experimental setups employed in this thesis, based on electrostatic actuation of the suspended devices and the piezoresistive detection of the movement, have been implemented in our group. Dr. Marc Sansa and Dr. Álvaro San Paulo developed and implemented these setups for the electro-mechanical characterization of silicon nanowires grown by a bottom-up approach [Sansa, M. et al. *Appl. Phys. Lett.* 101, 243115 (2012)].

The measurement of the electromechanical response of the fabricated devices has been performed in the Microsystems laboratory located outside the Clean Room. The electrical setup used for the electromechanical characterization of the devices is presented in figure 5. There are employed (i) two Analog Signal Generators, the E8257D PSG (Agilent) and the N5181A MXG (Agilent), (ii) a DC source (E3631A, Agilent), (iii) a lock-in amplifier (7280 DSP, Signal Recovery), (iv) a computer to control all the instrumentation by General-Purpose Instrumentation Bus (GPIB, Texas Instruments) and (v) RF circuitry composed by the following types of elements: bias-tee, frequency doubler and frequency mixer (Mini-circuits). Inside the vacuum chamber there is the device wire-bonded to a PCB and connected to the measurement setup through the vacuum feedthroughs. The electrical setup presented for the electromechanical measurements has also been connected successfully to the Crossbeam vacuum chamber.

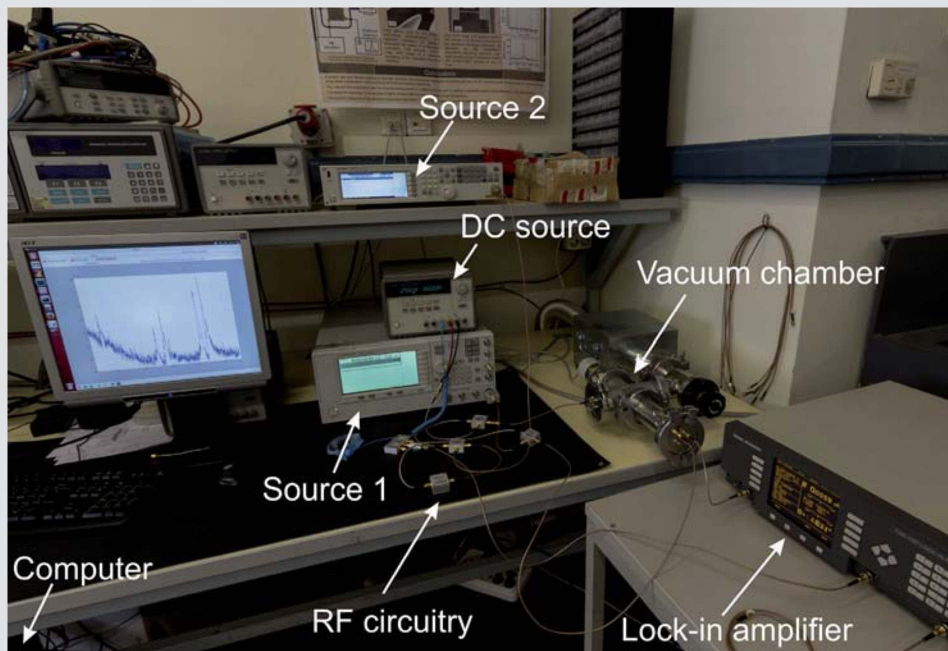

Figure 5. Photography of the setup used to characterize mechanically the devices by electrical methods. The setup is composed by 2 RF sources (Agilent), a DC source (Agilent), RF circuitry (Mini-circuits), a homemade vacuum chamber, a Lock-in amplifier (Signal Recovery) and a computer.

1.2 Objectives

When this thesis was proposed, it was decided to focus into two main goals, i) the fabrication of nanomechanical resonators by FIB implantation approach and ii) the investigation of their nanoelectromechanical properties. On the one hand, we were looking for a fast prototyping method capable to produce electrically functional suspended devices. We consider the possibility to work on the development and optimization of a new fabrication method based on FIB implantation according to our preliminary results on this process[1–3]. The characterization of the material at the different stages of the fabrication, as well as the characterization of the devices, becomes crucial pieces in order to understand the final behavior of the fabricated structures. In order to create the desired device it is important to control and optimize the design of the implanted patterns and all the etching parameters involved in the structure release.

On the other hand, once the fabrication method is stablished, the goal is to use it to design and produce on purpose devices. As this technique permits to obtain small suspended devices, it is interesting to investigate the fabrication and the performance of the devices. From the mechanical point of view we took advantage of the geometrical flexibility and simplicity of this technique to investigate the relationship between designed geometrical asymmetries on the electrical transduction signal. In addition, we have reported for the first time the operation of suspended Single Hole Transistors (SHoTs).

1.3 Thesis Outline

This thesis is organized in six chapters. Chapter 1 is an introduction to the fields of nanotechnology and nanofabrication. There are exposed some of the most used approaches to reach a nanometric device.

Chapter 2 is dedicated to FIB (Focused Ion Beam) technology. It is an overview of the principal phenomena that occurs when a FIB is used. As a result of the interactions of ions and electrons with matter a large number of applications emerge. In this chapter there are shown some of these applications that are useful for different disciplines of Science and Engineering. All the application examples have been performed by the author of this thesis.

In chapter 3 it is shown the fabrication of suspended silicon nanometric devices based on FIB that presents some advantages and singularities with respect other fabrication

approaches. It is presented the results of the material characterization at the different stages of the device fabrication and the electrical and electromechanical characterization of the final devices obtained by this method. This chapter compiles the activity on fabrication and design optimization. It shows the fine tuning of the ion dose and the etching selectivity. Moreover, there are presented design strategies to control the under-etching and to prevent the sticking of the structures during their release.

Because of the geometrical flexibility and fast prototyping capability, the approach presented in chapter 3 is very useful to obtain nanodevices for research. We use this technique to demonstrate the relationship between the shape of devices (chapter 4) and their mechanical transduction. In chapter 4 it is also explained the experimental setup used, the results obtained and the interpretation of those results. For this study we payed attention to the resonant transduction signals and how the signal amplitude can be tuned by changing the device geometry.

Chapter 5 is dedicated to the fabrication and the characterization of transistors and single hole transistors (SHoTs). The chapter starts with a brief introduction on single electron transistors (SETs), the experimental setup used and an explanation of why we can produce SHoTs by the fabrication approach presented in chapter 3. Then, there is a description of the I-V curves measured, the interpretation of the results and the extracted model.

Finally, chapter 6 remarks the conclusions of the overall thesis. It is recapitulated the principal advances from the fabrication point of view, the material and device characterization, the principal applications that we explore and the future work that could be followed in this field.

1.4 Publication list

Next it is listed the publications in which the author of this thesis is co-author. The first three works[1–3] has been developed during the Charpan EU project and they are the seed of this thesis. In addition, our previous work[4] that demonstrates the influence of the asymmetries on suspended NW on the piezoresistive transduction is an important pillar for this thesis. Then, the following four contributions are the heart of the thesis, in which it is described the fabrication[5] process, the optimization[6] of the devices, the electromechanical results[7] and realization and characterization of single hole transistors.[8]

As mentioned, there are other works performed during these years in which I have participated. On that point I list the contributions to those works in which I am co-author. My participation to those works could be classified as: (i) material and device characterization

by FIB cross section or the lamellae preparation,[9–17] (ii) mass sensing experiments performed by FIBID[18] and FEBID,[18,19] (iii) fabrication of devices and structures by FIB.[20–24]

Previous works that are the background and context of this thesis:

1. Rius, G., **Llobet, J.**, Arcamone, J., Borrisé, X. & Pérez-Murano, F. Electron- and ion-beam lithography for the fabrication of nanomechanical devices integrated on CMOS circuits. *Microelectron. Eng.* **86,** 1046–1049 (2009).
2. Rius, G., **Llobet, J.**, Borrisé, X., Mestres, N., Retolaza, A., Merino, S. & Perez-Murano, F. Fabrication of complementary metal-oxide-semiconductor integrated nanomechanical devices by ion beam patterning. *J. Vac. Sci. Technol. B Microelectron. Nanometer Struct.* **27,** 2691 (2009).
3. Rius, G., **Llobet, J.**, Borrisé, X. & Pérez-Murano, F. Fabrication Of Nanomechanical Devices Integrated In CMOS Circuits By Ion Beam Exposure Of Silicon. *AIP Conf. Proc.* **1336,** 239–242 (2011).
4. Sansa, M., Fernández-Regúlez, M., **Llobet, J.**, San Paulo, Á. & Pérez-Murano, F. High-sensitivity linear piezoresistive transduction for nanomechanical beam resonators. *Nat. Commun.* **5,** (2014).

Works that are the bases of this thesis:

5. **Llobet, J.**, Sansa, M., Gerbolés, M., Mestres, N., Arbiol, J., Borrisé, X. & Pérez-Murano, F. Enabling electromechanical transduction in silicon nanowire mechanical resonators fabricated by focused ion beam implantation. *Nanotechnology* **25,** 135302 (2014).
6. **Llobet, J.**, Gerbolés, M., Sansa, M., Bausells, J., Borrisé, X. & Pérez-Murano, F. Fabrication of functional electromechanical nanowire resonators by focused ion beam implantation. *J MicroNanolith MEMS MOEMS* **14,** 031207 (2015).
7. **Llobet, J.**, Sansa, M., Lorenzoni, M., Borrisé, X., San Paulo, A. & Pérez-Murano, F. Tuning piezoresistive transduction in nanomechanical resonators by geometrical asymmetries. *Appl. Phys. Lett.* **107,** 073104 (2015).
8. **Llobet, J.**, Krali, E., Wang, C., Arbiol, J., Jones, M. E., Pérez-Murano, F. & Durrani, Z. A. K. Resonant tunnelling features in a suspended silicon nanowire single-hole transistor. *Appl. Phys. Lett.* **107,** 223501 (2015).

Other works in those the author of this thesis has participated:

9. Pérez-Tomás, A., Lodzinski, M., Guy, O. J., Jennings, M. R., Placidi, M., **Llobet, J.**, Gammon, P. M., Davis, M. C., Covington, J. A., Burrows, S. E. & Mawby, P. A. Si/SiC bonded wafer: A route to carbon free SiO[sub 2] on SiC. *Appl. Phys. Lett.* **94,** 103510 (2009).
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A. Integration of HfO[sub 2] on Si/SiC heterojunctions for the gate architecture of SiC power devices. *Appl. Phys. Lett.* **97,** 013506 (2010).

11. Fontserè, A., Pérez-Tomás, A., Placidi, M., **Llobet, J.**, Baron, N., Chenot, S., Cordier, Y., Moreno, J. C., Gammon, P. M., Jennings, M. R., Porti, M., Bayerl, A., Lanza, M. & Nafría, M. Micro and nano analysis of 0.2 Ω mm Ti/Al/Ni/Au ohmic contact to AlGaN/GaN. *Appl. Phys. Lett.* **99,** 213504 (2011).
12. Fontserè, A., Pérez-Tomás, A., Placidi, M., **Llobet, J.**, Baron, N., Chenot, S., Cordier, Y., Moreno, J. C., Jennings, M. R., Gammon, P. M., Fisher, C. A., Iglesias, V., Porti, M., Bayerl, A., Lanza, M. & Nafría, M. Nanoscale investigation of AlGaN/GaN-on-Si high electron mobility transistors. *Nanotechnology* **23,** 395204 (2012).
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20. Rius, G., **Llobet, J.**, Esplandiu, M. J., Solé, L., Borrisé, X. & Pérez-Murano, F. Using electron and ion beams on carbon nanotube-based devices. Effects and considerations for nanofabrication. *Microelectron. Eng.* **86,** 892–894 (2009).
21. Campanella, H., **Llobet, J.**, Duch, M., Esteve, J., Plaza, J. A., del Real, R. P., Diaz-

Michelena, M. & Guerrero, H. Nanomagnet fabrication on FBAR for magnetic sensor applications. *IEEE Int. Ultrason. Symp. Proc.* 2166–2169 (2009).

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Chapter 1 Introduction

When we talk about nanotechnology we are referring to the capability to manipulate the matter with at least one dimension sized form 1 to 100 nm. The nanometer is a unit of length that is 1 U.S. billion (or 10^9) times smaller than a single meter. For two-dimensional nanostructures, it corresponds to thin films up to a few atomic layers thickness. Structures that exhibit two or three dimensions at the nanoscale are nanoparticles, nanotubes and nanowires.

The semiconductor industry is one of the human activities that more efforts have assigned in R+D with the objective of manipulating materials at the nanoscale. The fabrication of a semiconductor is based on a planar technology. When the dimensions of an element is reduced by a factor x, the occupied space is reduced x^2. For that reason, the number of elements that can be integrated in a fixed area also increases by x^2. In other words, the numbers of transistors integrated on that chip is highly increased due to the reduction of their dimensions. During the last years the number of transistors integrated in a microprocessor is doubled every two years because of the reduction of the dimensions. This tendency is described by the well-known Moore's Law.[1] In figure 1a (source: phys. org) it is depicted the number of transistors per die until 2012, and it is observed a good agreement between Moore's prediction and the achievements of the semiconductor industry.

Obviously, nanotechnology is not only a matter of increasing the number of devices by reducing the dimensions to enhance the capabilities of a microchip. It is found that, in many materials and structures below 100 nm, their properties and characteristics are very different from their bulk form. There are a lot of efforts invested on the investigation of alternative lithographic techniques, other fabrication alternatives and also different types of devices like Carbon Nanotube Field Effect Transistors (CNT-FETs), graphene or silicon nanowires. These approaches to the nanoscale are known as "Beyond Moore" or "Beyond CMOS".

Moreover, as a result of the introduction of nanotechnology methods and concepts in different scientific fields, a lot of new applications in an interdisciplinary environment are

appearing and growing. In the fields of micro and nanoelectronics it is called “More than Moore” strategy. Figure 1b represents the position of the different areas of development of devices.

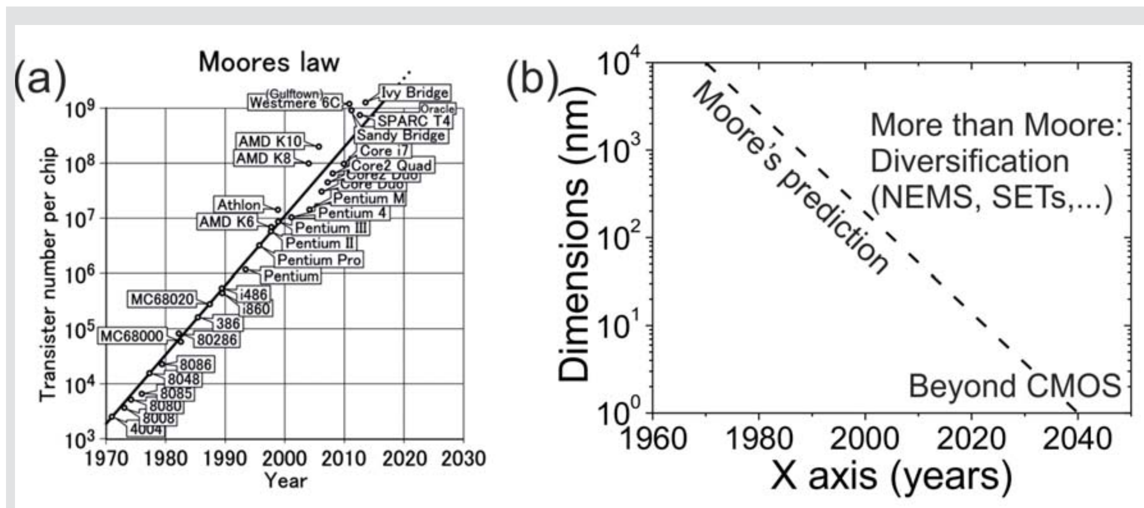

Figure 1. (a) Evolution of the number of transistors per die from 1970 to 2012 (source: phys.org). (b) Graphical representation of the More Moore, More than Moore and Beyond CMOS strategies where the x axis is the temporal axis and the y axis represent the dimensions to be achieved.

Nanotechnology is a collective term for a set of technologies, techniques and processes rather than a specific discipline. For that reason there are potentially a large number of very different applications for micro and nanotechnologies that involves the fields of nanoelectronics, nanomaterials, nanomechanics, nanophotonics, nanobiology, nanomedicine, etc. The applications goes from mass sensing, telecommunications, accelerometers, pressure sensors, strain gauges, gyroscopes, micro and nanomirrors, biomedical health care, implants, drug delivery, blood testing, dna testing, electronic components (high q inductors, electronic filters, switches, components for RF applications, antennas), low consumption mechanical components for electronics... In this thesis it is shown our last results in the fields of Nano Electro Mechanical Systems (NEMS) and Single Electron/Hole Transistors (SET/SHoT).

1.1 Nanofabrication. Basic concepts.

In order to explore and interact with the behavior of the matter at the nanoscale, it is necessary to fabricate nanodevices. Nanofabrication, that involves scientific and technological issues, is the set of methods, concepts and techniques to fabricate devices of, at least, one dimension in the nanometric or submicronic (< 100nm) range. There are two main strategies to reach nanometric dimensions, the bottom-up and the top-down approaches or a combination of both.

On the one hand the bottom-up strategy, or molecular manufacturing, consists on the construction or the assemble of a nanometric object or nanoparticle.[2–5] Those atoms or molecules could be arranged physically or by chemical reactions.

On the other hand, the top-down approach is based on the reduction of a large object or extended material until the achievement of nanometric dimensions. In micro and nanoelectronics this approach usually is performed at wafer level, where a high number of devices are produced in parallel. The fabrication processes typically starts by a lithography step followed by an etching, deposition or implantation step. Combining both approaches it is also feasible to define, by a top-down fabrication technique, the concrete place where the bottom-up fabricated object has to grow.

As this thesis is focused on a novel top-down fabrication approach, top-down fabrication techniques are briefly introduced next. It must be said that all the mentioned fabrication techniques has to be developed in a cleanroom environment in order to ensure the cleanliness and reproducibility of all the involved processes. For microelectronics, a cleanroom means an environmental controlled space where the particle contamination is below specifications and where the temperature, humidity and overpressure are fixed.

1.2 Top down fabrication processes

From the material point of view, silicon (Si) focuses the attention of this work. Silicon is a well-known semiconductor material with a great degree of technological development that permits the miniaturization of electromechanical devices, the integration at very large scale and the definition and place accuracy of devices with high precision within CMOS chip.

In the periodic table Si occupies the IV-A group, the same group than carbon and germanium, and it has 4 electrons in the conduction band. The forbidden gap for intrinsic silicon (energetic gap between the conduction band and the valence band) at room

temperature is of 1.2 eV. It is one of the most abundant elements on earth and it is found in silicon dioxide (SiO_2) form. SiO_2 is an excellent electrical insulator that exhibits an electrical resistivity around 10^{12} ~ 10^{16} [Ω·m], it is easily grown from Si and a native oxide of 1 ~ 2 nm is the natural protection of Si. The Young modulus of bulk silicon is 130 ~ 190 GPa. It is a piezoresistive material that means that an external mechanical strain produces a change in the electrical resistance. The electrical conductivity of intrinsic silicon is around $2.3 \cdot 10^3$ [Ω·m] but this magnitude can be tuned by doping, which is the introduction of a small quantity of dopant species in a substitutional lattice position. Usually Si is doped with elements of the III-A (p-type) or V-A (n-type) column. The expression p-type or n-type means that the element introduced in the crystalline lattice contains 3 or 5 electrons in the conduction band instead of 4. It means that there is an extra hole or electron for each introduced atom, without a strength bonding, available for the electrical conduction respectively. For example, by the addition of $1 \cdot 10^{18}$ atoms/cm^3 of boron, silicon electrical resistivity can be reduced to $4 \cdot 10^{-4}$ [Ω·m].[6,7]

The reachable dimensions are highly limited by the lithographic capabilities. Usually it is used optical lithography to define the structures on a photosensible resist that could be positive or negative. Then the resist is developed and:

- If a negative photoresist is selected, then the exposed resist remains and the not exposed resist is removed (figure 2a).
- If it is used a positive photoresist, the exposed resist is removed and the not exposed one remains (figure 2b).

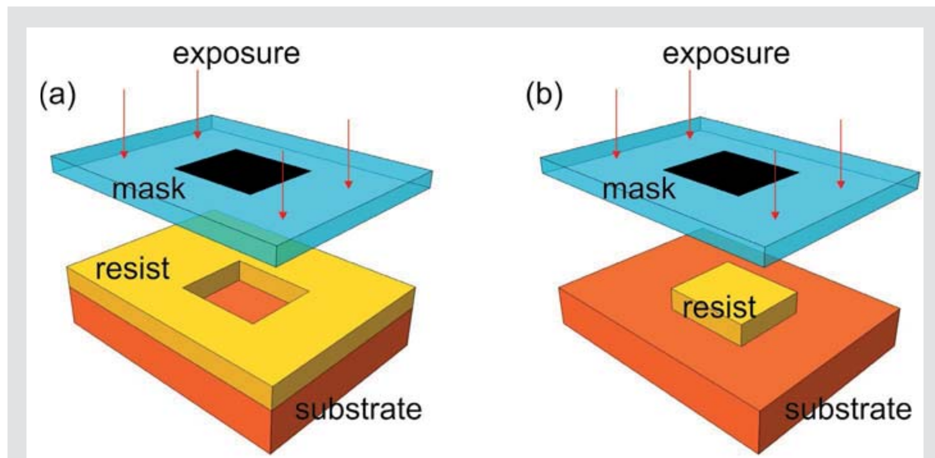

Figure 2. (a) Photolithography exposure performed through a mask on a negative resist. (b) Photolithography exposure performed through a mask on a positive resist.

The parameter that defines the achievable dimensions is the resolution, that is the smallest feature reachable, and it is influenced by the wave length as it is shown by the

following equation for the case of projection optical lithography:

$$R = K_1 \cdot \lambda / NA$$

Where R is the optical resolution, K_1 is an empirical constant, λ is the wavelength, and NA is the numerical aperture. The exposed resolution can be improved by reducing the wavelength, reducing the K_1 factor or by increasing the NA.

$$NA = n \cdot \sin\alpha$$

The reduction of the wave length enables the reduction of the dimensions. There are two alternatives:

- DUV (Deep Ultra Violet): The light source produces wavelengths of 248 nm (KrF) or 193 nm (ArF), that it is in the range of the deep ultraviolet (figure 3). The light source has to be narrow, stable, the repetition rate has to be high and the laser has to operate at high power (40W ~ 90W) according to Cymer, an ASML company, devoted in developing light sources for the semiconductor industry.

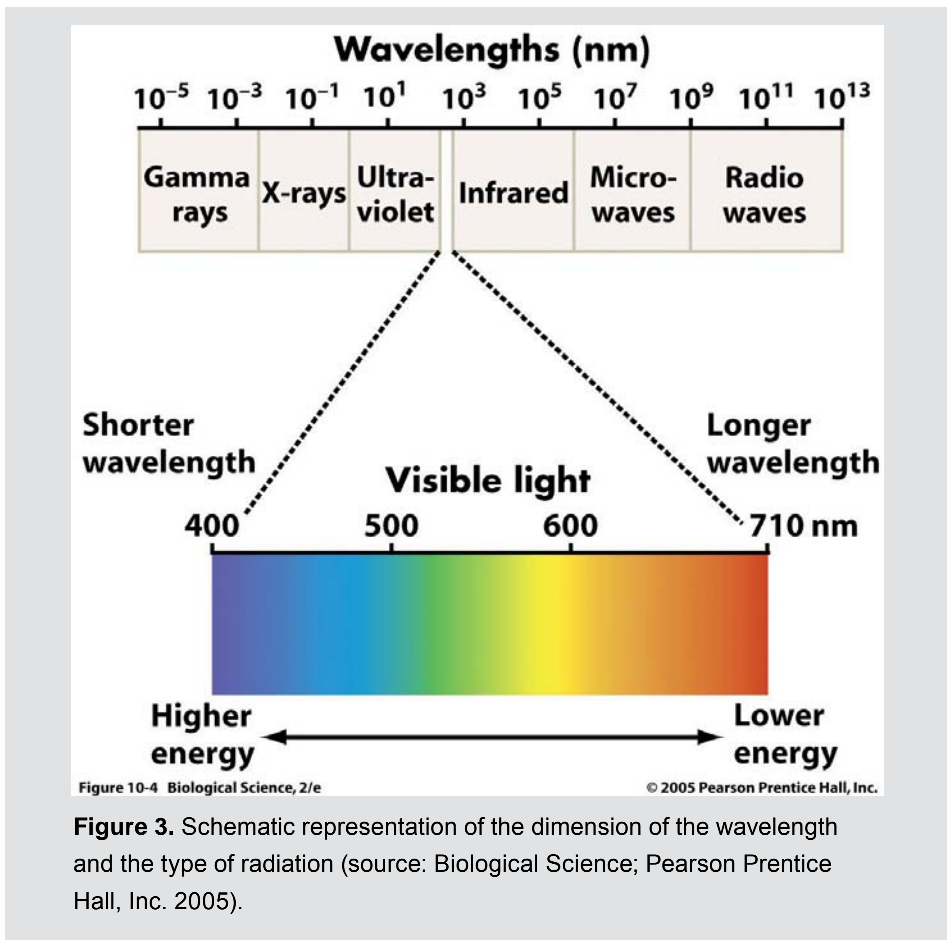

Figure 3. Schematic representation of the dimension of the wavelength and the type of radiation (source: Biological Science; Pearson Prentice Hall, Inc. 2005).

- EUV (Extreme Ultraviolet): The light wavelength for EUV is much shorter than for DUV. The light source selected can be a synchrotron (wavelength from 2.5 nm to 18 nm)[8] or a CO_2 high power laser for the creation of high energy plasma in a vacuum chamber achieving wavelengths of 13.5 nm according to Cymer. Traditional lenses cannot be used for EUV lithography because they absorb the light. Multilayer mirror (MLM) projection optics is used inside a vacuum chamber to reduce the absorption of light.

NA is an optical property that says how much light the lens can capture. By immersion the front-end surface of the lens in liquid (immersion DUV) it is possible to increase the value of n. It is also possible the reduction of the exposed dimensions by implementing double patterning strategy. Combining immersion lithography by changing the imaging medium with double patterning techniques it is possible enhance significantly the resolution achieving 40 nm and below.[9]

Due to the ultrahigh cost of the advanced photolithography tools used by the semiconductor industry it is needed other approaches for the fabrication of small batches of devices, for prototyping and for the academic study and research of nanoscale properties. Some of the lithographic technologies commonly selected are electron beam lithography (EBL), focused ion beam (FIB), nano imprint lithography (NIL) or atomic force microscopy (AFM). Some of these rising techniques are well establish and widely used.

- **EBL (Electron Beam Lithography):** In this type of lithography electrons are used instead of light.[10–13] Depending on the instrument, the resist used and substrate it is possible to achieve resolution below 10 nm.[14] In this case it is a serial lithographic technique, where the electron beam generated is used to scan the desired areas to expose the resist. The throughput is smaller than the obtained by optical lithography. A big advantage is that no mask (or reticle) is needed for the exposure. This technique is widely used for the fabrication of photolithography masks and reticles, for prototyping and for the production of small batches of devices.
- **FIB (Focused Ion Beam):** This is a very versatile technique[15–17] that could be used for fabrication, characterization and modification/edition of the samples. It exists a large number of available ion sources (helium,[18,19] gallium,[20] bismuth,[20] gold/germanium,…[21]) but the most used nowadays is the gallium source. For nanofabrication, gallium FIB technology permits to mill[22] (or etch) directly the desired structures on the sample (could be a metal, a semiconductor or even an insulating material), to assist the deposition of some species (Pt,[23,24] SiO_2,[25] C,[26] Au,[27] W,…[28]) and to implant gallium ions[29] into the sample. All these capabilities could be performed without depositing any resist and without employing any mask, allowing the fabrication on top of complex three dimensional samples.[30,31] (see chapter 2)
- **NIL (Nano Imprint Lithography):** This technique is based on the indentation of a

patterning media (commonly a polymer) by a mechanical load.[32,33] There are two main approaches for this technique, the thermal NIL and the UV-NIL. The first one was firstly reported by Chou et al[34] and it is performed by applying pressure and temperature to a thermoplastic material that is embossed above its glass transition temperature (T_g). Then, when the process is finished, the sample is cooled and the load is released. In the second approach it is used UV light to cure the polymer during the impression.[35]

- **AFM (Atomic Force Microscopy):** There are some fabrication techniques based on AFM. They can be classified into force-assisted AFM, where a force is applied to the tip for patterning (indentation,[36] thermomechanical writing,[37] nanomanipulation,[38] dip pen,[39] scratching),[40] or bias-assisted AFM, where a local electric field is applied through the AFM tip that acts as an electrode (anodic oxidation).[41–44] In the case of anodic oxidation, this lithographic technique could be applied on anodizable materials. It consists on the application of a positive voltage through the sample referred to the AFM tip. Then, in an atmosphere with a presence of a controlled humidity, the tip induces the local oxidation of the surface of the sample.[43,45–49]
- **Other techniques:** There are many other techniques developed for the fabrication of nanostructures. Among them nanostencil[50] consists on the fabrication of a perforated sample to be used as a hard mask for pattern replica. It is a very versatile technique that permits the definition of nanometric structures as the deposition of nanoparticles[51] to the deposition of structures at full wafer level[52] or by ion implantation.[53] It has been developed other strategies to produce micro and nanometric three-dimensional structures based on two-photon lithography,[54] when the polymerization of an excitable resin take place where the two-photon are absorbed simultaneously.

1.2. Pattern transfer

As it is observed in the previous example, once the lithography is performed, the next step consists on transfer the patterned designs from the resist to the sample. Basically there are three possible methodologies: (i) substractive methods, (ii) addition methods and (iii) modification methods. Here there are presented an example of each one:

i) Substractive method.

Substractive methods are referred to methods developed to remove material. It includes chemical methods, physical etching, mechanical sputtering or ablation.

Here it is shown an example of **silicon etching**. The first step consists on spin coat a resist on top of a sample (figure 4a,b), which could be a chip or a wafer. Then, a lithography step (photonic, electronic or ionic) is used to define the pattern on the sensitive resist (figure

4c). After developing the resist (figure 4d), silicon is etched using the remaining resist as a mask (figure 4e). There are some well-known approaches to etch silicon and they are classified in wet[55,56] or dry[57] etching. Once silicon is etched and the pattern is transferred onto the sample, the resist is removed (figure 4f).

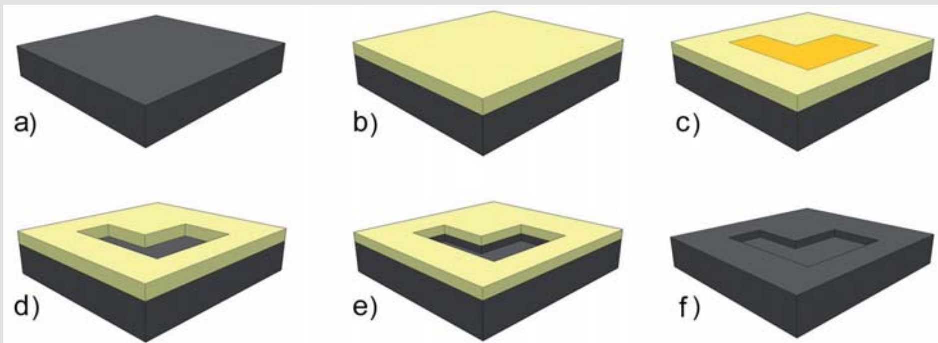

Figure 4. Schematic representation of the process: a) Si substrate, b) resist deposition, c) lithography step, d) resist development, e) etching process and f) resist removal.

ii) Addition method.

In this category it could be found technological approaches for the deposition of materials on top of substrates or devices to be processed, assembly using welding and bonding techniques and the controlled grown of materials with desired characteristics.

It is shown as an example the fabrication of metal structures (could be gold, titanium,…) by a **lift-off** process on top of a silicon dioxide layer. The first step consists on spin coat a resist layer (figure 5b) followed by a lithographic technique (photonic, electronic or ionic) to expose the sensible resist (figure 5c). After developing the resist (figure 5d) the sample can be coated with a metal layer (figure 5e) by evaporation or sputtering. Finally, by a lift-off process in acetone, the resist is removed and the desired pattern is defined on metal on top of the sample (figure 5f).

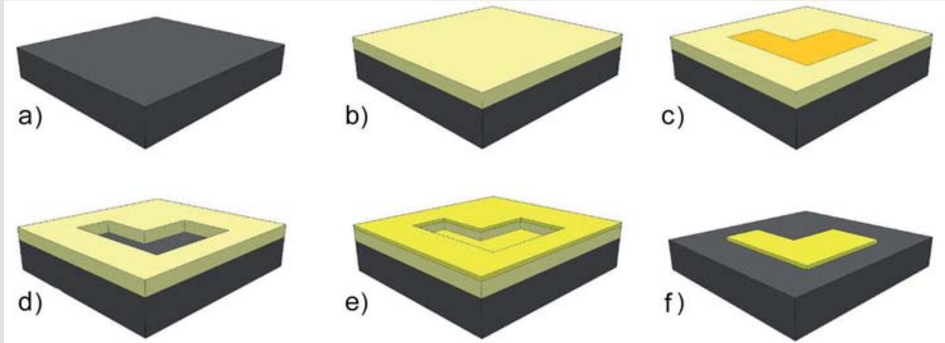

Figure 5. Schematic representation of the process: a) SiO_2 substrate, b) resist deposition, c) lithography step, d) resist development, e) coating and f) lift-off.

iii) Modification method.

There are some methods that permit the modification of the properties of the materials. It involves the introduction of carriers by doping a semiconductor (dopants introduced by diffusion or ionic implantation), changes in the nanostructure or crystalline structure by radiation or the change of solubility of a resist because of a lithographic exposure.

It is presented an example of modification of the material properties by **ion implantation**, where the resist does not sustain the complete process. For that reason it is needed to create another mask that sustains the whole process. This new mask is SiO_2 grown thermally from the Si sample in a controlled furnace (figure 6b). Once the SiO_2 mask is grown, the next step consists on spin coat a resist (figure 6c) and, by lithography (that it is a modification method by itself), the pattern to be transferred is defined (figure 6d). Then, the SiO_2 is etched using the resist as a mask (figure 6f). The resist is removed (figure 6g) and the ion implantation (figure 6h) is performed using the grown oxide as a mask. The last step consist on remove the SiO_2 mask (figure 6i) and the silicon properties of the sample are modified by the incorporation of a small quantity of ions and for the amorphization of the silicon structure according the defined pattern (figure 6i). Then, this volume of sample that is modified can be used as a mask for silicon etching (figure 6j).

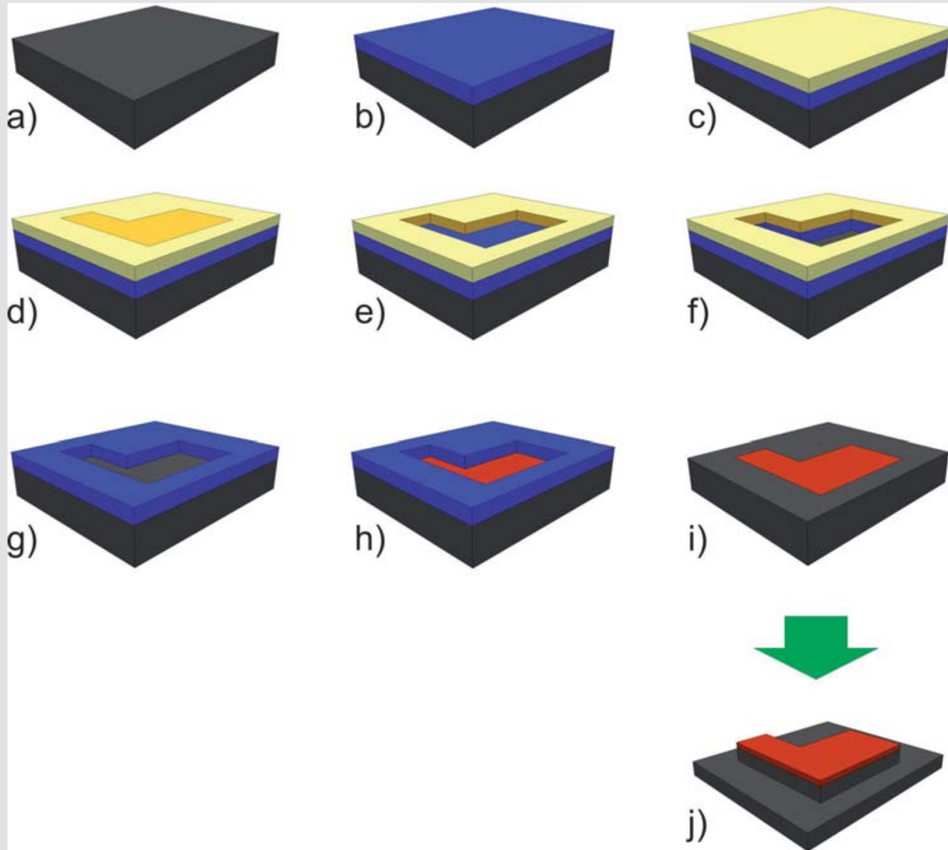

Figure 6. Schematic representation of the process: a) Si substrate, b) SiO_2 grown, c) resist deposition, d) lithography exposure, e) resist development, f) SiO_2 etching, g) resist removal, h) ion implantation, i) SiO_2 removal and j) Si etching.

In chapter 3 it is described the fabrication of micrometric electrical pads by ion implantation of boron onto silicon by the use of SiO_2 as a mask, patterned by photolithography and wet etching. Once the electrical pads are defined it is used FIB implantation to define nanometric structures in a mix and match approach between the high throughput provided by photolithography technology and the high resolution obtained by FIB.

1.3. Mix and match approach Fabrication exemple

Sometimes it is needed to combine different types of lithographic steps in order to fabricate the appropriate device for a particular application. For example, in the frame work of the SNM-EU project (described in the presentation of this thesis), we are working on the fabrication of suspended FET transistors and nanomechanical resonators of 10 nm diameter. One of the approaches that we are developing in this project involves up to 4 different lithographic techniques (figure 7). It starts with SOI (Silicon On Insulator) chips of 15 nm of top silicon and 150 nm of buried SiO_2 (figure 7a). To achieve these small dimensions AFM anodic oxidation is selected to fabricate the nanowires[43,49] on the top silicon(figure 7g-h). Optical lithography exhibits the highest throughput and it is used for the definition of the biggest parts in terms of exposed area, which are the electrical pads and the connections (figure 7c). Then, by AFM anodic oxidation, 5 silicon nanowires in parallel has been defined. In figure 8a it is shown 5 parallel silicon nanowires fabricated by AFM anodic oxidation between 2 gold connections defined by optical lithography.

Once the devices have been obtained the next steps are oriented to release the structures. First, by FIB direct milling, 4 alignment marks has been defined close to the nanowires (figures 7j and 8b). Then, a PMMA layer is deposited (figure 7k) as a mask for the subsequent wet etching and, by EBL, it is exposed the area to be released (figures 7l and 8c). Next, the chips are immersed in Sioetch solution in order to etch the SiO_2 (figure 7n) that is not protected by the PMMA, the PMMA etching mask is removed (figure 7o) and the chip is dried in a CPD (Critical Point Drier). The final suspended silicon nanowires are depicted in figures 7p and 8d.

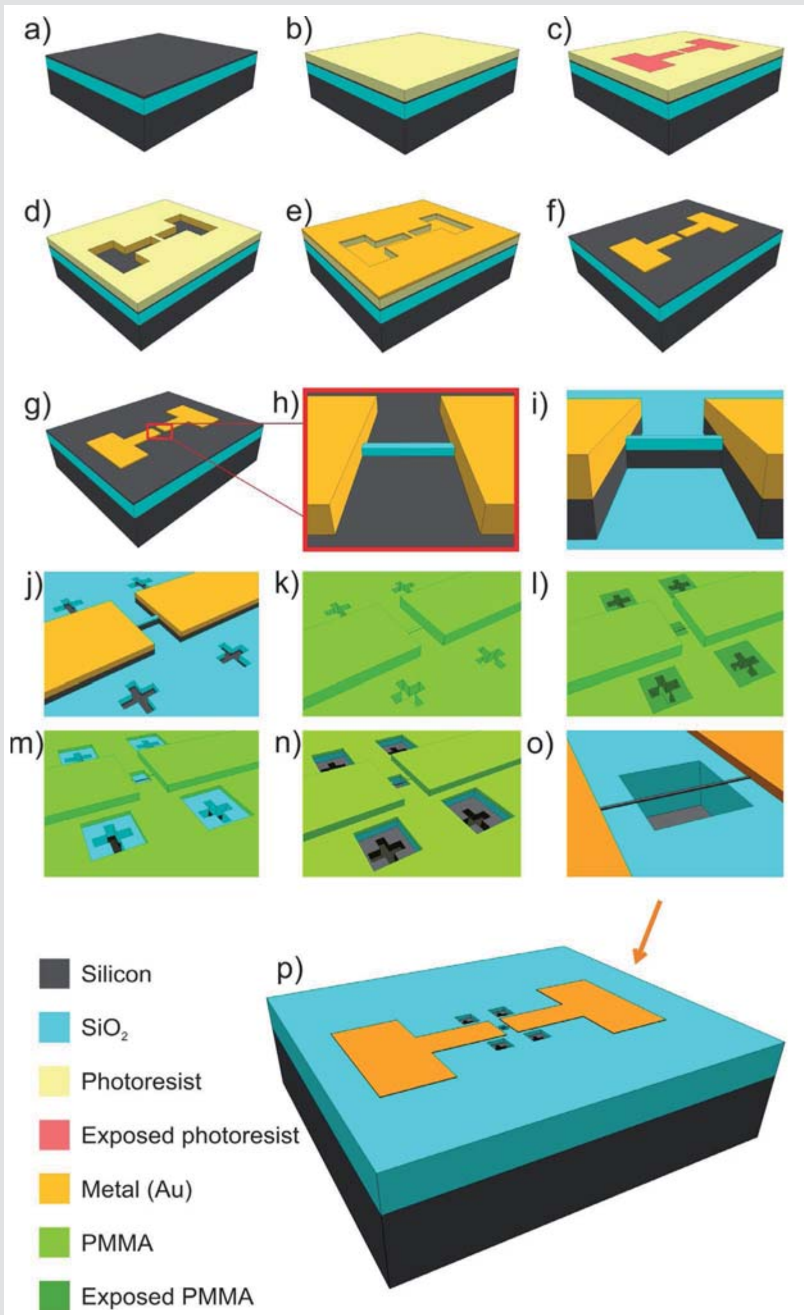

Figure 7. Schematic representation of the process: (a) SOI substrate, (b) resist deposition, (c) photolithography, (d) resist development, (e) Au evaporation, (f) lift-off, (g) AFM anodic oxidation, (h) zoom-in of the nanowires, (i) silicon reactive ion etching, (j) FIB mark definition, (k) PMMA deposition, (l) EBL exposition, (m) PMMA development, (n) SiO_2 wet etching, (o) PMMA removal, (p) representation of the complete device.

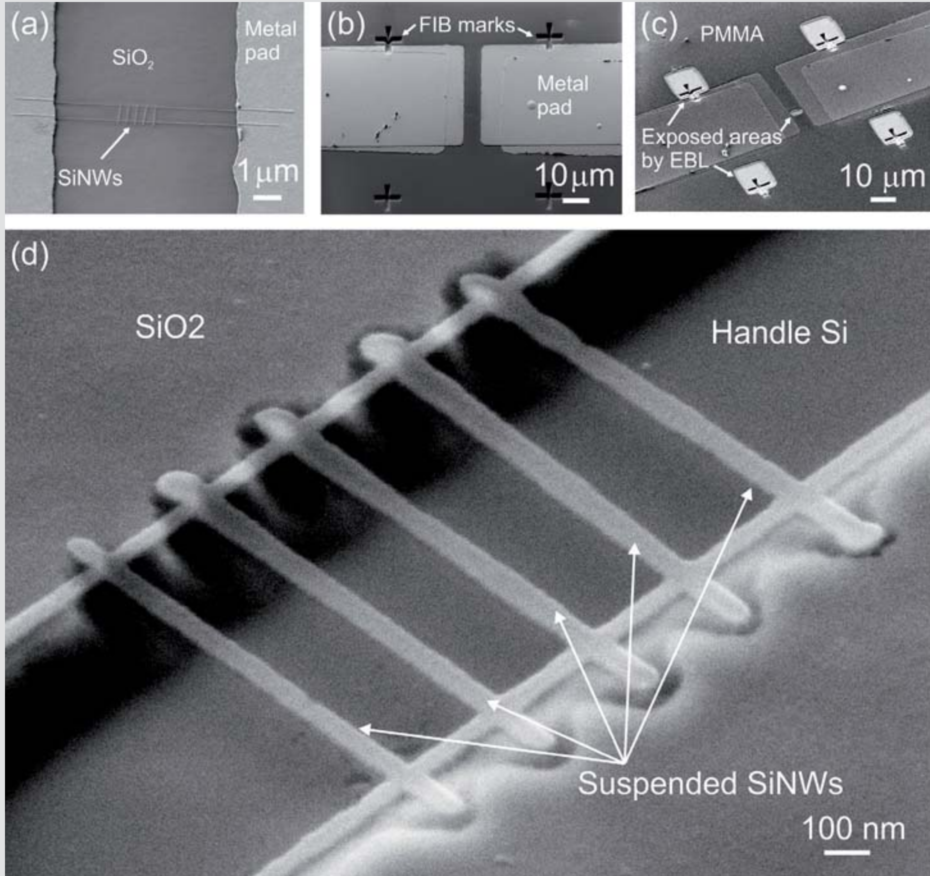

Figure 8. (a) SEM image of 5 silicon nanowires in parallel connected by 2 large nanowires to the gold electrical pads. (b) In this SEM image it is shown the alignment marks for the EBL defined by the FIB. (c) SEM image of the structures covered by PMMA where it can be observed the EBL exposed areas. (d) SEM close up image of the released nanowires.

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Chapter 2 Focused ion beam for nanotechnology and nanofabrication

2.1. Introduction

In this chapter it is summarized some of the physical and chemical phenomena encountered in FIB and their principal applications in the fields of nanotechnology and nanofabrication.

Currently, FIB systems are very versatile platforms that can be customized as a function of the research needs. The FIB equipment used during this thesis is the Crossbeam 1560XB (Carl Zeiss) and it can be described as a “nanoscale workstation” or a “nanoscale laboratory”. It is possible to use at the same time and on a fixed location of the sample the different parts of the equipment, which consist on:

- FIB column (Canion, Orsay Physics)
- SEM column (Gemini, Carl Zeiss)
- Gas Injection System (Multi-line GIS, Orsay Physics) with 5 different precursors:
    - Pt
    - SiO_2
    - C
    - XeF_2
    - H_2O
- 3 nanomanipulators (Kleindiek)
- 4 connection SMA feedthrough for high frequency excitation (designed and fabricated on demand)
- 2 x 25 pin connection (DB-25) feedthrough.
- EBIC (Electron Beam Induced Current) analysis.
- Electron detectors: In-lens detector and SE Everhart-Thornley detector.
- Ion/electron lithography capabilities (Elphy Quantum, Raith)

The integration of all this parts allows:

- The fabrication of nanometrical structures by direct gallium-ion milling (etching) of any solid material[1] with or without the addition of vapor chemical etchants (XeF_2 or H_2O)

- The fabrication of nanometrical structures by direct ion/electron induced deposition of platinum, silicon dioxide or carbon.
- The SEM characterization of multilayered materials or buried devices
- The electrical characterization, electrical read-out or electrical actuation of small devices.
- The fabrication of Transmission Electron Microscopy (TEM) lamellae
- The edition of electrical devices or photolithography masks.
- The local modification of materials by ion implantation or amorphization.

Actually there are some FIB-SEM systems available commercialized by the two principal FIB-SEM manufacturers, that are Carl Zeiss and FEI. Each company calls them in a different manner, for example Carl Zeiss uses the brand Crossbeam and FEI employs DualBeam. Nowadays FEI offers four DualBeam equipements and Carl Zeiss two Crossbeam. The next table summarizes some of the characteristics of the FIB-SEMs available according to the data supplied for the manufacturers compared with the Crossbeam 1560XB employed for this thesis.

Manu-facturer	Model	SEM resolution in nm at 30KeV (for STEM)	FIB resolu-tion in nm at 30KeV	FIB current	Other specifications
FEI	Helios	0.6	4	0.1 pA ~ 65 nA	Oriented for general purpose
	Scios	0.8	3	0.6 pA ~ 65 nA	High resolu-tion and high contrast in-lens detector
	Versa 3D	0.8	7	1.5 pA ~ 65 nA	High and low vacuum modes for uncoated or coated samples
	ExSolve	-	-	-	Automated TEM sample prepa-ration. High dimension vacu-um chamber (wafers diame-ter 30cm)

Zeiss	Cross-beam 340	0.9	< 3	1 pA ~ 100 nA	High vacuum, charge compensation and variable pressure. Laser optional for massive ablation.
	Cross-beam 540	0.7	<3	1 pA ~ 100 nA	High vacuum and charge compensation. Laser optional for massive ablation.
	Cross-beam 1560XB	1.2	7	1 pA ~ 50 nA	High dimension vacuum chamber (fully access to 15cm diameter wafers. Wafers of 20cm can be operated)

Table 1. Some of the principal characteristics of the commercial FIB-SEMs according to the manufacturers.

2.2. Electron beam. Interactions between electrons and matter.

A SEM column is mounted in the Crossbeam and it is placed perpendicular to the surface. The SEM produces an electron beam that is used to scan the surface of a sample or, for EBL applications, to exposure the desired pattern on a resist. The electrons emitted by the SEM are called primary electrons. Due to the interactions between the electrons and the sample some different phenomena occur. First of all, the incident beam produces different kind of electrons. The most important for SEM characterization are the backscattered electrons and secondary electrons. As it is explained below, they are used to construct images with different information of the sample, from composition to topography. Secondly, X-Rays are also produced, giving qualitative and quantitative composition information of the irradiated volume. Finally it is also possible to measure the electrical current that passes through the specimen that gives valuable information about

the conductivity of the sample.[2] There are also produced local heating of the sample that has to be taken into account to prevent the deformation of some low temperature samples with poor thermal conductivity. In a Transmision Electron Microscope (TEM) analysis it is also produced an electron beam for the sample analysis. In this last case, the electrons passes through the sample (it has to be very thin) providing a structural information of the atomic arrangement.

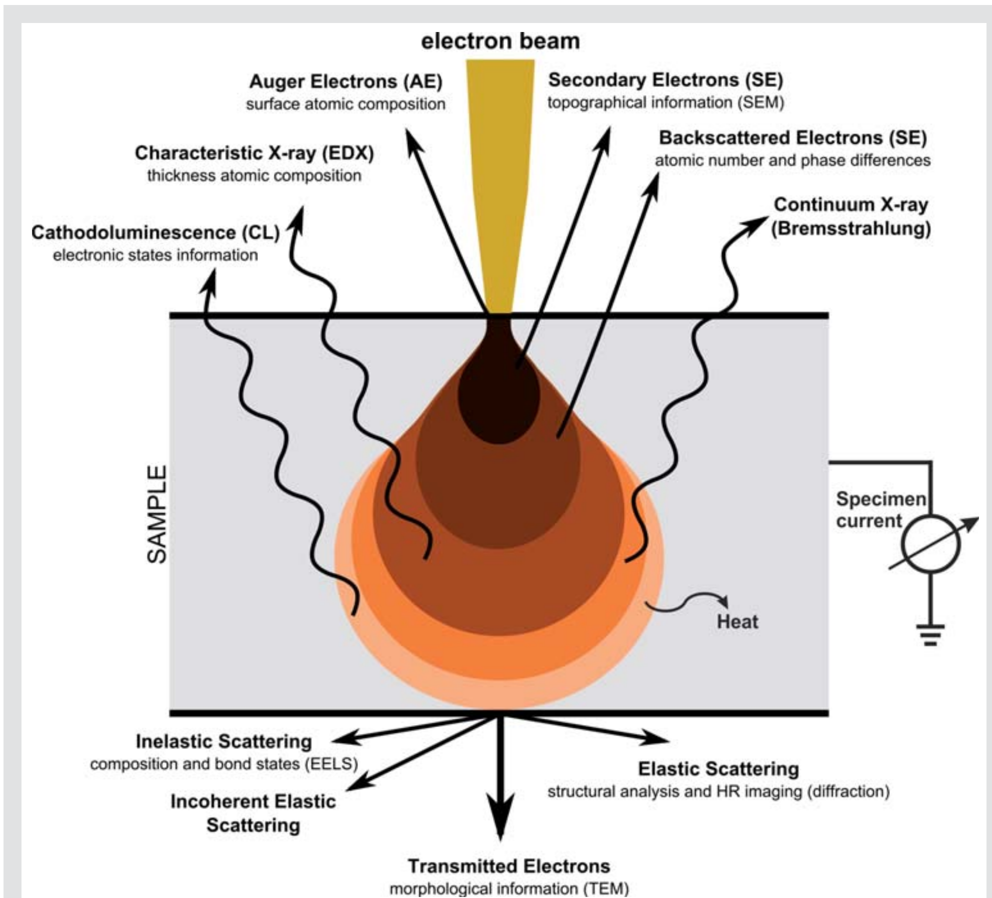

Figure 1. Principal interactions that are produced when the electron beam collides the sample (source: figure adapted from wikipedia.org). The effects represented in the bottom part of the figure only can be noticed for high energetic electron energy (typically 50 ~ 300 KeV or higher) and thin samples (in the order of 50 ~ 100 nm thickness).

When the electrons of the incident beam strike the surface of the sample some of them penetrate into the material. The penetration depth depends on the atomic weight of the elements of the sample and the energy of the incident beam. When the elements of the sample exhibit a low atomic number, then the penetration of the electrons are deeper

than in the case of a sample of high atomic number (figure 2 top). Regarding the electron beam energy (typically goes from 200V to 30kV) the higher the energy, the higher the penetration depth is (figure 2 bottom).

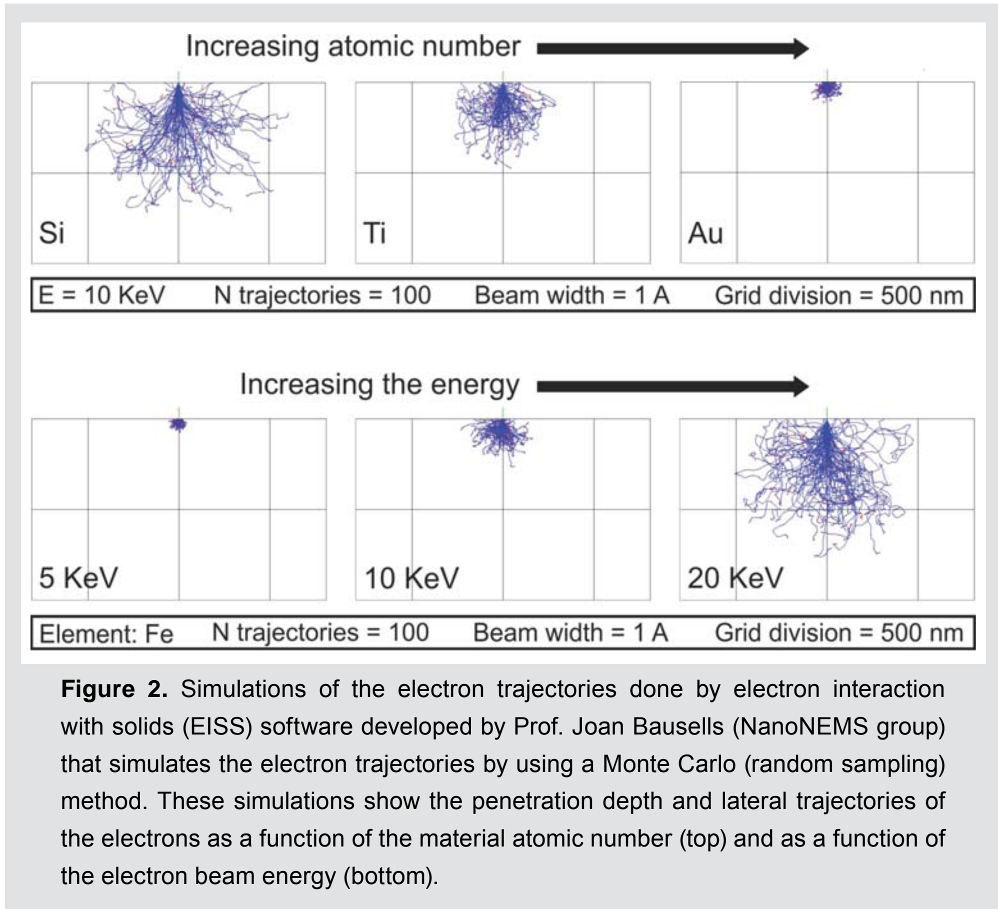

Figure 2. Simulations of the electron trajectories done by electron interaction with solids (EISS) software developed by Prof. Joan Bausells (NanoNEMS group) that simulates the electron trajectories by using a Monte Carlo (random sampling) method. These simulations show the penetration depth and lateral trajectories of the electrons as a function of the material atomic number (top) and as a function of the electron beam energy (bottom).

2.2.1. Backscattered electrons

The backscattered electrons are the electrons that are back-scattered or reflected by elastic scattering interactions with specimen atoms. They give information of the composition of the sample. The first condition for the production of backscattered electrons is that the incident electrons have to achieve the sample with enough energy to penetrate it. Then, the electrons travel through the sample interacting with matter where: i) part of the energy is absorbed by the sample by inelastic collisions and ii) another part of the energy comes back to the surface of the sample as backscattered electrons.[2]

The heaviest atoms could reemit more than the 50% of the energy and, for the lighter ones, the reemission could be in the order of the 6%. The topography and the incident angle

of the electrons are important parameters that influence the production of backscattered electrons. To enhance the production and detection of those electrons it is convenient to place the sample perpendicular to the incident beam. As the backscattered detector is mounted inside the electron column it is appropriate to approach the sample to the last lens of the electron column. According to the manufacturer an optimum distance is close to 1.6 mm.

2.2.2. Secondary electrons

Secondary electrons are the term used to describe the electrons emitted by the specimen when the primary electron beam (or the water fall of electrons that travels randomly through the sample) excites the electrons of an atom of the sample. Those electrons are not very energetic. For that reason, they are only detected when they are produced close to the sample surface. Consequently, secondary electrons are very useful to produce topographical images of the sample at good resolution. The secondary electrons could be produced by the incident beam and also for the backscattered electrons that crosses the sample surface in their return trip.[2]

2.2.3. X-rays

X-rays can be produced when the incident beam excites an electron of the sample. The electron is ejected from the atomic orbital creating a hole. A higher energetic electron from an outer orbital has the possibility to fill the hole. Then, the energetic difference between the two electronic states can be released as X-rays. The quantification of those energies is a signature of an element and can be used to characterize the materials of a sample.

2.3. Ion beam
Interactions between ions and matter

The Focused Ion Beam (FIB) column attached to the Crossbeam is mounted at 54 degrees respect to the SEM column. The FIB generates a positive gallium ion beam. The interaction of those ions and the sample produces some effects that are going to be studied in this section. Those interactions are different than the interactions electron-sample, basically because ions exhibit higher masses than electrons.

There are two basic interactions that occur when an ion beam hits a sample. On the one hand, an elastic collision (in which there is no loss of kinetic energy) produces a displacement of the atomic lattice, contributes to the defects formation, produces ion implantation and generates sputtering at high ion doses. The dosage corresponds to the number of incident ions per area. On the other hand, an inelastic collision (in which part of

the kinetic energy is changed to some other form of energy) produces other phenomena as the generation of secondary electrons, X-rays or photon emission.[1] Elastic and inelastic phenomena could be used for different scientific and technological applications. As an example, the sputtering effect could be used for the fabrication of a structure by ion milling and the secondary electrons could be used to generate an image of the sample.

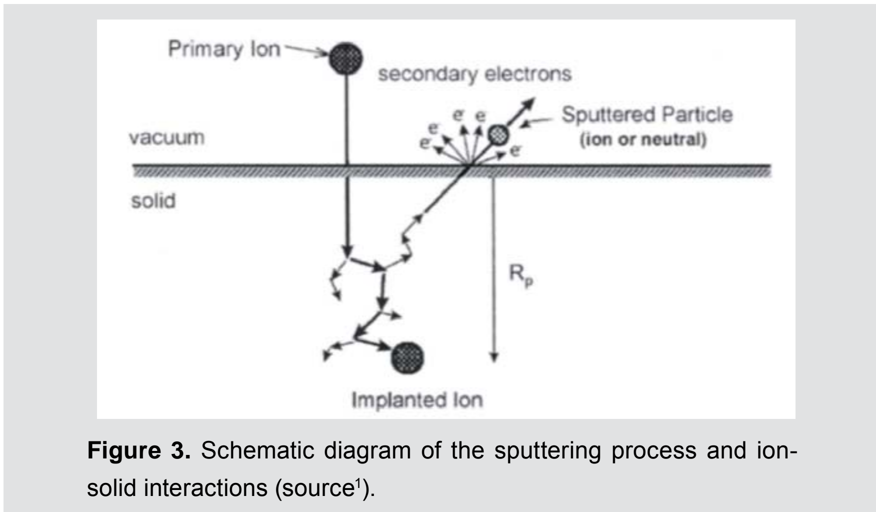

Figure 3. Schematic diagram of the sputtering process and ion-solid interactions (source[1]).

During the FIB machining there are produced some effects as damage, ion implantation, sputtering and secondary electrons (figure 3) due to the ion-matter collisions. There are some ions with enough energy to penetrate the sample producing dislocations inside the material. This damage creates amorphous volumes in crystalline materials. The ion range depth depens on the sample material, the ion used and the energy of those ions. Some ions losses their energy and can be trapped inside the sample, it is called ion implantation. Ion implantation is commonly used by the semiconductor industry to introduce dopants onto semiconductor materials like silicon. When the momentum transferred form the collision cascade to the sample is sufficient sputtering occurs.[1]

FIB is widely used to produce localized sputtering on a sample. Physical sputtering appears when the incident ions transfer enough energy to the surface atoms and some of them are extracted. That process is used to modify the shape and the structure of the sample. Part of the sputtered atoms are ionized and they could be used to produce an image or to be detected by a SIMS (Secondary Ion Mass Spectroscopy) detector. The ion beam diameter (d) is reasonably small ($d < 7$ nm according to the manufacturer) that permits to generate small structures and high resolution images.

It is also possible to produce chemical vapor deposition (CVD) reactions inside the Crossbeam chamber. This process is called FIB induced deposition (FIBID) when the reaction is induced by ions or focused electron beam induced deposition (FEBID) when the electron beam is used. The reaction is produced by the combination of the incident

beam with some introduced gases into the chamber producing chemical reactions that interacts with the surface of the sample creating new compounds. The gas molecules decompose in the places where they interact with the secondary electrons produced by the focused beam. For that reason material can be deposited in the desired places of the sample surface. The capabilities available on the Crossbeam used for this thesis allow the deposition of Pt, C or SiO_2 or the FIB induced etching (FIBIE) with XeF_2 or H_2O gas.

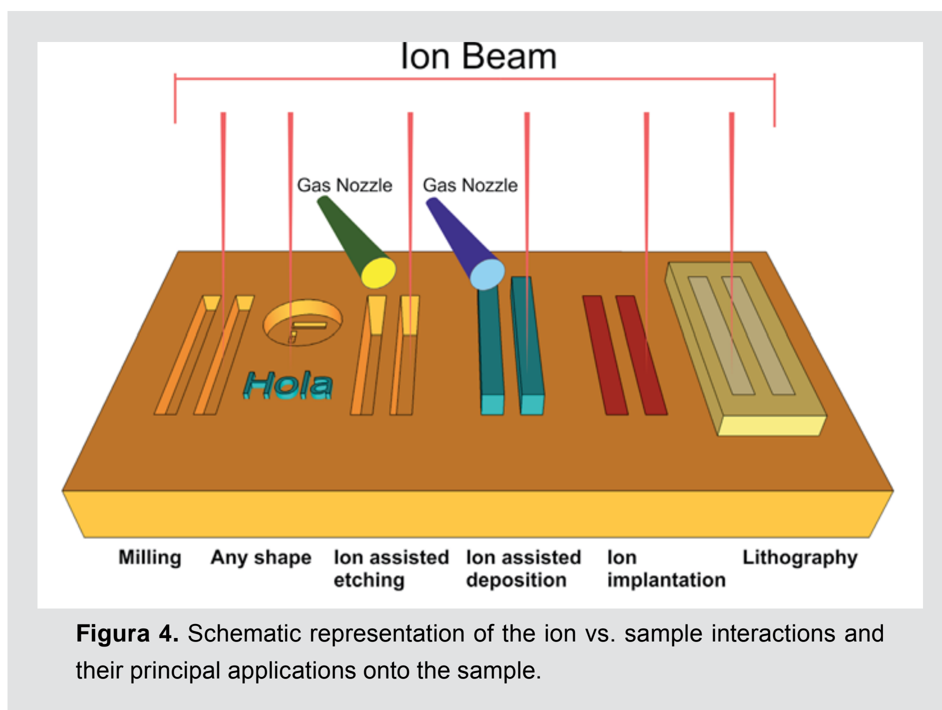

Figura 4. Schematic representation of the ion vs. sample interactions and their principal applications onto the sample.

There are different possibilities of ion sources for ion beam equipment (He^+,[3,4] Bi^+, Au^+,[6] etc.). For the commercial FIBs it is commonly used a liquid metallic ion source (LMIS) of Ga^+.[5] This type of metal source has some special characteristics: The fusion temperature of gallium is 29.8 C (very close to the room temperature). The low pressure of gallium vapor permits to use it at high purity. This sources exhibits high life time. The emission properties are very convenient to produce a high intensity and very focused beam. Gallium ions are heavier and exhibit higher sputter rates than other ion sources like helium. The sputter rate is the removed volume of material per quantity of charge. For that reason the gallium source FIB is very convenient for ion milling applications and the helium ion microscope (HIM) is oriented to imaging.

The capability for milling, imaging, implanting and depositing material by the FIB depends on the interactions between the ion beam and the sample. Milling is produced as a consequence of physical sputtering of the sample. Sputtering is the result of a series of elastic collisions where the incident ion energy is transmitted to the atoms of the receptor material producing an affected region and removing material in a localized way. In figure 5 it is depicted the phenomena produced when the incident ions produces sputtering on the sample. Part of the subproducts (removed material and some incident backscattered ions) produces redepositions. If there is enough energy, another part of the subproducts will produce second order sputtering. This process will go on and on while there is enough energy.

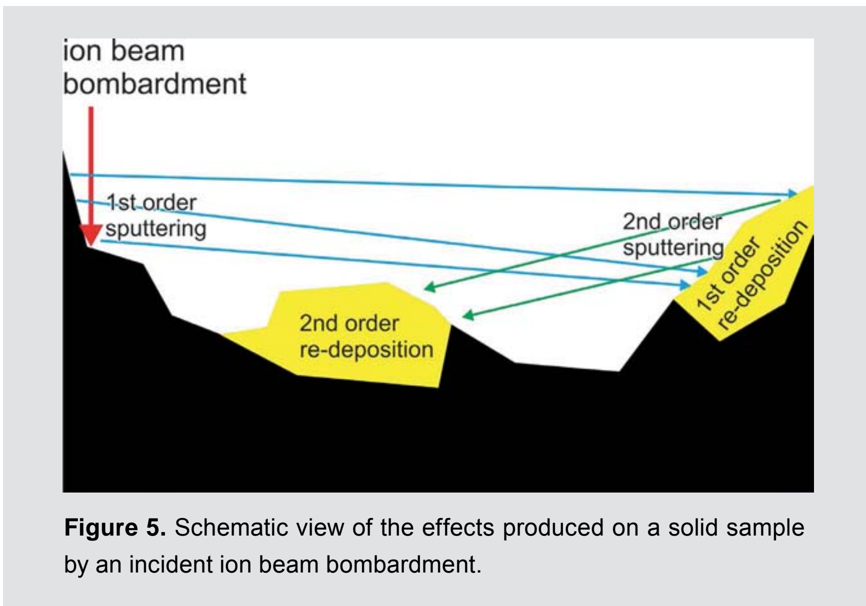

Figure 5. Schematic view of the effects produced on a solid sample by an incident ion beam bombardment.

Depending on the material that is bombarded and the energy of the incident beam, the volume of removed material is different. For instance, a gallium ion beam accelerated at 30 kV removes 0.27 $\mu m^3/nC$ of silicon, 0.2 $\mu m^3/nC$ of silicon nitride, 0.18 $\mu m^3/nC$ of carbon, 0.3 $\mu m^3/nC$ of aluminum, 1.5 $\mu m^3/nC$ of gold or 0.14 $\mu m^3/nC$ of nickel. Furthermore, the incidence angle of the beam has an important effect in the sputtering yield (figure 6). The sputtering yield is defined as the average number of atoms removed from a solid surface per incident particle.

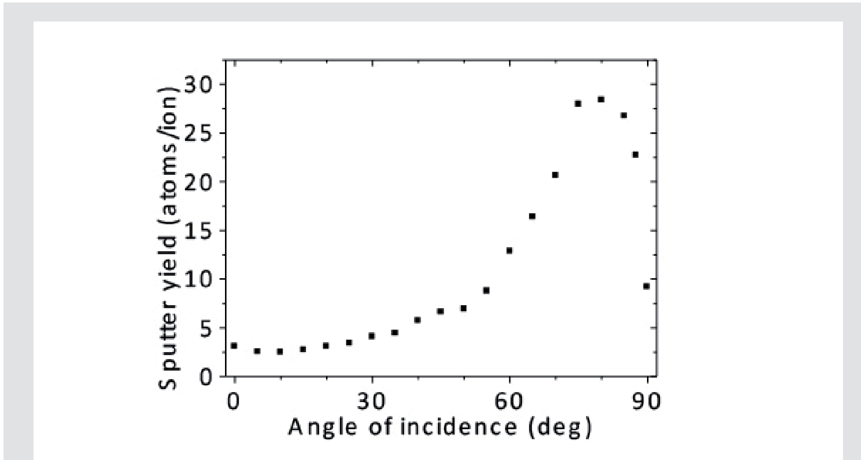

Figure 6. Stopping and range of ions in matter (SRIM version 2013.00) simulation that describe the relationship between the angle of the incident ion beam and the sputter yield. An angle of incidence equals to 0 deg corresponds to a situation of perpendicularity between the ion beam and the sample.

To sum up, the interactions between electrons and matter could be used to produce images of a sample with topographic or compositional information whereas the interactions between ions and matter could be used for milling, imaging and ion implantation. Moreover, both charged beams (ions and electrons) could be used as a lithographic tool to expose a sensitive resist or, in combination with some appropriate gases, they could be used to selectively deposit materials like platinum, gold or silicon dioxide.

2.4. Applications

As it is introduced at the beginning of this chapter, FIB permits to explore and/or interact with the matter at the nanoscale. All the examples of applications presented next in this section have been realized by the author of this thesis using the Crossbeam equipment and its add-ons that has been presented at the beginning of this chapter. The aim of this section is to show real examples of different kind of applications made with this equipment.

In general, when the Crossbeam is used, the first step consists on tilting the sample 54 degrees to reach the perpendicularity between the sample and the ion beam. It is also useful, but not mandatory, to find the eucentric point if the tilt angle has to be changed

during the SEM inspection or FIB processing. The next step consists on finding the coincidence point between the electron beam and the ion beam in order to control, in real time by the use of the SEM imaging, the ion processing performed by the FIB.

To structure this section, the principal applications have been classified in two main categories. On the one hand, the applications related with the material or device **characterization** and, on the other hand, the uses in which the objective is the voluntary **modification** of some characteristics or behaviors of a structure or device.

2.4.1. Characterization

From the characterization point of view, the Crossbeam could be used for the realization of **cross-sections** of multilayered materials and buried devices for the subsequent SEM characterization. In general, it is possible to resolve up to the order of 10 nm but this parameter will depend on the materials involved (it is more achievable for electrically conductive or semiconductive samples than for insulators) and also the depth where the features are found. In this section there are three examples of cross-sections. The first one has been done for the characterization, during the clean room fabrication, of the dimensions of silicon nanowires defined by photolithography (figure 7).[7] The second example (figure 8) shows the characterization of a released micro electro mechanical system (MEMS). The last example is focused on the characterization of a test structure of the IMB-CNM complementary metal oxide semiconductor (CMOS) technology (figure 9).

When it is needed more resolution than the obtained by an SEM or it is required an investigation of the atomic arrangement, usually it is required a **TEM lamella** done by FIB technology. In chapter 5 section 4 it is described the principal steps required for the fabrication of a TEM lamella that is part of an ongoing work.

Finally, in chapter 4 it is exposed some practical examples of **electrical characterization** done during this thesis that results from the combination of the Crossbeam with different external electronical setups that could be connected to the sample by the feedthrough or by the electrical probes.

Cross-sections

The first application example shows the cross-section of a suspended silicon nanowire and their side-gate electrode. This device has been fabricated by optical lithography and, in order to reduce de diameter of the nanowire, steps of oxidation (figure 7a) and oxide removal have been performed. A cross-section has been done just after an oxidation step (figure 7b) in order to characterize the thickness of the grown oxide (bright features). Here it can be also extracted the final thickness and width of the nanowire. This characterization

work has been performed during a fabrication batch in order to measure the dimensions of the devices measured for this study[7]. As the fabrication is performed in parallel at wafer level, there are thousands of devices in a single wafer. For that reason, although it is a destructive characterization technique in terms of a single device, the information extracted is very useful for the characterization of the process and to determine the dimensions of the rest of the devices of the wafer. Once the oxidation has been done, the oxide is removed by HF wet etching reducing the section of the nanowire (figure 7c).

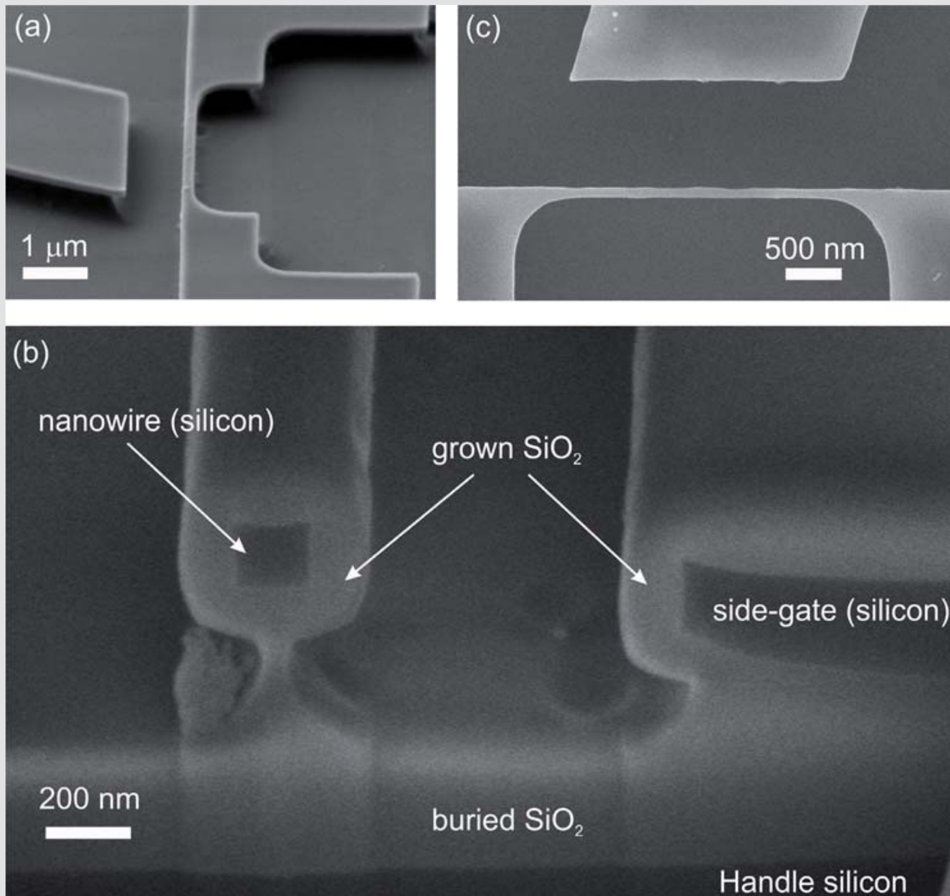

Figure 7. SEM images of different suspended silicon nanowires with a side gate electrode. (a) SEM image of a nanowire, defined by optical lithography, after an oxidation step. The nanowire width is 200 nm. (b) SEM image of the FIB cross-section of another oxidized nanowire. The width of this nanowire is 450 nm, 300 nm corresponds to the grown SiO_2 and 150 nm to the core Si. (c) SEM image of the suspended silicon nanowire at the end of the fabrication. Once the SiO_2 has been removed, the Si nanowire width is 72 nm for this batch of devices.

When a cross-section has to be done, it is important to assume that part of the removed material will be redeposited. This redeposit material could become a mask that precludes the SEM inspection of the section. In order to prevent this inconvenient, it is important to consider the ion beam scanning direction. The key is to start the ion milling far enough of the area to be investigated and finish it just in the place where the SEM inspection will take place. This method is very convenient to produce a fresh slice of material for the SEM analysis. In figure 8 redeposited materials could be clearly observed in the back of the section. The area to be investigated by the SEM (figure 9) is very clear and it is observed the gap of the suspended MEMS and the different layers that conforms the device. It is also observed waterfall effects that are artifacts created by the milling action because of the different sputter rates, hardness and atomic number that exhibit the different materials that conforms the final device and also for the topography of the surface. For this concrete example the curtain produced by the waterfall effects is not disturbing the SEM inspection of the desired area (figure 8). Otherwise, the strategy to prevent this effect consists on made the surface of the sample more homogeneous by depositing platinum or other high-Z material by FIBID before the ion milling.

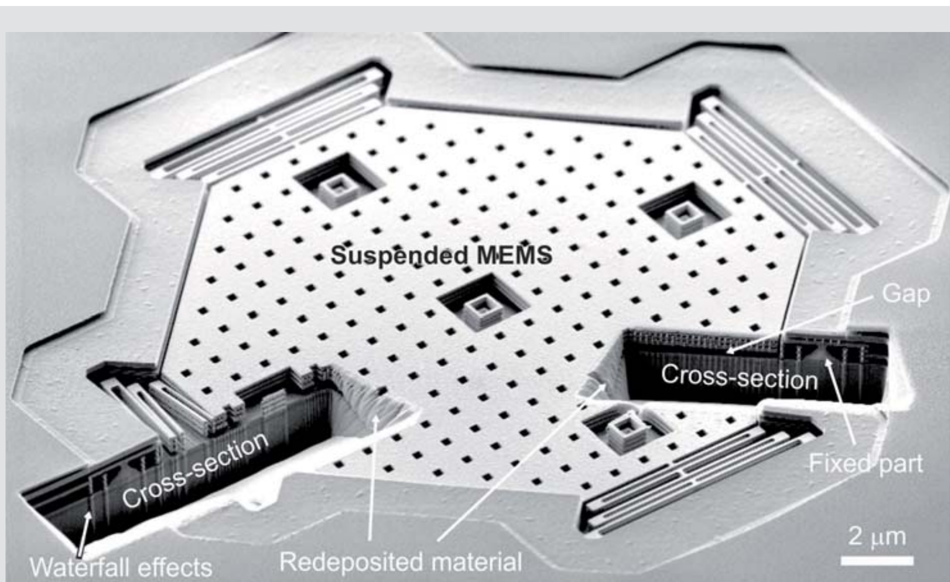

Figure 8. SEM image of two FIB cross-sections done in a suspended MEMS designed by Baolab Microsystems, S.L. In these cross-sections it is marked a gap that evidences the release of the device, the waterfall effects and the redeposited material that are artefacts introduced during the FIB cross-section processing.

The last characterization example shows a cross-section of a test structure of the Complementary Metal Oxide Semiconductor (CMOS) IMB-CNM technology (figure 9). To prevent the waterfall effects it is deposited by FIBID a layer of platinum to homogenize the surface of the sample (figures 9 a, c-d). Then the cross-section is done by ion milling. The SEM inspection shows very clearly the different parts of this technology. All the images presented in figure 9 have been performed by the In-lens detector. By tuning the SEM conditions it is possible to analyze the dimensions of small features as could be observed in figure 9b (low current, low voltage and small working distance) where it is possible to measure the thin gate dielectric layer. Increasing the SEM current it is possible to resolve the ion implanted volume that defines the source and drain regions despite the resolution loose as a consequence of using a high SEM current. The SEM current is defined by the selected aperture, the bigger the aperture is the higher the current is.

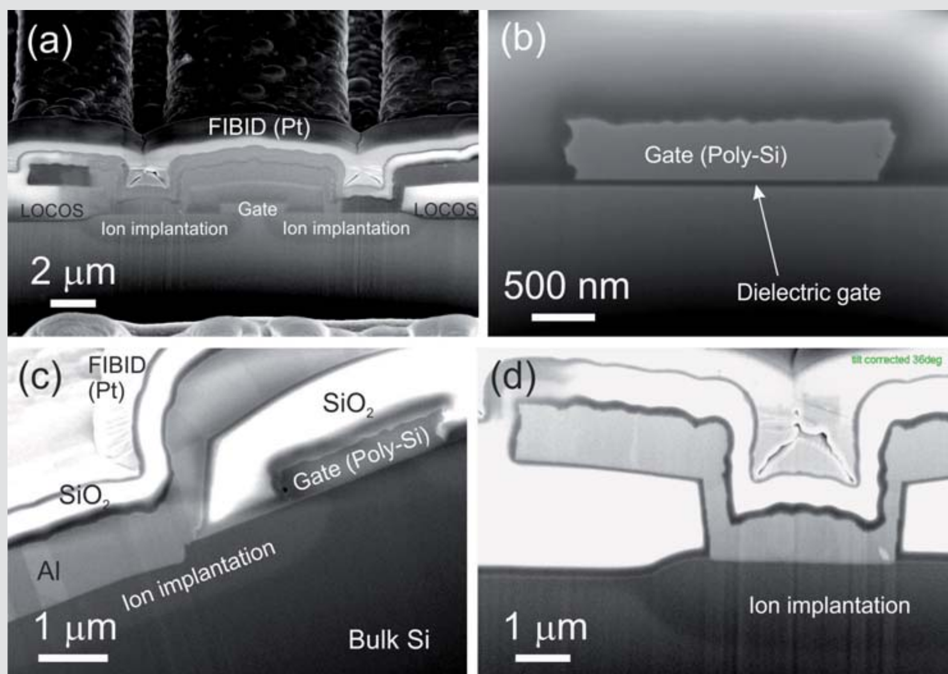

Figure 9. Four SEM images of a FIB cross-section of a CMOS test structure. In image (a) the ion implanted source and drain regions, the gate electrode, the local oxidation of silicon (LOCOS) insolating areas and the Pt-FIBID are observed. Image (b) is a high resolution SEM image that shows the 40 nm thickness of the dielectric layer that electrically insolates the gate electrode and the transistor channel. Rotated image (c) shows the grain structure of the aluminum layer, the ion implanted volume, the poly-silicon gate, the Pt-FIBID as well as the SiO_2 insolating regions that exhibit higher brightness. Image (d) indicates the 1.5 μm depth of the implanted regions in the contact zone.

2.4.2. On purpose device/sample transformation

In this section it is shown some of the applications developed with the aim of modify the behavior, the shape or the characteristics of a sample or a device. The first group of uses is related with **milling**, where the focused ion beam collides onto the sample and physical sputtering is produced. This subtractive method is commonly used for the production of nanostructures and has some peculiarities in comparison with other nanofabrication approaches: (i) in principle it is possible to mill any material,[1] (ii) it could be done without depositing any resist allowing the fabrication onto pre-patterned structures,[8–11] (iii) sub-5nm resolution can be achieved by depositing a sacrificial top layer of metal to overcome the Gaussian-like profile of the ion beam,[12] (iv) the throughput depends on the sputter rate of the materials of the sample and it is commonly slow. It could be enhanced by combining physical sputtering with chemical halogen-based species established for specific materials.[1]

The second group of applications evolves the **deposition** of selected materials. There are some materials developed to be locally deposited by the Crossbeam or other FIB workstations such as Pt,[13–15] C,[16] W,[17] Au,[18] SiO_2,[19]… that could be obtained from a gas, solid or liquid chemical precursor. The deposition is done assisted by ions, focused ion beam induced deposition (FIBID); or by electrons, focused electron beam induced deposition (FEBID). As an example, the deposition of Pt could be done induced by both beams (ion and/or electron). The reservoir is heated and the gas that contains the Pt, which is a metal-organic precursor trimethyl (methylcyclopentadienyl) platinum (IV) $MeCpPt^{IV}Me_3$, is introduced into the vacuum chamber very close to the desired position of the sample without raising the pressure significantly. The gas decomposes assisted by the energetic beam into Pt, that it is attached to the sample, and into volatile C and O. The precursor has to stick with sufficient probability to the sample surface and it has to decompose faster than the sputtering that it is produced by the energetic ion beam bombardment. If it is selected an ion beam the deposited material also contains Ga, C and O. FIBID and FEBID permits to deposit useful materials on almost any solid surface with very high spatial precision. They are employed for circuit editing because it permits the deposition of conductors and insulators. These techniques also are used to protect the sample surface during FIB micromachining for cross-section or TEM sample preparation (as shown in chapter 5) and they are very useful for scientific proposes as mass sensing experimentation.[15,20]

Finally, the ion beam could be used to **implant** (Ga^+ in the case of the Crossbeam) and to produce amorphization or damage locally to a sample or device. As it is explained in section 3 (figures 3 and 5), if it is used a high ion dose, then there is generated ion milling and ion implantation and amorphization/damage. In the case of working at lower doses,

then ion milling could be prevented and then only ion implantation and amorphization/ damage is produced. In chapter 3 there is exposed a new fabrication approach based on ion implantation for the definition of functional electrical and mechanical nanometric devices.

Milling

Next it is shown an approach for the fabrication of silicon nanowires or strips starting with a pre-patterned silicon membrane that is suspended between two metallic heaters (figure 10a). Part of this work, done by the GNaM group (Grup de Nanomaterials i Microsistemes, UAB) with the collaboration of the author of this thesis, has been published here.[10] This work demonstrates that the FIB technology is very convenient to fabricate nanostructures with high resolution and reproducibility and, as it is a resist-free approach and no resist has to be spin-coated, it is an appropriate method to pattern onto samples with abrupt slopes (figure 10b).

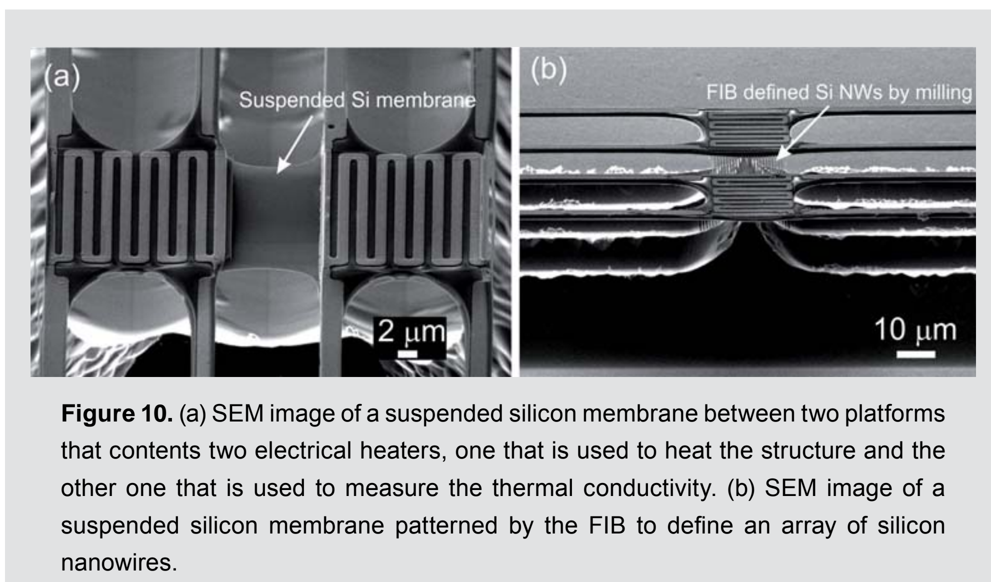

Figure 10. (a) SEM image of a suspended silicon membrane between two platforms that contents two electrical heaters, one that is used to heat the structure and the other one that is used to measure the thermal conductivity. (b) SEM image of a suspended silicon membrane patterned by the FIB to define an array of silicon nanowires.

FIB technology permits to pattern directly onto the sample by milling with high accuracy in the control of the beam. In the framework of the CHARPAN EU project, among the research activities, we also worked on testing and giving feedback in the development of FIB modelling software to enhance the fabrication capabilities by taking into account the redeposition effect. Figure 12 shows a rose micro-fabricated by ion milling with the help of Ion Rev Sims[21] software where it is resolved with high definition minimizing silicon redepositions.

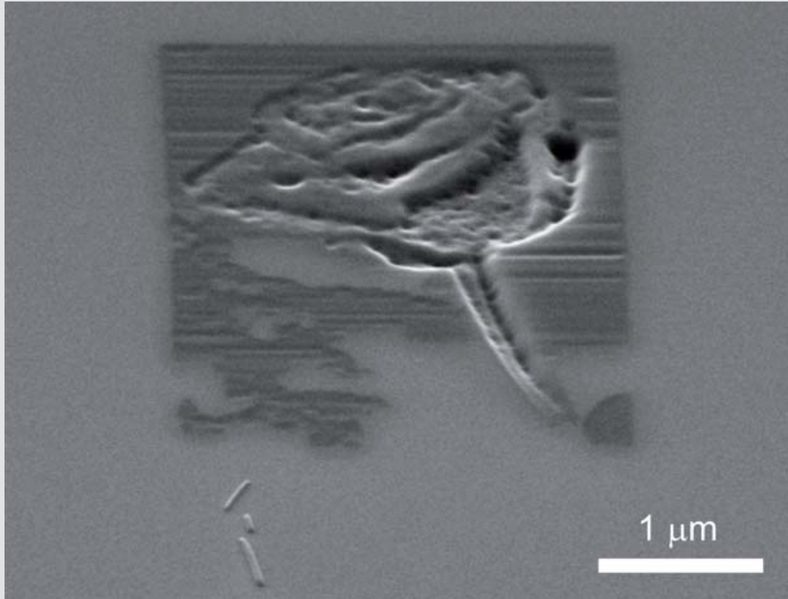

Figure 11. SEM image of a three dimensional pattern milled onto a silicon chip. The pattern has been generated from a grey scale picture of a rose.

Deposition

Apart of milling we also worked on the applicability of the Ion Rev Sims software to fabricate three-dimensional structures grown by FIBID of SiO_2 (precursors name: 2,4,6,8,10-pentamethyl-cyclopentasiloxane). In this case the software has not been employed to overcome the redepositions produced during the ion milling. Here it is used to convert a grey scale bitmap image into a .gds file transforming each individual pixel into layers. Figure 12 presents the old version of the Institut Català de Nanotecnologia (ICN) logo (inset figure 12) and a 45 degree tilted SEM image of their small dimensional version done by FIBID (figure 12).

Figure 12. SEM image of a three dimensional pattern defined by FIBID deposition of Pt onto a silicon chip. The pattern has been generated from a grey scale picture the ICN logo.

The fabrication of microelectronic devices supposes the employment of a large number of process steps. It is feasible to edit by the Crossbeam previously fabricated devices. In figure 13 there is an example of circuit editing. The edition consists of two parts. First of all it is cut an undesired metal line by FIB milling (figure 13a). For the second part it is opened a trench in the insulator material that passivates the metal connection by FIB milling. Then, by FIBID it is deposited Pt to fill the trench and to connect the metal line with the desired metal pad (figure 13b).

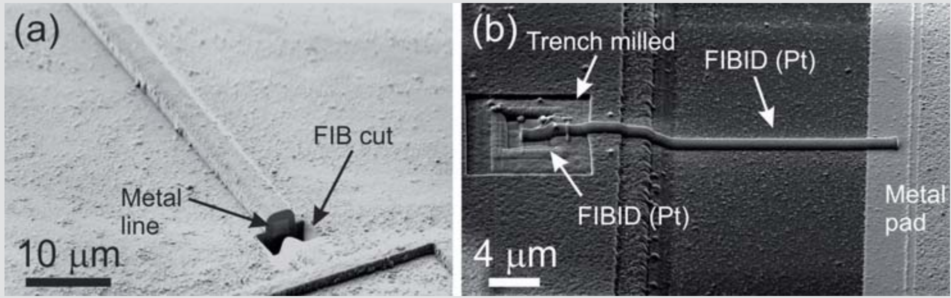

Figure 13. (a) SEM image of a metal line and its passivation cut by FIB. (b) SEM image of a platinum metal connection fabricated by FIBID that connects the trench opened on the passivation (allowing the access to the metal line) and a metal pad.

The next example illustrates the applicability of FIBID deposition as a tool to improve the mechanical anchor of a multiwall carbon nanotube (CNT) onto an etched SiO_2 layer (figure 14). As it is a resist-free method, it is feasible to deposit Pt onto samples that contain poorly attached devices. In order to prevent damaging the CNT, the valve of the precursor gas has been opened 30 seconds before the FIBID. Then, a small box of 300 x 300 nm^2 has been defined and a 15 seconds deposition at very low ion current (1 pA) has been done. It is worth to say that SEM imaging has not been performed (electron beam blanked) during the deposition process to prevent depositing Pt randomly through the image area.

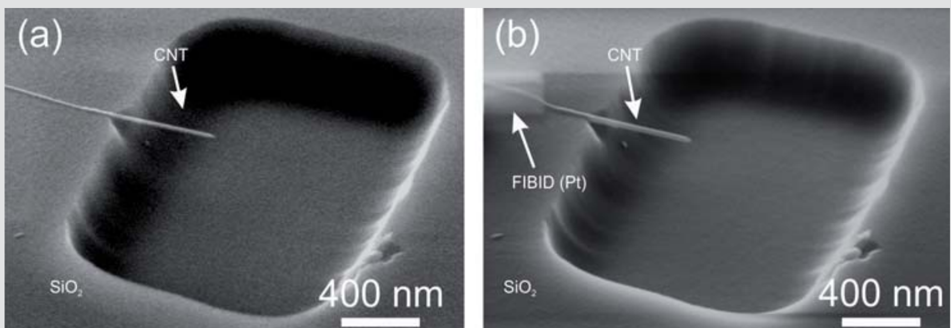

Figure 14. (a) SEM image of a CNT that is suspended from one of its sides over a pre-patterned cavity onto a SiO_2 layer. (b) SEM image after the deposition of a 300 x 300 nm^2 square of Pt deposited by FIBID to fix the CNT.

We have been successfully used FIBID and FEBID for the fabrication of Pt connections for electrical measurements on CNTs[22] and for mass experimentation, where an amount of mass has been deposited onto fabricated MEMS and NEMS. The mass change propitiates a shift of the resonant frequency of the device that has been detected electrically for different type of devices.[15,20]

Implantation/local damaging

As it is explained previously, when the ions hit the sample at higher doses ion milling is produced. Moreover, as a result of the ion bombardment and directly related with their energy, the first nanometers in depth of the fabricated structure becomes implanted (figure 3), damaged and amorphous in case of crystalline materials. Depending on the sputter yield of the sample material, there is a threshold value below which milling is not produced.[1,23] In this irradiation regime it is only produced a certain grade of ion implantation and damage as a function of the dose employed. In the next chapters it is presented a new fabrication approach based on FIB implantation and the material and device characterization.

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Chapter 3 Fabrication, characterization and optimization of silicon suspended nano-structures by FIB implantation

3.1. Introduction

In this chapter it is presented a top-down fabrication approach developed during this thesis that boosts the capabilities of FIB for the achievement of electromechanical functional devices. This fabrication technique is based on the use of the FIB as a tool to modify the silicon surface in order to change their properties locally. The fabrication method consists on only three steps: i) ion implantation; ii) silicon etching; and iii) annealing in boron environment. The structures are defined in the first stage (i) where focused ion beam implantation becomes the lithographic technique of this approach. It is important to note that the lithography is done without using any resist. It is especially useful when the sample to be processed has some topographic pre-patterns.

As it is explained in the previous chapter, FIB is often used to etch (**mill**) directly onto the sample or to locally assist the **deposition** of small amounts of material. In the case of milling, it could be understood as the lithographic equivalent of using a bright field mask with a **negative resist** to etch silicon. In other words, the exposed pattern is the volume to be removed (figure 1).

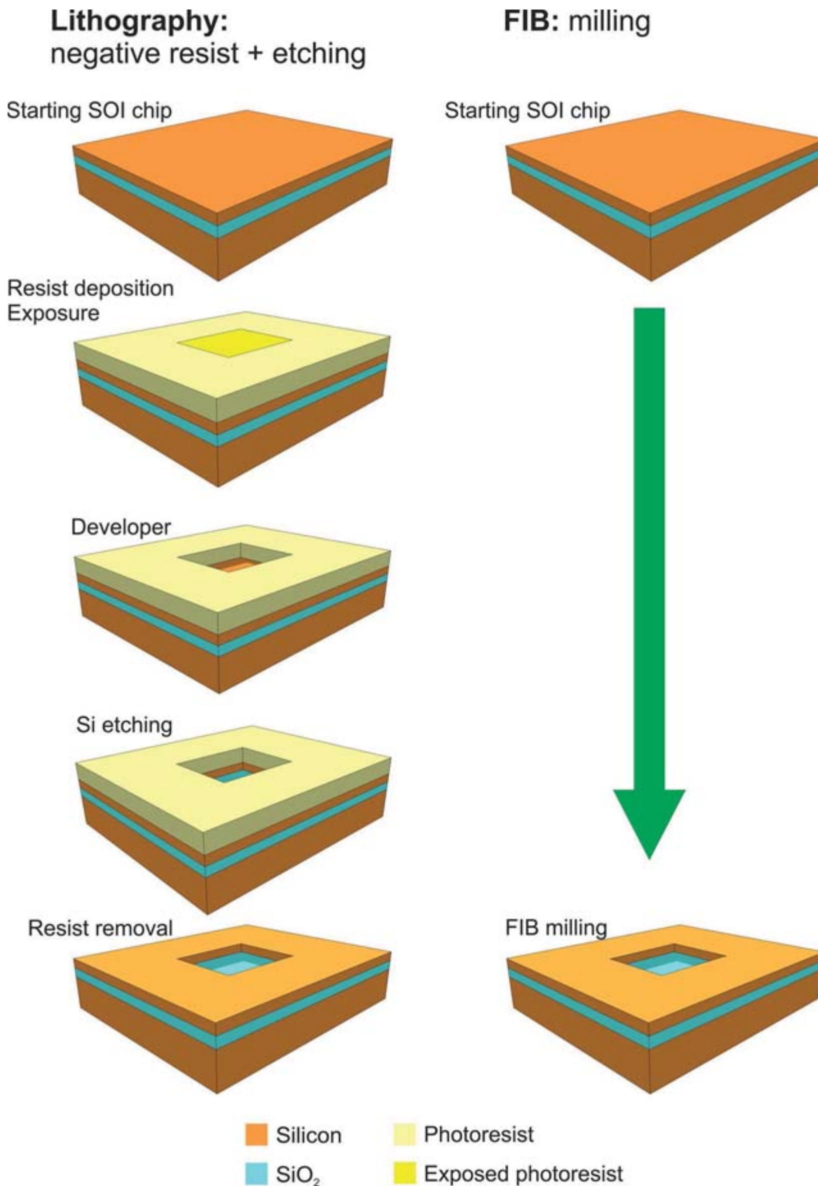


Figure 1. Schematic representation of (left column) photolithography process with a negative resist for an etching step for silicon, (right column) equivalent procedure performed by FIB milling.

On the other hand, the use of FIB to **implant** or modify the silicon surface for a subsequent silicon etching is the lithographic equivalent of using a bright field mask with a **positive resist** for an etching process. It means that the ion implantation is used to define directly the nanostructure and the electrical connections and the non-irradiated silicon corresponds to the etched or removed material. In other words, the exposed pattern is the remaining material (figure 2).

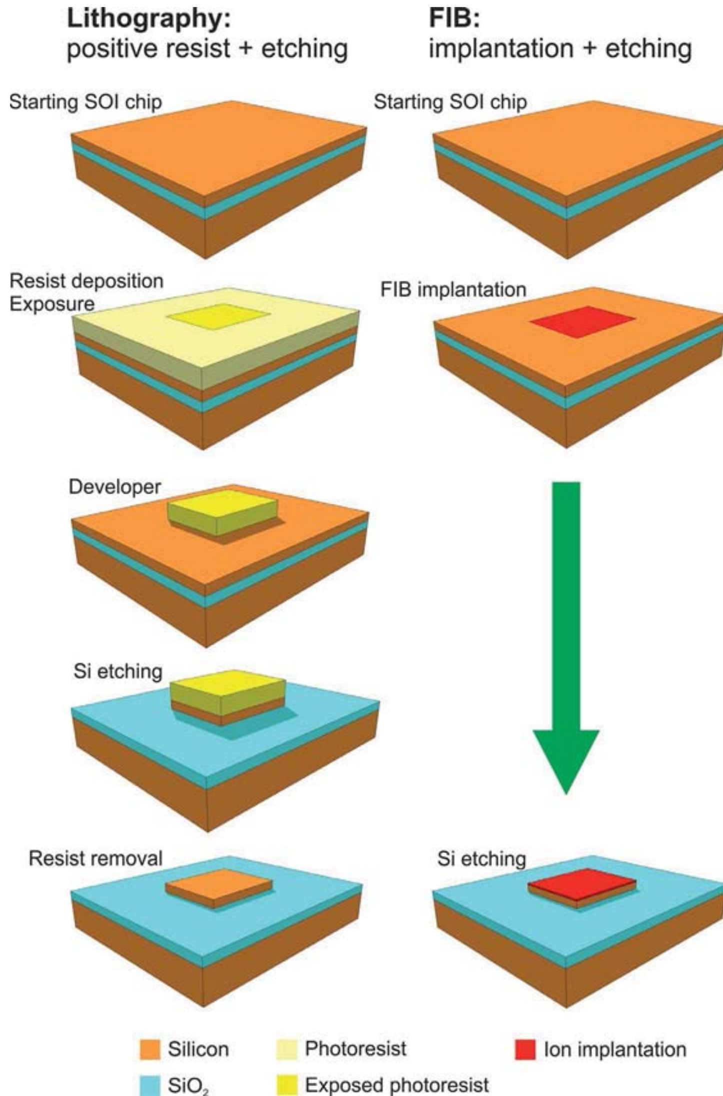


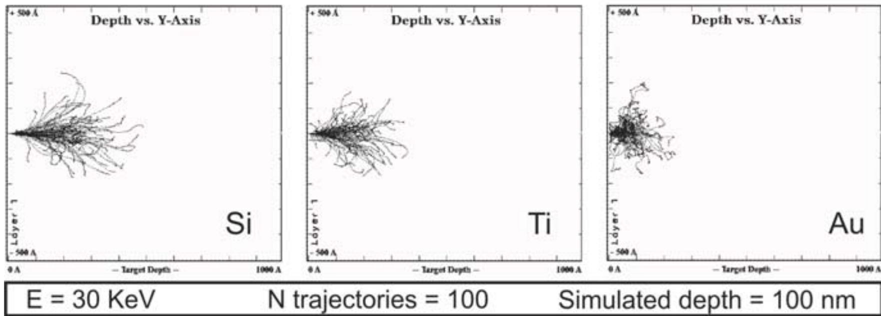
Figure 2. Schematic representation of (left column) photolithography process with a positive resist for an etching step for silicon, (right column) equivalent procedure performed by FIB implantation for creating a mask for the subsequent silicon etching step.

Our previous studies have been oriented on the investigation and fabrication of NEMS by ion beam milling and the integration of ion beam processing with CMOS technology.[1–3] It has been also demonstrated the compatibility of FIBID of Pt with fabricated NEMS structures integrated with CMOS technology.[4] These works have been done in the framework of the Charged Particle Nanotech (CHARPAN) FP6 EU project.

In this chapter it is presented the fabrication procedure used to obtain functional electro-mechanical suspended nanometric devices, the material characterization performed during the fabrication and at the accomplishment of functional devices as well as some early electrical and electromechanical results. This achievements have been published in this paper[5] that is presented in section 3.2 of this chapter.

Section 3.3 is focused on the optimization of the fabrication method presented in the previous section and the principal conclusions are published here.[6] First of all, ion implantation is studied. It is simulated the trajectory of gallium ions onto the silicon by the software SRIM[7] (The Stopping and Range of Ions in Matter) for the implantation conditions employed for the fabrication of the devices and also it is studied the ion dose and their etching selectivity. In figure 3 it is presented the trajectories of gallium ions into three different target materials (Si, Ti and Au) and for three different acceleration energies (5, 15 and 50 KeV) into Si. Secondly, the under-etching profile produced by the anisotropic wet etching is also optimized by two different design strategies applied during the ion implantation step. On the one hand, the first approach proposes the fabrication of sustaining posts to prevent the sticking of long and narrow structures. On the other hand, by the design and definition of compensation strips, it is possible to prevent the overhangs produced by the under-etching. Finally, there are presented devices of complex geometries fabricated by this technique. It is shown the electromechanical transduction and the electrical conductivity enhancement produced by the high temperature diffusive boron doping that is presented in the previous chapter.

Ion range of different elements



Increasing the energy

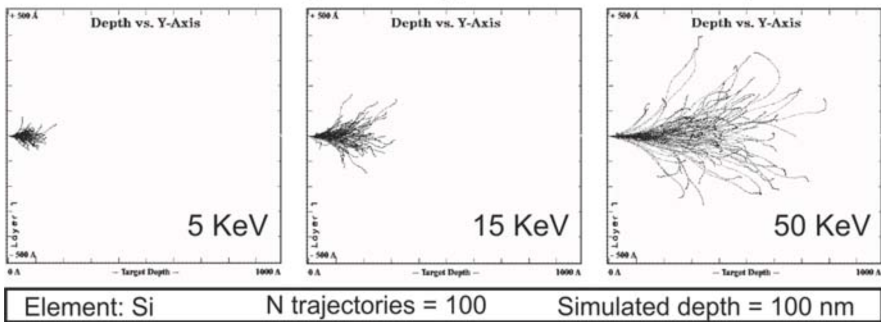


Figure 3. Simulations of gallium ion trajectories done by the stopping and range of ions in matter (SRIM version 2013.00) software. These simulations show (on top) the penetration depth and lateral trajectories of the ions for different materials (silicon, titanium and gold) and their trajectories into silicon as a function of the ion energy (bottom).

All the devices presented in this chapter, as well as the devices presented in next chapters, have been defined by direct ion implantation by FIB in the framework of the Single Nanometer Manufacturing (SNM) FP7 EU project. Therefore, in the FIB implantation step it is patterned the design, shape and dimension of the nanostructures in a two-dimensional manner taking into account that, at the end of the fabrication process, the systems will be released exhibiting three-dimensional features. In figure 4 it is presented three different fabricated devices illustrating (i) the **high resolution** of this technique where the minimum diameter reached for released devices corresponds to 10 nm (figure 4.a), (ii) the design **flexibility** to fabricate complex geometrical shapes (figure 4.b) and (iii) the **reproducibility** to fabricate identic devices as the eight nanowires (4.3 μm length, 100 nm width and 40 nm thickness) in series of figure 4.c. The optimization of

the parameters involved in this fast and flexible fabrication approach permits to obtain different kind of devices that can be oriented to specific applications as NEMS[8] (chapter 4), FETs and SHoTs[9] (chapter 5).

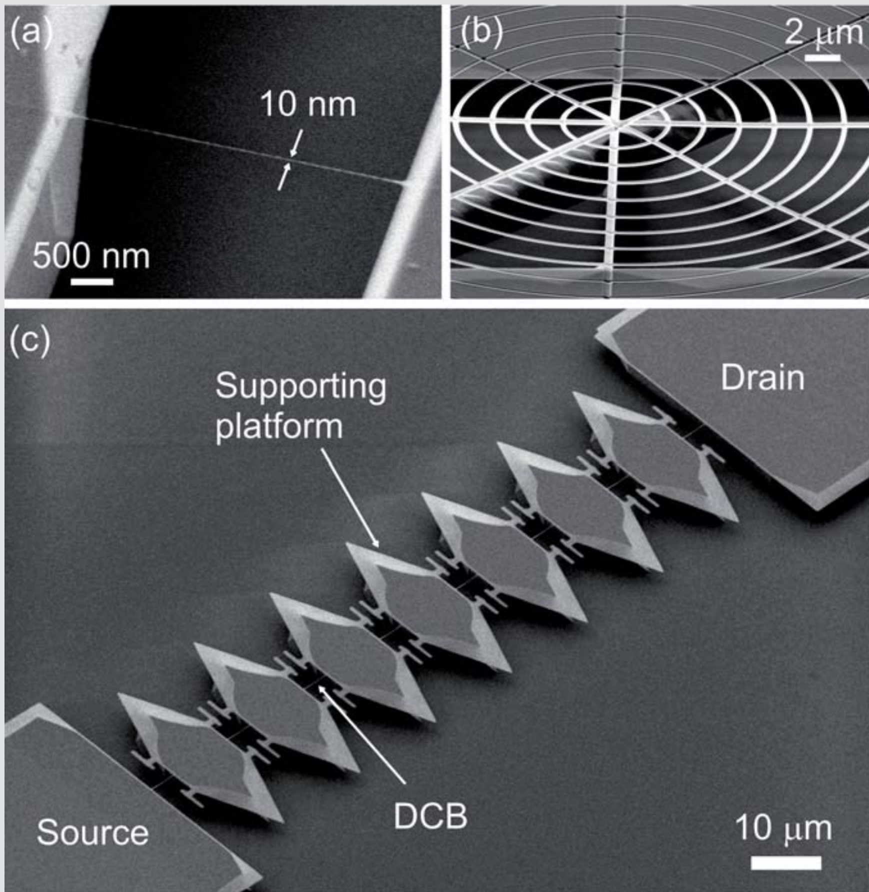


Figure 4. 45 degree SEM tilted images of different silicon suspended devices fabricated by the approach presented in this chapter onto SOI substrates. (a) SEM image of a 4.3 μm length and 10 nm diameter suspended silicon nanowire. (b) SEM image of a suspended silicon spider-web that consists on concentrically circular wires supported by straight wires. (c) Array of eight suspended silicon doubly clamped beams (DCBs) configured in series and supported by the source and drain electrodes and seven supporting platforms.

Once the devices are fabricated, they could be measured in a probe station. It is also possible to bond the devices in a printed circuit board (PCB) as shown in figure 5a and 5b or on a chip package (figure 5c).

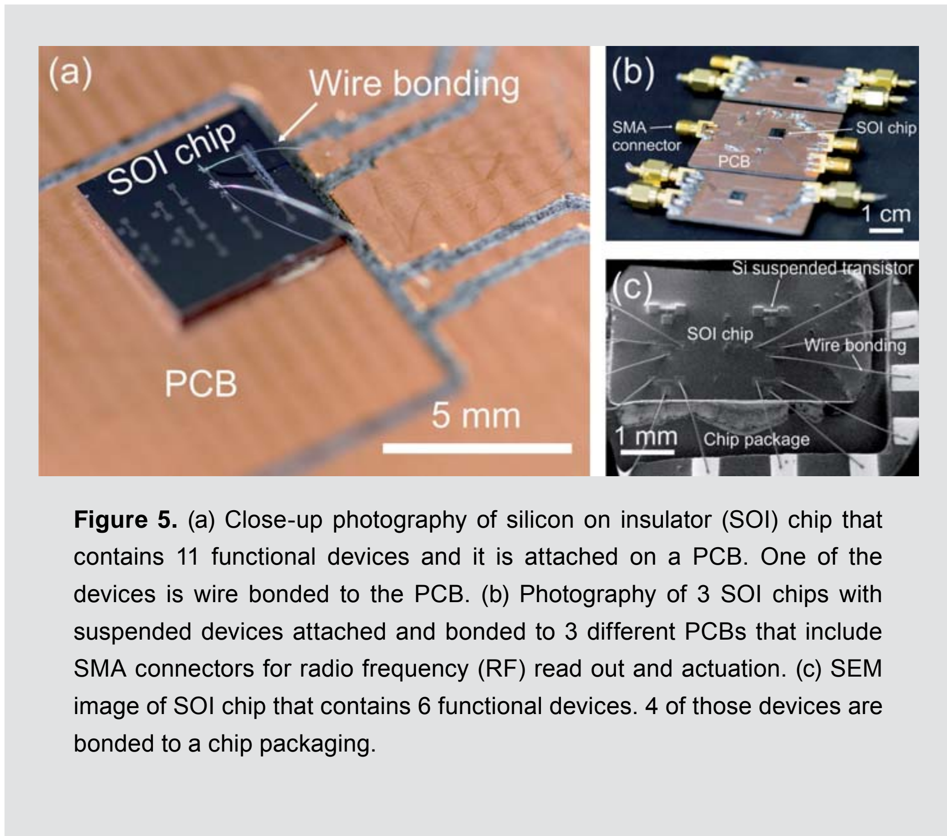


Figure 5. (a) Close-up photography of silicon on insulator (SOI) chip that contains 11 functional devices and it is attached on a PCB. One of the devices is wire bonded to the PCB. (b) Photography of 3 SOI chips with suspended devices attached and bonded to 3 different PCBs that include SMA connectors for radio frequency (RF) read out and actuation. (c) SEM image of SOI chip that contains 6 functional devices. 4 of those devices are bonded to a chip packaging.

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3.2. Enabling electromechanical transduction in silicon nanowire mechanical resonators fabricated by focused ion beam implantation

This section has been published in Nanotechnology:
Llobet, J., Sansa, M., Gerbolés, M., Mestres, N., Arbiol, J., Borrisé, X. & Pérez-Murano, F. Enabling electromechanical transduction in silicon nanowire mechanical resonators fabricated by focused ion beam implantation. Nanotechnology 25, 135302 (2014).

http://dx.doi.org/10.1088/0957-4484/25/13/135302

3.3. Fabrication of functional electro-mechanical nanowire resonators by focused ion beam (FIB) implantation

This section has been published in the Journal of Micro/Nanolithography, MEMS, and MOEMS:

Llobet, J., Gerbolés, M., Sansa, M., Bausells, J., Borrisé, X. & Pérez-Murano, F. Fabrication of functional electromechanical nanowire resonators by focused ion beam implantation. J MicroNanolith MEMS MOEMS 14, 031207 (2015).

http://dx.doi.org/10.1117/1.JMM.14.3.031207

Chapter 4 Nanoelectromechanical Systems

This chapter starts with a brief introduction to Microelectromechanical systems (MEMS) and Nanoelectromechanical systems (NEMS). There are presented the different setups used to measure the mechanical transduction of the fabricated devices and the principal results. It is also introduced an ongoing work that consists on the combination of MEMS and NEMS. Finally, it is presented our published work focused on the enhancement of the electromechanical transduction by engineering the asymmetry of the devices.

4.1 Introduction to NEMS

MEMS and NEMS are miniature devices that transduce a mechanical or electrical energy into an electrical or mechanical one respectively. NEMS are the natural evolution for MEMS towards the nanoscale. We talk of NEMS when two of the three dimensions of the structure are reduced to the nanometric range. The reduction of the dimensions permits new functionalities.

An electromecanical system usually can operate as a sensor or as an actuator. Sensors and actuators can be used as an interface that senses or interacts with the physical world. We talk of sensors when the mechanical part senses an external force (acceleration, pressure, vibration…) and it is converted to an electrical signal that can be measured. In the case of actuators a supplied electrical signal is the responsible of the movement of the mechanical part.

MEMS are used in aeronautics,[1] in the automotive industry as micro-accelerometers, gyrometers, magnetometers, airbag sensor and for gaming or mobile phones. Microactuators[2] are used in video projectors, microphones, micropumps for medical fluidic applications. In the field of energy generation, piezoelectric MEMS can harvest energy from the mechanical vibrations that could be used as the power source of other miniaturized devices.[3]

NEMS are an emerging technology. Miniaturization enhances the sensitivity to external stimulus, contributing to the development of biochemical analysis applications,[4] force sensors,[5] ultrasensitive mass sensors.[6–8] For instance, it is measured a shift in frequency produced by the attachment of a molecule. Otherwise, for mass sensing applications other phenomena appears that alters the measurement performed like a change in the rigidity of the resonator or changes in the electrical conductivity.[9] They are candidates for measuring the air quality and for biomarkers identification.[10] Among their promising functionalities NEMS can be used as transistors or mechanical switches and logics.[11] In chapter 5 it is presented our results related with the fabrication of single hole transistors that are potential candidates for the fabrication of low power consumption transistors.

NEMS and MEMS can convert mechanical energy provided by an external force at very high frequencies and small amplitudes in readable signals. At this point, two different device configurations can be considered. On the one hand, devices or nanowires clamped only by one of its ends (cantilevers) and, on the other hand, devices or nanowires anchored by both ends denoted as doubly clamped beams (DCBs). There are five mainly readout techniques successfully used in the last years that are important to take into account in order to detect the mechanical motion of the devices:

Optical detection: This detection method is used for the measurement of the deflection of cantilevers and DCBs. By this method, it has been achieved the detection of small devices as silicon nanowires.[9] This method is not suitable for measurements on integrated systems or the detection of mechanical actuations out of the lab because of the use of advanced optical setups and the difficulties to measure inside packaged devices. The AFM technology uses an optical detector device (photodetector) to sense the reflection of a laser beam onto the cantilever of the tip of the AFM in order to measure the deflection of the cantilever during the sample surface scanning.

SEM detection: As it is explained below, if the movement of the device is large enough (more than 10 nm) it could be used an SEM to measure the movement of the NEMS.[12] For that, the device has to be excited at their resonant frequency by an electrostatic force applied close to the device.

Piezoelectric detection: The first element needed is a piezoelectric material to transform the mechanical movement into an electrical signal. The mechanical movement produces the internal generation of electrical charge or vice versa[3,13]. There are some materials that exhibit piezoelectricity, for example AlN, GaN, ZnO, lead-zirconate-titanate (PZT), $BaTiO_3$.

Capacitive: In this method it is needed two electrodes, the first one is the mechanical element and the second one the sensing electrode. The movement of the mechanical part

produces a change in the capacitance between the two electrodes.[14,15] This mechanism is compatible with large scale integration.

Piezoresistive: When a material changes its electrical resistance because of a mechanical deflection it is called piezoresistance. The gauge factor is the ratio between the relative change in the resistance and the strain. This method is wildly used because of the piezoresistive properties of silicon and polysilicon.[16–23] This method is also compatible with large scale integration.

4.2 Electromechanical characterization

The mechanical transduction of the NEMS fabricated during this thesis have been measured by different setups. Next, are described the setups and some of the obtained results are shown.

4.2.1. Electrostatic actuation and SEM detection

It consists on the electrostatic actuation using an electrode located very close to the suspended device. This characterization is performed inside the Crossbeam vacuum chamber. To detect the motion of the device, it is used the SEM. The excitation electrode is one of the tungsten electrical probes installed inside the Crossbeam vacuum chamber. The distance between the electrode and the device can be easily tuned with the ultra-high precision piezo-motor (0.25 nm according to the manufacturer) of the nanomanipulator. The excitation signal applied to the electrode is sweep at high frequency at a maximum voltage of 10V pp supplied by the Function/Arbitrary/Pulse Generator TG5011 (Aim-TTi). As it is demonstrated in figure 1, the motion of the devices is large enough to be detected by the SEM images. The two great advantages of this setup are their simplicity and the possibility to measure on not conductive devices. The main disadvantages are the impossibility to perform the measurements on integrated systems and the needed of an expensive setup.

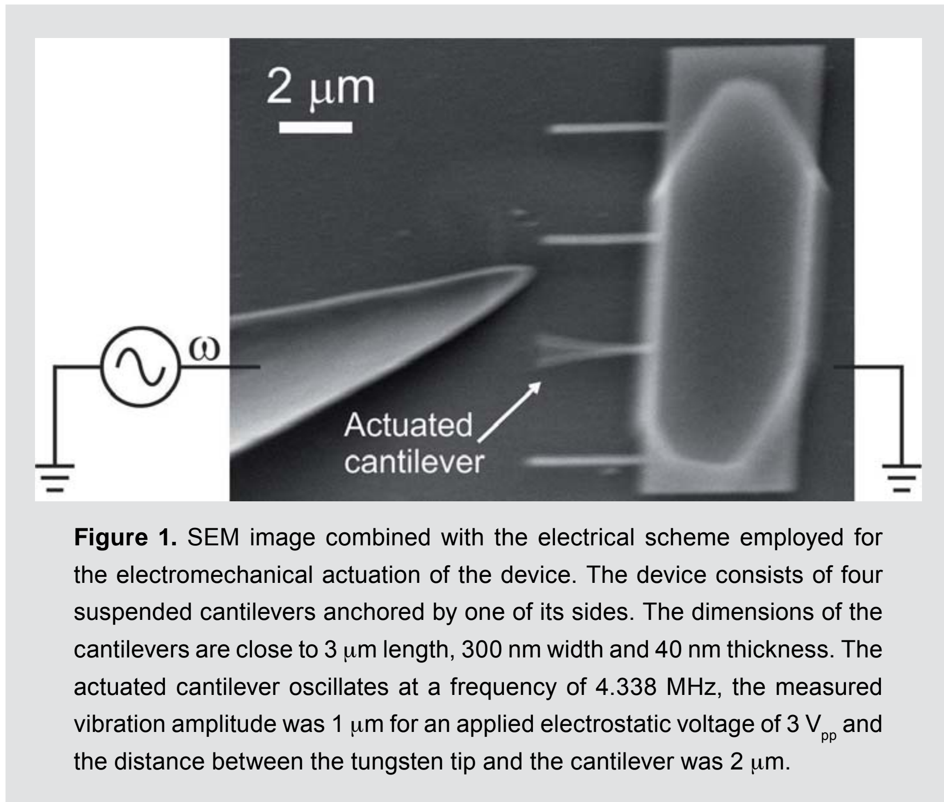

Figure 1. SEM image combined with the electrical scheme employed for the electromechanical actuation of the device. The device consists of four suspended cantilevers anchored by one of its sides. The dimensions of the cantilevers are close to 3 μm length, 300 nm width and 40 nm thickness. The actuated cantilever oscillates at a frequency of 4.338 MHz, the measured vibration amplitude was 1 μm for an applied electrostatic voltage of 3 V_{pp} and the distance between the tungsten tip and the cantilever was 2 μm.

We have fabricated cantilevers on a silicon chip by the approach presented in chapter 3 is based on FIB implantation and wet etching. The motivation of this study is to characterize the resonant frequency of the devices obtained by this method in order to compare the mechanical properties with the theoretical ones.

To perform the study they have been successfully fabricated devices of:

- 300 nm of width, 40 nm of thickness and 1.5 μm of length.
- 300 nm of width, 40 nm of thickness and 2 μm of length.
- 300 nm of width, 40 nm of thickness and 2.5 μm of length.
- 300 nm of width, 40 nm of thickness and 3 μm of length.

The characterization setup is based on applying a high frequency voltage through the probe of the manipulator at close proximity of the cantilever, as explained in figure 1. For the electrical excitation, we used the signal generator connected to an electrical probe and for the characterization of the resonant response SEM imaging has been used. Figure 2a corresponds to a SEM image of a cantilever and the electrical probe. When the electrical excitation setup is turned on, the generated electrical field interacts with the electron beam and the SEM image becomes blurred (figure 2b and 2c). Even though it is

clearly determined the resonant frequency of the device as it is demonstrated in figure 2c (cantilever that vibrates) and 2b (cantilever that does not vibrate).

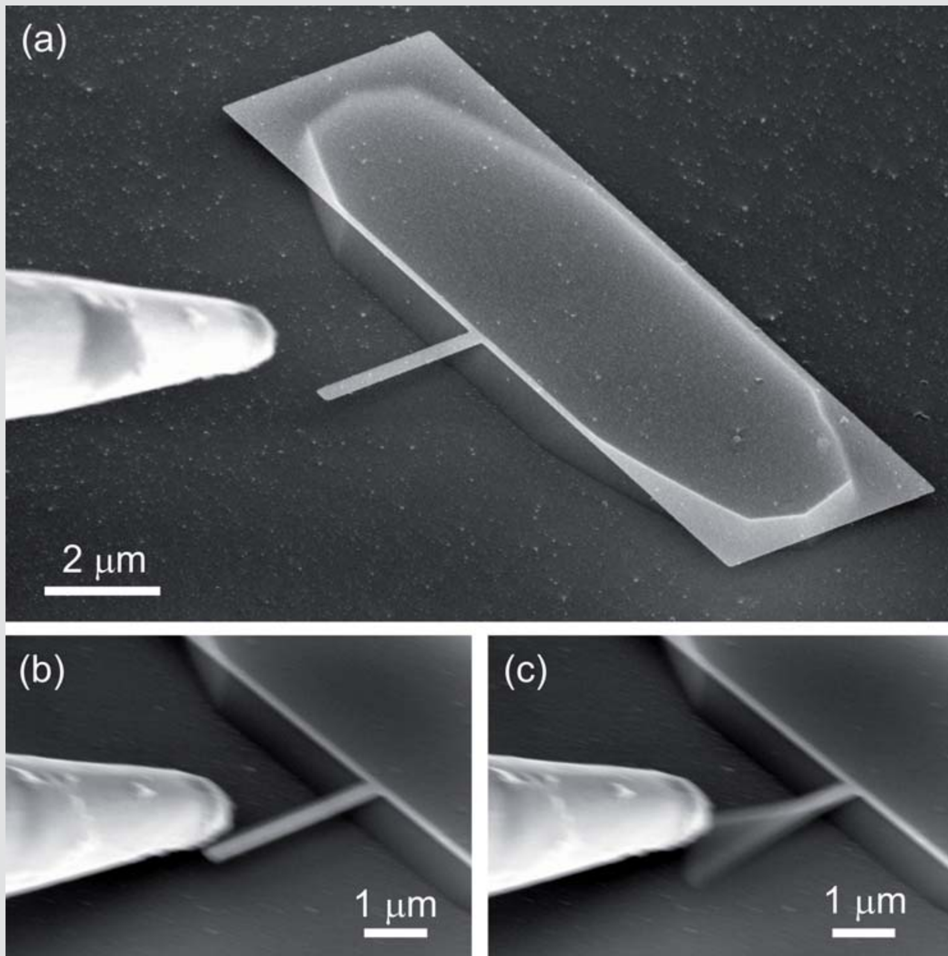

Figure 2. Three SEM images of a 3 μm length, 300 nm width and 40 nm thickness single silicon suspended cantilever and the tungsten electrical probe used for the electrostatic actuation. (a) SEM image of the cantilever without the application of any voltage through the electrical probe. (b) SEM image of the cantilever when a 3 V_{pp} electric field at 4.248 MHz is applied (out of resonance). (c) SEM image of the cantilever oscillating at their resonant frequency when it is applied a 3 V_{pp} electric field at 4.436 MHz.

In table 1 and figure 3 are summarized the experimental results of resonant frequency as a function of the device length. In that graph, it is represented the maximum and minimum measured values for the 4 different selected lengths and the theoretical values obtained from this formula that is an approximation expression extracted from the Euler-Bernoulli equation:[24]

$$f_0 \approx 0.16 \frac{t}{l^2} \sqrt{\frac{E}{\varphi}}$$

Where f_o is the resonant frequency of the cantilever, *t* represents the thickness of the device, *l* is the length, *E* corresponds to the silicon Young Modulus and φ the density of silicon. For this calculation, it is considered a Young Modulus of 68 GPa[25] and a density of 2330 Kg/m^3. The Young Modulus for ultrathin materials is not exactly the same than the exhibit for their bulks, as it is described in previous works.[25,26] As it is observed in the previous formula, by reducing the length of the device the resonant frequency is highly increased. In figure 3 it is observed a good agreement between the measured devices and the theoretical resonant frequency.

Device lenght (μm)	Minimum resonant frequency measured (MHz)	Maximum resonant frequency measured (MHz)
1.5	15.284	15.320
2	8.832	8.840
2.5	5.824	5.850
3	4.512	4.338

Table 1. Measured resonant frequencies for different cantilever lengths.

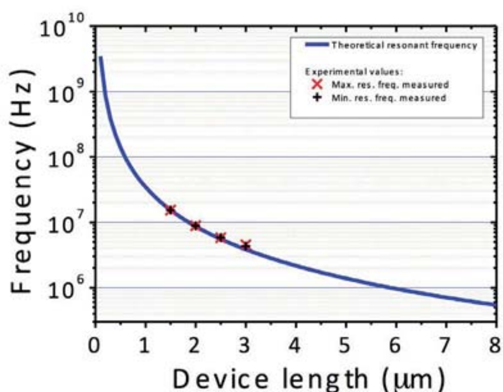

Figure 3. Theoretical (continuous line) and experimental values (crosses) of the resonant frequency of the cantilevers as a function of the device length. The theoretical values are calculated for devices of 40 nm thickness and 300 nm width. The cross marks summarizes the experimental measurements over 20 different devices, where the red and black crosses represents the maximum and minimum resonant frequencies measured respectively.

This method has also been employed to measure the transduction of suspended DCBs (figure 4). The movement obtained for this device configuration is much smaller than in the case of cantilevers. The maximum measured deflection for a 3.2 μm length DCB has been in the order of 50 nm (figure 4b), which is a smaller value than the 1 μm deflection detected for a 3 μm length cantilever (figure 3c). Because of the applied electrical field, the SEM image appears blurred or noisy (figure 4a). This artifact avoids the detection of small movements. For that reason this measurement setup is preferred for the measurement of cantilevers instead of DCBs.

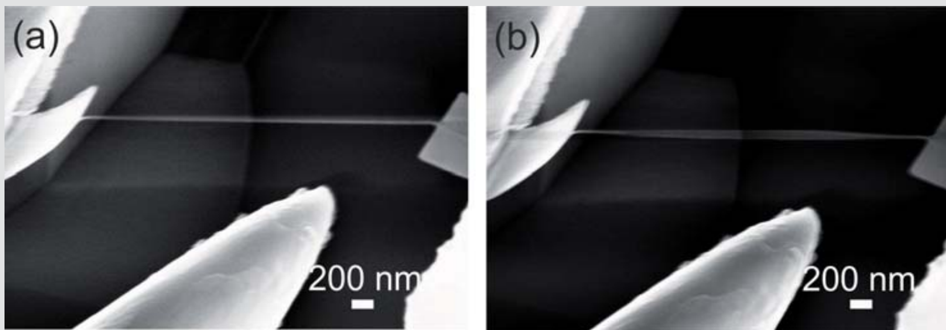

Figure 4. Two SEM images of a silicon DCB anchored by two silicon membranes to two metal electrodes. A tungsten electrical probe is used to electrostatically actuate the DCB. (a) SEM image of the DCB at rest. (b) SEM image of the DCB oscillating at 40 MHz.

4.2.2. Electrostatic actuation and piezoresistive detection

In this section, three electrical detection methods for measuring the vibration of electrostatically actuated DCBs are presented. It is measured the change in the electrical resistance produced by the movement of silicon DCBs (piezoresistive detection) when it is actuated by an external force. The piezoresistance is quantified by the gauge factor (G) $G = (\Delta R/R_0)/(\Delta l/l_0)$ that is the variation of electrical resistance ($\Delta R/R_0$) as a function of the elongation of the device ($\Delta l/l_0$). There is also a geometric increase of the resistance because of the decrease of the device cross-section and the increase of its length. For piezoresistive materials, as Si, with a relatively high gauge factor, the geometric effect is neglected.[16]

The electrical detection is performed by down-mixing radio-frequency methods, in which the high-frequency-transduced signal arising from the motion of the resonator is transferred to lower frequencies, and then detected using a lock-in amplifier. Three electrical detection set-ups based on three different down-mixing methods have been

established in our group[20]: the FM demodulation (figure 5a), the two-sources - 1ω (figure 5b) and the two-sources - 2ω.

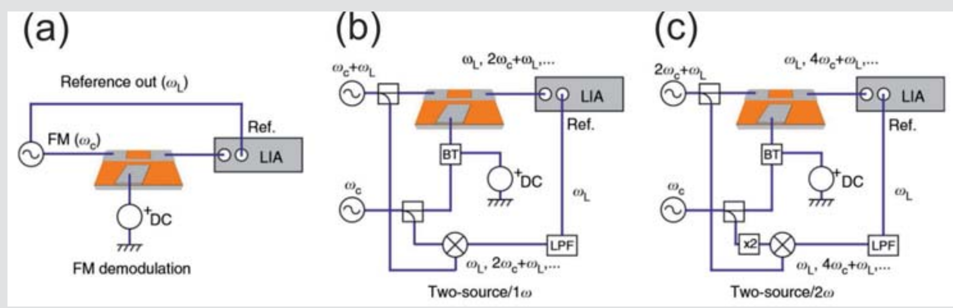

Figure 5. Schematics of the three electrical detection methods based on the electrostatic actuation and piezoresistance detection implemented by our group (source[20]). (a) FM detection method. (b) Two-source/1ω detection method. (c) Two-source/2ω detection method.

The first setup is the Frequency Modulation (FM) down-mixing method (figure 5a) that we successfully employed in[20–22] and it is used for the electromechanical results presented in chapter 3. The first element of the setup is the computer that is used to control, by general-purpose instrumentation bus (GPIB), all the instrumentation needed for the measurements. In this setup it is applied an FM-modulated signal to the nanowire of the form $V(t) = V \cdot \cos(\omega_c t + (\omega_\Delta/\omega_L) \cdot \cos(\omega_L t))$ where ω_c is the carrier frequency, ω_L is the low frequency of the modulated signal and ω_Δ is the frequency deviation. The nanowire is excited into motion electrostatically by the carrier frequency (ω_c) component of the FM signal (Agilent E8257D) combined with a DC voltage (Agilent E3631A) applied to the gate electrode. The current through the nanowire is demodulated by the change of electrical resistance because of the nanowire motion. The resulting signal has a component at low frequency which contains information about the motion of the device and it is detected using a lock-in amplifier (Signal Recovery 7280 DSP). These measurements have been successfully performed inside the Crossbeam chamber[21] and also in the vacuum chamber that is part of the setup developed by our group and it is used exclusively for the electromechanical characterization.

The second method presented is the called two-sources – 1ω (figure 5b). Here it is also used a computer to control all the setup by GPIB. It is used 3 different power sources, 2 corresponding to high frequency wave generators and 1 DC source. Source 1 is a wave generator (Agilent E8257D) that used to generate the signal that passes through the nanodevice and to generate a reference signal for the lock-in amplifier. Source 2 is a wave generator (Agilent N5181A) that it is connected to a DC source (Agilent E3631A) by

a bias-tee. They are used to produce an excitation signal for the nanodevice through the gate electrode. The Lock-in amplifier (Signal Recovery 7280 DSP) compares the signal at the device output with the reference signal. The RF circuitry is composed by the following types of elements: bias-tee, frequency doubler and frequency mixer (Mini-circuits). Inside the vacuum chamber there is the device wire-bonded to a PCB and connected to the measurement setup through the vacuum feedthroughs. The electrical setup presented for the electromechanical measurements has also been connected successfully to the Crossbeam. This method is described in detail in the chapter section called "Tuning piezoresistive transduction in nanomechanical resonators by geometrical asymmetries".[23]

The third method presented is the called two-sources – 2ω (figure 5c). From the instrumentation point of view, this method is quite similar to the two-sources – 1ω . The difference here is that the device is excited to the double of their resonant frequency.

The FM demodulation and the two-sources – 1ω methods provides linear transduction electrical response and the two-sources – 2ω method provides the quadratic component of the resistance variation (figure 6). As it is demonstrated in our previous work[20], for small vibrations (a_n) and pre-strained devices (d_0) the change in the resistance is clearer in the linear transduction mechanism than in the quadratic one (figure 6). We have used SEM imaging to estimate the actual vibration amplitude of the resonators while vibrating at resonance. We find that the vibration amplitude is below the resolution limit of the SEM instrument when the electrical setup is turned on, which was estimated to be 10 nm because of the electrical interferences.[20]

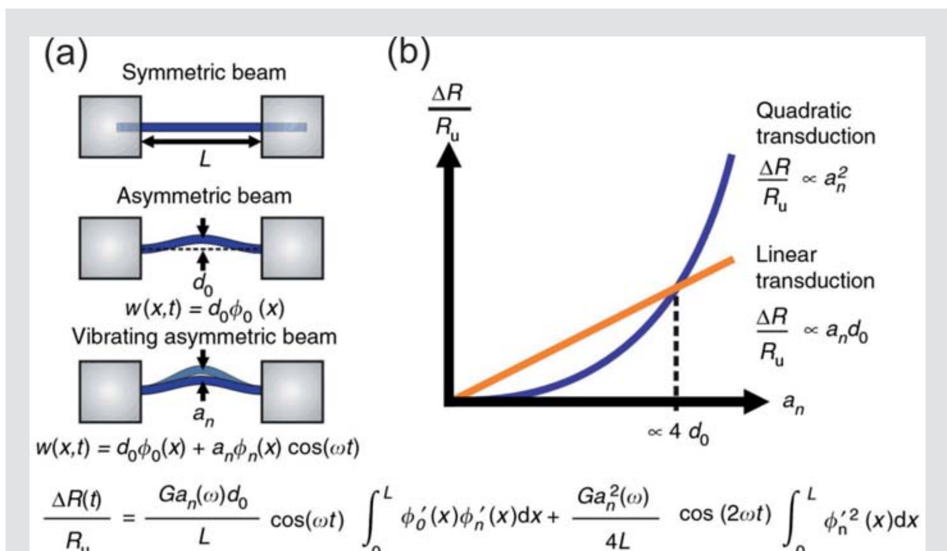

Figure 6. Modelling of piezoresistive transduction in DCB nanomechanical resonators. (a) Schematic representation of a symmetric beam and an asymmetric beam at rest and a vibrating asymmetric beam. (b) Relation between the relative change of resistance ($\Delta R/R_u$) and the amplitude of vibration a_n. The two curves represent the linear (orange) and quadratic (blue) components of the piezoresistive transduction. The plots shows that for vibration amplitudes smaller than the maximum deflection at rest ($a_n < 4d_0$), the linear component is larger than the quadratic one (source[20]).

In this previous work[20] we demonstrate the influence of the asymmetry of a device at rest (d_0) induced by pre-strains on the piezoresistive measurements. This mechanism enhances the sensitive on the linear detection of the vibration that is especial significant to detect small vibration amplitudes ($a_n < 4d_0$) due to the influence of the strain at rest (d_0) on the electrical resistance variation (ΔR). We have shown that it is a new phenomenon that increases the piezoresistive transduction efficiency of NEMS even for devices without large piezoresistive coefficients. For that reason we design, fabricate and measure nanometric devices with engineered asymmetries to demonstrate that improvement.[23] From the fabrication point of view, it is applied the fabrication approach presented in chapter 3 based on FIB implantation and wet etching, taking advantage of the design flexibility of this method that is very convenient for prototyping. To measure the fabricated devices it is used a variation of the 2 sources - 1ω setup to detect the linear transduction part of the piezoresistance as it is represented in figure 6. The results are published in this paper[23] and they are presented in the section 4.4 of this chapter.

4.3 Combination of NEMS and MEMS

In this section, it is presented an ongoing work that consists on the combination of a MEMS and a NEMS (figure 7). A suspended NEMS is anchored from one side to the mobile part of a MEMS or comb and to a fixed electrical pad from the other side. The idea is to produce a movement on the released MEMS by an electrostatic force. Then, because of the MEMS movement, the NEMS will be strained and tuned like a guitar string, changing their resonant frequency.

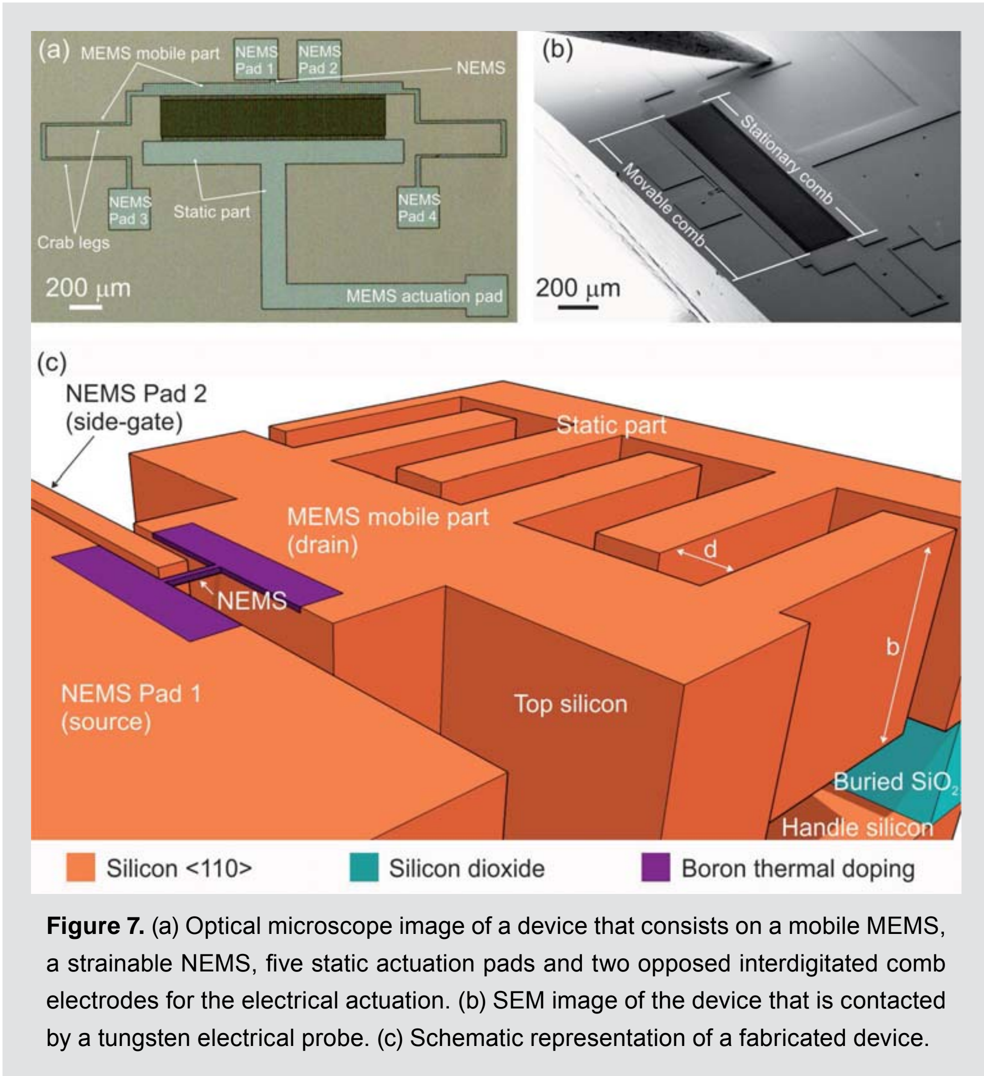

Figure 7. (a) Optical microscope image of a device that consists on a mobile MEMS, a strainable NEMS, five static actuation pads and two opposed interdigitated comb electrodes for the electrical actuation. (b) SEM image of the device that is contacted by a tungsten electrical probe. (c) Schematic representation of a fabricated device.

The MEMS structure is composed by two parts, the comb drive actuator and the crab leg suspension. The comb actuator is placed in front of a stationary comb. When a voltage is applied the moving comb (MEMS) moves into the stationary comb. The position of the moving comb can be controlled by the applied voltage. The applied force to the movable comb is:

$$F_x = d\,[\,(1/2) \cdot C \cdot V_D^2\,] / dx$$

Where V_D is the applied voltage and C the capacity between the two combs. This expression can be approximated to:

$$F_x = N_{DM} \cdot V_D^2 \cdot \varepsilon \cdot (b / d)$$

Where N_{DM} is the number of interdigitated electrodes, ε is the dielectric constant, b is the thickness of the device and d the gap distance between the movable and the static combs (figure 7c).

The crab leg is a structure designed to provide suspension for the moving comb (figure 7a). For a crab leg of length L and for an applied force F:

$$F = 3 \cdot E \cdot I \cdot x / L^3$$

Where E is the material Young Modulus and I the moment of inertia of the supporting leg:

$$I = b \cdot w_b^3 / 12$$

Where w_b is the width of the supporting crab leg and b their thickness. According to the previous expressions and taking into account that the displacement has to be divided by two because of the mechanical resistance of the two crab legs, the displacement of the structure is:

$$x = (2 \cdot N_{DM} \cdot V_D^2 \cdot \varepsilon \cdot L^3) / (E \cdot d \cdot w_b^3)$$

It has to be considered that the length of the crab legs and their width are the parameters that have more affectation in the movement of the structure. The electrical potential has also a big influence on the movement. The force and the displacement are proportional to the number of fingers of the movable comb.

The Yong Modulus defines the relationship between the stress (force per unit of area) and the strain (deformation) and it is used to numerically determine the elongation of the NEMS as a result of the force generated by the MEMS:

$$\Delta L = (F \cdot L_0) / (E \cdot A_0)$$

Where ΔL corresponds to the elongation of the NEMS for a length L_0 and a section A_0.

For the designs of the structures to be fabricated these expressions are taken into account. Table 2 and 3 are a summary of selected parameters in order to achieve detectable movements of the MEMS and suitable deflection of the NEMS respectively.

For a NEMS of 50 nm width, 40 nm thickness and 20 μm length, an elongation of 46 nm can be produced when a voltage of 25 V is applied to the fabricated MEMS.

<table>
<tr><th colspan="9">MEMS</th></tr>
<tr><th>N_{DM}</th><th>V_D [V]</th><th>ε [F/m]</th><th>L [mm]</th><th>b [μm]</th><th>d [μm]</th><th>w [μm]</th><th>x [nm] without NEMS</th><th>F [nN]</th></tr>
<tr><td rowspan="2">100</td><td>10</td><td rowspan="2">$8.85 \cdot 10^{12}$</td><td rowspan="2">0.5</td><td rowspan="2">5</td><td rowspan="2">4</td><td rowspan="2">10</td><td>36.88</td><td>110.63</td></tr>
<tr><td>25</td><td>230.47</td><td>691.41</td></tr>
</table>

Table 2. Parameters selected for the MEMS where N_{DM} corresponds to the number of fingers, L the length of the crab legs, b the thickness, d the gap between the fingers and w the width of the movable crab legs. The table summarizes the movement of the MEMS (x) and the produced force for two different applied voltages (F).

<table>
<tr><th colspan="2">MEMS</th><th colspan="6">NEMS</th></tr>
<tr><th>V_D [V]</th><th>F [nN]</th><th>w [nm]</th><th>t [nm]</th><th>A_o [nm^2]</th><th>L_0 [μm]</th><th>E [GPa]</th><th>ΔL [nm]</th></tr>
<tr><td>10</td><td>110.63</td><td rowspan="4">50</td><td rowspan="6">40</td><td rowspan="4">2000</td><td rowspan="2">6</td><td rowspan="6">150</td><td>2.21</td></tr>
<tr><td>25</td><td>691.41</td><td>13.83</td></tr>
<tr><td>10</td><td>110.63</td><td rowspan="4">20</td><td>7.38</td></tr>
<tr><td>25</td><td>691.41</td><td>46.09</td></tr>
<tr><td>10</td><td>110.63</td><td rowspan="2">500</td><td rowspan="2">20000</td><td>0.74</td></tr>
<tr><td>25</td><td>691.41</td><td>4.61</td></tr>
</table>

Table 3. Parameters selected for the NEMS where w corresponds to the width, t the thickness, A_0 the section and L_0 the initial length. The table summarizes the movement that can be reached by the NEMS (ΔL) for two different applied voltages to the MEMS.

For the fabrication of these devices it is employed a SOI wafer of 5 μm of top Si and 2 μm of buried SiO_2. In figure 8 it is illustrated the fabrication process of a complete device. For the fabrication of these devices two photolithography masks are designed. The MEMS are defined in the first photolithography step (figure 8.c). Then, the top silicon layer is etched by RIE (figure 8.e) until SiO_2 layer is reached. Then it is grown a 100 nm thick layer of SiO_2 to protect the MEMS for the subsequent fabrication of the NEMS. The areas where the NEMS have to be fabricated are defined by the second photolithography step (figure 8.g). Afterwards the SiO_2 is stripped by SiOetch employing the photoresist as a mask (figure 8.h). All these steps are performed at wafer level.

Once the MEMS are fabricated the next steps are focused on the fabrication of the NEMS. The wafer is cut in dices of 5 mm x 5 mm and each chip contains four complete

devices. Then, the NEMS are fabricated by FIB implantation (figure 8.i) and anisotropic silicon wet etching (figure 8.j) as presented in our previous work.[21] The MEMS structure is released by removing the SiO_2 with SiOetch (figure 8.k) and the device is annealed at high temperature (figure 8.l) as presented in chapter 3.[21]

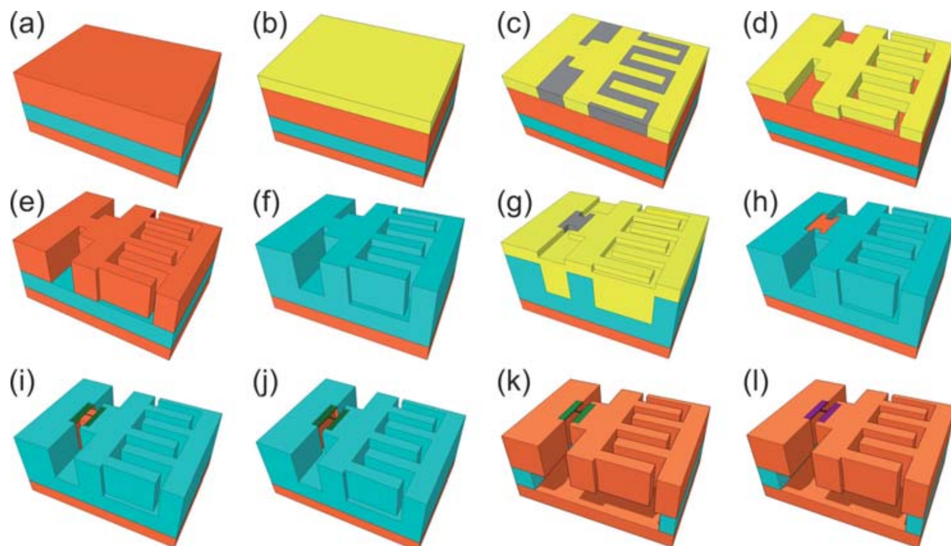

Figure 8. Schematic representation of the fabrication process: (a) SOI substrate, (b) photoresist deposition, (c) photolithography (1st mask), (d) resist development, (e) silicon dry etching, (f) grown of thermal SiO_2, (g) resist deposition and photolithography (2nd mask), (h) resist development and SiO_2 wet etching, (i) FIB implantation, (j) anisotropic silicon wet etching, (k) release of the MEMS by SiO_2 wet etching, (l) high temperature diffusive boron doping.

In our first attempt (first RUN) for the fabrication of the devices we detect some setbacks in the MEMS release. The first inconvenient has been the lack of uniformity during the RIE process. Only for the 30% of the devices of the first wafer the top silicon has been correctly etched. The majority of the devices present silicon residuals in critical parts that prevent the release of the structures by SiO_2 wet etching (figure 9a).

For the devices that silicon has been successfully removed by the RIE processing we observe a second setback related with the design of the devices. The MEMS have collapsed during the release by SiO_2 wet etching even when a Critical Point Dryer (CPD) has been used (figure 9c). Figure 9b shows a successfully released part of a structure. To overcome the release troubles, new masks for the MEMS part has to be designed and fabricated taking into account the needed to reduce the arm's length (figure 7) in order decrease the sticking force during the release to prevent the collapse of the structures.

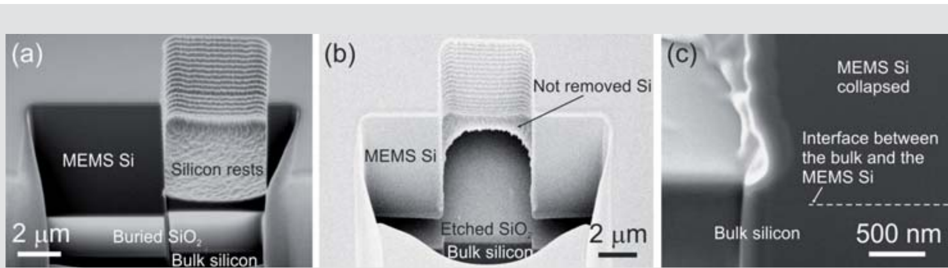

Figure 9. SEM images of three different MEMS release holes that have been cut by FIB to characterize the release of the structure. (a) SEM image of a release hole that has not been completely drilled by RIE. The silicon rests prevents the etching of the buried SiO_2 and the structure cannot be released. (b) SEM image of a successfully released structure. (c) SEM image of a released but stick structure.

It has been successfully moved the movable comb of one of the MEMS devices (figure 10) of our first RUN. For that concrete device the NEMS part has not been defined yet and the MEMS part was completely released. The displacement produced was close to 175 nm applying a potential difference of 70V, from -35 V to +35 V (figure 10b-d). For the measurements of the displacement of the movable MEMS different SEM images of the MEMS have been taken applying different actuation voltages and using the position of the induced etching induced roughness of the walls that are present on the movable comb as labels. The red line (figure 10b and d) corresponds to the relative position of the movable comb respect to the stationary one when it is applied a voltage of -35 V and the yellow one (figure 10c and d) when it is applied a voltage of +35V. In figure 10d it is depicted both lines in order to extract the movement of the movable comb when different voltages are applied. As it can be observed in figure 10a, the ending tip of the movable

comb was collapsed. It implies that there is an extra parameter to take into account, the friction force between the comb and the substrate. For that reason the movement produced to the MEMS has been so small.

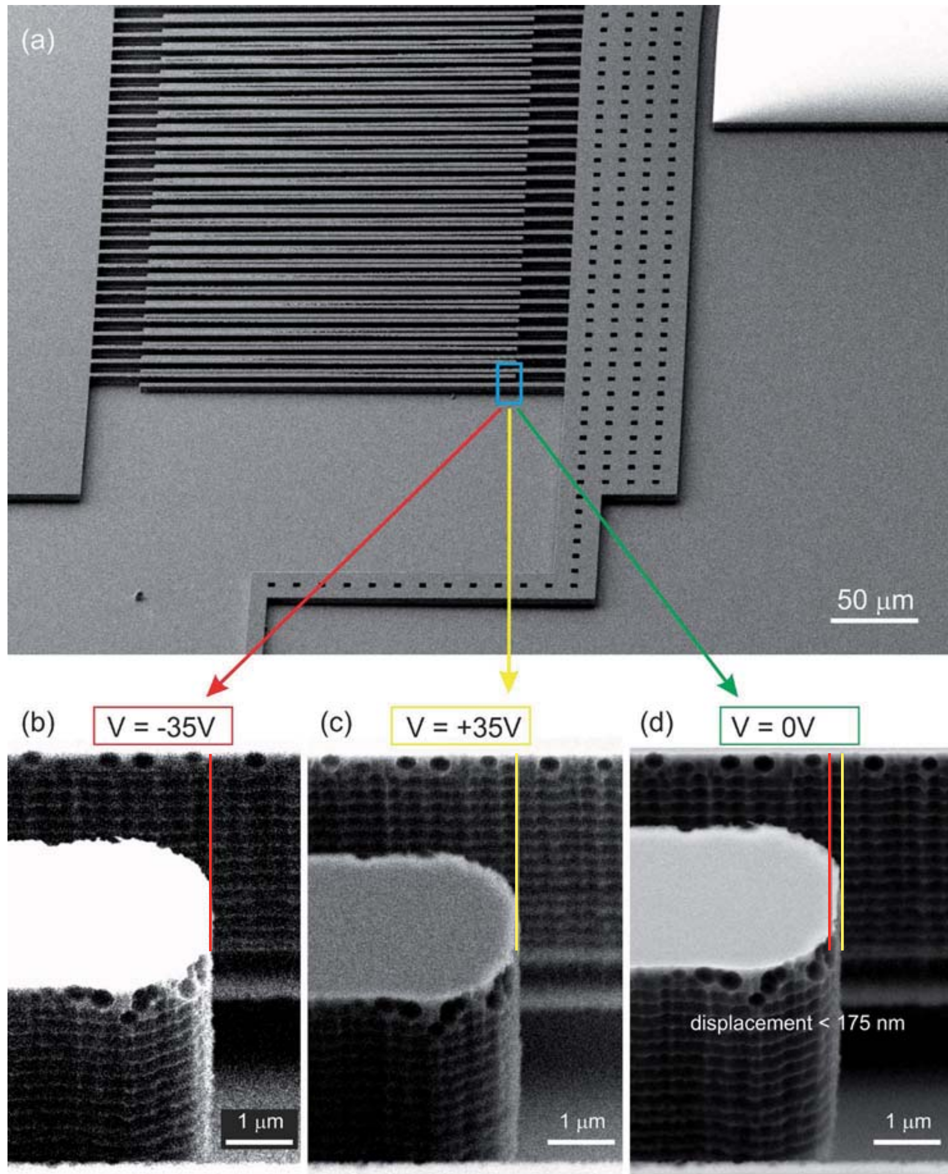

Figure 10. (a) SEM image of actuated MEMS. High detailed SEM images of the MEMS when (b) -35 V is applied, (c) +35 V is applied, (d) no voltage is applied. The red and yellow lines are the labels used to notice the movement of the movable comb compared with the position of the stationary comb.

The fabrication of the NEMS part of the device has also been approached in this prelaminar batch. Once the MEMS has been fabricated (figures 8f and 11a), a 2nd photolithography step (figure 8g) and SiO_2 wet etching (figure 8h) has been performed to depassivate the area to be exposed by the FIB implantation (figure 8i). Then, the fabrication of the NEMS proceeds as proposed in our previous works[21,22] that are presented in chapter 3. The NEMS fabrication consists on the definition by FIB implantation (figure 8i) followed by an anisotropic silicon wet etching (figure 8j) of the 5 μm of device silicon layer. Then, the SiO_2 buried layer is wet etched in sioetch (figure 8k) to release the MEMS device. Finally, by high temperature diffusive boron doping (figure 8l) the electrical conductivity of the NEMS is enhanced. In figures 11b and 11c shows two of the suspended NEMS fabricated in this batch.

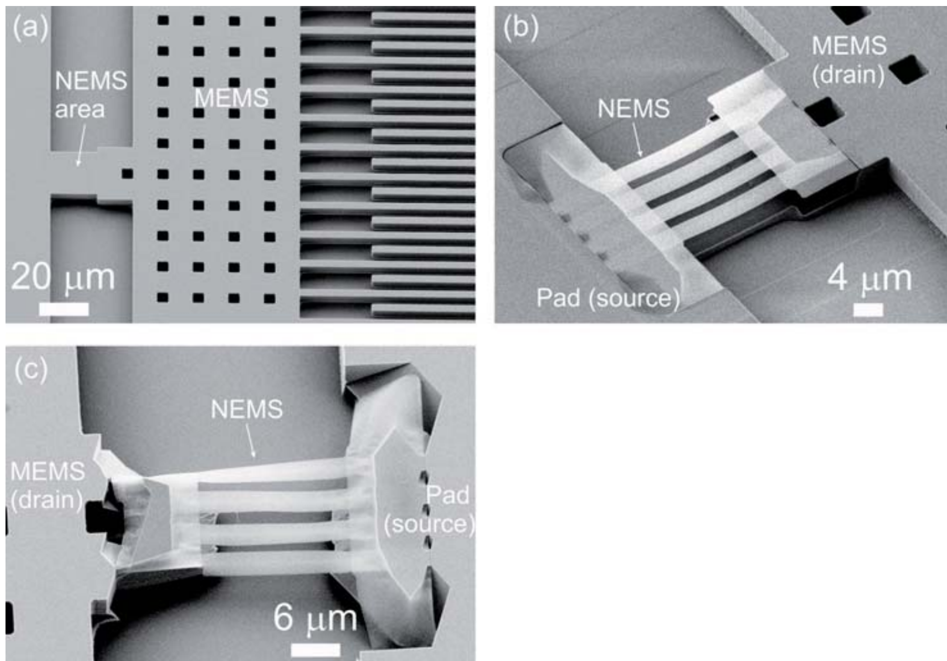

Figure 11. (a) SEM image of actuated MEMS and the area reserved for the NEMS definition. (b, c) SEM images of two different NEMS suspended between the MEMS movable part (NEMS drain) and the source electric pad.

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4.4 Tuning piezoresistive transduction in nanomechanical resonators by geometrical asymmetries

This section has been published in Applied Physics Letters by:
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Chapter 5 | Field effect, single electron and single hole transistors

In this chapter results on the development of silicon nanowires (SiNW) based devices beyond nanomechanical resonators for their employment as single hole transistors (SHoTs) are shown. They are realized by taking advantage of the improvements on the fabrication approach presented in previous chapters. It starts with a brief introduction to single electron transistors (SETs). Then it is described the characterization setups used for the measurements of the fabricated devices. Afterword's it is shown an ongoing work about the fabrication and measurements of ultra-thin Field-Effect Transistors (FETs) and the preparation of a TEM lamella for the characterization of those devices. In the last section of the chapter it is presented our work[1] on single hole transistors (SHoTs). The work reported has been performed in collaboration with the Department of Electrical and Electronic Engineering of the Imperial College of London in the framework of the Single Nanometer Manufacturing for beyond CMOS devices (SNM) FP7 EU project.

5.1. Introduction to SET

Single electron devices (SED) are promising candidates for the fabrication of advanced logic memories, where few electrons are enough to define a bit of information. The advantages of SED includes immunity from statically fluctiations[2,3] and very low power consumption because of the small operating currents that they need to operate. A single electron device can be formed a small conductive island electrically insolated from source and drain electrodes by 2 small tunnel capacities. As a result, discrete electron energy levels are created.

If we add a gate electrode then we get a SET (figure 1a). SETs are very promising devices for the next generation of silicon transistors[4,5]. It consists, basically, in the controllable transference of single electrons. For a gate voltage V_{G1} and small source-drain voltage, there are no accessible states into the island (fig 1c) and there is no conductivity (red line in figure 1b). When the gate voltage is increased to V_{G2}, then some states are accessible

and electrons can tunnel through the capacitances (figure 1d) and there is electrical conduction (black line in figure 1b).

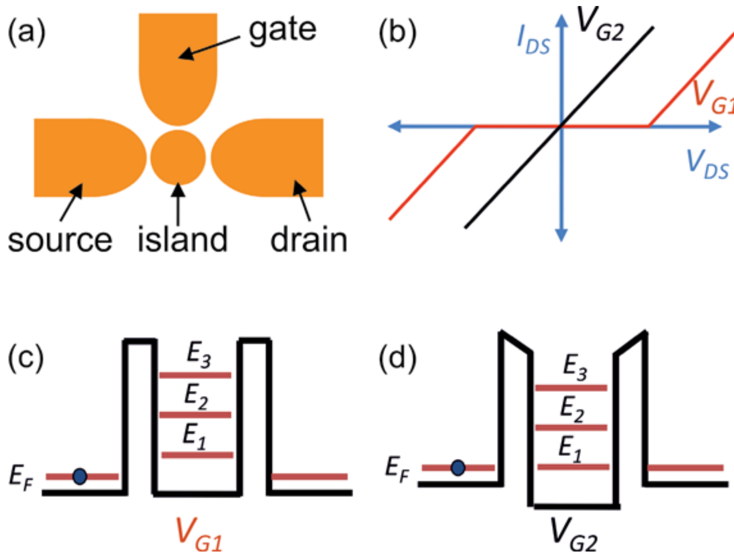


Figure 1. (a) Schematic picture of a SET showing a small island that is electrically insulated from source and drain electrodes by two tunnel capacitances. It is also depicted a side-gate electrode for the electrostatic actuation. (b) I-V schematic plots for two different gate voltages. For gate voltage V_{G1} and low V_{DS} there is no electrical conduction. When gate voltage is increased to V_{G2} there is electrical conduction. In (c) it is represented discrete energy levels into the island for gate voltage V_{G1}. For this condition there are no accessible states for the carriers into the island. In (d) it is represented the situation where the gate voltage is increased to V_{G2} and the Coulomb Blockade is overcome. Then, there is tunnel conduction through the tunnel capacitances.

The island that is electrically insulated from the source and drain electrode can be referred as a Quantum Dot (QD). There are a finite number of electrons into the island. The insulating material contributes as tunnel barrier to the equivalent circuit, adding two capacities C_1 and C_2. The charging energy $Ec = e^2 / 2C$ is the minimum energy needed to introduce an electron to the island, that is to overcome the Couloumb Blockade (CB) repulsion energy created by the electrons that are in the QD. In this context, the smallest the QD is, the biggest the Ec and the CB energies are. The charging energy Ec resulting of the addition of an electron inside the island has to be larger than the thermal energy k_BT, so low temperatures are required for the electrical conduction.

The energy levels on the QD are discrete. By applying voltages in multiples of 2Ec/e the number of electrons is increased one by one. When the tunnel resistances are dissimilar then there is observed periodical current steps in function of voltage. Each of these steps are the result of the inclusion of a new electron to the system. It is called Coulomb staircase.[5] It is possible to control de electrostatic charge of the QD by the gate electrode. By applying a V_{gs}, the I_{ds} varies in periodic oscillations.[6–9]

There are different approaches for the fabrication of QD. For example, they can be realized by carbon nanotubes[16] (CNTs) in which it could be observed coupling effects between electronic transport and phonons,[38] by silicon nanocrystals[12] or suspended quantum dots.[13] Very interesting contributions have been done on Si, mostly as n-type[1-19] doped Si (SETs) and only a few as p-type[20-22] (SHoTs). In the paper presented in section 6 it is reported, for the first time, the fabrication and operation of a suspended SHoT. For that propose, a chip cut from silicon on insulator (SOI) wafer has been used as starting material. As it is shown in Chapter 3 and 4 the definition of the devices are performed by FIB implantation and released by anisotropic wet etching. Because of the ion implantation the devices becomes amorphous and exhibits high resistivity. To surpass this constraint it has been implemented a final step that consists on a post-annealing at high temperature in a boron environment, allowing the formation of a nano-crystalline grain structures and the improvement of the electrical conductivity of the silicon nanowire.[28] It is important to note that the silicon nanowires measured are p-doped and, in consequence, the resulting devices will be SHoTs (Single Hole Transistors). The presence of this NC (size around 5 ~ 10 nm) surrounded by defects, when the device width is smaller than 50 nm, is the origin of the single charge effects that we measure.

5.2. Electrical characterization setup

For the measurement of the electrical characteristics of the devices we have defined silicon electrical pads, at the same time than the transistors, by ion implantation. Each pad is connected to a different element of the transistor that consists on a source, drain and side-gate electrodes. For some measurements it is used the back-gate electrode, that is the bulk silicon of the SOI chip.

Measurements are performed at room temperature and also at low temperature. The measurements at room temperature have been implemented in the 4-probe station (Probeshield, Karl Suss) of the Electrical Characterization Laboratory (SIAM) or in the Crossbeam of the Nanolithography area of the Clean Room, both located at IMB-CNM. On the other hand, the characterization of the transistors at different temperatures has

been realized inside a closed cycle helium cryostat (CTI-Cryogenics) of the Department of Electrical and Electronic Engineering of the Imperial College of London. These different setups have been connected to three different semiconductor analyzers respectively: (i) the 4-probe station to the 4155B (HP); (ii) the Crossbeam to the B1500A (Agilent) and (iii) the helium cryostat to the 4155B (Agilent).

To characterize the performance of the transistors we measure their I-V curves. Two types of measurements have been performed. The first one consists on sweeping the source-drain voltage for different gate voltages and the second one by sweeping the gate voltage for different source-drain voltages. In both cases the source-drain current (that is the current that passes through the nanowire) has been measured. For the measurements performed in the cryostat we swept the drain-source voltage for different gate voltages and different temperatures from 300K to 10K. In figure 2 it is represented the electrical setup employed for the I-V curves.

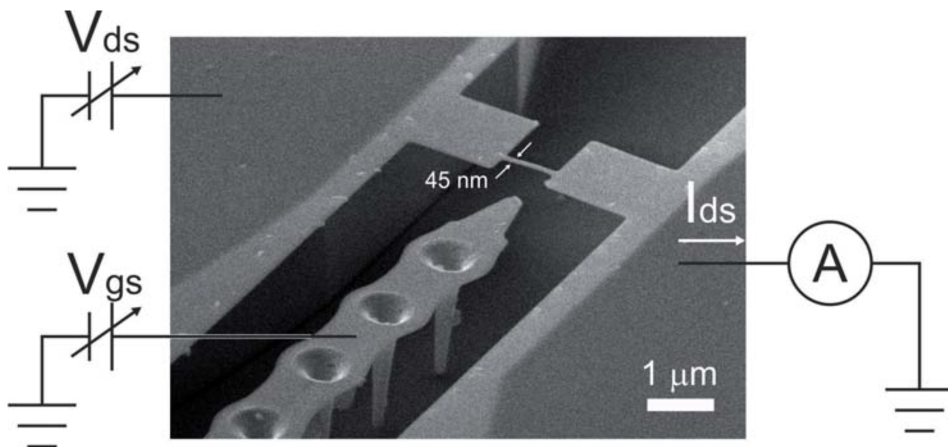


Figure 2. (a) Electrical scheme combined with a SEM image that represents the electrical setup used for the measurements. V_{ds} corresponds to the source - drain applied voltage, V_{gs} is the voltage applied in the side-gate electrode and I_{ds} corresponds to the measured source – drain current.

5.3. Field effect transistors

This section is part of an ongoing work. The objective of this work is the investigation of the electrical characteristics of FETs formed by very thin silicon nanowires (thickness among 10 ~ 15 nm) at different temperatures and it complements the results presented in 6.6. One of the motivations of this work is to compare the performance of SiNW FET when they are suspended or not suspended.

It is demonstrated the fabrication of a functional silicon transistors of 10 ~ 15 nm thickness. We start with SOI chips of 15 nm of device-silicon at the (100) orientation and 150 nm of buried oxide. These chips have been cut from a 50 nm device SOI wafer (figure 3a) previously thinned by thermal oxidation (figure 3b) in the IMB-CNM clean room from 50 nm to 15 nm (figure 3c) of device-silicon. After that it is performed the FIB implantation (figure 3d), the TMAH wet etching (t = 20 s) (figure 3e) and the high temperature annealing in boron environment[28,10] as explained in chapters 3 and 4 (figure 3f).

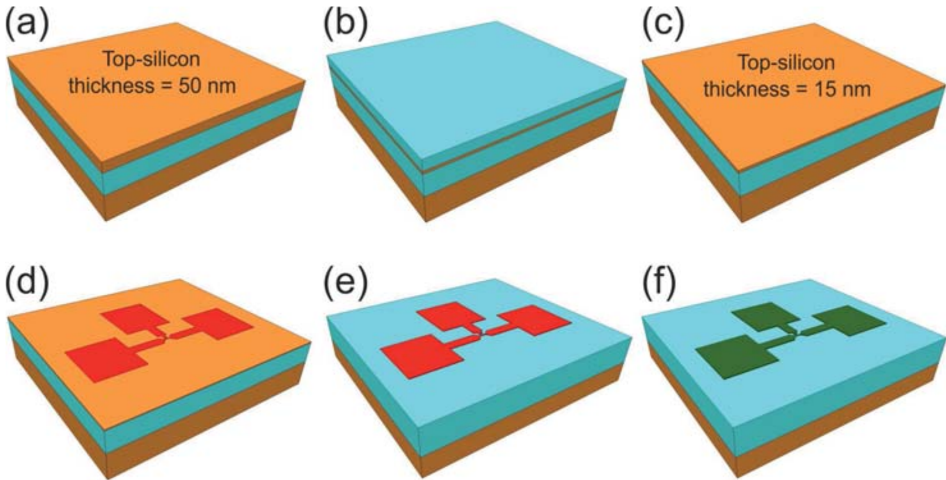
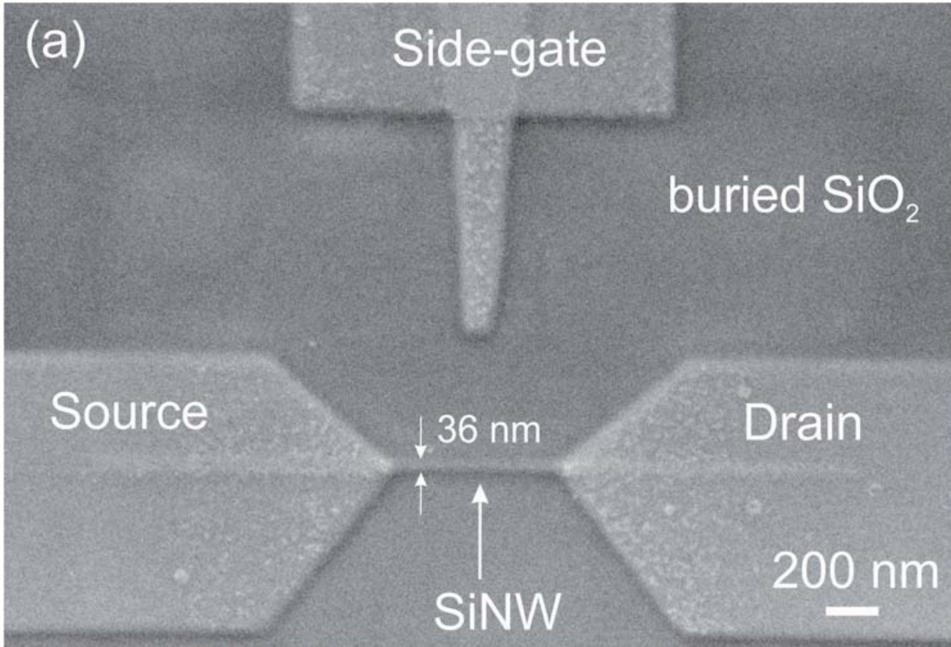


Figure 3. Schematic representation of the fabrication of the ultra thin field effect transistors. (a) Silicon on insulator (SOI) substrate with a top silicon thickness of 50 nm. (b) Dry thermal oxidation of silicon where 80 nm of SiO_2 are grown.[11] (c) Wet chemical etching for removing the grown SiO_2. The final thickness of the top Si layer is 15 nm ± 0.5 nm. (d) FIB implantation for the definition of the electrical pads, the silicon nanowire and the side-gate, source and drain electrodes. (e) Anisotropic silicon etching. (f) High temperature diffusive boron doping.

In figure 4a there is a SEM picture presenting one of the fabricated transistors of 10 ~ 15 nm thickness, 36 nm width and 650 nm length where the distance between the side-gate and the device is 470 nm. The I-V curve shows their transconductance when the voltage of the side-gate (V_{gs}) is swept from 4 V to 12 V. The drain-source current (I_{ds}) vs. side-gate voltage (V_{ds}) for a fixed drain-source voltage (V_{ds}) of 1.5 V is shown in figure 4b. The linear region in the I-V curve between 7 V and 8.5 V of V_{gs} is marked with a green line. The measured current that passes through the NW for V_{gs} = 6.5V is I_{ds} = 3 nA (on state) and for V_{gs} = 8.75V is I_{ds} = 7 pA (off state), that it is a variation of 3 orders of I_{ds} magnitude for ΔV_{gs} = 2.25 V.



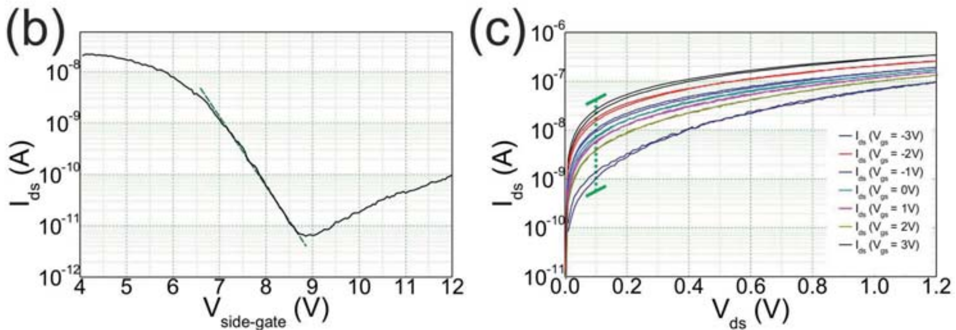


Figure 4. (a) SEM image of a SiNW FET. (b) I_{ds} vs. $V_{side\text{-}gate}$ characteristics for a V_{ds} of 1.5 V. A green dashed line emphasizes the lineal part of the plot. (c) I_{ds} vs. V_{ds} characteristics for $V_{side\text{-}gate}$ voltages from -3 to 3 V. The green dashed line corresponds to V_{ds} = 0.1 V where the I_{ds} variation as a function of $V_{side\text{-}gate}$ is larger.

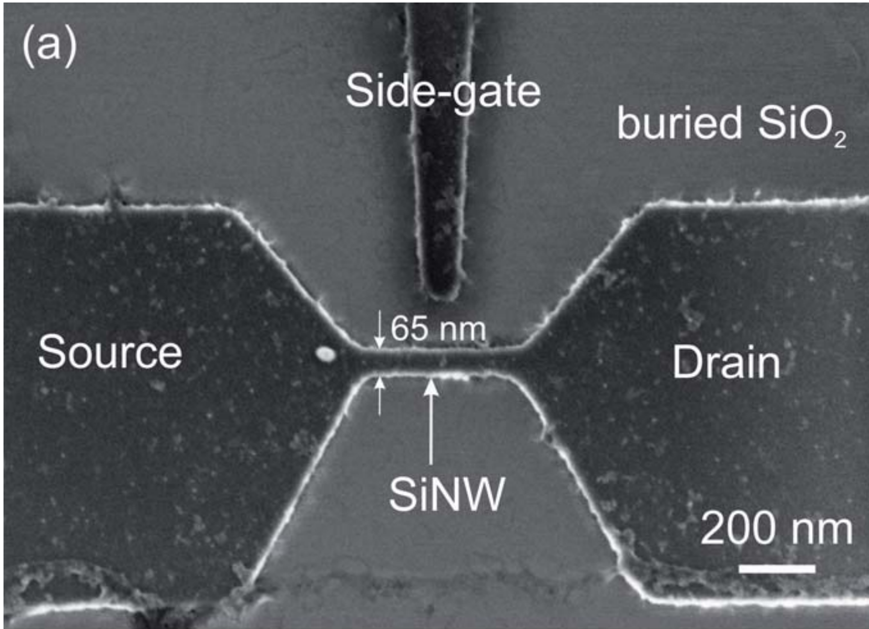
From this preliminary result it is extracted the transconductance (G_m) characteristics of the transistor. The G_m is the slope of the transference curve ($G_m = dI_{ds}/dV_{gs}$) that is close to 700 mV/dec. G_m gives an information of how good a transistor is; the smaller the value, the higher the slope it is. High slopes in the transference characteristics mean that it is

possible to switch the transistor (ON/OFF) with a very small change in the gate electrode potential. Just as a first approximation we comparted our preliminary result G_m value with the subthreshold swing (SS) of other devices reported in the literature. Our approach is close to the state of the art values according to table 1.

First author	Gate mat. / distance (nm)	Channel width (nm)	SS (mV/dec)	Ref.
Zheng	ZnO_2 / 60	20	300	12
Allen	Si_3N_4 / 200	50	600	13
Huang	SiO_2 + HfO_2 / 4 + 6.3	20 u. x 10 nm	80	14
Ryu	SiO_2 / 151	80	499	15
Chen	SiO_2 / 13.6	48	60	16
This work, device #1	Air / 470	36	700	ongoing

To improve the transconductance of our transistors it is required to reduce the gap distance between the NW and the side-gate electrode. On the other hand, the V_{ds} used for the measurement represented in figure 4b is too high (V_{ds} = 1.5V). As can be observed in figure 4c the optimum V_{ds} value for the transference curve graph is close to 0.1V (in the lineal region) that it is where the I_{ds} is more influenced by the V_{gs}. Consequently, for the next experiments, it is important to set the V_{ds} value according to the I_{ds} vs. V_{ds} curve (figure 4c) in order to enhance the I_{ds} vs. V_{gs} response.

Next it is shown a device of 10 ~ 15 nm thicknesses, 65 nm width and 385 nm length that is separated to the side-gate electrode 130 nm (figure 5a). The width of this device is almost 2 times the width of the previous device (figure 4a) and the side-gate distance to the transistor is 3 times shorter. The I-V curve of this device has been obtained by measuring the I_{ds} appling a V_{ds} = 1 V and sweeping the V_{gs}. With this conditions it is acquired a G_m = 2.75 V/dec, that is a worse value that the obtained in the previous device (figure 4). With this last device it is demonstrated that it is possible to reduce the distance between the side-gate and the NW at least to 130 nm. Unfortunately, the width of this NW is quite large revealing the importance that the reduction of the dimensions has in the performance of the device.



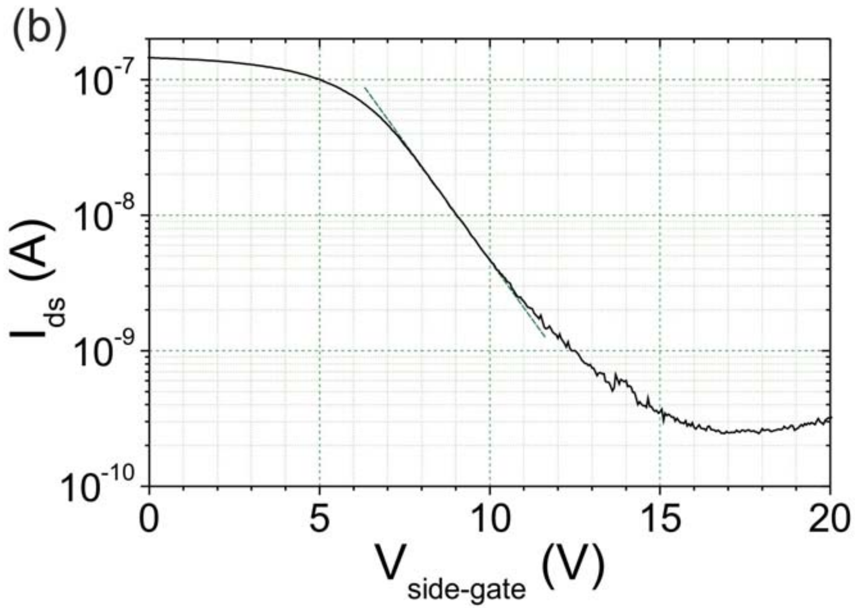


Figure 5. (a) SEM image of a SiNW FET. (b) I_{ds} vs. $V_{side\text{-}gate}$ characteristics for a V_{ds} = 1 V. A green dashed line emphasizes the lineal part of the plot.

Next batches of devices will be oriented to the achievement of narrower devices with a closer side-gate configuration. It will be investigated the possibility to get transistors going further with this fabrication approach by developing a three dimensional gate in order to surround the NW. It is also necessary to produce new devices with different widths and different gaps between the side-gate and the NW in order to generate enough statistics to stablish a relationship between these parameters and the transconductance. From the electrical characterization point of view it has to be done measurements at different temperatures down to 10 K to investigate the performance of these devices as SET/SHoT in close connection with the investigation presented in section 6. On the other hand, to better understand the behavior of this devices it becomes necessary to characterize by TEM the arrangement, the shape and dimensions of the expected nano-crystalline structure[28,1] of NWs. In the next section it is presented a TEM lamella of around 30 NW in cross-section that will help us to elucidate this important information.

5.4. TEM lamella

In this section it is described the fabrication of a lamella that is part of the ongoing investigation presented in the previous section. We wanted to characterize the dimensions and arrangement of silicon nanocrystals that are induced during a high temperature annealing in very thin silicon nanowires (thicknesses around 10 ~ 15 nm, widths around 35 ~ 70 nm). This investigation became crucial to understand the electrical behavior of these devices.

A TEM lamella is a very thin slice of material (in the order of 50 nm of thickness) that contains the features to be investigated. Then, by TEM characterization, electrons can pass through the thin slice of material and resolutions close to 0.1 nm (1 A) can be obtained.

The lamella under study contains the cross-section of approximate 30 nanowires. Figure 6 is an schematic description of the procedure followed for the fabrication of that lamella. Figures 7 and 8 show SEM images done during the lamella definition in order to illustrate the process.

Figures 6a and 7a are, respectively, a picture representation and a SEM image of the nanowires to be studied. The first step consists on depositing a protection strip of Pt (figure 6b and 7b). This strip has been defined:

- Firstly by Focused Electron Beam Induced Deposition (FEBID) that is a low throughput technique but it is safe with the first atoms of the surface (no sputtering is produced).
- Secondly by Focused Ion Beam Induced Deposition (FIBID) in which process the

throughput is higher than the previous one and the uncertainty between deposition and milling take place on top of the previously deposited Pt by FEBID.

Then it is milled two deep trenches at high ion current keeping the Pt strip in the middle of both cuts. It is selected a trapezoidal shape for that trenches to improve the material evacuation of the redeposits. The end of the cuts are defined just where the strip is, that it is the desired inspection zone and, thereby, the redeposit material does not affect the lamella (figure 6c).

Once the lamella is created it exhibit a thickness around 0.5 ~ 2 μm. The next step is called lift-out and consists on the extraction of the lamella, the manipulation of that lamella and their attachment to the TEM grid. At this point the lamella is united to their original sample by their bottom and their two sides. It is performed a cut of one of their sides and their bottom (figure 6d). Then, the manipulator is approached to the top of the lamella and Pt is deposited (FEBID + FIBID) in the junction between the tungsten manipulator tip and the lamella (figure 6e). The lamella becomes attached to the tungsten tip and it is cut the second side of the lamella in order to finish the release of the lamella from the sample (figures 6f and 7c).

After that the lamella is approached to the TEM grid (figures 6g and 7d) and, by FEBID + FIBID it is deposited Pt in the junction between the lamella and the grid (figures 6h, 7e and 7f). Next, it is cut the union between the lamella and the tip and the lamella becomes attached uniquely to the TEM grid (figures 6i and 8a).

Finally the lamella is polished by the FIB at low voltage (5 KeV) and low current (10 ~ 50 pA) until the area of interest starts to be brighter (figure 8b) to the SEM secondary electron (Everhart-Thornely) detector. That means that the ratio of collected electrons increases as the lamella becomes thinner, in the range of 50 ~ 100 nm. As it can be observed in figure 8c and represented in figure 6j the lamella is well polished in the interest area, where the section of the NWs are clearly observed by SEM inspection.

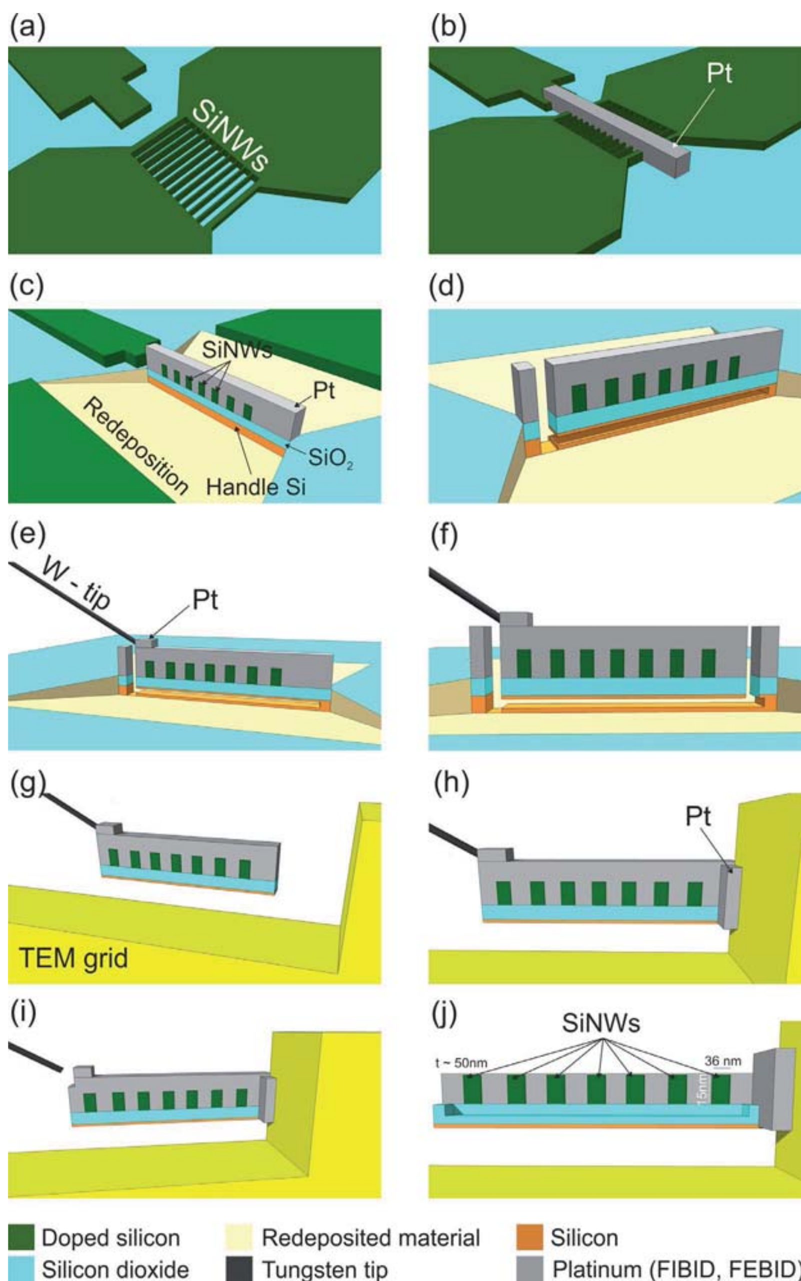


Figure 6. Schematic representation of the fabrication of the lamella. (a) Fabricated SiNWs in parallel defined between source and drain electrode. (b) FEBID and FIBID of Pt for the protection of the SiNWs. (c) Double cross-section of the SiNWs done by direct FIB milling. (d) FIB milling of the left and the bottom lamella - sample junctions. (e) Lamella mounted to the tungsten tip of the nanomanipulator by Pt deposition (FEBID + FIBID). (f) FIB milling to release the lamella from the sample. (g) Lamella approaching the TEM grid. (h) The lamella is attached to the TEM grid by Pt deposition (FEBID + FIBID). (i) FIB milling of the tungsten tip – lamella junction. (j) Final polishing of the lamella.

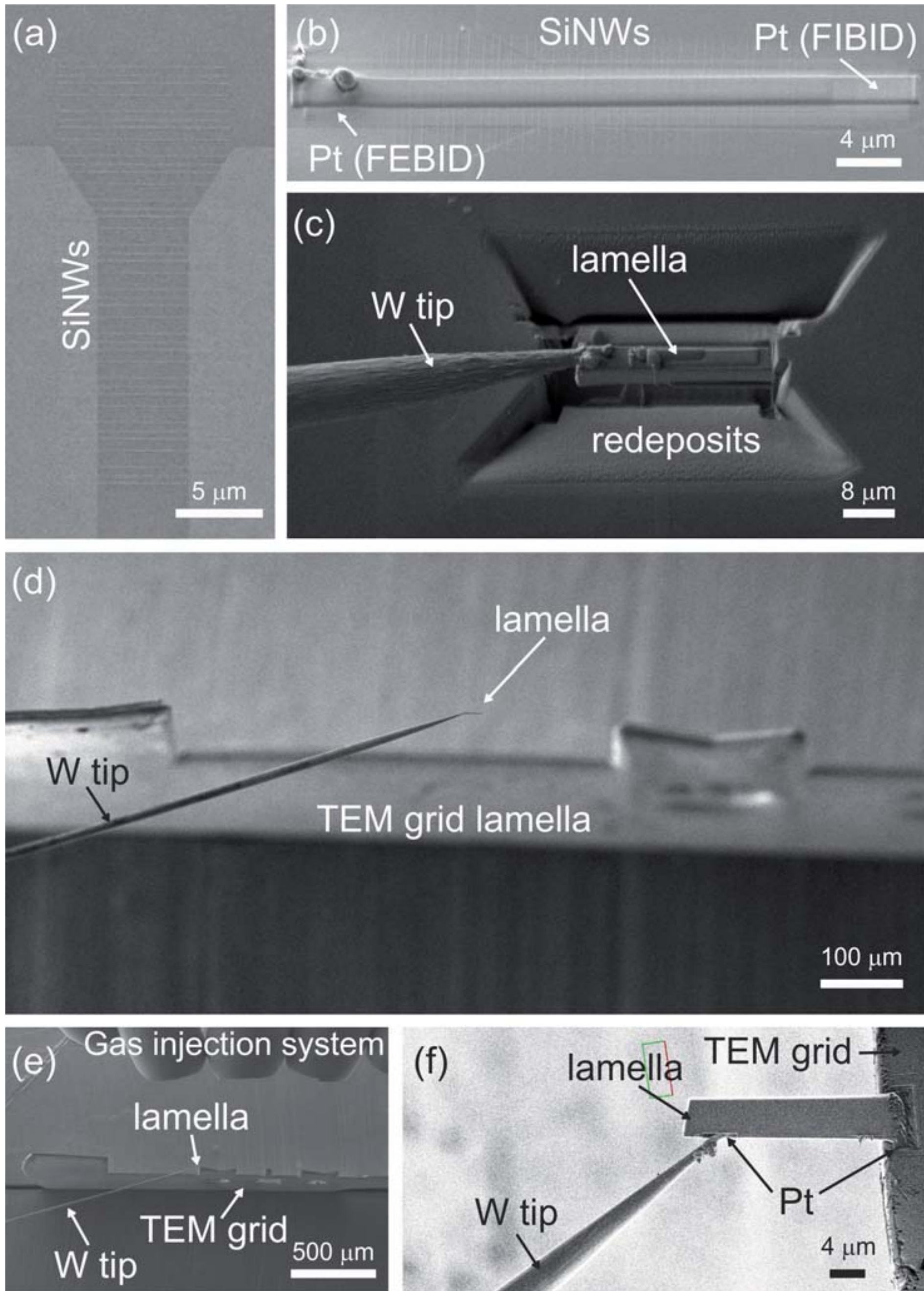


Figure 7. SEM images taken during the fabrication of the lamella. (a) Fabricated SiNWs in parallel defined between source and drain electrode. (b) FEBID and FIBID of Pt for the protection of the SiNWs. (c) Fabrication and lift-out of the lamella. (d) Lamella approaching the TEM grid. (e) The lamella is attached to the TEM grid by Pt deposition (FEBID + FIBID). (f) Zoom in image of the lamella attached to the TEM grid by deposited Pt (FEBID + FIBID).

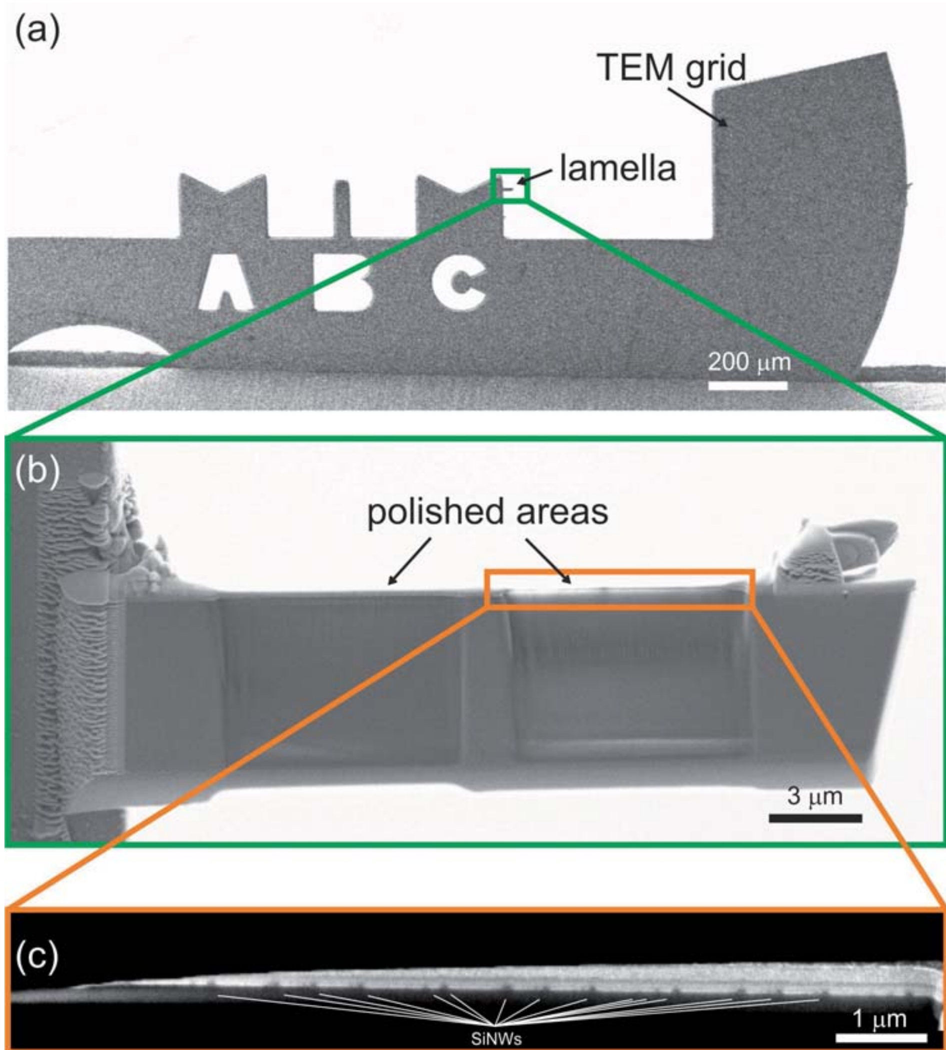


Figure 8. SEM images of the polished lamella. (a) SEM image of the lamella and the TEM grid. (b) Zoom in image of the lamella showing two polished areas for TEM inspection. (c) Zoom in image of one of the polished areas where the cross-sections of the SiNWs can be clearly observed.

5.5. Electrode sustained by pillars

The next devices that are presented are all suspended between the source and the drain electrodes. They are obtained from chips cut from a SOI wafer of 2 μm thickness of top-Si that is (110) oriented. For the purpose of the work presented in section 6, the length of the device has to be short. That means a close distance between the source and the drain electrodes that forces the side-gate electrode to be slight. On the other hand, there is an interest to avoid the position the clamping's of the device in the under-etched electrode area. For that cause the device has to be placed at more than 15 μm from the corner of source and drain electrodes (see figure 9a), dictating the fabrication of a large side-gate electrode. These two reasons impose the fabrication of a narrow and long side-gate electrode to approach the excitation signal close to the device. As can be observed in figure 9a, the fabricated side-gate collapses as a result of the sticking force produced during the anisotropic wet etching, increasing the effective distance to the device that reducing their driving signal.

Due to the small distance between source and drain electrodes there is not enough space to define compensation strips.[10] To overcome this limitation, pillars to sustain the excitation electrode have been fabricated in a similar way than it is depicted in chapter 3. The pillars have to be done perforating completely the top-silicon layer until the buried SiO_2. In figure 9b it is shown a SEM cross-section image of a dose experiment consisting in 6 spots at different doses. It is found that at $1.2\cdot10^{21}$ at$\cdot$cm^{-2} of exposure fluency the buried SiO_2 is reached. In figure 9c there is an example of a successfully fabricated structure where the pillars sustain the side-gate electrode reducing the distance to the device and enhancing their electrostatic actuation signal.

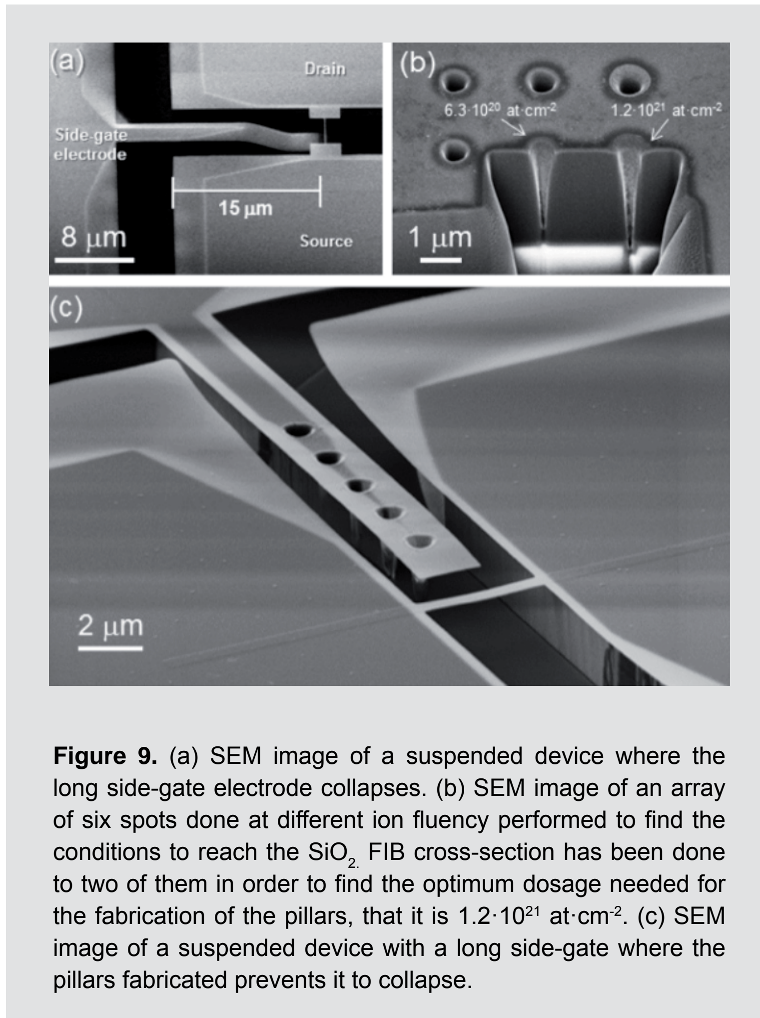


Figure 9. (a) SEM image of a suspended device where the long side-gate electrode collapses. (b) SEM image of an array of six spots done at different ion fluency performed to find the conditions to reach the $SiO_{2.}$ FIB cross-section has been done to two of them in order to find the optimum dosage needed for the fabrication of the pillars, that it is $1.2 \cdot 10^{21}$ at·cm^{-2}. (c) SEM image of a suspended device with a long side-gate where the pillars fabricated prevents it to collapse.

In the following article it is described the fabrication process followed to obtain a SHoT, the TEM characterization that shows the presence of nanocrystals surrounded by defects, the measured IV curves at low temperature, the extraction of the device characteristics from the measurements performed and, finally, the model and explanation of the measured phenomena.

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5.6. Resonant tunnelling features in a suspended silicon nanowire single-hole transistor

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Chapter 6 Conclusions

*In this thesis, it is presented a new and unique approach for the realization of conductive **silicon nanostructures** based on FIB implantation, anisotropic wet etching and high temperature annealing in boron environment. This **resistless** patterning method is very appropriate for **prototyping** and for the fabrication of small batches of devices.*

The developed processes are applied to the fabrication of devices of nanometric dimensions for the experimentation at the nanoscale with different resonator geometries, different transistor configurations (FETs, ShoTs) and combining coupled mechanical structures. This fabrication approach is **compatible** with traditional **semiconductor fabrication methods,** enabling a mix and match strategy in order to increase the throughput.

The effects on the material of the processes have been investigated. Before the FIB implantation silicon becomes (i) amorphous as it is demonstrated by Raman and TEM characterization, (ii) gallium implanted as observed by EDX and TEM and (iii) the electrical conductivity decreases as indicated in the I-V curves. To achieve functional electrical devices an additional step has been developed. It consists on a high temperature diffusive boron doping, obtaining a (i) **recrystallization of the material forming nanocrystalline grain structures** (supported by TEM and Raman characterization), (ii) **a gallium free material** (validated by EDX and TEM), (iii) **an electrical conductivity enhancement** up to 4 orders of magnitude thanks to boron doping (measured electrically by I-V curves) preventing (iv) the growth of SiO2 even when 1000ºC annealing temperatures are reached (validated by EDX, TEM and I-V curves). Devices fabricated by this method are **electrically and mechanically functional,** permitting the **electrical readout of the mechanical vibration** of the obtained free suspended devices.

The following **innovations that enhance the technological capabilities** have been introduced from the process point of view: (i) **compensation strips** to prevent undesired underetching of the structures, (ii) definition **of three dimensional supporting pillars** to

avoid the collapse of long structures and (iii) **fabrication of coupled and heterogeneous structures** that enables the investigation on complex structures.

Devices consisting of different structures and configurations have been investigated. A suspended device **reaching a 10 nm diameter limit** and **arrays** up to 100 **identical nanowires** in parallel have been fabricated. Resonant frequencies of the fabricated devices have been successfully measured in the range of 5 to 500 MHz. The **piezoresistive responses** of the devices are **comparable** with the devices defined by **other top-down fabrication techniques** as photolithography, achieving **quality factors up to 1000.** The fabrication of **integrated devices** combining **NEMS and MEMS** has been demonstrated.

It is demonstrated the effect of **engineered asymmetries** as a strategy to tune the electromechanical response of free suspended vibrating nanowires. It is possible to **geometrically enhance the piezoelectrical readout amplitude** of a resonance frequency mode up to 5 times that can be very useful for devices that: (i) are vibrating at small amplitudes and (ii) for materials that do not exhibit ultra-high gauge factors.

Field effect transistors has been designed, fabricated and measured. It is **reported** for the **first time the operation of a suspended single hole transistor (SHoT).** The transistor is fabricated by the novel method presented in this thesis that generates nanocrystals within a p-type silicon nanowire. Evidence for single hole charging of a nanocrystal island is provided by a clear appearance of **"Coulomb diamonds"** in the conductance characteristics. Moreover, there are observed the **presence of acoustic-phonon mode interactions in the nanocrystals.**

To sum up, a new fabrication approach that permits to obtain nanometric suspended silicon electrical and mechanical functional devices is presented. It has been demonstrated their applicability as NEMS and their functionalities as FET and SHoTs. Promising nanomechanical and nanoelectronic devices based on p-type suspended silicon nanowires can be further fabricated using this method.