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On the design of high-efficiency RF Doherty power amplifiers

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Nomenclature

ACPR	adjacent-channel power ratio
ADS	advanced design system
BER	bit error rate
BW	bandwidth
CA	carrier amplifier
CCA	current conduction angle
CS	Common Source
DPA	Doherty power amplifier
DPD	Digital predistortion
DSP	Digital Signal Processor
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
FB	Feedback
FF	Feed Forward
IBO	input back-off
IIN	Impedance Inverter Network
IMD3	third-order inter-modulation distortion
IMN	input matching network
IMP	Intermodulation Products
LINC	Linear Amplification with Non-linear Components
LMS	least mean square
LNAs	Low Noise Amplifiers
MEMS	micro electro-mechanical switch
m-HEMTs	metamorphic high electron mobility transistor
NPR	noise power ratio
OBO	output back-off
OMN	output matching network
PAE	Power Added Efficiency
PAPR	peak-to-average ratio
PAs	power amplifiers
PCN	Phase Compensation Network
PD	Predistortion
PkA	peaking amplifier
PLL	phase-locked loop
PT	Polar Transmitter
Q	quality-factor
RF	radio frequency
W-T	with tapered line
Wo-T	without tapered line

Abstract:

Nowadays, power amplifiers (PAs) are one of the most crucial elements in wireless standards. These elements have been focused on an important issue, which is related to the reduction of power amplifier efficiency at the output back-off (OBO) power level of transmitters so that the resulting signals have a high peak-to-average ratio (PAPR). The lower efficiency of PAs causes the waste of energy as heat. In fact, this lower issue leads to the increment of costs and size (e.g. the cooling requirements). Furthermore, the trade-off between linearity and efficiency in PAs can be considered as another major issue.

To cope with the undesired circumstances offered by efficiency degradation, the Doherty power amplifier (DPA) is one of the useful techniques which provide high efficiency for high PAPR of modern communication signals. Nevertheless, the limited bandwidth(BW) of these kind of PAs (about 10% of fractional bandwidth) and its importance (in modern wireless systems such as LTE, WiMAX, Wi-Fi and satellite systems) have encouraged the researchers to improve this drawback in recent years. Some typical BW limiting factors effect on the performance of DPAs: i) quarter-wave length transformers, ii) phase compensation networks in/output matching circuits, iii) offset lines and device non-idealities; Note that quarter-wave length transformers performs as an inverter impedance in the load modulation technique of DPAs. Concretely, the future objective of designing DPAs is to decrease the impact of these issues.

In this context, this PhD-thesis is focused on improving fractional bandwidth of DPAs using the new methods that are related to impedance transformer in load modulation technique. This study has two fold. First, a novel DPA is presented where a wideband GaN DPA in the 2.5 GHz band with an asymmetrical Wilkinson splitter are employed. Note that the impedance transformer of the proposed architecture is based on a matching network, including a tapered line with multi-section transformer in the main stage. The following results are obtained:

- The bandwidth showed from 1.8 to 2.7 GHz
- The power efficiency is obtained showing more than 33% drain efficiency in the range of 1.8 to 2.7 GHz at both 35 dBm and 30 dBm input power.

Second, based on the benefits of Klopfenstein taper, a promising DPA design is proposed since Klopfenstein taper has been replaced with tapered line. In fact, this substituting results on reducing the reflection coefficient of transformer.

This novel Doherty-like power amplifier has been fabricated using 15 W, 2.7 GHz, GaN HEMT transistors.

From a practical prototype realization, this modification has demonstrated that the resulting DPA BW is increased in comparison with the conventional topology while keeping the efficiency figures. Moreover, this study is shown that the Klopfenstein taper based design allows an easy tuning of the group delay through the output reactance of the taper, resulting in a more straightforward adjustments than other recently published designs where the quarter-wave transformer is replaced by multi-section transmission lines (hybrid or similar). Experimental results have shown 43-54% of drain efficiency at 42 dBm output power, in the range of 1.7 to 2.75 GHz. Concretely, the results presented in this novel Doherty-like power amplifier implies the specific load modulation technique that uses the mixed Klopfenstein tapered line together with a multi-section transformer in order to obtain high bandwidth with the relative efficiency in DPAs.

Keywords: Power amplifiers, OBO, Klopfenstein taper, Doherty power amplifier, wideband, GaN

Chapter 1

INTRODUCTION

1 Introduction

1.1 Motivation and statement of the problem

The power amplifiers (PAs) are the most power-consuming components in wireless transmitters. In the design of RF transceivers for modern communication systems, the non-linearity specification of PAs, which plays an important role in the bit error rate (BER) and adjacent-channel power ratio (ACPR) performance of radio frequency (RF) transceivers, has to be especially considered. With the evolution of RF standards, more complex signal modulation schemes have been presented to increase data transmission capacity. Therefore, in order to achieve to the broader bandwidths and higher peak-to-average power ratios (PAPR), RF PA designs will be targeted and get influence of these criteria. Normally, the efficiency of PAs is reduced while the PAPR is increased. These are due to the PAs have to amplify the signals in backed-off regions proportioned to the PAPR figures.

Based on the communication standards, with an increasing demand for higher data-rates, it has forced to use of advanced modulation formats with the information contained in the both amplitude and phase variations. Typically, the modern communication systems such as LTE, WiMAX, Satellite systems and Wi-Fi utilize the modulation schemes like M-QAM, CDMA and OFDM, with the high PAPRs where the PAs operate at an output power back-off. Based on working PAs in the back-off region, the performance of PAs is in the linear region and the efficiency degradation will occur in PAs chain. Hence, considering the linearity besides efficiency of PAs can be of a great importance. To tackle these problems, especially in linearity, some techniques have been proposed, such as Feedback (FB), Feed Forward (FF), and Predistortion (PD). More details about these techniques will be provided in future sections.

Furthermore, in order to enhance the back-off efficiency issue in the amplification, some strategies were suggested such as Kahn Envelope Elimination and Restoration (EER) [1], Envelope Tracking (ET) [2], Polar Transmitter (PT) [3], Linear Amplification with Non-linear Components (LINC) [4] and Load Modulation technique. These techniques are generally applied to enhance efficiency for high PAPR applications. All of these strategies have their own advantages and disadvantages that should be taken into consideration in order to select one. For

example, the EER adopts a saturated high-efficiency PA by using a driven switching current PA. Mentioned switches create constant envelope signal carrying phase information and amplitude information of the input signal. But the voltage supply tracking in the ET adopts by a linear PA. The main drawbacks of these methods are reduction of the efficiency in used modulator, the lack of broadband requirements in the amplitude path and the difficulty to sync the phase and envelop paths in PA. These matters lead to an increment of size and cost. In addition, the performance of PT is similar to the EER with a major advancement in utilizing the Digital Signal Processor (DSP) for modulating of digital signals. The principal drawback of the PT is synchronizing the modulated input signals related to delay matching [5]. Regarding this drawback, the dissipation of power can result in the form of heat. The insufficient bandwidth of the envelope path on the utilized DC-DC converter could be another problem of PT. LINC, based on the Chireix outphasing power amplifier, is a method of separating the signal into two vector summing constant amplitude phase-modulated signals to achieve efficient power amplification. Once the signal has been amplified by highly efficient (switched) amplifiers, both outputs are merged by means of a Chireix power combiner which uses parallel inductance and capacitance compensators for canceling the reactive part of the outputs. The matching of the delays between these two paths can be a problem, an issue that may reduce either efficiency or linearity. The last pointed technique is load modulation. The basic concept of this method is to change the slope of the load line match based on the instant demand of output power. The load impedance may be varied by a varactor based on a tunable matching network or by the Doherty technique. However, another solution can be the supply modulation that is based on controlling the supply voltage by envelope amplifier. More details will be discussed in the future sections.

As mentioned Doherty is a specific kind of load modulation technique which can deliver highly efficient operation at low output power levels, backed-off from maximum output power, without degrading any high power RF performances. Doherty PAs consist of two PAs namely peaking amplifier (PkA) and carrier (or main) amplifier (CA). The CA is typically biased at class AB and the PkA is typically biased at class C. Apart from some issues related to implementation constraints such as delay adjustments, reactance compensation or active devices biasing, the linearity and the insufficient bandwidth (BW) are drawbacks for using the Doherty PAs (DPAs) in broadband applications. The amount of fractional BW in conventional DPA is usually restricted up to 10%. This value is sufficient for a number of RF applications. However, other

ones require higher BW for base station configurations [6], [7]. Considering the fact that the biasing level of PkA is lower than CA, this will prevent the maximum PkA input drive to reach the acceptable maximum current level. Hence, the modulated load is not optimal and less power will be generated. Beside that in order to solve these problems, the trade-off among BW, gain, efficiency and linearity shall be considered. According to the mentioned discussion, the contribution of this study deals with the problem of enhancing the power efficiency and BW in DPAs using the proper technique related to impedance transformer in load modulation technique that will be justified later on.

1.2 Compromise between linearity and efficiency

Two significant factors in power amplifiers are linearity and efficiency. The trade-off between linearity and efficiency is unavoidable and achieving them is very difficult. Normally, reducing the nonlinearity requirements, which are related to the power efficiency, causes the transmission of signals whose peak amplitudes are below the compression point of the amplifier. So, in order to avoid the PA from these nonlinear effects, it is needed to operate more backed-off (far from the compression point) with the consequent degradation of the overall system efficiency. In other words, power efficiency performance gets influence from the input or output back-off (IBO, OBO respectively). In continue, some other impressment agents on efficiency and linearity will be mentioned in three levels of solution (device level, circuit level and system level) below.

The efficiency of an amplifier is a parameter to show how efficient DC power is converted to RF power, the common definition (drain efficiency) is expressed as:

$$\eta = \frac{P_{out}}{P_{DC}} \qquad [\%, \text{dimensionless}] \tag{1.1}$$

Moreover, in order to measure the actual power (previous definition may indicate a good efficiency even at 0 dB gain if $P_{out} = P_{in}$) we need to Power Added Efficiency (PAE) measurement. It is defined as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \qquad [\%, \text{dimensionless}] \tag{1.2}$$

On the other hand, linearity can be quantified in different ways, for example, in a two-

tone test, by the Third-order Interception Point (IP_3) or considering a modulated output signal spectrum by the Adjacent Channel Power Ratio (ACPR), defined in equation (1.3).

$$ACPR_{TOT} = \frac{P_{in-band}}{P_{adjacent-channel}} = \frac{\int_B P_{out}(f).df}{\int_{LS} P_{out}(f)df + \int_{US} P_{out}(f).df}[dB] \qquad 1.3$$

Furthermore, another way to indicate the performance of PA linearity with many carriers (>10) is using a noise power ratio (NPR) measurement technique. Usually, the NPR test generator consists of a white noise source connected in cascade with a bandpass filter and a notch filter. The notch depth which is the NPR amount can be measured with a Spectrum Analyzer.

1.2.1 Linearity

The linearity solutions can be classified into three different levels. These levels are discussed as follows [8] :

1- At the device level:

The applied semiconductor technologies are a solution at the device level for PAs linearization. A wide variety of semiconductor technologies exist: Si BJT, SiGe HBT, Si LDMOS FET, GaAs MESFET, GaAs HFET, GaAs HBT, SiC MESFET and GaN HEMT, which have been applied in RF power amplifiers. Based on PAs requirements, more specifically regarding the linearity and efficiency, each technology has been used for a particular application. For example, GaAs MESFETs are widely used in the semiconductor industry, due to their simple process and their excellent RF performance. Heterostructure FETs such as HFETs, p-HEMTs, and metamorphic high electron mobility transistors (m-HEMTs) provide a higher f_T and f_{max}, and a better noise figure and breakdown voltage compared to other device technologies, which makes them ideal candidates for Low Noise Amplifiers (LNAs) and PAs. Moreover, device technologies such as InP-based devices can be performed a great capacity for the quick and monolithic operation in RF circuit blocks with medium linearity. Nowadays, most of these technologies are nearly out of date, and the high demand for high power devices at higher frequencies made GaN technology important in the major market of the RF and microwave industry. It is worth mentioning that the GaN technology is flavored by two useful components Silicon and Silicon Carbide. They overcome the thermal dissipation problem shown in the pure

GaN technology and introduce two more suitable productions in GaN technology: GaN on Si and GaN on SiC. Because of the high cost of the SiC substrate, the development number of GaN on Si is 200 or 300 times greater than that of GaN on SiC [9], [10].

2- At the circuit level:

The main approach in this level is related to PA operation classes (i.e. Class A, AB, C, etc.). Each PAs are classified in specific classes based on its conductivity angle. This amount indicates the level of the conducted signal from the input to the output of the PA, and it has a direct relationship with both the power efficiency and the linearity of the PA. Typically, the theoretical conduction angles in these classes are 100% for class-A, 50% for class-B, and less than 50% for class C. Table 1.1 indicates the compromise between linearity and efficiency based on the operation class of PAs. In class C, the PA exhibits poor linearity and high efficiency. In classes A, B, and AB, the PAs present as linear PAs, with poorer efficiency. Classes D, E, and F behave as a nonlinear switching PA with a higher efficiency. However, it is important to consider some drawbacks in these PAs, which influence the efficiency and it will mention in the next sections. For example, based on the structure of classes D and E, the energy stored in the used capacitor is dissipated into heat through the switching operation. Moreover, in class F, the PAs have a complicated structure; also the harmonic resonators are difficult to control, which causes a loss of efficiency. Furthermore, the class-C, class-D, class-E, and class-F power amplifiers are, in different degrees, insufficient for non-constant amplitude applications [11].

Table 1.1 Theoretical efficiency and linearity performance for different PA classes of operation

Class of operation	Operation Mode	Maximum (theoretical) Efficiency (%)	Linearity
Class-A	Current source mode	50	Good
Class-AB	Current source mode	Better than Class-AB Worse than Class-B	Better than Class-B worse than Class-AB
Class-B	Current source mode	78.5	Moderate
Class-C	Current source mode	100	Poor
Class-D	Switch mode	100	Poor
Class-E	Switch mode	100	Poor
Class-F	Switch mode	100	Poor

In addition, linearization at the circuit level can be faced in three main approaches:

A. *Cancellation of Nonlinearities and Linear Transconductance Gain approach*

The main objective in this method is to cancel or reduce the nonlinearities which appears in the band due to the nonlinear gain of the PA device. Two techniques are considered as follows:

- *Harmonic Terminations:*

This technique applies the components to decrease the effects of third-order nonlinearities in the Intermodulation Products (IMP) generation. In this technique, a modulated second harmonic signal (centered at $2f_0$) is slowly mixed with the input of the power amplifier with the fundamental tone through the second-order non-linearity due to produce an in-band contribution. It can be adjusted to compensate or even completely cancel the corresponding term arising from third-order nonlinearity. For instance, in modern transmitters, PAs provide the harmonic termination network using open-circuit impedance in the drain of the transistors at odd-order harmonics and the short-circuit impedance at the even-order harmonics for class-F operation [12]. For more details, kindly refer to [13], [14], [15], [16] and [17]. The complexity of the harmonic termination circuit and its associated loss and required chip area are some drawbacks of this technique. Besides, inter-modulation distortion (IMD) sweet spots (operating points in the PA, where the nonlinearity is locally reduced from a two-tone test) can be used in order to improve linearity by controlling some relating factors to cancel the intermodulation components in PAs. The control factors such as gate bias voltage, input power, load impedance and temperature can affect the sweet spots. These relations are presented in [18], [19], [20]. In other words, the linearity modification using IMD sweet spots has been performed by controlling the load impedances and gate bias voltages in parallel-configuration PAs such as the N-way DPAs or balanced PAs [21], [22].

Derivative Superposition and Transconductance compensation:

Nonlinearity in Common Source (CS) FET amplifiers, mostly depends on the transconductance (g_m) non-linearity. This non-linearity can be expressed by applying the Taylor expansion series for the drain-source current i_{ds} such a CS FET: $i_{ds} = I_{dc} + g_m V_{gs} + (g_m'/2!)V_{gs2} + (g_m''/3!)V^3_{gs}$, where V_{gs} is a small-signal gate-source voltage and g_m (n) indicates the n-th

derivative of g_m with respect to V_{gs}. The derivative superposition technique [23] enhances linearity in the main transistor by minimizing the value of ($g_m''/3!$) V_{gs3}. Some relevant examples have been mentioned in [24] and [25].

B. *Active bias for dynamic power supply approach*

In this approach, using of active bias circuits to continuously optimize the performance of the circuit has a significant effect on improvement of the power efficiency in active devices. Active bias provides a possibility for lowering the power dissipation without a dominant decline in the circuit dynamic range or linearity. This method modulates the bias circuits when the receiver is near or in compression point [26], [27]. Since this technique utilizes active components such as transistor alongside other passive components, therefore, it prevents energy loss in the form of heat, size and cost increment.

C. *Thermal compensation approach*

Memory effects in power amplifiers can be divided into two main groups: electrical and thermal memory effects. Electrical memory effects are caused in a device by the delayed charge transport as so called charge carrier traps. This issue can be significantly reduced by a precise design of the biasing and matching circuit. Thermal memory effects fit into low modulation frequencies up to a few MHz and are brought by electro-thermal couplings. To overcome the difficulties associated with thermal memory effects, a compensation module can be employed. It required an accurate measurement of the memory effects in order to synthesize an allocated compensation module. For example, the compensation module could be found out by adding a memory effects compensator to a memoryless PD polynomial function. Some notable solutions are presented in [28] and [29].

3- At the System Level:

The system level of linearization can be categorized in 4 main families. Those four main families can be classified into two groups based on the linearity operation reason related to the distortion cancellation. These groups are as follows:

1. *Linearity aiming at distortion reduction:*

The two principal families of operation to reduce the distortion in the PA output area:

- FB:

In this technique, cancelling the distortion products are partially reduced by sampling the amplifier's output waveform and then processing, inverting and adding that with the input as it can be seen in Fig 1.1.

FB theory has been developed over time and plenty of advanced FB schemes have been proposed depending on the type of signal that is feed-backed ([30], [31], [32], [33] and [34]). This technique has a high risk of instability because the time delay introduced in the FB signal path. This fact causes in gain reduction and the bandwidth limitation. So, due to the enlarged BW needs in modern communications standards nowadays the use of FB technique is less common than before.

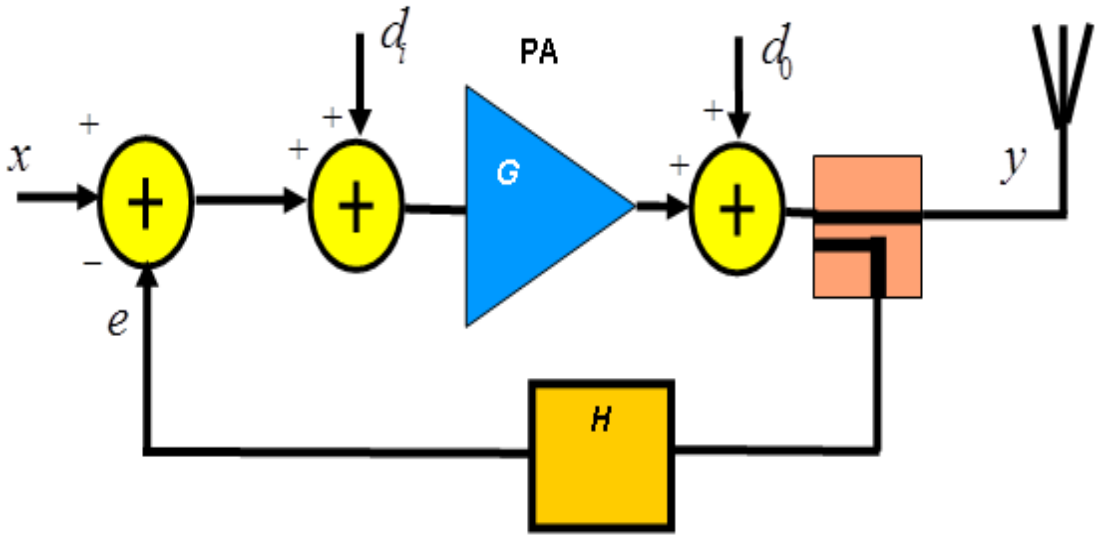


Figure 1.1 Basic structure of a classical FB

- FF:

The FF amplifier is recognized as a usable analog structure for wideband operation. It cancels the output signal distortion like FB method, but without considering the stability of the time delay of re-introducing an output sample at the input. As shown in Fig 1.2, two signal paths are included in this method. One of them is highly linear and carries a sample of the undistorted

output signal. The result of the comparison between this signal and sample of the main signal output path is an error signal consisting (ideally) of only distortion products. This error is inverted and added to the output signal to cancel some of the distortion products. Furthermore, delays are presented to match the main signal and the error channels.

FF is unconditionally stable (nevertheless, it does not imply a good behavior) and efficient for wide-bandwidth systems. Some patented progresses in basic FF structure are used to produce an arranged signal to control the phase and amplitude imbalances by using some pilot tones ([35], [36]). Moreover, in order to control the gain and phase components, compensation circuits have been used ([37], [38] and [39]). Generally, the problems with this technique consist of two aspects. First, the power efficiency is not high enough due to the need of using two PAs. Second, it is difficult to adjust the gain and phase compensation components if not using the automatic systems such as least mean square (LMS).

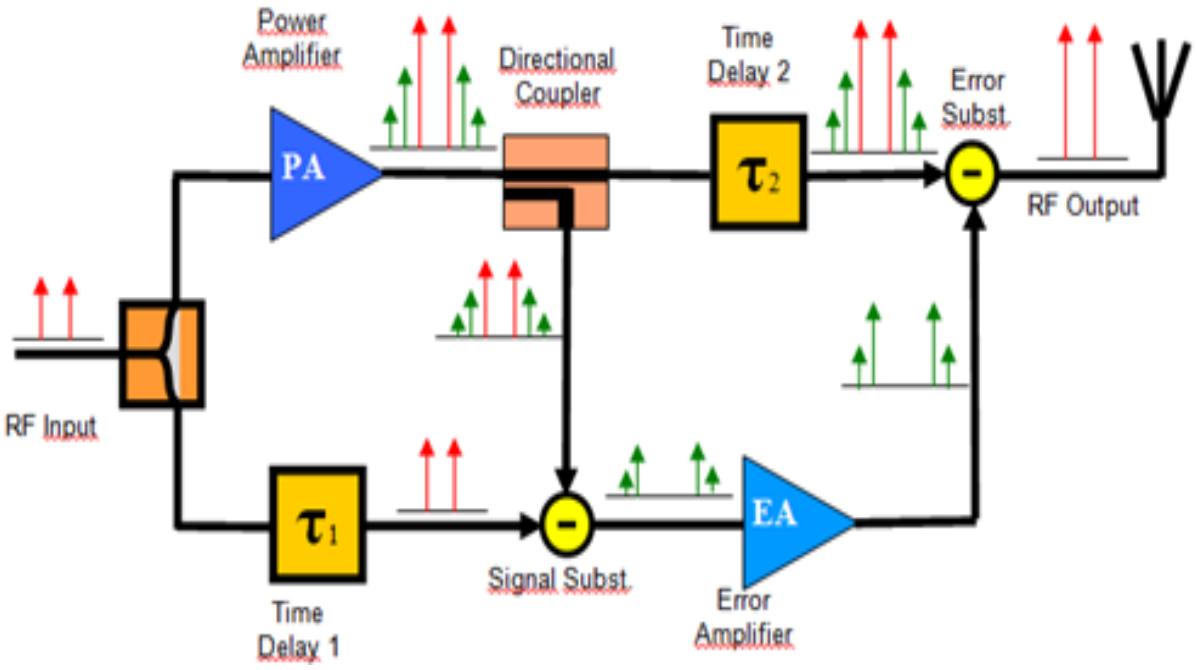


Figure 1.2 FF simplified block diagram and principles of operation

2. Linearization aiming at avoiding distortion:

In this principle the objective is to prevent from arising nonlinearities at the PA output by adjusting the operating point or from a previous source signal processing. The main

linearizing techniques related to this principle are:

- Power back-off tuning (not strictly a linearization technique, but the simplest one)

- Predistortion (analog or digital)

The basic idea of predistortion (PD) is the compensation of the nonlinearity of the PA by making a correction module. Typically, linearity improvement in RF systems by analog PD method is occurred by implementing a piecewise approximation of an amplitude transfer function that is opposite of the nonlinear amplifying device ([40], [41], [29] and [42]). In this way, the modification degree is limited by the accuracy and stability of the circuitry. Furthermore, considering the disadvantages of low bandwidth (in FB) or low power efficiency (in FF), PD linearization (analog and digital) provides a higher bandwidth and higher power efficiency linearization option. Digital predistortion (DPD) is nowadays a common solution for modern broadband communication transmitters, while the application of analog PD is shrinking and practically reduced to some particular satellite uses.

After the introduced solutions to linearity issues, the solutions for enhancing the efficiency are addressed as follows.

1.2.2 Power efficiency

The solutions of efficiency enhancement are classified into three levels as mentioned in the linearity section.

1. At the device level:

According to mentioned in linearity section, GaAs HEMT and InP HEMT technologies have a proper linearity and efficiency in RF applications. In addition, by developing high bandgap semiconductor materials, e.g. SiC and GaN, their roles are highlighted in the RF power technology [43]. Individually, GaN devices are recognized due to their high power density, gain and efficiency [44]. By comparing the material properties of Si, GaAs, SiC and GaN (Table. 1.2), it can be said that the technology of GaN is more suitable than other technologies for higher efficiency systems. In Table. 1.3, it has been indicated the advantages of

GaN-HEMT amplifier.

Table. 1.2 Material properties of common semiconductors devices [45]

Material	Breakdown electron field (MV/cm)	Heat conductivity(W/cm/K)	Traveling electron density(/cm^2)	Mobility (cm^2/Vs)	Saturated electron speed (cm/s)
Si	0.3	1.5	Up to 10^{12}	1300	$1*10^7$
GaAs	0.4	0.5	Up to 10^{12}	2000-4000(MESFET)	$1.3*10^7$
SiC	3	4.9	Up to 10^{12}	600	$2*10^7$
GaN	3	1.5	Up to 10^{13}	1500(HEMT)	$2.7*10^7$

High breakdown voltage

High-voltage operation

High-current-density operation

High-temperature operation

High-speed operation

High-efficiency operation

Table. 1.3 Advantages of GaN-HEMT amplifier [45]

Physical property	Advantage of HEMT technology	Advantage of HEMT as an amplifier
High breakdown voltage	High-voltage operation -High load impedance-Good linearity	Easy harmonic processing (higher efficiency) -Low matching loss -Simplified voltage conversion
Wide band gap	High-temperature operation	Small, lightweight cooling system
High heat conductivity -High current density	High-voltage operation -Small chip size	Small, lightweight amplifier

2. At the circuit level:

As shown in Table. 1.3, the linearity of PAs operation classes such as the class-D, class-E and class-F have a benefit to higher efficiency applications respect to other conventional PAs classes. Totally, these methods can be classified into two kinds of amplifiers: class F and switch-mode amplifiers. For instance, the class-D and class-E PAs are switch-mode. In these amplifiers, switch operation is performed by charging and discharging of the output capacitor (Fig 1.3). Furthermore, adjusting all harmonic components is conducted by using the LC resonator in these amplifiers. Hence, this performance is led to high efficiency in PAs. However, this point should not pass up the class-D PAs, which are limited to low-medium frequency

applications like, AM and short-wave broadcasting [46], [47]. Furthermore, an important drawback of these PAs (class-D and class-E) is based on the structure: the energy stored in the used capacitor is dissipated into heat through the switching operation.

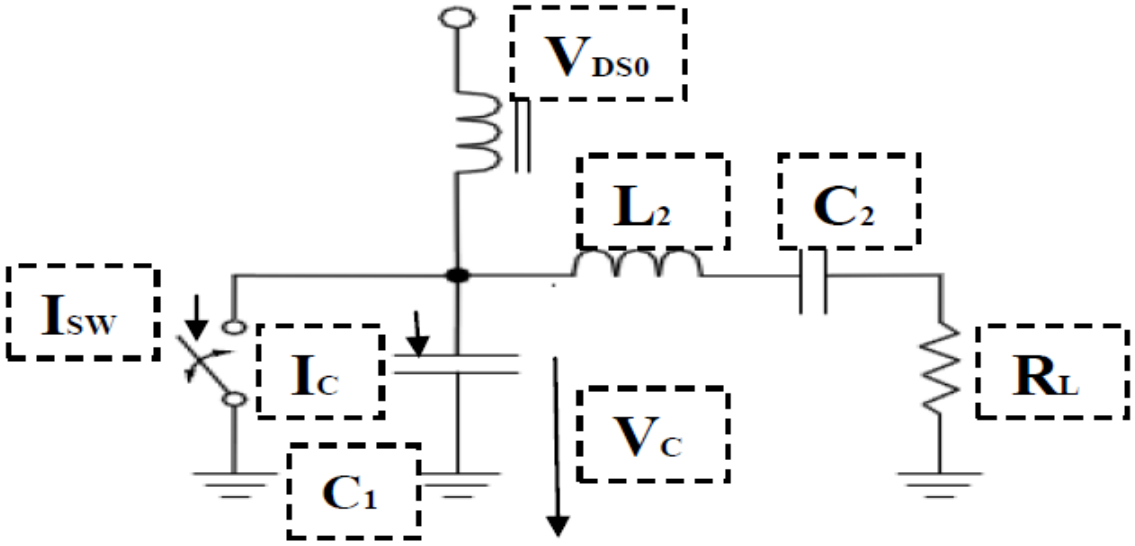


Figure 1.3 Schematic diagram of class- E amplifier

In addition, high efficiency can be fulfilled using the harmonically tuned PAs, such as class-F and class-F^{-1}amplifiers at the high frequency. The ideal class-F amplifier includes half-sinusoidal current and rectangular voltage waveforms. According to the Fourier series of both signals (just even harmonics for the rectified waveform of the sinusoidal current and odd harmonics for the rectangular voltage), the circuitry forces their profile by short or open circuiting through resonant networks in order to eliminate undesired harmonics, as shown in Fig 1.4. Thus, close to ideal waveform profiles avoids overlaps between the current and voltage, and so the internal dissipated power is theoretically null. Since harmonic power does not exist, the theoretical efficiency is 100% in class-F PAs. However, as mentioned above in practice this amount will be reduced based on more losses in coordination of even and odd harmonic components. Moreover, the drawback of class F PAs is related to complicated structure and also the harmonic resonators are difficult to control which cause the loss of efficiency due to the compromise between the harmonic filtering and the impedance matching.

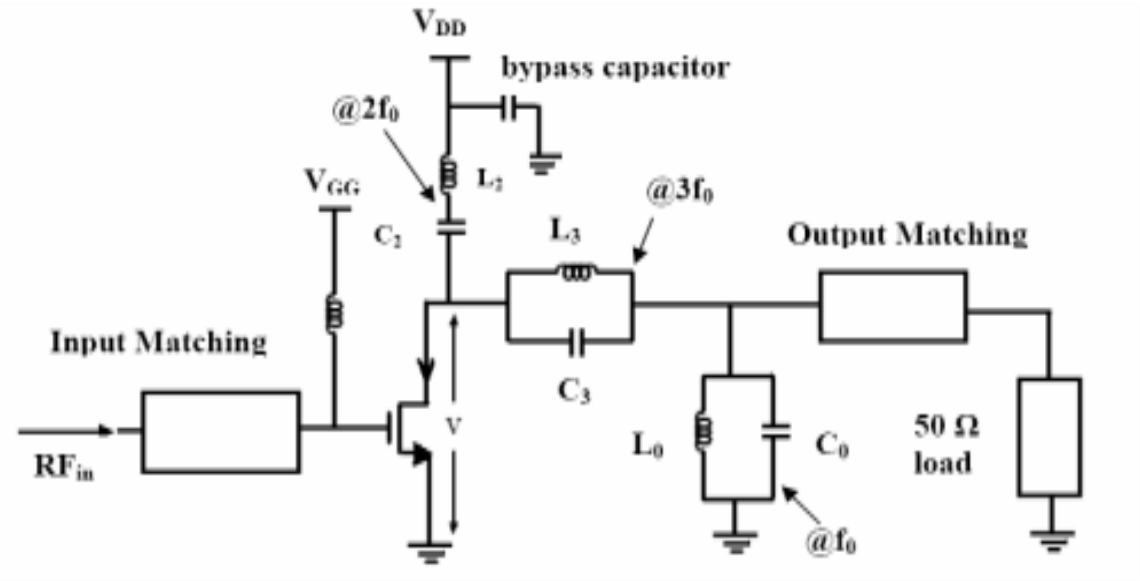


Figure 1.4 Schematic diagram of class-F amplifier [48]

The alternative way is the class-F^{-1}. It has used a dual of the class-F PA where the current and voltage waveforms are interchanged. This method can be another solution to enhance the efficiency as it is presented in [48], [49], [50], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61] and [62]. Furthermore, there are some other high efficiency classes such as G, H, and S. Such classes use different techniques to increase the efficiency. For example, G and H use resonators and multi power-supply voltage to reduce the average power consumption. While class-S uses a similar switching technique like class D and E.

3. At the system level:

This level can be organized by five different methods: EER, ET, PT, Chireix and DPA. Based on previous sections, the conventional and harmonically-tuned/switch mode PAs provide high efficiency in only near the maximum output power. Furthermore, the enhancement of the efficiency in output back- off could be a need. Thus, the five above techniques in system level can be proper for solving this problem.

-EER technique:

The EER method is a simple concept for improving amplifier efficiency. In this method the input signal passes through a limiter before being amplified. The output signal has

the constant amplitude besides retaining the phase modulation information. The amplifier can then be nonlinear, designed to operate in saturation plus maximum efficiency. In order to reform any amplitude modulation information to the signal, the envelope of the signal is extracted (before the limiter). This information is utilized to modulate the DC power supply of the amplifier as shown in Fig 1.5.

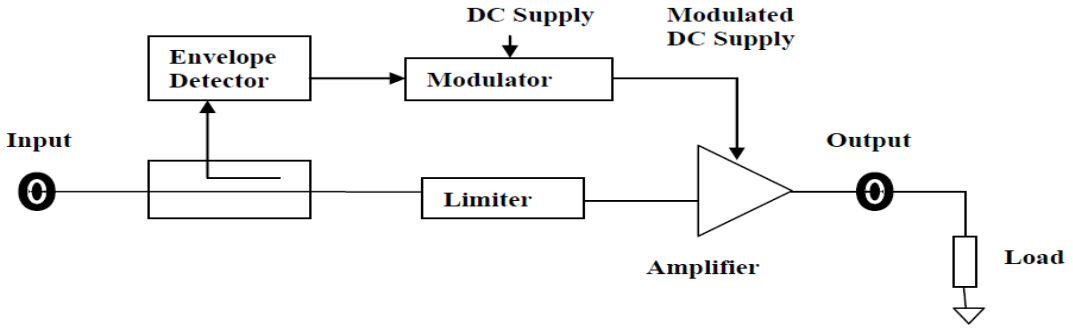


Figure 1.5 EER circuit design

The EER technique can have an excellent efficiency for all values of input power. However, in order to achieve the desired property numbers of challenges are inevitable. The most significant is necessity of a high efficiency power converter realization. Besides, all the major challenges for practical realization of EER RF PAs are outlined in Fig 1.6. More information is described in [63], [1], [2], [64], [65], and [66].

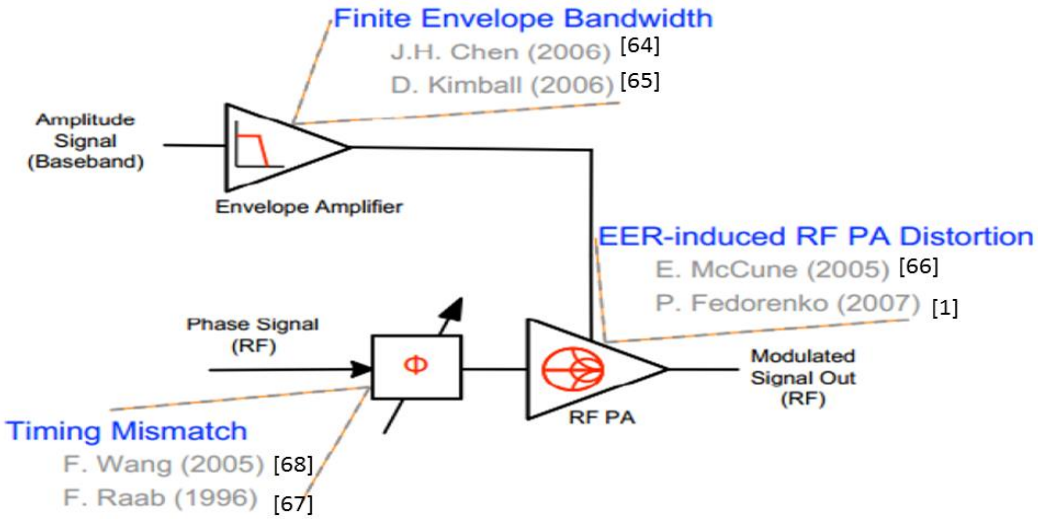


Figure 1.6 Challenges in practical implementation of EER systems

-ET technique:

ET method is similar to the EER method described previously. The limiter circuit is not essential as shown in Fig 1.7.

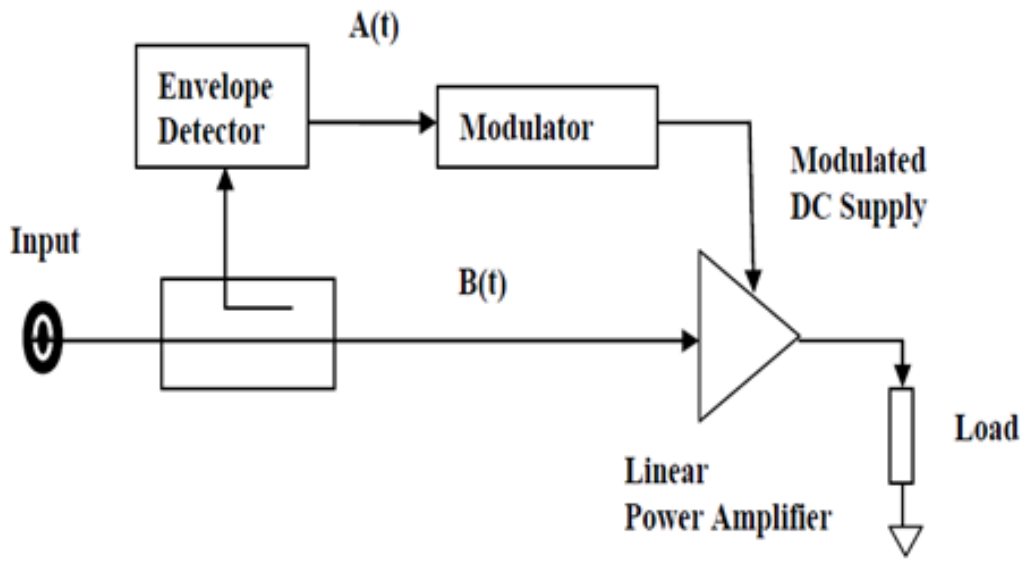


Figure 1.7 ET technique

The difference between this technique and EER is that the RF input signal contains both amplitude and phase information. Furthermore, the transistor is operated in a linear condition where the DC supply voltage is modulated with the input signal envelope. So, having a power source consummation is proportioned to the instantaneous value of the envelope. Based on that, gain reduction occurred in PA performance when operated in low-current conditions. The design of a highly-efficient DC modulator (with high output voltage and current) can be another challenge in this technique. In addition, since in this technique the supply modulation concept is applied by the voltage modulator, the challenging issue is to fulfill the high bandwidth requirements and a high efficiency at the same time. Nevertheless, this technique is more appealing than EER due to its simplicity and usage. Also, it has already been implemented in several RF applications for communication standards [67], [68].

-PT technique:

The PT is a modern type of EER that uses a DSP or similar device (i.e. FPGA) to generate the signals [69]. It provides a single architecture for different systems that may

eliminate some RF mixers with their associated spurious and leakage problems. The concept of polar modulation techniques is built on using magnitude and phase. In this way, applying the two resulting modulation components (phase and magnitude) is provided differently and more efficiently. Typically, the phase component PM and the amplitude component AM are applied using the phase-locked loop (PLL) and the PA respectively. Although, this technique can increase efficiency, extending battery life and leading to the higher output power capability but it has some drawbacks. One these depend on the restriction of bandwidth in the DC-DC converter in Polar system. Another one is related to mismatching the delays of the amplitude and phase paths that cause the increment of dissipation in the system [63].

- *Chireix technique:*

This technique is used to merge the output of two nonlinear amplifiers to amplify two input signals which have been obtained from the separation of an input signal into two components of constant amplitude and with different phases, as it has been elaborated in the previous section in the LINC transmitter (Fig 1.8). Important components in this technique are the AM-PM modulator and the output design of the power combiner. In the power combiner, inputted signals to combiner which convey two different paths have non-synchronous phase characteristics. However, this issue has been solved by a reactance compensation load design technique (combined LC resonance with the joint operation of the output impedances of both amplifiers) that has been led to improve the efficiency [4], [70].

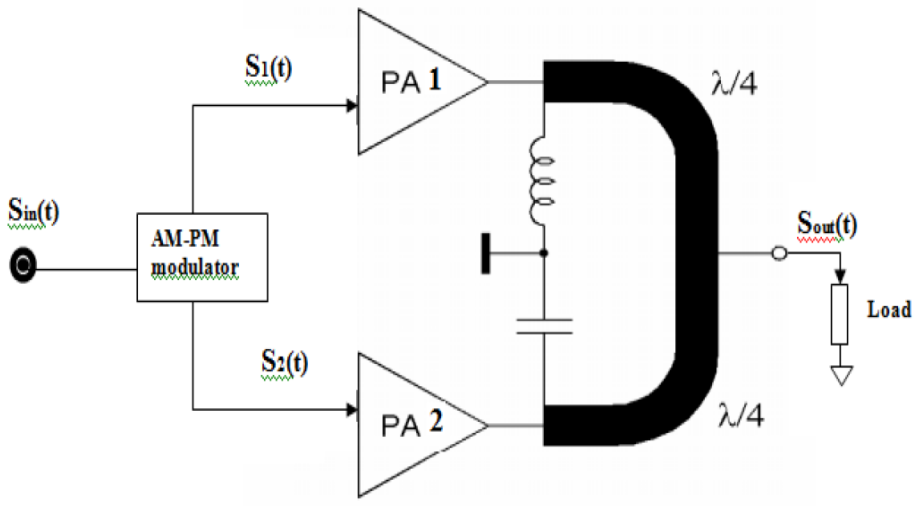


Figure 1.8 Chireix technique

-DPA technique:

The Doherty amplification, the core of this thesis, is one of the methods with a multi transistor approach to solve the low-efficiency PAs driven by communication signals with high PAPR. Typically, the implementation of a conventional Doherty amplifier consists of two amplifiers in which one operates as a class AB (main) and the other one as a class C (peaking) power stage (see Fig 1.9).

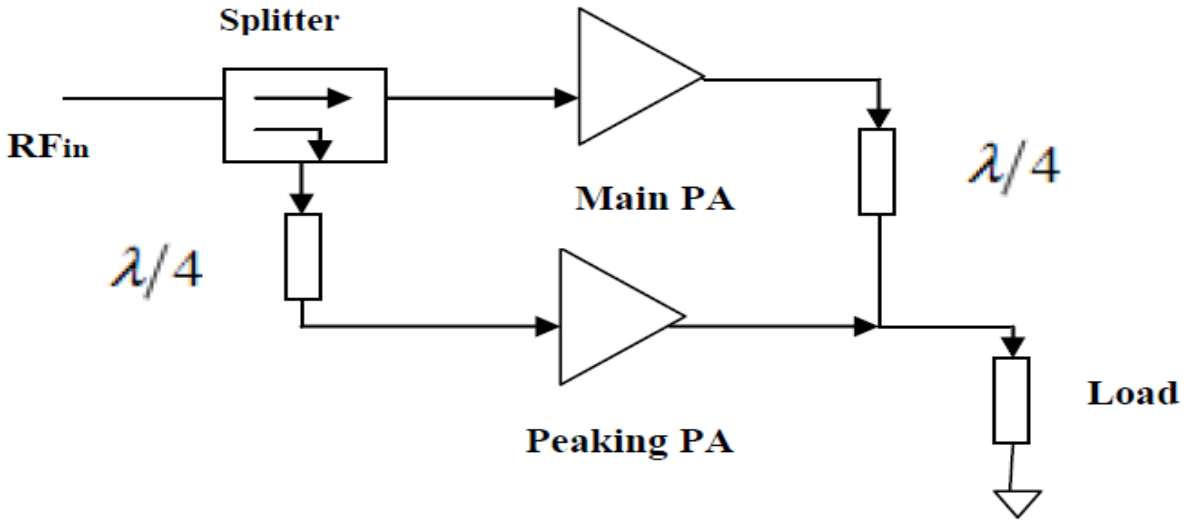


Figure 1.9 DPA technique

In this technique, the switching between each amplifier is performed directly without need to additional circuits, by the input power level when the PA is working. Besides, the output impedances of each amplifier are controlled by the loading from another amplifier. In this way, according to the close relation between load modulation and Doherty technique, this technique is described as below.

1.3 Load modulation

Load modulation is a technique in order to reach to a high efficiency for RF PAs in all of the cases. This technique performs by changing the effective load impedance seen by the transistor that is occurred during the variations in level of output power. Based on the DC load

line of transistors (see Fig 1.10), we can find the optimum load to reach the maximum efficiency. In this way, the so-called optimum load (R_{opt}) can be approximated from the DC load-line theory as shown in following:

$$R_{opt} = \frac{(V_{dc} - V_{Knee})}{I_{dc}} \quad 1.4$$

Where V_{dc} and I_{dc} are output bias voltage and current, and V_{knee} is the knee voltage. With this R_{opt} the maximum output power (P_{max}) and maximum drain efficiency (η_{max}) are given by:

$$P_{max} = \frac{(V_{dc} - V_{Knee})^2}{R_{opt}} = (V_{dc} - V_{Knee})I_{dc} \quad 1.5$$

$$\eta_{max} = \frac{P_{max}}{P_{dc}} = \frac{V_{dc} - V_{Knee}}{V_{dc}} \quad 1.6$$

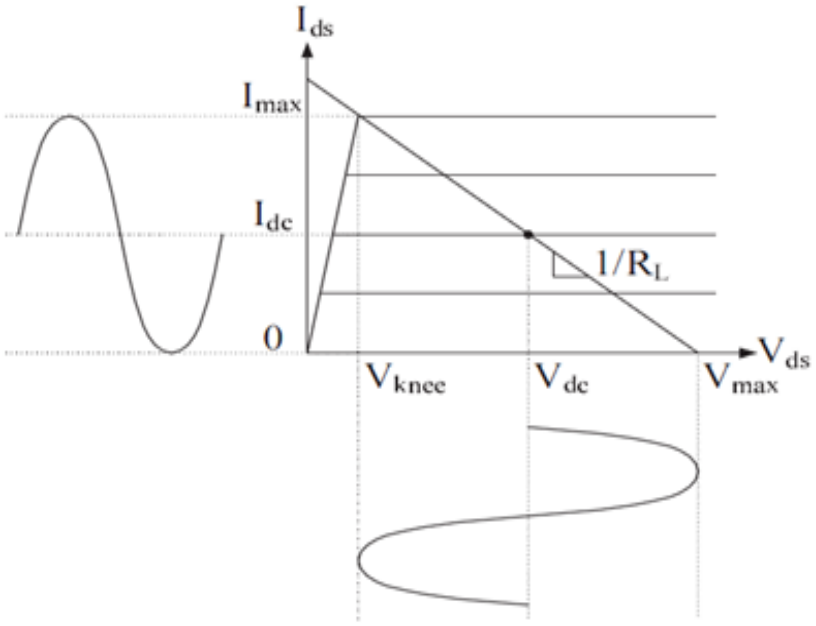


Figure 1.10 Ideal dc load line for the calculation of optimum load

By considering 1.5 can observe the maximum efficiency (about 100% theoretical) of PA by eliminating the V_{Knee}.

The load-line represents the maximum sinusoidal swing of the voltage (within the range between V_{max} and V_{Knee}) and current (between I_{max} and 0) of the transistor. This theory is used to

get a rough estimate of the load. Based on the target application, which could be maximum gain, maximum output power, maximum efficiency or maximum linearity of PAs, the load measurement is performed starting from this approach. Despite the practical problems, for example, parasitic of the components and biasing networks causing oscillation, this method is still a good approach for RF PAs [71]. Apart from DPA, feasibility of dynamic load modulation with varactor based networks is a proper method to modify the load and efficiency [72].

The basic concept in load modulation is to dynamically change the load line match depending on the instantaneous demand of output power level. As it can be seen, the mechanism of load modulation is shown in Fig 1.11. Based on the applied input power level the load line will change until reaching the maximum saturated power. These lines present the load values change from low power to maximum power in green, red and blue lines respectively (see Fig 1.11). As indicated the load impedance will be smaller by increasing the power level. More details on this technique, which has a vital role in DPAs, will be given in the next section.

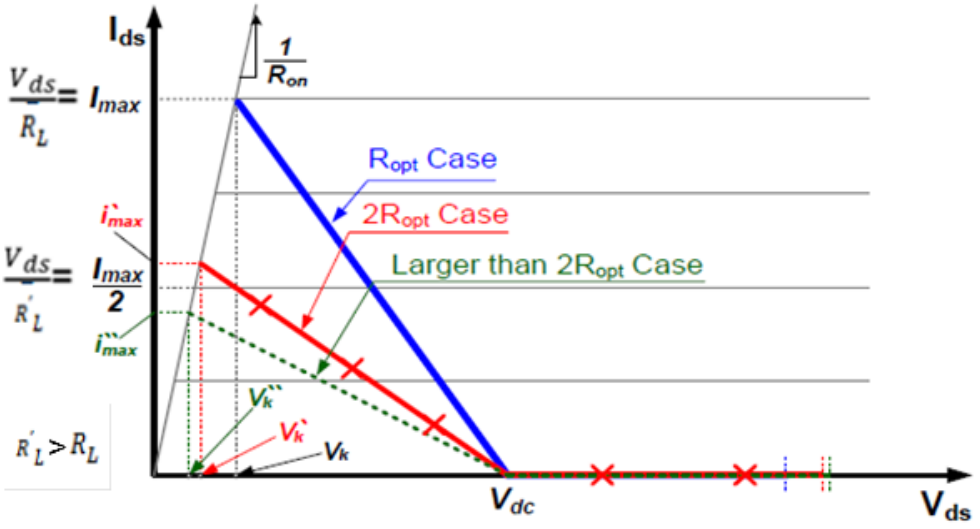


Figure 1.11 The performance of load curves in load modulation.

1.4 Doherty Power Amplifiers (DPAs)

As mentioned before, there are different approaches to achieve the efficiency enhancement PAs. For example, the Doherty amplifier and PAs with dynamically tunable matching networks are based on the dynamic modulation of the load. In DPA technique, it is easier to replace the power amplifiers using DPAs in the base stations rather than other techniques, which require the whole transmitter replacement instead of just the PA, a fact that affects the compatibility and cost.

The key advantages and disadvantages of DPAs, which they will be described in the next sub-sections, are the following [73],

Advantages:

1- Simpler to implement: The microwave Doherty amplifier can be realized using pure RF techniques to improve efficiency without using complex sub-paths and envelope control circuits which are used in envelope tracking techniques such as EER or ET.

2- Better power efficiency, respect to other techniques: The load modulation technique, using a quarter-wave transmission line, can deliver efficiency comparable to other advanced methods.

3- Direct replacement of, already existing PAs: The remaining sub-systems in the transmitter have not to be modified.

4- Adds little additional cost, as a consequence of the previous point.

Disadvantages:

1- Narrow bandwidth: Typically, caused by the quarter-wave transformer.

2- Poor output Standing Wave Ratio (SWR): It would be a problem if our concern is the possible impedance misadjustments due to the load modulation process which they may be solved by placing an isolator at the output guarantees good SWR.

3- Low IMD performance: The PkA may generate a large distortion due to a low biasing condition (class AB or C). The distortion components of the PkA can be released by the distortion components generated by the main amplifier if the bias condition is properly adjusted.

4- Questionable suitability in low power transmitters: the worthiness has to be carefully assessed in low power applications.

1.4.1 Fundamentals of the DPA

The DPA technique is one of the most common efficiency enhancement techniques. Due to its relatively simple circuits, it can achieve a significant efficiency enhancement at back-off operation with its inherent linearity [74], [75]. Its operation is based on the active load modulation principle. This principle is illustrated in Fig 1.12. Two amplifiers (modelled as current sources, generating the currents I_1 and I_2) are connected to a common load R_L.

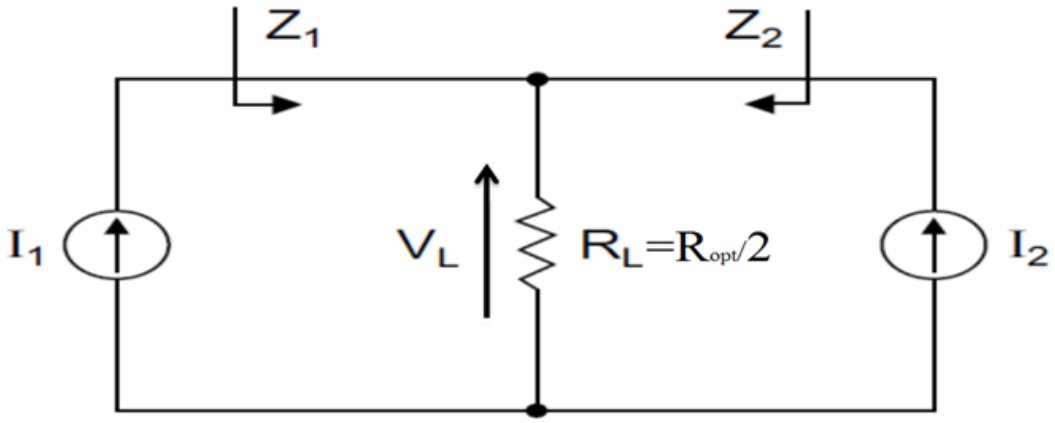


Figure 1.12 A simple schematic of load modulation [76]

The load modulation principle equations are the following:

$$V_L = R_L(I_1 + I_2) \qquad 1.7$$

$$Z_1 = \frac{V_L}{I_1} = R_L \frac{I_1+I_2}{I_1} = R_L\left(1 + \frac{I_2}{I_1}\right) \qquad 1.8$$

$$Z_2 = R_L \frac{I_1+I_2}{I_2} \qquad 1.9$$

From (1.7) it can be clearly noticed that the impedance seen by the amplifier to the left Z_1 can be changed (pulled) by changing the magnitude and/or the phase of the current I_2

generated by the other amplifier. As above mentioned the DPAs have used two devices; the main and the peaking devices having a common load and interconnected through a quarter-wave impedance inverter as shown in Fig 1.13. Since based on the changing load, need to the maximum efficiency of the main devices is important (by the current supplied by the peaking device), the output voltage swing should be kept at a constant value. Therefore, to reach this target, it is necessary to interpose an Impedance Inverter Network (IIN) between the load (R_L) and the main source, as shown in Fig 1.13. Based on this approach, the constant voltage value V_1at the main terminal will be transformed in a constant current value I_{1T} at the other IIN terminal, without considering the independent value of R_L.

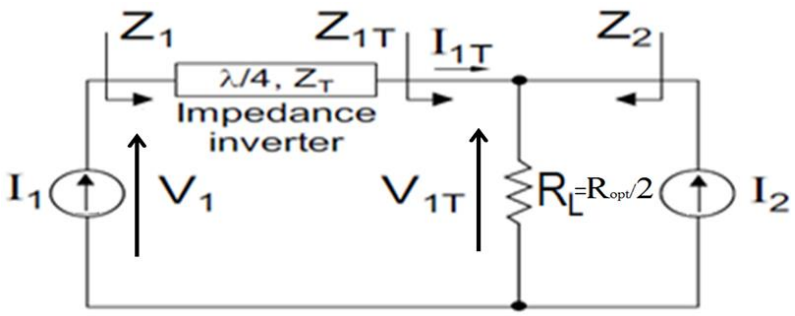


Figure 1.13 Simplified schematic of the Doherty amplifier [76]

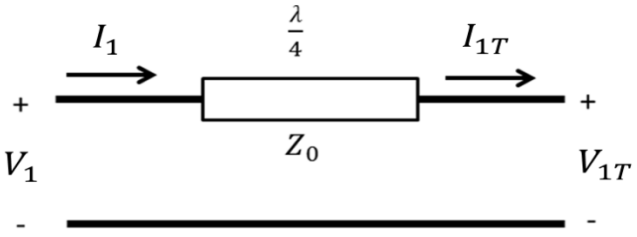


Figure 1.14 Quarter-wave transformer line as impedance inverter

Although, several design solutions could be chosen for the IIN implementations, but the most typical implementation is applying a quarter-wave transmission line ($\frac{\lambda}{4}$ TL) (see Fig 1.14) which is defined by an ABCD matrix as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & j.Z_0 \\ \frac{j}{Z_0} & 0 \end{bmatrix} . \begin{bmatrix} V_{1T} \\ I_{1T} \end{bmatrix} \qquad 1.10$$

Where Z_0 is the characteristic impedance of the line. Considering the equation 1.10, the direct dependence of the voltage at one side (V_1) with only the current at the other side (I_{1T}) through Z_0 is observable.

For a more details on the Doherty amplifiers, a typical DPA structure is presented in Fig 1.15. Its structure consists of two active devices that are connected by an IIN at the output of the main branch, a Phase Compensation Network (PCN) which are connected to the input of the peaking device and to the output of the main one (90 ° in the Fig 1.15). In addition, an input power splitter used to transfer the input signal in the proper ratio between two paths besides the output load (R_L).

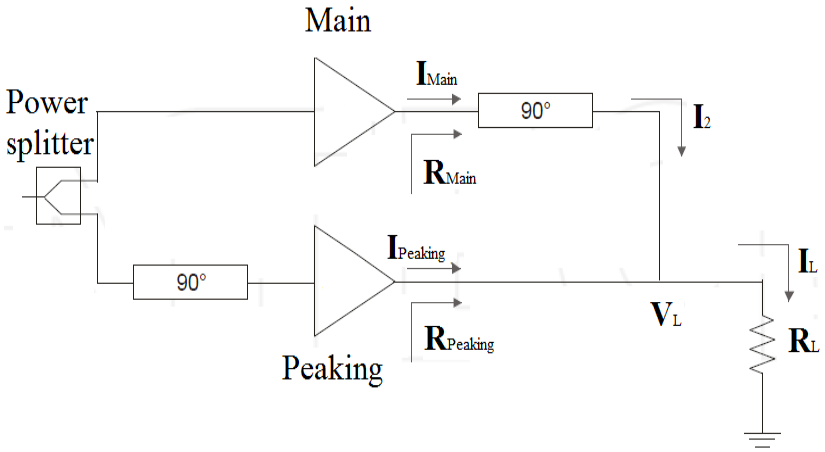


Figure 1.15 Typical Doherty amplifier structure

The PCN plays an important role to create a phase delay for coordination in phase of the output signals from the two active devices. Typically, the performance of conventional DPA is separated to two operating conditions. First, in the low input power level in which only the main device is on and the peaking device is kept off based on its class C bias behavior. Second, by increasing the input power level, the current fed the R_L by the main device rises, while the main device reaches to the saturation condition ($I_{critical}$). This causes the maximum efficiency condition. In this way, as we can see the expected load curve of both devices (main and peaking) in Fig 1.16 with the letter A, the corresponding input power level touches a “break point” condition. By increasing the input power level ($P_{in\_DPA} > P_{in\_DPA\ (break\ point)}$), the peaking device will turn on and the current will flow into the output load R_L. Based on this view, the impedance (Z_1) seen by the main device will modulate to a lower value by using the quarter-wave length

impedance inverter at the break point as shown in Fig 1.16 (load curve “A”). Besides, the efficiency of the main device will keep a constant value, while the increment of the efficiency of the peaking device will occur (see Fig 1.16) (referred as Doherty region). According to Fig 1.16 (letter ‘’C’’), in the peak envelope value, where both devices reach to their saturation corresponding the performance of DPA will terminate. Also, overall DPA efficiency (including the efficiency of the main and peaking devices separately) is presented in the Fig 1.17 based on the previous mentioned conditions (in low and medium level of input power).

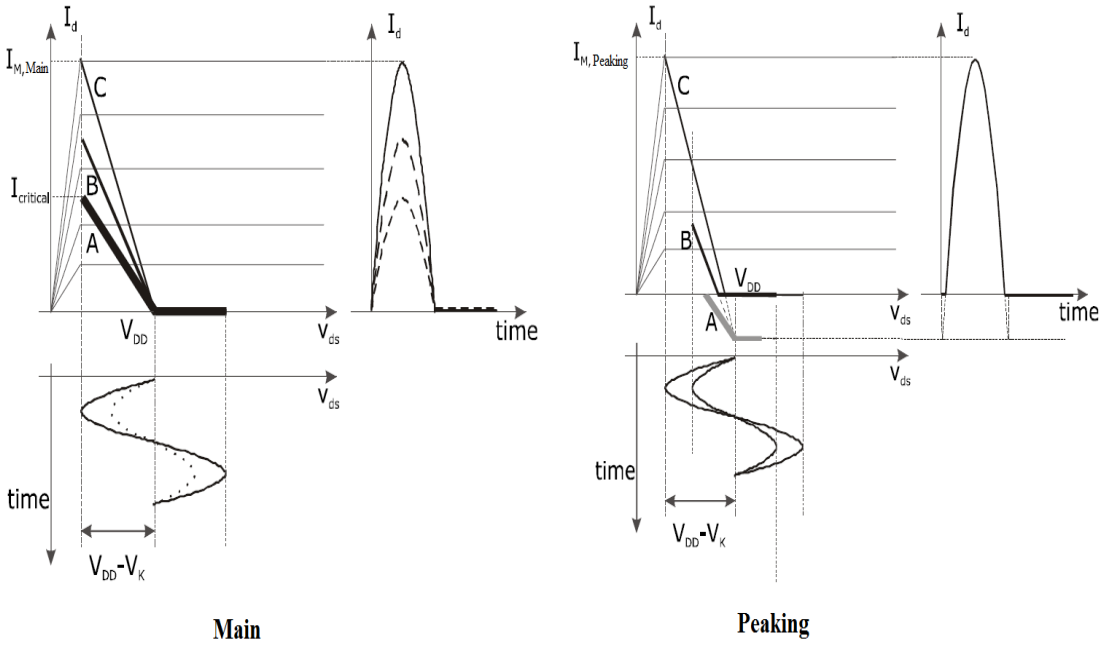


Figure 1.16 Evolution of the load curves for both DPA active devices: main (left) and peaking (right) amplifiers [77]

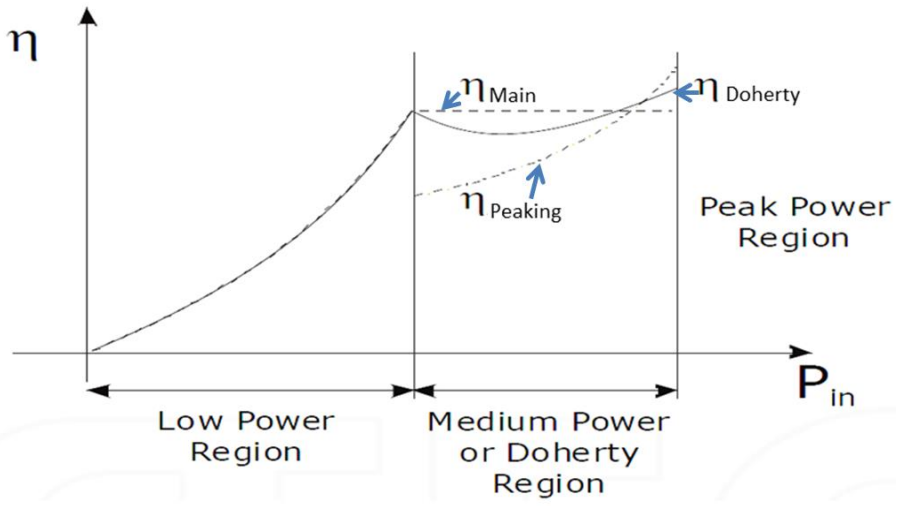


Figure 1.17 Typical DPA efficiency behavior versus input power [77]

The behavior of DPA can be analyzed regarding the changing the load impedances of two devices (main and peaking) based on mentioned conditions (at low power level and Doherty region) (see Fig 1.18a) as follows:

In this way, the value of OBO that will introduce below is assumed to be 6dB. The theoretical load impedances of the two amplifiers are expressed as (see Fig 1.13):

$$Z_1 = \begin{cases} \dfrac{Z_T^2}{R_L}, & 0 < v_{in} < V_{in,max/2} \\ \dfrac{Z_T^2}{R_L(1+\frac{I_2}{I_1})}, & V_{in,max/2} < v_{in} < V_{in,max} \end{cases} \quad 1.11$$

$$Z_2 = \begin{cases} \infty, & 0 < v_{in} < V_{in,max/2} \\ R_L\left(1+\frac{I_1}{I_2}\right), & V_{in,max/2} < v_{in} < V_{in,max} \end{cases} \quad 1.12$$

The output load impedances of the main and peaking amplifiers are shown in Fig 1.18b. Considering the low-power region (0 to $V_{in,\,max}/2$), the peaking amplifier is off, and the load impedance of the main amplifier is two times larger than that of the conventional amplifier (i.e. Z_{opt}=50 Ω). When the input voltage reaches to ($V_{in,\,max}$)/2, the saturation state obtains by the main amplifier. In other words, the maximum fundamental current swing is half and the maximum voltage swing reaches V_{dc}. Therefore, the maximum power level will result in half

value of allowable power level in main amplifier (as shown in Fig 1.20 at 6 dB down from the total maximum power).

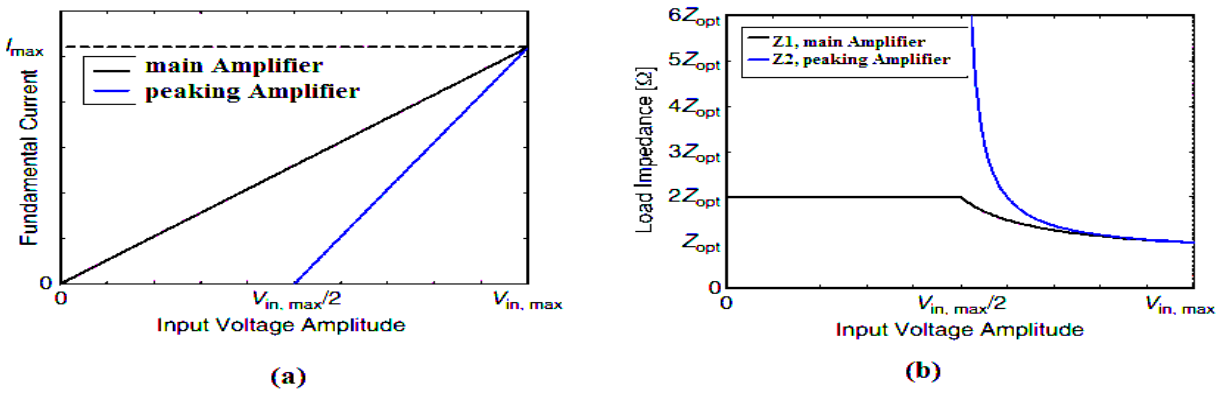


Figure 1.18 Fundamental currents versus input voltage (a), Load impedances versus input drive (b) in DPAs [78]

Furthermore, in the high-power region ($V_{in,\ max/2}$ to $V_{in,\ max}$), the peaking amplifier is starting to be on. As it has been described in Fig 1.18a, the current and voltage swings of the peaking amplifier increase depending on the input voltage level and the voltage swing reaches the maximum voltage swing of V_{dc}. Thus, changing the load impedances of the main and peaking amplifiers occur from $2Z_{opt}$ (100 Ω) to Z_{opt} (50 Ω) and ∞ to Z_{opt} (50 Ω) respectively depends on the input voltage level as shown in Fig 1.18b. These changes would also be shown in Figs 1.19a and 1.19b based on Z_{opt}=50 Ω. In this view, Figs 1.19a and 1.19b indicate the performance of DPA in the low and high power levels respectively. In both conditions, considering the impedance inverter (90 º in Fig 1.15) performance, the load impedances of the main and peaking amplifiers change based on given information and the value of impedance in point ‘’A’’ lead to 25 Ω. This impedance would be transformed to the output impedance (R_L=50 Ω) by using a 35 Ω transmission line as depicted in Fig 1.19.

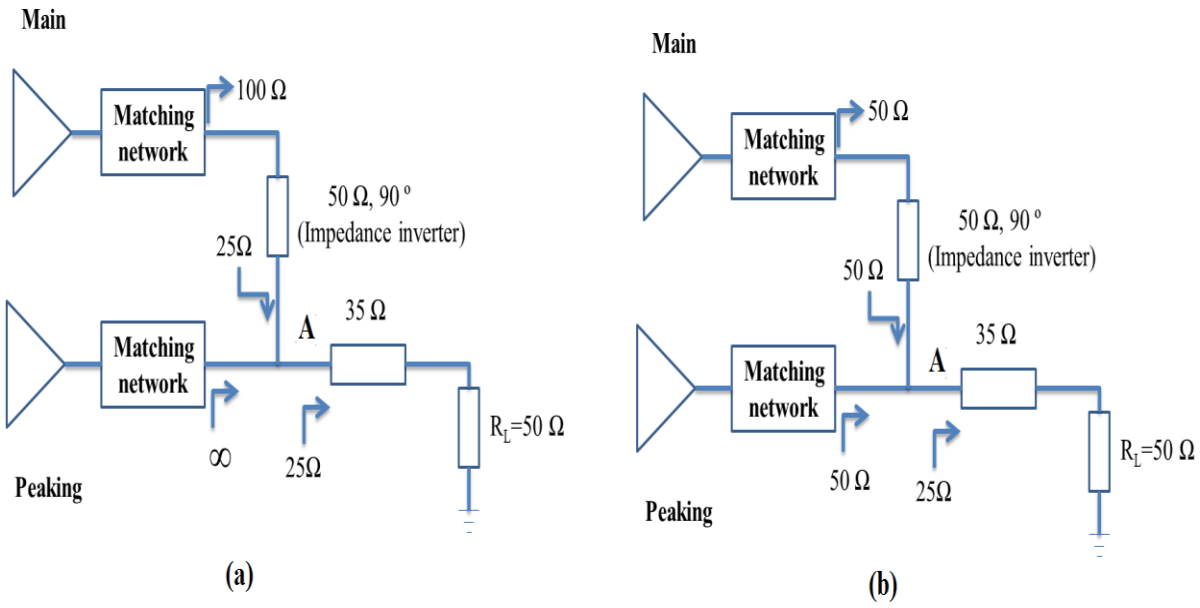


Figure 1.19 Schematic of DPA performance based on changing the load impedances of the main and peaking amplifiers in low (a) and high (b) power region

Regarding the change in impedances performance in different power levels of the main and peaking amplifiers, the efficiency of DPA is shown in Fig 1.20. Furthermore, it can be said a DPA with a high efficiency for a large PAPR signal in comparison with conventional class AB amplifiers as depicted in Fig 1.20.

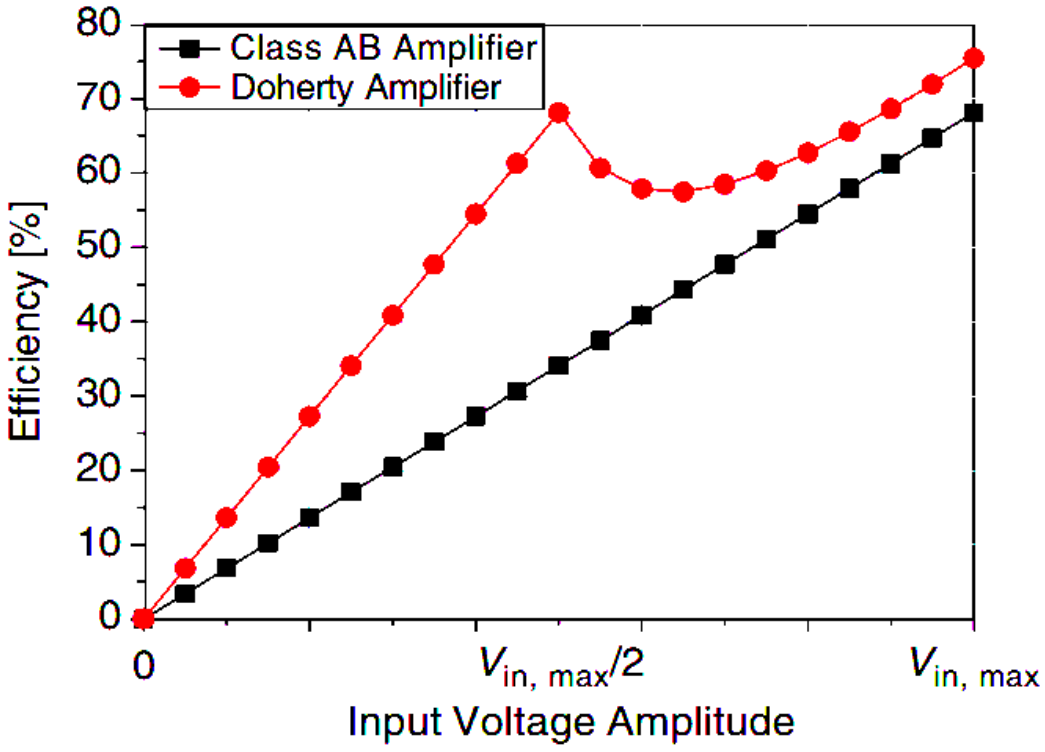


Figure 1.20 Plot of efficiencies versus the input drive level for the Doherty amplifier and the class AB amplifier [78]

1.4.2 Asymmetrical power splitting

In the previous sub-section we have introduced the DPA by assuming a 6 dB OBO value, which is the usual value for basic designs and for explanations because the associated voltage level is 1:2 (Fig 1.18a): the peaking power amplifier is switched-on at half the dynamic range of the input voltage. However, the OBO value has to be compliant with the PAPR of the signal in order to be amplified, and this is happening by adjusting asymmetrically the power splitter. Additionally, because, the different types of PAs are used in the DPA, the gain of the main and the peaking ones are different, and so it should be necessary to readjust the splitting of the input power to compensate the gain differences.

The first design step begins by identifying the OBO level that can be affected to the efficiency of DPA. Also, it is necessary in DPA for accounting the PAPR of the application which applied by the relative DPA. The definition of OBO is following the equation 1.13:

$$OBO = \frac{P_{out,DPA(x=x_{break})}}{P_{out,DPA(x=1)}} = \frac{P_{out,Main(x=x_{break})}}{P_{out,Main(x=1)}+P_{out,peaking(x=1)}} \quad 1.13$$

Where the mentioned subscripts depend on the whole DPA (in the main and peaking amplifiers). Besides, a parameter x ($0 \leq x \leq 1$) is used in order to determine the dynamic point depends on the applied input power. For example, the quiescent state (when the RF signal is not applied to the input) points to x=0, and the saturation condition (when the DPA reaches its maximum output power level) presents by x=1. Plus, the break point condition (when the peaking amplifier is turned on) identifies by $x = x_{break}$.

In continue, by considering the changes of the load lines of main and peaking amplifiers for $x = x_{break}$ (load curves "A" in Fig 1.16) and x=1 (load curves "C" in Fig 1.16) the relation of OBO and the ratio between the main device currents at x=1 and $x = x_{break}$ can be estimated.

The value of bias voltage and drain voltage amplitude of the main device for $x = x_{break}$ and x=1 are assumed V_{DD} and V_{DD}-V_k respectively. Besides, as presented in Fig 1.16 (load curve ''C''), the drain voltage of the peaking device for x=1 will reach the same amplitude value.

Based on the mentioned criteria, the output powers delivered by the main and peaking amplifiers will define:

$$P_{out,main(x=x_{break})} = \frac{1}{2}.(V_{DD} - V_K).I_{1,main(x=x_{break})} \quad 1.14$$

$$P_{out,main(x=1)} = \frac{1}{2}.(V_{DD} - V_K).I_{1.main(x=1)} \quad 1.15$$

$$P_{out,peaking(x=1)} = \frac{1}{2}.(V_{DD} - V_K).I_{1.peaking(x=1)} \quad 1.16$$

Where the added subscript "1" in the current is referred to its fundamental component By considering the performance of the lambda quarter wave length based on its defined by ABCD matrix and the combination of some equations that refer to [79] with the above ones, it can be written:

$$V_{L,(x=x_{break})} = (V_{DD} - V_k).\frac{I_{1,main(x=x_{break})}}{I_{1,main(x=1)}} = \alpha.(V_{DD} - V_k) \quad 1.17$$

Where α is the ratio between the currents of the main amplifier at $x = x_{break}$ and x=1.

$$\alpha = \frac{I_{1,main(x=x_{break})}}{I_{1,main(x=1)}} \quad 1.18$$

Accordingly to satisfy two conditions occurred by the voltage and current ratios at $x = x_{break}$ and x=1, the output resistance (R_L) calculates respectively:

$$R_L = \frac{V_{L,(x=x_{break})}}{I_{2(x=x_{break})}} = \frac{\alpha.(V_{DD}-V_k)}{I_{1,main(x=1)}} \quad 1.19$$

Thus, from combining the previous equations it follows:

$$I_{1,peaking(x=1)} = \frac{1-\alpha}{\alpha}.I_{1,main(x=1)} \quad 1.20$$

$$OBO = \alpha^2 \quad 1.21$$

Which shows that, the ratio between the main amplifier currents for $x = x_{break}$ and x=1 is fixed also by choosing the desired OBO. Based on the mentioned relation between OBO and the ratio of the main device current at $x = x_{break}$ and $x = 1$, a degradation of power efficiency by increasing the value of OBO and inversely can be seen.

Consequently, since the maximum output power value of DPA is obtained in x=1, it can be estimated in another way by the following equation:

$$P_{out,DPA(x=1)} = P_{out,main(x=1)} + P_{out,peaking(x=1)} = \frac{1}{\alpha}.\frac{1}{2}.(V_{DD}-V_k).I_{1,main(x=1)} \quad 1.22$$

Also, by identifying the maximum current at fundamental, the values of R_L will compute by 1.19 and it is possible to calculate the required characteristic impedance of the output $\frac{\lambda}{4}$ TL (Z_0) as follows:

$$Z_0 = \frac{(V_{DD}-V_k)}{I_{1,main(x=1)}} \quad 1.23$$

It is assumed that the output voltage (V_L) achieves the $V_{DD}-V_K$ value for x=1. Obviously, based on the value of $I_{1,\,main(x=1)}$, the main device maximum allowance output current I_{max} and its chosen bias point will be estimated.

In the previous analysis the OBO has been adjusted, independently of their different biasing and the power gain, by only considering the power splitting between both PAs. Following are the analyses of the main and peaking device's currents behavior based on their bias points. In order to facilitate current analyses of DPA, a simplified current waveform is presented by assuming a generic class AB bias condition regarding Fig 1.21. Based on this assumption the following parameter defines:

$$\xi = \frac{I_{DC,main}}{I_{Max,main}} \qquad 1.24$$

Where $I_{DC,main}$ is the quiescent (i.e. bias) current of the main device. According to different values of ξ, the bias conditions would be occurred in class A, class B and class AB. For example, ξ =0.5 and ξ =0 identify a Class A and Class B bias conditions, respectively, while $0< \xi < 0.5$ refer to a class AB bias condition.

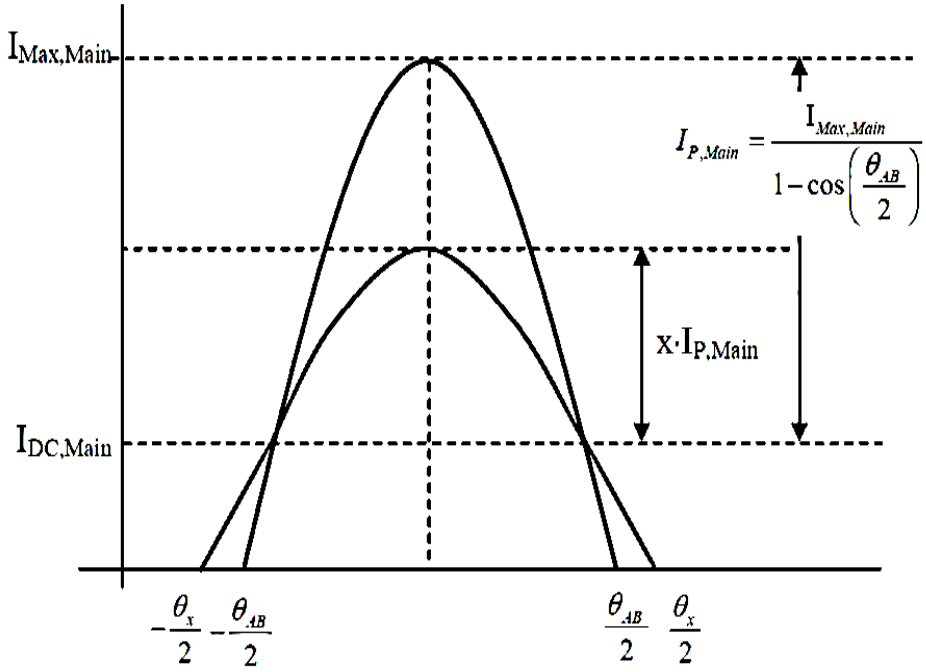


Figure 1.21 Current waveform in time domain of the main amplifier [79]

Describing the current waveform of Fig 1.21 is given below:

$$I_{D,main} = I_{DC,main} + x.\frac{I_{Max,main}}{1-\cos\left(\frac{\theta_{AB}}{2}\right)}.\cos(\theta) \qquad 1.25$$

Whose fundamental component can be expressed:

$$I_{1,main(x=1)} = \frac{I_{Max,main}}{2\pi} . \frac{\theta_{AB} - \sin(\theta_{AB})}{1-\cos(\frac{\theta_{AB}}{2})} \quad 1.26$$

Where $\theta_{AB}$the current conduction angle (CCA) of the main output current, achieved for x=1. The relationship between the bias point ξ and the CCA θ_{AB}can be easily shown by the following:

$$\theta_{AB} = 2\pi - 2\arccos(\frac{\xi}{1-\xi}) \quad 1.27$$

The value of $I_{Max,main}$ that required to reach the desired maximum power can be estimated by manipulating the equation 1.26, where the bias point ξ of the main amplifier has been selected.

As we indicated in the previous equations to the current performance of main amplifier, the maximum current value of the peaking amplifier can be obtained by using the equation of the first order coefficient of the Fourier series, since the value of $I_{1,peaking,(x=1)}$ should fulfill 1.20.

Therefore, it follows:

$$I_{1,peaking(x=1)} = \frac{I_{Max,peaking}}{2\pi} . \frac{\theta_c - \sin(\theta_c)}{1-\cos(\frac{\theta_c}{2})} \quad 1.28$$

Where θ_c is the CCA of the peaking device output current for x=1. Based on the Fig 1.17 (the current waveform of the peaking amplifier) and assuming a virtual negative bias point, the peaking device current is defined same as the equation 1.24, thus:

$$I_{D,peaking} = I_{DC,peaking} + x. \frac{I_{Max,peaking}}{1-\cos(\frac{\theta_C}{2})} . \cos(\theta) \quad 1.29$$

As highlighted in Fig 1.22 the peak of the current has to reach zero for $x=x_{break}$ in order to achieve proper performance in peaking amplifier. Based on this condition:

$$x_{break} . \frac{I_{Max,peaking}}{1-\cos(\frac{\theta_C}{2})} = -I_{DC,peaking} \quad 1.30$$

According to direct relationship between x_{break} and $\theta_c(\theta_C = 2.\arccos(x_{break}))$ and

manipulating the equation related to $I_{D,main}$, the value of x_{break} will identify.

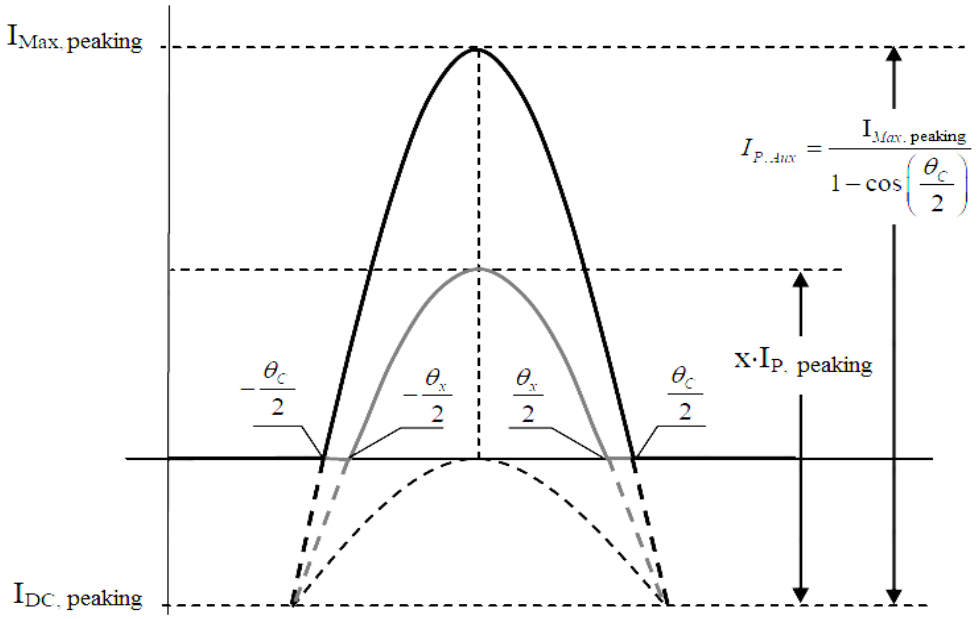


Figure 1.22 Current waveform in time domain of the Auxiliary amplifier for $x=x_{break}$ and x=1 [79]

Based on above mentioned descriptions, the value of x_{break} , α (related to OBO) and ξ (related to the main device bias point) will fix. Since the value of $I_{Max,peaking}$ is obtained, the value of $I_{DC,peaking}$ is calculated as follows:

$$I_{DC,peaking} = -I_{Max,peaking} \cdot \frac{x_{break}}{1-x_{break}} \qquad 1.31$$

Based on these discussions, the ratio between the maximum currents can be considered by the required devices in DPAs. As shown in Fig 1.23, this ratio is as a function of OBO and ξ. Regarding Fig 1.23, the coherence of ξ is negligible in the very high OBOs. Moreover, the same value of maximum current will be occurred in near 5dB OBO, while providing the greater OBO is possible by higher current of peaking device.

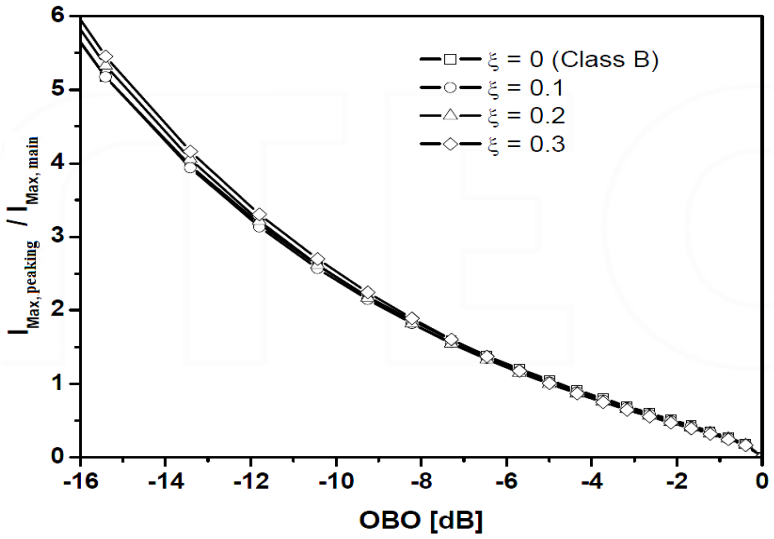


Figure 1.23 Ratio between Auxiliary and Main maximum currents as function of OBO and ξ [80]

Totally, the maximum current ratio can be used as useful information to choose the proper device periphery.

Another highlighted subject in DPAs is considering the power splitter dimensioning. It can influence in the power gain of DPAs. Accordingly, to have a critical role by power splitter in DPA architecture, the simplified analysis is described as follows.

Based on an active device with the constant transconductance (g_m) and definition of $V_{gs,main(x=1)}$, $V_{gs,peaking(x=1)}$ in [79] with merging the previous equations the power values at the input of the devices can be derived as follows:

$$P_{in,main(x=1)} = \frac{1}{2}.\frac{(V_{gs,main(x=1)})^2}{R_{in,main}} = \frac{1}{2}.\frac{(I_{Max,main}.(1-\xi))^2}{R_{in,main}.(g_{m,main})^2} \quad 1.32$$

$$P_{in,peaking(x=1)} = \frac{1}{2}.\frac{(V_{gs,peaking(x=1)})^2}{R_{in,peaking}} = \frac{1}{2}.\frac{(I_{Max,peaking})^2}{R_{in,peaking}.(g_{m,peaking}.(1-x_{break}))^2} \quad 1.33$$

Where $R_{in,main}$ and $R_{in,peaking}$, the input resistors of the main and the peaking devices, respectively. Furthermore, by defining the splitting factors of $\Lambda_{main} = \frac{P_{in,main}}{P_{in,DPA}}$ and $\Lambda_{Peaking} = \frac{P_{in,peaking}}{P_{in,DPA}}$ for main and peaking amplifier respectively, the ratio $\frac{\Lambda_{Peaking}}{\Lambda_{main}}$ can be computed as:

$$\frac{\Lambda_{peaking}}{\Lambda_{main}} = \left(\frac{I_{Max,peaking}}{I_{Max,main}}\right)^2 . \frac{R_{in,main}}{R_{in,peaking}} . \left(\frac{g_{m,main}}{g_{m,peaking}}\right)^2 . \frac{1}{[(1-\xi)(1-x_{break})]^2} \qquad 1.34$$

According to the relationship between the splitter factors and input powers of the main and peaking amplifiers, the power gain of the whole DPA is given by:

$$G_{Doherty} = G_{main} . \Lambda_{main} + G_{peaking} . \Lambda_{peaking} \qquad 1.35$$

The computed values for $\Lambda_{peaking}$, as function of OBO and ξ parameters, by assuming the same values for g_m and R_{in} for both devices is reported in Fig 1.24.

In this Figure, requiring an uneven power splitting is highlighted so that a large amount of input power has to be sent to the peaking device. For instance, regarding a DPA with 6dB OBO and a class B bias condition (i.e. $\xi = 0$) for the main amplifier, the ratio of applied input power in order to provide peaking and main device is 87% to 13% respectively. However, it is important to consider the degradation of gain in this condition rather than using a single amplifier. Regarding the previous discussions, the relationship between design parameters of DPAs besides its performance investigated. In addition, the important roles of OBO and the ratio of power splitter in power efficiency and power gain identified respectively.

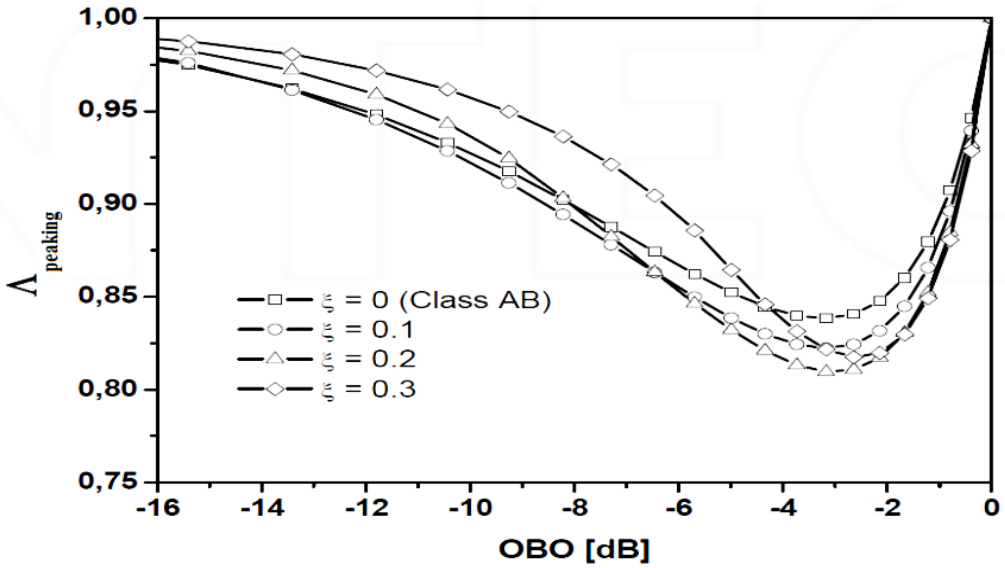


Figure 1.24 $\Lambda_{peaking}$behavior as a function of OBO and ξ, assuming for both devices the same values for g_m and R_{in} [80]

1.5 An overview of the rest of the thesis

In chapter 2, a summary of the state of the art DPAs on its solutions and trends to improve the efficiency and BW besides of its linearity will be discussed. Individually, in the different sections of this chapter the most important applications of DPA with its applied device technologies have been presented. In addition, the main adopted solutions for DPA efficiency and linearity improvement, together with some enhancing BW techniques, are described. Other sections of this chapter consist of multi-band DPAs and the integrated solutions.

Chapter 3 involves in a preliminary design of the DPA to reach a proper implementation considering the trade-off between BW and efficiency. Furthermore, the analysis includes DC simulations, nonlinear load-pull simulations and small signal S-parameters simulations as well as the measurement results of designed DPA in sketch; that are discussed and extended to the new approach of impedance inverter networks in the next chapter.

In chapter 4, it is presented the main contribution of this thesis, which describes a method to utilize a novel impedance transformer network in DPAs to derive a convenient fractional BW, besides a proper power efficiency alongside its simulations and laboratory measurements. Moreover, the comparison between the implemented DPA and other recently published implementations is presented.

Finally, chapter 5 presents a conclusion about the implemented DPA design, as well as some suggestions in future work in order to progress this thesis.

List of published papers on this research:

Letter:

-Eduard Bertran, **Mehran Yahyavi**, ***'' A Wideband Doherty-like Architecture using a Klopfenstein Taper for Load Modulation''***, IEEE Microwave and Wireless Components Letters (MWCL), vol 25, no. 11, pp:760-762, Nov 2015.

Conference paper:

- **Mehran Yahyavi,** Eduard Bertran, '' ***A Doherty Power Amplifier based on a Tapered Line Impedance Inverter''.*** In Proc. 2014 IEEE 11th International Multi-Conference on Systems, Signals & Devices (SSD-14) 11-14 February 2014.

Chapter 2

State of the art in DPAs

2 State of the art in DPAs

2.1 Introduction

According to the main objective of DPAs to increase efficiency while maintaining linearity and filling the specified bandwidth, in this section a survey on the state of the art in advanced design aspects of DPA will be presented. Most important manufacturers of PAs have already outpaced for using in DPA research. Nowadays it is possible to have on the shelf both connectorized amplifiers and dedicated DPA as RFICs. DPA is currently the most popular method for linearization of the base-station amplifiers [75]. DPAs have been constructed in different transistor technologies, such as Si LDMOS, GaN HEMT, GaAs PHEMT, GaAs HBT or GaN. Besides, some designs of DPAs with transmit power ranging from a few watts to 250-500 W have been presented [79]. Measured efficiencies range from 35% to 80% at medium-high power levels, depending on the applications and the particular structure of the DPA. Considering the PkA is biased lower than the main amplifier, the current of the PkA at the maximum input drive cannot reach, in practice, the maximum allowable current level. Thus, the modulated load is not optimal and less power than expected is produced. On the other hand, the memory effects difficult to high linearity achievement in wideband applications. Based on different issues on DPAs we investigate a brief overview of DPAs as follows:

-More important applications used by DPAs and exploited device technologies for implementation of DPAs

- Applied solutions to improve the efficiency and linearity of DPA for 6dB and higher back-off.

- Enhancing bandwidth techniques of DPAs

2.2 Technologies and applications related to DPAs

According to Fig 2.1, the physical layer for the down and up-link of mobile and wireless services is spread on several frequency bands, but all of them are limited to lower than 6

GHz. As shown in Fig 2.1, the GSM bands occupied below 2 GHz nevertheless the trend has been to engage also higher frequencies after the third generation of mobile networks. Despite broadening UMTS in 2.14 GHz band, the fourth mobile generation, i.e., LTE and WIMAX, is extended up near 6 GHz. Also, wireless Local Area Networks (LNAs) that determined by the Wi-Fi protocol, are used on the ISM 2.4 GHz band and on the upper frequencies such as 5.5 GHz band. According to power levels, mobile base stations cover power levels up to 100 watts, while the user terminals such as Wi-Fi is bounded around few watts.

There are some factors for limiting the usage of higher frequencies in radio access systems, among which visible connection exigency that would bound the mobility of users and the high cost of high-frequency devices. Regarding these factors, for example 60 GHz wireless LANs is developed for communicating in small spaces such as inside buildings. Moreover, an important presented system to connect the base stations to the core of the networks is backhaul [81]. This system demonstrates an implementation of mobile infrastructure which works from few GHz to mm-wave frequencies through microwave point to point radio links. Considering the future progress, applications of mm-wave carrier for fifth generation mobile networks will relate to bandwidth requirements and spectrum resources access.

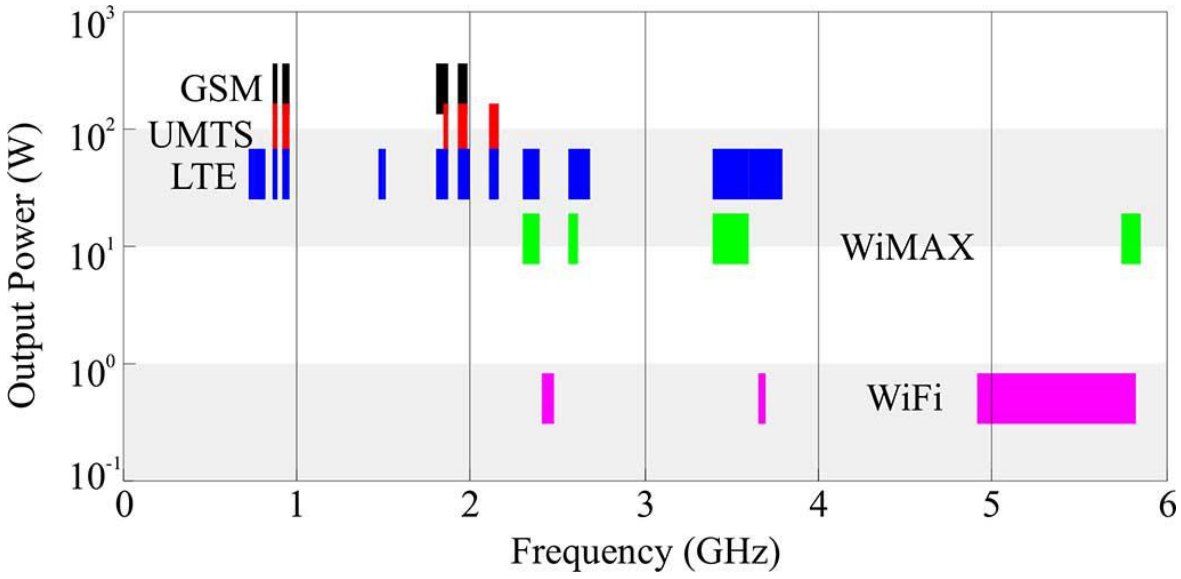


Figure 2.1 Output power levels besides the used frequency band of wireless services [82]

Choosing the semiconductor technology for designing power amplifiers is related to its operation frequency and power level. However, other factors among cost, power, efficiency

and linearity can be important to select the useful technology.

LDMOS and GaN HEMT devices utilize based on their characteristics among high breakdown voltage and power density for base-stations. Commonly, the LDMOS presents a proper behavior of linearity besides a low-cost. The GaN HEMT is used due to high efficiency, especially on SiC substrate with a more expensive cost. In above mentioned technologies, the bias voltage is the same (availability of 28, 40, 50 V drain bias). As well as, a higher operation of frequency and wider bandwidth [83] besides reducing the capacitive effects can be obtained base onto the intrinsic characteristics of GaN HEMT. For handset applications, the HBT devices are opted with drain voltage below 4.5V and about 1 W level PAs, because of its reliable besides low-cost technology process. DPAs based on CMOS technologies are also investigated because of their capability in co-integration and their flexibility. However, due to some drawbacks of CMOS among low break down and low power density, HBT DPAs have a respectful performance compared with CMOS DPAs.

Finally, GaAs pHEMTs are more useful for developing medium-/high-power, mm-wave PAs at frequencies higher than 20 GHz as well as GaN transistors are used. In view of DPA design, the place of GaN is more respectable in GaAs due to impedance levels, applying for broadband matching networks besides reducing losses. In addition, the higher power density, helped reduce the complex combiners and implementing the advance technologies such as DPA [84].

In the applications section of DPAs, there are many useful works that are implemented by industry companies such as NXP and Freescale. For instance, some of these applications will be presented as below.

One of these applications is optimized for use in 1.5 GHz 3GPP E-UTRA LTE base stations applications by using two BLF6G15L-250PBRN LDMOS power transistors in a Doherty architecture. The results of fractional bandwidth and efficiency on average of power are 1476 MHz to 1511 MHz and 36% respectively. In Fig 2.2 is shown the Photograph of this DPA. For more details it can be referred to the reference [85].

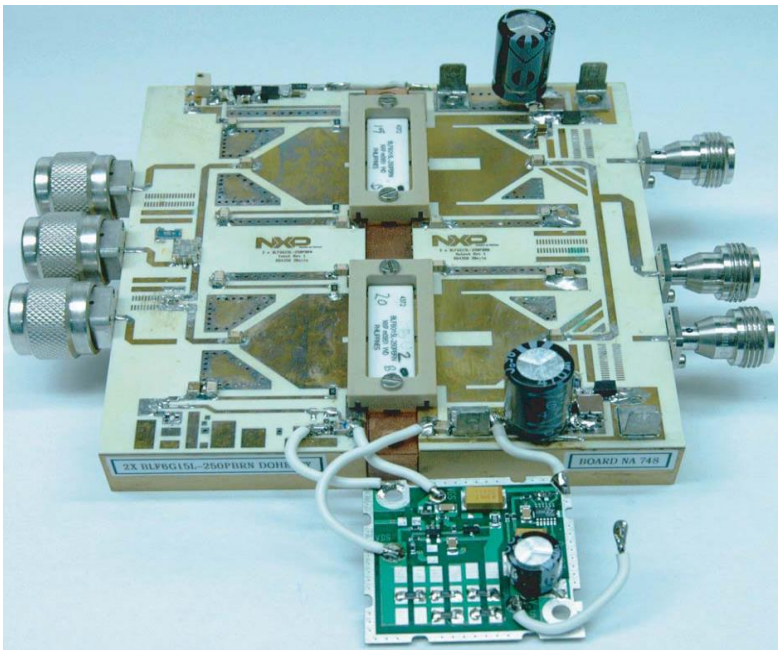


Figure 2.2 Photograph of the BLF6G15L-250PBRN Doherty power amplifier [85]

Another application of DPA is related to NXP industry, it announced as an ultra-wideband Doherty reference design using the BLF884P and BLF884PS power amplifiers (see Fig 2.3). Its frequency band is operated from 470 to 806 MHz. The average DVB-T power level of 70 W is presented by this application [86].

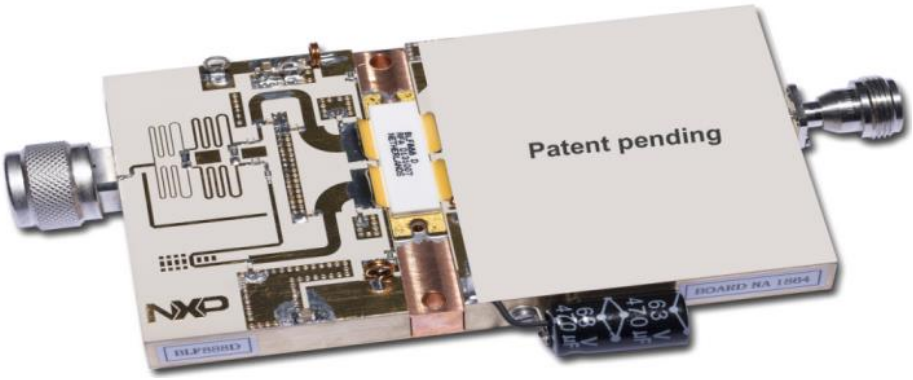


Figure 2.3 Ultra-Wideband Doherty Amplifier announced in [86]

A 2-way Doherty amplifier using two BLF888A UHF LDMOS transistors (in NXP technology) is presented in [87] (see Fig 2.4). The amplifier has minimum output power of 200 W average (DBV-T) and approximately 50 MHz of bandwidth (depending on the center frequency).

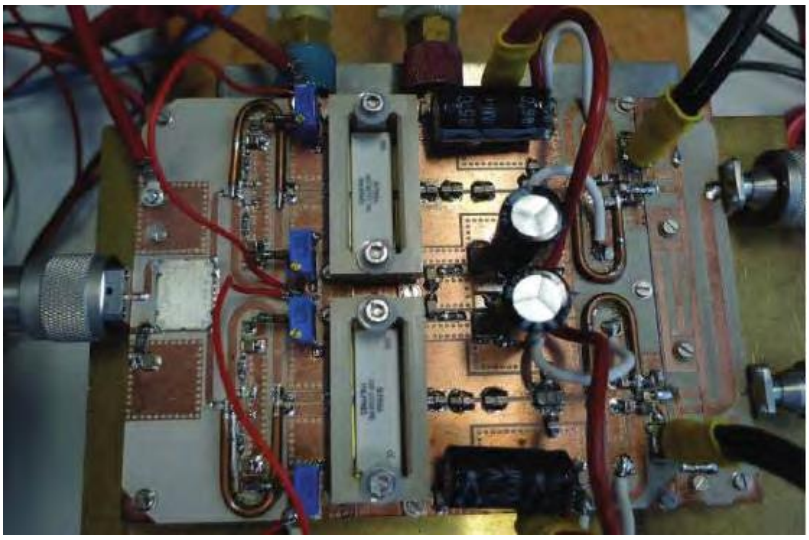


Figure 2.4 Doherty amplifier designed for 710 MHz [87]

At last, an advanced Doherty alignment module is designed specifically to optimize the performance of Doherty amplifiers using an innovative class of highly integrated GaAs MMIC control circuits by Freescale technology [88]. Its frequency bands are spanning from 700 MHz to 2700 MHz (see Fig 2.5).

Figure 2.5 Cellular power amplifier reference design in [88]

2.3 Trends on increasing efficiency and linearity of DPAs

Commonly, implementing the DPA is face to limitations on linearity and proper efficiency. These issues can be related to the intrinsic DPA and non-desirable characteristics of

devices. To solve these limitations on linearity, digital pre-distortion practically applies. Since pre-distorters need to reduce their complexity besides enhancing the overall system operation, some other works used memory effect techniques, which is effective in nullifying amplitude and phase distortion. For instance, in [78] and [89] compensating distortion high power levels besides optimizing bias and dimension of devices are presented. Moreover, there is a research on the relationship between load modulation and phase distortion in DPAs based on various trends. The importance of efficiency enhancement in DPAs is directly related to power consuming reduction.

Table 2.1 demonstrates some works relating to the applied technology, frequency range, output power, OBO amount and OBO efficiency of DPAs in recent years. The design approaches are detailed as follows.

Table 2.1 Performance comparison between DPAs in different works [82]

Ref	**Freq(GHz)**	**Tech**	**Psat (dBm)**	**OBO(dB)**	**Eff (%)**
[20]	2.14	Si LDMOS	50.5	10.5	35
[21]	1.85	GaAs HBT	30	6,10	37,31
[22]	2.6	GaN HEMT	41.9	7,12,17	62
[23]	2.655	GaN HEMT	51.7	8.1	60.5
[17]	2.14	Si LDMOS	53	6	50
[24]	0.87	Mixed	51	6,8,10	61,56,51
[25]	10	GaN HEMT	49.8	7.8	49
[26]	10	GaAs pHEMT	29	6	43
[27]	2.01	Si LDMOS	42.5	6	33
[28]	2.14	GaAs pHEMT	31.6	6	53
[29]	3.5	GaN HEMT	49.5	6	46
[30]	1.8	GaN HEMT	31	7	31
[31]	2.1	GaN HEMT	42	6	48
[32]	1.88	GaAs HBT	33.5	6	44

2.3.1 Enlarging output back-off (OBO)

Regarding the limitation of OBO range at 6 dB for conventional DPAs and request to enlarging the high efficiency range in most of the modern communication systems with high PAPR, some viable solutions are presented that called Multi-way and multi-stage DPAs.

In N-way DPA the PkA is made by combining the output power of N-1 power amplifiers (see Fig 2.6a), thus allowing increased linearity (larger OBO), while in N-stage DPA the PkA is made with multiple Doherty structures working in a parallel configuration (see Fig 2.6b).

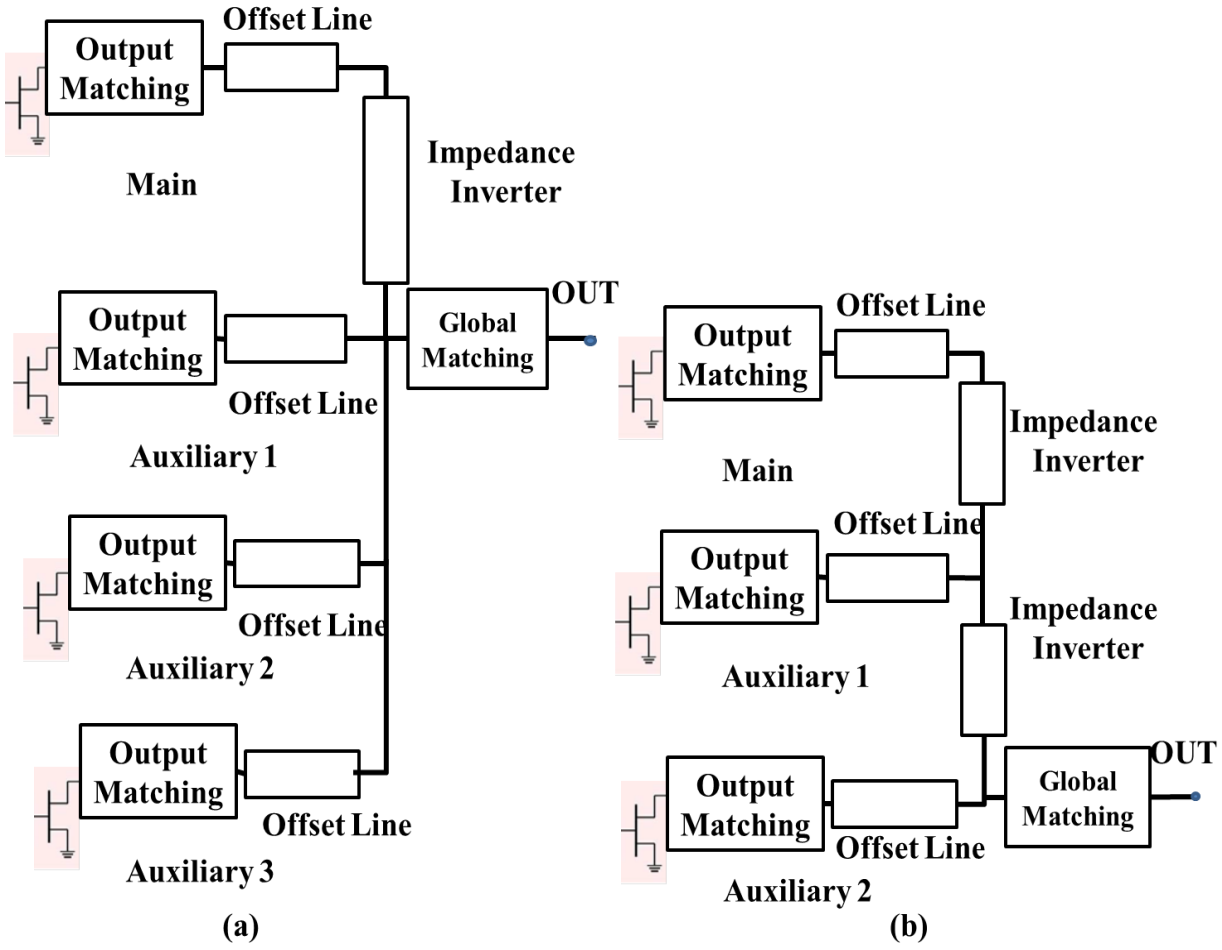


Figure 2.6 Multiway asymmetrical DPA (a), and multi-stage DPA (b) [82]

As it can be seen in Fig 2.7, the increment of N besides a proper optimization on power splitting and bias can due to increasing the first efficiency peak beyond 6 dB. It is usual in

the 3-stage DPA, where the first PkA modulates the load of the CA, and the second PkA modulates the load of the previous Doherty PkA [75].

[90] Presented a WCDMA DPA, where applying three separated inputs in the main besides the two peakings. The work of [91] is proposed the gate bias adaptation technique to improve the linearity of DPA.

The implementation of 3-stages inverted DPA in LDMOS technology for 2.14 GHz center frequency is reported in [92]; where fabricated DPA are using different sizes for main and peaking stages, due to reclaim OBO efficiency. The maximum output power delivering of proposed DPA is 50.5dBm besides 35% drain efficiency with 9.5 dB gain at 10.5dB OBO by using a WCDMA signal. The work of [93] is focused on a DPA using InGaP/GaAs HBT technology (at 1.85 GHz) in two different modes: in high-power mode, applying a DPA but in low power mode the performance of the mentioned hardware as a switched load to improve the efficiency at 10 dB back-off. Another DPA is also demonstrated based on multi-mode technique [94]. The fabricated DPA is employed the reconfigurable matching networks based on micro electro-mechanical switch (MEMS) and adjusting the bias networks of the peaking stage in order to reach the best efficiency OBO. The applied technology in this DPA is GaN HEMT, where its output power saturation is 41.9 dBm and depends on the opted configuration in average power levels of 35, 30 and 25 dBm; the PAE demonstrates a value higher than 62%.

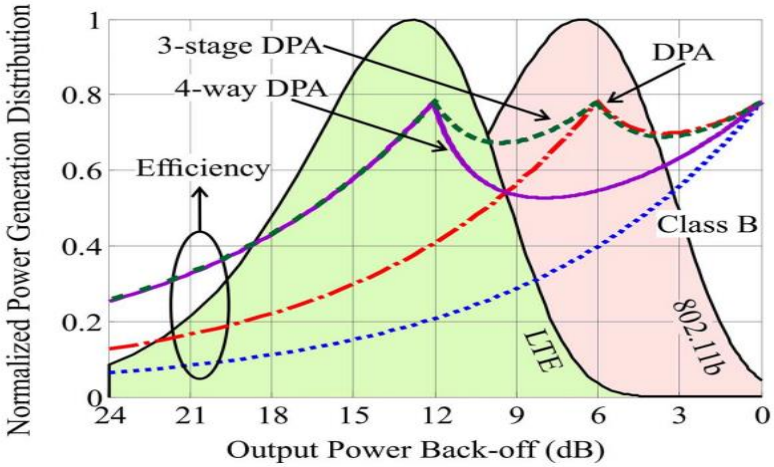


Figure 2.7 Normalized efficiency of class B and Doherty PAs (standard, 4-way and 3-stage) versus normalized output power over-imposed to examples of normalized power distributions of modulated signals for wireless applications [82]

In designed DPA of [92] a new output combiner is utilized in order to facilitate matching in peaking stage. Aforementioned DPA has applied GaN HEMT devices at the working frequency of 2.665 GHz with delivering output power saturation about 51.7 dB. However, measured average efficiency and output power using WiMAX signals with 8.3 dB PAPR are higher than 60% and about 43.6 dBm respectively.

2.3.2 Uneven power driving and asymmetrical devices

By driving the CA and the PkA by asymmetrical power, (applying more power to the PkA, typically, 60-70% of the total input power) the load may be better modulated (by avoiding the overdriving of the CA). Amplifiers with the uneven power drive show more linear and efficient operation. Another way is using the asymmetrical devices solution. This solution is useful in monolithic implementations and is flexible in selecting the device size. In [93], the implemented DPA is applied PkA larger than CA that can be mentioned to its obtained profits as follows: well timing in, turn on the devices, modifying the load modulation, allowable affecting on nonlinear distortion cancelation and simple topology. As studied in an investigated structure in order to optimize the linearity and efficiency, two DPAs using LDMOS devices are implemented and measured for 2.14 GHz, with 4-carrier WCDMA signal. By comparing with a conventional DPA can be achieved around 1 dB, increasing in output power versus the measured value (53dBm) (modified linearity) and in other optimized DPA has a better efficiency (5% improving in efficiency).

The work of [94] is based on a DPA with a LDMOS in CA and a GaN in PkA. This implementation is also utilized the uneven voltage biasing besides the maximization of device power factor [76]. By a proper tuned bias, the first efficiency peak can be occurred at 6, 8 and 10 dB of OBO.

2.3.3 Optimizing output combiner

In [95] and [96], a modification of Doherty load modulation is adopted using the variety of knee voltage for different currents in order to the on-resistance of the device. As shown in Fig 2.8, these structures are applied an OBO main load larger than 2 R_{opt} due to modify the efficiency at back-off .The proposed DPA in [95] is implemented using GaN CREE

transistors with around 50 dBm output power. While, the used technology in [96] is GaAs MMIC. It is exploited at X-band with achieving 29 dBm in output power.

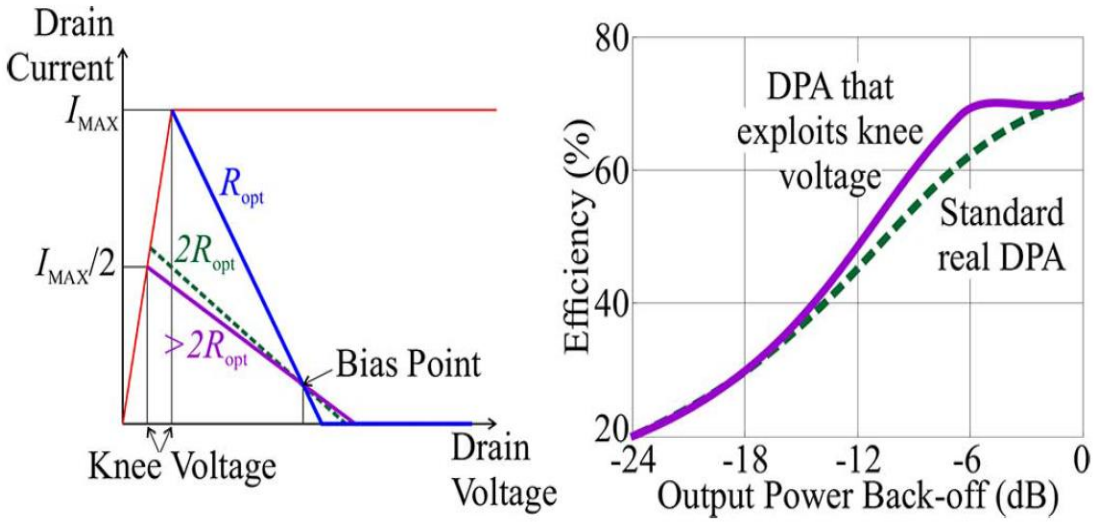


Figure 2.8 Larger back-off impedance for efficiency maximization [95], [96]. Dynamic load lines of the main device at saturation and back-off (left). Typical efficiency improvement (right).

The structure of [97] indicates a replacing the impedance inverter of conventional DPA to a coupled-line loaded with a capacitor. Using this structure with proper tuning can be suspending the harmonic besides reduction of intermodulation distortion by 23 dB. The designed hardware is fabricated by LDMOS devices at 2.01 GHz yields 42.5 dBm of output power at saturation point and 33% drain efficiency at 6 dB OBO. Another design is presented in [98] by adjusting the impedance inverter and global matching network due to the correction of the unbalanced current among the main and peaking stages. According to the use this structure with a developed prototype on GaAs pHEMT at 2.14 GHz, a 13% increment in back-off efficiency and 31.6 dBm of output power is obtained.

In [99], several mentioned techniques are combined to enlarge the back-off efficiency. The structure of this work utilizes stepped impedance network to improve the efficiency at 6 dB back-off are achieved under applying large instantaneous bandwidth signal (100 MHz LTE).

2.3.4 Other techniques

The proposed works in [100] and [101] indicate a different variety of DPA structure considering the DPA load. Designed DPA in [104] has used the structure of [102], [103] in order

to have a proper impedance transformation. However, by reducing the phase and gain deviations among the main and peaking stages through useful bias tuning, is derived to reduce the distortion. This DPA is employed in GaN HEMT technology at 1.8 GHz with reported results, 31 dBm maximum power output with 31% PAE at 7 dB back-off.

The solution of [101] is applied a replacing between a branch line coupler and the output combiner of the conventional DPA. The results of this implementation are the same as a standard DPA, while the impedance level is far from the proper value, particularly for the high-power level. The designed DPA is developed at 2.1 GHz applying GaN HEMT devices with obtaining 42 dBm maximum output power and 48% drain efficiency at 6 dB OBO.

In [104], improving the non-linear behavior in HBT DPAs is investigated, where using class F harmonic closure the back-off efficiency is optimized. This design is achieved 33.5 dBm of output power at 1.88 GHz.

2.4 Broadband techniques

The demand for higher BW in DPA is evident in multicarrier applications. For a single carrier, the typical 5-10% of fractional BW is enough for new solutions, including Advanced LTE (40 MHz). However, in multicarrier power stations, this demand should be considered. The limiting factors of bandwidth in DPAs can be related to the DPA impedance inverter, the offset lines, the phase synchronization at the output common node, and applying harmonic terminations. In summary, a quarter-wave length transmission lines can be considered as an impedance inverter, which contains the intrinsic narrowband property.

In order to solve the problem of offset lines, which commonly employed for single frequency operation, embedding the offset line aboard the output matching network is suggested. This performance leads reduction of the overall quality-factor of the filter and a proper effective on bandwidth. In addition, by a relevant synchronization of main and peaking branches, an optimal load modulation over a large frequency band can be achieved.

A summarized report of comparison between proposed DPAs related to bandwidth enhancement is indicated in Table 2.2. In cited Table, the applied technology, center frequency, fractional bandwidth, output power at saturation level, OBO, and drain efficiency at maximum

output power are reported. More details on the structure of referenced DPAs are visible as following.

Table2.2 Bandwidth enhancing performance in recent proposed DPAs [82]

Ref.	Technology	Frequency (GHz)	BW (%)	P_{SAT} (dBm)	OBO (dB)	Efficiency (%)
[37]	InGaP/GaAs HBT	1.83	27	35	7.5	30
[38]	GaN HEMT	3.3	18	43	6	38
[39]	GaN HEMT	0.85	35	50	6	52
[36]	GaN HEMT	2.6	31	39.5	5, 6	40
[40]	GaN HEMT	0.85	30	43	9	49
[41]	GaN HEMT	0.776	21	49.3	6	43
[29]	GaN HEMT	0.98	41	40.2	6	30
[43]	GaN HEMT	2.2	22	42	6, 7	40
[44]	GaN HEMT	2	41	42	6	42
[45]	GaN HEMT	1.73	115	43.1	6	45

2.4.1 Optimizing the matching networks

According to the effect of the correct load modulation in DPA bandwidth, designers have focused on optimizing the output section of the DPA. This focus is due to have higher back-off efficiency over the large bandwidth. For instants, the cited technique is applied in [105], by merging the offset lines and impedance inverter blocks in a simple matching network block .The hardware works in the 1.6-2.1 GHz band by testing with a LTE signal with 7.5 dB PAPR and 10 MHz bandwidth, based on InGaP/GaAs HBT technology, and achieves average efficiency higher than 30% at the average power of 27.5 dBm.

In [106], by exploiting wideband compensator networks, the reactive effects of the devices are compensated. In addition, for obtaining flat power and efficiency, second harmonic tuning is applied at back-off for higher frequencies of the band. The implemented DPA is based on 10 W GaN HEMTs from CREE (see Fig 2.9), and exhibits the frequency band of 3-3.6 GHz. The measured result of maximum power output is 43 dBm besides 6 dB OBO efficiency larger than 38%. The work of [107] is reported a DPA include the quasi-lumped quarter-wave transmission line besides the Klopfenstein taper [108] in order to broaden the bandwidth of the conventional DPA. The work in [107] has the similarity with this thesis that both use the

Klopfenstein taper. The main difference is that in [107] the Klopfenstein taper is used just to broaden the impedance matches to the load, while in this thesis it is used instead of the usual quarter- wave transformer to spread the BW of the whole load-modulation sub-circuitry. In [107] the impedance matching networks of the output of both main and peaking devices are directly made by taking advantage of the device output capacitances, together with a modified transmission line (see Fig 2.10). This matching network is applied considering the existence of the device parasitic and package in real transistors. The delivery of maximum output power in [107] is reported about 50 dBm with 52% OBO efficiency over the band frequency of 0.7-1 GHz (about 35% fractional bandwidth). The designed DPA in [109] is focused on a simplified real frequency technique [110] in order to obtain the broadband matching networks besides the proper frequency-dependent optimum impedances. According to two prototypes fabricated using GaN HEMTs from CREE and measuring tests, one of these samples is obtained to broader bandwidth (2.2-3 GHz) with maximum output power of 39.5 dBm and 6 dB OBO power efficiency higher than 40% at over the band.

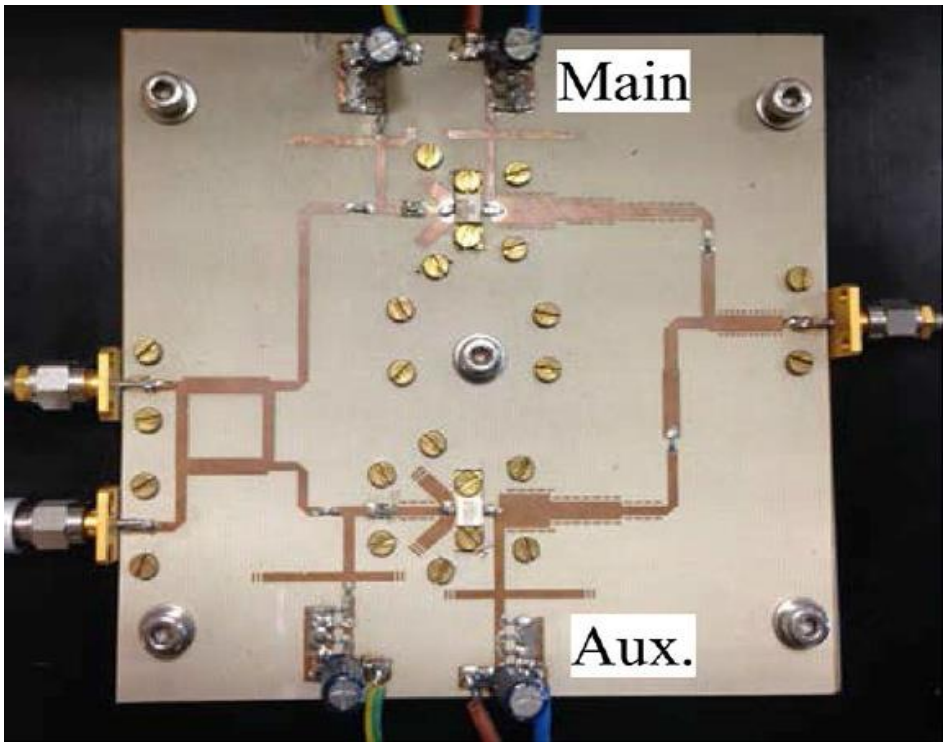


Figure 2.9 Fabricated DPA using a 20 W GaN-based 3–3.6 GHz [106]

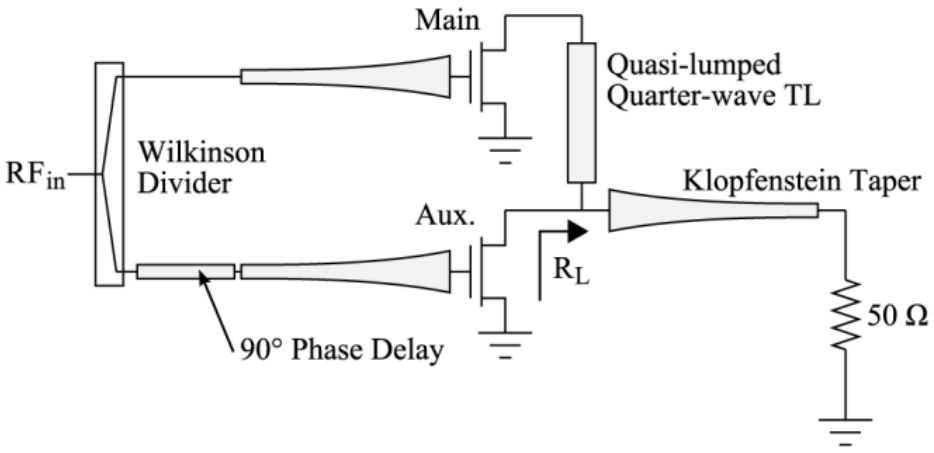


Figure 2.10 The scheme of the proposed DPA by using quasi-lumped quarter-wave transmission line in load modulation [107]

A three-way DPA is fabricated in [111] due to improve bandwidth and OBO by canceling/ absorbing the device output capacitances. The used devices in main and peaking stages of implemented DPA are a 10 W GaN HEMT from CREE and two 25 W GaN HEMT from CREE, respectively.

The presented DPA in [112] is focused to optimize the instantaneous bandwidth in order to handle 100 MHz LTE signals. To achieve this aim, by designing the drain bias networks, electrical memory effects are minimized besides applying ad-hoc LC resonators.

However, the enhancement of bandwidth is obtained using an integrated Doherty combiner (RDO750A03 from RN2 Technologies Co.) and broadband output matching networks based on a simplified real-frequency technique. The fabricated prototype used 60 W GaN HEMT devices from CREE. The measurement results reported a significant enhancement in ACLR (4 dB) and ACLR asymmetry (3 dB) against to the same DPA applying standard bias networks. Another different solution is presented in [113], as a kind of Doherty by removing the impedance inverter in the work of [113]. However, the results of fabricated DPA are sufficient. The prototype of cited DPA is realized Based on 10W GaN HEMTs from CREE, with about 40% fractional bandwidth (0.8-1.2 GHz), the maximum output power higher than 40.2 dBm besides 6dB OBO efficiency higher than 30%. The work of [114] is focused on using ultra-wideband

output combiner that consists of a mixed group of quarter- wavelength transmitters and capacitors. Due to used method and optimizing the quarter- wave lengths, an 83% fractional bandwidth is obtained. The designed DPA is realized based on GaN HEMT devices, and shows a maximum output power around 41 dBm with 6 dB OBO efficiency higher than 35% in 1.05 to 2.55 GHz band.

2.4.1. Digital DPA

As shown in Fig 2.11 the strategy of digital DPAs is driving main and peaking stages independently from baseband. In this case, using the separated baseband processing to redefine the transmitter besides applying proper digital signal conditioning for two branches can be with the pros and cons that is comparable with conventional DPAs. For instance, in [115] is shown a 2.8 factor increasing in bandwidth with respect to conventional DPA. In fabricated DPA in [115] are used 10 W GaN CREE transistors, and depicted output power larger than 42 dBm, with 6dB OBO efficiency, greater than 40% from 1.96 to 2.46 GHz band.

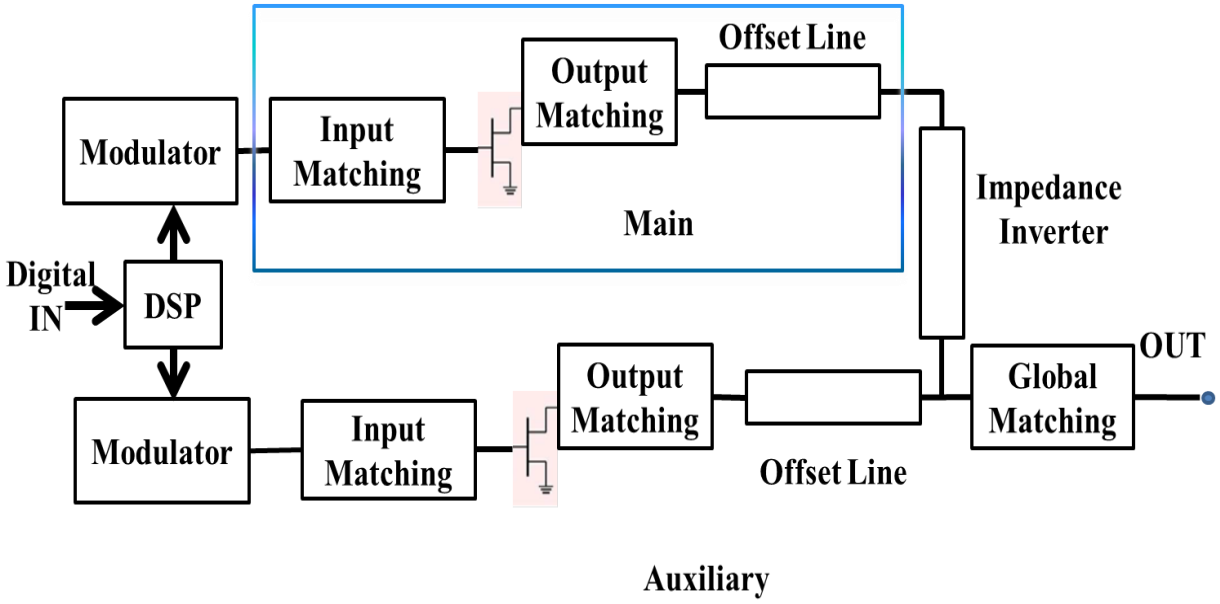


Figure 2.11 Typical schematic of digital DPAs [82]

The work of [116] is used a novel output combiner in order to modify the bandwidth features in the digital Doherty aspect. As well as, to reach a proper configuration at OBOs 6, 8, and 10 dB, are applied a desired biasing network on the main branch. To implement the

prototype, 15 W GaN CREE transistors are used. The measurement results are shown a maximum output power about 42 dBm, with 6 dB OBO efficiency, greater than 40% in over the band from 1.5 to 2.5 GHz.

In [117], a linear multi-harmonic analysis method is presented to evaluate on digitally controlled dual driven DPA operation. In this case, under ideal conditions, a design based on a Doherty- Outphasing continuum is demonstrated. However, in actual implementation using a combiner with non-ideal conditions have resulted in high efficiency over 100% fractional bandwidth DPA. The designed DPA is based on 15 W GaN CREE devices, and shows an output power greater than 43.1 dBm, with 6 dB OBO efficiency higher than 48% on the 1-3 GHz band.

2.5 Load modulation in DPAs

As mentioned above, in order to decrease the limitation of bandwidth in DPAs needs to a proper load modulation between two branches of DPA (main and peaking path) at low and high level of power. Obviously this concept presents the two different types based on recently published works:

1- Impedance inverter

Impedance inverter is a kind of load modulation approach already introduced in section 1.4.1 for a DPA. In some papers, the classical quarter-wave transmission line is replaced by other impedance inverter alternatives; some of them use smaller transmission lines with symmetrical impedances on both sides ([118] and [119]). Other alternatives are based on quasi-lumped quarter-wave transmission lines, as above-mentioned [107].

2- Impedance transformer

Another type of applied load modulation in DPAs is related to impedance transformer, as indicated in [113] and [120]. According to this concept, both references show that the elimination of the quarter-wave transmission line as a load modulation element is a solution in order to reach a broadband DPA.

This concept that uses broadband matching networks in both output paths of DPA and without the need of an impedance inverter will operate on the proper adjustment of the output reactance in the main and peaking PAs. For instance, in [113] it is optimized the return loss at all input power levels, both output matching networks (OMNs) are matched to 70 Ω instead of the usual 100 Ω and 50 Ω at the output of the main and peaking branches in conventional DPAs respectively (see Fig 2.12).

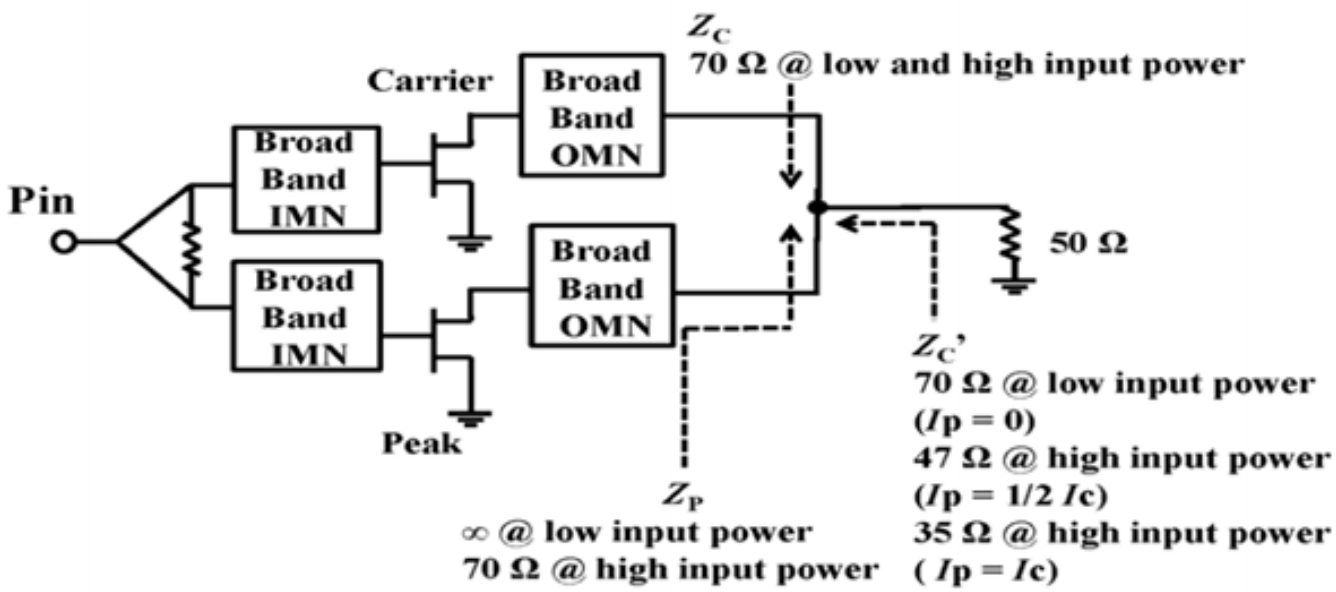


Figure 2.12 The scheme of the proposed DPA by using the impedance transformer type in load modulation [113]

Furthermore, the implemented DPA in [120] has a structure that implements the impedance transformer in a way more optimized than in [113] (see Fig 2.13). In [120], a proper impedance transformation at the output of the transistor is obtained by using lumped elements based on pi(Π) and T networks. Besides, considering the output powers and bias conditions (the bias voltages are different in the two branches), different kind of transistors are used in both branches (main and peaking). Additionally, to usage of the impedance transformer produces a proper phase delay at the output of the two branches. This means that the bandwidth improvement is occurred in implemented DPA in [120], taking advantage of the OMN to also compensate delay mismatching between branches.

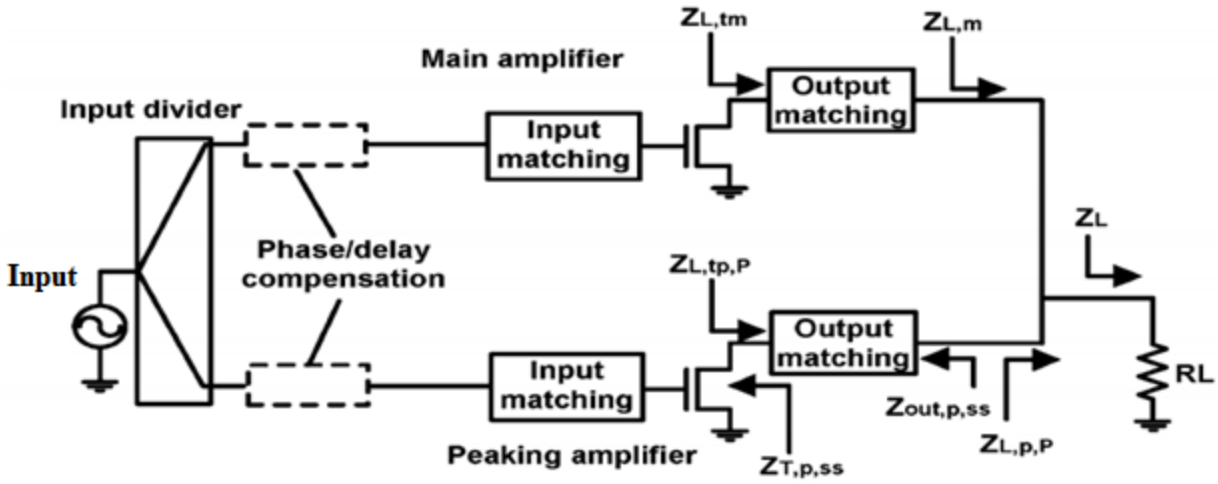


Figure 2.13 The scheme of the proposed DPA by using the impedance transformer type in load modulation [120]

In this thesis, underpinned by recent works proposing the use of the above-mentioned impedance transformer method, it is aimed to reach a better bandwidth by spreading the bandwidth of the impedance transformation while adjusting delays by controlling the reactance of the OMNs. In the next chapter, the steps of the work and its implementation will be presented.

Chapter 3

Design of DPAs

3 Design of DPAs

As stated before, multi-band communication schemes have enlarged the BW needs. Along the literature, there are two main approaches regarding the BW improvement of the PA: to employ resonant narrowband structures split along the whole application band or the employment of a wideband PA [82]. Hence, for such multi-band applications, the limited BW of the DPAs has become a drawback. The investigations guided to increase the DPA BW may be roughly classified into two main lines: reduction of the frequency constraint of the quarter-wave line inverter [105] and solving imperfections in the OMN [82], i.e., modifying their reflection coefficients.

Some works pursuing the BW enhancement use either a design strategy based on lowering the quality-factor (Q) of the quarter-wave transformer or on the use of low Q matching circuits (to compensate the bandwidth constrain imposed by the output capacitances of the active devices) [105], [6] and [109]. Low Q designs offer good broadband performance with decreased sensitivity to load variation, at the price of poorer harmonic suppression. By mismatching the impedance of the transmission line (λ/4), relative bandwidths ranging 40 - 60 % have been reported with PAE values of 30 % (40% in drain efficiency) [6], [109]. Even by modifying the impedance of the transmission line, PAE values in the range 50-60% have been achieved, although sacrificing the relative bandwidth (to 15 % in [121]). In [122] a 35% of fractional bandwidth is reached by compensating the phase difference between the two PA paths and using a wideband uneven Wilkinson divider in the input of the DPA. The output combiner network was designed using conventional λ/4 lines.

According to the above approaches, in this chapter, two DPAs with 3 stages wideband even Wilkinson divider are assessed in the frequency range of 1.6 to 3.3GHz. The main contribution is to employ a coordinated network that a tapered line is applied in the output matching network of the main branch. Moreover, this study investigates a pure comparison of the proposed DPA scheme with a conventional one. Eventually, a DPA included 1-stage asymmetrical Wilkinson divider is evaluated.

3.1 Main aspects in the design of DPAs

This section provides the key factors in order to implement the DPA and carry out the respective simulations which can be categorized as

- Load-pull and source-pull
- Bias network
- Stability

Where the impact of these factors will be justified later on.

3.1.1 Load-pull and source-pull

In low signal designs, where the non-linear effects are not too remarkable, the impedance matching is quite straightforward from the direct use of linear tools, such as the Smith chart. Even in the basic microwave literature, it is explained the matching network design according to different objectives such as the gain, the noise, etc.

However, in the case of PAs, they are intrinsically nonlinear, and especially at high power levels the active devices evidence that nonlinearity. Then in order to specify the optimum impedances in the load and source of the device, it is used an empirical technique that depends on the design objective (i.e. gain, efficiency, noise, etc.). This technique is known as impedance pulling, so that it is referred to load-pull and source-pull at the device output and input, respectively.

In this context, it sweeps the fundamental and harmonic impedances of input and output at the package reference randomly in several times; this then tends to the proper gain, efficiency, and output power since a specific input level, frequency and bias condition are considered. Figure 3.1 depicts a simplified load pull setup.

Simulations based on load Pull and source-pull need large signal models of the active device. These models may be often obtained from empirical models given by the device manufacturer, but other times it is necessary to extract a simulation input-output model. A first way to have such models is the use of the large signal S-parameters (LSSP). LSSP are a set of S-parameters obtained not only at the fundamental frequency, but also at the significate harmonics, in a number that depends on the distortion level produced by the non-linearity. They are used in

simulations in a similar way to those parameters that have been used in Harmonic Balance.

A recent alternative to model the device at large signal levels are the X-parameters, which are a mathematical enlargement of S-parameters in large-signal or even nonlinear conditions [123]. As a difference with LSSP, X parameters are applicable to both large-signal and small-signal conditions, for both linear and nonlinear components. The incident and reflected waves to compute the X-parameters include harmonic component, and they are computed with equations including the device memory (Volterra series).

When the designer has not experimental parameters, from the manufacturer, to model the nonlinear device the employment of X-parameters or LSSP jointly in the load/source-pull studies would be more recommendable than the use of basic S-parameters models.

As an example, Figure 3.2 depicts the fundamental load-pull simulation of a 10 W GaN device at 2 GHz where the optimum impedance for peak power added efficiency (PAE) is located at the center of the contours. In this context, each contour is decreased in efficiency based on obtained variation of impedances. This procedure is also visible in the Figure for output power contours (see Fig 3.2).

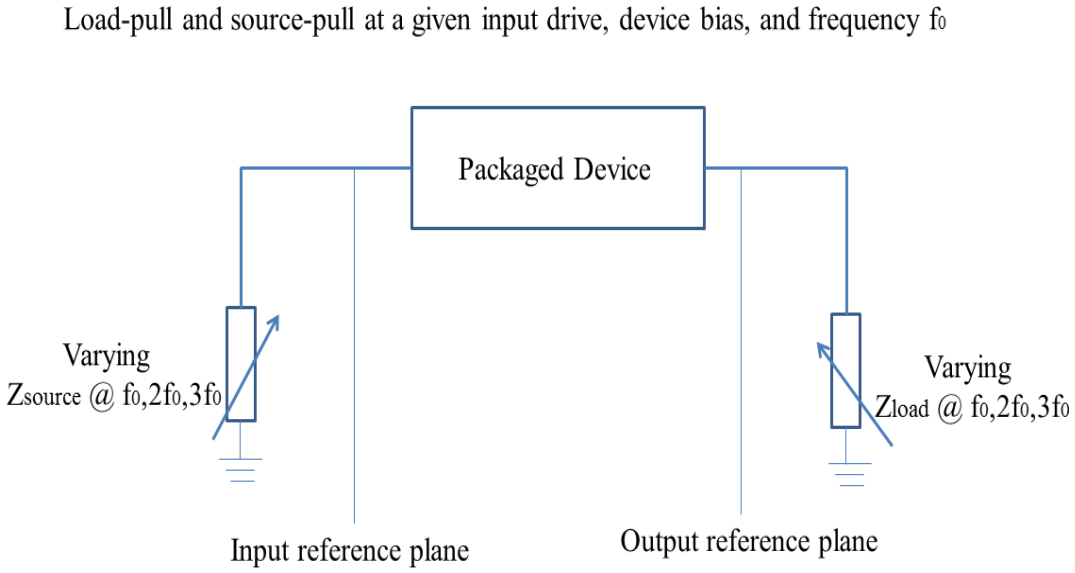


Figure 3.1 A simplified load and source pull setup

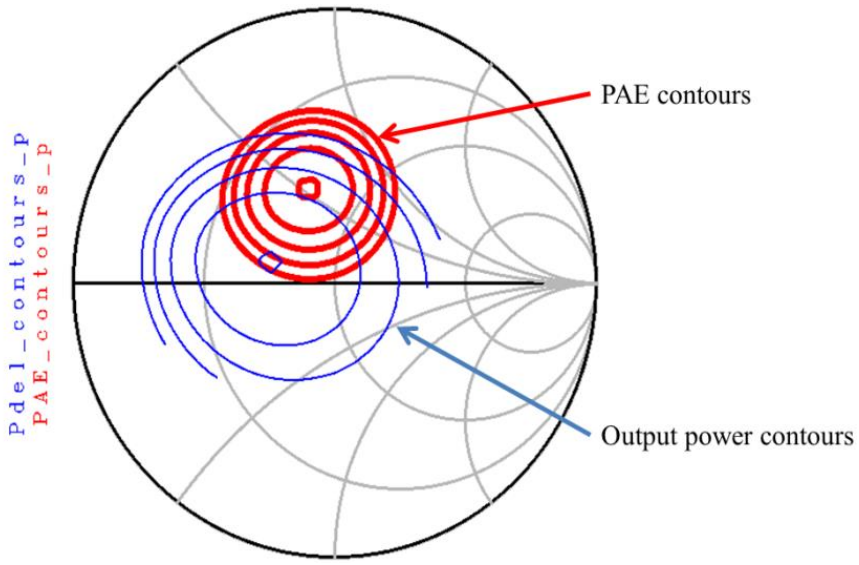


Figure 3.2 The simulated fundamental load-pull contours of a 10 W GaN device at 2 GHz

3.1.2 Bias network

Bias network is used for transmitting desired voltage and current of supply voltage to the amplifier. It is too important to get the suitable biasing network in order to avoid a spoiling of the RF energy while biasing the device.

This network may include: i) The multiple decoupling capacitors in order to minimize the supply ripple ii) An RF choke (i.e. An inductor, a short circuited quarter-wave transmission line) which is applied in the bias network to isolate RF signals from the device to the DC supply. Considering the RF chokes, the connected matching network to bias network experiences a high impedance at the fundamental frequency.

3.1.3 Stability

The device stability is analyzed for preventing low frequency oscillations in the RF amplifiers [76]. Basically, in practical designs the conventional ROLLER (K-|Δ|) test and stability circles would be emphasized to a desired method in order to evaluate the device stability when the large signal S-parameters (LSSP) are applied.

In this context, the requirement of unconditional stability in K-|Δ| test is defined by:

$$K = \{1- |S_{11}|^2- |S_{22}|^2 + |S_{11}*S_{22}- S_{12}*S_{21}|^2\}/ \{2*|S_{12}*S_{21}|\} >1, \ |\Delta| = |S_{11}*S_{22} - S_{12}*S_{21}| <1.$$

Remarkably, the large signal S-parameter of an active device depends on the frequency and drive level. In this way, the values of K and $|\Delta|$ are calculated through low frequencies up to the design frequency at different drive levels.

The instability problem in RF power devices exists, especially at low frequencies [76]. Therefore, in order to make the amplifier unconditionally stable at low frequencies, a common solution is to add a resistance (ballasting resistor) at the gate of the device. In principle, this stabilization resistor is just added at the device gate in order to increase stability without other relevant effects on the RF performance.

3.2 Beginning of the work

This section aims to design a DPA based on aforementioned approaches: i) elimination of quarter-wave line inverter in order to enhance the PA BW, and ii) modification of OMN's reflection coefficients in order to improve the phase delay between both paths of DPA (main and peaking). The resulting PA is compared with a conventional DPA by using the advanced design system (ADS) software.

In this context, it is presented a wideband GaN DPA in the 2.6 GHz band where low Q matching circuits are applied. Moreover, the conventional quarter-wave transmission line is eliminated and the performance of the load modulation is obtained by combining a multi-section transformer and a tapered line, relying on its benefits in the BW increasing. In this way, the wideband GaN DPA is designed by using: a) a 3-stages symmetrical Wilkinson splitter, b) wideband multi-section input and output matching networks, c) delay line in peaking path and d) an added tapered line in the output matching network of the main path. The Figure 3.3 depicts the schematic of the proposed DPA with the mentioned components.

The DPA presented in this section is based on two 15W GaN HEMT (CGH35015F) transistors, used in both the main and the peaking amplifiers. The substrate is RO4003, which has a dielectric constant of 3.55, a thickness of 0.8 mm and a dissipation factor of 0.0021 at 2.6 GHz. The bias points of the main and peaking amplifiers are determined by using the DC load line simulation in the ADS. In this case, the main amplifier based on class AB condition,

operates on a bias point of V_{GSm}= -2V and V_{DSm}= 28V (I_{DSm} = 250 mA), as well as, the peaking amplifier is biased at V_{GSp}= -3.2V, in class C.

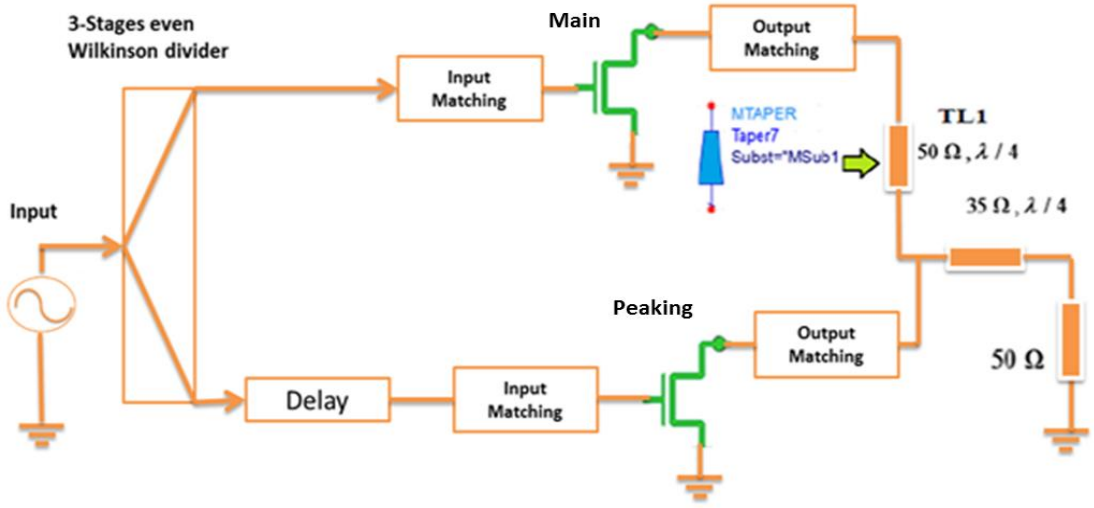


Figure 3.3 The first proposed DPA by using a tapered line as impedance inverter

Optimum impedances of the gate and drain in both PAs (main and peaking) are determined by using the load-pull and source-pull technique based on maximum delivered power as introduced before. According to this technique, the input and output impedances that have to be seen from the main PA are 3.6-j8 Ω and 25.6+j6.5 Ω respectively. Furthermore, 2.5-j8 Ω and 32.7+j26.6 Ω are related to the impedances seen by input and output of the peaking amplifier respectively. The mentioned impedances are matched to 50 Ω in the input stages of both amplifiers by using multi-section transformers. Besides this kind of matching network is used in the output stages of the peaking amplifier in order to match the transistor into the 50 Ω while, the output matching network of the main stage is matched to 25 Ω by using a mixed matching network in two separated sections. First by using a multi-section transformer is transferred to 100 Ω based on the fundamental DPAs section. Second via a tapered line 100 Ω is matched to 25 Ω in order to have a desired phase delay between both paths in designed DPA.

As stated above, a 3- stages even Wilkinson divider (see Figure 3.4) is applied in order to improve the BW of the DPAs. Based on the performance of even Wilkinson dividers, the input signal is divided into two 50 Ω branches that are connected to the main and peaking stages, as shown in Figure 3.4.

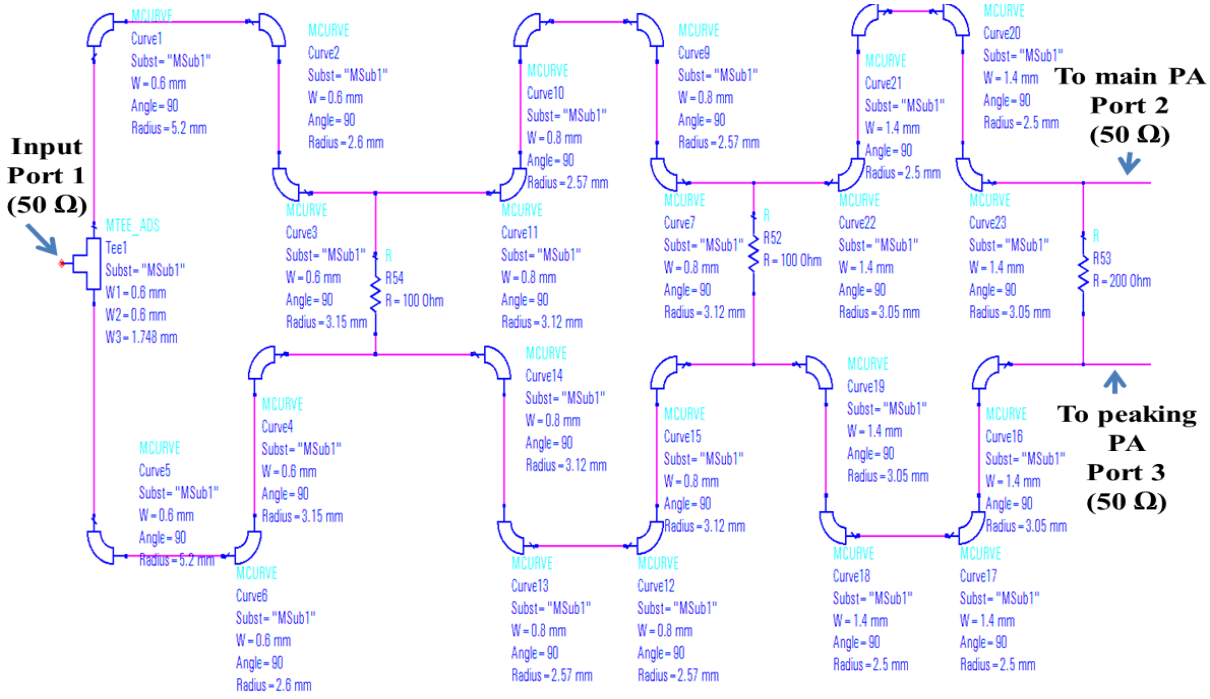


Figure 3.4 The used 3-stages even Wilkinson divider in designed DPAs (with tapered line (W-T) and without tapered line (WO-T))

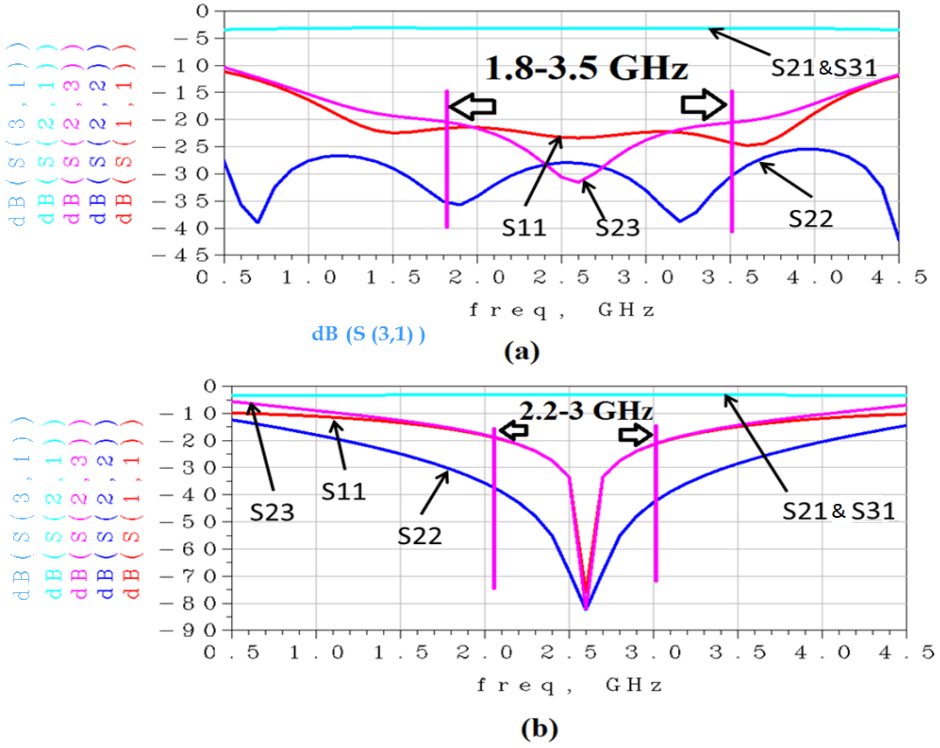


Figure 3.5 The performance of 3-stages even Wilkinson divider (a) and 1-stage even Wilkinson divider (b)

To verify the advantages of a 3-stages even Wilkinson divider over a 1-stage one, the S-parameters of 3 ports connected to the designed 3-stages even Wilkinson divider (see Figure 3.5a) besides 1-stage even Wilkinson divider (see Figure 3.5b) have been simulated. From Figs 3.5a and 3.5b, it can be seen a proper behavior in designed Wilkinson against that a conventional Wilkinson divider. The 3-stage Wilkinson divider shows an improved bandwidth at the expense of reducing the magnitude of some S-parameters. However, this reduction still keeps the resulting magnitudes into acceptable ranges, so we can take advantage of the BW improvement. Considering the isolation parameters between two output ports (see ports 2 and 3 in Figure 3.4) of two Wilkinson dividers (S_{23}) (lower than -20 dB) besides the flatness performance of S_{21} and S_{31} of two Wilkinson dividers as it is illustrated in Figs 3.5a and 3.5b, it can be resulted the BW of the 3- stages even Wilkinson divider about 1.1 GHz higher than the one in conventional 1-stage even Wilkinson divider. This could be introduced as a benefit for the 3- stages even Wilkinson divide. Even though, this divider (3-stages even Wilkinson divider) is good for the isolation splitter, when this divider will be applied to the DPA, because of the whole effects of different sub-systems in the DPA, this benefit is not an evidence.

Figure 3.6a and 3.6b illustrate the scattering parameters of W-T DPA and WO-T DPA in terms of the frequency range from 1 to 4 GHz, respectively. Considering to Figs 3.8a and 3.8b, the value of S_{21} points around 10 dB in the range of 1.6 to 3.3 GHz. Moreover, due to the S_{11} and S_{21} parameters, it is verified that the bandwidth of both configurations ranges from 1.6 GHz to 3.3GHz.

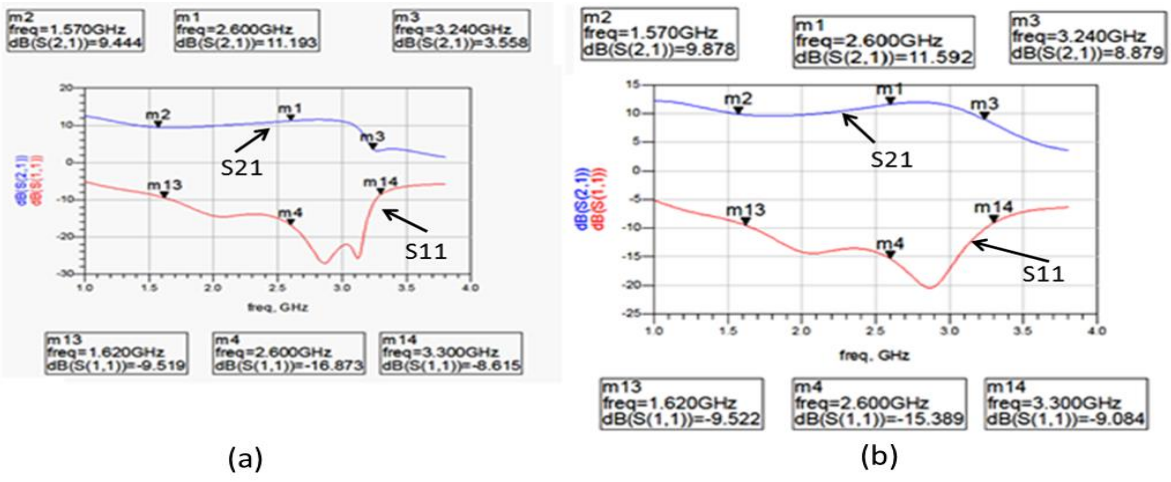


Figure 3.6 Scattering parameters of DPA: (a) without tapered line and (b) with tapered line at 2.6GHz

For more bandwidth validation, the S-parameters of both proposed DPAs (W-T DPA and WO-T DPA) has been simulated using the large-signal test in ADS as shown in Figure 3.7. The indicated simulations in Figure 3.7 are also applied in the frequency ranges between 500MHz to 4 GHz. These simulations show coherent results regarding the previous results obtained in Figure 3.6a and 3.6b.

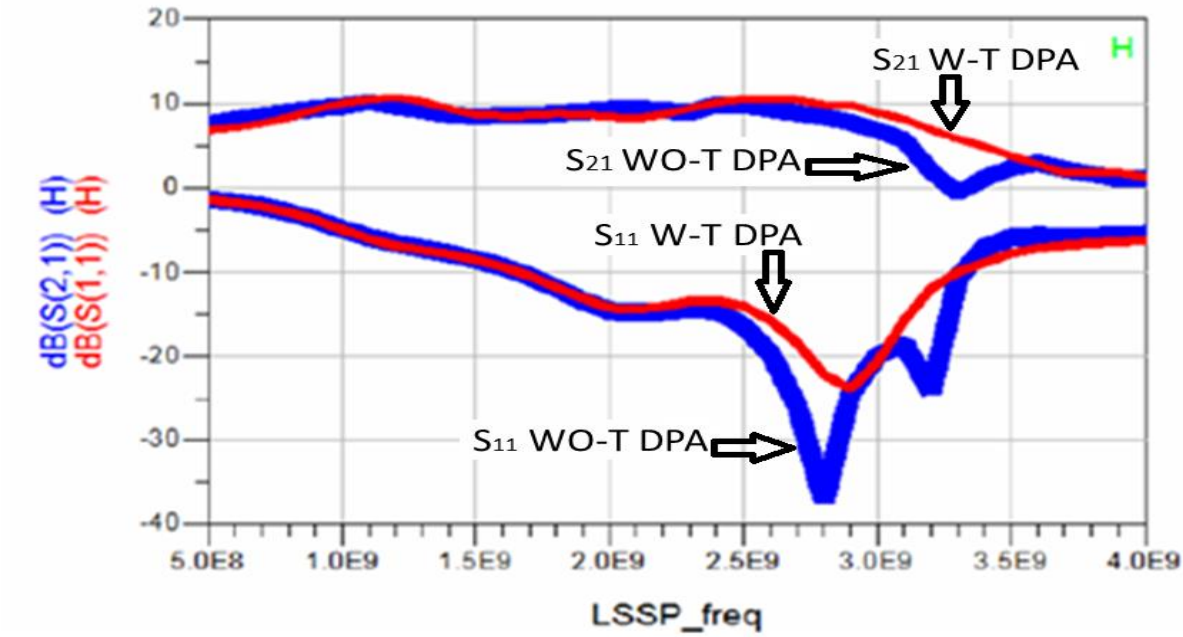


Figure 3.7 Large-signal S-parameters of DPA: in WO-T and in W-T at 35dBm output power

Considering the use of a combination of a tapered line with the broadband matching networks, it is expected to increase the bandwidth of the proposed DPA. But, as it is illustrated in Fig 3.7, both of DPAs (WO-T and W-T) have the same bandwidth. It may be caused to improperly adjust the phase delay between two branches (main and peaking amplifiers) in the W-T DPA.

The resulting PAE of both DPAs is shown in next Figures. According to the results, shown in Figure 3.8, which has been obtained at 2.6 GHz, the simulated PAE in WO-T DPA (red line) and W-T DPA (blue line) are 40.46% and 61.17%, respectively, for a 35 dBm single-tone power input. This means a relative PAE increase of 50% at the maximum output power. This increment depends on the proper connection between the two branches (main and peaking) into the load via the combination of broadband multi-section transmission line with a tapered line.

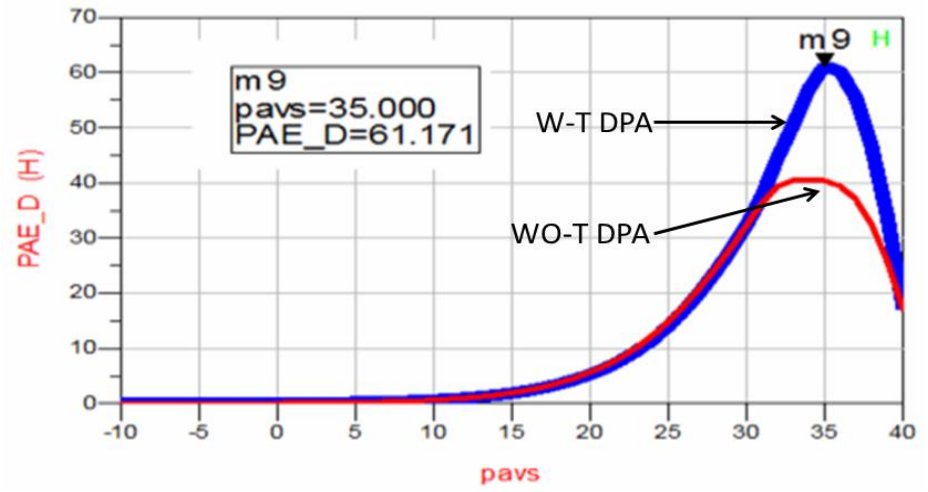


Figure 3.8 PAE in: WO-T DPA (red line) and W-T DPA (blue line), at 2.6GHz

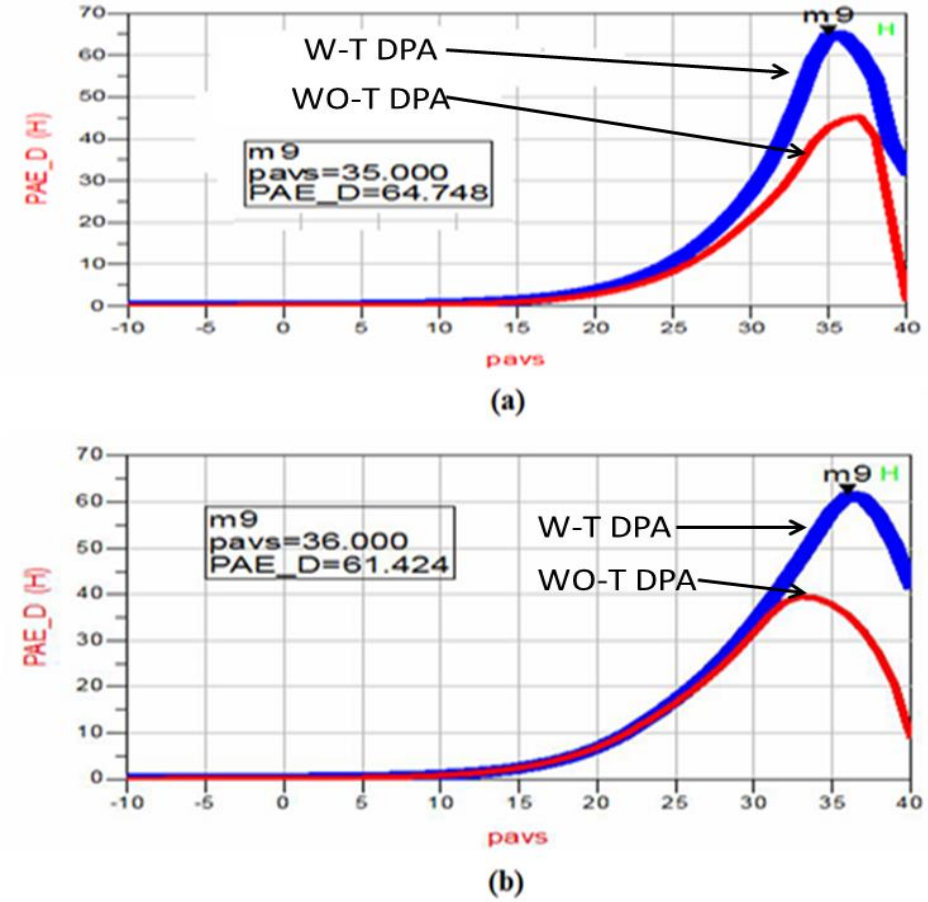


Figure 3.9 PAE in: (a) WO-T DPA (red line) at 1.6 GHz, (b) W-T DPA (blue line), at 3 GHz

Figure 3.8a and 3.9b display the value of PAE at 1.6 GHz and 3 GHz, respectively, for both of DPAs. It shows the amounts of PAE in both of the proposed DPAs are varied near a constant range of 61% to 65% and 41% to 45% across the whole frequency range for W-T and WO-T DPAs respectively.

The gain versus input power is characterized at center of frequency in order to assess the linearity of two DPAs. As demonstrated in Figure 3.10, the gain of the WO-T DPA is around 12 dB, practically the same than for the W-T DPA, which is slightly over 13 dB. Concerning the gain deviation of two DPAs at the higher input powers, it is clear the linearity of both DPAs is similar.

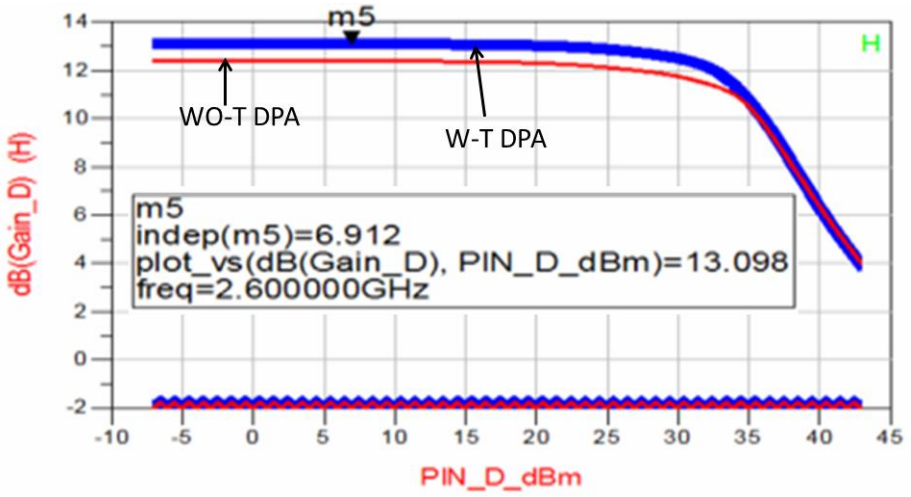


Figure 3.10 Gain versus input power in: WO-T (red line), W-T DPA (blue line)

The comparison of the resulted performance of the non-tapered line based DPA with the tapered line indicate a broad bandwidth (65% of fractional bandwidth), which is the same for both implementations. In terms of PAE, we have experienced an increment around 50% in the proposed W-T DPA. Additionally, the gain and output power have similar values in both amplifiers.

3.3 Design and fabricate a DPA with a tapered line

The previous study is underpinned on the simulations; the constructed PCB is just to evaluate divergences between them and the physical world.

3.3.1 Design rules

This section is focused on the design and construction of an advanced DPA based on the discussed approach. The matching networks in input and output stages of the two power amplifiers (main and peaking) are designed by multi-section transformer configurations based on ADS software. Furthermore, the biasing circuit of the proposed DPA is utilized a quarter-wave length transformer besides radial stubs in order to have a broadband response. As shown in Figure 3.11, RF bypass capacitors are applied to eliminate the ripple of the voltage from the power supply.

The main step of this section is improving the bandwidth in DPAs besides a trade off with sufficient power efficiency. According to this approach, a wideband GaN DPA in the 2.5 GHz band is designed and fabricated with a 1-stage asymmetric Wilkinson splitter. This kind of splitter is used in order to compensate the gain reduction in Doherty region, as illustrated in Figure 3.12. In doing so the impedance inverter in the output of the main path is removed and replaced by a combination of a wideband matching network and a tapered line. To be more precise, in this experiment λ/4 transmission line has been eliminated and a tapered line besides multi-sections transformers is used in the output matching network of the main stage (see Figure 3.12).

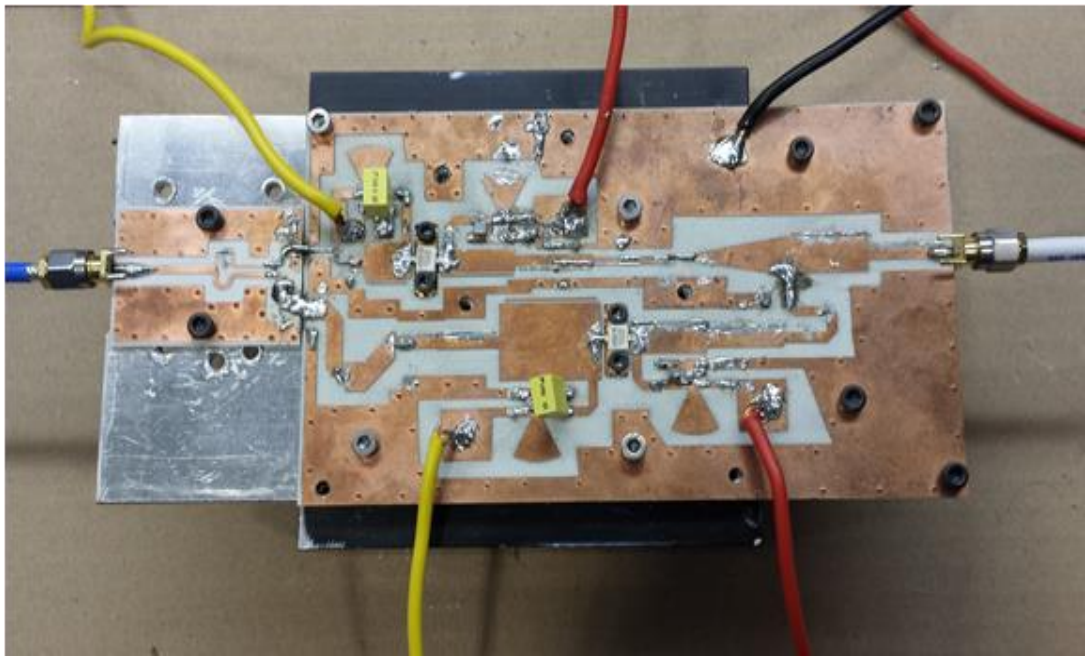


Figure 3.11 The PCB of proposed DPA with tapered line

The discussing DPA in this section is also based on two 15W GaN HEMT (CGH27015F) transistors, used on both the main and the peaking amplifiers. The substrate is RO4000, which all of its characteristics such as dielectric constant, the thickness and the dissipation factor is the same with previous work at 2.5 GHz. According to bias in class AB, the main amplifier operates on a bias point of V_{GSm}= -2.2V and V_{DSm}= 28V (I_{DSm}=280 mA), as well as, the peaking amplifier is biased at V_{GSp}=-3.52V, in class C.

The following sections describe the detailed design of the proposed DPA with Class AB main stage and Class C peaking stage, step by step.

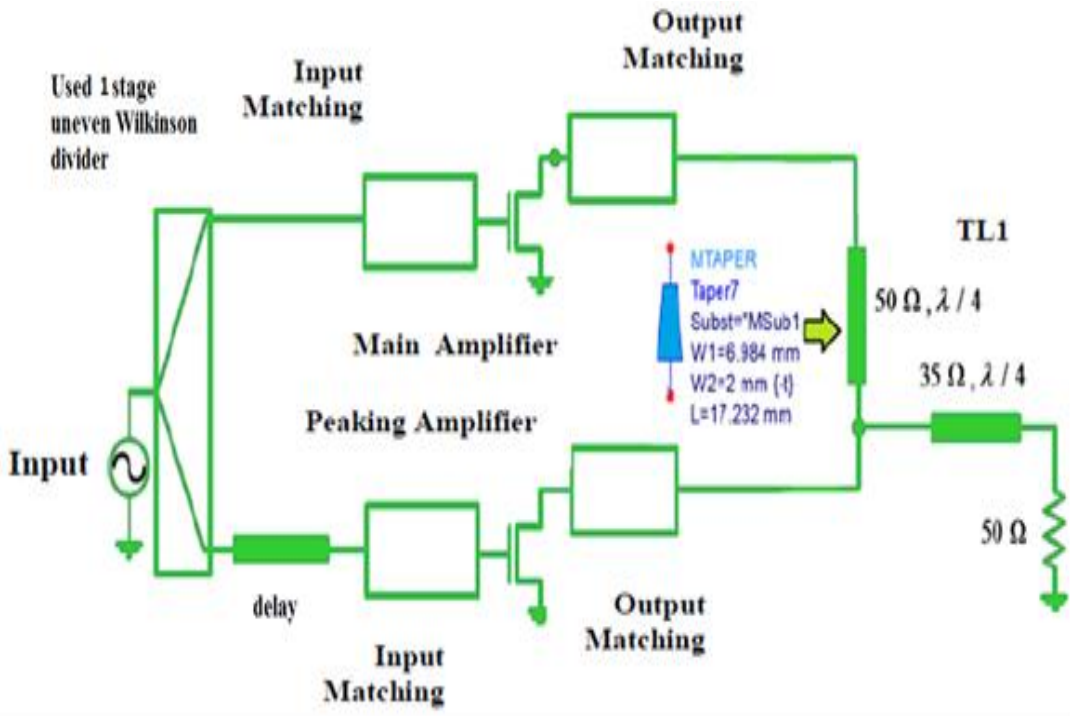


Figure 3.12 Proposed DPA by using a tapered line as impedance inverter

3.3.2 DC analysis

In Figure 3.13 the operating points of the used HEMT corresponding to the different classes of operation can be easily determined from the transfer characteristics of used transistor (CGH27015F). In addition, it can be seen from Figure 3.13, the simulated circuit of the used transistor in ADS with the drain current of transistor versus the V_{GS} of CGH27015F based on the selected drain voltage (28V) in Figure 3.14.

The Figure 3.14 represents the performance of the drain current of transistor versus V_{DS} of the transistor in a variable frame of V_{GS} (from -4 to -1.5 V) in 0.2V steps with the load line of the transistor. Considering to the need a proper biasing voltage and the corresponding mode of operation the drain voltage is selected in 28V as mentioned before. Plus, regarding the applied different amplifier classes (class AB and C) working in the DPA and the DC load line of the used transistor (CGH27015F), the values of V_{GS} in both amplifiers are addressed to -2.2 V and -3.5 V as shown in Figure 3.14.

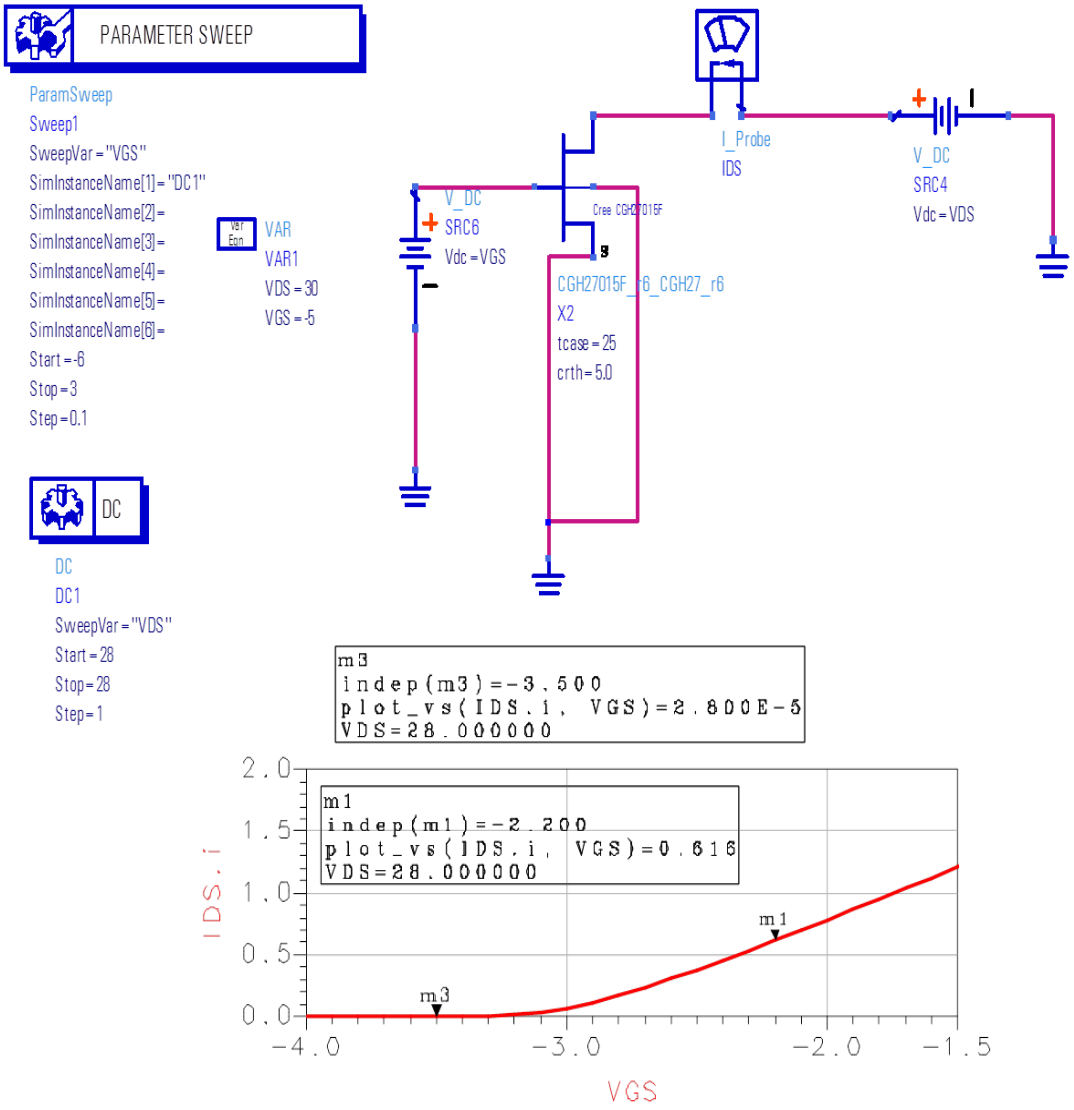


Figure 3.13 Transfer Characteristics of CGH27015F

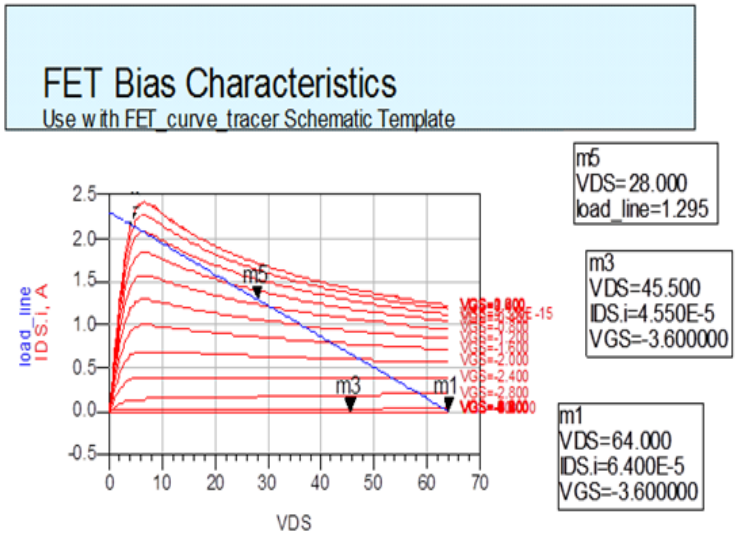


Figure 3.14 Output Characteristics of CGH27015F

3.3.3 Biasing network

As it mentioned before, a bias network should be designed without any influence in the matching networks and not spoiling RF power in the amplifier. Although using transmission lines with bypass capacitors is an ideal way to bias the voltage supply in PAs, however, in order to have an enhancement bandwidth performance on biasing network, a new design of this network is presented in Fig 3.15. In this way, the biasing network may be implemented by using microstrip components such as λ / 4 lines and radial stubs as shown in Figure 3.15.

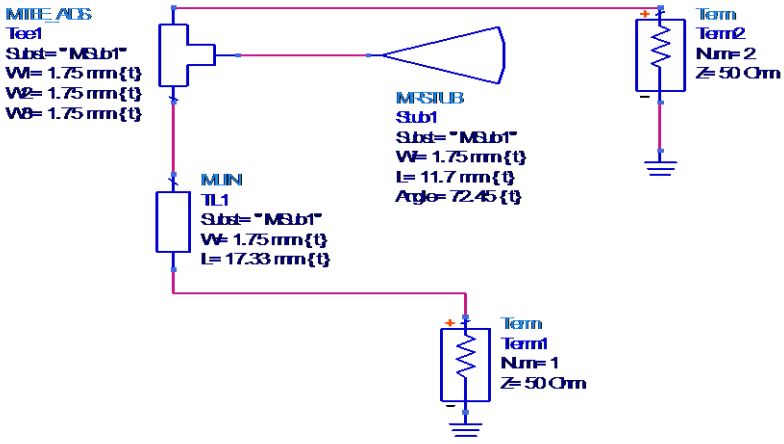


Figure 3.15 Biasing network in proposed DPA

To indicate the performance of the proposed bias network for both of the gate and the drain nodes of the main and peaking amplifiers, the seen impedances of the bias networks are simulated with the reflection coefficient S_{11} and S_{22}. As shown in Figure 3.16, by using the Smith chart, the impedance of the biasing network from the transistor drain and the biasing voltage is mentioned by Term 1 (S_{11}) and Term 2 (S_{22}), respectively.

Based on these results in the Smith chart, at the center frequency of 2.5 GHz the seen impedance in Term1 (see Figure 3.15) is very high compared to the seen impedance in Term 2, which has a low magnitude. Furthermore, considering the S_{21} parameter, it results in a proper performance with the proposed bias network in the frequency range of 1.7 to 3.3 GHz in order to reach a desired bandwidth (see Figure 3.16).

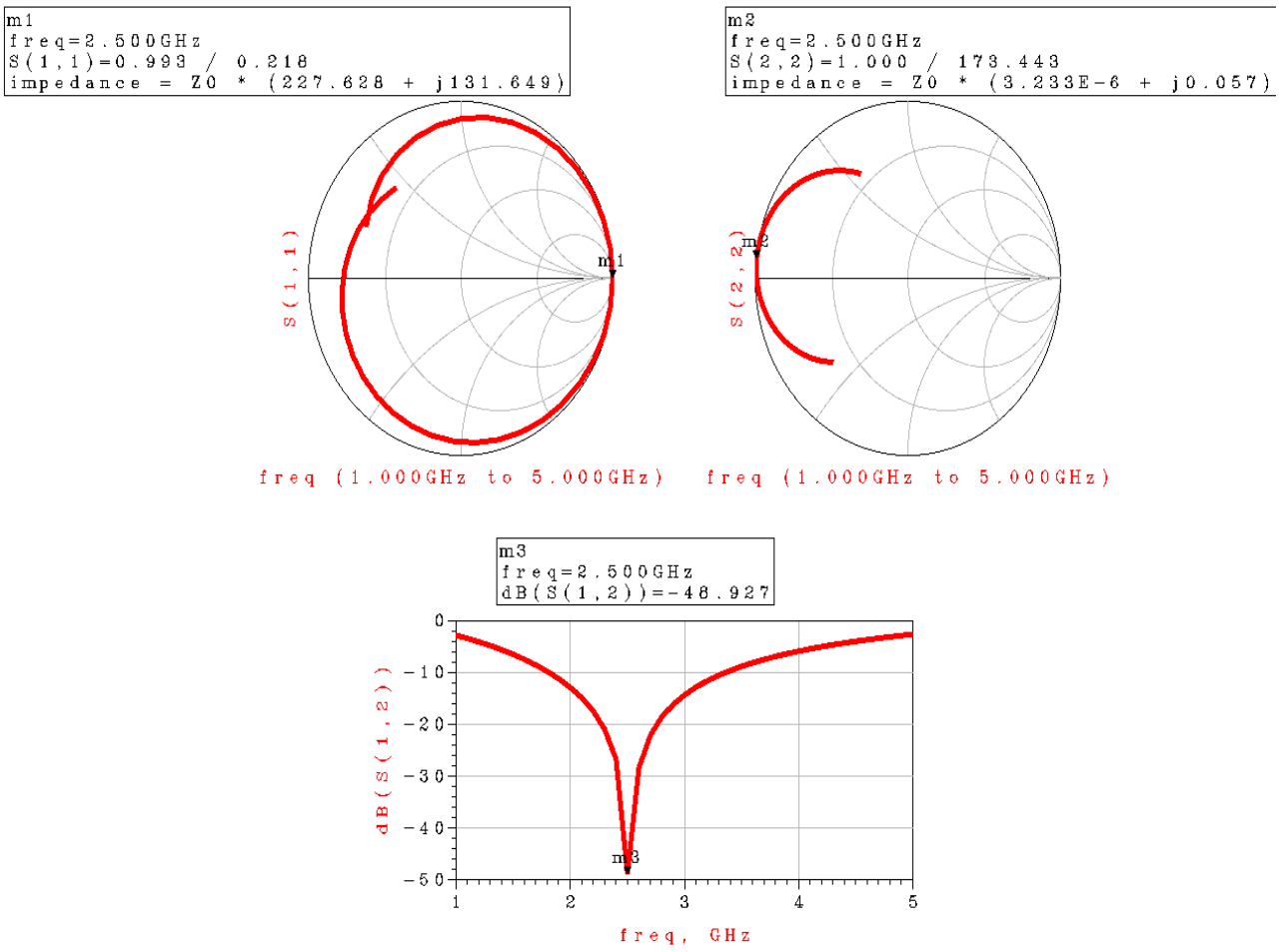
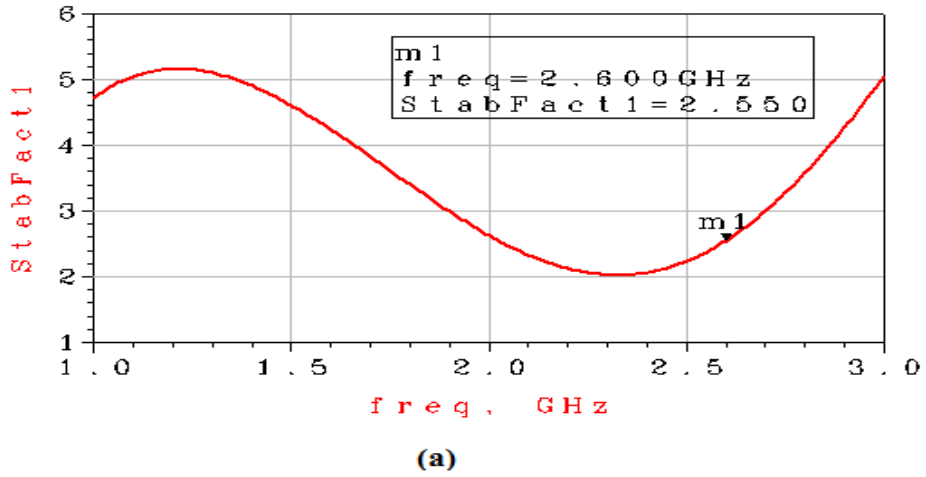


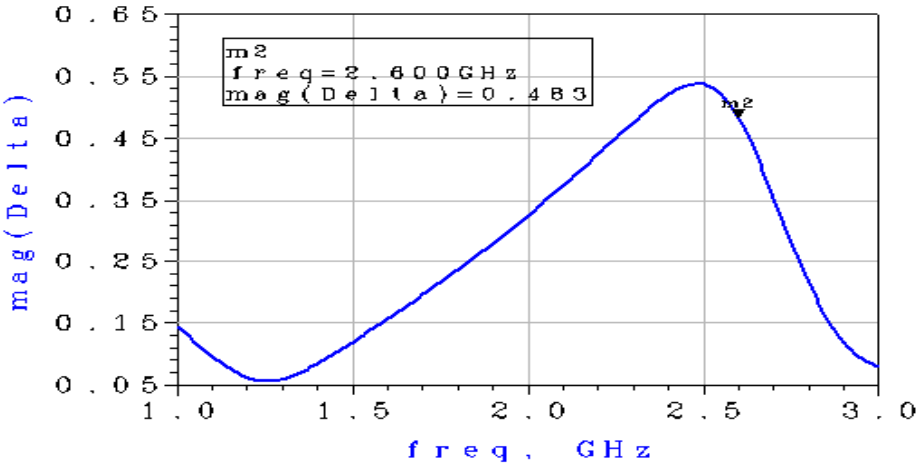
Figure 3.16 Performance of used biasing network

3.3.4 Stability of DPA

As it mentioned before, the stability is one of the most important criteria that shall be considered in amplifier designs. In order to have a stable circuit in the proper frequency range of the proposed DPA, we have used 18 Ω ballasting resistors in both the input stages (class AB and class C) without wasting too much gain. As shown in Figure 3.17 and 3.18, both designed main and peaking amplifiers are verified to be stable in the entire frequency band from 1 to 3 GHz.



(a)



(b)

Figure 3.17 Stability in Circuit of Class AB (Stab factor (a) and Delta (b))

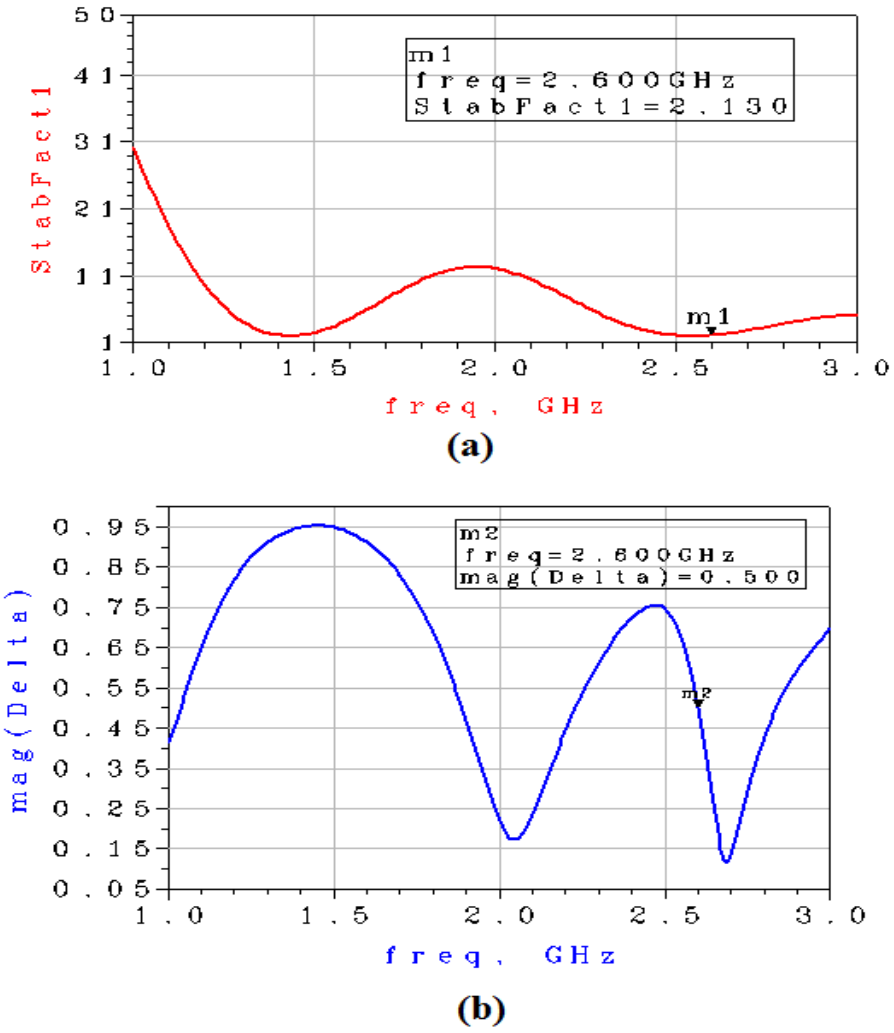


Figure 3.18 Stability in Circuit of Class C (Stab factor (a) and Delta (b))

Symbols of stab_factor and Delta (|Δ|) are related to the stability factors of the circuit. As discussed in section 3.1, in order to have an unconditional stability in circuit, we have used the K-|Δ| test. In other words, parameters of stab_factor and Delta are determined as K and |Δ| factors respectively. In particular, Figure 3.17a and Figure 3.17b indicate K and |Δ| factors of the main amplifier versus the frequency band in the range of 1 to 3 GHz respectively. As similar, Figure 3.18a and 3.18b show K and |Δ| factors of peaking amplifier versus the frequency band respectively. In this view, the factor of K should be higher than one as well as the |Δ| factor should be lower than one in whole of frequency ranges from 1 to 3 GHz respectively as shown in Figure 3.17 and Figure 3.18 for both amplifiers.

3.3.5 Matching networks

Before designing the matching networks for both amplifiers (main and peaking), we need to choose the optimum impedances that can be seen from the gate and drain of the utilized transistor (CGH27015F). To reach this purpose, source-pull and load pull techniques are used as it mentioned in previous sections. Source-pull and load pull simulations can be done in ADS by using the HB1Tone_LoadPull and HB1Tone_SourcePull designs guide with a nonlinear model of transistor (CGH27015F). Figure 3.19 to 3.21 show the simulation setup from this design guide and resulting load-pull contours for output power and PAE as a function of load impedance for both amplifiers (main and peaking). In this simulation, the device is biased at a drain voltage of 28 V and a drain current of 290 mA. The proposed biasing network besides the drain and gate biasing points based on their operation class (class AB or C) is utilized in this setup. Each contour in Figs 3.20 and 3.21 indicates a 10 % drop from the maximum efficiency. Optimum impedance in the peak efficiency is determined at the center of efficiency contours as mentioned in section 3.1.2. Regarding this point, the impedances seen from the gate and drain of both amplifiers are chosen.

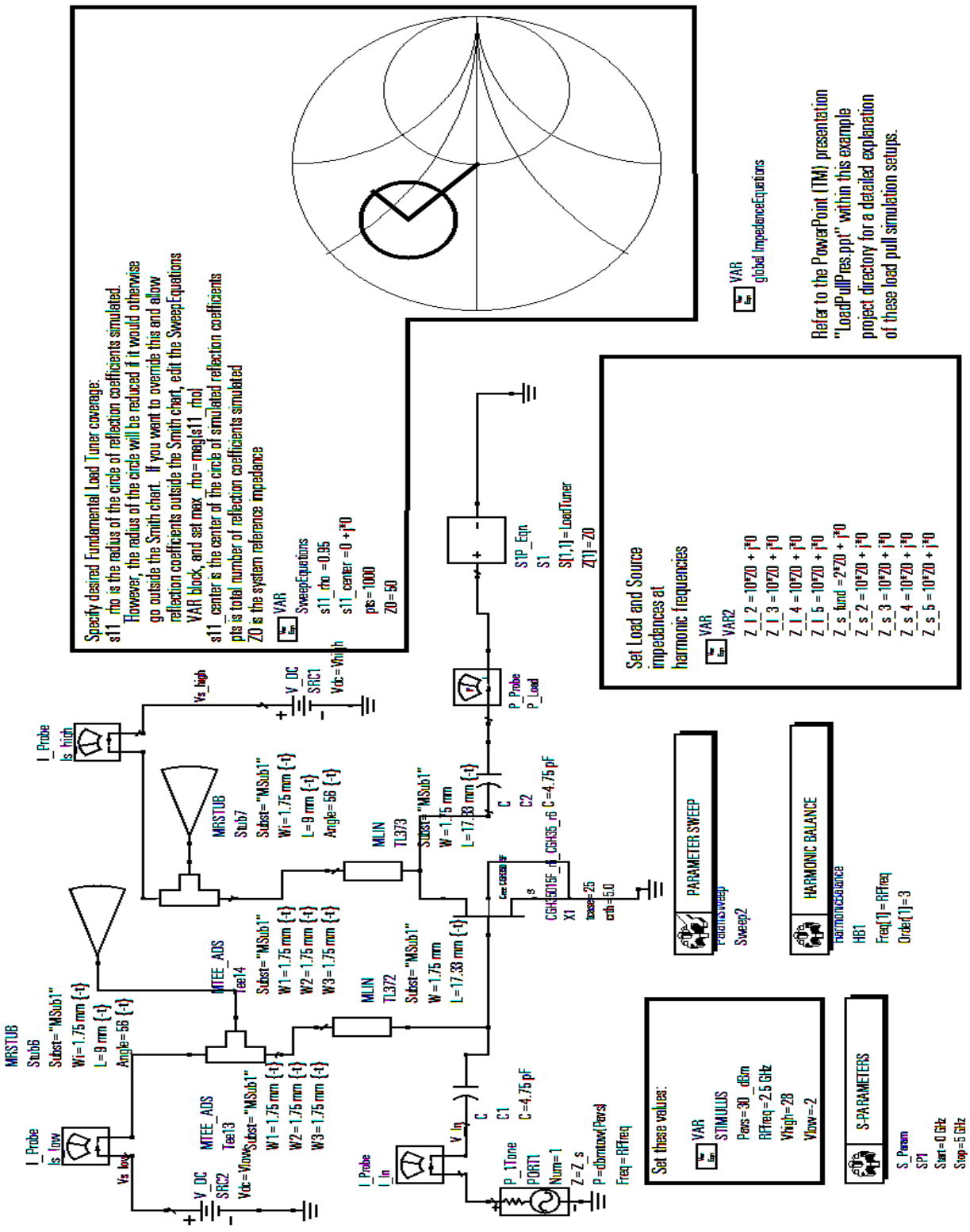


Figure 3.19 Circuit of design guide HB1Tone_LoadPull for 1-tone analysis in both amplifiers with difference biasing voltages

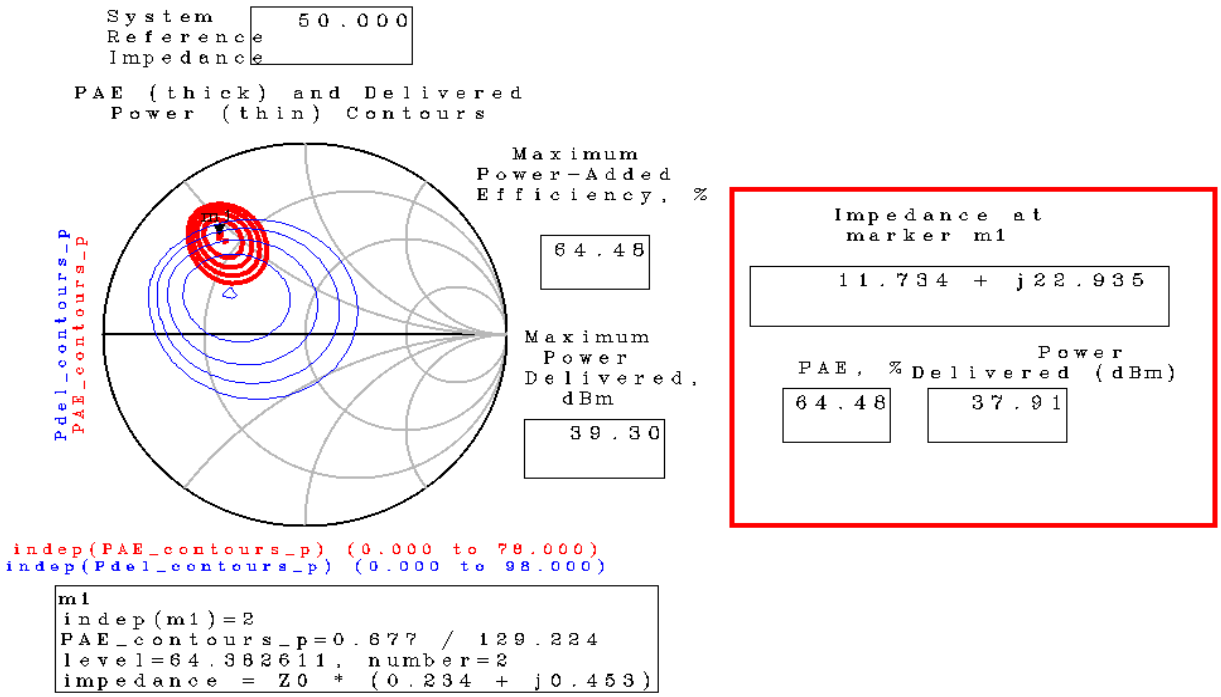


Figure 3.20 Resulting PAE and delivered power contours drawn in the Smith Chart in main amplifier for load pull analysis

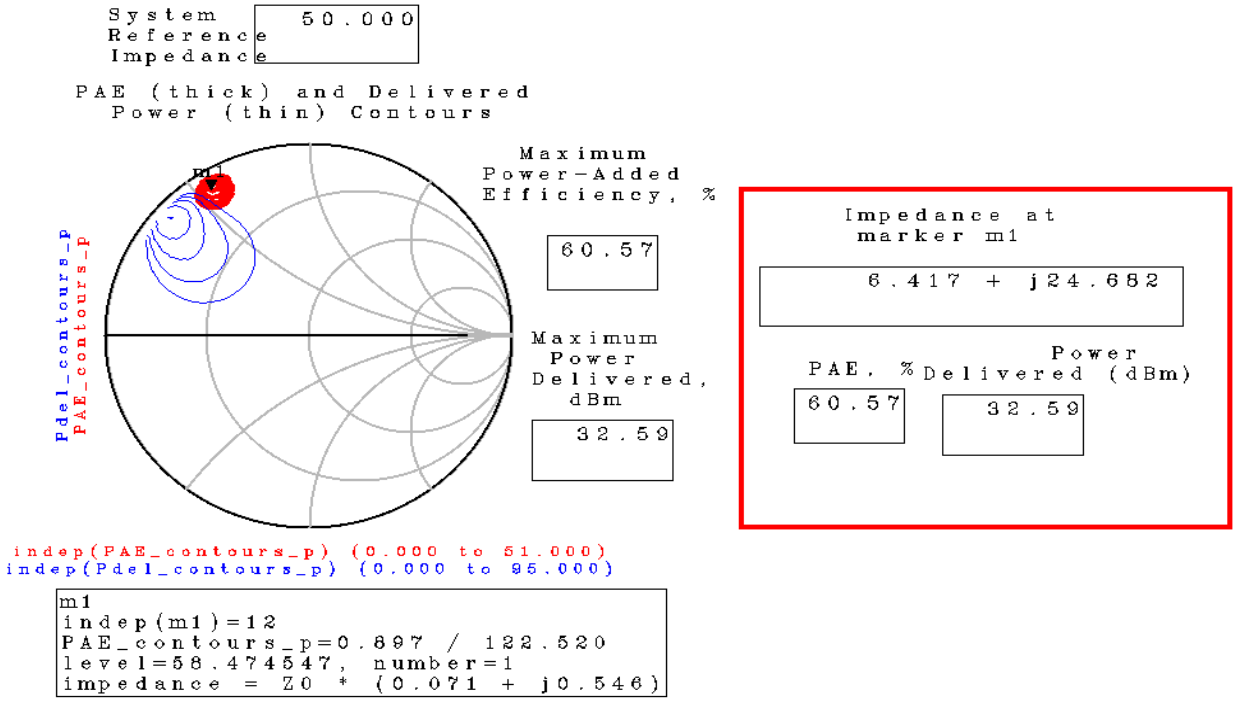


Figure 3.21 Resulting PAE and delivered power contours drawn in the Smith Chart in peaking amplifier for load pull analysis

In a similar way, as mentioned in previous sections, the source pull analysis is used for input matching as depicted in Figure 3.22. In addition, the optimum impedances in peaking amplifier are determined based on the maximum PAE in the source ports of main and peaking amplifiers as shown in Figure 3.23 and 3.24 respectively.

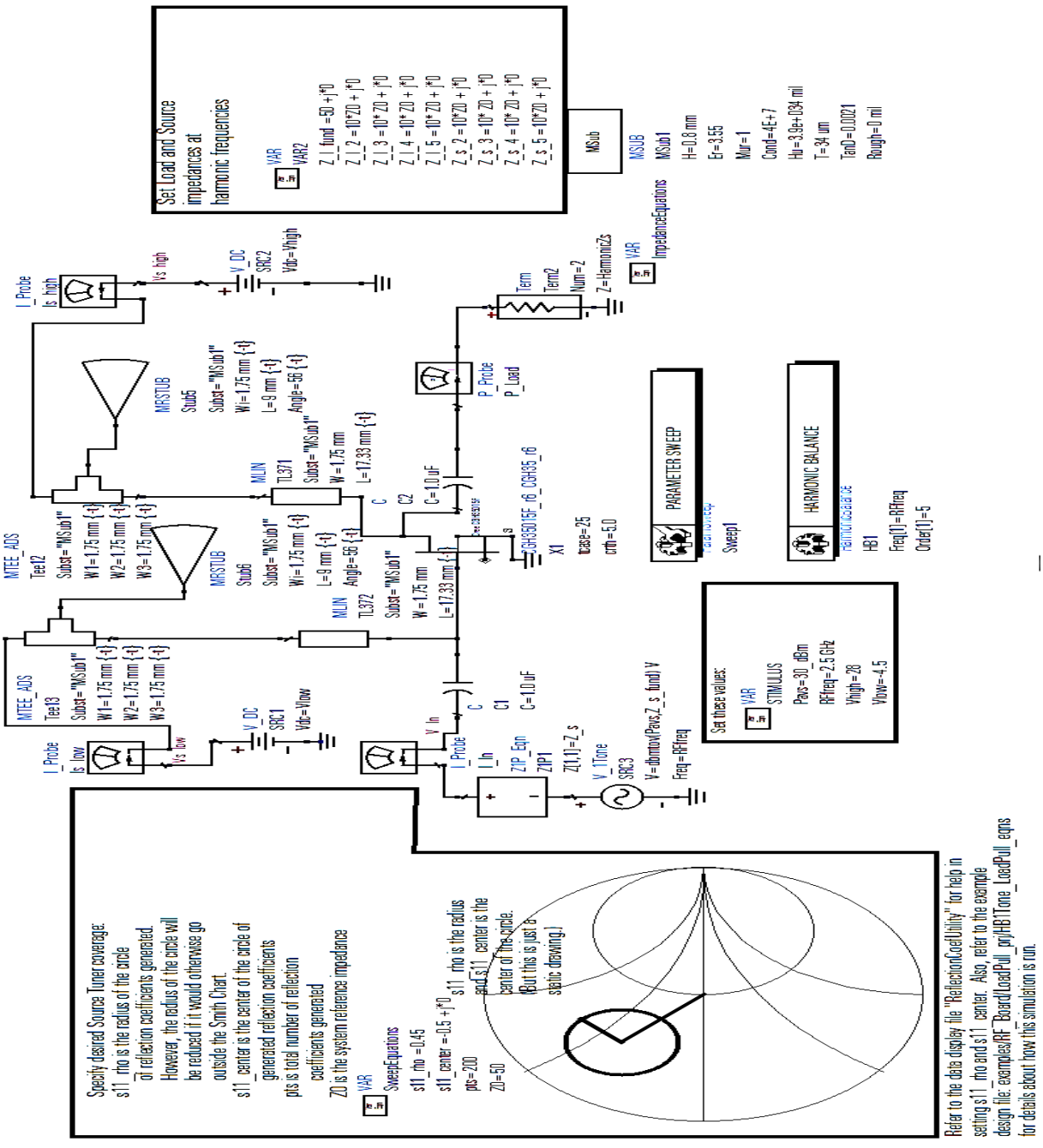


Figure 3.22 Circuit of design guide HB1Tone_Source Pull for 1-tone analysis in both amplifiers with difference biasing voltages

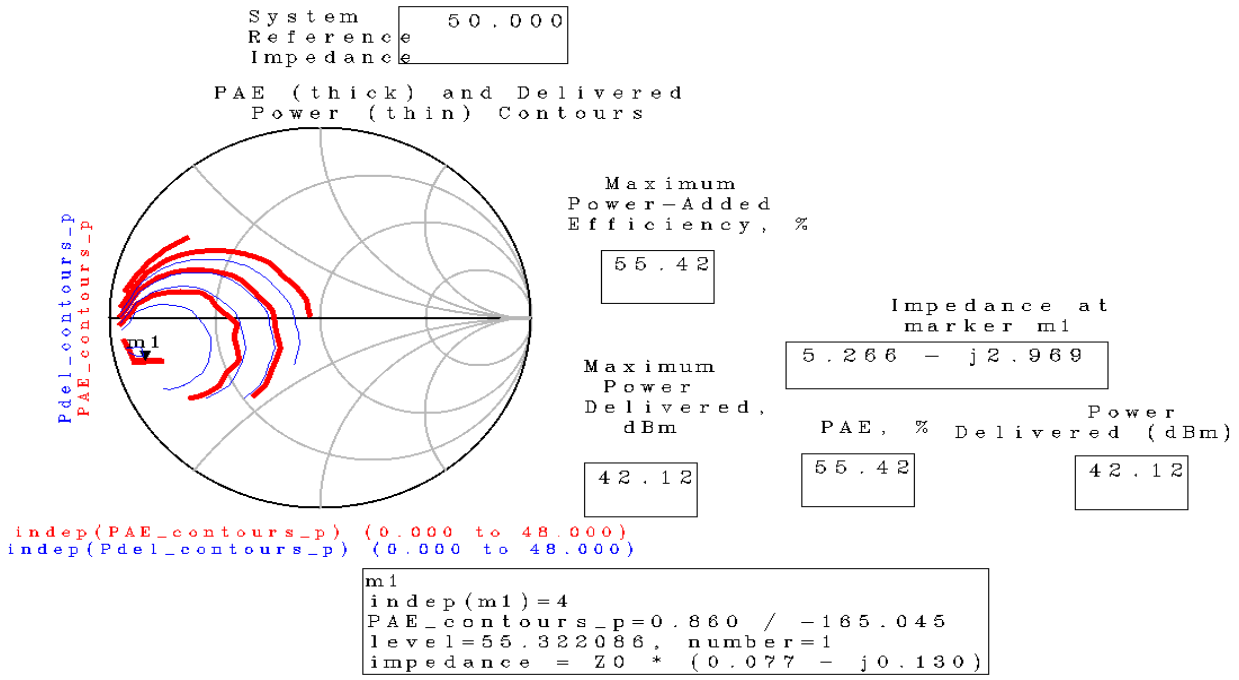


Figure 3.23 Resulting PAE and delivered power contours drawn in the Smith Chart in peaking amplifier for source pull analysis

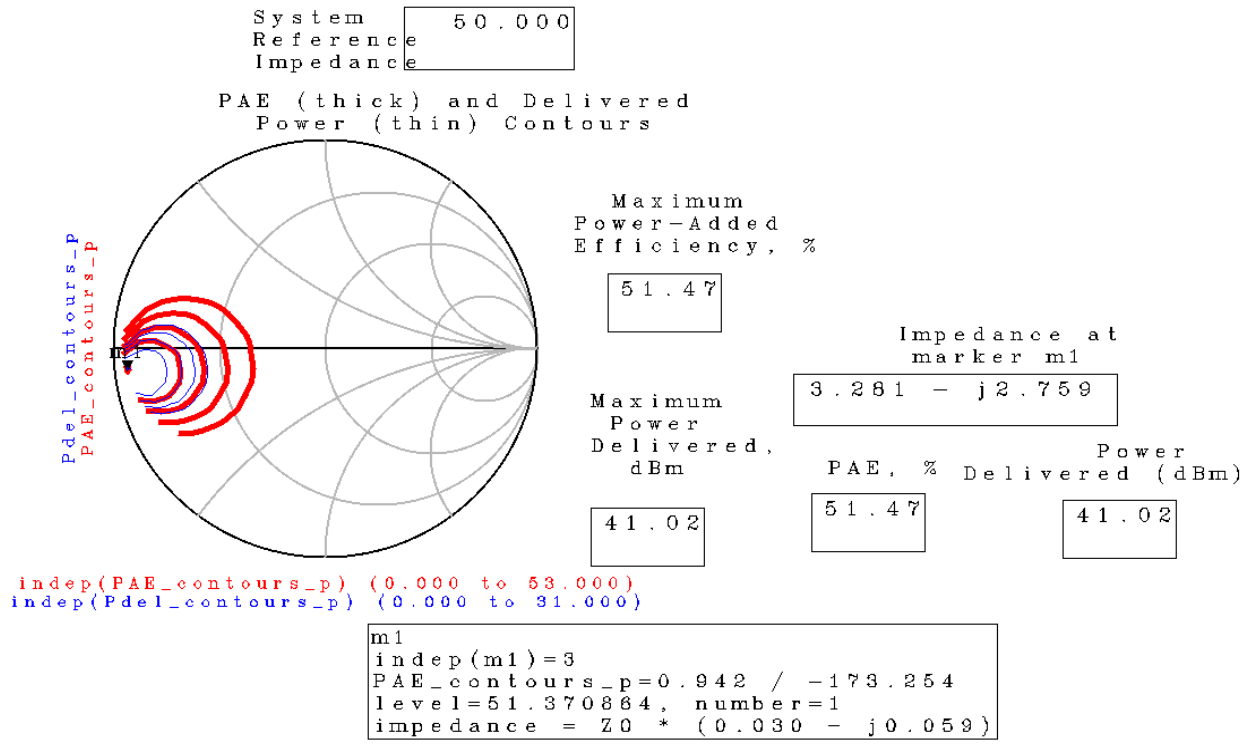


Figure 3.24 Resulting PAE and delivered power contours drawn in the Smith Chart in peaking amplifier for source pull analysis

Regarding the above load pull and source pull simulations, matching networks in both amplifiers have been implemented according to the obtained impedances from the input and output of main and peaking amplifiers. Output impedances of 11.73+j22.93 Ω and 6.41+j24.65 Ω in both main and peaking amplifiers, respectively, have been chosen aiming at having the maximum PAE. In a similar way, the optimum input impedances have been obtained with values of 5.2-j8 Ω and 3.26-j2.75 Ω for the main and peaking amplifiers respectively. The determined input impedances would be matched to 50 Ω in both input paths, while the chosen output impedances would be transferred to 100 Ω and 50 Ω in output of main and peaking amplifiers respectively, as indicated in section 1.4.1. In order to broad the band of the matching network in both the input and output impedances of the two amplifiers multi-section Chebyshev transformers have been used. In addition, the matching network of the main amplifier would be completed by using a tapered line in order to transfer impedances from 100 Ω to 25 Ω and to adjust the phase delays of the two paths. Moreover, a 1-stage unequal Wilkinson divider has been used in order to have a flat gain in the back-off range (Doherty region) for the proposed DPA (see Fig 3.13) [6] as previously mentioned. From the aforementioned design considerations and replacing the classical $\lambda/4$ transmission line by a tapered line, the proposed layout of the DPA is shown in Fig 3.27 were the 1-stage unequal Wilkinson is also displayed.

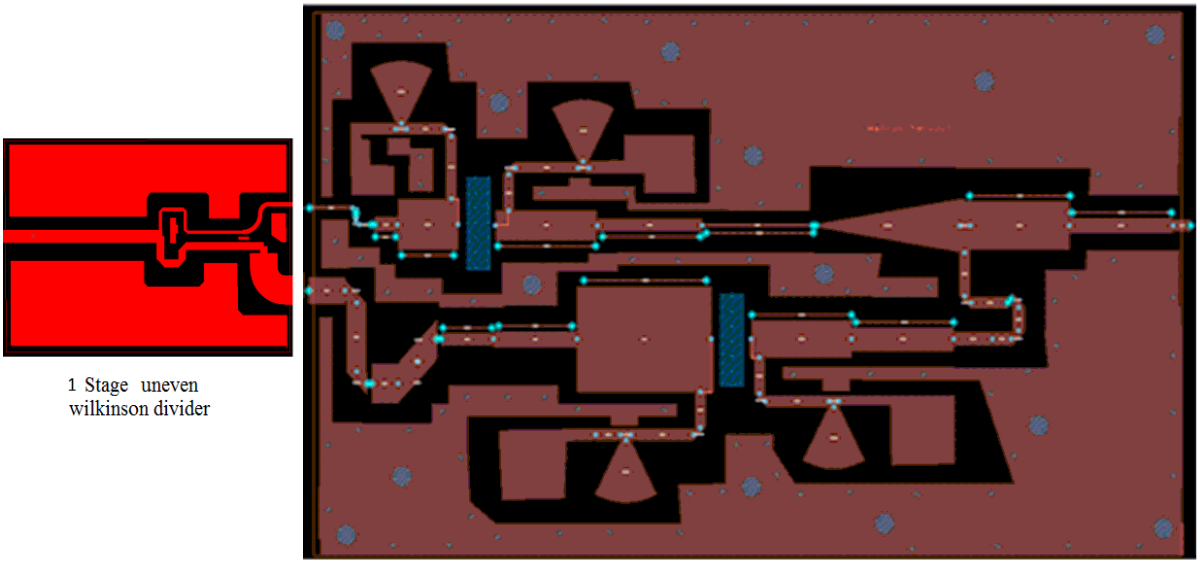


Figure 3.25 Layout of proposed DPA (two separated PCB layout 1-stage uneven Wilkinson and DPA)

Bearing in mind that the gain degradation in high power levels of DPA, as explained in section 1.4.2, the applied splitting ratio of the unequal Wilkinson divider is a combination of 1:4 such that 1 and 4 refer to the main and peaking inputs, respectively.

3.3.6 Simulation and experimental results

In this section simulation and measurement results of the proposed DPA will be presented. Figure 3.26 and 3.27 illustrate the scattering parameters of the proposed DPA, from simulation results and experimental measurements to assess the bandwidth of proposed DPA respectively. The S-parameters simulations are addressed in the frequency range of 1.5 to 2.9 GHz. Referring to these Figures, the measurements clearly show the same results as predicted by simulation results. According to the simulation and measurement of S_{11} and S_{21} parameters, it is verified the proposed design has an acceptable operation in the range from 1.8 GHz to 2.7 GHz.

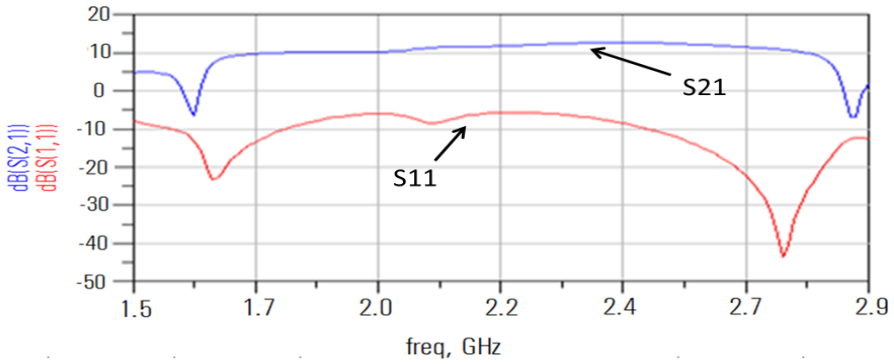


Figure 3.26 Scattering parameters of proposed DPA with 1- stage uneven Wilkinson divider in simulation

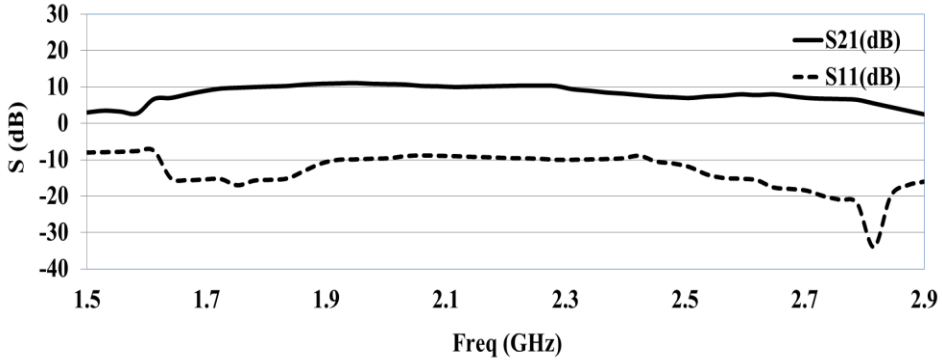


Figure 3.27 Scattering parameters of experimental proposed DPA with 1- stage uneven Wilkinson divider

However, a little degradation is observed at higher frequencies (>2.3 GHz) in S_{21} measurements. It may be due to the use of an improper connection between the load and the junction point of two branches (main and peaking), especially at high frequencies, as mentioned in the previous section.

The resulting PAE of the proposed DPA at saturated (maximum) output power and 6 dB output back off (OBO) is shown in Figure 3.28. According to these results, the simulated PAE at 6 dB OBO is higher than 30% and PAE in the maximum amount of output power is higher than 34% from 1.8 to 2.7 GHz. This indicates an allowable trade- off between the efficiency and bandwidth ratio.

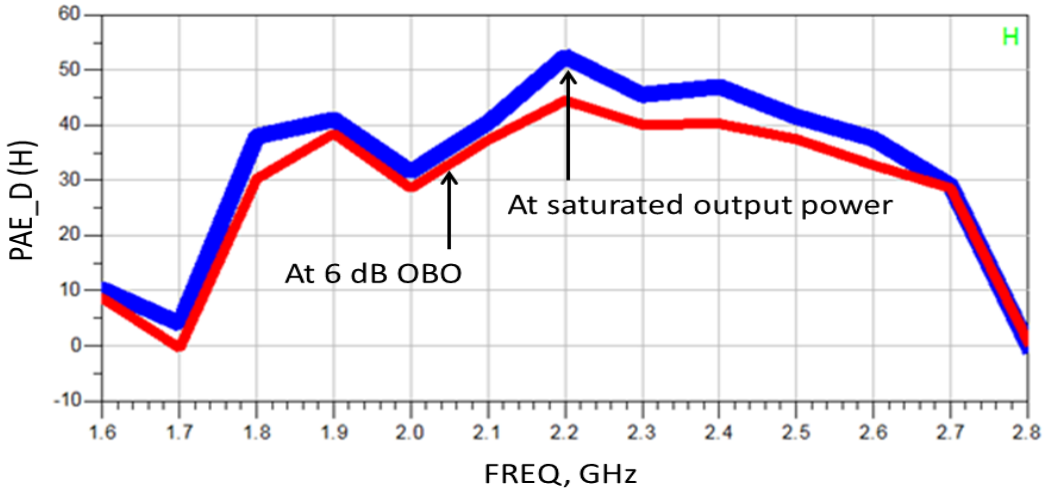


Figure 3.28 PAE of proposed DPA at: saturated output power (blue line), 6dB OBO (red line)

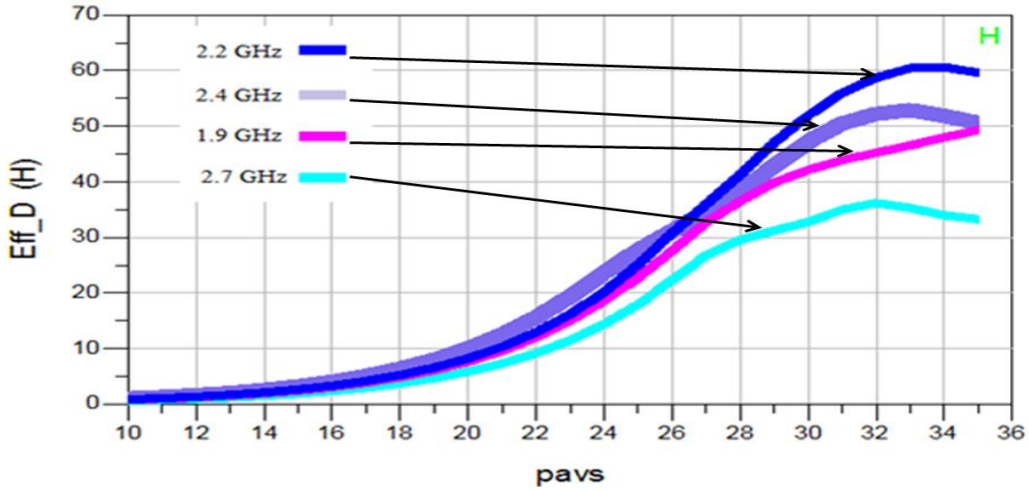


Figure 3.29 Simulated drain efficiency at 1.9, 2.2, 2.4 and 2.7 GHz as a function of output power

To consider the efficiency enhancement at the back-off power levels, the drain efficiency versus input power was simulated at different frequencies. Figure 3.29 depicts the simulated results of drain efficiency at 1.9, 2.2, 2.4 and 2.7 GHz versus input power. Based on these results, the variation of drain efficiency for the whole of the bandwidth is demonstrated from 36% to 60% at the maximum output power. As can be seen the reduction of efficiency in 2.7 GHz is occurred because of improper delay in turn-on the peaking amplifier. Besides the simulated drain efficiencies observe at maximum output power and at 6 dB OBO in Figure 3.30. According to this result, a reasonable drain efficiency performance is obtained by showing more than 33% drain efficiency in the range of 1.8 to 2.7 GHz at both 35 dBm and 30 dBm input power. In other words, these results have also confirmed the previous results in Fig 3.29. Considering the results of the power efficiency, it can be seen a trade-off between power efficiency and bandwidth. It means that by increasing the bandwidth, the power efficiency can be reduced.

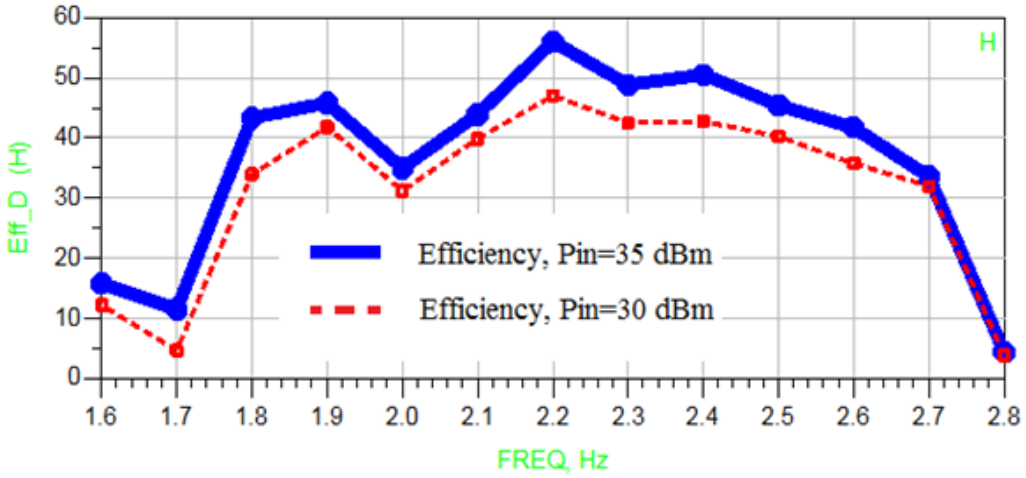


Figure 3.30 Simulated drain efficiency versus frequency at 35 dBm and 30 dBm (6 dB OBO)

From Figure 3.31, the gain of the proposed DPA is between 9 to 13 dB in both full Power output and 6 dB OBO, from 1.8 to 2.7 GHz. Moreover, as illustrated in Figure 3.32, the gain of the simulated DPA is greater than 10 dB at 1.8, 2.4 and 2.7 GHz. This two simulated results verify a nearly flat gain over the 1.8-2.7 GHz bandwidth, regarding the used asymmetrical Wilkinson divider. However, it should not be ignored the deviation of the gain in higher power levels, which is caused by the nonlinear device transconductance and the imperfect load

modulation as mentioned in previous sections.

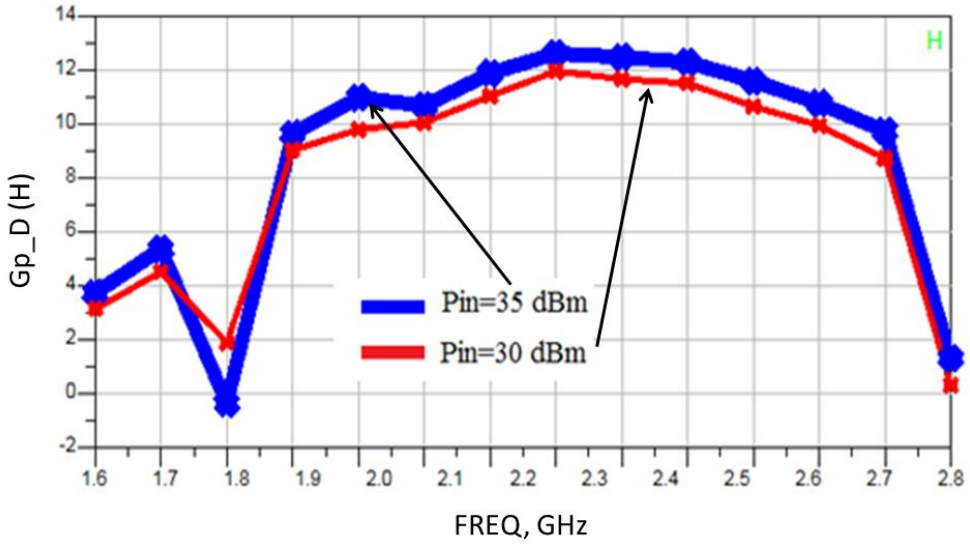


Figure 3.31 Simulated gain versus frequency at the input power 30 and 35 dBm

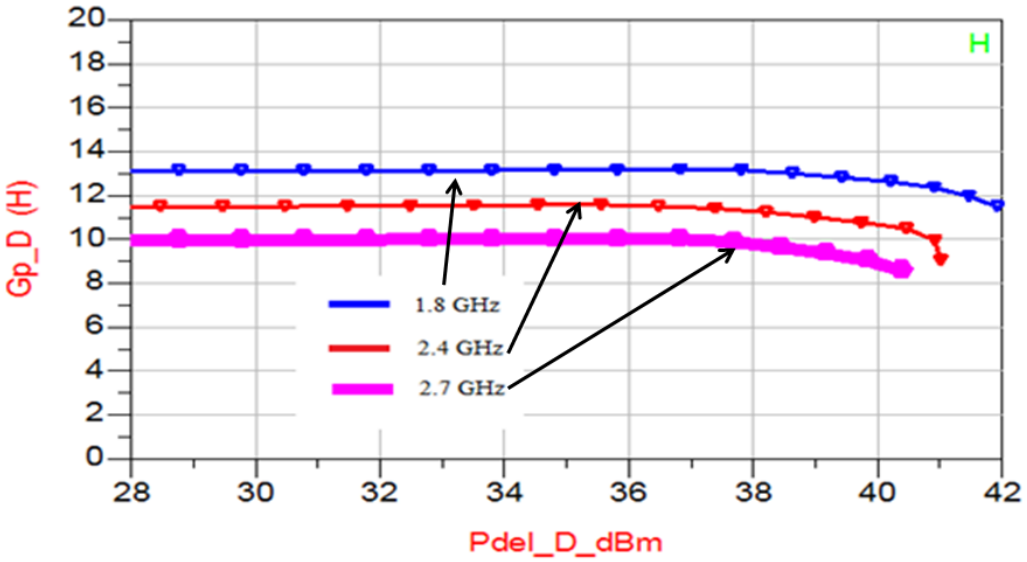


Figure 3.32 Simulated gain of proposed DPA versus output power at 1.8, 2.4 and 2.7 GHz

Based on Figure 3.33, the simulated output power in proposed DPA illustrates greater than 39 dBm in both full power output and 6 dB OBO for 1.8 to 2.7 GHz. In addition, the maximum output power is ranged in the whole of bandwidth between 10 W to 16 W. In order to confirm the whole characteristics of the implemented DPA, we have measured the output signal

of the implemented DPA by using the spectrum analyzer. Considering this operation, Figure 3.34 reports the measurement of output power by using 33 dBm Attenuator in the output of DPA with a Pre amplifier in order to supply our input power by 32 dBm (the linearity performance of the Pre amplifier is mentioned in Figure 3.35 from 1.4 to 3 GHz). Due to the limitations of the used signal generator (by 20 dBm), in order to measure the proposed DPA and more power for turning on the peaking amplifier, a pre amplifier with the 20 dBm output power is used.

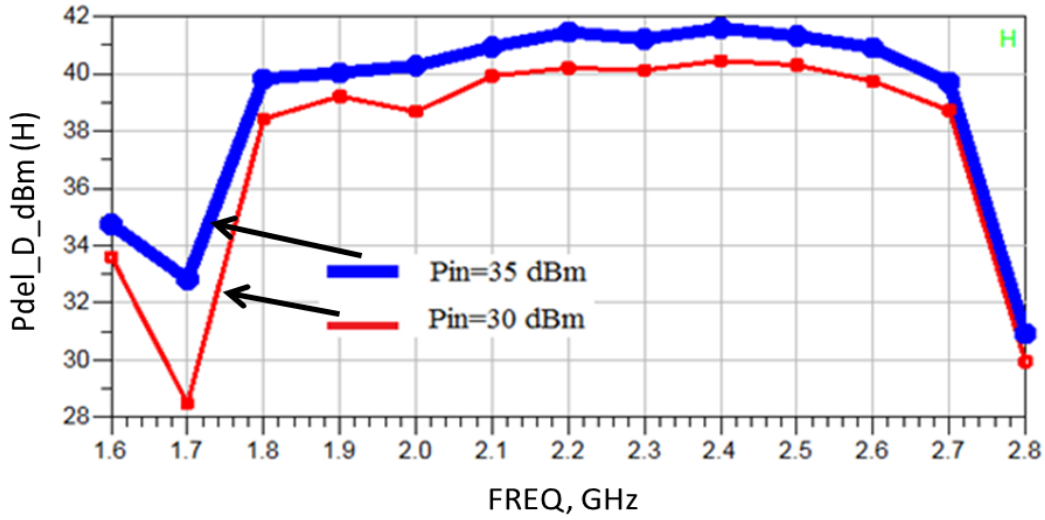
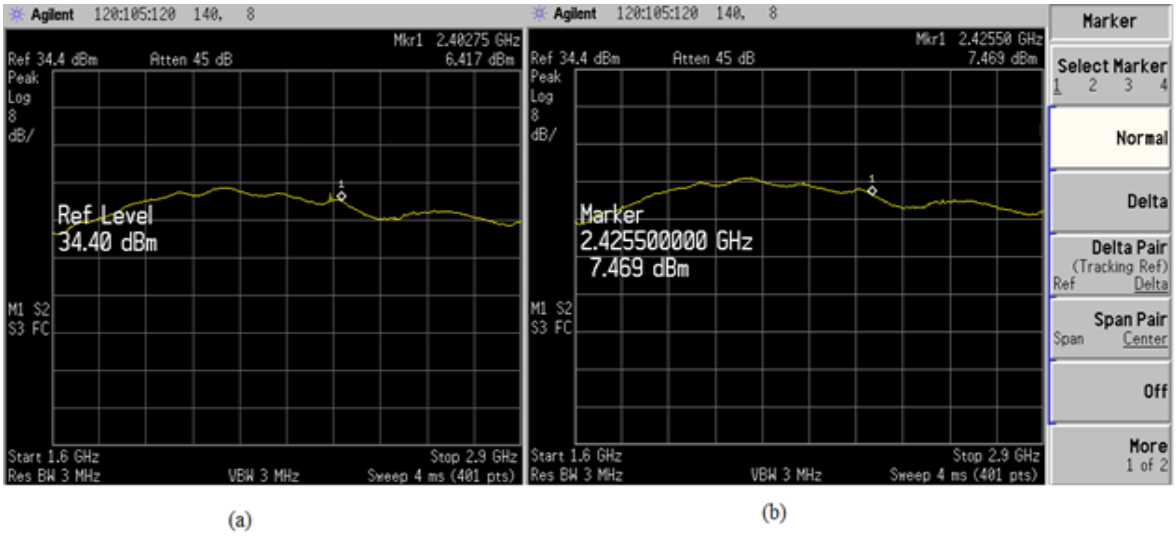


Figure 3.33 Simulated maximum Power output versus frequency at full power output (35 dBm Pin) and 6 dB OBO (30dBm Pin)



(a) (b)

Figure 3.34 Measured output power by using 33 dB Attenuator at P1dB (a) and saturated power of proposed DPA (b)

As shown in Figure 3.34, using a 30 dBm applied power driver, the output (by using a 33 dB attenuator) 7.47 dBm power has been observed at 2.5 GHz. Besides that, it has been shown for 28 dBm in power input (P1dB); output power of 39.42 dBm was achieved. This shows the results of measurement is close to the simulation and can be verified the proper performance of designed DPA.

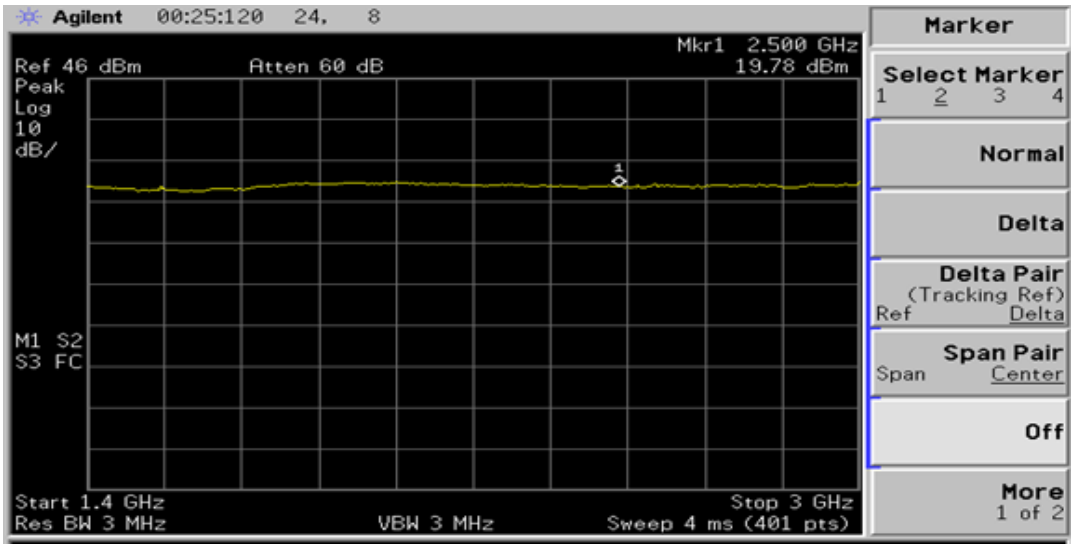


Figure 3.35 Performance of used the linear Pre amplifier to supply proper input power

In summary, according to the results of simulation and measurements, it can be concluded the frequency bandwidth in the proposed DPA is from 1.8 to 2.7 GHz for the 2.5 GHz center frequency. Moreover the achieved results have been compared with recent publications. The compared results suggest that our work has a competitive fractional bandwidth, keeping a proper gain (around 10 dB) and PAE in this range of frequency. The results are close to the achieved results in the reference [119], whose frequency range is similar and where it is used a Chebyshev transformer in the 35Ω, λ/4 transformer (see Figure 3.11) with the twice sections more than in our design. This is a fact to be improved in our next PCB design.

Chapter 4

Doherty-like architecture using a mixed combining network

4 Doherty-like architecture using a mixed combining network

4.1 Introduction

A recent and effective approach is based on the replacement of the λ/4 impedance inverter by lumped π networks or by multi-section transmission lines [124], [116], [114] and [118] as mentioned before. Other solutions, similar to Doherty [120] and sometimes even presented as DPA [113] use a combining network, which instead to act as an inverter; it makes the load modulation by means of a transformer that matches the DPA to the optimum load at the power back-off.

According to the tapered line which has been used in the previous design, and considering the obtained results together with some drawbacks, such as the reduction of the reflection coefficient when using a tapered line, in this section, a Klopfenstein taper is used as a transformer. Typically, a low reflection coefficient over the passband may be achieved by using a Klopfenstein taper. Moreover, that yields the shortest matching section; this allows the device to be as compact as possible. As explained before in this thesis, Klopfenstein taper has been experimented in DPAs [107] for matching the load, but not as an alternative to the load modulation scheme. In the line of [120] and [113], eliminating the narrower factors of DPA by using comparable load modulation architecture can be counted as the main idea. In summary, the work of [113] has been utilized a structure of DPA without using two quarter wavelength impedance inverters like the conventional DPAs. In this work, the both of amplifiers (main and peaking) are matched to 70 Ω at the output ports in order to reach an easier implementation of broadband matching networks as mentioned in state of the art.

Moreover, as it presented before in [120] the wideband matching networks has been applied in both branches of DPA by eliminating the output impedance transformer and offset lines, which are introduced as the main limiting factors of the widening the DPAs. Consequently, the proper load modulation at the transistor drain levels have been achieved by designing the main and peaking amplifier's matching networks. Furthermore, the design of the output impedance of the peaking amplifier as a frequency-varying susceptance has been led to a more

helpful structure than a quasi-open circuit impedance (as used in DPAs). Therefore, based on the works of [113] and [120], in next design we use a combining network as an impedance transformer. Here we merge multi-section transformers and a Klopfenstein taper. This combiner aims at solving the compromise between the DPA gain, PAE and BW, while providing a tool for the broadband adjustment of the main PA output reactance. This adjustment is based on the relatively easy control of the reactance at the output of the Klopfenstein taper, so allowing a good regulation of the relative group delay between branches.

According to the above presented, the design and the results of a DPA-like would be evaluated as follows.

4.2 Design approach

In this chapter, a novel Doherty-like power amplifier (DPA) has been fabricated by using 15W gallium nitride (GaN) CGH27015F transistors from Cree. At the beginning of the design procedure, a load-pull analysis for finding the optimum impedances for the HEMT devices has been performed (Fig 4.1). Referring to the Fig 4.1, the optimum loads are indicated on the 1.7-2.8 GHz band and the output power range from 33 dBm to 41 dBm for both of amplifiers (main and peaking). By comparing the impedances in different frequencies and varying impedance in different power levels (Doherty region) for 2 GHz in load-pull and source-pull, the optimal impedances are selected. For the class AB amplifier (main amplifier), the optimal impedances (regarding the power efficiency at saturated power and at the intermediate frequency of 2 GHz) have resulted 5.5+j7.5Ω for the input and 19+j7.2Ω for the output.

Similarly, for the class C (peaking amplifier), the input and output impedances have been 3+j4.5Ω and 7.8+j29.1Ω, respectively. In this design, the amplifiers are biased in Class AB (VGS = -2.5V, VDS = 28V) and class C (VGS = -5.5V, VDS = 28V) respectively. The substrate has been R04000. The passive biasing networks use radial stubs along with grounded bypass capacitors. Especially relevant has been the choice of the capacitors in the biasing of the class C amplifier, because of the risk of low-frequency oscillations (the μ–factor was delicate in this region).

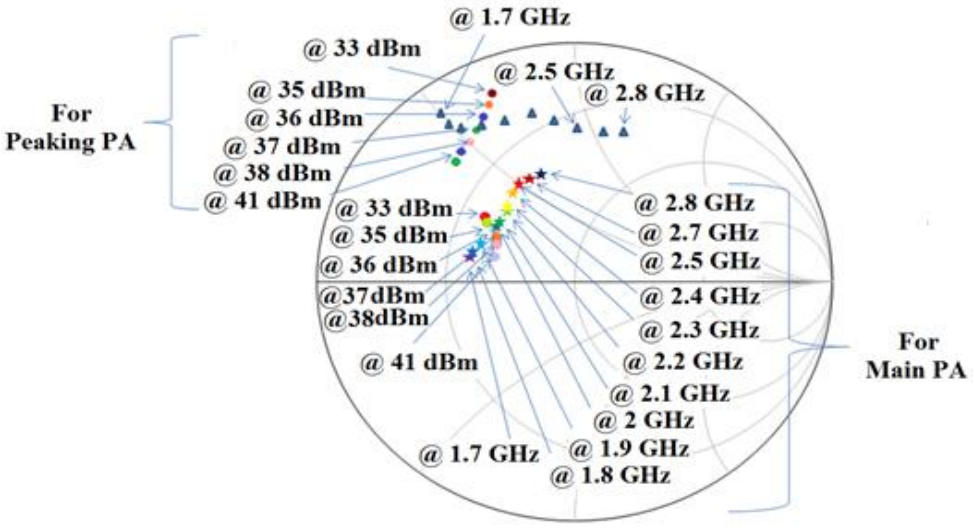


Figure 4.1 Output impedances of the main PA and peaking PA for maximum

power at different frequencies

The biasing networks of this design are following the previous one (using the $\lambda/4$ transmission line besides radial stub), but with two kinds of differences: a proper matching network at the frequency center of 2.25 GHz and changing in the schematic of the biasing network as depicted in Fig 4.2.

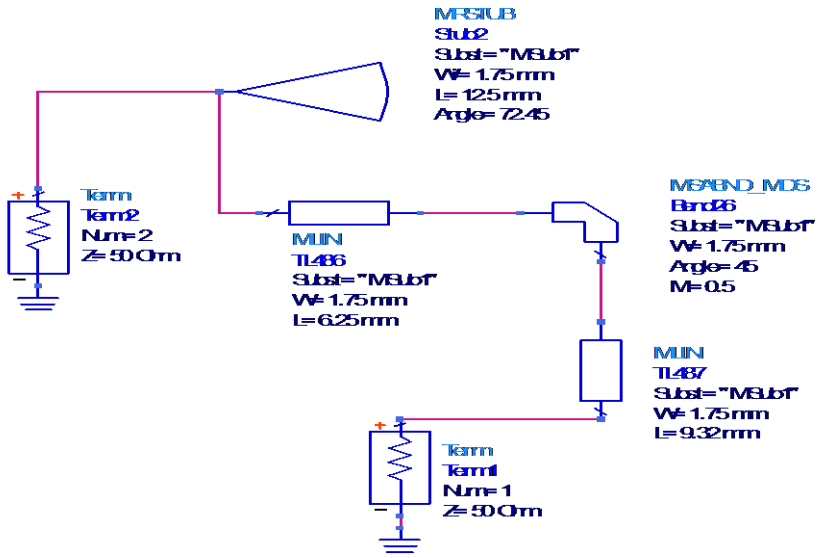


Figure 4.2 The schematic of the biasing network in implementing Doherty-like

Figure 4.3 shows the simulation performance of S_{11}, S_{22} and S_{21} parameters depend on designed biasing network in Fig 4.2 by the smith chart and a graph in terms of frequency range from 1 to 3.5 GHz. Such as previous simulations in the biasing network design, the value of S_{11} and S_{22} in terms of seen impedances illustrate a very high and few values in the center of frequency 2.25 GHz respectively.

Therefore, considering the above proposed biasing network and obtained results (shown Fig 4.3), the biasing networks can be acted without any affection on the performance of the matching networks in input and output of branches. Moreover, the performance of transferring factor (S_{21}) shows a reasonable bandwidth (from 1.5 to 3.1 GHz) in order to achieve a proper bandwidth in designed DPA. According to this result, the seen impedance of the bias network side that connected to the matching networks indicates a high value in order to reach an adequate performance in matching networks.

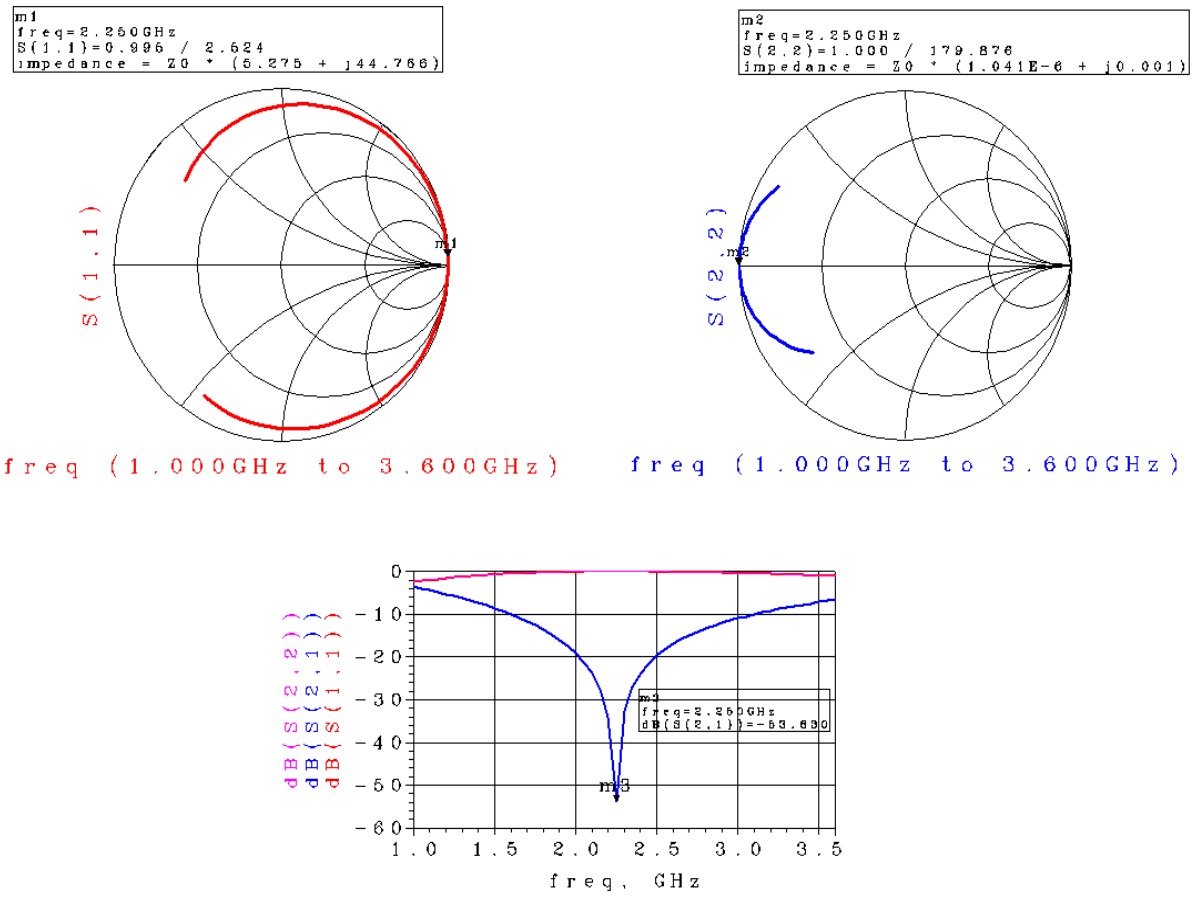


Figure 4.3 Results f biasing networks for DPA-like

The stability of main and peaking path is guaranteed by using an 18 Ω resistor as mentioned in previous design of chapter 3. To verify the stability of two amplifiers (main and peaking), the K-|Δ| test is simulated as mentioned before. Figures 4.4a and 4.4b indicate to stability factors of stab_factor and Delta of the main amplifier in terms of frequency range 1-3 GHz. Similarly, these factors are illustrated in Figs 4.5a and 4.5b for the peaking amplifier respectively. As it has discussed in the previous chapter, symbols of stab_factor and Delta in Figs 4.4 and 4.5 depend on the stability factors of the circuit. In this view, the value of stab_factor in both of simulations (see Figs 4.4 and 4.5) represent higher than one. Besides, the Delta values of both power amplifiers (main and peaking) are lower than Figs 4.4 and 4.5. Therefore, based on these results in Figs 4.4 and 4.5, the stability of the implemented DPA is guaranteed in over the band (from 1 to 3 GHz) based on the applied ballasting resistor.

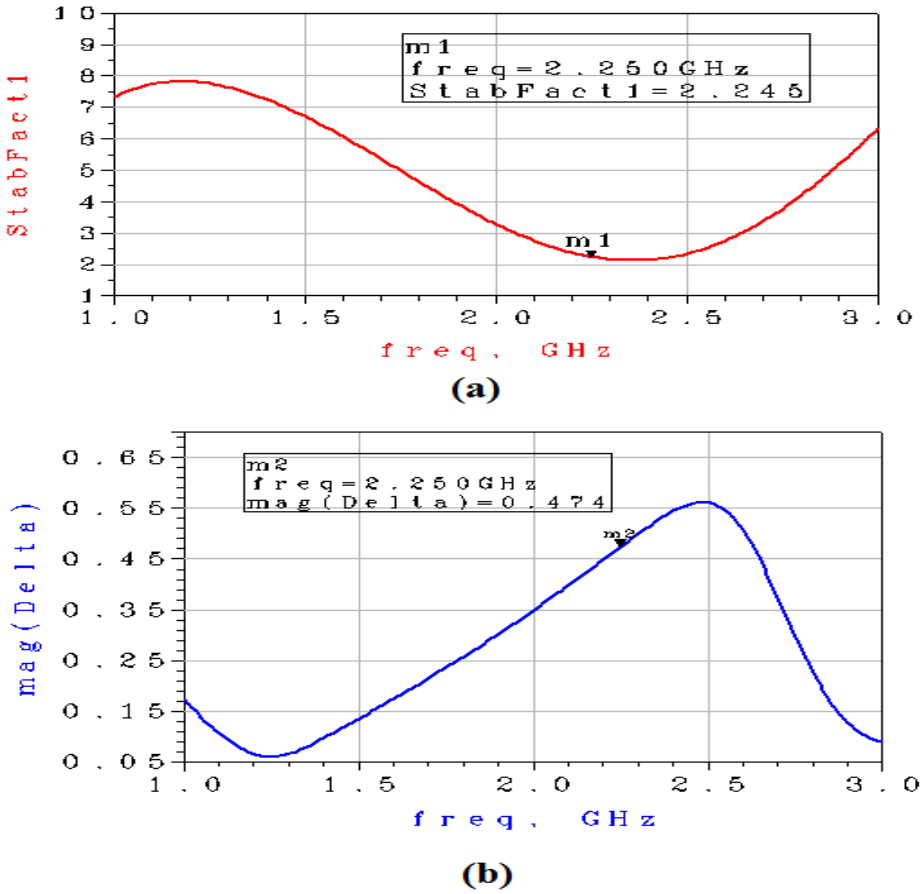


Figure 4.4 Stability in main stage: (Stab factor (a) and Delta (b))

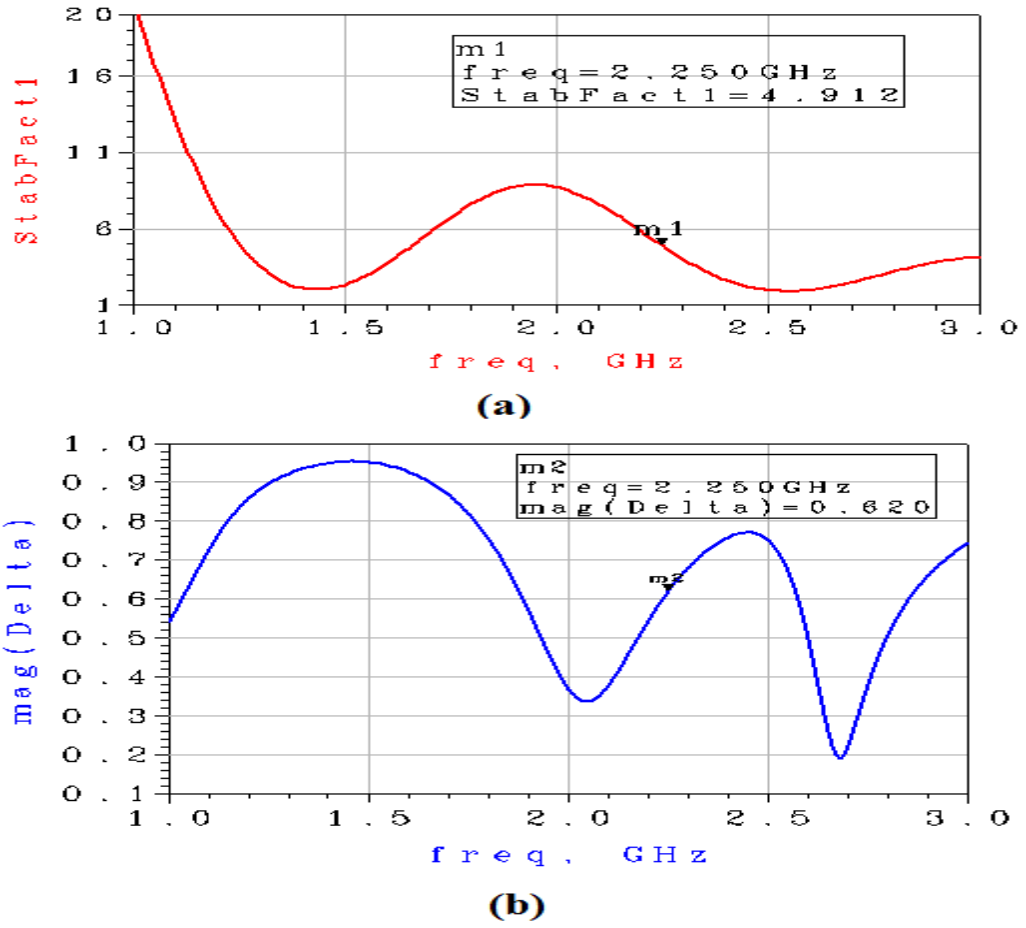


Figure 4.5 Stability in peaking stage :(Stab factor (a) and Delta (b))

The schematic of the proposed broadband DPA is shown in Fig 4.6. As it is described before, it follows the general structure of [113] and [120], being our OMN made in microstrip by merging binomial transformers and a Klopfenstein taper (the last just in the OMN_m on the main amplifier). The impedance at the Z_j junction point may be calculated as usual:

$$Z_m = Z_j\left(1 + \frac{I_p}{I_m}\right) \qquad 4.1$$

$$Z_p = Z_j\left(1 + \frac{I_m}{I_p}\right) \qquad 4.2$$

Where I_m and I_p are the drain currents of the main and the peaking amplifiers, respectively.

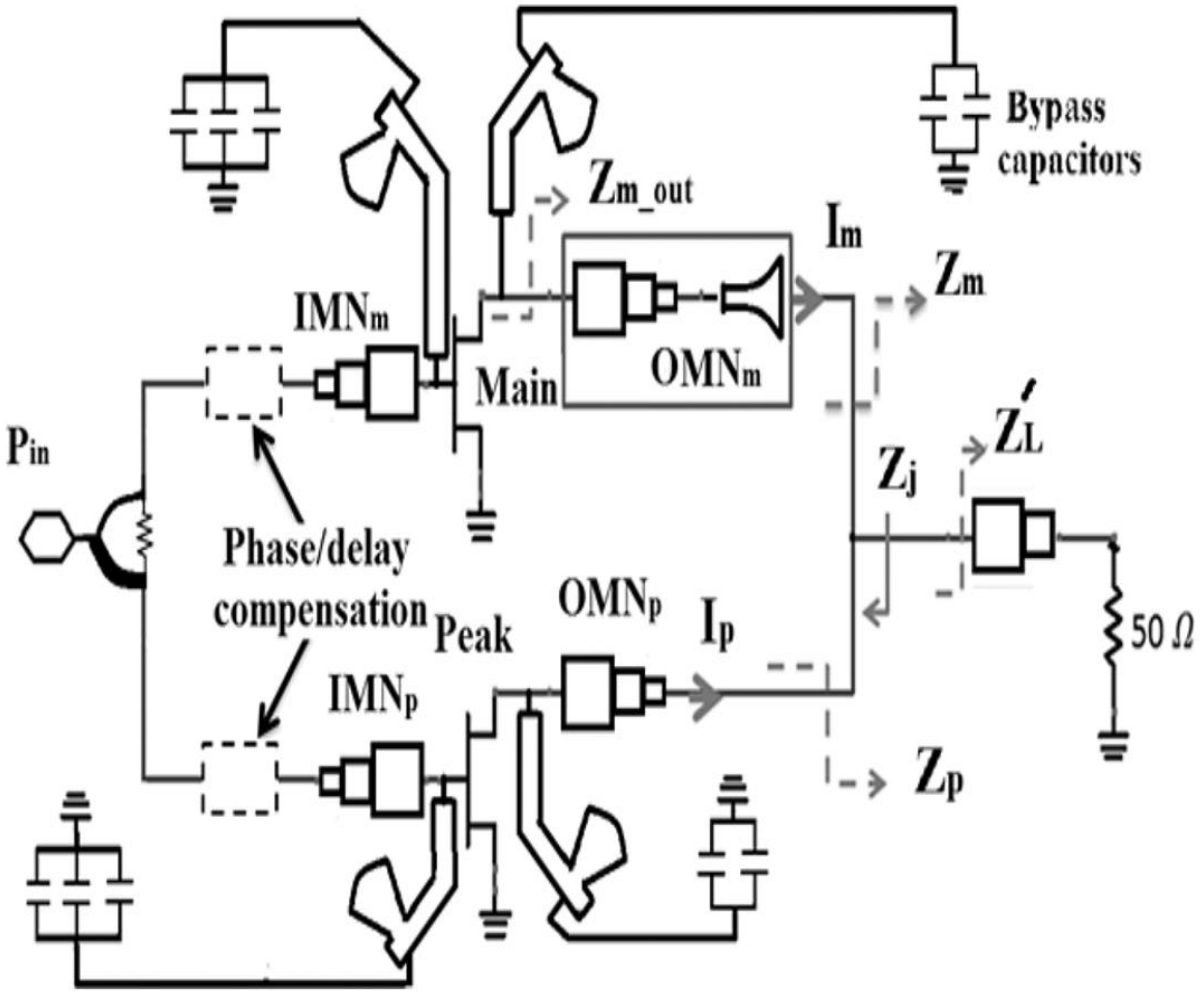


Figure 4.6 Schematic of the proposed Doherty-like PA

To tune the design, there are two starting points: 1) the value of Z_j should be, ideally, the same as Z'_L (25 Ω in the design) to nullify the return losses ($\Gamma(\theta)$), and 2) the OMN_m is split into a binomial transformer (for its BW) and a Klopfenstein taper [125] that, apart from the increased BW, allows a direct control of the Z_m susceptance by adjusting the length of the taper, according to

$$\Gamma(\theta) = \Gamma_0 e^{-j\beta L} \frac{\cos\sqrt{(\beta L)^2 - A^2}}{\cosh A} \quad \text{for } \beta l > A \qquad 4.3$$

Being $\Gamma(\theta)$ the reflection coefficient, and $A = \cosh^{-1}\left(\frac{\Gamma_0}{\Gamma_m}\right)$, $\Gamma_0 = \frac{1}{2}\ln\left(\frac{Z_L}{Z_0}\right)$, where Γ_m is the maximum ripple in the passband. The cutoff frequency of the taper decreases when either the

taper length increases or the value of the factor A decreases. No upper-end cutoff frequency exists (theoretically) as defined in the relationship of $\beta L > A$. The objective of the reactance adjustment is to control the OMN_m delay. As demonstrated in [6], a non-zero susceptance is preferable to a quasi-open circuit impedance (as in Doherty amplifiers) to achieve better BWs. The OMN_m is a reciprocal, loss-free two-port network:

$$S = \begin{bmatrix} S_{11} & \sqrt{1-|S_{11}|^2}\, e^{j\theta} \\ \sqrt{1-|S_{11}|^2}\, e^{j\theta} & -S_{11}^{*}\, e^{j2\theta} \end{bmatrix} \qquad 4.4$$

Being θ a parameter dependent on the network reactance that controls the group delay and, consequently, helps to equilibrate delays among branches. After ADS simulations searching for the compromise among gain, PAE and BW, with priority to the last feature; the tuned value of Z_j has been 22.68-j7.34 Ω (at 2.25 GHz).

The similarity of this value to the optimal Z_{m_out} may invite to match them directly, but in this case the filter parameters become too sensitive.

In particular, the PAE results are too sensitive to small tolerances in the design of such matching network (PAE drops by 10 -15 %). Therefore, we have constructed the OMN_m by combining a multi-section transformer and a Klopfenstein taper. The multi-section transforms the optimal Z_{m_out} (20.6+j12.67Ω) of the transistor to 85Ω, a value obtained from an optimization process aiming at the minimization of the R_L in the center of the band (2.25 GHz), and the taper moves this impedance to produce the aforementioned value of 22.68-j7.34 Ω at saturation (for Z_p = 48 Ω. At power back-off level the value of Z_m is 36- j24.4 Ω). According to (4.3), adjusting the reactance is so easy as to change the length of the taper or, alternatively, to allow different ripples in the passband. Our design has been made for $\Gamma_m = 0.01$. I.e. for a taper of 37 mm to allow the double in the ripple figure reduce the reactance to the half. Generally, based on the phase and group delay theory that depends on characteristics of used components in microwave systems for propagation of signals, adjusting the delays is necessary. The influence of these adjusting will determine especially in DPAs that there are two separated paths with each path performing at a determined time.

Indeed, by this adjusting, the loss of the output power in two paths of the DPA would be

reduced considerably. Moreover, regarding the direct influence of Γ (reflection coefficient) in phase delay of the output matching network in DPA especially in the main path, the value of Γ in applied Klopfenstein taper (from 85 Ω to 22.68-j7.34 Ω) is presented as depicted in Fig 4.7. In this method, according to practical limitations of PCB to match the two branches (main and peaking) outputs and proper amount of Γ (close to zero in real and imaginary part); the selected length for Γ of the proposed Klopfenstein taper is 37 mm.

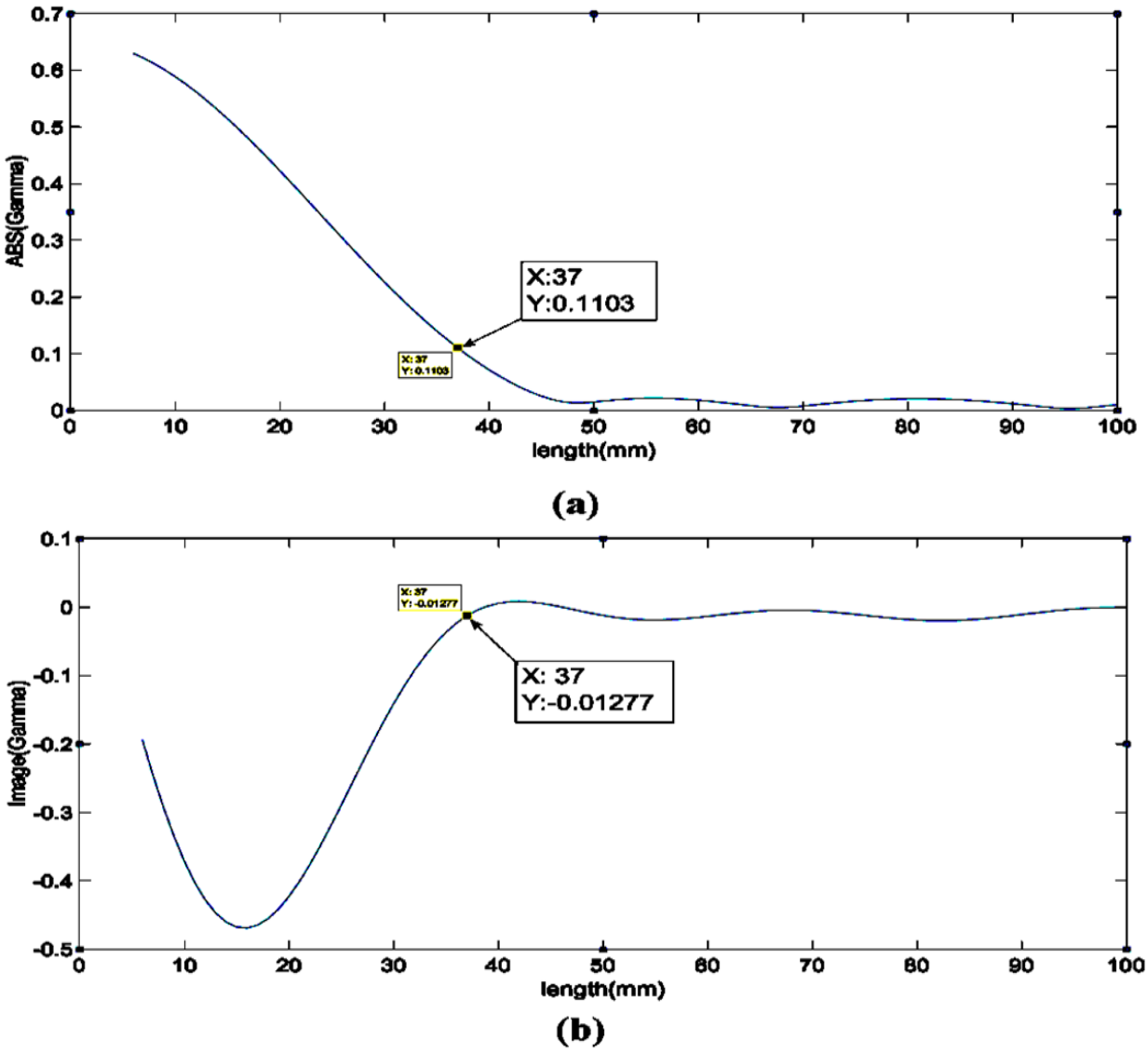


Figure 4.7 Real (a) and imaginary (b) part of Γ(θ) for used Klopfenstein taper

In order to confirm the length of proposed Klopfenstein taper (37mm), a comparison among S-parameters of Klopfenstein tapers in different lengths are presented in Figs 4.8a and

4.8b. In addition, as shown in Fig 4.8a, the S_{21} of Klopfenstein taper in 37mm has more relevant result than lower and higher lengths for low frequency until 10 GHz. Moreover, the S_{11} parameters of simulated Klopfenstein tapers have been reported the similar values (see Fig 4.8b). Obviously, based on obtained results and considering the phase delays in both paths of the DPA, a trade-off between adjusting the group delays (of main and peaking paths) and selecting the length of the Klopfenstein taper with a proper reflection coefficient is necessary.

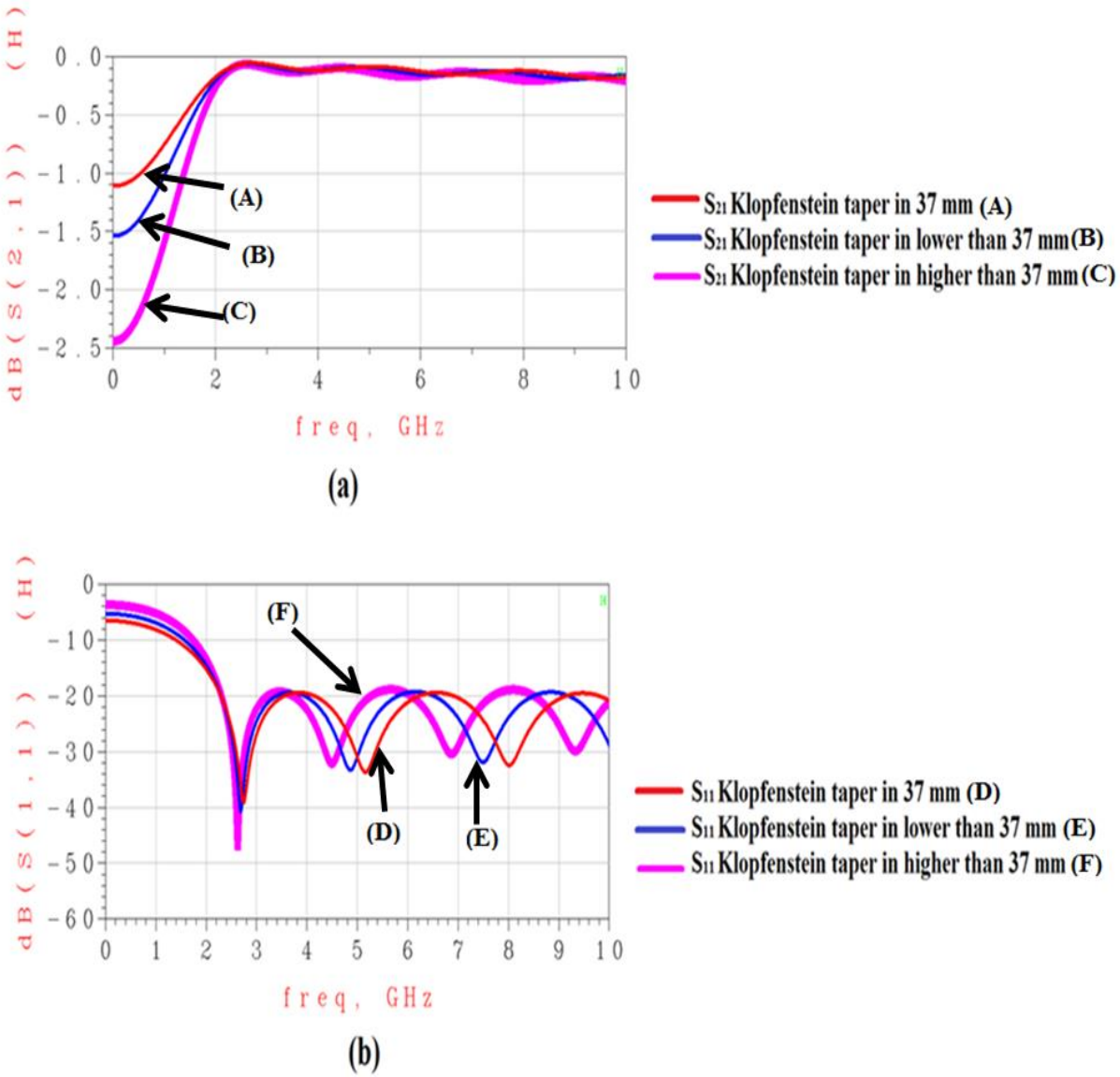


Figure 4.8 Comparison the S_{11} and S_{21} of the Klopfenstein taper can be used to transfer 85 Ω to 25 Ω in different lengths

In addition, in order to highlight the importance of the length of the Klopfenstein taper,

the output susceptance of the Klopfenstein taper is compared in 3 different lengths at the frequency range from 0 to 4 GHz. (see Fig 4.9). Based on this simulation, the values of susceptance on the Klopfenstein in the length of 37 mm are more closer to the zero value in the whole mentioned frequency rather than other lengths (in lower and higher value). Besides, the Klopfenstein shows a better performance in the length of 37 mm in order to have a proper control the susceptance in output impedances of the main and peaking paths. So, according to all of mentioned results, the reason of selecting 37 mm for the proposed Klopfenstein taper is justified.

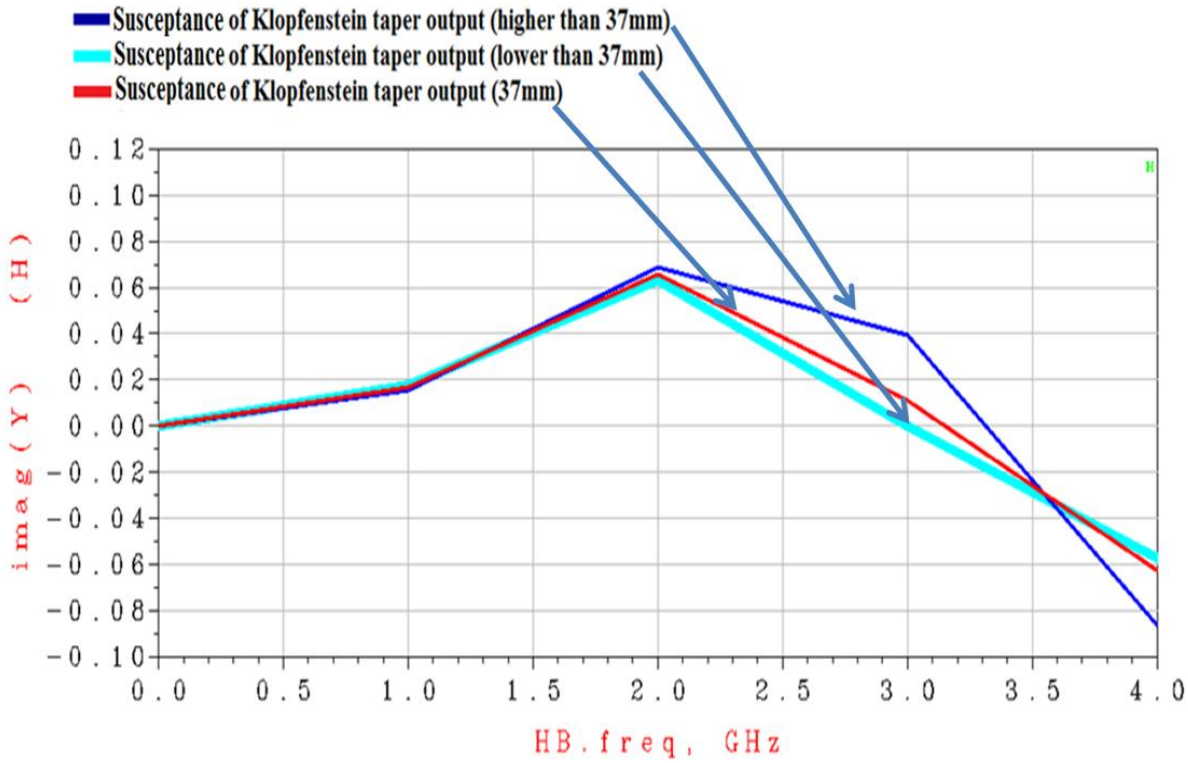


Figure 4.9 The susceptance of Klopfenstein taper output in different lengths

As advanced in Fig 4.6 to match the input impedances resulted from Fig 4.1 in both amplifiers (main and peaking), binomial multi-section transformers have been employed. Besides, a Wilkinson divider has been used to compensate the gain reduction in the Doherty region, with power asymmetries of 80% (20 % for the main amplifier) (see Fig 4.10), empirically adjusted for gain flatness as mentioned in chapter 1.

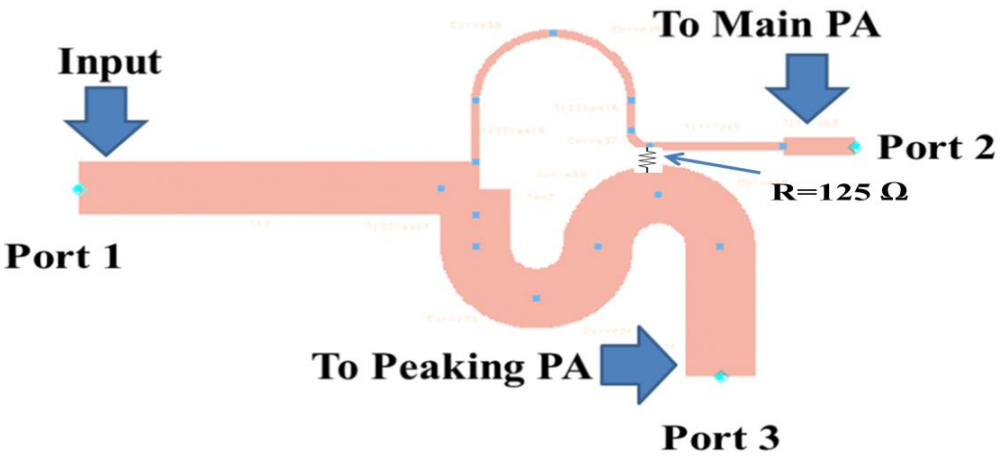


Figure 4.10 PCB design of uneven Wilkinson splitter (with Wilkinson divider resistance of 125 Ω).

To confirm the desired performance of the applied power divider, we are simulated the S-parameters of 3 ports related to the input and outputs connected to the main and peaking paths as shown in Fig 4.10. The simulated S-parameters of the proposed uneven power divider are shown in Fig 4.11. According to these parameters the isolation, matching and transmission parts are well designed in over the band (from 1 to 3.6 GHz). Considering the ratio of signal transmission between two paths, a 6 dB difference between see S_{21} and S_{31} can be seen in Fig 4.11. Based on the 80% - 20% division between two paths (main and peaking), the above mentioned, optimal impedances of inputs in main and peaking amplifiers have been matched to 120 Ω and 30 Ω using the binominal multi-section transformers with stability resistors and delay compensations, respectively.

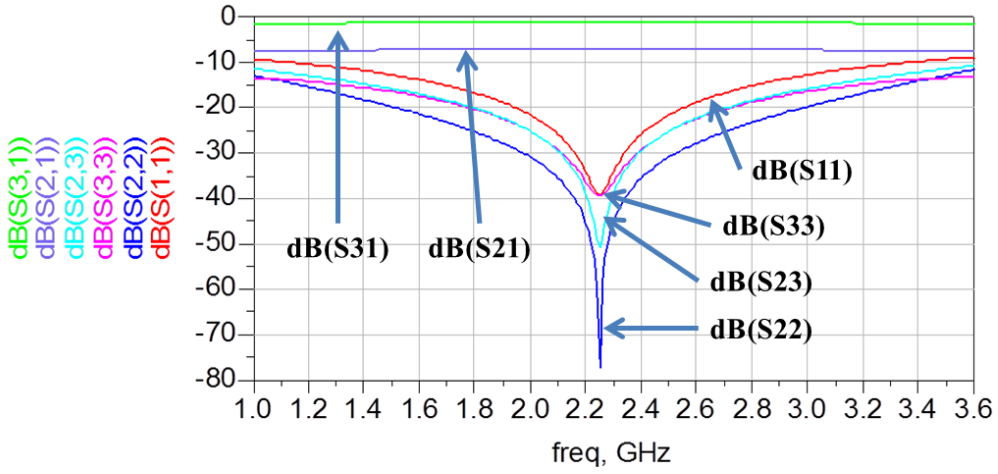


Figure 4.11 S-parameters of implemented uneven power divider

Considering the mentioned impedance values in the output of the unequal Wilkinson divider, input matching networks (IMNs) are matched by the binominal multi-section transformers from 5.5+j7.5Ω to 120 Ω and from 3+j4.5Ω to 30 Ω in the main and peaking amplifiers respectively.

Based on mentioned details, the fabricated prototype of the DPA is shown in Fig 4.12 .

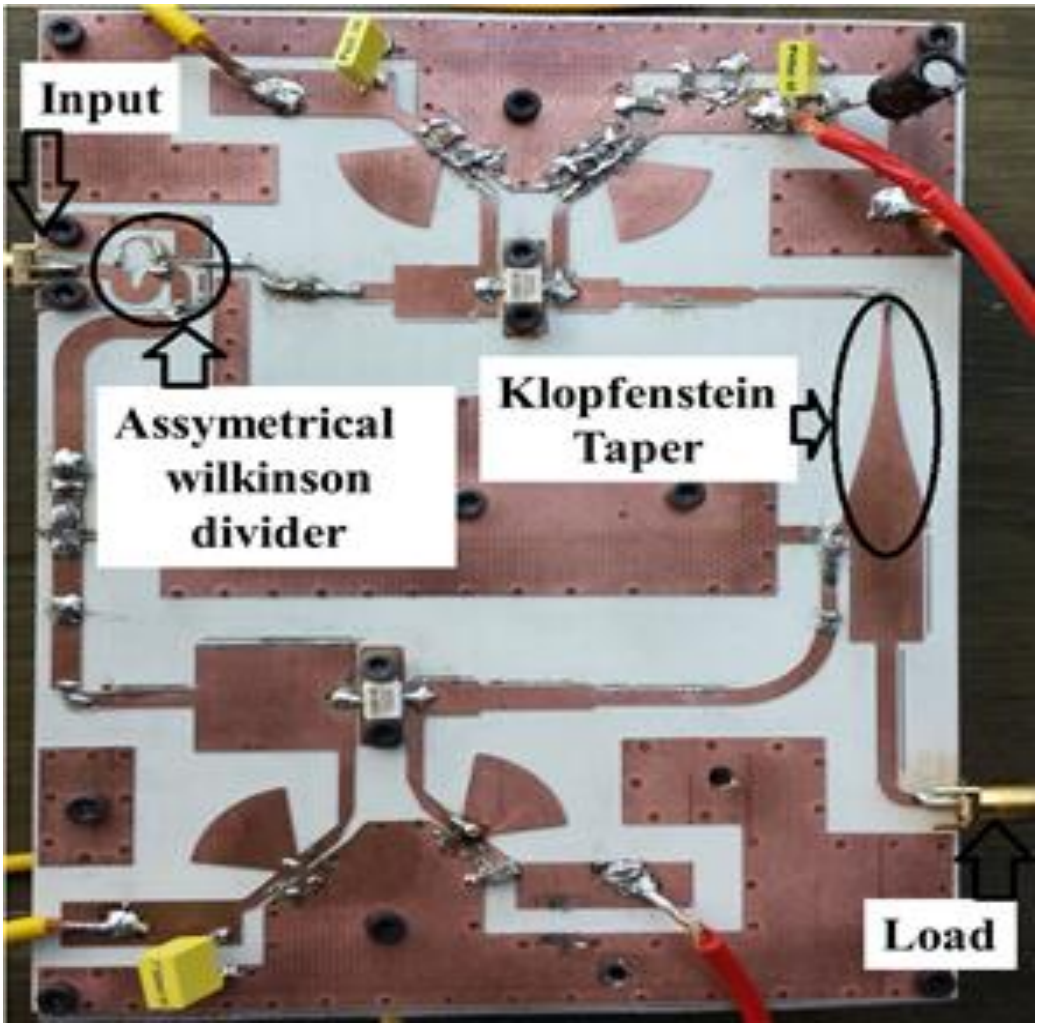


Figure 4.12 Photograph of the implemented Doherty-like PA

4.3 Experimental results

To assess the bandwidth performance of implemented DPA, the scattering parameters of proposed DPA and conventional DPA are compared. As depicted in Fig 4.13, the scattering parameters of the proposed DPA indicate a bandwidth operation from 1.7 GHz to 2.75 GHz (47

% of fractional bandwidth). Furthermore, considering the S-parameters of conventional DPA, it can be seen a frequency band from 1.85 to 2.6 GHz. By comparing these two DPAs, a 14% increasing in the bandwidth of proposed DPA is visible. It can be caused to adequate adjusting the group delays between two paths.

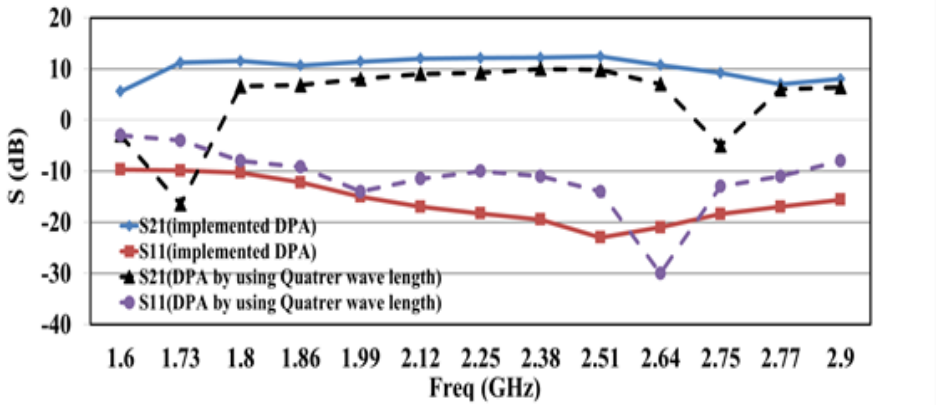


Figure 4.13 Measured S-parameters of the proposed amplifier, compared with a conventional DPA (some schematic, but with the classical λ/4 transformer)

To evaluate the efficiency enhancement and gain power at the back-off power levels, the drain efficiency versus output power was measured at different frequencies. The power gain and the drain efficiency versus output power for 3 selected frequencies along the operating band (1.7 GHz, 2.25 GHz and 2.75 GHz) are presented in Fig 4.14. Drain efficiency (DE) ranges from 37% to 48% in a 6 dB of OBO operation. DE at saturated output power ranges from 43% at 2.75 GHz to 54% at 2.25 GHz.

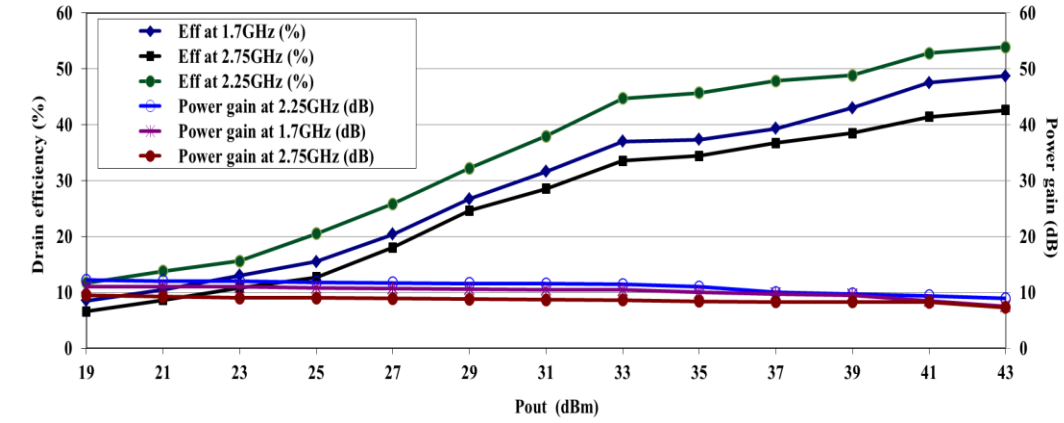


Figure 4.14 Measured drain efficiency and power gain versus output power (Pout)

Figure 4.15 illustrates the power efficiency and output power measurements versus frequency at peak and OBO power level. They have been carried out at input power levels of 26 dBm (6 dB OBO) and 32 dBm (saturated output power). As it can be seen in Fig 4.15, the maximum power level is reported about 42 dB in whole of frequency band (1.7 to 2.75GHz). Besides, the variation of efficiency in peak power level is shown from 43% to 54%. These results have been verified the previous results in Fig 4.14.

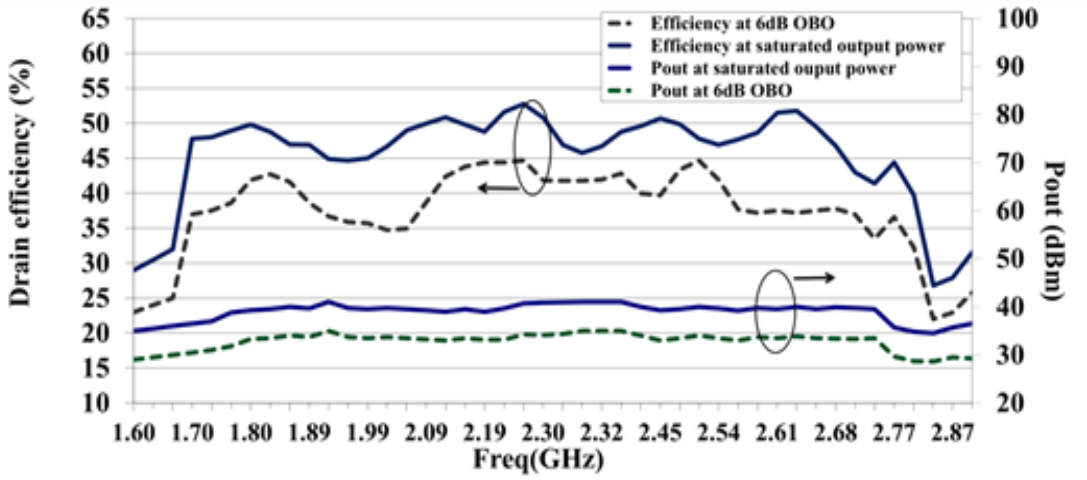
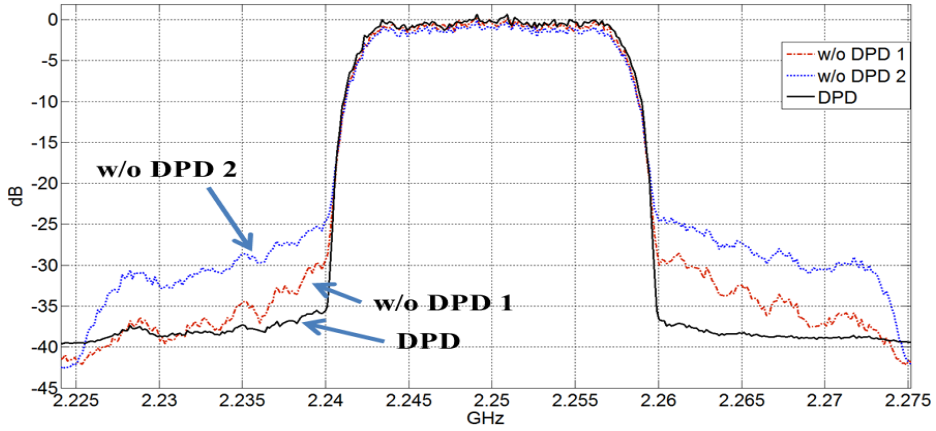


Figure 4.15 Measured power out and DE (at 6 dB OBO and at saturated power)

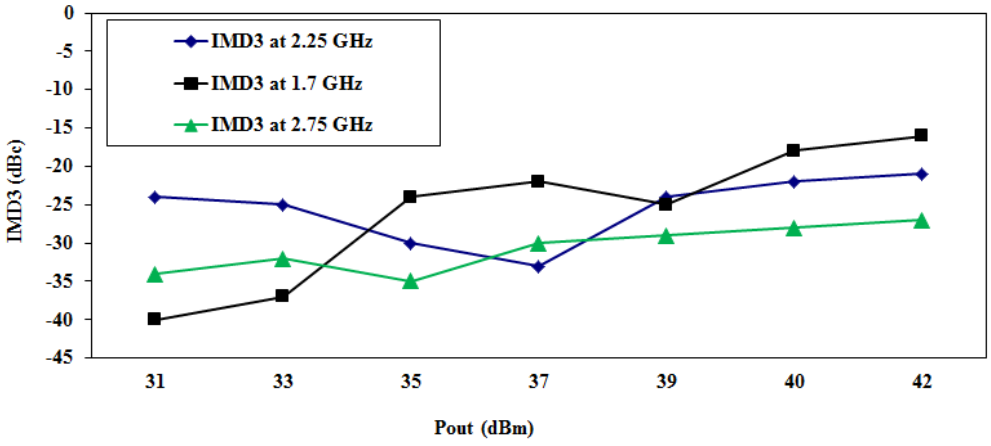
To assess the linearizability needs of the broadband implemented DPA at different frequencies, the third-order inter-modulation distortion (IMD3) for different power levels of the proposed DPA is depicted in Fig 4.16b. These IMD3 measurements, showing the usual order of magnitude in other DPAs, have been made by using two-tone signals with 1MHz frequency offset, around three different frequencies of 1.7 GHz, 2.25 GHz and 2.75 GHz. In the center frequency of 2.25 GHz, the IMD3 figure ranges from -25 dBc to -35 dBc in the Doherty region. From the two-tone tests, no relevant memory effects have been detected (i.e., no visible IMD asymmetry) for tone separations up to 200 MHz (approximately, 20% of the BW) (see Fig 4.17). The two-tone test measurement has been done by using a 30 dB attenuator between the output of DPA-like and input of the spectrum analyzer in order to prevent the spectrum analyzer damage at maximum power output level.

Besides, with a HSPA+ expanded to 20 MHz (Release 10) the ACPR results of 34.2 dB

(at 9 dB OBO) and 27 dB (at 6 dB OBO) (see Fig 4.16a). Considering these measurements can be resulted the linearization of implemented DPA is the weak point of this implementation, even though DPAs are not usually a linear PA. Therefore, in order to modify the linearization of implemented DPA can utilize a DPD. By using a DPD, these figures may be typically improved by 10 - 15 dB as shown in Fig 4.16a. For the HSPA+ modulation (centered at 2.25 GHz) the resulting average efficiency is 47.2 %. In Table 4.1, the performance of the fabricated wideband DPA has compared with some previous works.



(a)



(b)

Figure 4.16 (a) output spectrum with a 20-MHz WCDMA (HSPA+ expanded, release 10) driving signal, at center frequency of 2.25 GHz and average output power of 33 dBm (w/o DPD1) and 36 dBm (w/o DPD2). Common benefits to apply a memory polynomial DPD (ACPR increased in 10-15 dB) are indicated in the figure and (b) IMD3 measured at 3 different frequencies

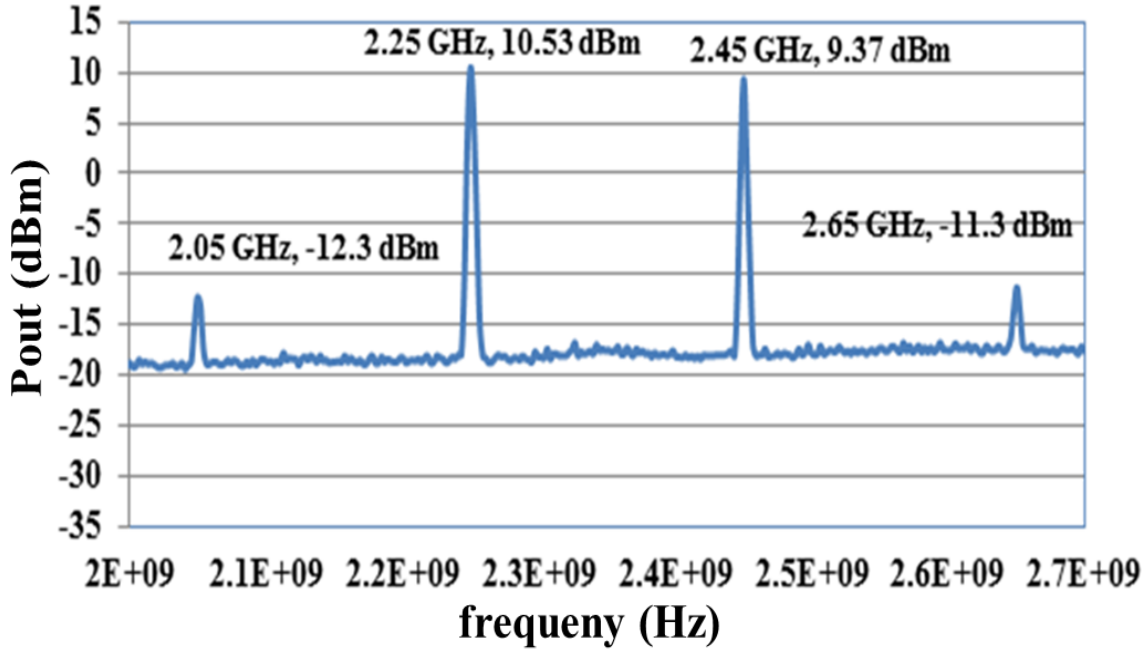


Figure 4.17 Two-tone test measurements

Table 4.1 Comparison the implemented DPA-like with other wideband DPAs

	Freq. (GHz)	BW (%)	DE (%)	Gain (dB)	Max. Pout (dBm)	IMD3 @ SAT dBc
[124]	1.7 - 2.4	36.3	43 - 59 (6 dB OBO) 53 – 72 (@ SAT)	9.4 - 10	42	-
[116]	1.5 – 2.5	50	> 49 (6 dB OBO and SAT)	4.2 - 11	42	-
[126]	1.05 – 2.55	83.3	35 - 58 (6 dB OBO) 45 – 83 (@ SAT)	9 – 12.5	40 - 42	-
[118]	6.8 – 8.5	22	39 - 42 (6 dB OBO) 45 – 55 (@ SAT)	6 - 13.5	35	-
[120]	1.96– 2.46	23	> 40 (6 dB OBO)	7 – 15	40 – 41	14
[113]	0.8 - 1.2	40	30.3 - 40.1 (6 dB OBO) 50.8 - 78.5 @ SAT	10.8 - 14.8	40.2 - 42.9	16
[107]	0.7 - 1	35.3	50 - 60.6 (6 dB OBO) 65 - 67.3 @ SAT	14.5 - 23.5	49.9	-
TW	1.7 - 2.75	47	37 - 48 (6 dB OBO) 43 – 54 (@ SAT)	8.5 - 11	42	18

As reported in Table. 4.1, the bandwidth of proposed DPA-like is close to other recent works. Reported drain efficiencies at OBO and saturated output power level evidence the reasonable efficiency values of the implemented DPA in this thesis. The maximum output power in all the DPAs are close together. Also the IMD3 performance of the implemented DPA at saturation power is 3dB better.

In summary, a novel architecture for a wideband DPA-like has been presented in this chapter of the thesis. This architecture is based on the replacement of the classical quarter-wave impedance inverter by a hybrid network, including a Klopfenstein taper which facilitates the adjustment of the group delay. According to the results concerning the peak output power, the drain efficiency, the bandwidth and the linearity performance, the resulting DPA-like shows similar figures compared with alternative solutions recently presented, with the merit of showing a straightforward design adjustment. Due to the obtained results in simulations and measurements, the frequency bandwidth in the proposed DPA is from 1.7 to 2.75 GHz for the 2.25 GHz center frequency. Moreover, the fabricated DPA-like presents a 47% of fractional bandwidth, with a drain efficiency, higher than 43% at saturated output power.

Chapter 5

Conclusions and proposals for the future works

5 Conclusions and proposals for the future works

5.1 Conclusions

This study focused on developing fractional bandwidth of DPAs using the new methods that are related to impedance transformer in load modulation technique. In this context, the key objective was to fabricate a novel DPA using 15 W, 2.7 GHz, GaN HEMT transistors. The quarter-wave transformer used in the classical DPA topology is replaced by a matching network, including a Klopfenstein taper that, apart from the increased BW, allows a direct control of the susceptance of output peaking path by adjusting the length of the applied taper. Moreover, the implemented design led an easy tuning of the group delay through the output reactance of taper, resulting in a more straightforward adjustments than other recently-published designs where the quarter-wave transformer was replaced by multi-section transmission lines.

5.2 Future works

This thesis could have further modifications; in the following there are the some suggested improvements:

- The proposed biasing network may be perhaps broadened using circuital alternatives, and also considering their effects on the intermodulation products, i.e, to assess the benefits of using choke inductors in the resulting BW and in the generation of IMD products.
- Using an adaptive bias technique in order to adjust the bias point of main and peaking amplifiers.
- The additional use of a DPD is recommended for commercial exploitation to meet stringent ACPR requirements in some new communication standards.

Acknowledgment

I want to thank the people that made this work possible:

My supervisor Prof. Eduard Bertran for their guidance, inspiration and support. This work would not have been possible without you.

My dear friends and fellow colleagues at UPC for making it fun to go to work and for helping me now and then.

Dedicated to my mom and father.

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