

#### 4.2.3.3.3 *Implantation procedure*

Right before implantation a final test of functionality of both internal and external unit was performed. The animal experiments were carried out at the Experimental Surgery Unit of the Fundacion Cardio-infantil Instituto de Cardiologia in Bogota, Colombia, with the PhD candidate present<sup>5</sup>. Experimental subjects were adult dogs, weighing 12-15 Kg. The experimental protocol was reviewed and approved by the “comité de etica de experimentacion animal” a committee for ethical evaluation in order to comply with the standards of the National Institutes of Health “Guide for the Care and Use of Laboratory Animals” (NIH Publication N0.86-23, revised 1985). The animals were being subjected to normovolemic hemodilution to a target hematocrit of 15%. A week before to the experiment, the animals underwent to surgical splenectomy through an abdominal incision in order to avoid sequestration of erythrocytes in the spleen. Anesthesia was induced intravenously with thiopental (10-15mg/Kg), and pancuronium (0.1-0.3 mg/Kg), and maintained by inhalation of isoflurane (0.5-2.5%) in oxygen. The animals were intubated and ventilated with 100% oxygen.

The left femoral artery was cannulated using an 18-gage catheter. A Swan-Ganz catheter access guide was inserted through the arterial access. The intravascular pressure transducer (IPT) catheter was introduced through one of the guide ports. The other port was used to place a dome-type of the Mikro-tip catheter and Mean Arterial Pressure (MAP) was monitored through the dome-type transducer. Left Ventricular Pressure (LVP) was recorded in a PC. The right and left external jugular veins were cannulated using a 18-gage catheter. In the right jugular vein, a Swan-Ganz catheter was placed to monitor cardiac output. Through the left jugular access, 20% of volemia was extracted. The same volume of PFC-OC Oxyfluor™ (40% vol/vol, HemaGen/PFC, St. Louis, MO, USA) was reinfused. Blood extraction and volume replacement are repeated by the same

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<sup>5</sup> Thanks to a short-term grant “borsa de viatge” Generalitat de Catalunya

amount until hematocrit reaches 15%. Samples of arterial and mixed venous blood were taken after each replacement. These samples were analyzed for complete blood gasimetry and hematology using a gas analyzer and a Coulter counter respectively. In addition, MAP, LVP, central venous pressure (CVP) and heart rate are monitored every 5 minutes during the procedure.

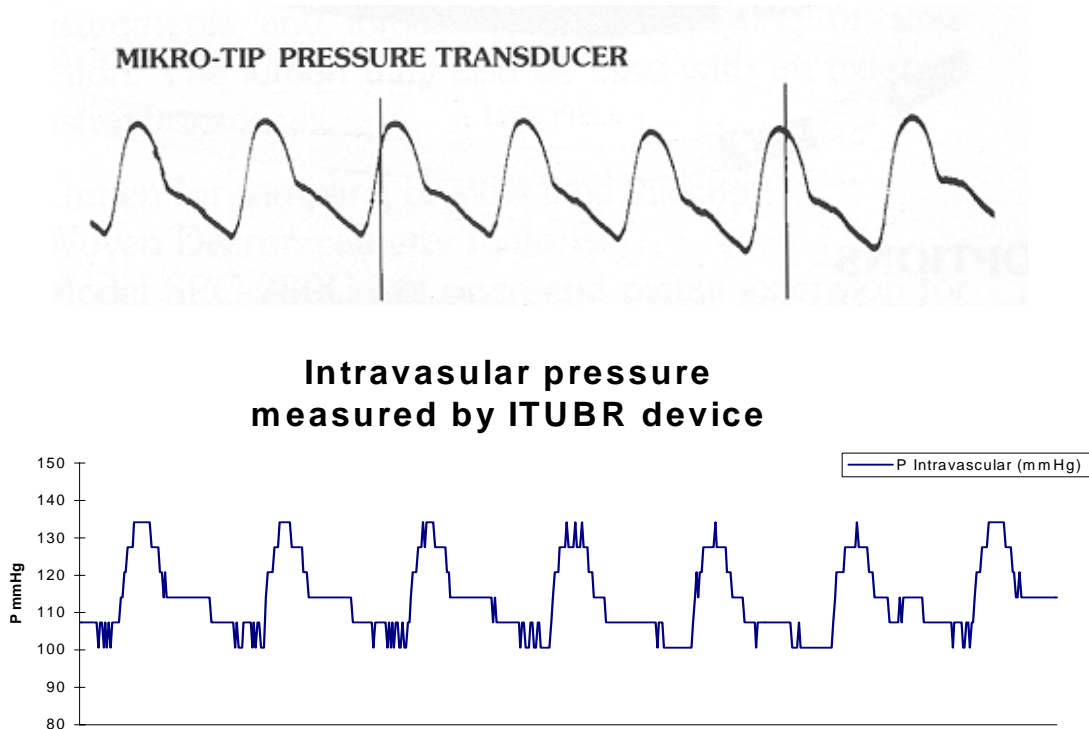
Once the normovolemic hemodilution was finished, the ITUBR device was subcutaneously implanted in the abdominal area and held by sutures to the endodermis. The intravascular pressure transducer was connected to the device and the telemetry was tested. The abdominal incision was sewn up and the telemetric monitoring of LVP was started placing the external telemetric unit over the skin of the animal in the same area where the implant was placed.

#### 4.2.3.3.4 *“In-vivo” recordings*

Once finished the implantation procedure, “in-vivo” recordings were performed. Before implantation measurements of the atmospheric pressure were done with the device to set the baseline of the arterial pressure. The pressure sensor sensitivity was 5uV/V/mmHg. The system used 5V as the sensor supply hence the sensitivity was of 25uV/mmHg. Once the atmospheric pressure reference was stored in memory we were ready for in-vivo recordings. After the procedure explained in previous section the telemetry device started to transmit to the external unit data. The digital data was processed and stored in a file. Also we were able to display the data in real time in the screen of a computer.

An initial visual inspection of the waveform in the screen by the doctors confirmed that effectively the implant was recording and sending through wireless a typical arterial pressure signal. At the same time all information was stored in a disc. Figure 4-18 shows one of the recorded blood pressure signals with a fully implanted device being powered by RF. In the upper side there is a typical arterial pressure signal provided by the sensor manufacturer. In the lower side we see the data recorded and

wireless transmitted by the implanted device. The data was processed in the external unit as follows: (1) converting back to analog following the inverse of the implant A/D transfer function. (2) Calculating the real analog input dividing by the implant amplifier gain. (3) Converting the voltage to pressure (in mmHg) following the sensitivity of the sensor. (4) Finally calibrating the value related to the previously measured atmospheric pressure.



*Figure 4-18. Signal recorded and telemetered by the ITUBR device versus expected arterial pressure waveform provided by the sensor manufacturer (Millar)*

We can see a fairly similar waveform pattern between both the expected signal and the actual recording. A clear difference is the resolution of the signal. The overall pressure ranges that the device is capable of sensing, goes from  $-349\text{mmHg}$  to  $+322\text{mmHg}$ . The 8-bit converter provides a resolution of  $6.7\text{mmHg}$ . For this particular application we see a large DC offset of about  $115\text{mmHg}$  (that is relevant and cannot be canceled) with an AC signal swing around  $40\text{mmHg}$  providing a poor waveform resolution. So, even though the signal processing capabilities are certainly subject to improvement (if higher resolution were desirable), the result certainly proves that we

were capable with the implanted batteryless and wireless device of recording in-vivo data resulting in comprehensive and clearly identifiable arterial pressure signals.

### **4.3 CHEMICAL SENSOR-MARID DEMONSTRATOR**

Chemical sensors are major players in the development of implantable instrumentation. The following section describes the work done by the PhD candidate aiming to obtain an implantable wireless battery-powered device capable of monitoring some chemical parameters (in particular we show a ISE sensor). As opposed to the ITUBR device exposed in profusion earlier where a complete development cycle was performed, the MARID (**MA**ssive **R**ecording **I**mplantable **D**evice) demonstrator goes only from system design to board level prototyping (with two custom ASICs), including in-vitro measurements. It is important to note that even though system level integration was not performed the results were encouraging enough to be use as a proof of concept (demonstrator) of the novel concepts introduced.

#### **4.3.1 Introduction**

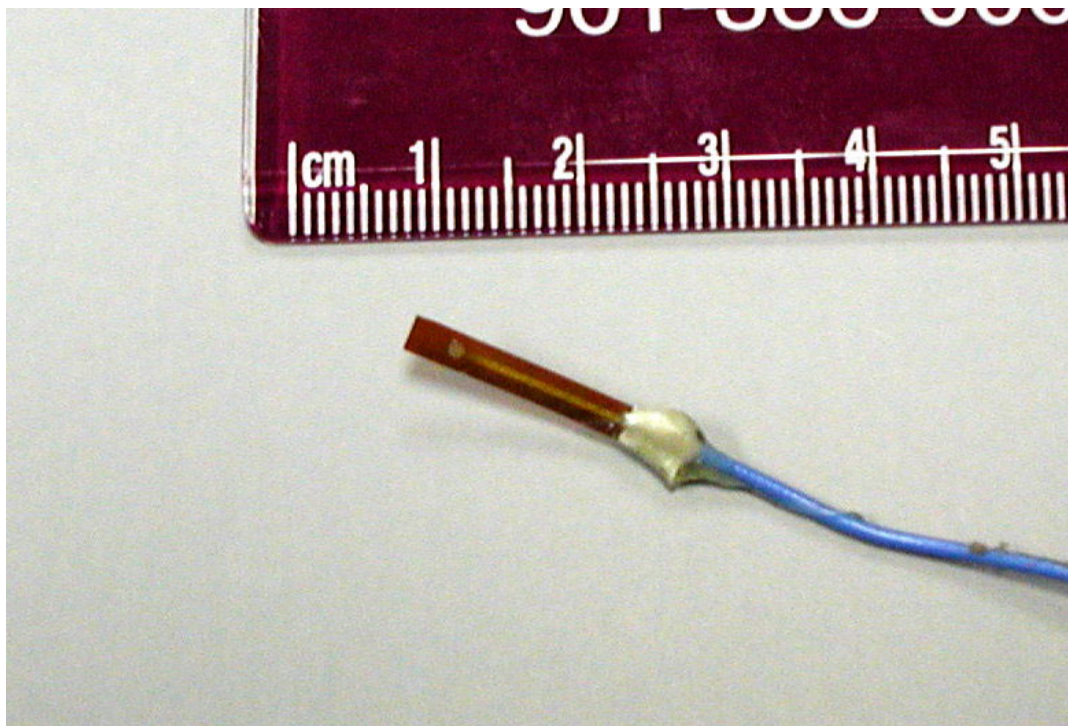
##### ***4.3.1.1 ISE sensors Complete system assembly***

During the past several years, practical micro-sensor devices have entered the fields of biology and medicine and are beginning to drive discoveries in cell biology, neurobiology, pharmacology, and tissue engineering. The integration of micro-fabricated sensors, liquid handling, and biochemical-processing devices with separation systems has led to complete chemical analysis systems on the surfaces of planar devices. However, these “lab-on-a-chip” devices are envisioned primarily for in vitro, high-throughput screening<sup>[3][4]</sup>.

Ion-selective electrodes (ISE) are chemical sensors that respond to the activity (concentration) of a single ion in the presence of others with the same charge sign. Ion-selective potentiometry is a routine analytical technique for both in vivo and in vitro

analysis, in which the cell voltage is measured as a function of the sample's solution activity. The essential part of an ISE is the ion-sensitive membrane that is commonly placed between two aqueous phases—for example, the sample and the inner electrolyte solution. Ion-selective membranes made from glass, single crystals (e.g.,  $\text{LaF}_3$ ), pressed pellets of insoluble precipitates (e.g.,  $\text{AgCl}$ ,  $\text{AgBr}$ ,  $\text{AgI}$ ), or solvent polymeric membranes (highly plasticized polymeric films, also known as liquid membranes) are widely used in analytical practice.

Most of the micro-fabricated ion sensors are based on solvent polymeric or liquid membranes. Over-plasticized poly(vinyl chloride) (PVC) is most frequently used as the membrane matrix. The selectivity of these membranes is determined by the dielectric properties of the plasticizer and the selective, hydrophobic complexing agents, which are neutral or charged carriers (ionophores), within the membrane phase <sup>[5]</sup>. Figure 4-19 shows an ISE sensor developed at the University of Memphis and the University of Tennessee–Memphis <sup>[6]</sup> and used in the “in-vitro” testing validation of the system here presented.



*Figure 4-19. Potassium ( $\text{K}^+$ ) ion-selective electrode sensor*

Calibrating ISEs by serial dilution gives a plot of the cell voltage as a function of the logarithm of the primary ion activity. It is linear over a wide concentration range (generally from  $10^{-1}$  to  $10^{-6}$  M) with a  $59 \text{ mV}/z_i$  slope at  $25 \text{ }^\circ\text{C}$ . In the linear (Nernstian) response range of the membrane, the composition is constant <sup>[7]</sup>. There are no concentration gradients in the membrane, and the concentration of negatively charged sites is matched with positively charged complexes of the ionophore, which sustains electroneutrality in the membrane bulk. Outside the Nernstian response range, the membrane composition changes with the composition of the sample solution. At very low ( $10^{-6}$  M) or very high ( $10^{-1}$  M) sample concentrations, time-dependent concentration gradients develop within the membrane. Interference-induced cross fluxes and steady-state salt co-extraction are examples of ion transport throughout the membrane and ion leakage into the aqueous solution. Reduced slopes, slow drifts, and higher detection limits accompany ion-transport-related changes in the membrane bulk and in the adjoining aqueous solution.

#### ***4.3.1.2 Technical specifications***

The MARID implant was conceived as a miniature electronic device with the capability of interfacing with a variety of chemical sensors requiring large input impedance. The device will also have a build-in capability of storing massive information with a quick wireless Uplink download when requested by the external reader.

In summary the system is being conceived as a signal recording instrumentation device with the following features:

- Embedded large memory
- Wireless programming and data download
- Programmable analog front-end
- Large versatility (Micro-controller based system)
- Long implant lifetime

Table 4-2 shows the sensor interface specifications.

Table 4-2. ISE sensor/analog front-end specifications

Feature	Value
Sampling rate	1 sample / second
Number of Sensors	4
Signal level	High impedance $\pm 25\text{mV}$
Offsetting correction	$\pm 100\text{mV}$
Bandwidth	dc-LPF (depending on external capacitor)
AD resolution	8bits
Recording time	8 hours
Implant lifetime	> 1 year
Battery specs	10mm diameter/3V/30mAh capacity
Download time	10-20 seconds
Telemetry range	1 inch

### 4.3.2 System design and development

#### 4.3.2.1 Functional description

From a behavioral perspective the device shall be capable of: (1) interfacing with a number of sensors (front-end), (2) store the recorded data in an embedded memory, (3) provide data downloads when required by an external reader and all this performed with (4) an intelligent power management. Functionally the implant can be described as follows in the figure 4-20:

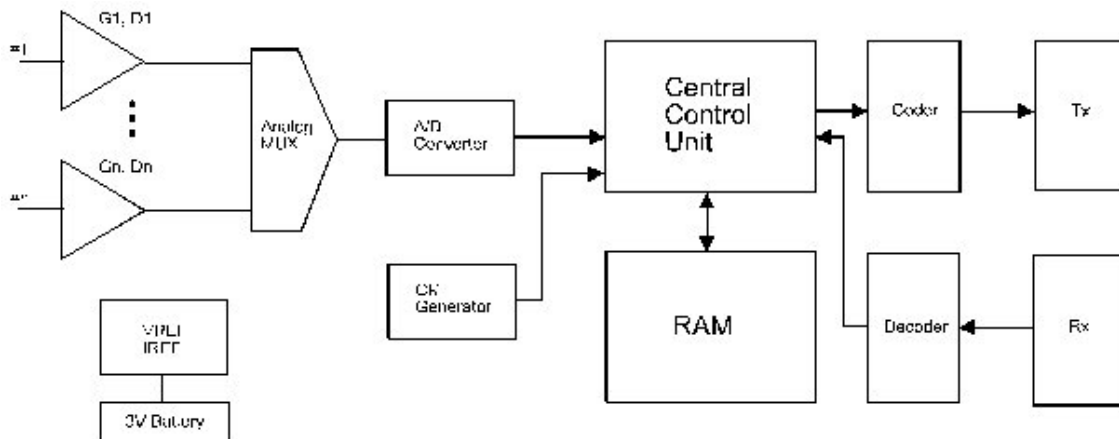


Figure 4-20. Functional block diagram of the implant

Four operating modes are requested for the device to perform according to specifications:

*Sleeping mode:* Just the switched-power RF detector will be waked-up (very low consumption), waiting for an external demand of operation. About 1uA of current consumption is achieved (see 3.2.1.2) with the proposed receiver scheme. What gives approximately 3.5 years of life for a 30mAh battery in this state (very important for shipping and other practical uses).

*Listening mode:* Through an inductive link, an external device programs the implant in order to send the system to (1) a recording mode, (2) a download mode or (3) a sleeping mode.

*Recording mode:* Analog front-end plus the AD converter are enabled. Sampling, conversion and data storage to a RAM memory is performed at a certain programmable time-rate. Once performed the recording, the system will go to sleep mode just preserving the RAM memory.

*Downloading mode:* Through an inductive link, the implant transmit to an external device (reader) the data stored in a RAM during the recording mode. Once the data transfer is complete the system will go automatically to the sleeping mode.

The actual system behavior is illustrated in the figure 4-21:



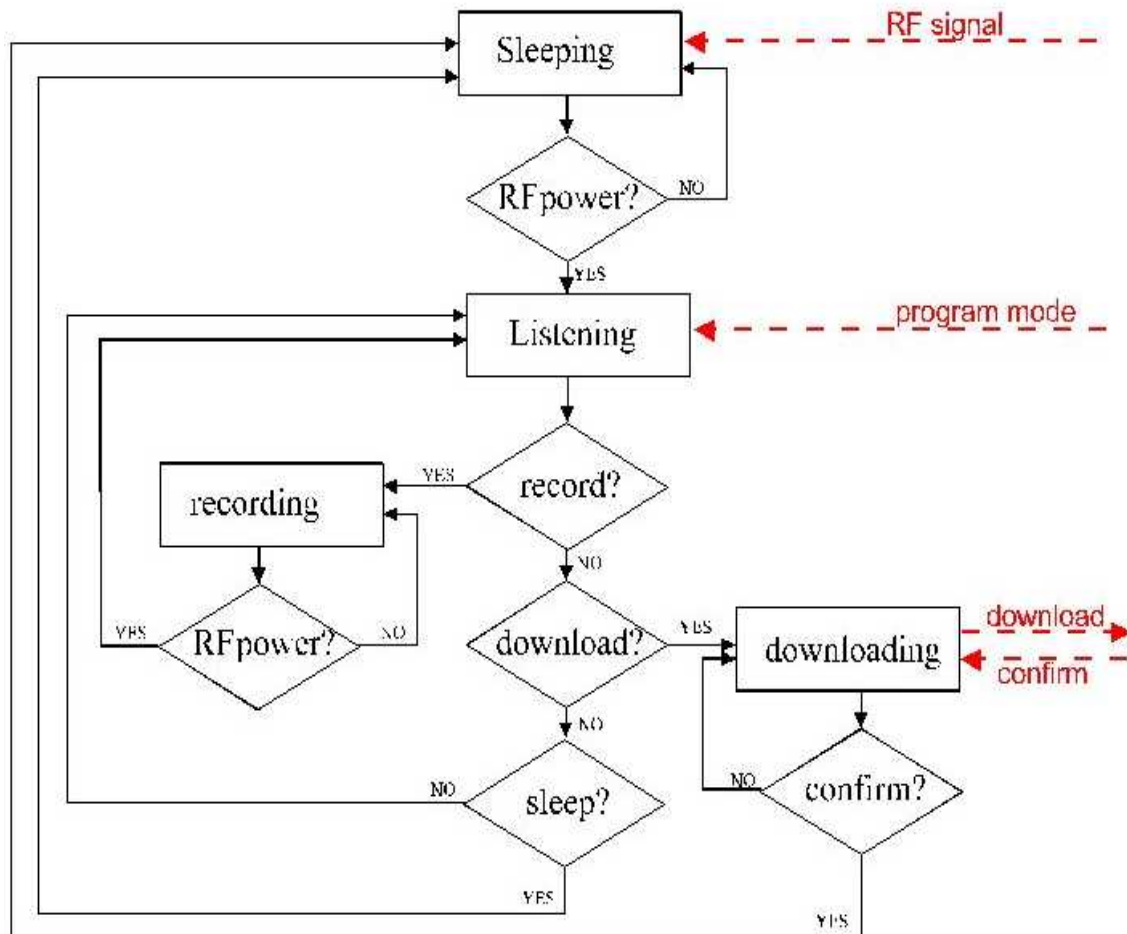


Figure 4-21. MARID behavioral diagram

#### 4.3.2.2 Architecture

The system implementation of the functional description provided above uses two commercial IC (memory chip and PIC micro-controller) and a custom ASIC. The only additional component is a single coil. Figure 4-22 shows the way the design has been divided from an architectural perspective:

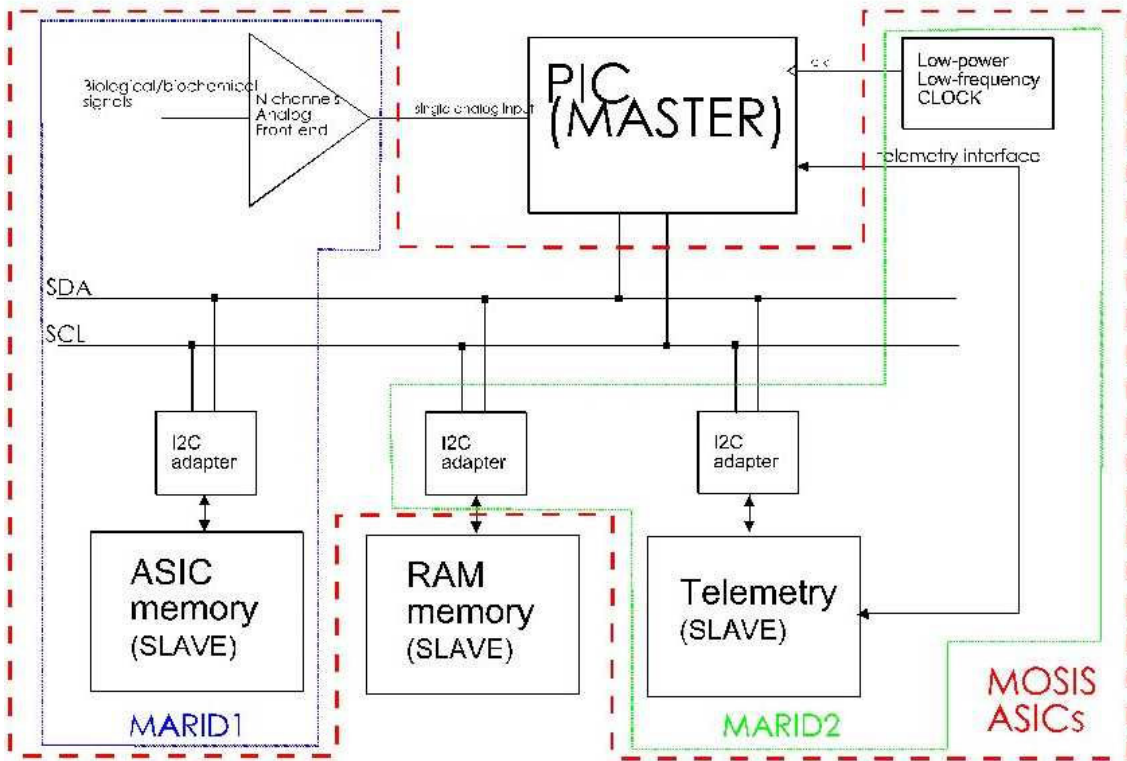


Figure 4-22. MARID architecture

One of the key elements of this architecture is its high level of flexibility. As opposed to what was presented within the ITUBR device where a rigid state machine was the master control of the system, in here a stand-alone micro-controller (PIC16C72 from microchip, which is a high performance and low power 8-bit RISC processor) executes the control. In addition to that, the interface between the Master controller and the rest of peripherals (like sensor front-end, telemetry or memory) is implemented using the Philips standard I2C bus. So expandability is a build-in feature of this architecture. The custom ASIC part (inside the dashed red line) was in reality implemented with two chips. The reason (in this phase of prototyping) was the fact the ASICs were fabricated using the

Tiny-chip MOSIS<sup>6</sup> program where die size was very limited. More details in next section. With this architecture the two custom chips were separated as shown in Figure 4-22.

The MARID1 chip (blue box) contained four offset calibratable self-biased analog amplifiers with programmable gain ranging from 20 to 40 dB. Internal registers set all the parameters. An I2C interface was also included to allow standard control by the controller. The AD conversion was implemented in the micro-controller chip because the PIC16C72 included a built-in analog interface with an 8-bit AD converter.

The MARID2 chip (green box) contained a low-power low-frequency oscillator (feeding the clock to the controller), a dedicated I2C adapter to interface a standard memory chip with the bus and the telemetry circuits described in chapter 3, including the ultra-low power low bandwidth receiver and the high bandwidth BPSK transmitter.

The rest of the components are a memory chip (SRAM), a primary 3.0V/30mAh coin battery and a flat coil. With no additional components. So even though the system design is highly flexible and modular, miniaturization and low power can be achieved with this architecture. Moreover, using one of the characteristics of the I2C interface, (open collector data line) the modules could potentially have different supplies if required.

#### ***4.3.2.3 ASIC design***

As mentioned above, two custom ASICs where designed to full-fill the architecture requirements. The telemetry section has already been presented earlier in

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<sup>6</sup> Equivalent in the USA to the Europractice program where low cost silicon is offered through a MPW service

chapter three. In this section will be presented the remaining IC design performed by the candidate.

#### 4.3.2.3.1 MARIDI IC design

The first chip is the analog interface to the chemical sensors. In total four channels were implemented, with gain and offset controllable through the I2C port by the micro-controller.

##### 4.3.2.3.1.1. Analog Front-end sensor

Major considerations of the recording channels were (1) a very high input impedance, (2) a differential input, (3) a programmable gain, (4) a power-down capability, (5) an offset control per channel and (6) reasonable values of consumption (no need to go to ultra-power design).

So the final topology chosen is a 3-OpAmp-based Instrumentation Amplifier (IA) with a further inverter-second stage gain as showed in figure 4-23:

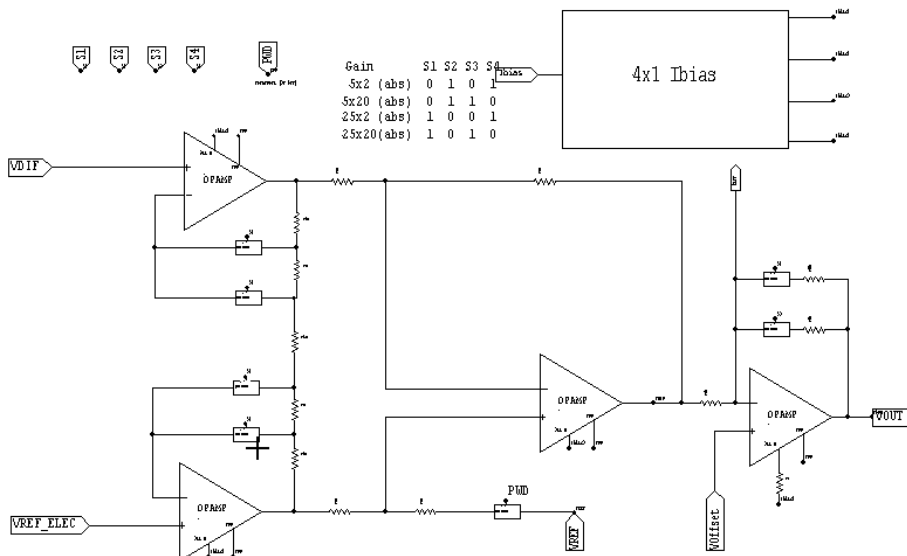


Figure 4-23. Programmable Instrumentation Amplifier schematic

Very high Input impedance is assured due to the topology (ideally infinite) with a extremely high input impedance in the CMOS gates (in the order of fA of leakage currents).

First stage gain is programmable changing the ratio of resistors using CMOS switches. A unity-gain second stage allows a best control of common-mode, avoiding unbalanced signals. Third stage provides a late gain control, again changing the ratio of resistors in a typical inverter configuration of an OpAmp which is used at the same time for an offset control (driving the positive input of the OpAmp) and also as a first order low-pass filter with a time constant variable with an external bonded capacitor if needed.

Post-Layout AC simulations with 3V supply voltage and 5uA bias current produced the following results:

*Table 4-3. Instrumentation Amplifier post-layout corner simulation results*

5X2 program <sup>[S1=0, S2=1, S3=0, S4=1]</sup>			
	<i>BSIM3v3 TYP</i>	<i>BSIM3v3 WCP</i>	<i>BSIM3v3 WCS</i>
Overall Gain (dB)	23.16	21.41	28.75
FC @ 0f CLPF	140kHz	211kHz	95kHz
FC @ 1n CLPF	9.4kHz	11.6kHz	4.8kHz

25X2 program <sup>[S1=1, S2=0, S3=0, S4=1]</sup>			
	<i>BSIM3v3 TYP</i>	<i>BSIM3v3 WCP</i>	<i>BSIM3v3 WCS</i>
Overall Gain (dB)	37.08	35.35	42.65
FC @ 0f CLPF	50kHz	65kHz	39kHz
FC @ 1n CLPF	10.8kHz	10.9kHz	4.6kHz

5X20 program <sup>[S1=0, S2=1, S3=1, S4=0]</sup>			
	<i>BSIM3v3 TYP</i>	<i>BSIM3v3 WCP</i>	<i>BSIM3v3 WCS</i>
Overall Gain (dB)	40.35	40.13	41.42
FC @ 0f CLPF	48kHz	74kHz	34kHz
FC @ 1n CLPF	1.3kHz	1.3kHz	1.1kHz

25X20 program <sup>[S1=1, S2=0, S3=1, S4=0]</sup>			
	<i>BSIM3v3 TYP</i>	<i>BSIM3v3 WCP</i>	<i>BSIM3v3 WCS</i>
Overall Gain (dB)	56.26	54.06	55.31
FC @ 0f CLPF	29kHz	44kHz	23kHz
FC @ 1n CLPF	1.3kHz	1.3kHz	1.1kHz

Voltage supplies swings from 2.7V to 3.3V showed slight effect on main amplifier parameters. It has been observed some small gain variations and some biasing

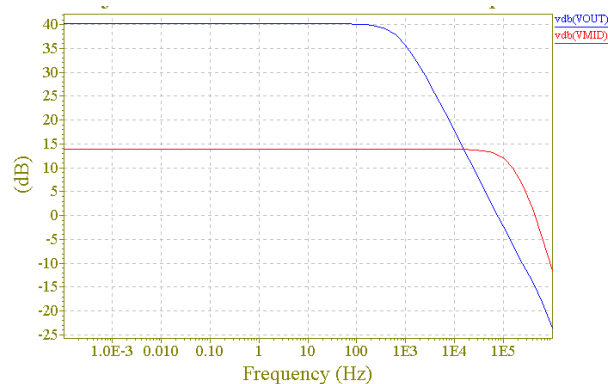
drift, but none of these effects may have any functional consequence and are totally normal. Due to the topology used (three transistors per branch as maximum) amplification behavior can be achieved near 2V of supply. Minimum theoretical rail-to-rail voltage would be about  $2xV_{thN} + V_{thP}$  what is close to 2V in the AMI 1.2u technology.

The rejection to common mode (ratio between differential and common mode gain named as CMRR) simulation results with BSIM3v3 are presented in table 4-4:

*Table 4-4. Gain and CMRR on Instrumentation Amplifier*

<b>Gain Program</b>	<b>Differential Mode Gain</b>	<b>Common Mode Gain</b>	<b>IA CMRR</b>
5x2	23.16dB	-51.90dB	75.06dB
25x2	37.08dB	-54.80dB	91.88dB
5x20	40.35dB	-56.03dB	96.38dB
25x20	54.26dB	-48.51dB	102.77dB

Figure 4-24 shows an AC analysis of an amplifier with 5x20 selected gain. The first stage gain is about 14dB (5 in absolute value) and the overall gain is about 40dB (100 in absolute value). Low Pass Filter cutting frequency can be controlled with the value of the external capacitor CLPFX.

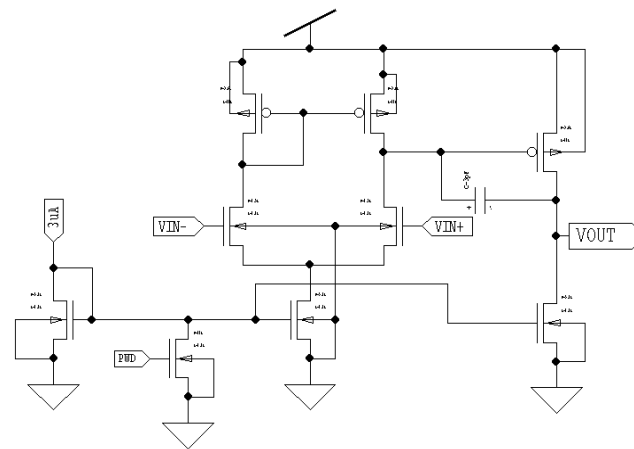


*Figure 4-24. IA Post-layout AC simulation waveform for a 5x20 selected gain*

The current consumption depends on the current reference applied. Nominally through the design a  $4x(11xI_{bias})$  sets the power consumption of the overall recording channel.

Related to the input impedance, the IA configuration assures a virtual infinite dc input impedance. Obviously this is not the case in reality. Through simulations the impedance model is basically the impedance model of a MOS transistor which is a capacitor with a very high parallel resistance (above  $1e15$ ). Once simulated the ac impedance is:  $1/(73fF \omega)$ . So about  $2.17G\Omega$  at 1kHz and  $217 G\Omega$  at 10Hz. The dc impedance was above  $1e+15$ .

The custom OpAmp was a Miller OTA with a compensation capacitance to achieve reasonably good phase margins. Next a schematic of the OpAmp:



*Figure 4-25. OpAmp Schematic*

The requirements of this application were not critical in bandwidth or gain, so a moderate GBW was enough. Main concern was due to the bias current tolerance of the OTA, thus a 3uA to 8uA current range was mandatory. Final transistor geometry and miller capacitance values were found out meeting a GBW near 500kHz with a good 99° phase margin (thus avoiding undesirable stability problems). Power Supply Rejection Ratio (PSRR) was found to be about 72dB and the Input Offset 1.3mV.

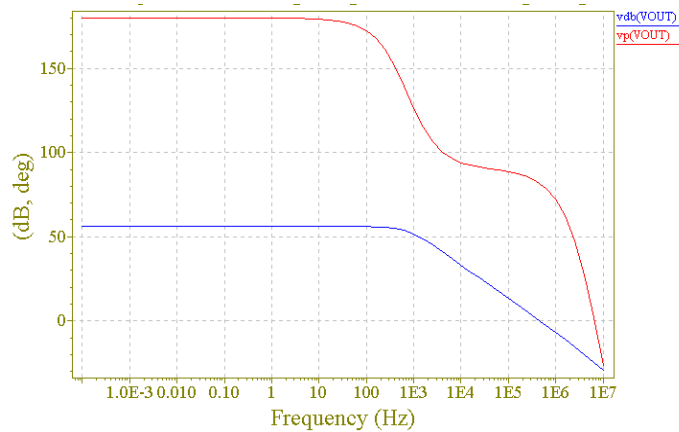


Figure 4-26. OpAmp AC simulation

In order to avoid channel modulation effects, a minimum channel length for transistors operating in saturation mode was never used. Additionally, a NMOS switch was added to provide a power-down performance when requested. First to second stage gain was fixed in 10, thus the overall OpAmp current consumption will be 10+1 times the biasing current.

#### 4.3.2.3.1.1 House keeping staff

Additional analog circuits necessary to provide functionality to the four instrumentation amplifiers were a PTAT current reference, a linear voltage regulator and a delay-based power-on reset.

#### 4.3.2.3.1.2 I2C interface and register bank

The logic design requirements for this chip were mainly to implement a bank of registers to keep the setting parameters for the four IA as well as an I2C interface between these registers and the system bus. A Semi-custom approach was used to implement the logic. Thus a standard-cell-based design using a schematic level development (no need to go to upper abstraction levels as description languages) was done. The logic simulator was *Gatesim*.



One of the main features of the MARID1 ASIC is that provides a I2C bus compatible programmability of the recording electronics. Thus a I2C interface was designed. Basically there is a decoding circuit to detect start and stop signals and moreover additional logic to receive and store in a shift register the data coming from the master. A knowledge pulse provided every 8 input bits is also generated. Once the MARID1 memory is full-filled the master ends the communication.

Figure 4-27 shows a sequence of programming the MARID1 through the I2C bus:

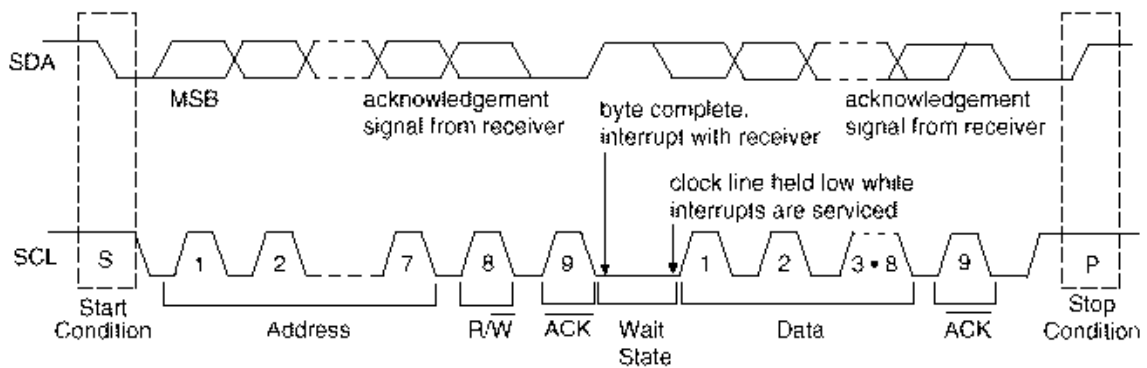


Figure 4-27. MARID1 programming through I2C bus

In the MARID1 both SDA and SCL are just inputs (the module is only for writing). In order to decode properly the information the ASIC needs an additional clock line (named 2CLK) that must be synchronous with the negative edge of SCL and twice the frequency of SCL as shown in figure 4-28:

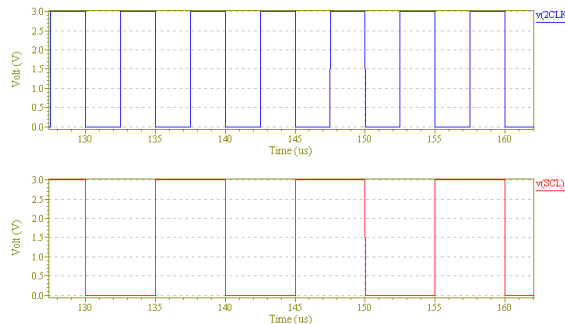


Figure 4-28. SCL (100kHz) vs 2CLK waveform

In the I2C protocol every beginning of a communication the master provides a 8bits address to indicate which is the slave to be activated. To initiate the MARID1 programming the address is: 0000100/0

The overall MARID1 memory bank is organized as showed in figure 4-29.

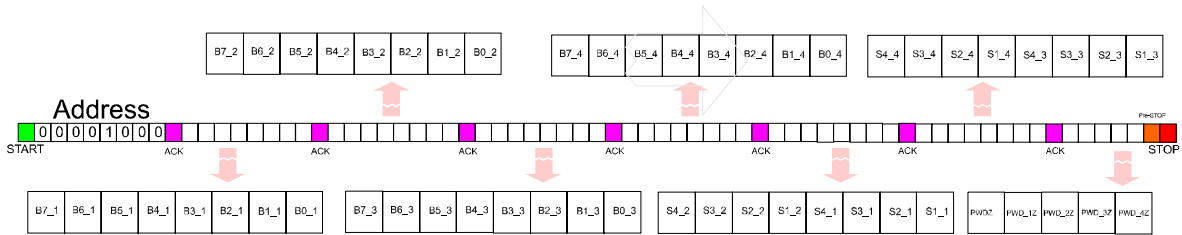


Figure 4-29. MARID1 Communication Protocol

An explanation of each memory block follows:

B<0:7>\_Y : DAC input for offset control in channel #Y. B0 (LSB) / B7 (MSB)  
(see DAC section 3.2.2.2.1.1 for further explanation)

S<1:4>\_Y : Gain program of channel #Y as follows in table 4-5 :

Table 4-5. Gain programmability

S1	S2	S3	S4	GAIN
0	1	0	1	5x2
0	1	1	0	5x20
1	0	0	1	25x2
1	0	1	0	25x20

PWD\_YZ : Powers Down the channel #Y when Low

PWDZ : Powers Down the current and voltage references when Low

#### 4.3.2.3.1.3 Layout

Due to special requirements of the design a totally automatic Placement & Routing was only possible in the logic circuit. The analog part was placed and routed manually as well as the pads and the Core-to-pads routing.

Figure 4-30 shows the MARID1 Top layout including the CheckSum and ByteCount parameters, which are necessary to validate the design to be fabricated through MOSIS:

Checksum: 34096431  
ByteCount: 704834

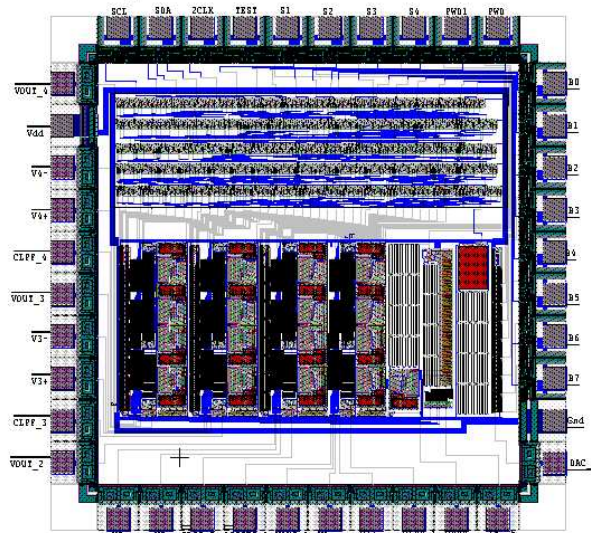


Figure 4-30. MARID1 Top Layout

Overall mask dimensions are  $2.2 \times 2.2 \text{mm}^2$  fitting within the maximum dimension of a TinyChip defined within the MOSIS program. In total there were 40 pads: (2) power, (9) analog inputs, (11) analog outputs, (3) digital inputs and (15) digital IO.

#### 4.3.2.3.2 MARID2 IC design

The design of this chip has been mostly reported in previous chapters, like the low power low-bandwidth receiver (section 3.2.1.2.3.) and the tunable BPSK transmitter, including the VCO, the modulator and the coil driver (section 3.2.2.2.1.). In terms of analog circuits the additional requirement was to have a system clock. The rest of the design was a digital implementation of the I2C interfaces of the different peripherals like the internal bank of registers (VCO calibration bits), the telemetry circuit and the memory chip.

##### 4.3.2.3.2.1 Low frequency clock

Low frequency clock generation was based in the time constant defined by charging a capacitor with a certain amount of constant current. Nominal frequency was

depending linearly on the  $I_{\text{charge}} \times C_{\text{charge}}$  product. Thus a clear sensibility on technology will apply, but a fairly chip-to-chip constant frequency will allow to use this clock as a good time reference for prototype testing. Two low-power comparators are required to discharge the capacitance every period and to define the pulse clock:

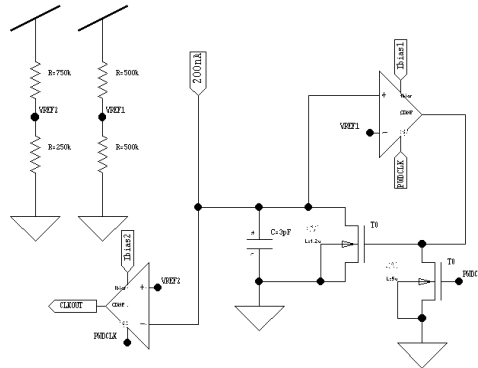


Figure 4-31. LFClock schematic

The final frequency depends on the biasing current, thus it has all the variability than the PTAT reference itself. An even more important point is that also depends on the absolute value of a capacitor. Typical value of frequency is around 35kHz with a current consumption of 30uA. As long as the PTAT reference and the supply conditions are stable, the frequency should not change. The dependence with the capacitor value makes this design very problematic if it is intended to be manufactured in large quantities, because the possible variation could be as large as 25%. For prototype development though, this issue is less critical. The PIC code will handle the clock variation once the chip clock value is known. In case that the design has to be transferred to manufacturing a digitally programmable capacitor or a programmable current reference can be used to calibrate at wafer level the clock to a pre-defined value.

An interesting point of this system is that allows external lecture of the internal supply voltage through the analysis of the Uplink communication. The reasons are (1) because through the Uplink it is possible to measure the internal clock frequency, and (2) because this frequency depends on the supply in a deterministic way so it is possible then to monitor the battery voltage of the implant.

As shown in figure 4-32, the capacitor is charged constantly (Icap node) up to reach a point (1.5V) where the comparator triggers a NMOS transistor and discharges the capacitor, defining a triangular voltage shape. The second comparator (triggering at .75V) is used to have a clear output clock signal. The 1.5V and the .75V references are derived from a resistive divider, with high resistance values (720kΩ). A power-down option disables the consumption to virtually zero levels.

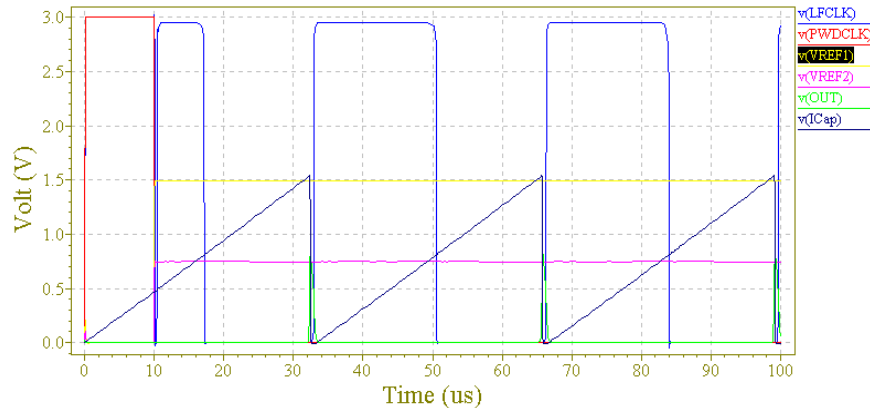


Figure 4-32. Post-layout Simulation waveform

#### 4.3.2.3.2.2 I2C/peripherals interface

##### i) I2C Interface

Because in MARID2 the slave modules may act as receivers or transmitters, a custom-made bonding pad has been designed to allow communication with the I2C bus for the SDA line. The SCL line remains as an input-only pad, because the PIC-master is the only one to generate any signal in this line. Moreover like in MARID1, a 2CLK signal (synchronized with SCL in negative edge) is mandatory for a good performance of the logic.

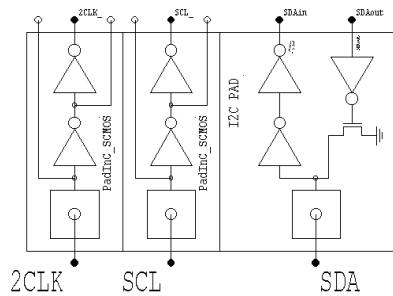


Figure 4-33. Special I2C SDA pad with open collector output

ii) MARID2 register bank

Likewise MARID1 memory, MARID2 has also a register bank of memory bits. Programming is as shown in figure 4-34.

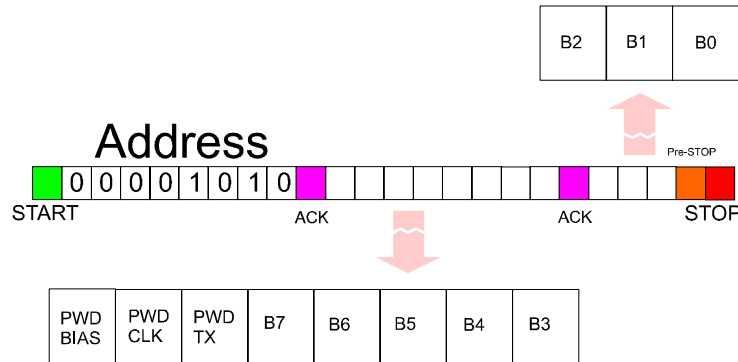


Figure 4-34. MARID2 programming protocol

- PWDBIAS : Powers down the current bias reference when High
- PWDCLK : Powers down the low-frequency clock generator when High
- PWDTX : Powers down the telemetry transmitter when High
- B<0 :7> : DAC input to fix the carrier frequency for the Telemetry TX

iii) RAM read

Read uses a standard common I/O protocol compatible with many RAM chips : N-bit address bus, 8-bit data I/O bus, CSZ (chip select), WEZ (write

enable) and OEZ (output enable). For reading we use an “address controlled” read waveform (see figure 4-35). It means that once the address bus is stable then data is ready (after the minimum read time, typically 100ns) in the output. During reading CSZ=OEZ=Low and WEZ=High.

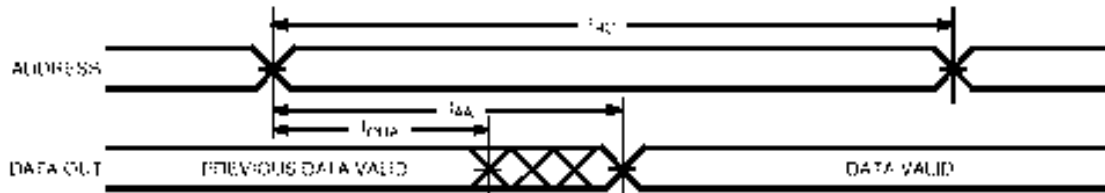


Figure 4-35. Read RAM cycle

The logic implemented uses a counter that goes from memory address 0 to up, until a STOP signal coming from the PIC is detected. Thus a continuous non-address-selective RAM reading is performed (download). The output is totally I2C compatible, so that data is packed in 8-bits+ACK. An STOP signal must come always before all RAM is being read (figure 4-36).

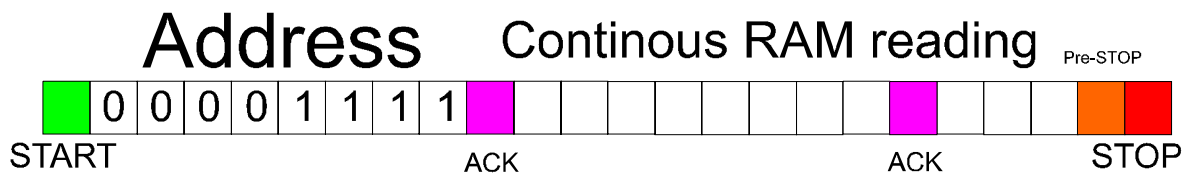


Figure 4-36. Read from RAM protocol

#### iv) RAM write

Write uses a standard common I/O protocol compatible also with many RAM chips : N-bit address bus, 8-bit data I/O bus, CSZ (chip select), WEZ (write enable) and OEZ (output enable).

For writing, a “CS controlled” protocol is performed (figure 4-37). Once address bus and the data bus are stable there is a low-pulse in the CSZ and WEZ lines simultaneously (it takes a CLK period). As an example the Hyundai HY62U256B SRAM memory fits with this protocol when OEZ is Low. In that

case there is no need to use ADD13 as OEZ and overall 14 bits of address can be used.

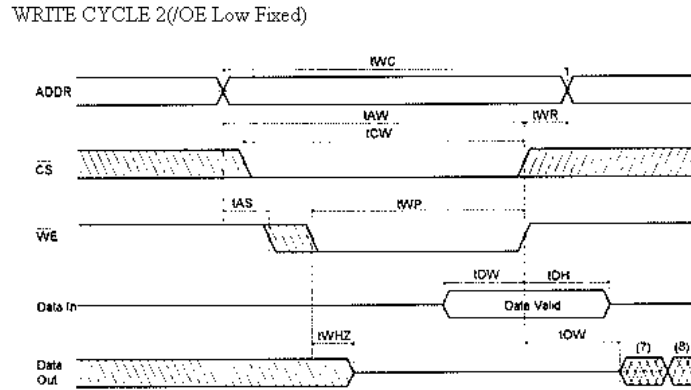


Figure 4-37. SRAM write cycle

The I2C-based communication with the PIC is as follows (figure 4-38):

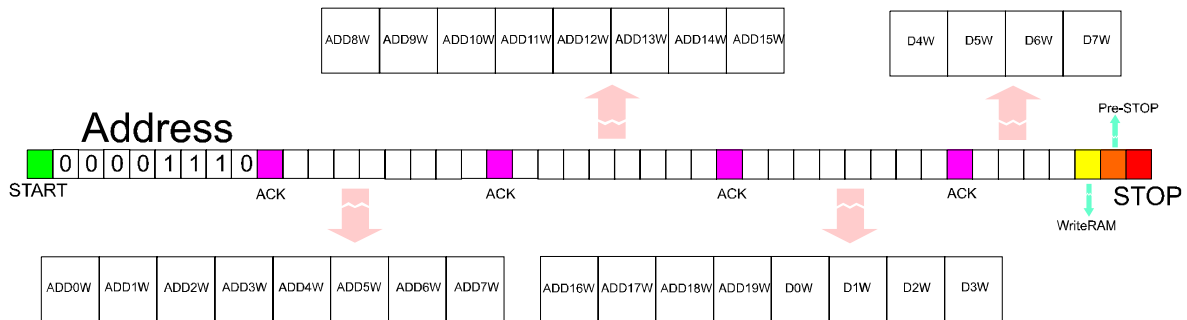


Figure 4-38. Write to RAM protocol

The writing cycle is done bit by bit, so every time the address and the data must be selected before effective writing. The logic design has been done for up to 20 bits of address bus (despite the maximum real address bits are 14, due to pad-number constrains). It is only a question of adding more pads if future needs require bigger memory. The communication protocol includes all 20 address-bits, so this must be considered, just putting to Low the non-used bits (from ADD14 to ADD19). ADD13 may be as already seen a real address bit or the OEZ line. In the later case for writing ADD13=High.



