Integration of CMOS-MEMS resonators for radiofrequency applications in the VHF and UHF bands

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CERTIFICA

que la memoria *Integration of CMOS-MEMS resonators for radiofrequency applications in the VHF and UHF bands* que presenta Jordi Teva Meroño per optar al grau de Doctor en Enginyeria Electrònica, s'ha realitzat sota la seva direcció.

Bellaterra, juny de 2007

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To my wife, Paola

Abstract

This thesis is focused on the monolithic integration of microresonators in a commercial CMOS technology, AMS-0.35μm, by using the standard layers of the process. The structures are released in a maskless post-CMOS process based on a wet hydrofluoric etchant. Those resonators will make the role of frequency selective devices replacing off-chip components of present front-end tranceivers communication systems relying on their reduced size, cost production and lower consumption.

In order to design and modelize those microresonators, an electromechanical model based on the real deflection of flexural resonator will be described allowing the designer to predict the maximum current levels at resonance. In addition to that, a set of mechanical design equations will be presented for all fabricated devices.

Along this report, different technological approaches using the available layers of the standard technology for fabricating microresonators will be introduced and discussed. From the design point of view, reducing the gap distance between resonator and driver becomes one of the relevant parameters that will enhance the electrical response of the device. Then, the approaches will be focused on reducing gap distances as much as possible. For the most promising approaches, limitations based on the vertical stiction in the releasing process will be considered in order to avoid the design of structures with limited performance.

A fabrication approach based on the layers of the standard capacitance module will stand out as the most promising approach for successfully fabricate integrated MEMS resonators in the VHF and UHF frequency range, as expenses of 40nm gap distances. Devices exhibiting frequencies in the VHF range, with high quality factors up to 3000 at 290MHz will be presented, giving a figure of merit of $Q \times f = 9 \cdot 10^{11}$Hz. Furthermore, preliminary results on the characterization of a ring bulk acoustic resonator at 1GHz will be described.

Agraïments

La realització d'una tesi doctoral implica una relació més enllà de la purament laboral entre el doctorant i el seu entorn. Per això i per damunt de tot, voldria destacar la excepcional qualitat humana del meu director de tesi, en Gabriel Abadal i Berini, que m'ha proporcionat un ambient de treball idoni per a la realització d'aquesta tesi doctoral i al qual sempre li estaré agraït. A més a més, la seva professionalitat, la seva quantitat i qualitat d'idees, el seu suport, la seva paciència i les discussions compartides han fet possible el desenvolupament d'aquest projecte i el meu creixement professional.

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L'Arantxa Uranga i en Jaume Verd han estat els responsables de dissenyar la circuiteria CMOS que han acompanyat els 'meus' ressonadors. Sense la seva feina no hauria estat possible obtenir els resultats que al llarg de la tesi s'han presentat. L'ambient en el grup de recerca ha propiciat la discussió i l'aparició de moltes idees entre els meus companys, dels quals he après contínuament. Els haig d'agrair a tots ells per aquestes llargues discussions i de tot allò que m'han fet veure, sense distinció entre ells, a en Jaume Verd, l'Arantxa Uranga, en Francesc Torres i en Joan Lluís López.

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etapa; és clar, sense el bon fer de les 'Martes', res d'això no hagués estat possible. La Marta Duch i la Marta Gerboles han sigut un exemple continu de feina ràpida i ben feta.

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No em voldria oblidar d'agrair tots els companys de departament, des de tots els becaris, associats, ajudants, titulars, agregats,..., fins al director, pels bons moments compartits. Mai oblidaré tot el suport logístic i personal que m'han brindat la Mari Carme, (darrerament també la Toñi) i en Javier Hellín, que ha patit la meva poca traça alhora de treballar al taller.

Ja de petit, els meus pares, l'Adela i en Manel, em van inculcar valors com la paciència, la confiança, i l'esforç per aconseguir aquells reptes que a primera vista podien semblar tan llunyans. De ben segur, que sense aquests valors avui no hi seria aquí. D'alguna manera ells són coautors i partíceps de tota aquesta feina. Ja farà uns quants anys, el meu germà Manel em va insistir en assistir-hi a unes classes extraescolars d'anglès, i sense saber-ho em va proporcionar una eina de futur molt valuosa, mai ho oblidaré. La Dolors, la meva germana, sempre m'ha demostrat la seva confiança en mi i m'ha donat peu a aconseguir tot allò que semblava un somni.

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CHAPTER 1

Introduction

Micro Electro Mechanical Systems (MEMS) were predicted by the legendary physicist Richard P. Feynman, who theorized in 1959 that size was not a barrier to advanced technology (*"there is plenty of room at the bottom"* [1]). However, it took three decades until the first commercial MEMS appeared in cars in the early 1990*s* under the name of *airbag*. MEMS also exist in such diverse devices as ink jet printers, blood pressure monitors, Digital Light Processor (DLP) and digital video projection systems. The acronym MEMS, includes (at least) micro, electrical and mechanical systems that are fabricated by microfabrication techniques. In the large and dynamic world of MEMS, devices showing intrinsic frequencies in the RF band are taking more and more relevance in recent years, motivated by the appearance of new wireless and more autonomous demanding applications.

This chapter introduces main concepts related with microresonators fabrication technologies as well as present and future applications in RF communications front ends. Special attention is given to capacitive transduced resonators, which is the base of the work developed during this thesis.

1.1 Motivation

The increasing demand on mobile communications and devices, that is observed by the new generation of wireless protocols developed recently [2][3] that sum up to existing ones like Bluetooth [4] and Wifi [5], are driving to a miniaturization of radio transceivers. In this miniaturization process, tradeoff between cost, size and power consumption is crucial. In terms of size, passive off-chip components of the front-end transceiver architectures represents the bottle neck for miniaturization.

The possibility to implement the filtering, mixing and frequency control functionalities present in a front-end transceiver by MEMS devices, allow the system size and power consumption reduction, consequently improving the functionality and reducing costs.

The Radio Frequency Micro Electro Mechanical Systems (RF-MEMS) market includes products such as Bulk Acoustic Wave (BAW) resonators, switches, inductors and micromechanical resonators is expected to be the next major breakthrough for MEMS technology, driven by the RF systems for telecommunication offering the possibility to integrate and miniaturize, lowering power consumption, lowering losses and lowering costs.

In figure 1.1 are depicted the commercial status from 2003 up to 2006 for 6 types of RF-MEMS components. BAW devices are currently the most mature components. On September 2005, several other companies were close to commercializing BAW, including *EPCOS* and *FUJITSU*. However, in the field of switches only a handful companies have started or are close to commercializing MEMS switches.

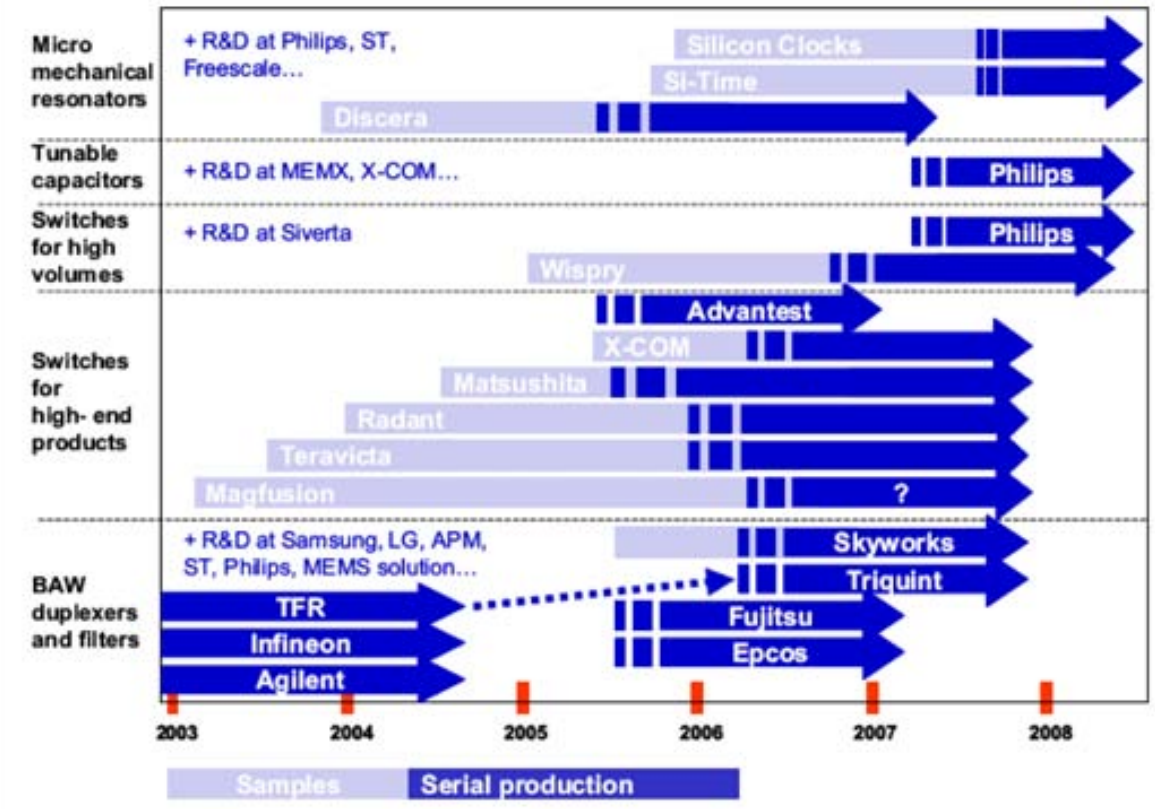


Figure 1.1: *Commerzialization of RF-MEMS products divided into* 5 *categories, showing the companies involved [6].*

Recent progress on micro-mechanical resonators have been significant and specifically involves temperature stability and packaging. *DISCERA*, *SILICON CLOCKS* and *SiTIME* expect serial production by the end of this year.

The market for RF-MEMS components was 126 million in 2004. Furtherthemore, it is expected to grow rapidly in the next few years to over 1.1 billion in 2009. In addition, the market will accelerate quickly in the period 2007 to 2009 as full-scale production starts for the majority of RF-MEMS components. The turnover forecast for the RF-MEMS market by application are shown in figure 1.2. Micromechanical resonators start to replace bulky off-chip quartz oscillators used as timing devices in consumer electronics. MEMS resonator-based clock devices will account for more than 20% of the RF-MEMS market in 2009. Switches are expected to penetrate cell phone applications from 2007 onwards, mainly for band and mode switching functions.

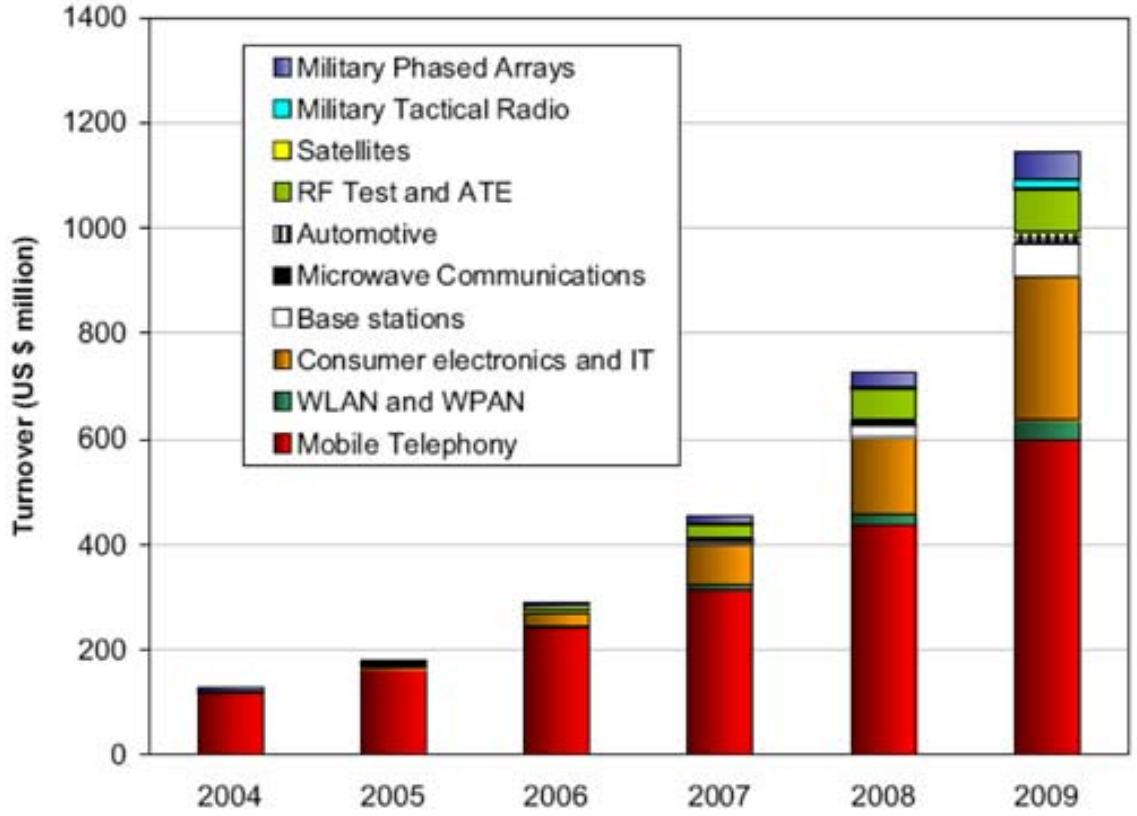


Figure 1.2: *Forecasts for RF-MEMS components market, separated by applications, from* 2004 *to* 2009 *[6].*

In this excellent situation for the RF market, this thesis has the main motivation of exploring, at the device component level, the integrability in a standard Complemetary Metal Oxide Semiconductor (CMOS) technology of MEMS resonators in the Very High Frequency (VHF) and Ultra High Frequency (UHF) frequency band.

1.2 Transceiver Architectures

The evolution of radio transceivers was extraordinary in the last whole frequency and conditioned by the increasing request of available frequencies for radio-communication and with the limited frequency spectrum. In the second half of the last century, improvement was provided, mainly, by technological evolution and by the advent of digital modulation techniques. However, the typical radio architectures remain inalterable. Now, with the advent of portable revolution and the industrialization of MEMS devices, innovative radio-architectures are being designed to make possible the single chip fully integration.

1.2.1 Superheterodyne transceiver

The superheterodyne transceiver is based on the idea of downconverting the signal band high frequency to lower frequencies in order to relax circuitry design. Figure 1.3 shows a typical superheterodyne transceiver architecture implemented in most of the actual RF communications transceivers. The transceiver is implemented with a collection of discrete-components filters and various technologies, Galium Arsenide (GaAs), Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) and CMOS.

The integrated circuitry include the low noise amplifier, Low Noise Amplifier (LNA), and the Solid State Power Amplifier (SSPA), which has a similar function but in the transmit path), Phase Locked Loop (PLL) electronics and lower frequency digital circuits for baseband signal demodulation.

In superheterodyne receivers, the signal (centered at frequency f_{RF}) captured by an antenna is initially filtered by the band selective filter and amplified by the LNA; then, that frequency is translated to the *IF* stage by the first mixer, driven by the local oscillator LO: the frequency f_{LO} is tunable and its value is a function of the carrier frequency of the channel that is received and demodulated ($f_{LO} = f_C + f_{IF}$); the correct value of f_{LO} is fixed by an RF channel select frequency synthesizer. Note that the whole signal band is frequency translated, and not only the desired channel.

A first filtering of the received signal is performed at the *IF* stage (shadowed boxes in figure 1.3), in order to highlight only the desired channel. This filtering operation is performed at *IF* because channels they have typically a very narrow frequency occupation and then, excessive Q in the RF filter should be required. Then, the desired channel is amplified by a variable gain amplifier that adjust the desired signal in turn of reducing the dynamic range

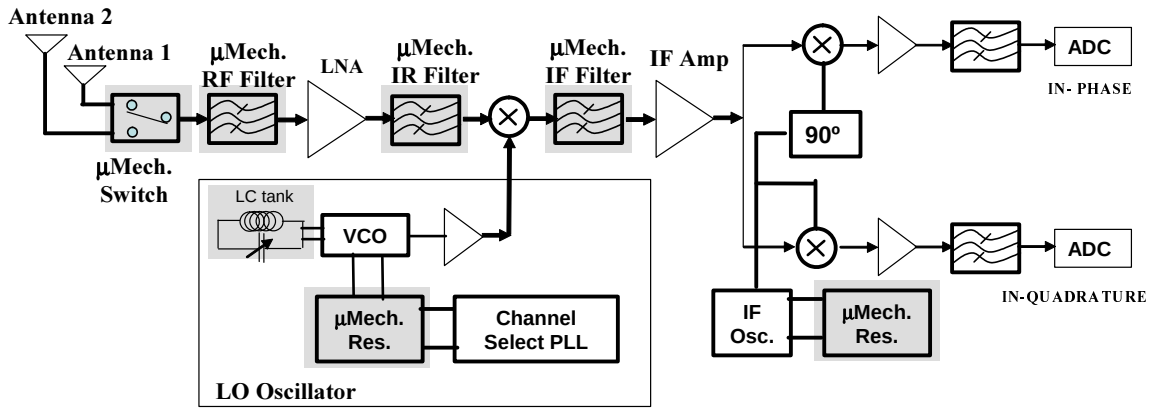


Figure 1.3: *Block diagram for a RF channel-select receiver architecture showing potential replacements via MEMS-based components. Components to be replaced by MEMS are gray-shaded.*

requirements of all subsequent blocks.

The most important thing in the design of a superheterodyne receiver concerns the choice of *LO* and *IF* frequencies. This choice is strictly related with the problem of the "image frequency, f_{IM}"; in a superheterodyne architecture, the bands symmetrically located above and below f_{LO} are downconverted to the same center frequency *IF*. The problem of the image is a serious one, whereas each wireless standard imposes constraints upon the signal emissions by its own users, it may have no control over the signals in other bands. Typically the channel at f_{IM} could be the channel of another user, and in general, can be very strong.

The classical solution to the image problem consist on the insertion, between the LNA and the mixer, of an image-rejection filter; this filter must present a relatively small loss in the desired band and a large attenuation in the image band. Obviously these two requirements can be simultaneously met if f_{IF} is sufficiently large (as f_{IF} increases, increases the distance in frequency between the channel frequency and its image with respect to f_{LO}, and decreases the performance on the image-rejection filter). If the choice of an high f_{IF} relaxed the Q requirement of the image-rejection filter, in order to relax the selectivity specifications of the channel selection filter, f_{IF} should be chosen as low as possible. This trade-off between image rejection and channel selection is the most important limitation of a superheterodyne receiver, and it can be lighten only using a multiple downconversion, each followed by filtering and amplification; this solution performs partial channel selection at progressively lower center frequencies, relaxing the required Q for each filter; this technique is known as "Dual-IF topology".

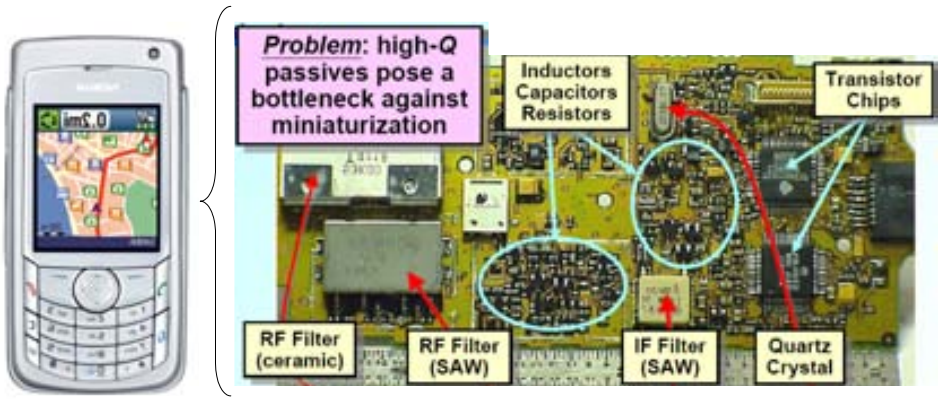


Figure 1.4: *Optical image showing the replaceable off-chip components [8]* .

The last step of the transceiver depicted in figure 1.3 corresponds to the digital demodulation of the IF signal, that is performed in phase and in quadrature in order to minimize the effect of noise on the demodulation.

1.2.2 RF-MEMS in superheterodyne architectures

In present superheterodyne communication transceiver depicted previously, vibrating components, such as crystal and Surface Acoustic Wave (SAW) resonators, are widely used because of their high quality factor and exceptional stability against thermal variations and aging.

High Q ($10^2 - 10^3$ in frequencies above $1GHz$), low insertion losses, and large attenuation below and above the frequencies of interest shown by SAW and bulk acoustic wave-based resonators are used to achieve adequate frequency selection in the RF and IF stages [7]. On the other hand, those high Q values imply the required low phase noise and thermal stability to their local oscillators (LO). In order to complete the design of the superheterodyne architecture, off-chip discrete inductors and variable capacitors are used to properly tune and couple the front end sense and power amplifiers. However, this actual design is size limited because of the external off-chip resonator tanks and discrete passive elements, as shown in figure 1.4. In this sense, these devices pose a bottleneck against the ultimate miniaturization and portability of wireless transceivers.

The miniaturization of those high-Q resonators can be done as expenses of the high quality factors exhibited by MEMS devices. Furthermore, the rapid growth of IC-compatible micromachining technologies and the possibility to monolithically integrate those microresonators may bring the strategy to miniaturize on-chip those resonator components.

Among the off-chip components targeted for replacement are RF filters, including image rejection filters, with center frequencies ranging from $800MHz$ to $2.5GHz$; IF filters, with

center frequencies ranging from $455kHz$ to $254MHz$; high-Q, tunable and low phase noise oscillators, with frequency requirements in the $10MHz$ to 2.5 GHz range; and switches for transmit/receive (T/R) selection, antenna selection, and multi-band configurability. The main benefits form this replacement using MEMS are the size reduction, lower overall insertion losses and the ability to tailor the termination impedances required by RF and IF filters.

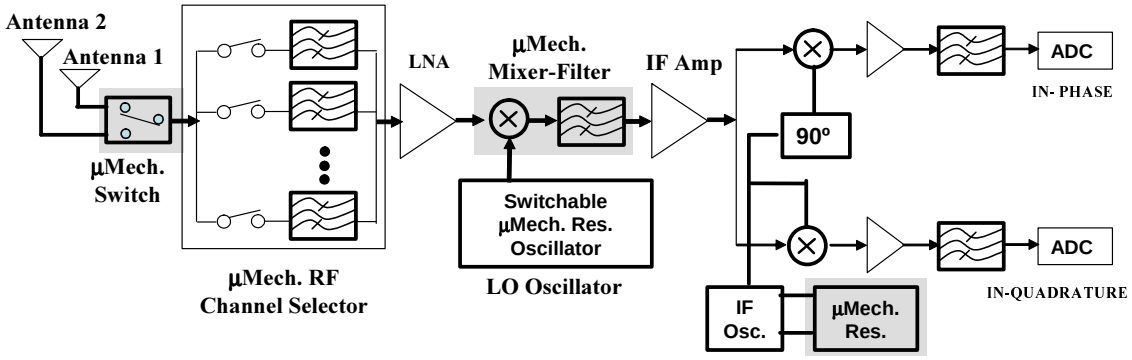


Figure 1.5: *RF channel select receiver architecture using large number of micromechanical resonators to lower power consumption.*

However, the direct replacement of off-chip high-Q passives is not the only possible approach using micromechanical resonators. A RF channel select architecture using a large number of high-Q micromechanical resonators in filter banks and switchable networks shown in figure 1.5 has been previously proposed [8]. By this approach, the RF architecture is based on two new blocks that minimize power consumption using the MEMS high-Q selectivity. The first new block is the *Switchable RF channel select filter bank*, where the channel selection is done at RF frequencies instead at IF frequencies, making following electronic blocks in the receiver path (LNA, *mixer*) no longer need to handle the power to alternate channel interferes. Then, a significant power reduction is achieved if the circuit is removed, or if the circuitry is maintained, more robust receivers are designed.

The use of a micromechanical mixer-filter (mixler) in the receive path (figures 1.3 and 1.5) eliminates the DC power consumption associated with the active mixer normally used in present day receiver architectures. This corresponds to power savings on the order of $10mW$-$20mW$ [8] . In addition to that, the requirements for designing the LNA are relaxed, because the mixler appears as purely capacitive, not requiring a driver stage to match a certain impedance characteristic of the present day mixers.

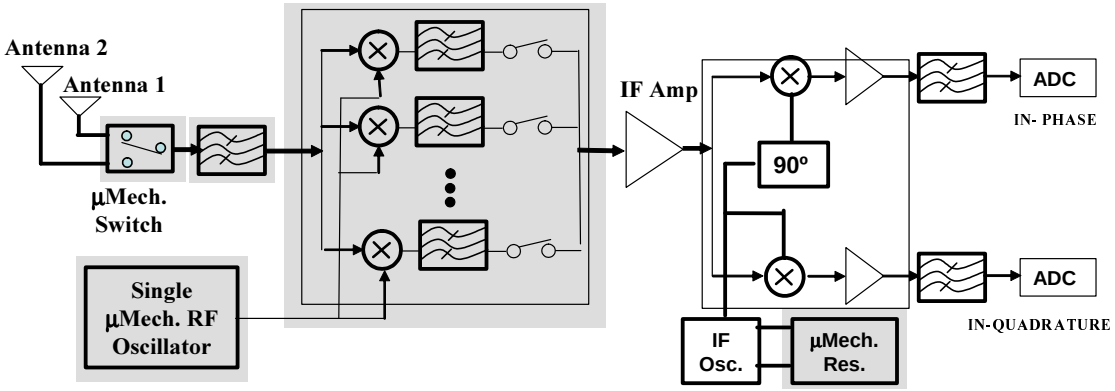


Figure 1.6: *Advanced RF front end without LNA and based on MEMS devices.*

Another approach to design a Radio Frequency (RF) architecture using MEMS devices is depicted in figure 1.6. By this new approach, the LNA amplifier is suppressed as expenses of the high-Q values with low insertion losses provided by the MEMS. Again, a band filter is necessary to solve the problem related with the image frequencies, that can be implemented by a bank of MEMS filters at high frequencies. Then, the signal follows a bank of narrow-band mixer-filter for the channel selection that feeds the subsequent electronics. In comparison to the front end architecture depicted in figures 1.3 and 1.5, the only active electronics operating at RF in this system are those associated with the LO, which uses a bank of micromechanical resonators, that can operate at $1 - 4mW$. The architecture of figure 1.6 clearly presents enormous power advantages, eliminating completely the power consumption of the LNA and active mixer of figure 1.3, saving a total power of $40mW$. However, the plausibility of this last front end scheme is subjected to implementing low insertion losses filter at high frequencies with high-Q factors.

1.3 MEMS fabrication technologies

In the $70's$ and early $80's$, the incipient fabrication technology of MEMS devices was borrowed from the integrated circuitry (IC) industry. The batch-fabrication processing common in the IC industry, allowed to reduce costs as expenses of fabricating thousands of devices at the same time, thus significantly reducing the unitary cost.

Although many of the fabrication techniques and materials used to produce MEMS have been borrowed by the IC industry, the field of MEMS has also driven the development and

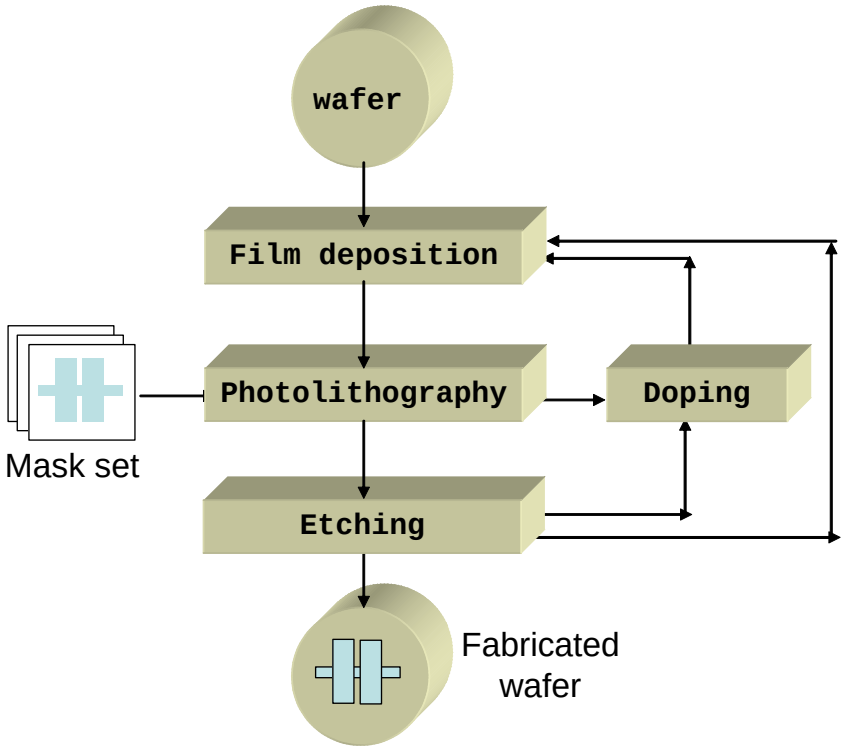
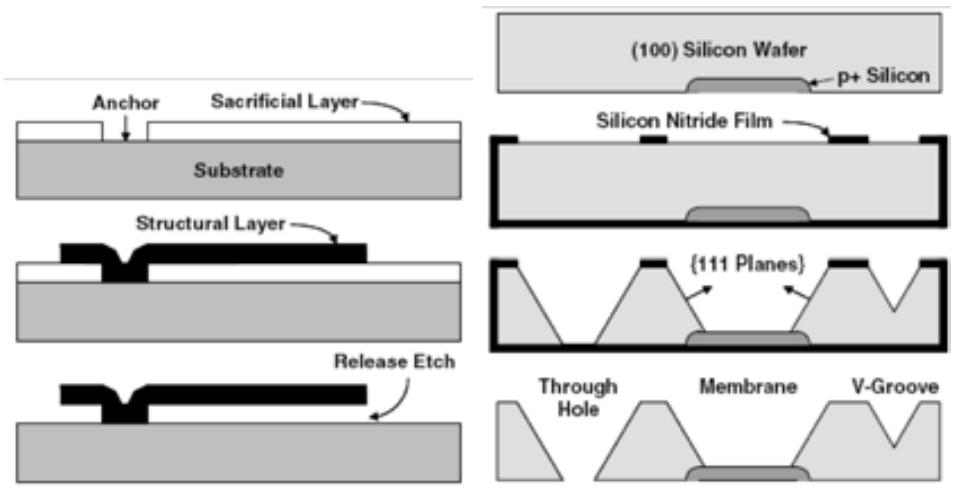


Figure 1.7: *Flow diagram of IC fabrication technologies.*

refinement of other microfabrication processes and materials like. For example, some relevant processes and new materials come from the hand of MEMS, like: anisotropic wet etching of single-crystal silicon, deep reactive-ion etching (Deep Reactive Ion Etching (DRIE)), X-ray, Atomic Force Microscopy (AFM) and Electron Beam Lithography (EBL) lithography as processes and piezoelectric films, magnetic films, Silicon Carbide (SiC), ceramics and polymers as new materials.

The fabrication of integrated circuits is based on four basic microfabrication techniques: deposition, patterning, doping and etching. The fabrication starts with the election of the wafer, typically single-crystal silicon is the standard substrate, and followed by iterative film deposition, patterning and etching processes, as shown in figure 1.7 [9].

The fabrication methodology to fabricate MEMS devices is derived from the scheme showed in figure 1.7. However, the necessity to release mechanical structures incorporates a new step in the overall process depicted previously for integrated circuitry fabrication. The film chosen to be the MEMS structure is named *structural material* whereas the film that has to be selectively etched in order to release the MEMS structure is named *sacrificial layer*.



(a) Surface micromachining and the sacrificial layer technique

(b) Bulk micromachining along crystallographic planes

Figure 1.8: Surface and bulk micromachining techniques.

The fabrication methodology for MEMS devices is classified into two large categories: surface micromachining and bulk micromachining. In the bulk micromachining, the substrate material, typically single-crystal silicon, is patterned and shaped to form an important functional component of the resulting device. On the other hand, in surface micromachining, the process fabrication follows an iteration of depositing, patterning and etching of a sequence of films. In this approach, the selective removing of the sacrificial layer is crucial. In figure 1.8 it is shown those two approaches used to fabricate MEMS.

In order to reduce the number of off-chip components required to operate in a sensing system, more and more building blocks are integrated together with the microresonator on the same chip. Then, to be able to produce systems-on-chip Systems On Chip (SoC) with integrated functions, the technology used to fabricate the microsensor must be merged with standard *IC* technologies, i.e., CMOS or bipolar process technology. The field in charge of integrating MEMS devices along CMOS processes is named CMOS-MEMS. The CMOS circuitry typically makes the role of amplification and conversion of the analog signal of the transducer to the digital domain [10].

However, not all devices are fabricated by compatibilizing CMOS and MEMS fabrication processes. Figure 1.9 shows two different approaches for fabricating MEMS devices that need, for example a CMOS building block to implement conditioning signal performance. These two approaches are named CMOS-MEMS monolithic fabrication and CMOS-MEMS hybrid fabrication, respectively.

The monolithic CMOS-MEMS approach allows the highest integration density and shortest

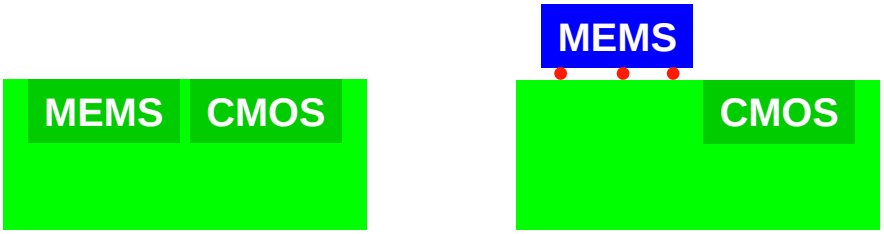


Figure 1.9: *Left: CMOS-MEMS monolithic fabrication; right: CMOS-MEMS hybrid fabrication approach.*

electrical interconnections. This reduces parasitic loads and yields high operation speeds. Furthermore, process assembly steps are necessary. On the other hand, thermal budges and limitations due to the inherent integration will limit and conditione the design. As a example of the hybrid approach, a $14MHz$ oscillator based on a micromechanical resonator is the objective of this work [11]; in one chip the microresonator is fabricated whereas in the other chip a CMOS amplifier complements the design. Another similar work has been published more recently [12], also relating a fabrication of a MEMS-based oscillators.

As an example of the monolithic approach, a CMOS amplifier is integrated monolithically with the resonator [13], in order to build a gyroscope. The advantages of incorporating a design into a CMOS process are paid by the restrictions imposed by the layers technology. In that case, parasitic capacitances are reduced due to the proximity of the resonator with the circuitry and also the assembling (not the packaging) is easier. However, the standard technology will impose conditions that will limit the design of the resonator. Devices fabricated by the hybrid approach take advantage of the no imposed restrictions on the design step but then, the designer is forced to think about the assembly with the CMOS circuitry.

The CMOS-MEMS technological approaches can be divided into three different categories, depending when the micromachining module is fabricated with respect to the standard CMOS sequence [14].

When the MEMS fabrication module precedes the standard CMOS, the CMOS-MEMS approach is named pre-CMOS. This approach, named also *MEMS-first*, avoids thermal budget constraints during the MEMS fabrication. Then, thermal annealing needed for thick polysilicon structural materials can be cointegrated with CMOS circuitry. Examples of polysilicon microstructures implemented in a pre-CMOS approach include the M^3EMS (modular, monolithic microelectromechanical systems) technology [15].

A recent work categorized in this approach is depicted in table 1.1 [16]. This new process module, called *Mod MEMS*, allows the integration of thick polysilicon structures ($> 6\mu m$)

Pre-CMOS or MEMS-first fabrication process [16], [15]	
Advantages	**Disadvantages**
1. Avoids thermal Budgets	1. Planarization before the CMOS
2. Supports high temperatures required for releasing stress	2. Pre-processing not always allowed by the CMOS foundry

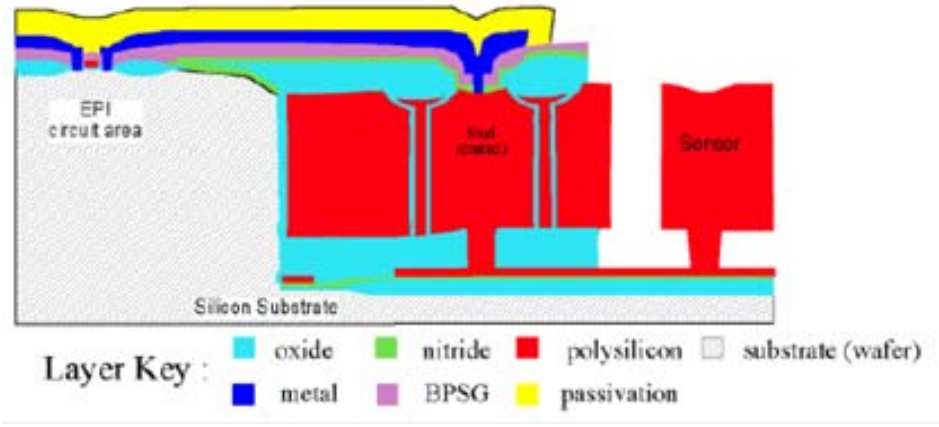


Table 1.1: *Pre-CMOS or MEMS-first process fabrication.*

annealed at 1100^oC or higher temperatures for complete stress relief.

If the MEMS fabrication is performed in between the regular CMOS step, which is the most common case, is named intra-CMOS. This approach consists on inserting the micromachining process steps before the backend interconnect metalization, ensuring process compatibility with the polysilicon deposition and annealing.

An example of this approach was developed by *Siemens* and reported in [17], where is described the fully integration of a pressure sensor into a standard $0.8\mu m$ analog BiCMOS process. One additional photolithography step and an etching step are necessary to achieve the micromachined structure whereas the sensor membrane is a $400nm$ polycrystalline silicon standard layer of the basic BiCMOS process. In table 1.2 is shown the cross section of the standard BiCMOS process within the integrated pressure sensor.

When the MEMS fabrication is completed after the CMOS fabrication, the approach is named post-CMOS. The main advantage in this case, is that the MEMS and CMOS fabrication processes can be performed in different foundries. However, this advantage is paid in terms of the thermal budget, that now is reduce down to 450^oC, in order to prevent damaging on the aluminum metalization.

Intra-CMOS fabrication process [17]	
Advantages	**Disadvantages**
1. Process compatibility between polysilicon deposition and anneal.	1. Anneal temp. limited to 900^oC.
	2. Polysilicon layer limited to few microns.

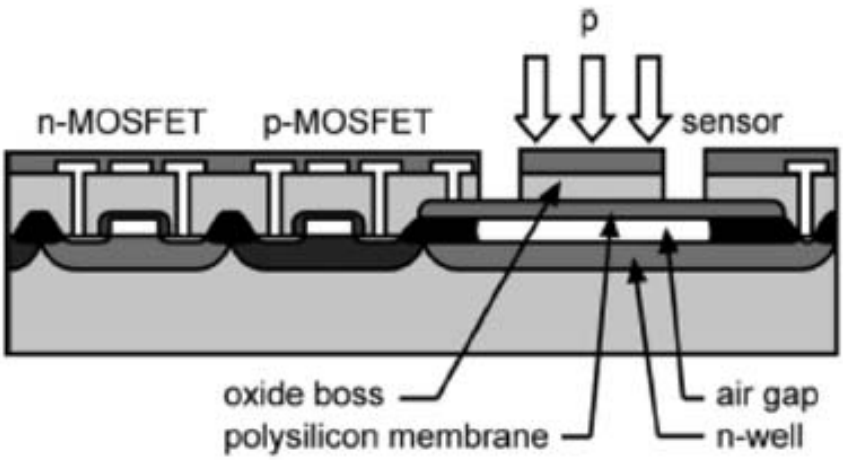


Table 1.2: *Intra-CMOS process fabrication.*

Two general post-CMOS micromachining approaches can be distinguished: the microstructures are formed either by machining the CMOS layers themselves or by building the complete microstructures on top of the CMOS substrate. In the first approach, most of the microstructure is already created within the regular process sequence using the available standard layers. Then, the post-CMOS process module typically requires very few process steps, such as an etching step to release the microstructure. Building the complete MEMS on top of the CMOS substrate might require more process steps but can save valuable real estate, because the MEMS part can be build directly on top of the CMOS circuitry. However, the thermal budget is always limited below 450^oC.

An interesting example of the first approach was developed and published by Prof. Fedder [13]. The MEMS structure is a sandwich of metals and inter-metal oxides that are patterned after the CMOS completion by DRIE techniques. A cross-section of the technology is depicted in table 1.3. The fabricated gyroscope has a noise floor of $0.02^o/s/Hz^{1/2}$ at $5Hz$. This technology also has been used to design a commercialized CMOS-MEMS microphone [18] and frequency selection elements in a RF transceiver [19].

In the second approach, the advances are focused on depositing at low temperatures the structural layer of the MEMS structure. Recent efforts have been done at Inter-universitary of Micro Electronics Centre (IMEC), in order to develop MEMS-structural and CMOS compatible layers in an above-CMOS technology [20]. Low tensile stress of hydrogenerated micro-

Post-CMOS fabrication process [13], [19]	
Advantages	**Disadvantages**
1. The fabrication can be completely outsourced from the CMOS foundry.	1. Stringent thermal budget.

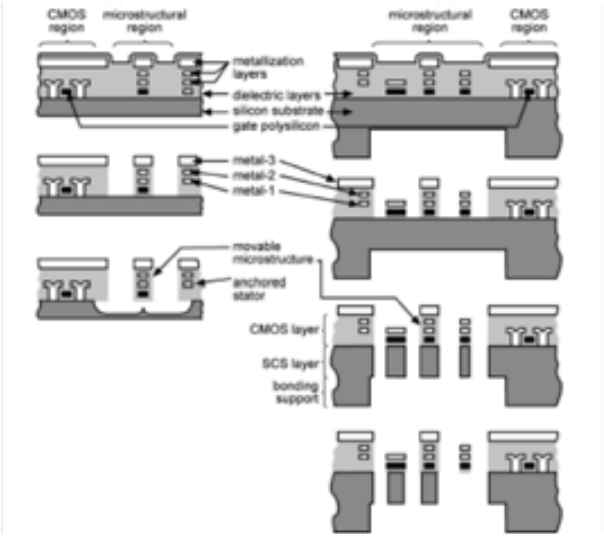


Table 1.3: *Post-CMOS process fabrication where the microstructures are formed by machining the CMOS layers themselves.*

crystalline silicon germanium ($\mu cSiGe:H$) have been deposited on top of CMOS by Plasma Enhanced Chemical Vapor Deposition (PECVD) techniques at temperatures of $300-400°C$, showing good mechanical and electrical properties.

In our research group at UAB [21], an effort to monolithically integrate MEMS based transducer along the CMOS circuitry has been performed in order to develop an ultrasensitive mass sensor. The integration approach has been developed, basically, in the framework of two research projects, *Nanomass-II* [22] and *Nanosys* [23]. In the *Nanomass-II* project, Si and SOI wafers were the starting point for the circuitry fabrication [24]. The structural layer for the resonator was a deposited polysilicon (for the Si wafer process) and the Single Crystal Silicon (SCS) (for the SOI wafer process) that was patterned after the circuitry finalization, by using different technological approaches, such as optical lithography, EBL [25] and by AFM-local [26] oxidation methodologies. The circuitry was based on a $2.5\mu m$-technology available at the *Institut de Microelectrònica de Barcelona*.

Following this research line, the *Nanosys* project envisaged the integration of multiple microresonators for frequency selection operation in future frontend transceivers in a standard and commercial CMOS technology. On that case, the post-CMOS process is designed just to

release the microresonators; the resonators are fabricated at the same time as the circuitry and only a maskless process will be necessary to remove the sacrificial layers and release the structures. Recently, a monolithically mass sensor has been fabricated by that CMOS compatibility, showing a mass sensitivity in the attogram/Hz range [27].

1.4 Transduction in RF-MEMS

Microresonators exhibit typical mechanical resonant frequencies ranging from few kilohertz to Gigahertz, depending on their dimensions and resonance modes. Several techniques have been developed in order to excite the resonance state of such devices: electrostatic, thermal, electromagnetic, electromotive and piezoelectric; and different detection techniques have been developed in order to obtain experimental data concerning the dynamic state: capacitive, piezoresistive, inductive, optical and piezoelectric readout are the most common. Most of those techniques were first developed to excite and detect the resonance state of resonators used in sensor applications.

1.4.1 General actuation and detection methods

The **Thermal actuation** technique uses the bimorph effect of a cantilever (as an example) with several layers each having a different thermal expansion coefficient. The cantilever is heated by placing a resistor on or near the cantilever. When a current is passed through this resistor, the temperature rises locally on the resonator and the material expands, bending the resonator due to stress. Resonant frequencies as high as $400kHz$ have been actuated and actuation frequencies in the MHz range are claimed to be possible, with cantilevers integrated on CMOS circuitry [28], [29].

The **Piezoelectric** technique utilizes the electromechanical coupling found in piezoelectric materials, such as single-crystalline quartz. The technique is to sandwich a piezoelectric material between two metal contacts, which is then placed on a silicon resonator. By again applying an alternating voltage across the piezoelectric material, one can actuate the resonator. The drawbacks of this technique are that most piezoelectric materials are not CMOS compatible.

The **Magnetomotive actuation** is done by applying a static magnetic field perpendicular to a beam structure and alternating an AC current through the beam. The Lorenz forces acting on the electrons will drive the resonator. The disadvantages are that in order to achieve a large actuation force, large magnetic fields need to be applied. This technique or similar techniques has been demonstrated in other works [30].

In the **Magnetic actuation** the cantilever is a magnetic material and an oscillating magnetic field is applied parallel to the vibration of the cantilever. The magnetic field induces a force on the cantilever. Several examples of this actuation method have been demonstrated [31],

[32]. The main problem with this method is the need for a magnetic material on the cantilever and the aligning of the magnetic field to the cantilever.

The most common detections methods are described hereby:
The **Piezoresistive readout** is a readout technique widely used since both single-crystal Si and poly-Si are good piezoresistive materials at the right doping level [33], [34]. The idea is that when the resonator bends, the resistance of the piezoresistor changes due to the stress in the material. Thus, one could detect the bending of a cantilever by simply measuring the resistance of the piezoresistor. A drawback for this detection method is that one needs to have a circuit on the actual resonator structure. This limits the minimum size of the resonator in the case of the cantilever, because one needs two contacts to the cantilever. Piezoresistive readout has been demonstrated for Si based AFM cantilevers [35], [36].

The **Optical detection** is based on the reflection of a laser beam on the cantilever and onto a position sensitive photo diode. When the cantilever bends, the movement is registered by the photo diode. This method is used in most AFM microscopes. However, since the typical laser spot diameter is approximately $10\mu m$, the minimal size of the mechanical device is limited. Another disadvantage is that this type of detection method requires a laser and photo diode, which takes up lots of space, and is not compatible with some possible applications.

1.4.2 Capacitive transduction

Present MEMS components in transceiver architectures are based on two of the previous described approaches, piezoelectric resonant structures electrostatically excited and mechanical vibrating structures electrostatically driven and capacitively transduced. Each group of devices present some advantages and drawbacks that makes impossible to decide which are the best, so the final application will decide which is the most suitable in each case.

The main advantages of choosing Film Bulk Acoustic Resonator (FBAR) devices in front of mechanical microresonators capacitive transduced:

- The design, operability and implementation in the range of frequencies above $1GHz$.
- The power management of such devices, leading to a low series resistances, mismatchable along the circuitry in the RF design.

However, the election of FBAR resonators presents some drawbacks:

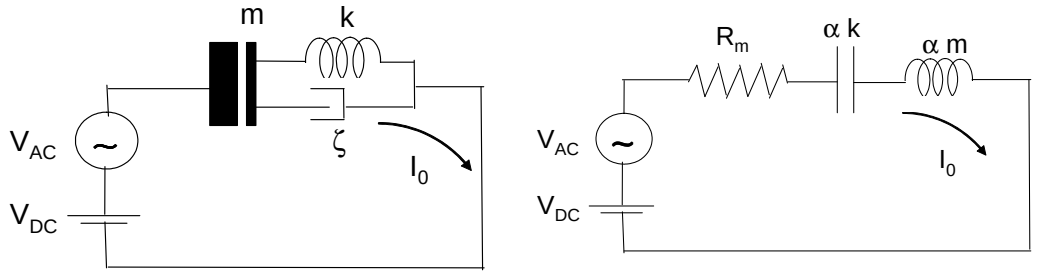
- The piezoelectric material deposition is not CMOS compatible. This makes more difficult the fabrication process of the resonator even if the FBAR is fabricated in a different chip.
- The thickness of the piezoelectric material determines the frequency of operation, yielding to only one frequency per chip. Furthermore, the non-uniformity of piezoelectric

material thickness leads to variability on the resonance frequency. Some works have been focused on solving this restriction, for example, it has been suggested to use the piezoelectric lateral mode (d_{31}) instead of the vertical mode (d_{33}).

- The capacitive transduced resonators can be easily switched off by removing the DC voltage applied. This is very useful when designing a bank of filters. However, for FBAR an additional switch is needed.

Due to the CMOS compatibility, and the possibility of integrating such devices in a CMOS commercial technology, the devices developed on this thesis are focused on capacitive transduced microresonators. In this microresonators, the excitation is done by an alternate voltage applied to a structure called excitation electrode and the signal detection is done by transducing the change on the capacitive due to the resonance mode in the read-out driver, as shows figure 1.10. A DC signal has to be applied to the resonator electrode in order to convert the capacitance change on electrical current.

The total capacitive current can be written as:



(a) Mechanical domain

(b) From mechanical to electrical domain

Figure 1.10: *Equivalent electrical circuit for a resonator, showing the mechanical magnitudes, effective mass, spring constant and damping coefficient, and their conversion to a pure electrical domain: motional resistance, capacitance and inductive elements .*

$$I_O = V_{DC}\frac{\partial C}{\partial t} + C\frac{\partial V}{\partial t} \simeq V_{DC}\frac{\partial C}{\partial t} + C\frac{\partial v_{ac}}{\partial t} \tag{1.1}$$

where C is the capacitance between resonator and electrode.

Electrostatic actuated and capacitive transduced MEMS resonators have been demonstrated up to GHz range frequencies exhibiting quality factors above 10.000 [37]. However, achieving good enough signal coupling becomes increasingly difficult as increasing the target frequency. The motional resistance is an equivalent electrical parameter related inversely proportional to the output current produced by the mechanical movement of the structure at resonance. This parameter will allow the reader to get in touch for the first time in the most relevant parameters related with the capacitive transduced MEMS.

$$R_{mot} = \frac{v_{ac}}{I_o} \simeq \frac{k_r}{\omega_0 V_{DC}^2} \frac{d_0^4}{\epsilon A^2} \frac{1}{Q} \tag{1.2}$$

where k_r is the equivalent elastic constant of the resonator at the modal frequency ω_0. V_{DC} is the DC voltage applied to the resonator and d is the gap distance between the read-out electrode and the resonator. ϵ is the gap material permitivity and can be expressed as $\epsilon = \epsilon_0 \times \epsilon_r$, where subindex 0 and r refer to the value in air (or in vacuum) and to the relative permitivity of the medium, respectively. As it will be explained in future chapters, a way to increase the read-out current is fabricate these devices with a solid high permitivity transducer gap. A is the coupling area between resonator and electrode. This factor is closely related with the reduced electrical transduction that occurs when dimensions are reduced for increasing the frequency.

And finally, the parameter Q represents the mechanical quality factor of the structure. This dimensionless parameter models the losses in a resonating system. The definition can be written as:

$$Q = 2\pi \frac{Energy \quad stored \quad per \quad cycle}{Energy \quad dissipated \quad per \quad cycle} \tag{1.3}$$

The quality factor can be written also in terms of the damping coefficient (ξ), $Q = \frac{1}{2\xi}$. When the resonator in immersed in a fluid, the sources of damping are related directly to the friction with the fluid [38], [39]. The friction with the surrounding fluid represents two terms on the total damping. The first contribution is due to the friction of the resonator movement with the fluid whereas the second term is a consequence of the capacitive transduction as expenses of the proximity of the read-out electrode. However, when the resonator is in a low pressure ambient, losses are then due, basically, to the acoustic vibrations transmitted through the anchor structure supporting the resonator [38], the surface effects in thin resonators [40] and the thermoelastic damping inherent to the structure [41].

In general, the Q factor can be expressed as:

$$\frac{1}{Q_{Total}} = \frac{1}{Q_{Air-Damping}} + \frac{1}{Q_{Air-Squeezing}} + \frac{1}{Q_{Anchor}} + \frac{1}{Q_{surface}} + \frac{1}{Q_{TED}} \tag{1.4}$$

In air, the Q-factor is limited by the air damping and squeezing. In vacuum, the main losses are due to the anchoring, surface effects and in minor importance, thermoelastic losses.

In order to integrate MEMS devices along circuitry in RF frontend receivers, an equivalent 50Ω-motional resistance is often desired and pursued. Then, the maximum quality factor (Q), together with the coupling area (A), the gap distance (d), the applied voltage (V_{DC}) and the gap spacer permitivity are the design parameters in order to achieve that goal.

1.5 Objectives, challenges and outline of the thesis chapters

This phd thesis is defined in the framework of the *Nanosys* project, which main purpose is the monolithically fabrication of a MEMS-based oscillator operating at $1GHz$.

Then, the main objective of this thesis is the monolithic fabrication of RF microresonators in a commercial technology using available standard layers of the technology. The conception of the post-CMOS process is a maskless process in order to release the resonators.

This main objective presents some challenges from the design point of view, due to the lack of knowledge of the technological process. The MEMS designer only has the electrical datasheets of the technology, and the information regarding the mechanical properties of the structural layers and how the process is being carried out is not provided by the foundry, and has to be deduced from run to run. Then, different approaches will be defined starting from the crossection of the technology and one of the aims is to conclude which of the technological approaches is the best option and which are the real limits for fabricating MEMS resonators using this technology.

This limitation of information together with the limitation in costs and in time, condition the development and the achievement of the main goal of the project.

Secondary objectives that have been pursued during the achievement of this phd thesis are:

1. Electromechanical modelization. From the circuitry design point of view, it is desired to predict the current levels that will be produced by the resonator. Then, an electrical equivalent model of the resonator will be developed. Furthermore, resonance modes for different vibrating structures will be presented, in order to have a library of resonators to match the target frequencies.

2. Hybrid fabrication. In addition to monolithic integrated resonators, two technological process sequences independent of the CMOS circuitry will be implemented in order to study resonators fabricated in single crystal silicon and to study the transduction by a solid dielectric gap resonator.

The thesis is divided into six chapters. The first chapter gives an introduction to the microresonators electrostatic excited and capacitive transduced, depicting their frequency selection functions in present superheterodyne transceiver architectures. Furthermore, a state of the art for CMOS-MEMS technologies will be presented.

The second chapter is focused in the design and modelization of the vibrating structures in order to accomplish the target frequency as well as predicting the resonance current levels crucial for the CMOS circuitry design.

The third and fourth chapters are dedicated to the MEMS fabrication. In the third chapter the microresonators are fabricated by the hybrid approach; two different technological

processes will be presented: the first one is focused on fabricating resonators in SCS with gaps smaller than $100nm$; the second hybrid approach has as main characteristic to study the transduction by a solid dielectric gap.

In chapter 4 different alternatives are discussed in order to fabricate monolithically RF microresonators using the standard layers available in the Austria Micro Systems (AMS)-$0.35\mu m$ technology.

In chapter 5 and 6, the electrical as well as the structural characterization of the resonators fabricated by the previous technological processes will be described. The experimental results are divided regarding the intrinsic frequency of the devices; then, in chapter 5 will be described the resonators with resonating frequencies in the VHF ($10MHz$ up to $300MHz$) range, and in chapter 6 the resonators showing resonance frequencies in the UHF (from $300MHz$ up to $1GHz$) range.

CHAPTER 2

Resonator Electromechanical modeling

In this chapter an electromechanical model of the capacitive readout system, electrostatically excited, has been described and implemented. The model was firstly conceived to modelize a cantilever-driver system for mass sensing [42], and afterwards was used to modelize a clamped-clamped beam. The chapter starts with the description of the electromechanical model and its implementation in *Matlab* [43] and *Spice* [44]. The extension of this model to bulk acoustic resonators is of immediate application. For all resonators devices designed along this phd thesis, a set of equations relating resonance frequency and effective mass in the proposed vibrational modes is done. In some cases, those design equations have been complemented with Finite Element Method (FEM) solver simulations in order to corroborate the analytically calculated data.

2.1 The electromechanical model

In the design phase of a microresonator it is very important to predict approximately output current levels, as well as maximum DC voltages that can be applied without collapsing the structure and resonance frequencies for the different vibrational modes.

In that sense, FEM tools (*ANSYS* [45], *Coventor* [46]), give to the designer the possibility to simulate and predict accurately resonance frequencies, and hence extract effective mass and spring constants. This is really helpful when designing structures that do not have analytical equations for resonance frequency, elastic constant and effective mass, for example when designing an elliptical-shaped microresonator. However, this programs tends to fail when performing transient analysis or if not, they are time consuming. For this reason it is highly recommended to have an approximated model but non-time consuming and easily reconfigurable.

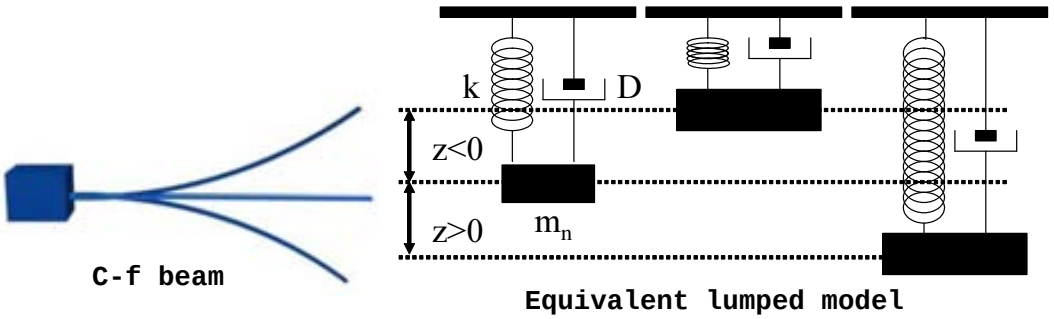


Figure 2.1: *Clamped-Free beam modelized by the lumped model approximation. The static mass of the system m_0 is modelized by m_n, taking into account the n vibrational mode.*

The model here depicted is based on a lumped model but taking into account the real deflection for flexural microresonators, like clamped-free beams and clamped-clamped beams. For bulk acoustic resonators, with inherent lower displacements at resonance a simplification of the model is done.

Two different versions of the model have been carried out; the first version is based on the implementation of the equation of movement in *Matlab*, which allows calculation of the current levels around resonance as well as frequency calculation, effective mass and spring constant. However, the limitation of the model arises when demanding electrical parameter such as transmission power and equivalents. For that reason, the same model has been done in a pure electrical environment *Spice* with the same functionalities. In addition to that, and due to the inherent conditions of an electrical environment, the model allows to simulate directly the transmission curves of the microresonator adding electrical impedances and circuitry elements.

This tool is very important for predicting the behavior of the transducer along with the CMOS circuitry. Then, the CMOS designer has a simulation tool to predict accurately microresonators output levels in order to evaluate (previous to fabrication), the CMOS circuitry performance in a preliminary design phase.

The start point of the model is the second degree equation of movement 2.1, which has implicit the lumped model approximation. Under this approximation, the resonator system is described under one variable with an effective mass (m_n) that accounts for the movement of the whole resonator in terms of the maximum displacement point. For a clamped-free beam, the maximum displacement point is the free end of the structure, whereas for a clamped-clamped beam that point is the middle of the structure. The equation of movement is described in terms of the variable z, which represents the movement of the maximum dis-

placement point.

This lumped mass model approximation is depicted in figure 2.1. The system, in that case a resonating clamped-free beam of static mass m_0 is modelized via a lumped model approximation. The parameter that takes into account the pondered movement of the whole beam in the one-variable time dependent (z) is the effective mass.

$$m_n \cdot \frac{d^2z}{dt^2} + D \cdot \frac{dz}{dt} + k \cdot z = F_{ext}(t, z) \tag{2.1}$$

which is derived from the system hamiltonian, H:

$$H = \frac{p^2}{2 \cdot m_n} + \frac{k \cdot z^2}{2} + \int \frac{D}{m_n} \cdot p \cdot dz + W_{ext} \tag{2.2}$$

by the second Newton's law:

$$m_n \cdot \frac{d^2z}{dt^2} = -\nabla \cdot H \tag{2.3}$$

The first term in equation 2.1 is the inertial force of the system. m_n is the effective mass of the system at the vibrational mode n, taking into account the movement carried out by the whole resonator. The second term is due to losses of the system. D is the damping factor which is related with the quality factor Q by:

$$D = \frac{\omega_n \cdot m_n}{Q} \tag{2.4}$$

where ω_n is the resonance frequency in rad/s of the n-vibrational mode. Typically, operating in a fluid, the system loses are mainly associated to the friction with the fluid. However, when operating in vacuum, losses are due to other sources of dissipation, like anchor losses (Q_{anchor}), surface effects ($Q_{surface}$) and intrinsic thermo-elastic loses (Q_{TED}). So, in general, the quality factor can be written as:

$$\frac{1}{Q_{Total}} = \frac{1}{Q_{Air-Damping}} + \frac{1}{Q_{Air-Squeezing}} + \frac{1}{Q_{Anchor}} + \frac{1}{Q_{surface}} + \frac{1}{Q_{TED}} \tag{2.5}$$

In the following section 2.9 it will be described in more detail the mechanisms of dissipation as well as analytical equations in order to predict approximately those values, which are an input parameter in the modelization and simulation process.

The third term in equation 2.1 is due to the recovering force on the system that tries to force the position of the system to its equilibrium. In general, this term is kz where k is the equivalent elastic constant of the system and z is the displacement. For large displacements it has to be taken into account non-linear terms that appear in the equation of movement 2.1. For example, in clamped-clamped beams some non-linearities are observed when deflections

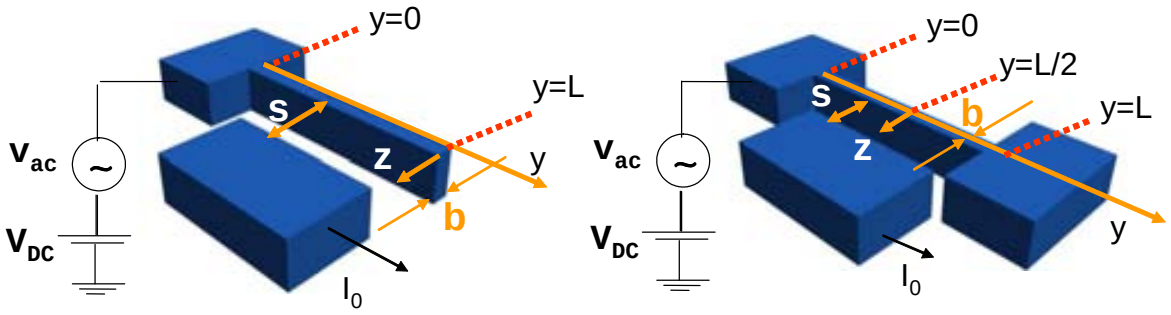


Figure 2.2: *c-f (left) and c-c (right) resonators in one port configuration. For the c-f resonator, the maximum displacement is produced at the free end ($z = L$); for the c-c beam, the maximum displacement is obtained at $Z = L/2$. b and s are the beam width and lateral gap distance, respectively.*

are bigger than $0.02L$ (where L is the length). On those cases the non-linear term is expressed as $k_3 z^3$, where k_3 is the non-linear elastic term [47].

In electrostatic excited MEMS microresonators, the external force on equation 2.1 is due to alternate electric field applied to the driver electrode (F_{ext}). In general this electrostatic force is written as:

$$F_{ext} = \frac{1}{2} V^2(t) \frac{\partial C}{\partial z} \tag{2.6}$$

where C is the capacitance between the resonator and the driver electrode. $V(t)$ is the voltage applied between driver electrode and resonator, with AC and DC components:

$$V(t) = V_{DC} + v_{ac} \cdot \sin \omega_{ext} \tag{2.7}$$

where v_{ac} is the amplitude of the AC applied voltage.

For flexural resonators, characterized with large oscillation amplitudes, the dependence of the displacement on the capacitance can not be neglected. Then, the capacitance is function of the displacement: $C(z,t)$. Let's consider the direction along the microresonator as y, as shows figure 2.2. Then the capacitance is the integral of the deflection profile along the beam length (L):

$$C(z(t)) = \frac{C_0}{L} \int_0^L s \frac{dy}{\left(1 - \frac{z(y)}{s}\right)} \tag{2.8}$$

where C_0 is the static capacitance between resonator and driver:

$$C_0 = \frac{\epsilon_0 \cdot h \cdot L}{s} \tag{2.9}$$

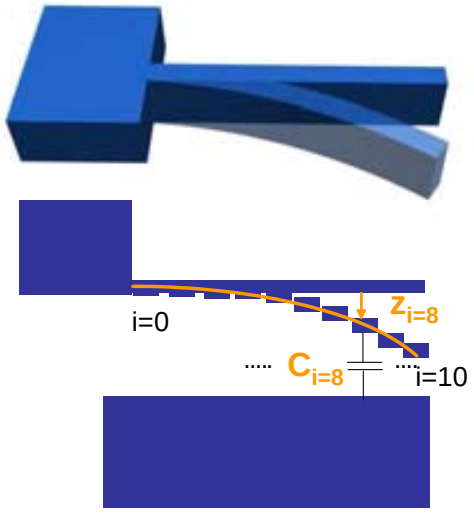


Figure 2.3: *The figure shows how the resonator (a c-f beam in this case) is sliced into* 10 *elements. The total capacitance between resonator and driver is the sum of the capacitance of each element.*

Because the profile displacement $z\,(y)$ depends on the external force, and the external force depends on the displacement profile, the profile is determined numerically by a FEM solver in static conditions. The FEM solver allows to calculate by static modelization the displacements along the direction y of the resonator. This has been done by Coventor and/or Sugar. A model of the transducer has to be designed in this FEM tools slicing the beam length L in finite lengths l_i. Each sliced element i is displaced a quantity z_i when applying an external force. In the FEM tool, a set of voltages are simulated, obtaining a matrix of displacements z_i versus z. Then, when solving equation 2.1 by numerical methods (Matlab, Spice or others), the matrix of containing z_i values is invoked.

Then, the total capacitance between driver and electrode is calculated as the addition of each sliced beam i, supposing N sliced elements. Displacements z_i are obtained from the FEM solver. The length of sliced elements, l_i, can be logarithmic in order to describe better the free end without increasing N too much. In case the spacing is linear, $l_i = \frac{L}{N}$.

Equation 2.8 can be rewritten as, substituting the integral by the sum of each capacitance to the total beam capacitance:

$$C\,(z(t)) = \frac{C_0}{L} \sum_{i}^{N} \left(\frac{l_i}{\left(1 - \frac{z_i}{s}\right)} \right) \tag{2.10}$$

The external force can be rewritten as:

$$F_{ext}(z(t),t) = \left(\frac{V^2(t)}{2}\frac{C_0}{L\cdot s}\right)\left(\sum_i^N\left(\frac{l_i\cdot z_i}{\left(1-\frac{z_i}{s}\right)^2}\right)\right) \tag{2.11}$$

When computing equation 2.1, the set of displacements previously calculated by a FEM tool are used to compute the total capacitance, and hence the total force for each time of the transient analysis. Those lateral displacements are obtained from previous calculation on a FEM solver platform, named *Sugar* [48]. Those displacements were corroborated by another FEM solver, *Coventor* [46] It shall be pointed that the matrix of values z_i is invoked by the value of the variable $z(t)$ at each time t of the simulation. So for each value of z corresponds a vector of displacements z_i. In fact the nodal displacement of each sliced element can be expressed as a function of the maximum displacement z as:

$$z_i = b_i\cdot z \qquad \forall \qquad i = 1\ldots N \tag{2.12}$$

Equations 2.10 and 2.11 are complemented by the fringing field contribution on the capacitance between resonator and electrode. Due to the proximity of the resonator with respect to the electrode, the static capacitance is enhanced due to the fringing fields that appears between both structures. The fringing field correction is modelized by an analytical equation which depends only on the cantilever driver geometry. That term is inspired from a semiempirical formulation developed to determine the fringing field contribution to adjacent lines in a CMOS circuitry [49]. Then, the total electrostatic force applied to the cantilever can be written as:

$$C_{0-ff} = C_0\times\left(1+\alpha\left(\frac{s}{h}\right)\left(\frac{b}{s}\right)^{0.222}\right) \tag{2.13}$$

Replacing C_0 for C_{0-ff} in equations 2.10 and 2.11, allows the consideration of the fringing capacitance on the modelization. Then, the term of the external forces F_{ext} takes into account the two main features previously presented: the cantilever real deflection shape and the fringing field correction. Focusing in the real deflection consideration, the model calculates the external electrical force applied to the resonator by slicing the resonator length in N components and computing the time-variable capacitance of each sliced element.

The output electrical current is also calculated when solving numerically equation 2.1. The output current is given by the equation:

$$I_0(t) = \frac{d(C\cdot V)}{dt} = V(t)\frac{\partial C(z(t))}{\partial z}\frac{dz}{dt} + C_0\frac{dV(t)}{dt} \tag{2.14}$$

where the first term takes into account the resonance current due to the movement of the resonator at resonance; the second terms takes into account the parasitic current between excitation electrode (in one-port measurement -as described in appendix B- this electrode is the resonator itself) and the readout electrode. The capacitance C_0 is the static capacitance between both electrodes. In two-port measurements (see appendix B), parasitic capacitance between resonator and readout electrode is reduced, lowering the specific weight of the parasitic current in the overall current.

2.1.1 Two-port modelization

Figure 2.4 shows a c-f resonator in a two port configuration scheme. The benefits of using a two port configuration is that the effect of the parasitic current (generated as a consequence of applying an AC voltage to driving the structure to resonance) is minimized in the output resonator current. In that case, the AC and DC voltages are applied separately in the driver electrode and resonator, respectively. The output current is collected at the readout electrode, as shows figure 2.4.

The consequences in the modelization are that the external force has two contributions, one force term for each driver, named F_{ext_1} and F_{ext^2}, that appear due to the differences of voltages between excitation driver and resonator ($V_1(t)$) and between resonator and detection electrode ($V_2(t)$).

$$\begin{aligned} F_{ext_1^2}\left(z(t),t\right) &= \left(\frac{V_{\frac{2}{1}}(t)}{2}\right)^2 \frac{\partial C_{\frac{2}{1}}}{\partial z} = \\ &= \mp\left(\frac{V_{\frac{2}{1}}(t)}{2}\right)^2 \left(\frac{C_{0-ff}}{s}\cdot\left(\sum_i^N\left(\frac{l_i\cdot z_i}{\left(1\pm\frac{z_i}{s}\right)^2}\right)\right)\right) \end{aligned} \tag{2.15}$$

l_i and b_i are the length and the normalized lateral displacement (on the lateral direction, z) of the sliced element i, respectively.

The voltages of each port, taking the configuration of figure 2.4, can be written as:

$$\begin{aligned} V_1(t) &= V_{DC} + v_{AC}\sin\left(\omega_{ext}t\right) \\ V_2(t) &= V_{DC} \end{aligned} \tag{2.16}$$

The output current is the sum of the resonance current and the parasitic current, very similar to expression 2.14. The only difference is that now, the parasitic capacitance from AC input signal to output current signal is given by the fringing capacitance between excitation and readout drivers (C_{12}), as depicted in figure 2.4.

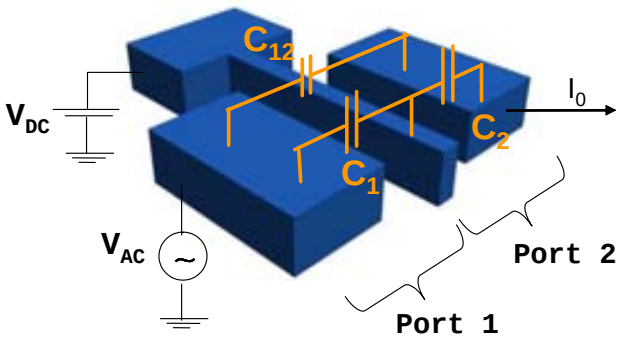


Figure 2.4: *Scheme showing a c-f beam resonator in the two port configuration. Voltages and capacitances related with each port are named C_1, V_1 and V_2 and C_2.*

$$I_0(t) = \frac{d(C \cdot V)}{dt} = V(t)\frac{\partial C(z(t))}{\partial z}\frac{dz}{dt} + C_{12}\frac{dV(t)}{dt} \tag{2.17}$$

2.1.2 Implementation in Pspice

The implementation of the previous described model in an electrical environment opens new and interesting possibilities from the modelization point of view. Despite the implementation of the model in *Matlab* platform favors a fast and dynamic implementation of the model due pre-designed functions focused on numerical methods, some difficulties arise when electrical elements are added to the transducer. An electrical environment facilitates the addition of such devices into the simulation panel as well as allows to work easily with electrical variables, as transmission magnitude and phase.

However, in order to translate the modelization to an electrical environment the following conversion from mechanical to electrical variables is needed:

$$F_{ext} \xleftrightarrow{T} U_{ext} = \frac{F_{ext}}{T} \qquad z \xleftrightarrow{\dot{T}} I_v = T \cdot \dot{z} \tag{2.18}$$

where the external force (F_{ext}) has been transformed to an external voltage in the new domain (U_{ext}), and the velocity ($\dot{z}$ has been transformed to an equivalent current (I_v). The factor which defines the transformation between the two domains is given by the equation:

$$T = \frac{C_0}{s}U_R \quad [N/V] \tag{2.19}$$

where C_0 has been defined previously in equation 2.9 and s is the lateral gap between the cantilever and the driver electrode. U_R is a transformation voltage, and is considered $U_R = 1V$. By this transformation, it is possible to obtain the electrical equivalent for the position (z) and acceleration ($\ddot{z}$):

$$z = \int_0^t \dot{z}dt = \frac{1}{T}\int_0^t I_v dt \tag{2.20}$$

$$\ddot{z} = \frac{\dot{I}_v}{T} \tag{2.21}$$

Then the mechanical equation (2.1) of the cantilever-electrodes system is rewritten to its electrical one (in the two port configuration) as:

$$L\dot{I}_v + RI_v + \frac{1}{C}\int_0^t I_v dt = U_{ext-1} + U_{ext-2} \tag{2.22}$$

These equivalent electrical parameters are the same as found in the literature [50] [51], with the voltage transformation normalized to $1V$. Defining the electrical equivalent parameters:

$$L = \frac{m_n}{T^2}; \qquad C = \frac{T^2}{k}; \qquad R = \frac{\sqrt{m_n \cdot k}}{Q \cdot T^2} \tag{2.23}$$

In fact this R is the normalized motional resistance introduced in chapter 1, equation 1.2. Starting from the above expression of R (equation 2.23), and defining the voltage reference of the translation as the DC voltage applied to the structure V_{DC}:

$$R = \frac{\sqrt{m_N \cdot k}}{Q \cdot \left(\frac{C_0 \cdot V_{DC}}{s}\right)^2} \tag{2.24}$$

Substituting $C_0 = \frac{\epsilon A}{s}$ and $\sqrt{m_N} = \frac{\sqrt{k}}{\omega_n}$ in equation 2.24, equation 1.2 is reobtained:

$$R = \frac{k}{\omega_n}\frac{s^4}{Q \cdot A^2 \epsilon_0^2} \tag{2.25}$$

In the literature, the parameter T is found as η, and is given by the following expression:

$$\eta = \frac{C_0 \cdot V_{DC}}{s} \tag{2.26}$$

In fact, the parameter T is the parameter η normalized to $V_{DC} = 1$.

The equivalent potentials U_{ext^1} and U_{ext_2} are the force applied to the resonator by each one of the drivers transformed to the electrical domain, and are obtained by combining equations 2.6, 2.18 and 2.19.

$$U_{ext_{\frac{1}{2}}^{1}}(z,t) = \mp\frac{V_{\frac{1}{2}}(t)^2}{2}\left(\frac{1}{L}\sum_{i}^{N}\left(\frac{l_i \cdot b_i}{(1 \pm b_i \cdot z/s)^2}\right)\right) \times \left(1 + \alpha\left(\frac{s}{h}\right)\left(\frac{b}{s}\right)^{0.222}\right) \tag{2.27}$$

The currents I_1 and I_2 generated at each port of the cantilever-electrodes system can be expressed as [42]:

$$I_{\frac{1}{2}}(t) = \dot{V}_{\frac{1}{2}}(t)^2\frac{C_0}{L}\sum_{i=1}^{N}\left(\frac{l_i}{(1 \pm b_i \cdot z/s)}\right) \mp I_v \cdot V_{\frac{1}{2}}(t)\frac{1}{L} \cdot \sum_{i=1}^{N}\left(\frac{l_i \cdot b_i}{(1 \pm b_i \cdot z/s)^2}\right) \tag{2.28}$$

The electrical equation of movement, equation 2.18 with the external potential term represented by equation 2.27, and the current generated at the electrodes 2.28 can be solved in the electrical design environment *Spice* [44].

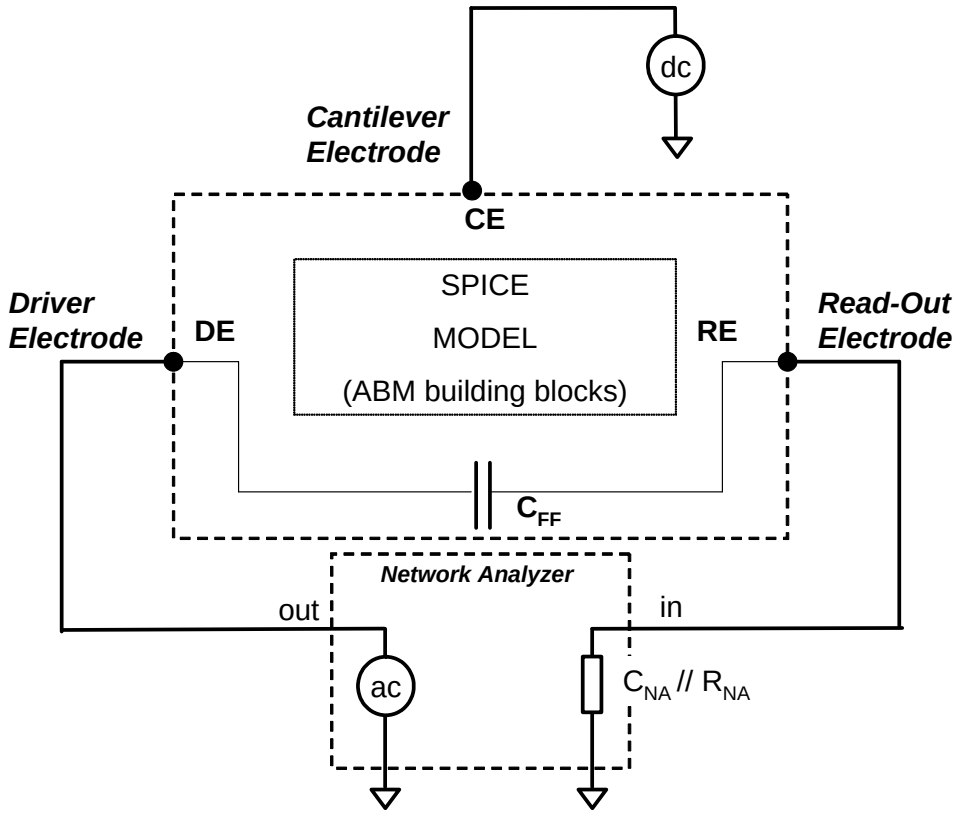


Figure 2.5: *Scheme showing the electrical connections to the driver, read-out and resonator electrodes.*

Figure 2.5 shows the electrical connections performed to each electrode in a typical two-

port configuration (see appendix B). The resonator is driven to resonance by applying an AC signal to the driver electrode combined with the DC voltage applied to the resonator electrode. The readout electrode is connected directly to the input port of the network analyzer, whose equivalent circuit is depicted in figure 2.5. The modelization takes into account the input impedance of the network analyzer port. This impedance is modelized by a resistor and a capacitor in parallel. The value of the capacitor is adjusted to reproduce the magnitude levels measured out of resonance, and the value of the resistor is fixed to be $1M\Omega$.

Figure 2.6 shows a schematic based on block diagrams of the model implemented in *Spice*. In *Spice*, the functionality of each block is implemented by Analog Building Blocks (ABM) modules, [52]. The core structure of the model is represented by the RLC branch and the lateral displacement (z) is derived from the voltage drop in the motional capacitor of this RLC branch:

$$z = \frac{V_c}{U_R}\frac{C}{C_0}s \tag{2.29}$$

where V_c can be deduced from the voltage on the capacitor:

$$V_c = \frac{1}{C}\int I_v dt \tag{2.30}$$

and equation 2.20.
This variable z feeds up the current and force modules determining the current (equation 2.28) generated at both electrodes, and the forces (equation 2.27) applied to the cantilever. The new force obtained determines the current level at the RLC branch (I_v), obtaining again a new value of the lateral displacement (z). Using this feedback, the electrical equation 2.18 is solved. The current I_v is obtained by integrating the lateral displacement as shown in equation 2.20 (as shows figure 2.6). This variable feeds the calculation of the current generated at each electrode.

Also, the module that calculates the current at each port needs the variable z and the voltage applied at the port. In the same way, the module which calculates the force (equation 2.27) has to have two inputs, z and the voltage associated to the port, as can be seen in figure 2.6. The modelization is completed by adding a capacitance between the driver and readout electrodes (named C_{12}) considering the effects of the fringing field that appears between the two ports.

2.1.3 Bulk acoustic resonators

For bulk acoustic resonators, a simplfication on computing the capacitance and the electrostatic force (equations 2.10 and 2.11) can be done as expenses of small displacements exhibit by those resonators at resonance ($10^{-9}m$ or less). Those displacements can be considered

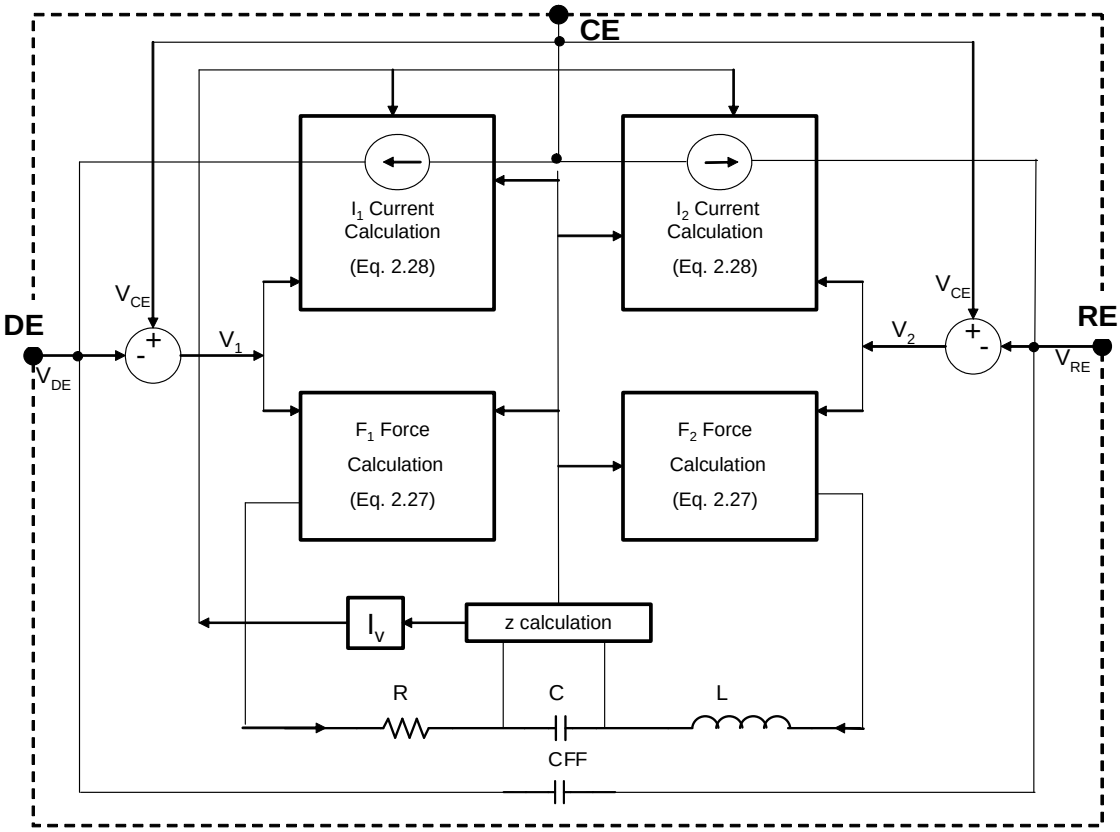


Figure 2.6: *SPICE schematics implementation of the electromechanical model equations.*

parallel between driver and electrode, yielding to simplified equations when computing the capacitance and hence, the external force. Then, the variation of the capacitance can be obtained by the following expression:

$$\frac{\partial C}{\partial z} = \frac{\partial}{\partial z}\left(\frac{\epsilon_0 A}{s-z}\right) = \frac{C_0}{s}\frac{1}{\left(1-\frac{z}{s}\right)^2} \tag{2.31}$$

where C_0 has been defined previously in equation 2.9.

The total external force and the output current are computed using equations 2.11 and 2.14, taking into account the new simplified expression for the capacitance.

2.1.4 Two-port modelization: In-Phase and Out-Phase resonance modes

Up to here, the modelization described for two-port modelization was based on a c-f beam, that in the fundamental resonating mode approaches to one driver at the same time that moves further away from the other driver. This is called an Out-Phase vibrational mode.

Then, the sign on equations envolving the electrostatic forces and the currents generated at each driver are valid. However, some resonator exhibits vibrational modes, where the resonator approaches and moves away from the two drivers at the same time: this resonating mode is named In-Phase.

For example, the paddle shaped structure, that will be analyzed in the following section 2.3, presents this In-Phase behavior when resonates in the translational mode. The resonator approaches and moves away from the driver and excitation electrodes at the same time. However, for the same resonator vibrating in the torsional mode, the resonator approaches to the excitation electrodes, and at the same time it moves away from the reading electrode, exhibiting an Out-Phase behavior. Also, a disk shaped resonator shows this duality depending whether it vibrates in the Radial Mode (In-Phase) or in the Wine-Glass Mode (Out-Phase).

In figure 2.7 is depicted a cross section of a paddle shaped resonator vibrating in the translational mode. The paddle plate approaches to the driver and sensing electrode at the same time, producing the so-called In-Phase vibrational mode.

Considering the capacitances between resonator and electrodes as plane-parallel, the capacitance and the variation of capacitance along the vertical displacement z, can be calculated by the following expressions:

$$C_{\frac{2}{1}} = \left(\frac{\epsilon_0 A}{s - z}\right) \tag{2.32}$$

$$\frac{\partial C_{\frac{2}{1}}}{\partial z} = \frac{C_0}{s} \frac{1}{\left(1 - \frac{z}{s}\right)^2} \tag{2.33}$$

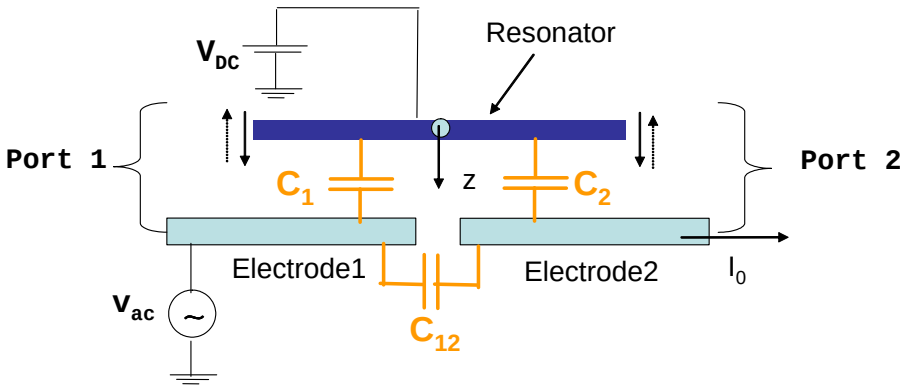


Figure 2.7: *Scheme showing the modelization of a paddle vibrating in the translational (In-Phase) mode.*

The mechanical current I_o will be given by the sum of the parasitic current and the resonance current generated between resonator and read-out electrode:

$$I_o = V_2(t)\frac{\partial C_2(t)}{\partial^o t} + C_{12}\frac{\partial V_1(t)}{\partial t} \tag{2.34}$$

2.2 Flexural modes in beams

This section will start deriving the natural vibrational modes of beams with different boundary conditions, the c-f beam and the c-c beam, shown in figure 2.8.

The free resonance modes are given in all cases by the Euler-Bernouilli equation. Eliminating the external force term, the Euler-Bernouilli equation is written as follows:

$$E \cdot I \cdot \frac{\partial^4 z(y,t)}{\partial^4 y} + \rho \cdot h \cdot w\frac{\partial^2 z(y,t)}{\partial t^2} = 0 \tag{2.35}$$

where E and ρ are the Young's modulus and mass density of the beam material.

The solution of equation 2.35, $z(y,t)$, can be written as the product of one function that depends on the displacement z along the axis direction y and another function time depending, i.e:

$$z\,(y,t) = z(y) \cdot [cos\,(\omega_n \cdot t + \theta)] \tag{2.36}$$

Then, the deflection profile is separated from its dependence on time. Replacing the equation 2.36 on the equation 2.35, we obtain:

$$\frac{\partial^4 z(y)}{\partial y^4} = \omega_n^2\frac{\rho \cdot h \cdot w}{E \cdot I}z(y) \tag{2.37}$$

The subindex n denotes the n vibrational mode of the resonator.

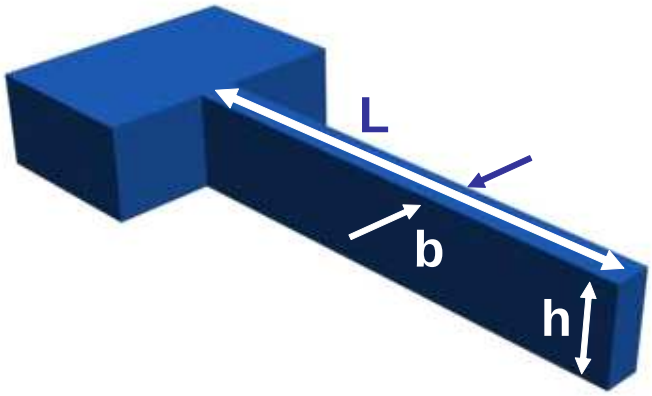
Defining the parameter κ:

$$\kappa_n^4 = \omega_n^2\frac{\rho \cdot h \cdot w}{E \cdot I} \Longleftrightarrow \omega_n = \kappa_n^2\sqrt{\frac{E \cdot I}{\rho \cdot h \cdot w}} \tag{2.38}$$

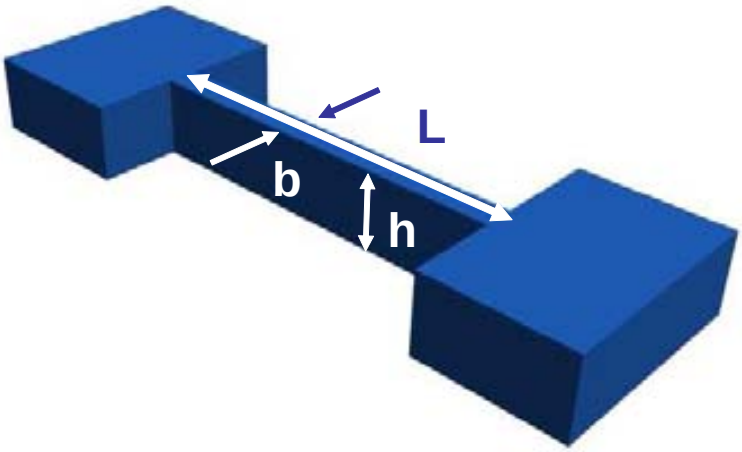
where I is the moment of inertia of the beam; for an oscillating beam vibrating in-plane, the moment of inertia can be written as:

$$I = \frac{h \cdot b^3}{12} \tag{2.39}$$

For oscillating beams in the vertical plane, the moment of inertia would be $I_{vertical} = \frac{b \cdot h^3}{12}$, just replacing b by h and viceversa.



(a) Scheme of a clamped-free beam



(b) Scheme of a clamped-clamped beam

Figure 2.8: *c-f and c-c flexural beam resonators showing their characteristic dimensions. The resonators are designed to resonate in-plane.*

When applying the boundary conditions to equation 2.36, the constant κ_n is obtained in normalized in terms of the beam length L. Then, taking into account equation 2.39 and replacing κ_n by $\kappa_n L$ in equation 2.38, the resonance frequency of the mode n is given by:

$$\omega_n = (\kappa_n L)^2 \sqrt{\frac{E \cdot b^3}{12 \cdot \rho \cdot b \cdot L^4}} \tag{2.40}$$

Then, equation 2.37 can be rewritten as:

$$\frac{d^4 z(y)}{dy^4} = \kappa_n^4 \cdot z(y) \tag{2.41}$$

The general solution of equation 2.41 can be written as:

$$z(y) = A_n \sin(\kappa_n \cdot y) + B_n \cos(\kappa_n \cdot y) + C_n \ \sinh(\kappa_n \cdot y) + D_n \cosh(\kappa_n \cdot y) \tag{2.42}$$

where A_n, B_n, C_n and D_n are integration constant that have to be determined from the boundary conditions.

Equation 2.42 will give the deflection profile for the n resonating mode and equation 2.38 will give the resonance frequencies for the n-mode. In the following, a numerical solution for the coefficients and resonances frequencies for the fourth first modes will be calculated for the c-f beam and c-c beam.

2.2.1 The flexural c-f beam

Before starting with the calculation of the natural frequencies of a c-f beam, the equivalent spring constant of the device will be given. The calculation of the structure spring constant is done starting from the Hook's law and calculating the bending in the free end when an external force is applied. The result is expressed as [53]:

$$k_{cf} = 3\frac{E \cdot I}{L^3} = \frac{E \cdot h \cdot b^3}{4 \cdot L^3} \tag{2.43}$$

Considering equation 2.43, the equation of the resonance modes 2.40 can be rewritten as:

$$\omega_{n-cf} = \frac{(\kappa_n L)^2}{\sqrt{3}} \sqrt{\frac{k_{cf}}{m_0}} \equiv \sqrt{\frac{k_{cf}}{m_{n-cf}}} \tag{2.44}$$

where m_0 is the static mass of the beam and m_{n-cf} is the effective mass of the beam in the clamped-free configuration, that depends of the resonant mode (n) by the expression:

$$m_{n-cf} = \frac{3}{(\kappa_n \cdot L)^4} m_0 \tag{2.45}$$

In order to derive the relationship between the natural frequencies of a c-f beam, it is necessary to know the boundary conditions. For a cantilever, one end is clamped ($y = 0$) and the other end is free ($y = L$). This implies that the displacement at the clamped end has to be zero as well as its first derivative. Besides, zeros at the curvature (second and third derivatives) at the free end ($y = L$) give the third and fourth boundary conditions.

$$z(y=0)=0 \quad \left.\frac{\partial z}{\partial y}\right|_{y=0}=0 \quad \left.\frac{\partial^2 z}{\partial^2 y}\right|_{y=L}=0 \quad \left.\frac{\partial^3 z}{\partial^3 y}\right|_{y=L}=0 \tag{2.46}$$

Substituting the first and second boundary conditions (equation 2.46) in equation 2.42 two relationships between the integration constants A_n, B_n, C_n and D_n are obtained:

$$\begin{aligned} B_n &= -D_n \\ A_n &= -C_n \end{aligned} \tag{2.47}$$

The third and fourth row of 2.46 gives:

$$\begin{aligned} 0 &= A_n\left(-\sin(\kappa_n\cdot l)-\sinh(\kappa_n\cdot l)\right)+B_n\left(-\cos(\kappa_n\cdot l)-\cosh(\kappa_n\cdot l)\right) \\ 0 &= A_n\left(-\cos(\kappa_n\cdot l)-\cosh(\kappa_n\cdot l)\right)+B_n\left(\sin(\kappa_n\cdot l)-\sinh(\kappa_n\cdot l)\right) \end{aligned} \tag{2.48}$$

Combining these two equations a relationship between both coefficients A_n and B_n is obtained.

$$\frac{A_n}{B_n}=-\frac{\cos(\kappa_n\cdot l)+\cosh(\kappa_n\cdot l)}{\sin(\kappa_n\cdot l)+\sinh(\kappa_n\cdot l)}=\frac{\sin(\kappa_n\cdot l)-\sinh(\kappa_n\cdot l)}{\cos(\kappa_n\cdot l)+\cosh(\kappa_n\cdot l)} \tag{2.49}$$

Combining the term on the right of this last equation 2.49:

$$0=1+\cos(\kappa_n\cdot l)\cosh(\kappa_n\cdot l) \tag{2.50}$$

where $\kappa_n L$ is calculated numerically from last equation 2.50. Numerical solutions have been calculated, obtaining:

$$\kappa_n\cdot L = 1.87510 \quad 4.69409 \quad 7.85475 \tag{2.51}$$

From equation 2.49, the relationships between A_n and B_n for the first four modes are obtained.

$$\frac{A_n}{B_n}=-0.734092 \quad -1.01846 \quad -0.999224 \tag{2.52}$$

Constants C_n and D_n are obtained from the relationships in 2.47. The profile is calculated from equation 2.42 taking into account equation 2.47 and solutions expressed in equation 2.52:

$$z(y) = A_n \left[(\sin(\kappa_n \cdot y) - sinh(\kappa_n \cdot y)) + \frac{B_n}{A_n} (\cos(\kappa_n \cdot y) - \cosh(\kappa_n \cdot y)) \right] \tag{2.53}$$

One constant is still present in equation 2.53. When drawing the deflected profile of a c-f beam, the displacement at the free end ($y = L$) is given by B_n:

$$z(y)\Big|_{y=L} = B_n \tag{2.54}$$

2.2.2 The flexural clamped-clamped beam

In order to derive the vibrational modes of a clamped-clamped beam a similar procedure than in previous section is followed. For a clamped-clamped beam resonating in-plane, the spring constant is [54]:

$$k_{cc} = 16 \frac{E \cdot h \cdot b^3}{L^3} \tag{2.55}$$

Considering equation 2.55, the equation of the resonance modes 2.40 can be rewritten as:

$$\omega_{n-cc} = \frac{(\kappa_n L)^2}{\sqrt{192}} \sqrt{\frac{k_{cc}}{m_0}} \equiv \sqrt{\frac{k_{cc}}{m_{n-cc}}} \tag{2.56}$$

where m_0 is the static mass of the beam and m_{n-cc} is the effective mass of the beam in the clamped-clamped configuration:

$$m_{n-cc} = \frac{192}{(\kappa \cdot L)^4} m_0 \tag{2.57}$$

For a c-c beam, the boundary conditions applied to both ends ($y = 0$ and $y = L$) are: no displacement for z and neither its first derivative is allowed in $y = 0$ and $y = L$.

$$z(y=0) = 0 \quad z(y=L) = 0 \quad \frac{\partial z}{\partial y}\Big|_{y=0} = 0 \quad \frac{\partial z}{\partial y}\Big|_{y=L} = 0 \tag{2.58}$$

Applying those conditions (equation 2.58) on equation 2.42 in a similar way than for the c-f beam, the characteristic $\kappa_n L$ values are obtained:

$$\kappa_n \cdot L = 2.365 \quad 3.927 \quad 5.4978 \quad 7.069 \tag{2.59}$$

The profile for a c-c beam is given by the equation:

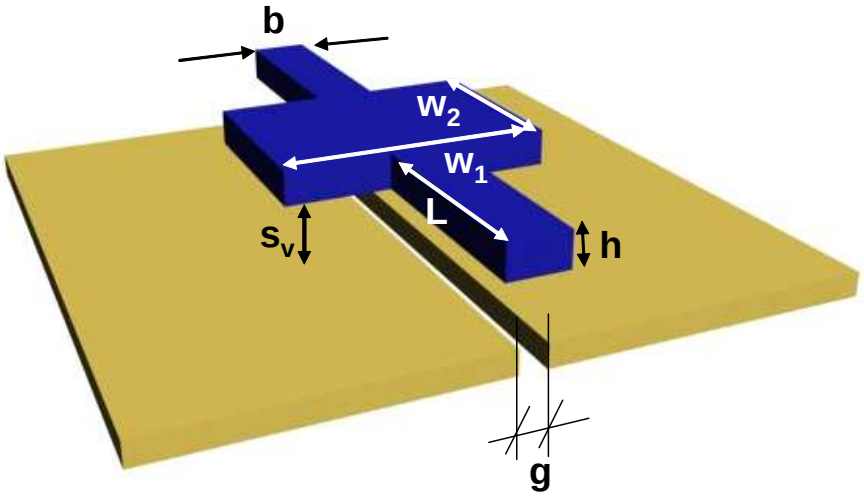


Figure 2.9: *Three dimensional scheme of a paddle shaped mechanical resonator with the two driver and sensing electrode.*

$$z(y) = A_n \left(\cos\left(\kappa_n \cdot y\right) - \cosh\left(\kappa_n \cdot y\right)\right) - \frac{\cos(\kappa_n L) - \cosh(\kappa_n L)}{\sin(\kappa_n L) - \sinh(\kappa_n L)} \cdot \left(\sin\left(\kappa_n \cdot y\right) - sinh\left(\kappa_n \cdot y\right)\right) \tag{2.60}$$

2.3 Torsional-Translational resonators. The paddle structure

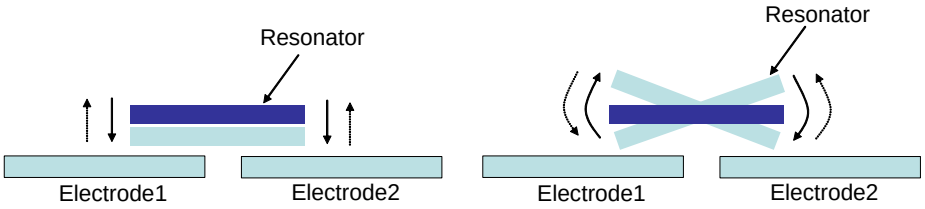
A paddle shaped structure is drawn in figure 2.9. The paddle is characterized by their plate dimensions, w_1 and w_2, the width and length of the arm, b and L, its thickness h and the vertical distance to the resonator. In figure 2.9, two electrodes are drawn below the resonator; one electrode serves as driver electrode exciting asymmetrically the resonator to promote the torsional mode whereas the second electrode collects the resonating current. Both electrodes are separated by a lateral distance g.

The paddle resonator presents two flexural modes, the translational mode and the torsional resonating mode. Those two flexural modes are depicted in figure 2.10.

The translational frequency mode is calculated by the equation [55]:

$$f_{TRA} = \frac{1}{2\pi}\sqrt{\frac{k}{M}} \tag{2.61}$$

where k and M are the spring constant and effective mass of the translational mode; the spring constant is given by the equation:



(a) Translational vibrational mode (b) Torsional vibrational mode

Figure 2.10: *Translational and torsional vibrational modes of a paddle resonator.*

$$k = 2\frac{Ebh^3}{L^3} \tag{2.62}$$

resulting the frequency of the translational mode:

$$f_{TRA} = \frac{1}{2\pi}\sqrt{2\frac{Ebh^3}{ML^3}} \tag{2.63}$$

The frequency of the torsional mode is given by the equation:

$$f_{TOR} = \frac{1}{2\pi}\sqrt{\frac{\kappa}{I}} = \sqrt{\frac{3}{\pi^2}\frac{\kappa}{\rho w_2 h w_1^3}} \tag{2.64}$$

where I is the moment of inertia of the paddle and κ is the combined restoring elastic constant for the two arms. The constant κ can be found in [56]:

$$\kappa = 2\beta\left(\frac{h}{b}\right)\frac{hb^3}{L}G \tag{2.65}$$

where $\beta\left(\frac{h}{b}\right)$ is a function that varies slowly with the relation b/h, and G is the shear modulus of the resonator structural material.

2.4 Longitudinal Bulk Acoustic Resonators

The longitudinal bulk acoustic cantilever was firstly proposed as resonator by Mattila *et al.* [50], possibly inspired by the bulk acoustic modes observed by Nguyen and previously published [57]. Figure 2.11 shows the bulk acoustic cantilever resonator and its characteristic dimensions.

In its first bulk acoustic mode, the resonator vibrates on the lateral length extensional mode. The two arms of the resonator move in anti-phase decreasing the anchoring losses. The first mode is achieved when the length of the resonator L equals a quarter of the wavelength of the bulk acoustic wave:

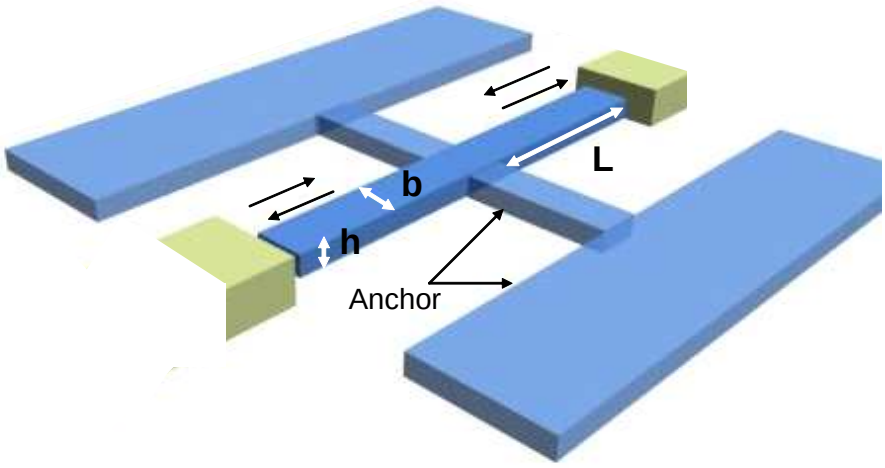


Figure 2.11: *Longitudinal Bulk Acoustic Resonator, showing its characteristic dimensions, length (L), width (b), and thickness (h). The arrows described the phase movement of each arm.*

$$f_{LBAR} = \frac{1}{4L} \cdot \sqrt{\frac{E}{\rho}} \tag{2.66}$$

where the second term $(\frac{E}{\rho})$ corresponds to the speed of sound on the structural material.

Sometimes, it is taken into account the Poisson ratio in the above equation 6.1, then the resonance frequency is given by:

$$f_{LBAR} = \frac{1}{4L} \cdot \sqrt{\frac{E}{\rho\,(1-\sigma^2)}} \tag{2.67}$$

The spring constant and the effective mass on the bulk mode are written as [58]:

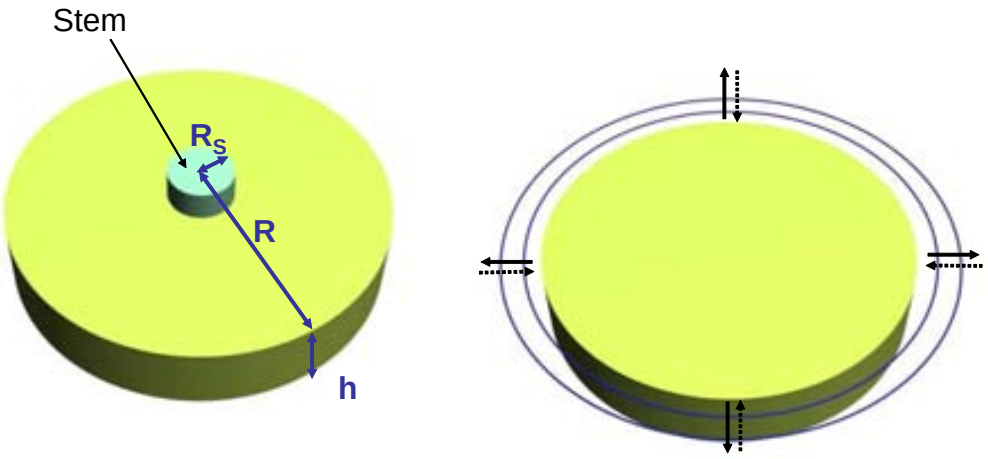
$$k_{LBAR} = \frac{\pi^2}{8}\frac{Ehb}{L} \tag{2.68}$$

$$m_{LBAR} = \frac{\rho bhL}{2} \tag{2.69}$$

2.5 Disk-shaped resonators in Radial Mode

Disk shaped resonators were first introduced by Nguyen *et al.* [57]. Figure 2.12 shows a disk shaped resonator supported by a central stem and a sketch of its bulk radial resonance mode.

In the radial bulk acoustic mode, the shape of the disk expands equally in all the lateral surface, promoting an infinitesimal nodal point in the disk center.



(a) Disk shaped resonator supported by a stem (b) Radial bulk resonance mode (first mode)

Figure 2.12: *Disk shaped resonator showing the radial bulk acoustic mode.*

The resonance frequency for the radial bulk acoustic mode is given by the following equation expressed in terms of Bessel functions [59]:

$$\frac{\delta_{rdm} J_0\left(\delta_{rdm}\right)}{J_1\left(\delta_{rdm}\right) - (1-\sigma)} = 0 \tag{2.70}$$

where J_0 and J_1 are the Bessel functions of the first kind of zero and first order, respectively.

The relation between the disk radius, R, and the variable δ_{rdm} is given by:

$$\delta_{rdm} = R\frac{2\pi f_0 \sqrt{\rho(1-\sigma^2)}}{E} \tag{2.71}$$

The effective mass is calculated by the equation:

$$m = \frac{2\pi\rho h_{rdm} \int_0^R r dr \left(J_1\left(h_{rdm} r\right)\right)^2}{\left(J_1\left(h_{rdm} R\right)\right)^2} \tag{2.72}$$

where h is the resonator thickness and h_{wgm} is given by the equation:

$$h_{rdm} = \sqrt{\frac{\left(2\pi f_0\right)^2 \rho}{\frac{2E}{2+2\sigma}} + \frac{E\sigma}{1-\sigma^2}} \tag{2.73}$$

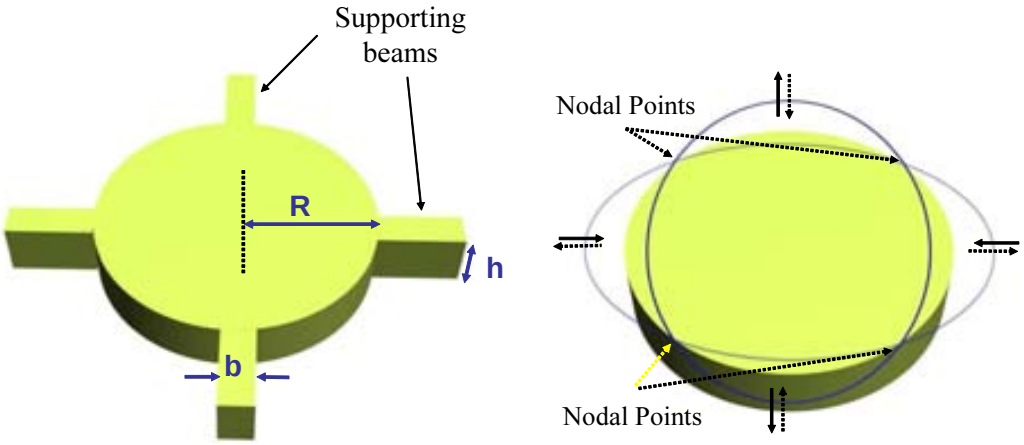
The elastic constant is derived from the effective mass and the resonance frequency:

$$k = m\,(2\pi f_0)^2 \tag{2.74}$$

Solving equation 2.70 numerically, different δ_{rdm} values are obtained; those values corresponds to the different bulk acoustic readial modes. Those values are depicted in the summary table 2.1.

2.6 Disk-shaped resonators in *Wine-Glass* Mode

Disk-shaped resonators have another bulk vibration mode, close in frequency range to the radial vibrational one, as shows figure 2.13. The vibrational mode (see figure 2.13(b)) consists on the expansion and contraction of the contour shape of the disk, conforming 4 nodal edges on the structure, forming two alternate and perpendicular ellipses per cycle of vibration. Typically, this is the main resonant mode expected when anchoring the disk-shaped resonator by different beams on the edge.



(a) Disk shaped resonator supported by 4 lateral beams

(b) *Wine-Glass* resonance mode (first mode)

Figure 2.13: *Disk shaped resonator showing the wine-glass mode.*

The frequency equation is written as follows:

$$\left[\frac{\frac{\delta}{\xi}J_1\left(\frac{\delta}{\xi}\right)}{J_2\left(\frac{\delta}{\xi}\right)} - 2 - \frac{2\delta^2}{2n^2-2}\right]\left[2\frac{J_1(\delta)}{J_2(\delta)} - 2 - \frac{2\delta^2}{2n^2-2}\right] - \left(n\frac{2\delta^2}{2n^2-2} - n\right)^2 = 0 \tag{2.75}$$

where δ_{wgm} is the variable of the equation and it is related with the disk radius (R), as:

$$\delta_{wgm} = R\frac{2\pi f_0\sqrt{\rho(1-\sigma^2)}}{E} \tag{2.76}$$

and ξ is a constant:

$$\xi = \sqrt{\frac{2}{1-\sigma}} \tag{2.77}$$

Equation 2.75 is solved numerically by a program implemented in *Matlab*, which calculates the zeros for the n-radial mode.

$$\delta_{wgm} = \frac{R\,(2\pi f_0)\left(\sqrt{\rho(1-\sigma^2)}\right)}{E} \tag{2.78}$$

In order to calculate the equivalent RLC model, the effective mass has to be calculated. In the *Wine-Glass Mode*, the effective mass is given by the equation:

$$m_{eff} = \frac{\pi\rho h \int_0^R r dr \frac{\delta_{wgm}}{2\xi R}\left(J_1\left(\frac{r\delta_{wgm}}{R\xi}\right) - J_3\left(\frac{r\delta_{wgm}}{R\xi}\right) + \frac{2\times BA}{R}J_2\left(\frac{r\delta_{wgm}}{R}\right)\right)^2}{\frac{\delta_{wgm}}{2\xi R}\left(J_1\left(\frac{\delta_{wgm}}{\xi}\right) - J_3\left(\frac{\delta_{wgm}}{\xi}\right)\right) + \frac{2}{R}BAJ_2(\delta_{wgm})} \tag{2.79}$$

The spring constant is calculated by the equation:

$$k = (2\pi f_0)^2\, m \tag{2.80}$$

BA is a numeric constant and its value is $BA = -4.5236$ [60].

2.7 Ring-shaped resonators

A ring resonator is a bulk mode resonator defined by the geometry described in figure 2.14.

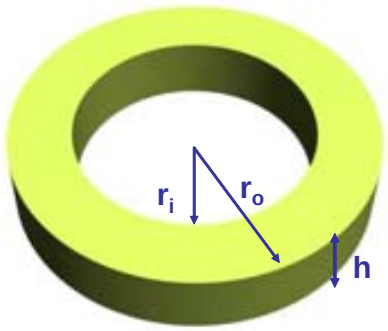


Figure 2.14: *Ring shaped resonator showing its dimensions.*

A ring-shaped resonator presents a clear advantage respect to the disk shaped resonator. Whereas in the disk the radius dimensions is inversely proportional to the resonance frequency,

in the ring the resonance frequency is proportional to the difference of inner and outer radius. This fact allows to fabricate resonators at RF frequencies ($1GHz$ and above) without losing coupling area, electromechanical current, and hence power management.

The frequency of the first bulk resonating mode is given by the equation [82], [61]:

$$\begin{aligned}&[J_1(h_{ring}r_i)\sigma - J_1(h_{ring}r_i) + r_i h_{ring} J_0(h_{ring}r_i)] \cdot [Y_1(h_{ring}r_o)\sigma - Y_1(h_{ring}r_o) + r_0 h Y_0(h_{ring}r_o)] \\ &- [Y_1(h_{ring}r_i)\sigma - Y_1(h_{ring}r_i) + r_i h Y_0(h_{ring}r_i)] \cdot [J_1(h_{ring}r_o)\sigma - J_1(h_{ring}r_o) + r_o h_{ring} J_0(h_{ring}r_o)] = 0\end{aligned} \tag{2.81}$$

where h_{ring} is a constant that depends on the target resonance frequency and the mechanical properties of the structural material as:

$$h_{ring} = \frac{2\pi f_0}{\sqrt{\frac{E}{\rho(1-\sigma^2)}}} \tag{2.82}$$

where f_0 is the ring resonance frequency and E, ρ and σ are the structural material Young's modulus, mass density and Poisson's ratio (σ), respectively. Inner and outer annular ring radiuses are represented by r_i and r_o, respectively.

A program *Matlab*-based was designed in order to facilitate those calculations in the design step. The program solves graphically and numerically equation 2.81.

Once the material properties of the structural layer (Young's modulus (E), mass density (ρ) and Poisson ratio (σ)) are defined, the variables in equation 2.81 reduces to three: inner radius (r_i), outer radius (r_o) and resonance frequency (f_0). Then, two variables are needed and the third one is given by numerically solving equation 2.81.

For a desired resonance frequency and a chosen inner radius, the outer radius is calculated numerically by equation 2.81. Because of the inherent cyclic behavior of Bessel functions [59], equation 2.81 will produce different values for the variable r_0 that would equal to zero the equation. Hence, multiple solutions (values of r_0) will accomplish the resonating mode of equation 2.81 for a desired frequency and inner radius (r_i).

An example of the multiple solutions given by equation 2.81 is shown in figure 2.15. On that case, the target frequency was $f_0 = 1GHz$ and inner radius was $r_i = 5\mu m$; the material constants were $E = 110GPa$, $\rho = 2.23 \times 10^3 kg/m^3$ and $\sigma = 0.2$. The first solution given graphically is a trivial solution of equation 2.81, $r_i = r_o$. The second solution gives a zero to the equation between $8\mu m$ and $10\mu m$. Numerically, the solution is obtained at $8.66\mu m$.

The ring with the completed design has been simulated by the FEM tool, *Coventor*. The material parameters have been chosen the same as before and a modal analysis has been performed near the target frequency. The bulk acoustic mode of the ring shows a nodal circle on the inner part of the ring that remains immovable whereas the inner and outer shapes are

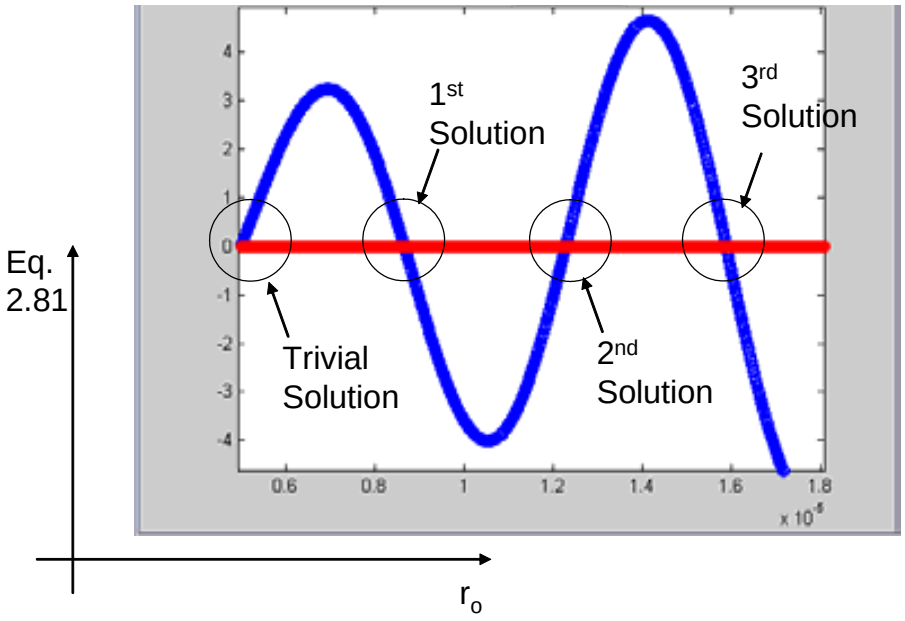


Figure 2.15: *Graphical solution of equation 2.81 for the given parameters:* $E = 110GPa$, $\rho = 2.23 \times 10^3 kg/m^3$, $\sigma = 0.2$, *target frequency* $f_0 = 1GHz$ *and inner radius* $r_i = 5\mu m$. *The first solution is* $r_o = 8.66\mu m$.

deformed by the resonating movement. The result of the modal analysis is shown in figure 2.16. The simulated resonance frequency is $1.04GHz$.

2.8 Square-shaped resonators

A scheme of a squared shaped resonator is depicted in figure 2.17. The square resonator is supported by 4 beams, one in each corner of the device. This square resonator presents two kinds of resonances [62]: the *Lamé* mode, where two opposites edges of the resonator move in out-of-phase with respect the others two edges, and the extensional mode, where the four edges move in phase preserving the square shape of the resonator. The extensional mode can be approximated as a superposition of two orthogonal sound waves with displacements given by $u_x = Asinxx/L$ and $u_y = Asinxy/L$, where A is the vibration amplitude and x and y indicate the position on the plate.

The effective mass and effective spring constant are related to the device geometry by the following equations:

$$m = \rho h L^2 \tag{2.83}$$

$$k = \pi^2 E_{2D} h \tag{2.84}$$

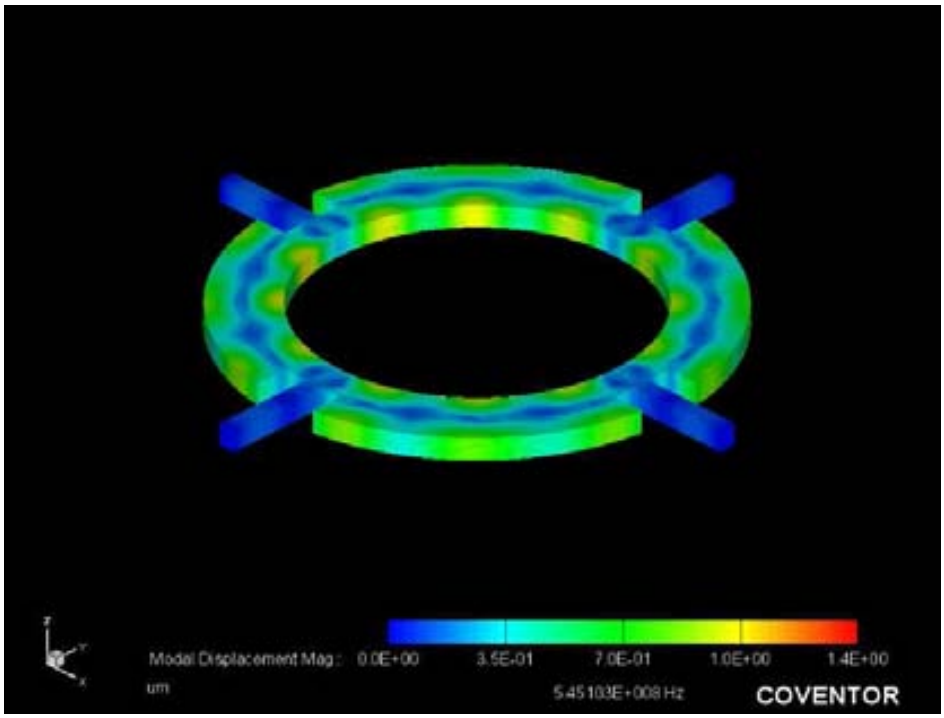


Figure 2.16: *Ring bulk resonance mode obtained by Coventor. The material parameters and dimensions are:* $E = 110GPa$, $\rho = 2.23 \times 10^3 kg/m^3$, $\sigma = 0.2$, *target frequency* $f_0 = 1GHz$, *inner radius* $r_i = 5\mu m$, *and outer radius* $r_o = 8.66\mu m$.

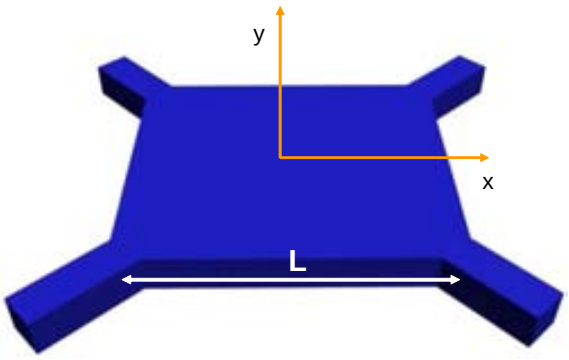


Figure 2.17: *Square shaped resonator supported by* 4 *beams at its corners.*

where ρ is the structural layer density, h is the device height, and E_{2D} is the effective elastic modulus for the 2-D expansion. This effective elastic modulus can be pondered by the mechanical stiffness of the material by the equation:

$$E_{2D} = c_{11} + c_{12} - 2\frac{c_{12}^2}{c_{11}} \tag{2.85}$$

where c_{11} and c_{22} are the mechanical stiffness in the two perpendicular directions of the square plate.

2.9 The Q-factor

The Q-factor is a relevant parameter in the microresonator modelization that accounts for the losses produced by non-conservative forces. In addition to that, high quality factors are essential for improving electrical functionalities in RF applications. The quality factor is determined by the energetic losses produced in the vibrational state of the microresonator, and those mechanism of dissipation are different in air or fluidics ambient than in vacuum. The Q-factor is limited by a set of loss mechanisms, as shown in equation 2.5, and hereby rewritten:

$$\frac{1}{Q_{Total}} = \frac{1}{Q_{Air-Damping}} + \frac{1}{Q_{Air-Squeezing}} + \frac{1}{Q_{Anchor}} + \frac{1}{Q_{surface}} + \frac{1}{Q_{TED}} \tag{2.86}$$

In the following, it is presented an overview of the main losses mechanisms in beam resonators and some expressions will be described in order to predict approximately its value. However, due to the most studied case found in literature is for the c-f beam, some expressions are limited to be extrapolated for studying the loss mechanisms in bulk acoustic resonators.

2.9.1 Losses in air

Traditionally, losses in air represent the cycle energy that losses the resonator in its vibrational state when removing the air surrounding it. In addition to that, for capacitive readout and electrostatic excited resonators, an additional term of losses in air has to be considered as a consequence of the presence of a close wall to the resonator.

The first contribution is named air-damping and the second one receives the name of squeeze damping.

The air-flow around the oscillator is described by the Navier-Stokes equation. However, there is no analytical solution for such equation and beam shapes. Hosaka et al. [63] solved analytically the Navier-Stokes equation, approaching the beam shaped resonator to a sphere, obtaining an analytical solution. The losses due to the air damping are expressed as:

$$Q^{-1} = \frac{\rho h^2 b \omega_n}{\beta} \tag{2.87}$$

where β is a parameter that depends on the fluid characteristics:

$$\beta = 3\pi\mu h + \frac{3}{4}\pi h^2 \left(2\rho_f \mu \omega_n\right)^{\frac{1}{2}} \tag{2.88}$$

When an oscillator is placed close to a rigid wall, a new air flow force, the squeeze force, appears due to the gap between the oscillator and the driver wall. This force can be calculated by the *Reynolds* equation [63]. Solving that equation and considering that the resonator length is much bigger than the width, an approximation to the damping factor can be derived [63]:

$$Q^{-1} = \frac{\rho s^3 h \omega_n}{\mu b^2} \tag{2.89}$$

where ρ, μ are the resonator mass density and the fluid viscosity, and s is the lateral distance between the resonator and the electrode. In principle, equation 2.89 can be applied to any resonator that accomplish those conditions.

However, for a beam operating in vacuum, the sources of dissipation are reduced to anchor losses, surface effects and thermoelastic dissipation. In the following, the discussion will be focused on those effects for microresonators, and especially for in-plane resonators.

2.9.2 Suport losses

Several works have pursued the calculation of the quality factor due to anchor losses. The clamped-free beam is the most studied case due to its relevance and applications possibilities in the sensor field. First works established that the anchoring losses of a clamped-free beam could be calculated by the expression [63], [64]:

$$Q_{c-f}^{-1} \alpha \left(\frac{h}{L}\right)^3 \tag{2.90}$$

where h is the thickness and L is the length of the beam.

However, that equation did not consider the bending moment contribution to the total losses. Considering this effect, the width appears on the following equation [65]:

$$Q_{c-f}^{-1} = A_{c-f} \left(\frac{w}{L}\right) \left(\frac{h}{L}\right)^4 \tag{2.91}$$

where A is a numerical coefficient that depends weakly on the Poison's ratio σ and is 0.31 for $\sigma = 0.3 - 0.25$.

This formulation can be extended to the case of a clamped-clamped beam (c-c), just replacing the constant A_{c-f} in equation 4.21 by:

$$A_{c-c} = 2A_{c-f}\frac{\left(\beta_n\left(k_nL\right)^2\right)^2_{c-c}}{\left(\beta_n\left(k_nL\right)^2\right)^2_{c-c}} \tag{2.92}$$

where coefficients β_n and eigenvalues k_nL have been previously derived and calculated in this chapter for both cases, i.e, the c-f and c-c beams. For the fundamental mode, the relationship between both constants is: $A_{c-c} = 145.1 \cdot A_{c-f}$.

2.9.3 Surface effect

Surface effects as losses mechanism on MEMS resonators has been previously reported [66], [67], [68]. However, the absence of theoretical studies makes very difficult to predict the quality factor due to those losses mechanism. On the other hand, several works have been published in order to control the surface of such microresonators in order to enhance the measured quality factor [69].

Losses due to surface effects can be semiempirically calculated by the following equation [66]:

$$Q^{-1}_{empirically} = \gamma\frac{S}{V} \tag{2.93}$$

where γ is a parameter empirically obtained from fitting experimental data to equation 2.93.

Losses due to surface-volume ratio can be explained by surface mechanical dissipation originating from a thin layer of adsorbates on the structural layer surface or by plasma damage produced on the surface in Reactive Ion Etching (RIE) dry etching processes. On that case, the damage is localized, basically, on the sidewalls of the patterned structure, due to the protecting layer (photoresist, oxide layer, metal layer).

It has been experimentally demonstrated that the quality factor can be increased by a rapid thermal annealing with temperatures ranging from 600^oC to 800^oC in short periods of time ($30s$) after the fabrication process [66]. However, immediately after annealing, Q decreases continuously over a long period of time (several months). After that time the quality factor is stabilized in stationary value, that is a factor 3 the factor measured after fabrication.

From those experiments is derived the surface mechanism loss of two types: surface loss due to plasma damaging that is repaired in the annealing process and surface losses (time-dependent) due to an adsorbate layer on top of the silicon layer that is removed in the annealing, but grows as soon as the annealing process is finished, decreasing constantly the measured Q value.
From the structural point of view, the plasma damaging is similar to the ion implantation damage. Assuming an Arrhenius relaxation of defects [67], the relaxation time τ needed to anneal a certain defect with a barrier height of V is related to annealing temperature T by:

$$\tau = \tau_o e^{\left(\frac{V}{k_BT}\right)} \tag{2.94}$$

where τ_0 and k_B are a time constant of defects and Boltzmann's constant, respectively. That equation refers that for annealing a defect, more temperature implies less annealing time and vice versa. Furthermore, the annealing process reduces the stress on silicon layers, increasing the Q-factor.

From the time-dependent surface losses, some authors [67], associate this losses to surface contamination of monolayer of unknown substances in either air ambient or vacuum conditions. The time dependent loss is reversible upon each anneal at 800^oC . This phenomenon may be explained by absorption of water, oil, hydrocarbons or even metallic particles. Annealing would either desorbate particles or dissociate them to form stable particles, such as oxides and silicides, removing the source of mechanical losses at the surface. Some fraction of those contaminants are weakly bonded, and are ready to desorbate into vapor phase at moderately high temperatures ($200^oC - 300^oC$).

In ref. [69] Yang et al. found that Q decreased significantly one month after annealing. They also found that exposure to atomic hydrogen as a method to terminate silicon surface preserved the Q to some extent. In [70], Henry et al. reported some kind of surface chemical dissipation on the atomic scale may be the cause of surface dissipation. Althoug those observations are consistent with surface contaminations, it can not be excluded the possibility of some kind of reversible structural aging effect at the surface upon annealing. It was reported in [70] that the time dependence persisted even in 10^{-8}-torr vacuum. In addition to that, Liu et al [67] grew a thin silicon dioxide layer ($50nm$ and $100nm$) on top of a silicon surface and did not observe any change on the measured quality factor.

Indistintevely of the nature of the contaminants on the surface of silicon resonators, it is concluded that those losses induced at the surface of the resonator increases as the surface to volume ratio increases [67], [68], [66].

In order to study the losses mechanism with surface related effects, anchoring related losses have to be neglected. For this reason, experiments have to be carried out when anchoring losses do not affect the system. For example, let's consider a c-c beam for demonstrating purposes. If anchoring losses are present a variation on the quality factor is produced when reducing the resonator length. In general, the anchoring losses are evident when the bridge length is comparable to its width and to the dimensions of the clamping supports. For c-c beams with $L > 30\mu m$, the intrinsic quality factor is independent of L, then losses are due to surface to volume effect and to thermoelastic damping. If the material is thick enough, then losses are mainly due to thermoelastic effects, obtaining quality factors in the range $10^5 - 10^6$ and above. In order to study the energy dissipated and only related to surface to volume ratio, the thickness of the resonator is decreased considerably below its width and length, maintaining the length of the resonator above $L > 30\mu m$ (by equation 4.21, anchoring losses is strongly dependent on the resonator length, L). A published work [66] considered c-c beams, with $L > 30\mu m$, $10\mu m$ wide and thicknesses in the range $< 1\mu m$ down to $100nm$.

Results are reproduced here and shown in figure 2.18.

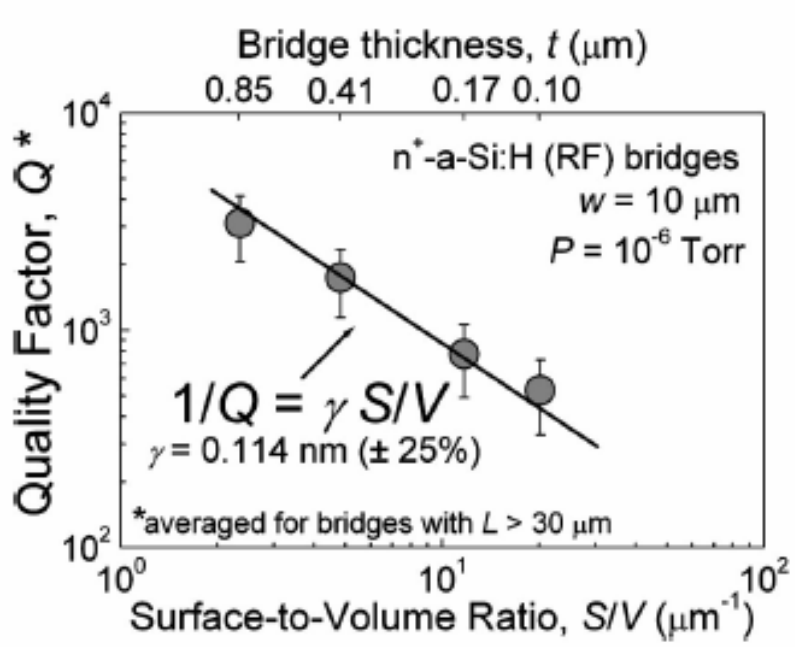


Figure 2.18: *Quality factor measured at* 10^{-6} *Torr, and plotted as a function of the surface-to -volume ratio* S/V*, [66].*

Other works have measured the quality factors of c-c beams, but resonators dimensions implied that no anchoring losses could be neglected [68], concluding that anchoring losses could also contribute to total resonator losses.

An interesting work was done in order to derive analytically surface losses dependence with the resonator thickness in beams [71]. The energy dissipation was modeled by considering a complex-valued Young's modulus for the volume $E = E_1 + iE_2$ and for the surface layer of thickness δ: $E^S = E_1^S + iE_2^S$, where E_1 and E_1^S are the conventional and real-valued Young's modulus and E_2 and E_2^S are the dissipative parts. Calculating the energy lost per cycle due to the surface layer and the total stored energy in terms of the elastic energy, an expression of the losses due to the surface can be derived:

$$Q_{surface}^{-1} = \frac{2\delta\,(3w+t)}{w\cdot t}\frac{E_1^S}{E_1}\frac{E_2^S}{E_1^S} = \frac{6\delta}{t}\frac{E_1^S}{E_1}\frac{E_2^S}{E_1^S} \tag{2.95}$$

By this equation the dependence of the surface losses on the thickness is demonstrated.

2.9.4 Thermoelastic damping, TED

Another possible source of energy loss in cantilever microstructure is ThermoElastic Damping (TED). Thermoelastic energy dissipation is caused by irreversible heat flows across the thickness of the resonator as it oscillates. This loss mechanism is the dominant in thicker and long cantilevers when losses concerning anchoring and surface can be neglected. In resonator geometries where those losses can be neglected, the maximum Q factor is then limited by the material properties of the resonator structural material.

A theory for thermoelastic damping in homogeneous and isotropic beams was firstly established by Zener [72]. Roszhart demonstrated that TED can be a dominant source of energy loss in single-crystal silicon cantilevers as thin as $10\mu m$ [73]. This mechanism of energy loss becomes less relevant as thickness is decreased, being anchoring and surface losses the main mechanism that limit the quality factor in vacuum.

Losses due to thermoelastic losses can be expressed as:

$$Q_{TED}^{-1} = 2\Gamma(T)\Omega(f) \tag{2.96}$$

where $\Gamma(T)$ contains the relevant information concerning the material dependencies of the TED process: coefficient of thermal expansion ($\alpha_{thermal}$), device temperature (T), Young's modulus (E), mass density (ρ) and specific heat (C_p).

$$\Gamma(T) = \frac{\alpha_{thermal}^2 \cdot T \cdot E}{4 \cdot \rho C_p} \tag{2.97}$$

The second term $\Omega(f)$, depends on the ratio of the cantilever frequency f to a characteristic frequency F_0, which quantifies the rate of heat flow across the thickness of a resonator.

$$\Omega(f) = \frac{2f/F_0}{1 + (f/F_0)^2} \tag{2.98}$$

TED is maximized at $f = F_0$, and F_0 can be expressed as:

$$F_0 = \frac{\pi \kappa_{cond}}{2\rho C_p h^2} \tag{2.99}$$

where κ_{cond} is the cantilever material thermal conductivity and h is the material thickness.

That work based on single crystal silicon has been extended to polysilicon resonators [74]. When extending Zener's analysis to poly crystalline materials, it shall be pointed that more contributions to thermoelastic losses arise due to:

- *Intracrystalline Damping.* A new mechanism of dissipation energy appears on polycrystalline resonators due to the conduction of heat within each layer is much faster than the contribution between different layers. The contribution to the overall damping is done in the same way that for homogeneous materials, but here the dimensional values are appropriated by a single grain.

- *Intercrystalline Damping.* In an elastically anisotropic polycrystalline solid, the lateral and transverse strains are constrained to be equal at the grain boundaries. Additional dilatation stress and temperature inhomogeneities on the scale of the average scale grain size.

The TE damping for polycrystalline resonators can be expressed as:

$$Q^{-1}_{TED-polycrystalline} = Q^{-1}_{Intra} + Q^{-1}_{Inter} \tag{2.100}$$

2.10 Summary

In this chapter an electromechanical model has been derived based on a flexural clamped-free beam. That model takes into account the real deflection of the beam and the fringing field contribution to compute the capacitance between electrodes and resonator. The model has also been developed for a clamped-clamped beam. For bulk resonator structures, a complete set of equations, that will be used for designing the resonators in the following chapters, relating the resonance frequency and effective mass and spring constants with the resonator characteristic dimensions have also been described.

Table 2.1 shows a summary of the design equations for the previously described resonators. Especifically, equations governing the resonance frequency, the effective mass and the elastic constant are hereby reproduced. The resonators that have been described are: the c-f and c-c beam and the paddle resonator for the flexural resonators and for the bulk acoustic resonators: the Longitudinal Extensional Bulk Acoustic Resonator (LBAR), the Radial Disk Bulk Acoustic Mode (RDM) and Wine-Glass Disk Bulk Acoustic Mode (WGDM), the Square Shaped Bulk Acoustic Resonator (SBAR), and the Ring Shaped Bulk Acoustic Resonator (RBAR).

Furthermore, at the end of the chapter it has been introduced the main loss mechanisms present in those dynamic microresonators. From the dominant loss mechanism observed in air ambient to the main loss mechanisms that limits the maximum quality factors that can exhibit the microresonators in vacuum.

	Elastic constant	Effective mass	Resonance Frequency
c-f beam	$\frac{Ehb^3}{4L^3}$	$m_{n_cf} = \frac{3}{(\kappa_{n_cf}L)^4} m_0$	$\omega_{n_cf} = \frac{(\kappa_{n-cf}L)^2}{\sqrt{3}} \sqrt{\frac{k_{cf}}{m_0}}$
	$\kappa_n L = 1.875 \quad 4.694 \quad 7.854$		
c-c beam	$\frac{16Ehb^3}{L^3}$	$m_{n-cc} = \frac{192}{(\kappa_{n-cc}L)^4} m_0$	$\omega_{n-cc} = \frac{(\kappa_{n-cc}L)^2}{\sqrt{192}} \sqrt{\frac{k_{cc}}{m_0}}$
	$\kappa_n L = 2.365 \quad 3.927 \quad 5.4978 \quad 7.069$		
PTRA	$2\frac{Ea^3h}{L^3}$	M	$\omega_{TRANS} = \frac{1}{2\pi}\sqrt{2\frac{Ea^3h}{ML^3}}$
PTOR	$\kappa = 2\beta\left(\frac{h}{b}\right)\frac{hb^3}{L}G$	$I = \frac{\pi^2 \rho w_2 h w_1^3}{3}$	$\omega_{PTOR} = \frac{1}{2\pi}\sqrt{\frac{3}{\pi^2}\frac{\kappa}{\rho w_2 h w_1^3}}$,
SBAR	$\pi^2 E_{2D} h$	$m_{SBAR} = \rho h L^2$	$\omega_{SBAR} = \frac{1}{2\pi}\sqrt{\frac{\pi^2 E_{2D} h}{\rho h L^2}}$
	$E_{2D} = c_{11} + c_{12} - 2c_{12}^2/c_{11}$		
LBAR	$\frac{16Etb^3}{L^3}$	$m_{LBAR} = \frac{\rho b h L}{2}$	$\omega_{LBAR} = \frac{2\pi}{4L}\sqrt{\frac{E}{\rho}}$
RDM	$k = m(2\pi f_0)^2$	$m = \frac{2\pi\rho t \int_0^R r dr (J_1(hr))^2}{(J_1(hR))^2}$	$f_{0,n} = \frac{\delta_{RDM,n} R}{2\pi E\sqrt{\rho(1-\sigma^2)}}$
	$\delta_{RDM,n} = 1.9844 \quad 5.3702 \quad 8.5200 \quad 11.7232$		
WGDM	$k = m(2\pi f_0)^2$	*Equation*2.79	$f_0 = \frac{\delta_{RDM} R}{2\pi E\sqrt{\rho(1-\sigma^2)}}$
	$\delta_{wgm} = 2.0784$		
RBAR	$k = m(2\pi f_0)^2$		Equation2.81

Table 2.1: *Summary table, synthesizing all the design equations for the set of resonators previously described.*

CHAPTER 3

Hybrid Approach for RF-MEMS Integration

In this chapter, fabrication processes defined and carried out during this phd thesis for the hybrid integration of vibrating, capacitively transducer RF-MEMS are described. The chapter starts with a review of the state-of-the-art of present technologies for fabrication of capacitively transduced microresonators for high frequency applications. Stand-alone microresonators have been fabricated by exploding two kinds of capacitive transducer readout, based on sub-100nm air and dielectric solid gaps and target frequencies in the VHF (from 100MHz to 300MHz) and UHF (300MHz to 1GHz) bands.

3.1 State of the art for RF-MEMS fabrication

When designing and fabricating micromechanical resonators, different variables are pursued in order to obtain the best performance of such devices. Those variables are, the electrical transducer gap, the material thickness and excellent material properties.

In chapter 1, the motional resistance parameter was introduced when defining the capacitive transduction, equation 1.2. Assuming the motional resistance as a figure of merit to be minimized, a dependence on the power to the fourth is observed on the gap transducer distance, s. Then, this parameter becomes more and more relevant as the target frequency increases, due to smaller vibration amplitudes of the resonator and, then the consequently decrease of resonance current generated. Also, this parameter wants to be minimized in order to decrease the DC operation voltage to the structure. When increasing frequency, only gap distances below 100nm makes the resonance movement detectable. So, a lot of works pursue the minimization of those gaps distances.

Another relevant parameter in the microresonators design is the structural material thickness.

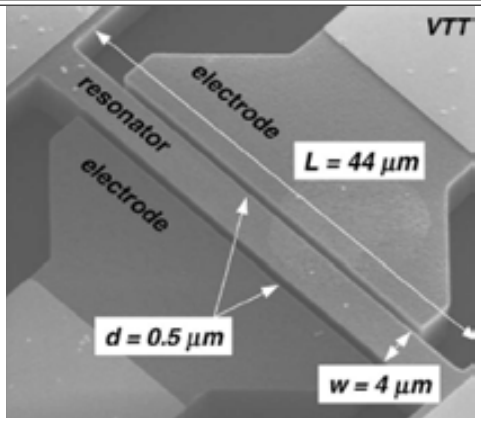
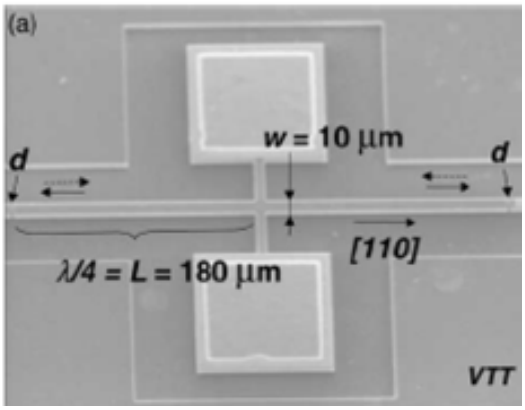
Resonator properties	**Fabricated device**, [11]
SOI wafer One-mask Process Optical lithography Str. Mat: Silicon Elec. Mat: Silicon Gap=500nm L=44μm Thickness=8μm $f_{RES} = 14MHz$ $Q = 1500$ $V_{DC} = 100V$	
Resonator properties	**Fabricated device**, [50]
SOI wafer One-mask Process Optical lithography Str. Mat: Silicon Elec. Mat: Silicon Gap=1μm L=8μm Thickness=8μm $f_{RES} = 12MHz$ $Q = 180000$ $V_{DC} = 100V$	

Table 3.1: *Review of the two different resonators (flexural-resonance and bulk resonance fabricated by one-mask process and optical lithography for patterning electrodes and resonator simultaneously).*

Coupling depends directly on this parameter, and hence, the resonance current generated. In addition to that, a thick structural material ensures the minimization of the sticking of the structures on the substrate, that would yield to a lower device robustness. Furthermore, surface effects that limits the maximum quality factor are more important as the material thickness is smaller. Then, thicker structural materials are related with higher quality factors.

The structural material properties are also a very important parameter when designing microresonators. Excellent material properties are sought in terms of achieving high frequencies and high quality factors. This is the reason why silicon material is preferred as structural material for microresonators, and hence, Silicon On-Insulator (SOI) wafers are the start point

for the fabrication.

In table 3.1 are depicted two resonators fabricated by the same research group at VTT (Mattila et al. [11], [58]) starting the process from SOI wafer. Both resonator and electrodes are fabricated patterning the top silicon single crystal (SCS) in the same photolithography step. Then, only one mask is necessary for fabricating both electrodes and resonators. However, the resolution in this technique is limited by the phtolithography step and it is difficult to decrease the gap distance below $500nm$ with high reproducibility. Those large distances become a problem when scaling such resonators to higher frequencies. Then smaller resonators with smaller movements at resonance will need a smaller transducer gap in order to detect the resonance current. Furthermore, the design of such devices in a future RF transceiver will demand sometimes matching impedances of 50Ω, and a way to decrease this motional resistance characteristic of the MEMS devices will be by reducing the gap distance.

Aware of the crucial importance of the gap distances, the research group leaded by Prof. Nguyen developed a technological process to achieve gap distances around $100nm$ for vertical flexural beam resonators; the vibrating structure is a free-free beam supported by a pair of clamped-clamped beam vertically actuated.

The technological process, a Scanning Electron Microscopy (SEM) micrograph of one fabricated device and its dimensions are shown in table 3.2. The start-up point for the technological process is a Si wafer, when an isolating thin layer of Si_3N_4 is deposited by Low Pressure Chemical Vapour Deposition (LPCVD). In the next step, a layer of polysilicon is deposited, doped and patterned in order to form the electrode. Then, the sacrificial oxide layer that will form the gap spacer is deposited by LPCVD techniques. The cross section of the process at this point corresponds to the a) sequence step in the cross-section in table 3.2. Then, the structural material of the resonator is deposited by LPCVD with a thickness of $2\mu m$. This polysilicon is doped and annealed in order to reduce internal stresses and finally patterned by an oxide layer acting as mask (step b)). Finally, the resonator is released in Hydrofluoric Acid (HF) solution (step c)). A SEM micrograph of the final device is depicted also in table 3.2 with its characteristic dimensions and electrical properties. The device is $14.9\mu m$ long and $4\mu m$ wide, exhibiting a resonance frequency of $71.5MHz$ and a quality factor in vacuum of $Q = 8250$.

A substantial difference between both technological processes depicted up to now lies on the gap spacer technique. Whereas on the first technological process, the gap distance was controlled by optical lithography (which is very difficult to achieve a good alignment below $1\mu m$ with high reproducibility), on the second approach a silicon oxide layer will make the role of the gap spacer. It shall be pointed that controlling the thickness of this sacrificial layer will yield to the desired and designed electrical gap. From now, we will see variants of this gap spacer technique for the fabrication of more complex resonators, in terms of thickness (above $3\mu m$) and in terms of shape and geometries.

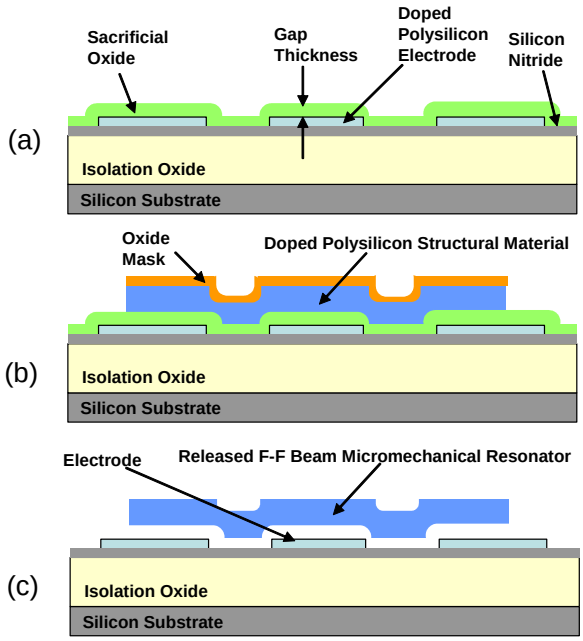
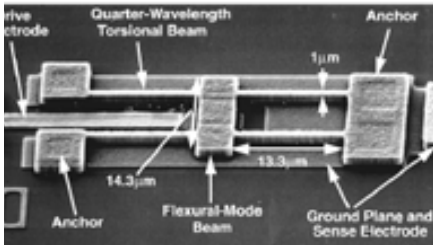
<table>
<tr><td colspan="2">Technological process sequence, K. Wang et al. [75]</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td>Measured properties</td><td>Fabricated device</td></tr>
<tr><td>Structural Material: Silicon
Elec. Mat: PolySilicon
Gap=123nm
$L = 14.9\mu m$
$f_{RES} = 71.5MHz$
$Q = 8250$
$V_{DC} = 126V$</td><td> 
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Table 3.2: *Technological process introducing a thin silicon oxide for forming the gap spacer. By this process, vertical free-free beams with gaps of* 120nm *are fabricated.*

The next relevant technological process for fabricating microresonators is depicted in table 3.3. The process is focused on fabricating thick (3μm and above) MEMS microresonators in a SOI wafer, taking advantage of the mechanical properties of the single crystal silicon [76]. In fact, this process is based on a previous one named High Aspect-Ratio Combined Poly and Single-Crystal Silicon MEMS Technology (HARPSS) [77],[78] but adapted to SOI wafers.

The HARPSS process on a SOI wafer is reduced to a 3-lithographic steps. The advantages of using an SOI substrate compared to a regular silicon substrate used previously [77], [78] on this process, are the possibility to apply different voltages to the structures reducing the

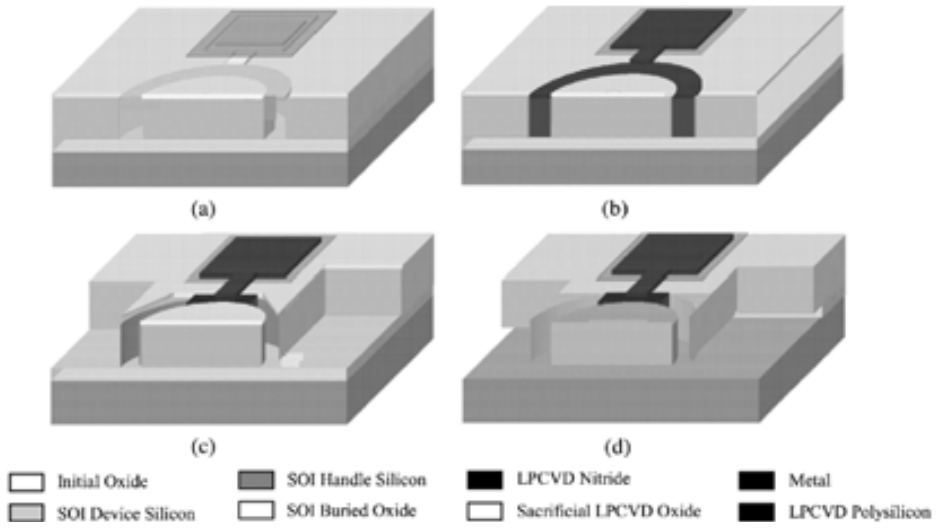
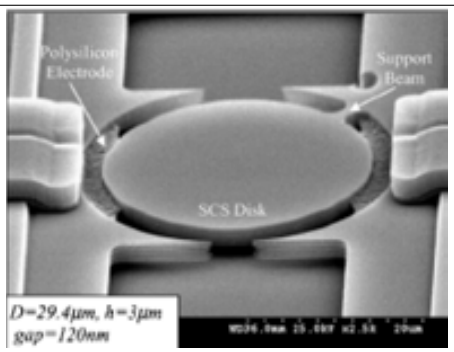
<table>
<tr><th colspan="2">Technological process sequence, Pourkamali et al. [76]</th></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><th>Measured properties</th><th>Fabricated device</th></tr>
<tr><td>Structural Material: SCS
Electrodes Material: PolySilicon
Gap=120nm
Thickness=3μm
Diameter=29.4μm
$V_{DC} = 12$
$R_m = 883k\Omega$
$f_{RES} = 147.8MHz$
$Q_{vacuum} = 39300$,</td><td> 
</td></tr>
</table>

Table 3.3: *HARPSS process sequence applied to a SOI wafer.*

parasitic capacitances, better definition of width structures (disk, ellipses, needed for higher frequency resonators) and no need of the gap sacrificial oxide as a protective layer for silicon structures during the isotropic etch.

The processing steps for fabrication of SCS, HARPSS resonators on SOI substrates is shown in table 3.3. The fabrication process starts growing a $1\mu m$ of silicon dioxide on top silicon. The patterned initial oxide allows an isolation between the substrate and input and output pads, and serves as a mask for the subsequent silicon trench etching step. A thin layer of Si_3N_4 is deposited and patterned on the pad area to protect the pad oxide during the HF release step at the end of the process. In order to avoid undesired nitride residues (produced

in the anisotropic plasma etching of the nitride), the nitride layer is wet etched isotopically in phosphoric acid. A thin layer of LPCVD-High Temperature Oxide (HTO) oxide patterned in buffered HF (Buffered Hydrofluoric Acid (BHF)) is used as a mask.

The microresonators are defined by etching trenches in the device layer all the way down to the buried oxide layer of the SOI in a DRIE system using the Bosch process [79]. Due to high selectivity of the silicon etching plasma used in the inductively coupled plasma system to oxide and nitride , the patterned oxide and nitride layers are used as the protecting mask layer for silicon. A thin layer of LPCVD-HTO oxide, conformal covering all the resonator sidewalls is then deposited at 850^oC. The sacrificial oxide is removed on the surface by a short anisotropic oxide plasma etching, while keeping it on the resonator sidewalls, so that the deposited polysilicon for the pads will be in direct contact with the nitride layer and remains firmly anchored during the HF release. Trenches are subsequently refilled with doped LPCVD polysilicon to form the vertical electrodes. The deposited polysilicon ($3\mu m$ thick) is patterned on the surface to form the wirebonding pads for the input and output electrodes. The resonators are then released from the handle silicon layer and the electrodes

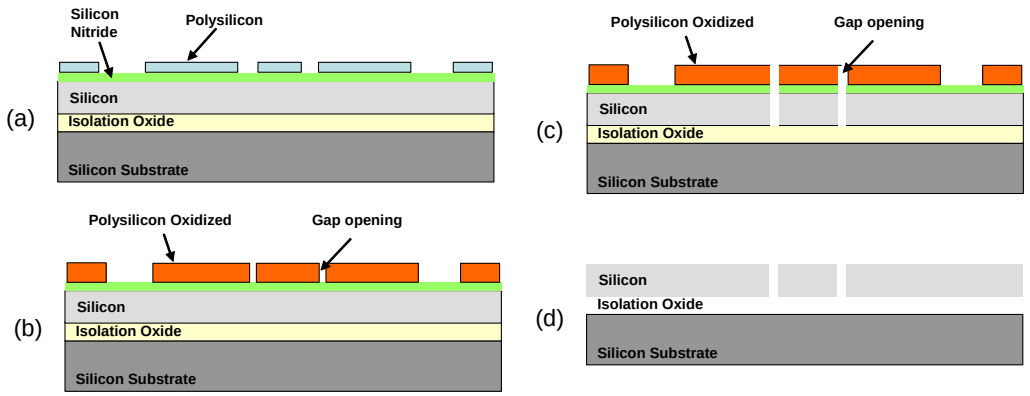
by removing the Buried Oxide Layer (BOX) of the SOI and the sacrificial oxide in a BHF. BOX thickness for the substrates used in this work was $2\mu m$.

Results of a device are shown on table 3.3. A disk of $29.2\mu m$ on diameter, and $3\mu m$ thick shows a resonance frequency of $149.3MHz$ and a quality factor in vacuum of 45700. This quality factor is 40 times larger than the highest achieved Q-frequency products for the flexural mode SCS-HARPSS beam resonators [78].

Another work carried out from the same group at University of Georgia ([80]) is depicted in table 3.4. The main characteristic in this process is that only one mask is necessary to obtain $10\mu m$-thick resonators and gaps below $200nm$. The process begins with the deposition of a thin layer of LPCVD nitride which will prevent the oxidation of the silicon layer in subsequent process steps. A thin-film polysilicon layer is deposited and patterned. The smallest feature size on the polysilicon layer is determined by optical lithography. The patterned polysilicon will be thermally oxidized in an oxidation furnace. The smallest feature size on the polysilicon layer is determined by the lithography ($> 1\mu m$).

Finally the patterned polysilicon will be thermally oxidized in an oxidation furnace to form a thick oxide mask for DRIE step. Meanwhile all the openings are reduced in size by 2 times due to the oxidized polysilicon. Then, the minimum distance achievable by optical lithography is improved by this step of oxidation. The final opening size in this process varies with the thickness of the polysilicon layer and the subsequent oxidation step. The thick oxide acts as the mask for the DRIE etching of the silicon underneath, which is the structural material for the resonator. As an example, a bulk acoustic resonator is fabricated and demonstrated by this technological process. The dimensions of the bulk resonator are $140\mu m$ long, $20\mu m$ wide and $10\mu m$ thick. The measured resonance frequency is $205MHz$ for $50V$ applied in vacuum

Technological process sequence, Abdolvand et al. [80]



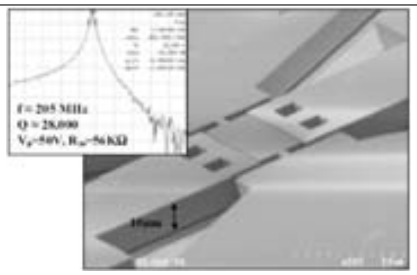
Measured properties	**Fabricated device**
Str. Mat: Silicon Elec. Mat: PolySilicon Gap=210nm Thickness=11μm $f_{RES} = 205MHz$ $Q_{vacuum} = 28000$, $V_{DC} = 50V$	

Table 3.4: *One-mask based technological process to achieve sub-*100nm *gaps in thicknesses above* 10μm.

exhibiting a quality factor of 28000.

The next relevant fabrication process corresponds to Prof. Nguyen [81], depicted in table 3.5. The process pursues the fabrication of disk-shaped resonators at 1GHz frequency. The main feature of this process is the self-alignment of the stem that supports the disk. The importance of the alignment of the stem with respect to the disk is crucial in order to decrease losses by the anchor; also, the dimensions of this stem determines the lost energy. The process defines both the stem position and disk edges all in one mask, effectively eliminating the possibility of misalignment.

The process is characterized by choosing LPCVD deposited polysilicon (2μm thick) as structural material for the disk. The gap distance is formed by the deposition of silicon oxide sacrificial layer and a ground plane is also included in the fabrication process in order to decrease the parasitic capacitances. A final device is depicted in table 3.5. The stem and disk diameter are 20μm and 2μm, respectively. The disk shows a resonance frequency in the

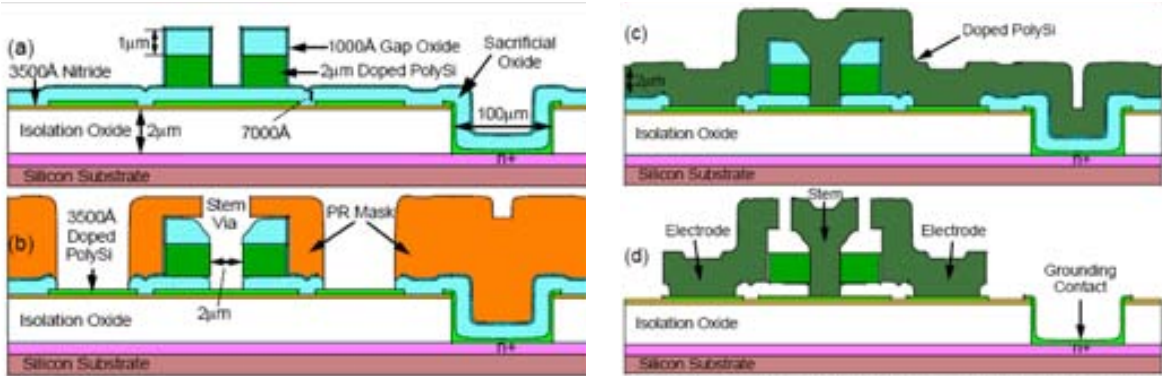
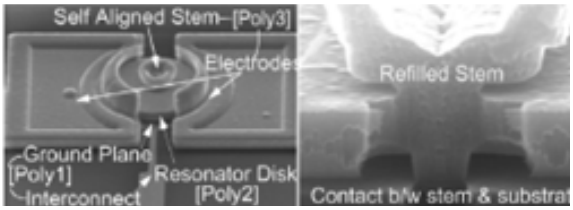
Technological process sequence, Nguyen et al. [81]	
	
Measured properties	**Fabricated device**
Str. Mat: Silicon Elec. Mat: PolySilicon Gap=210nm Thickness=$2\mu m$ $f_{RES} = 1139.9MHz$ $Q_{vacuum} = 1595$, $V_{DC} = 12.9V$	

Table 3.5: *Process sequence for fabricating disk acoustic bulk resonator with self-aligned stem.*

first radial mode of $274MHz$ and $1139.9MHz$ in the third mode, with a Q-factor of 1595 (in vacuum).

This technological process has been the basis for two works specially relevant published in the framework of the same group; the first works published [82] refers to the benefits of substituting the stem material for another material different from the microresonator in order to lower the anchor energy losses. The second work [83] explores the advantages of implementing high frequency resonators with solid and high permitivity gap materials.

3.1.1 Reducing anchoring losses. Anchor material

In the first work [82], the material of the stem is chosen to be different from the disk structural material in order to decrease losses due to the anchoring. Figure 3.1 shows a representation of the acoustic waves traveling around the disk. When the stem and disk present different structural materials, a reflection of those acoustic waves is produced.

The acoustic impedance mismatch between two materials implies that a part of the incident acoustic waves into the stem are reflected instead of being transmitted to the substrate through the stem, increasing losses and hence, decreasing the quality factor.

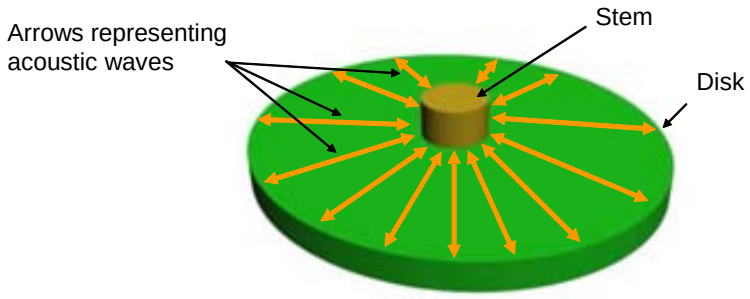


Figure 3.1: *Scheme of a disk with a stem of different material illustrating the first radial mode.*

If Z_1 is the disk material acoustic impedance and Z_2 is the acoustic impedance of the stem material, the reflected coefficient, that express the ratio of reflected energy arriving to the stem can be written as:

$$R = \frac{Z_2 - Z_1}{Z_2 + Z_1} \tag{3.1}$$

The acoustic impedance of a given material is defined as the product of the material mass density and the acoustic wave velocity, which is also related with its Young modulus and mass density:

$$Z = \rho \times v = \rho \times \sqrt{\frac{E}{\rho}} = \sqrt{E\rho} \tag{3.2}$$

where E and ρ denote the material Young's modulus and mass density.

The same technological process as depicted in table 3.5 is used to fabricate polydiamond disk resonators with a stem refilled of polysilicon. The differing acoustic velocities of disk (polydiamond: $Z_1 = 6.18 \times 10^7 kg/(m^2 s)$) and stem (polysilicon: $Z_2 = 1.85 \times 10^7 kg/(m^2 s)$) built in intentionally dissimilar materials create an impedance mismatch at the disk stem interface that substantially reflects the acoustic wave ($R = 54\%$) and attenuates acoustic energy radiated from the vibrating disk to the stem.

More specifically, this process differs from the previous self-aligned polysilicon disk resonator surface micromachining process [81] mainly in the diamond deposition and dry etching steps, which essentially replace those for polysilicon in the process of [81]. A $20\mu m$ diameter polydiamond disk resonator ($1.6\mu m$ of diameter stem) operating in its second radial-contour mode shows a Q-factors of $11,555$ in vacuum and $10,100$ in air at $1.51GHz$, achieving an exceptionally high frequency-Q product of $1.74 \times 10^{13} MHz$.

3.1.2 The solid transducer gap

The second work specifically relevant for our purposes refers to the solid dielectric transducer gap. The idea beyond this work is to substitute the traditional air transducer gap by a solid dielectric gap in order to enhance the electrical resonance current [83]. The technological process is similar to the one depicted in table 3.5. In that process, lateral electrode-to-resonator air-gap spacings were defined by the thickness of a conformal deposited sidewall oxide layer, which was later removed by an isotropic HF wet etchant to achieve the desired electrode-to-resonator air gaps.

For solid-gap resonators, silicon nitride, instead of silicon dioxide, is deposited via LPCVD to form the sidewall spacer. During the sacrificial hydrofluoric acid release step, the oxide underneath and above the disk-electrode structure is removed, as is any exposed nitride (due to the finite 10 nm/min etch rate of nitride in HF), but the nitride in the electrode-to-resonator gap remains intact, since it is effectively protected from HF attack by the slow diffusion of the wet etchant into the tiny solid nitride-filled electrode-to-resonator gap. Interestingly, the air-gap process actually proved to be the more difficult of both, because it required removal of oxide in small gaps, which is a difficult, diffusion-limited process. As a consequence, the solid-gap designs were able to achieve smaller gaps of $20nm$, whereas the air gaps were limited to about $60nm$.

The advantages of the implementation of microresonators with a high-permitivity solid dielectric is the enhancement of the electrical read-out current in combination with the improvement on the reliability associated with the releasing process. Figure 3.2 shows the advantage to have the solid gap. Moistures and products derived from chemical wet etching during the releasing process can be trapped in the gap region, causing a non-optimal operation of the device and possibly provoking the breakdown of the device when applying the DC voltage.

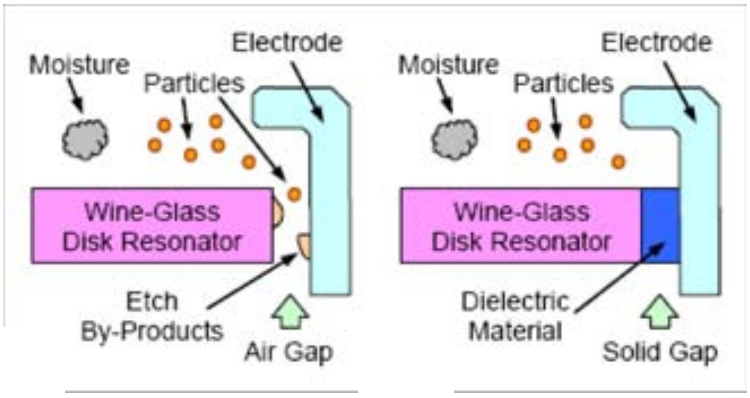


Figure 3.2: *Comparison scheme between air gap (left) and solid gap (right) [83].*

Furthermore, an enhancement of the electrical current is expected as expenses of increasing the dielectric permitivity of the gap medium.

The resonator motional resistance is defined as the fraction of the input AC voltage divided by the output current generated by the movement at the resonance.

$$R_{x_{solid}} = \frac{v_{ac}}{I_o} = \frac{k_r}{w_0 V_{DC}^2} \frac{d^4}{\epsilon_o^2 \epsilon_r^2 A^2} \frac{1}{Q} \tag{3.3}$$

In fact, the motional resistance is a figure of merit for designing microresonators and its value is sought to be as low as possible and close to the standard of the electrical circuit, which is 50Ω or 75Ω. From equation 3.3 the motional resistance has a significant dependence with:

- The gap spacing between resonator and electrode, s, has a dependence as a power to the fourth. The designer will try to lower as much as possible the gap distance.
- The coupling area, A. The designer will focus on resonators with large coupling area.
- The dielectric permitivity on the gap spacer, considering the possibility to be filled of a material of relative permitivity, ϵ_r.
- The DC applied voltage.

Traditionally, the gap spacer is air, so the dielectric permitivity is $\epsilon_r = 1$. The resonance current generated by the resonator increases as the gap distance decreases; however, some problems related with stiction and with the etching of the sacrificial gap spacer appears when reducing those gap distances below $60nm$ (for $2\mu m$-thick and above resonators) [83]. The limitation on reducing the gap distance are due to the difficulty of the HF solution to penetrate and the subproducts of the reaction to leave; also, if the gap spacer is not properly removed, stiction occurs when operating electrically the device, lowering the device performance and reliability. In this sense, a solid gap not only incorporates the possibility of decreasing the gap distance by controlling the gap material deposition, but also assures an improvement of the capacitive transduction by means of increasing the relative permitivity.

In order to compare both possibilities, a new figure of merit relating motional resistances for both cases is defined:

$$\beta = \frac{R_{x(AirGap)}}{R_{x(SolidGap)}} = \epsilon_r^2 \gamma \frac{Q_{SolidGap}}{Q_{AirGap}} \frac{d_{AirGap}^4}{d_{SolidGap}^4} \tag{3.4}$$

where the γ parameter takes into account the reduction of the displacement of the resonator at resonance ($\gamma < 1$). In table 3.6 the main advantages and drawbacks introduced by the solid gap concept are depicted. As main advantages arise the increased capacitive transduction by means of increasing the relative dielectric permitivity and the decreasing of the gap distance. As drawbacks, the movement at the resonance frequency will be decreased whereas induced losses on the gap will increase, reducing the Q factor of the structure.

Solid Gap Resonators	
Advantatges	**Drawbacks**
Relative dielectric permitivity ↑	↓ Movement at resonance
↓ gap distances	Anchor losses ↑, ↓ Q factor

Table 3.6: *Advantages and drawbacks of replacing the traditional air gap by a dielectric solid gap.*

Up to now, the restriction imposed for choosing the solid gap material are based on its dielectric properties. However, acoustic losses in the gap region will now increase due to the anchoring of the resonator to the drivers. Then, a new restriction has to be imposed in terms of mismatching acoustic impedances between two mediums. The solid gap is pretended to have a different acoustic impedance from the polysilicon in order to reduce anchor losses. In table 3.7 are depicted different proposal as gap material, showing their acoustic impedances as well as the reflection coefficient normalized to the polysilicon value.

Material	ϵ_r	Acoustic Impedance $10^6 kg/m^2 s$	Reflection Coefficient	$\epsilon_r \times R$
$PolySi$		18.5	0	
$Diamond$		61.8	0.53	
$Si0_2$	3.9	12.6	0.19	0.74
Si_3N_4	7	25	0.15	1.05
AlN	$9-10$	43	0.39	3.51
C_4F_8	2	3	0.72	1.44

Table 3.7: *Dielectric constants, acoustic impedance and reflection coefficient (choosing polysilicon as reference material) for possible gap materials.*

From the design point of view, a combination of high dielectric constant with a high reflection coefficient is the most wanted option. In this criteria, piezoelectric materials are the best choice, due to its excellent dielectric properties and high acoustic impedance (derived from their high Young's modulus). However, difficulties on combining CMOS standard processes with the deposition of piezoelectric materials open a window to other more CMOS-compatible options like SiO_2 and Si_3N_4, as expenses of increasing losses and lowering the dielectric constant. Another relevant material depicted in table 3.7 is the carbonfluoroteflon, which presents the best reflection coefficient due to its soft condition. However, the future incorporation of high dielectric materials (high-k) to the fabrication of sub-52nm long transistors could open the possibility to incorporate those materials in the microresonators fabrication.

Due to the importance of the dielectric constant of the gap material and the reflection of the acoustic waves in the transducer area, a figure of merit $\epsilon_r \times R$ is defined in order to designate which of the above approaches are the most suitable. In fact, the figure or merit could be defined as $\epsilon_r^2 \times R$, but the exact dependence of the quality factor in the reflection coefficient is not clear at all, let's suppose that the relative permitivity and the reflection coefficient have the same weight on the motional resistance. Results of those calculations are shown in the last column of table 3.7. From the calculations, the approaches based on the carbonfluoroteflon as well as the aluminum nitride seems to present better possibilities, one due to the moderate high dielectric constant (the AlN) and the other one because shows higher reflection coefficient. The SiO_2 and the Si_3N_4 show a relative low figure of merit because they have a similar acoustic impedance than polysilicon.

Then, the AlN as well the C_4F_8 will be included in the technological process in order to be tested as solid gap materials.

3.2 Fabrication process of air-gap resonators

The fabrication of air-gap resonators has been carried out by Dr. Francesc Torres at the facilities of the National Center of Microelectronics (CNM, *Centro Nacional de Microelectrónica*) in Barcelona (IMB, *Institut de Microelectrònica de Barcelona*). In this section, the fabrication process for the definition of nanometer scale air-gap resonators are introduced. This process presents some similarities with the HARPSS process in SOI wafers described previously.

The technological process has the main objective of fabricating SCS high-frequency bulk-acoustic microresonators $5\mu m$-thick and sub-$100nm$ capacitive gaps on SOI wafers. The process sequence, which is based on 3 masks, is depicted in figure 3.3.

The starting point on the design is the choice of SOI wafers of $5\mu m$ of top silicon and $2\mu m$ of buried oxide.

Starting from a SOI wafer, a $n+$ doping is performed on the top layer in order to increase the conductivity of the active material. This top silicon will be the structural layer for the resonators, due to the excellent mechanical properties of the silicon [84]. The technological process starts with the definition of the vertical trenches employing the first mask. A $2\mu m$ wide and $5\mu m$ deep trenches partially surrounding the resonator are formed by a DRIE etching process. These trenches, when filled of polysilicon, will define the in-plane electrodes, see figure 3.3, steps *a* and *b*. After the dry etching of the trenches, that are performed along all the thickness of the top silicon, a thin layer of silicon dioxide is grown. A dry oxidation process is chosen in order to grow conformal sub-$100nm$ thicknesses due its controllability and low growth rate. This thin oxide makes the role of the gap spacer between resonator and electrode, see figure 3.3.c. The oxide is then patterned by an anisotropic etching in order to avoid the subsequent stiction of the polysilicon with the SCS silicon when releasing the

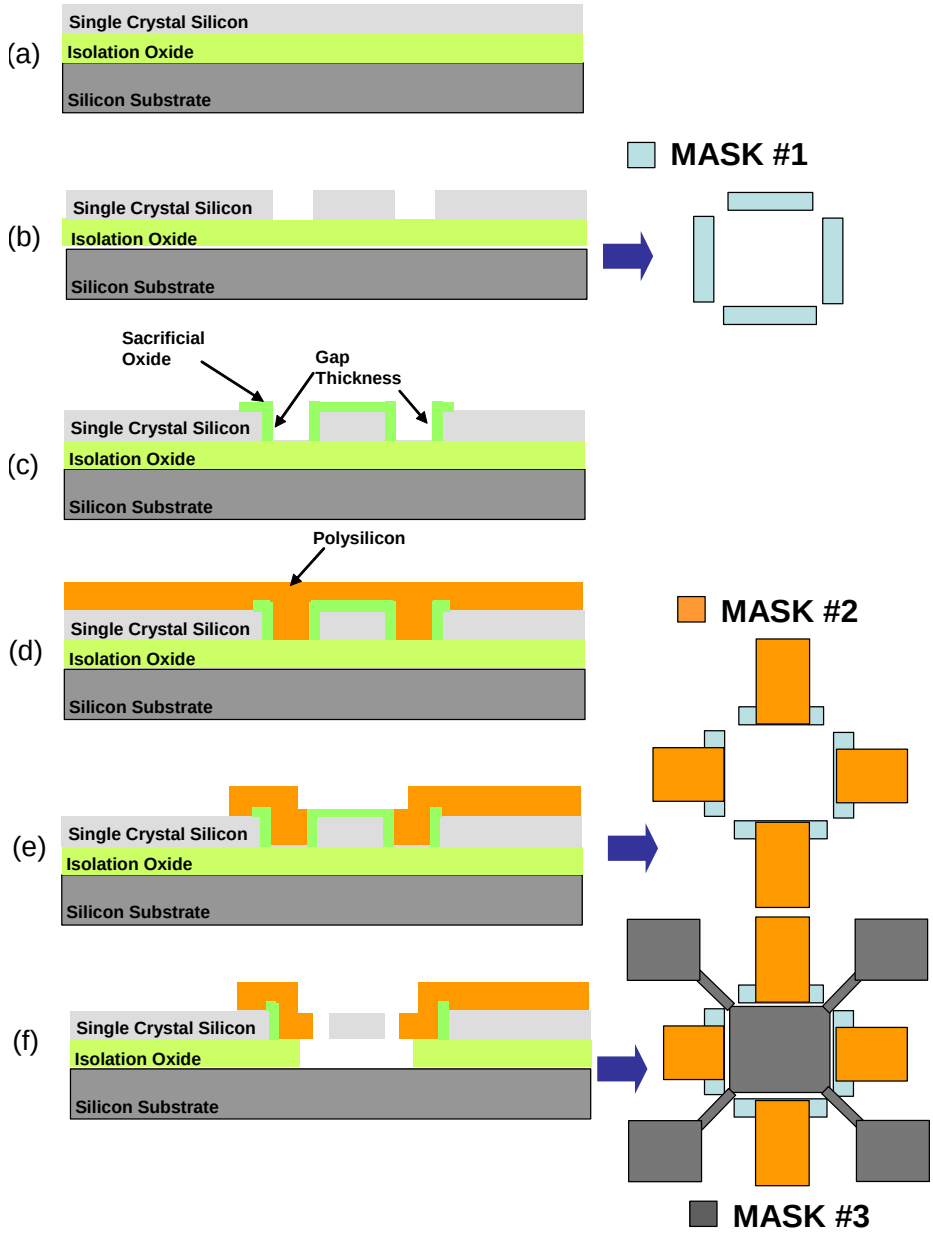


Figure 3.3: *Process sequence for the air-gap resonators.*

resonators in the last step.

Once the silicon dioxide is patterned, a polysilicon layer is deposited in order to refill the trenches for forming the electrodes and pads of the overall device circuit, figure 3.3.d. A photolithography step is then performed (with mask number 2) in order to define the electrical pads and to eliminate the excess of polysilicon in areas close to the gap region, 3.3.e. Finally,

and with mask number 3, a DRIE process is carried out in order to pattern the resonating structure (step f) . The final process is the release of the resonators, that is performed in a wet HF solution.

This technological process allows the fabrication of a broad number of geometries, like beams, disk topologies, frame and solid squares, elliptical shapes and annular rings. In comparison from another technological processes, this process avoids the superposition of the electrodes with the resonator, preventing the resonator to be excited in vertical modes and reducing problems with the stiction of the resonators to the electrodes.

The designs of the structures implemented in this run as well as the preliminary electrical tests performed to those resonators, will be presented in following chapters 5 and 6.

3.2.1 Layout description

In table 3.8 are depicted the different structures that have been fabricated by means of the technological process described. Traditionally, chips fabricated at CNM have dimensions of $(15 \times 15)mm^2$, due to the sample holder of the stepper. In a 4-inches wafer, 21 full-exposed chips are obtained.

The chip area is divided into 10 different regions, according to the type of resonator, their dimensions and hence, their expected resonance frequency. The different types of resonators that have been fabricated are shown in table 3.8.

3.3 Solid-gap resonators

In this section, the fabrication process for solid-gap resonators definition is presented. Structures for the test of solid-gap properties are also described.

The process sequence is depicted in figure 3.4. The main objective is testing different gap materials in order to conclude which is the best choice and if the solid gap shows an improved performance in comparison to the traditional air-gap configuration.

Starting from a non-doped one-side Si wafer, the fabrication process sequence is as follows (see figure 3.4):

- **Step a**. Thermal oxidation in order to form the sacrificial layer and PolySi deposition and doping. In case of starting from a SOI wafer, this step is reduced to doping the top silicon layer.
- **Step b**. PolySi patterning in order to define the structures. Because of the presence of narrow beams in the design, a dry etching technique based on a RIE process will be employed. *MASK1* is needed for this step.

Resonator type	Resonance mode	Frequency expected	Resonator Dimensions
Disk	*Wine-Glass Mode*	$100MHz$	$R = 27.9\mu m$ $b = 1\mu m$
Disk	*Wine-Glass Mode*	$434MHz$	$R = 6.5\mu m$ $b = 1\mu m$
Longitudinal Beam	*Extensional Bulk Mode*	$60MHz$	$L = 36.2\mu m$ $w = 10\mu m$
Square	*Extensional Bulk Mode*	$100MHz$	$L = 42.3\mu m$ $b = 1\mu m$
Square	*Extensional Bulk Mode*	$434MHz$	$L = 9.8\mu m$ $b = 1\mu m$
Ellipse	*Wine-Glass Mode*	$100MHz$	$M_a = 23.7\mu m$ $m_a = 11.8\mu m$
Ellipse	*Wine-Glass Mode*	$434MHz$	$M_a = 10.2\mu m$ $m_a = 5\mu m$

Table 3.8: *Different resonator types included in the air-gap design, showing their dimensions, resonance mode and its expected resonance frequency.*

- **Step c**. Solid-gap material deposition or growth. The growth or deposition process has to be conformal showing a good step coverage with thickness layer ranging from $10nm$ to $50nm$.
- **Step d**. Electrodes material deposition and patterning. For this step, the main alternative from the material point of view is the polysilicon. However, the polysilicon deposition process will not be compatible with all the gap materials proposed. In such cases, the alternative material has to be conductive as well as providing a good step coverage. *MASK2* corresponds to the electrodes design.
- **Step e**. Metal deposition on top of the connection pads in order to improve electrical connectivity with the electrical equipment. An option is perform a liftoff process based on the deposition of $Cr - Au$, that are selective to the HF bath. *MASK3* is the mask used in this step.
- **Step f**. Release of the resonator in a wet HF solution.

In general, the deposition electrode material has to be compatible with the previous step, i.e., the material gap deposition. Also, the electrode's material has to be selective with the resonator releasing step, so, not etched in a HF solution. The fabrication process will be characterized by the gap deposition material process, that will determine the electrode material deposition.

3.3.1 Wafer description

From the wafer design point of view, the wafer is divided into three chips categories:

- Device chips containing resonators. Resonators are based on two designs: Longitudinal Bulk Acoustic Resonators and Ring Acoustic Resonators. Also, in these chips some capacitance structures were designed in order to test the material dielectric properties.
- Step coverage devices. Chips designed for studying the step coverage of the material for the solid gap as well as for the electrode material.
- Chips containing the alignment marks.

Chips size are defined to be small, in order to maximize the total number of devices per wafer. The dimension of the chip is : $(4 \times 3.2)mm^2$. Figure 3.5 shows the chip distribution on the wafer design.

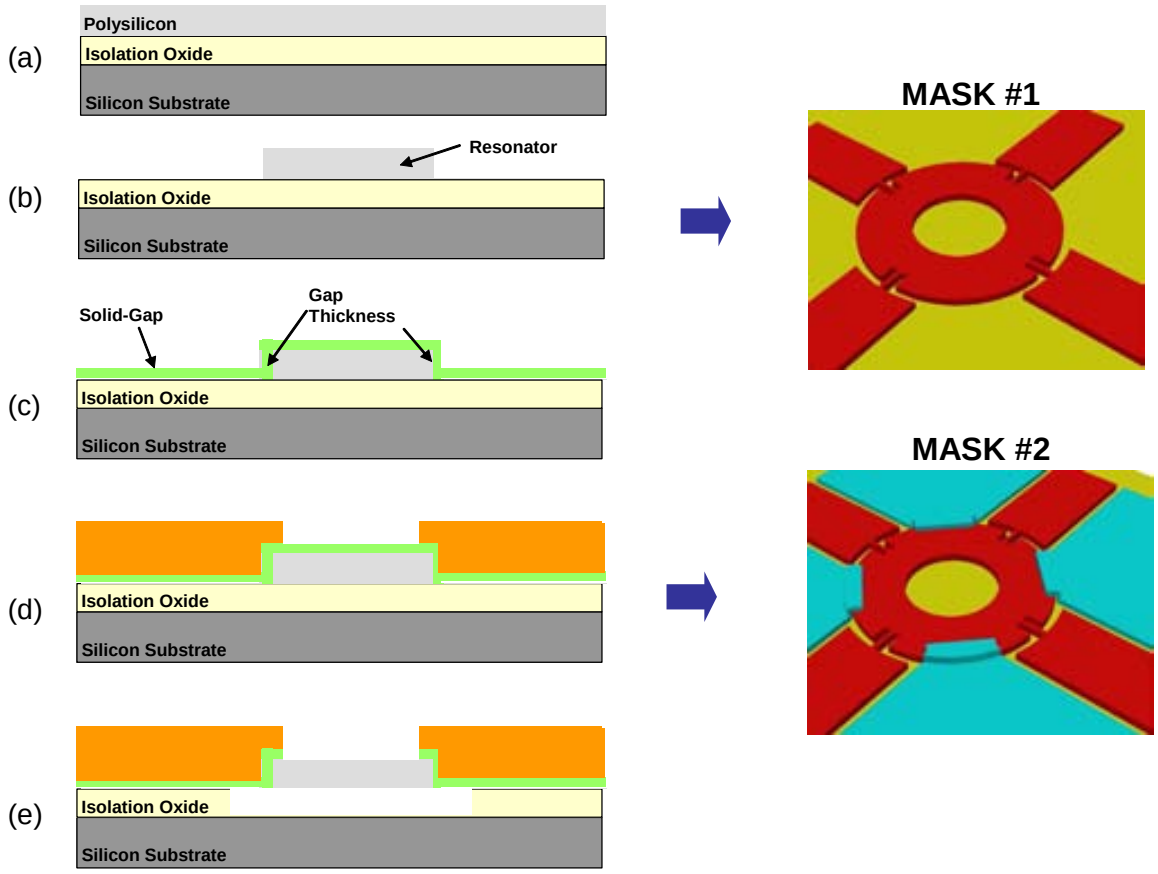


Figure 3.4: *Sequence of the technological process. The technological process is a three mask-process.*

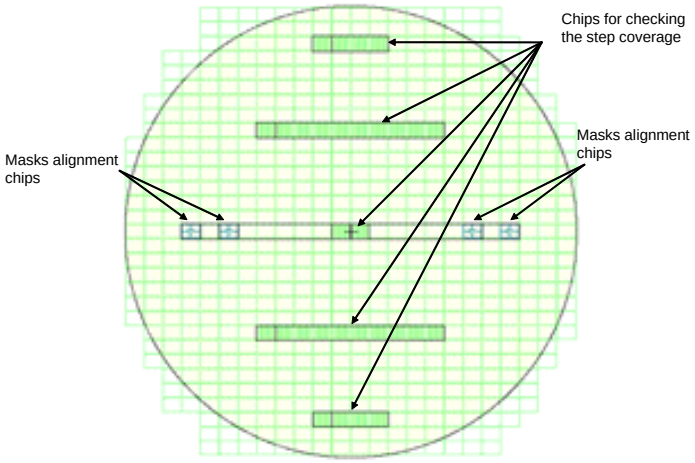


Figure 3.5: *Design of the wafer showing the distribution of the chips.*

In order to test the step coverage of the gap material deposition process, chips containing a set of lines with two different widths were designed. Line length is $3200\mu m$ for all cases, whereas line width are $20\mu m$ and $70\mu m$.

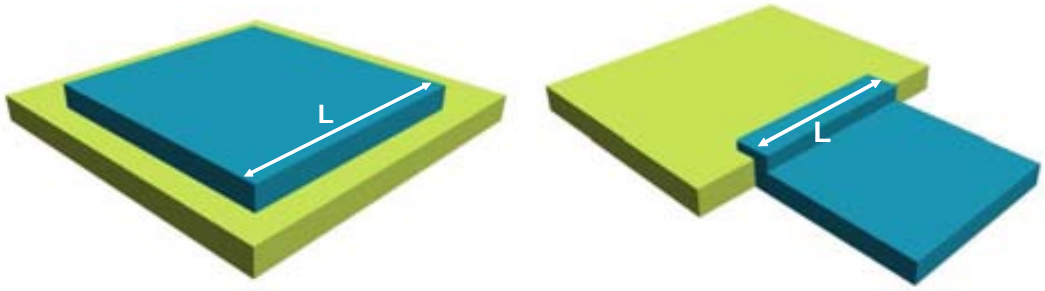
Alignment marks were designed carefully in order to achieve a good alignment between resonator and electrodes, (i.e., between Mask1 and Mask2). Also alignment marks were designed in order to align Mask2 and Mask3.

3.3.2 Chip description

Resonator chips are divided into 10 columns and 5 rows, yielding a total area of $(4 \times 3.2) mm^2$. Each chip contains resonators of different dimensions based on Bulk Acoustic Resonators:

- *LBAR*. Longitudinal Bulk Acoustic Cantilever. Due to their simplicity on releasing and fabrication processes, they were the main choice for the design process. *LBAR* resonators are characterized by their arm length (L) and their arm width (w). However, in order to increase the coupling area, the width resonators were increased at the end of both arms. The addition of those 'ears' changes the equivalent spring constant and the effective mass of the device, reducing the expected resonance frequency of the device. The end arm width is $10\mu m$ for all the designs.

- *RBAR*. Ring Bulk Acoustic Resonators. As an alternative to *LBAR* resonators, these devices exhibit higher coupling area and are the best choice for frequencies designs above 200MHz. In particular, the chip contains two different designs, for $500MHz$ and for $1GHz$. *RBAR* are characterized by the inner and outer radius (r_i and r_o, respectively), and by the beam width supporting the ring (b).



(a) VCAP capacitances (b) LCAP capacitances

Figure 3.6: Scheme showing the vertical test capacitances (VCAP) and the lateral test capacitances (LCAP).

In addition to those resonators, the chip includes some capacitances in order to test the dielectric properties of the gap material. *VCAP* are square, plane-parallel capacitances included in the design showing sides of: $40\mu m$, $65\mu m$, $90\mu m$, $140\mu m$ and $165\mu m$ and designed in order to extract the experimental dielectric permitivity of the material. Because of the bulk resonators designed are in-plane resonators, the necessity to study the lateral deposition of this gap material becomes crucial. Three lateral capacitances (included under the name *LCAP*), and with lengths, $40\mu m$, $90\mu m$ and $140\mu m$ were designed. *LCAP*s allow to extract (indirectly) the lateral thickness of the deposited material. In some cases, this is the only way to know how is the step coverage during the gap material deposition, because of the difficulty of taking SEM images of these thin layers. Figure 3.6 shows a scheme of the *VCAP* and *LCAP* capacitances fabricated in the technological process.

Furthermore, by electrical measurements performed on these capacitances the reliability of the gap material can be deduced.
In table 3.9 are depicted the resonators included in the design, specifying type of resonator and characteristic dimensions. Theoretical resonance frequencies of those resonators are summarized on table 3.10. The values for the mechanical properties are $E = 120GPa$ and $\rho = 2.23 \cdot 10^3$. Resonance frequencies for *LBAR* resonators do not take into account the "ear" effect, i.e., wider arms at the end of the resonator. This effects decreases the resonance frequency from 10% to the 20%.

In chapter 5 are shown the experimental results concerning this technological approach.

	Col.1	Col.2	Col.3	Col.4	Col.5	Col.6	Col.7	Col.8	Col.9	Col.10
Row1	LBAR L=15 w=1.5	LBAR L=15 w=1.5	LBAR L=15 w=2	LBAR L=20 w=3	LBAR L=20 w=1.5	LBAR L=20 w=2	LBAR L=20 w=2	LBAR L=20 w=3	LBAR L=20 w=5	Cantilever L=20 w=2.5
Row2	LBAR L=20 w=5	LBAR L=30 w=2	LBAR L=30 w=3	LBAR L=30 w=4	LBAR L=15 w=4	LBAR L=15 w=4	LBAR L=30 w=6	LBAR L=15 w=3	LBAR L=15 w=5	LBAR L=20 w=3
Row3	LBAR L=30 w=4	RBAR $r_i = 15$ $r_o = 21$ $b = 3$	RBAR $r_i = 15$ $r_o = 21$ $b = 3$	RBAR $r_i = 15$ $r_o = 21$ $b = 3$	VCAP L=40	VCAP L=65	VCAP L=90	VCAP L=140	VCAP L=165	
Row4	DLBAR L=10 w=2	DLBAR L=10 w=2	DLBAR L=10 w=2	DLBAR L=10 w=2	DLBAR L=10 w=2	LCAP L=40	LCAP L=90	LCAP L=140	LBAR L=40 w=10	
Row5	RBAR $r_i = 15$ $r_o = 32.5$ $b = 3$	RBAR $r_i = 15$ $r_o = 32.5$ $b = 1.5$	LBAR L=25 w=1.5	LBAR L=30 w=6	LBAR L=30 w=5	Cantilever L=40 w=2.5	Cantilever L=40 w=2.5	LBAR L=15 w=10	LBAR L=30 w=6	

Table 3.9: *Resonator distribution along the chip. Legend:* LBAR*: Longitudinal Acoustic Cantilever.* DLBAR*: Double Longitudinal Acoustic Cantilever, consists on a couple of two LBAR.* RBAR*: Ring Bulk Acoustic Resonator, r_i, r_o are the inner and outer radius, respectively; b is the beam width supporting the ring.* Cantilever*: Flexural cantilever.* VCAP*: Vertical Capacitance.* LCAP*: Lateral Capacitance. All the dimensions are given in microns.*

RBAR

r_i, (μm)	r_o, (μm)	f_{res}, (MHz)
15	32.5	500
15	21	1000

LBAR

L, (μm)	w, (μm)	(f_{res}), (MHz)
10	2	180
15	1.5,2, 3	122
20	2, 3, 5	91
30	2, 3, 5, 6	60

Table 3.10: *Theoretical resonance frequencies for designed structures.*

3.4 Summary

In this chapter, two technological processes have been introduced and described. One process has the main goal of fabricating microresonators based on SOI wafers and characteristic gap distances below $100nm$, whereas the other technological process is focused on the exploration of solid and dielectric materials for the gap formation. The chapter is complemented by a study of the state-of-the-art for the fabrication of those capacitive trasduced resonators. The technological processes presented are in the vanguard of the present state-of-the-art technologies.

CHAPTER 4

Monolithic CMOS approach for RF-MEMS integration

In this chapter, the monolithic approach for the resonators fabrication by means of a commercial and standard CMOS technology is presented. An intra-CMOS strategy is followed, so that the resonators are fabricated during the CMOS process, using the standard layers of the technology. A maskless post-CMOS process is only needed to release the resonators. The chosen standard technology, from *Austria MicroSystems* [85], is characterized by a minimum transistor length of $0.35\mu m$, four interconnecting metal layers separated by inter-metal planarized oxide layers and a capacitance module composed of two polysilicon layers separated by a thin silicon oxide.

Different approaches for designing monolithically integrated resonators will be described; in-plane resonators designed using the metal layers and in-plane and vertical resonators combining the two ploysilicon layers of the technology will be presented and discussed. Furthermore, in the last section of the chapter, the limits for the microresonator design will be analyzed in terms of the restrictions imposed by the technology.

4.1 Precedents on CMOS-MEMS resonators fabrication

The incipient field of CMOS-MEMS was firstly developed under the sensor technologies. Sensing systems on-chip combines micromachined structures and microelectronic building blocks on a single chip. The full potential of this microsensor integration approach has been enhanced by the recent expansion of Sensing Systems On Chip (SSoC) into new application areas, ranging from chemical and biochemical sensing to atomic force microscopy [14].

In order to reduce the number of off-chips components required to operate a sensing system, more and more microelectronic building blocks are integrated together with the microsensor

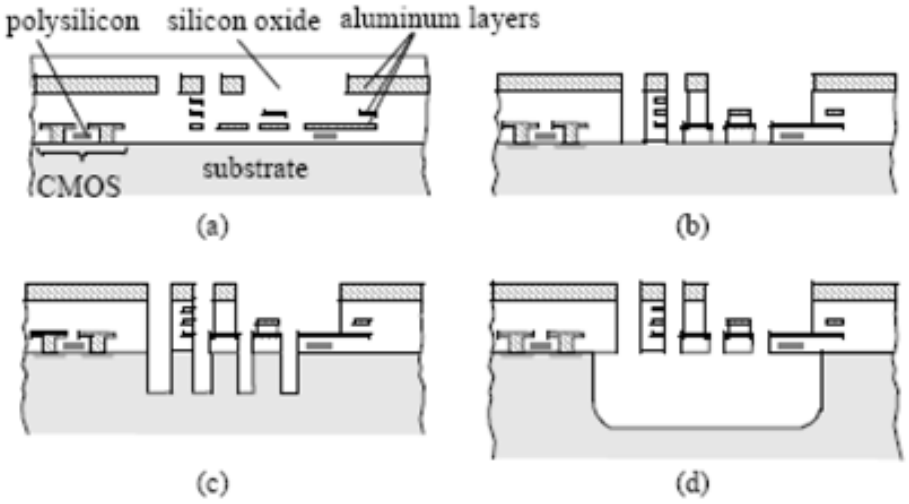


Figure 4.1: *Technological process sequence for integrating MEMS resonators in the TSMC-0.35μm, [19].*

on the same chip. Depending on the application, the resulting sensing SoC might feature "only" analog signal processing in addition to the actual transducer or they might incorporate sophisticated digital signal processing enabling on-chip testing, calibration, and off-chip communications via a bus interface. To be able to produce SoC with integrated sensing functions (SSoC), the technology used to fabricate the microsensor must be merged with standard Integrated circuits (IC) technologies, CMOS or bipolar process technology. The challenges and prospects of the resulting integrated microsystems, often named CMOS-MEMS, are the main part of this phd thesis.

In previous chapter 1, different approaches for monolithically integrating MEMS resonators with CMOS circuitry were described. The three different approaches, named pre-, intra- and post- CMOS were discussed showing the advantages and drawbacks for each one. One of the works depicted and discussed again here has been carried out at the Carnegie Mellon University by G. Fedder [19], where a MEMS structure monolithically integrated with a CMOS amplifier circuitry is used as a mixer for down-converting RF frequencies (up to $3GHz$) into the IF band $< 1MHz$. The cross-section of this intra-CMOS MEMS technology process is depicted in figure 4.1. The structural layer of the in-plane resonator and electrodes corresponds to the metal and inter-metal oxide standard layers of the technology. The resonator consists on a stack of metal and oxide layers that are defined in a post-CMOS RIE etching using as a mask a top metal layer of the technology. The post-CMOS process is composed of three etching steps.

The process starts with the CMOS chip, as shown in step.a of figure 4.1. The CMOS technology is the TSMC-0.35μm technology, characterized by four metal inteconnection layers.

The in-plane resonator and electrodes are defined by drawing a stack of the four metal of the technology. Then, the structural layer of the resonator is a layer stack composed of the four metal layers as well as the inter-metal oxide layers. The top metal acts as a mask for the oxide RIE etching (step b of figure 4.1). The minimum allowable gap is constrained by RIE etching process, because of the polymer present on the top metal sidewalls. So the minimum achievable gap is $1\mu m$, which is bigger than the minimum distance allowed by the $0.35\mu m$ process but limited by the RIE performance. The second post-CMOS step corresponds to a RIE etching of the exposed silicon substrate. This step sets the spacing from the microstructure to the substrate. The final step (d) is a timed isotropic silicon etch in a SF_6 plasma to undercut and then, release the structures.

By this CMOS-MEMS process, a demonstrator of a mixer based on a torsional paddle structure was fabricated and tested. The resonance frequency of the device was $435kHz$, exhibiting a quality factor of $Q = 1000$ in vacuum. Taking advantage of the CMOS integration, that allows to reduce the parasitic capacitance because of the promiximity between the resonator and the circuitry, they demonstrated a download conversion signal of $3GHz$. A frame-square shaped resonator at $6.5MHz$ has also been demonstrated with a quality of factor of $Q = 1000$, reducing the gap distance down to $0.68\mu m$. The possibility to integrate on the same substrate the resonant structure with the circuitry reduces the parasitic capacitances, improving the electrical performance of the MEMS device.

4.2 AMS-$0.35\mu m$ standard technology. General description

From an academic institution or public research center, the access to commercial technologies is done via Europractice [86]. The available foundries here are: AMIS, AMS, IHP, TSMC and UMC. In general, all the foundries offer CMOS process ranging from $0.8\mu m$ down to $0.35\mu m$, which further accomplish the needs imposed by the CMOS designers team. UMC and TSM offers technologies down to $90nm$ and $130nm$, respectively. In order to make a right decision, available metal and polysilicon layers are analyzed as well as the possibilities to access to different runs through the year. Specifically, AMS-$0.35\mu m$ has two polysilicon layers (thinking on the microresonators structural material) and four metal layers, enough for the interconnectivity of the CMOS circuitry. Finally, the experience in the framework of the group with AMS-$0.35\mu m$ pointed out the selection to this technology.

AMS-$0.35\mu m$ process family is divided into 4 different categories, as it is shown in table 4.1. The family start with the process C35B3C0, composed of the CMOS core and CPOLY modules. The CMOS core module consists on p-substrate, single poly, triple metal and 3.3 Volt process. The CPOLY module, also named POLY1-POLY2 capacitor module, consists on the CMOS module with the addition of a second polysilicon layer, in order to form integrated capacitances. The thick metal module is characterized by having a top metal thickness of $2\mu m$. The MIM capacitor module is similar to the CPOLY module, but in that case, the structural layers for the capacitances are the matal layers MET2 and METC, which

Process name	CMOS Core Module	CPOLY Capacitor Module	5-Volt Module	High resistivity module	Metal-4 module	Thick Metal Module	MIM Capacitor Module
C35B3C0	x	x					
C35B3C1	x	x	x				
C35B4C3	x	x	x	x	x		
C35B4M3	x	x	x	x		x	x

Table 4.1: *AMS*-0.35μm *process family.*

is an additional metal layer between MET2 and MET3. The equivalent oxide thickness of this module is 29nm. The 5 Volt module consists on N-MOS and P-MOS transistors with a different gate oxide thickness in order to obtain the expected performance with 5V as gate voltage in front of the standard 3.3Volt. The high resistivity module allows to design integrated resistance by a low doped polysilicon. The 4-metal layer adds an additional metal layer to the standard core of the technology, increasing the possibilities of interconnection.

The process finally chosen for fabricating monolithically integrated microresonators will be the one that accomplish the needs for designing the resonators as well as the CMOS circuitry. From the microresonator point of view, the CPOLY and MIM modules may incorporate new opportunities to the design of such structure in terms of a reduced gap achievable (thinking on the thin silicon dioxide present on those capacitance modules) and structural materials. From the circuitry point of view, it becomes necessary to include a fourth metal layer in order to improve the interconnectivity in the CMOS circuitry. Another aspect important for the CMOS circuitry is the possibility to fabricate integrated resistances (for example, the one used in the transimpedance amplifier, depicted in next chapter 5). The 5 Volt option is not a relevant module for our purposes, but is included by default on the CMOS core. Tipically the thick metal module (2μm-thick instead the 1μm) is used for fabricating integrated inductors. Although a thicker material can improve the mechanical properties of the microresonator, the minimal distance between two top metal lines also increases, then determining a larger gap distance on our resonators. Initially, the MIM module was forseen as another main attractive of this technology. However, the possibility to implement microresonator with polysilicon (which exhibits better mechanical properties and can simplify the post-CMOS releasing process), in addition to the fact that MIM module was not always available, conditioned the election of the COPLY module.

Finally, the process chosen is *C35B4C3*, which is characterized with the 4 metal layers as

well as for the high resistivity module needed for the circuitry design. The 4 metal layers are needed for the interconnectivity and the high resistivity module is needed for the design of the resistance of the transimpedance amplifier (the designed circuitry is presented in section 5.2.1). The CPOLY module, mandatory for fabricating polysilicon resonators, is incorporated in all the family processes. The process *C35B4M3*, characterized by the thick metal module and the MIM capacitance module, has not been always available by the foundry and has limited the options to fabricate resonators based on the MIM module.

4.2.1 Layers description

The general AMS-0.35μm profile is shown in figure 4.2. The CMOS technology is characterized to be one-well technology: all the NMOS transistors share the p-well substrate whereas the PMOS transistors are fabricated in isolated n-well regions.

The cross section of the AMS-0.35μm technology is shown in figure 4.2, where are represented all the layers and their nomenclature. In general, layers are named starting from bottom to top in the cross section profile. IMD refers to the inter-metal oxides, ILDFOX is the oxide between the polysilicon layers and the first metal layer (MET1) and FOX refers to the field oxide. The technology, as it was introduced before, presents 4 metal layers for interconnection purposes,

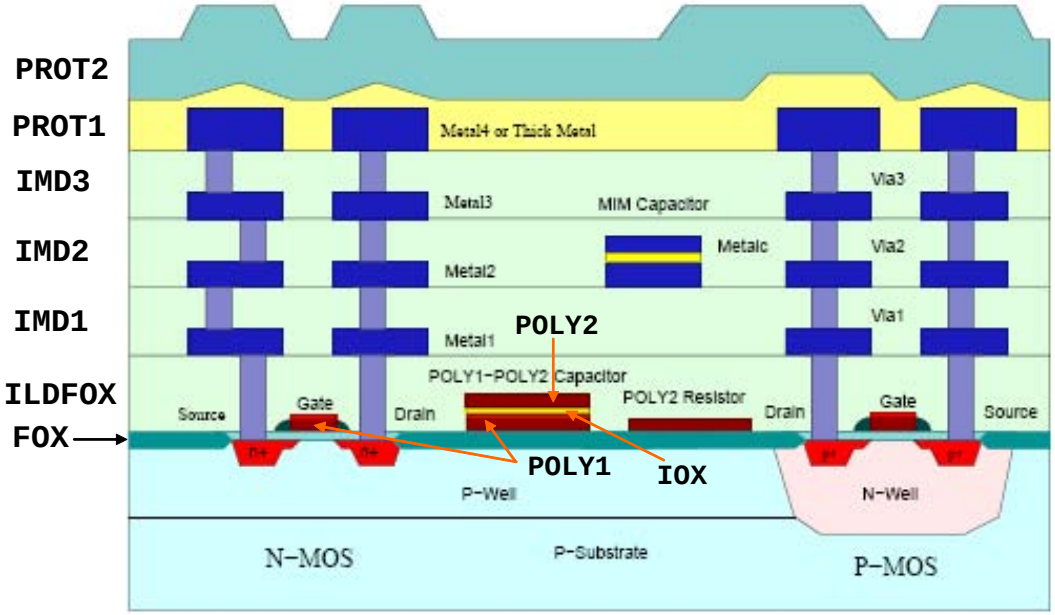


Figure 4.2: *AMS-0.35μm technology cross section showing all polysilicon and metal layers.*

named from MET1 to MET4. The CPOLY module is composed of the two polysilicon layers (POLY1 nad POLY2) separated by a thin silicon dioxide layer, named IOX. Two passivation layers protects the circuitry from the external environment and only the electrical pads are uncovered. At least one of the passivation layers is a silicon nitride component, that is not etched by the HF-based wet solution used in the releasing process. Thicknesses, minimum line widths and minimum line distances between layers (when applicable) are depicted in table 4.2.

4.2.2 Process for structure relasing

In order to complete the fabrication sequence, a releasing process is necessary to release the movable structures. The process is characterized to be out-foundry, i.e., is done after the CMOS process is finished.

Another relevant aspect that characterizes this process is that any additional post-CMOS photolithography step is needed to protect any structural layer of the microresonator and the CMOS circuitry. The releasing process was thought to be maskless. In fact, the chemical solution does not etch the passivation layer, so the circuitry is protected against the wet solution. In the microresonators areas, where structures have to be released, a pad aperture is opened in order to promote the sacrificial oxide layers to be etched. Electrical bonding pads (made of Aluminum) are not protected against the wet etching solution, so the etchant has to be selective with aluminum layers. This condition is more critical when the resonator is designed in aluminum layer.

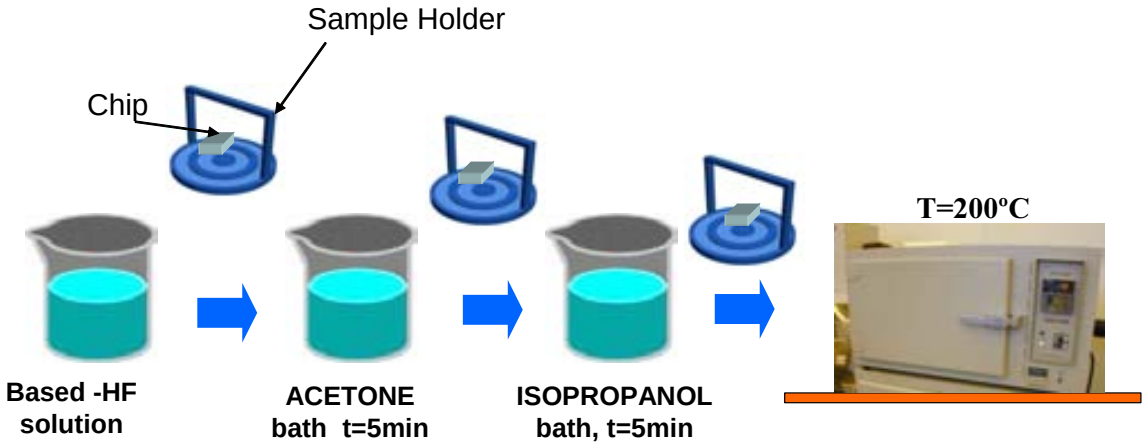


Figure 4.3: *Schematic sequence of the releasing process. The sample is wet during the whole process before drying it in the oven.*

The chemical etchant is a HF-based solution, that is selective to aluminum. The right pro-

Layer Name	**Thickness** h, nm	**Min. line width** w_{min}, nm	**Min. line separation** d_{min}, nm
Field Oxide (FOX)	290	$n.a*$	$n.a.$
Gate Oxide (GOX)	290	$n.a.$	$n.a.$
Polysilicon1 (POLY1)	282	350	450
CPOLY Oxide (POX)	41	$n.a.$	$n.a.$
Polysilicon2 (POLY2)	200	650	500
Metal1-poly oxide (ILDFOX)	645	$n.a.$	$n.a.$
Metal1 (MET1)	665	500	450
Metal2-Metal1 oxide (IMD1)	645	$n.a.$	$n.a.$
Metal2 (MET2)	640	600	500
Metal3-Metal2 oxide (IMD2)	620	$n.a.$	$n.a.$
Metal3 (MET3)	640	600	500
Metal4-Metal3 oxide (IMD3)	1000	$n.a.$	$n.a.$
Metal4 (MET4)	925	600	600
Passivation1 (PROT1)	900	$n.a.$	$n.a.$
Passivation2 (PROT2)	1000	$n.a.$	$n.a.$

Table 4.2: *Thicknesses for all the layers of the standard AMS* 0.35μm *technology [85].* $*$ *n.a refeers to Non Aplicable.*

Structural layer	Resonator width	Sacrificial layer(s)	Oxide to remove	Time
MET4 (Top metal)	$1\mu m$	IMD3	$500nm$	4min
MET1 (Metal 1)	$1\mu m$	IMD2, IMD1 ILDFOX	$2.5\mu m$	$18 + 10$min
Poly1 or Poly2	$1\mu m$	IMD1, ILDFOX DFOX	$2.5\mu m$	$18 + 10$min

Table 4.3: *Releasing time for resonators fabricated by different approaches on the AMS-0.35μm technology.*

portion of chemicals controls the pH of the solution, etching the silicon dioxide and preserving the aluminum [87], [88].

Table 4.3 shows the time needed for releasing resonators with different sacrificial layers. The etch rate of a fresh solution is less than $200nm/min$, but the etch rate decreases with the etch time, so each $18min$ the solution has to be changed in order to follow the etching. For MET4 resonators, the sacrificial layer is the inter MET3-MET4 oxide (IMD3) under the resonator. For other alternatives, the resonator presents sacrificial oxide layers on top and at bottom. For example, MET1 resonators, present a sacrificial oxide layer on top, IMD2 and IMD1. IMD3 and passivation layers are removed during the CMOS process because an open VIA3 and PAD apertures are drawn on the design.

The releasing process sequence consists on different steps, as shown in figure 4.3:

1. The first step is the etching of the sacrificial oxide layers. The duration of the etching is determined by the oxide thickness to be removed. In table 4.3 are depicted the timing for each technological approach. The maximum time etching for a solution is $18min$.

2. After the etching time, the sample is submerged in an acetone bath in order to clean the chip from sub-products of the reaction. The time the sample is kept in acetone is 5 minutes. The sample is always kept wet in order to reduce possible stiction on the structure on the surface; the holder sample has some edges on its surface in order to promote the formation of drops covering the chip when transporting the sample from one bath to another.

3. After the cleaning in acetone, the sample is immersed in the isopropanol bath for 5min, approximately. After those 5min, if the etching has not finished (because more time is needed for totally releasing the structures), the sample is immersed again in the based-HF solution, starting the whole cycle again.

4. If the structures are released, the holder with the sample (and a drop of liquid covering it) is put into the oven for an approximated time of $10min$ in order to dry the sample. The chip is ready to be characterized, whether at SEM whether by electrical measurements.

4.3 Top Metal in-plane resonators

When designing resonators employing metal layers, both resonator and electrodes structures are designed on the same material. Then, the minimum distance between two metal lines determines the maximum achievable current coming out from the resonator. The structural material chosen to fabricate the resonators by this approach is the top metal (*Metal4*). Using the top metal as a structural layer a shorter post-CMOS releasing process is needed, minimizing damage on the metal structures. Furthermore, the election of another metal layer does not imply a substantial improvement of the read-out current. Table 4.4 shows the typical thickness, the minimum width and minimum distance between two metal wires for each metal layer. For inner metal layers, as *Metal1*, the minimum distance between two wires is only $0.45\mu m$ in comparison to $0.6\mu m$ of *Metal4*, but also the thickness is reduced from $0.9\mu m$ down to $0.665\mu m$.

In order to evaluate the right selection among the available metal layers, a figure of merit is defined in terms of the output current, but also in terms of the vertical stiction. After the post-CMOS wet etching, the sacrificial layers are removed, exposing the silicon substrate. The probability of vertical stiction, considered by the vertical stiffness of the resonator, is also taken into account. The output current is evaluated in terms of the motional resistance, previously introduced in chapter 2. As the output current wants to be maximized, it corresponds to R_m^{-1} maximum. The figure of merit, then is the product of the inverse motional resistance per the vertical stiffness. Then, motional resistance is rewritten here:

$$R_m = \frac{\sqrt{k \cdot m} s^4}{V^2 Q \epsilon_0 A^2} \tag{4.1}$$

For in-plane resonators, the coupling area is $A = Lt$. For comparison purposes, let's consider a generic resonator with an equivalent stiffness constant k and effective mass m. For simplicity, the quality factor and the voltage applied is considered the same for all the implementations. Then, the inverse motional resistance can be written as:

$$R_m^{-1} \alpha \frac{h}{s^4} \tag{4.2}$$

In order to extract the dependence on the vertical stiction of the resonators, an expression of the collapsing voltage is used. It has been demonstrated, that the voltage collapse function depends as [89]:

Metal Layer	**Thickness** h $(nm\ )$	**Min. line separation** s, nm	**Vertical distance** s_v, (μm)	$R_m^{-1} \cdot V_{collapse}$ (μm)
Metal1 (MET1)	665	500	1	8.79
Metal2 (MET2)	640	600	1.5	9.63
Metal3 (MET3)	640	600	2	14.82
Metal4 (MET4)	925	600	3	**32.99**

Table 4.4: *Thicknesses for all the layers of the standard AMS-0.35μm technology [85].*

$$V_{collapse} \quad \alpha \quad \sqrt{h^3 s_v^3} \tag{4.3}$$

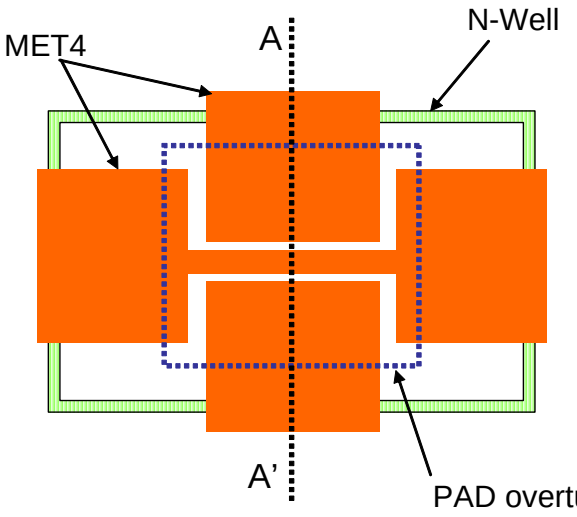
where the parameter s_v refers to the vertical gap that exist between the resonator layer and the silicon substrate and h is the resonator thickness.

Then, taking into account equations 4.2 and 4.3, an approximated figure of merit for simple calculations purposes can be derived:

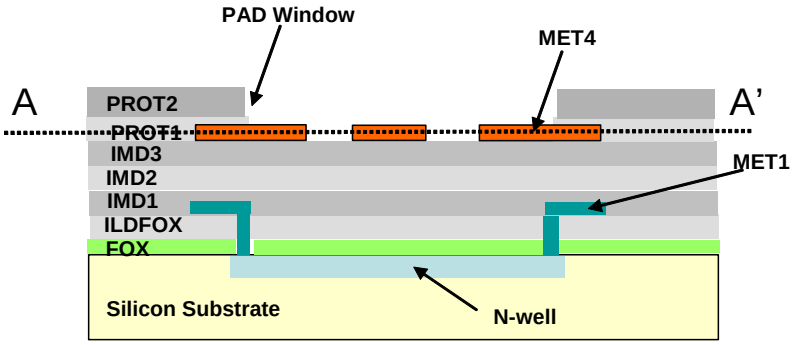
$$R_m^{-1} \cdot V_{collapse} \quad \alpha \quad \frac{h\sqrt{s_v^3 h^3}}{s^4} = \frac{\sqrt{s_v^3 h^5}}{s^4} \tag{4.4}$$

In table 4.4 are depicted the values for the typical thickness and the minimum distance between two metal lines, for all the available metal layers. The table is complemented by the vertical separation that exhibits each metal layer to the silicon substrate and with the figure of merit for each case, calculated from equation 4.4. For the calculated values, the best choice corresponds to the top metal that presents a reduced probability to obtain collapsed structures. However, sometimes not all the intermetal oxide is etched, so the vertical distance is lower than the theoretical one.

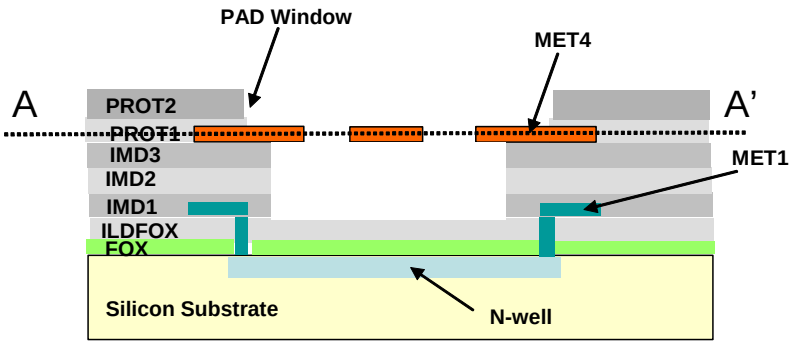
Figure 4.4 shows the mask design for a clamped-clamped beam using *MET4* (top metal) layer as structural material. The *Metal4* layer is used to design the resonator as well as the electrodes; then, the minimum separation between the structures is $600nm$. A pad aperture is also designed in order to remove the passivation layer above the resonator. The minimum pad aperture allowed by the technology is $(15 \times 15)\mu m^2$. The design is complemented by a surrounding n-well in order to avoid parasitic electrical signal in the MEMS performance.



(a) Design of a c-c beam using the MET4 as structural layer



(b) Cross-section before the post-CMOS process



(c) Cross-section before the post-CMOS process

Figure 4.4: *Design layers for a c-c beam in MET4 (a). Cross section before (b) and after (c) the releasing post-CMOS process.*

Resonator-Electrode	**Thickness** h (nm)	**Vertical separation** s_v, (nm)	$R_m^{-1} \cdot V_{collapse}$ (μm)
MET4-MET3	925	1000	1.04
MET3-MET2	640	1000	1.25
MET2-MET1	640	1000	1.25
MET1-POLY1	665	645	3.67

Table 4.5: *Figure of merit for different possibilities of vertical resonators fabrication in AMS-0.35μm.*

4.4 Vertical Metal-Polysilicon resonators

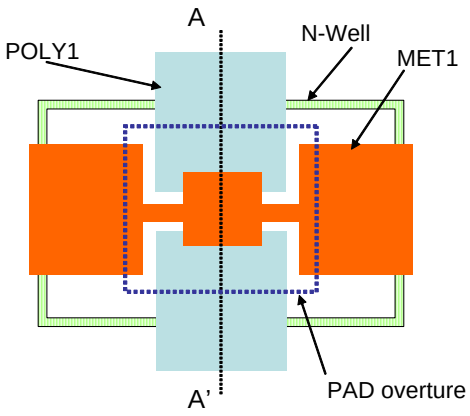
In order to design vertical structures, the designer has to play with different layers for fabricating resonator and electrode. For facilitating the releasing process, the top layer should be the resonator whereas the bottom layer is used to implement the electrodes. The possibilities are MET4/MET3, (always Resonator/Electrode), MET3/MET2, MET2/MET1 and MET1/Poly1 (or Poly2). In table 4.5 are shown all those possibilities with the figure of merit calculated in previous subsection, equation 4.4.

For vertical resonators, the transducer gap distance s coincides with the stiction distance, s_v, and is given by the inter-metal or inter-metal-polysilicon oxide thicknesses. Also in evaluating the motional resistance, the thickness of the layer is not relevant, because it does not imply capacitive transduction for vertical transduction. Then, for those vertical resonators, the figure of merit can be rewritten as:

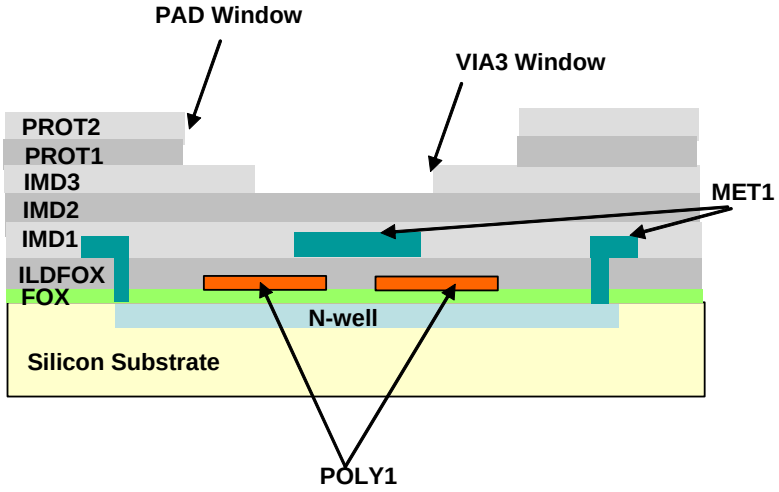
$$R_m^{-1} \cdot V_{collapse} \quad \alpha \quad \frac{1}{h^2 s_v^4} \cdot \sqrt{h^3 s_v^3} = \sqrt{\frac{1}{h \cdot s_v^5}} \tag{4.5}$$

Table 4.5 shows the four possible election of the layers and the best option among them. The minimum distance between MET1 and POLY1 makes this choice the most suitable in order to enhance the electrical response of the device.

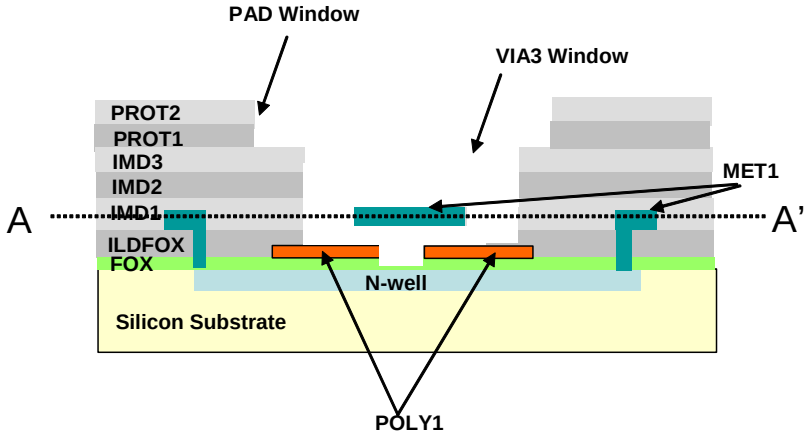
A design based on a paddle shaped microresonator is shown in figure 4.5. The structural material is the first metal (MET1), which presents a vertical distance of $640nm$ with respect to the POLY1, which is the structural material for the electrodes. Two electrodes are placed symmetrically with respect to the axis of the paddle in order to promote the torsional mode instead of the translational one.



(a) Design of a paddle structure in MET1-POLY1 approach



(b) Cross-section before the post-CMOS process



(c) Cross-section after the post-CMOS process

Figure 4.5: *Design layers for vertical paddle structure in MET1-POLY1 approach (a). Cross section before (b) and after (c) the releasing post-CMOS process.*

Layer	**Thickness** h $(nm\ )$	**Min. line separation** s, (nm)
POLY1	282	450
POLY2	200	650
IOX	40	n.a. $*$
FOX	300	n.a.

Table 4.6: *Specifications for the CPOLY module and FOX layers.* $*$ *refeers to Non applicable situations.*

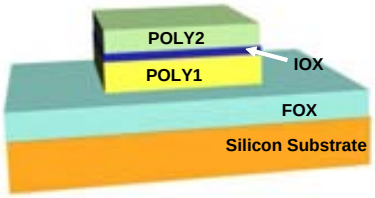
A PAD window as well as a VIA3 are opened on top of the resonator in order to facilitate and reduce the time of the post-CMOS releasing process. It shall be pointed that the resonator is protected always with a silicon dioxide on top of the resonator, so a VIA2 window is not opened.

4.5 Vertical and in-plane polysilicon resonators

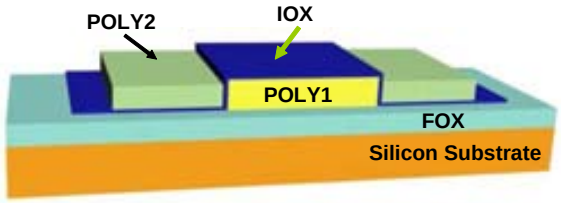
In previous sections, the design of integrated MEMS resonators in the commercial *AMS*-$0.35\mu m$ by means of a top metal layer was introduced. The main drawback for those approach was the impossibility of reducing the minimum distance between driver and resonators below design rules which limits the functionality for the devices for medium frequencies (below $100MHz$) and avoids the design of resonators at higher frequencies.

A new approach focused on the possibility of reducing the minimum gap distance between driver and electrode was pursued. The standard capacitance module, composed of two thin polysilicon layers separated by a very-thin oxide together with the conformal deposition of these layers was pointed out as a solution to overcome the design specifications. This module is traditionally used for designing integrated capacitances for the analog circuit designer. Figure 4.6(a) shows the two polysilicon layers, *Poly1* and *Poly2* corresponding to the bottom and top polysilicon, separated by the inter-polysilicon oxide layer, named *IOX*.

Table 4.6 shows the typical thicknesses for capacitance module layer, i.e., bottom and top polysilicon and inter-polysilicon oxide, POLY1, POLY2 and IOX, respectively. The polysilicon layers present thicknesses of $282nm$ for poly1 and $200nm$ for poly2, whereas the thickness of the interpoly silicon oxide layer is nominally $40nm$. In addition to those layers, the thickness of the field oxide layer has been added.



(a) CPOLY module layers, POLY1, POLY2 and Inter-poly oxide, (IOX) in vertical configuration



(b) CPOLY module layers in lateral configuration

Figure 4.6: *CPOLY module layers in vertical and lateral configuration. The module yields on top of the field oxide, FOX.*

The small value of thickness of this layer (less than 300nm) will limit the design of the resonant because large structures will collapse down to the exposed silicon substrate. At the end of this chapter a discussion of the limits for this approach will be done. Table 4.6 also shows the minimum distance between two adjancent lines of polysilicon, $450nm$ for POLY1 and $650nm$ for POLY2. The design rule distance between POLY1 and POLY2 corresponds again to $650nm$. Then, by those imposed distances, the gaps of the resonators will be as large as for the metal resonator, and due to the reduced thicknesses of those polysilicon layers, the electrical coupling would be even worse than for metal resonators.

However, the conformal deposition of layers IOX (inter-polysilicon oxide of the CPOLY module) and POLY2 with respect to POLY1 opens new possibilities for the resonator designer. For this new approach on the design, one of the polysilicon is selected indistinctively to be the resonating structure whereas the other one is designed to be the electrode structures.

Figure 4.6 shows this new insight on the design step. In figure 4.6(a) is shown the vertical approach fabrication. On that case, the top polysilicon is POLY2 used to define the resonator (and hence, facilitating the post-CMOS releasing) and POLY1 is used to define the electrodes. The IOX layer makes the role of gap vertical spacer, that is removed in the post-process. Figure 4.6(b) shows how to use the CPOLY module in order to define in-plane resonators. On that case, the polysilicon layers are defined indistinctively for electrodes and resonator,

but POLY2 is drawn laterally to POLY1. The IOX layer again makes the role of lateral gap spacer.

The price to pay for this new insight on the design is that the design rules are violated, mainly because POLY2 layer overlaps laterally the POLY1, and the technology rules 'sees' a capacitance not properly defined.

In table 4.7 is shown a study of the viability of using POLY1 and POLY2 as structural layers for fabricating vertical and lateral resonators. The possibilities of fabrication are three, because POLY1 is discarted as resonator structual material for vertical resonators. Then, for vertical resonators the choice is POLY1 as structural material for the microresonator and POLY2 as material for the electrodes. The options for lateral resonators are two, POLY1 and POLY2 exchanges the roles of microresonator and electrode material.

In order to study the viability of each of those three approaches, a calculation of the figure of merit (represented in equation 4.4) was performed. For vertical resonators, the major disadvantage is the $40nm$-gap between resonator and electrode which dramatically enhances the probability for vertical stiction. This drawback is clearly represented in the final value of the figure of merit (equation 4.4), obtainning a value 25 or 40 times lower in front of the values corresponding to the other two lateral approaches. For the lateral approaches, both seem to be favorables. The best case occurs when POLY1 is chosen as structural material, because its major thickness implies better behaviour in front of vertical stiction.

The advantage of the lateral approach in front of the vertical one is, in fact, the vertical collapsing distance. Lateral resonators are limited by the FOX thickness layer ($300nm$); on the other hand, the vertical approach is limited by the gap spacer thickness, which is only $40nm$. Furthermore, because the area of coupling wants to be maximized, this provokes more long resonators, and hence, more probabilities to obtain a collapsed structure. The lateral

Resonator-Electrode	**Thickness** h (nm)	**Lateral separation** s, (nm)	**Vertical separation** s_v, (nm)	$R_m^{-1} \cdot V_{collapse}$ (μm^{-3})
POLY2-POLY1 Vertical	200	40	40	56
POLY2-POLY1 lateral	200	40	340	1385
POLY1-POLY2 lateral	282	40	300	2711

Table 4.7: *Figure of merit for different possibilities of vertical and lateral resonators fabrication in AMS-*$0.35\mu m$ *using the CPOLY module layers.*

approach takes advantage of the $40nm$-gap spacer reducing the stiction to the limits of the technology, i.e. the thickness of the FOX layer.

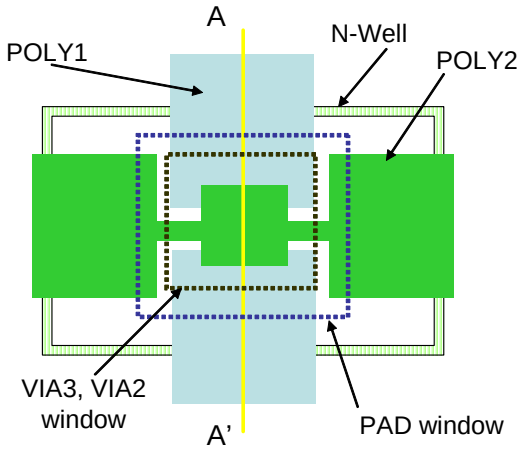
Two examples of those both approaches are depicted in figure 4.7. The left side of figure 4.7 corresponds to the fabrication of a vertical resonator, specifically a paddle shaped structure. The resonator is fabricated choosing POLY2 (the top polysilicon layer) as structural material for the resonator and POLY1 for the electrodes. In order to promote the torsional resonant mode of the paddle (that offers higher Q than the translational mode), two electrodes are drawn symmetrically with respect to the longitudinal axis of the device. The two electrodes are separated by the minimum distance allowed by the design rules, which is $450nm$. The IOX and POLY2 layers are deposited conformal on top of the POLY1 layer. The vertical gap distance between resonator and electrodes is determined by the thickness of the inter-polysilicon oxide.

In order to release the structure in the post-CMOS process, a PAD window is open in top of the resonator area, with dimensions of $(15 \times 15)\mu m^2$. When opening the PAD window, the passivation layers (PROT1 and PROT2) are removed, making possible the releasing of the resonator by the wet etchant. In order to fasten the releasing process, a VIA3 and VIA2 windows are also opened, removing interoxide layers IMD3 and IMD2, respectively, as shows figures 4.7(a), 4.7(c) and 4.7(e). The presence of those PAD and VIA2-VIA3 windows without any metal to interconnect implies the clearly appearance of the design rules violation.

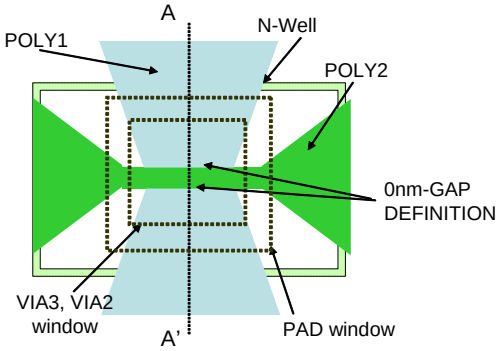
Actually, the vertical fabrication approach was a first trial in order to explore the capabilities of the CPOLY module for fabricating integrated resonators with gap distances below the $100nm$ barrier. It shall be pointed that the information about this CPOLY module prior to sending the design to the foundry was very reduced. For example, intuitively it was thought that the deposition of those layers was more or less conformal but the exact behavior was totally unknown and unpredictable.

For this reason, a FIB profile was performed on a fabricated structure like the one depicted in figure 4.7(a). The result of the FIB profile is shown in a SEM picture, figure 4.8. A releasing process of $10min$ was performed previously to the FIB profile in order to open the cavity resonator and after the FIB profile an aggressive HF (at 49%) etching of $30s$ was done in order to remove the oxide sacrificial layers and improve the image contrast at SEM. The resonator is a paddle shaped resonator and the FIB profile was done in one of the arms.

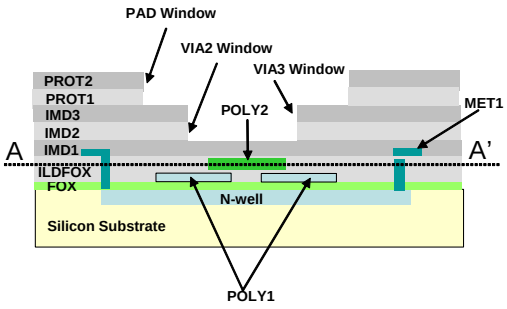
Above the silicon substrate, a cavity represents the FOX layer, which was etched in order to increase the contrast of the image. The two electrodes are fabricated in POLY1 and the minimum separation between them is $450nm$. The inter-polysilicon oxide IOX ($40nm$-thick) and POLY2 ($200nm$-thick) are conformal deposited above and on the sideways of POLY1. However, the shape of the paddle resonator was not exactly the expected one. It was expected a smooth transition between the two polysilicons but the result was a perfect defined vertical sidewalls. Then, the performance of the paddle can be affected by this beam in the axis of



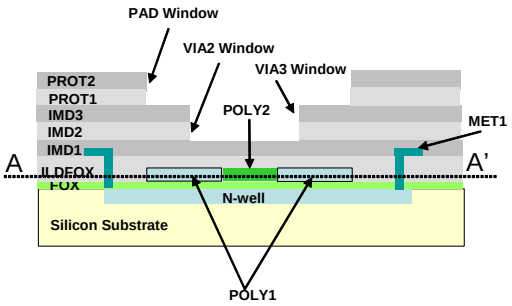
(a) Design of a vertical paddle structure in POLY2-POLY1 approach



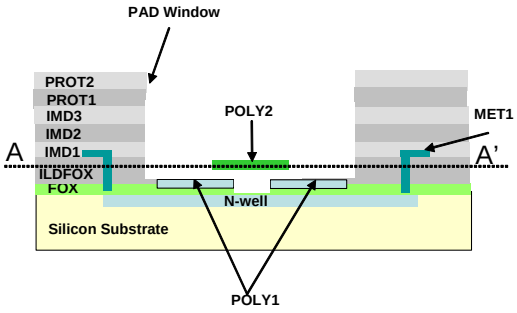
(b) Design of a in-plane c-c beam structure in POLY2-POLY1 approach



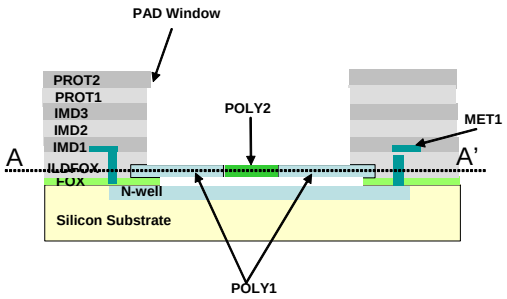
(c) Cross-section before the post-CMOS process (Vertical approach)



(d) Cross-section before the post-CMOS process (Lateral approach)



(e) Cross-section after the post-CMOS process (Vertical approach)



(f) Cross-section after the post-CMOS process (Lateral approach)

Figure 4.7: *Design of a vertical and in-plane structure by the POLY1-POLY2 technological approach.*

the paddle, making difficult the torsional mode.

Although the design of vertical resonators can be affected by the perfect conformal deposition of the CPOLY module layers, the image of figure 4.8 opened a new possibility on the design of $40nm$-gap resonators: lateral resonators.

With that idea, a lateral c-c beam, like the one shown in figure 4.7(b) was designed taking advantage of the vertical sidewalls between POLY1 and POLY2. The electrodes were designed in POLY1 (separated $650nm$), and the POLY2 is chosen to be the electrode material. The design is characterized by drawing POLY1 and POLY2 layers at $0nm$ of distance. Then, in the fabrication process the IOX layer will make the role of gap spacer. In order to avoid asymmetries in the gaps, it is indispensable to accomplish this criteria.

Again a FIB profile was performed on c-c beam with POLY2 as structural material. The result of the FIB profile is shown in figure 4.9.

The cross section obtained by the FIB has been performed to a previously etched device (time $=18+10min$) $4\mu m$ long and $650nm$-wide. The gaps are again vertical along the sidewalls, showing distances close to $40nm$ for the two gaps. However, there is a difference between

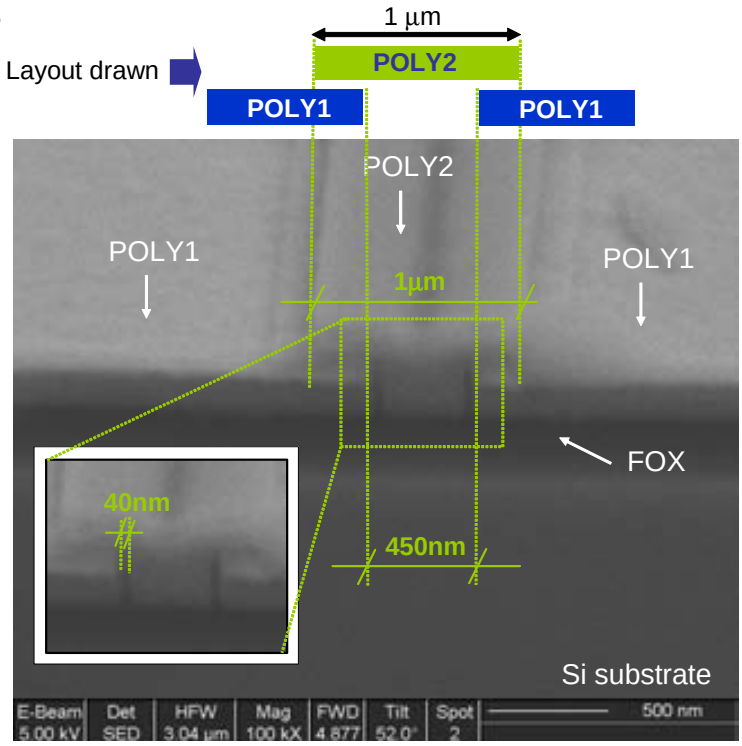


Figure 4.8: *SEM image after a profile made by FIB on a POLY2-POLY1 vertical paddle resonator. The cross-sectional layers of the structure are depicted in figure 4.7(c) and 4.7(e).*

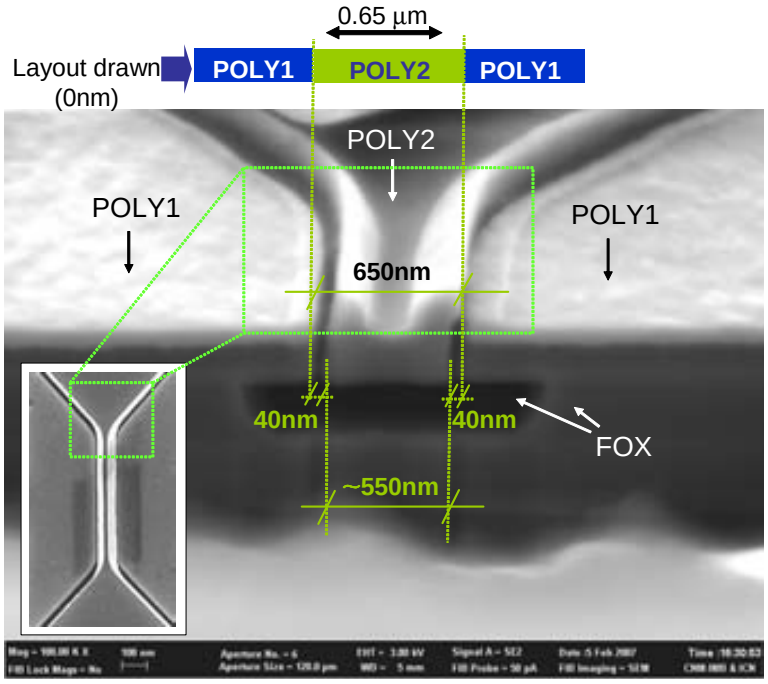


Figure 4.9: *SEM image after a profile performed by a FIB on a POLY2-POLY1 lateral c-c beam resonator.*

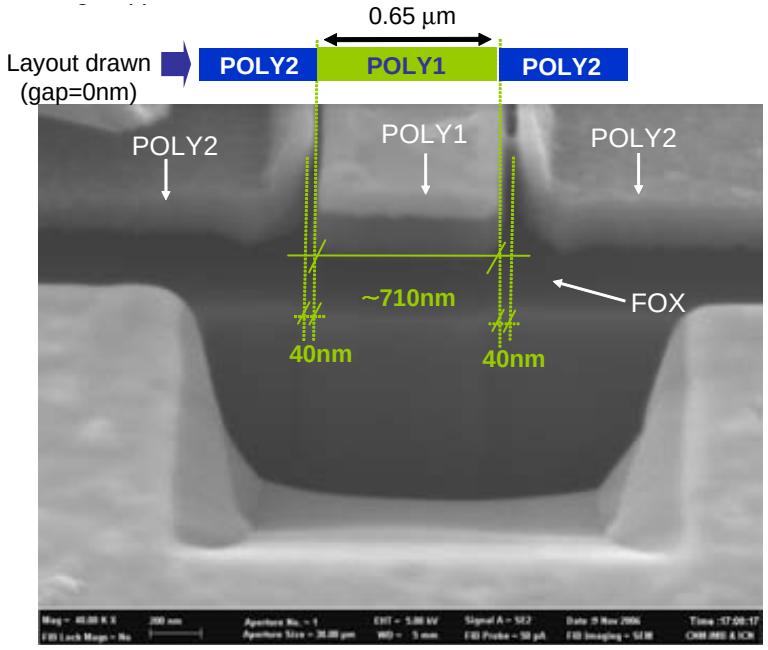


Figure 4.10: *SEM image after a profile performed by a FIB on a POLY1-POLY2 lateral c-c beam resonator.*

the drawn profile and the fabricated resonator; due to the coincident POLY1 and POLY2 layers on the layout and the thickness of the IOX oxide, the final device has a width of approximately $650nm - 2 \times 40nm$.

It shall be pointed that the technology has an alignment error when patterning POLY2, but this does not influence on the gap distance, that remains inalterable to that process step. This fact can be deduced from figure 4.9, looking at the vertical superposition at POLY2 and POLY1 edges; the inset of that figure shows the same device in a SEM image, top view. Drawing the lateral spacing between the two polysilicon to be $0nm$ ensures the gap to be the nominal value of the inter-polysilicon oxide thickness, independently of the alignment error of the technology.

Also, the cross section performed with the FIB shows that the resonator releasing is achieved without stiction after the time $18 + 10min$. The etchant penetrates by the POLY1-POLY2 areas and releases the resonator. Once IMD1, FOX and IOX oxides are etched, the structure is released.

A similar approach to the previous described consisted on exchanging the roles of POLY1 and POLY2. From previous calculations showed in table 4.7, the figure of merit choosing POLY1 as structural material was still better as expenses of the bigger thickness, $282nm$ in front of $200nm$, which represents an improvement of a 30% approx.

In addition to that, when choosing POLY1 as structural material for the microresonator, the final width (that determines the resonance frequency on the lateral mode), is closer to the width defined in the layout in contrast to the other approach.

Furthermore, the expected rectangular section of POLY2 results on a rectangular-horned shape that can limit the quality factor as a result of enhancing surface effects.

Figure 4.10 shows the profile of a c-c beam fabricated by the POLY1-POLY2 approach and choosing POLY1 as structural material. In this case, the width of the resonator corresponds to the drawn layers. The conformality deposition of POLY2 is now observed in the electrodes, showing a total coupling along the POLY1 thickness despite the thinner of POLY2 layer ($200nm$ in front of $282nm$ of POLY1). Both gaps seem to be symmetric and with a value of $40nm$.

4.6 Limits on CMOS-MEMS integration

In this section, an analytical study is done in order to answer, which devices fabricated in the MET4 and POLY1-POLY2 approaches are forbidden. For example, let's consider that a device with $50MHz$ wants to be implemented in the POLY1-POLY2 approach. Consider that the possible designs are a c-c beam and a LBAR resonator. The LBAR that will meet the specifications of frequencies would have an approximated length of $L = 20\mu m$, and the c-c beam would have a length of $10\mu m$. The possible vertical collapsing that can be produced when releasing the resonator might introduce a variable on the design in order to discard one of the above resonators. In the following, a model for estimating the vertical collapse will be described and the results for forbidden devices will be analyzed in terms of MET4 and POLY1-POLY2 approaches.
First of all, the vertical spring constants for both resonators are calculated; the equations are:

$$k_{v-LBAR} = \frac{Eh^3b}{4L^3} \tag{4.6}$$

$$k_{v-CC} = 16\frac{Eh^3b}{L^3} \tag{4.7}$$

where k_{v-LBAR} and k_{v-cc} are the vertical stiffness constants for a LBAR and a c-c beam. It shall be pointed that the vertical stiffness constant of the LBAR is the vertical stiffness constant of a c-f beam and does not corresponds to the equivalent spring constant of the bulk acoustic resonant mode.
The vertical stiction can also be expressed in terms of a vertical collapse voltage. Using a simplified model [89], the vertical stiction of a LBAR and c-c beam can be written as:

$$V_{si-LBAR} = \sqrt{0.29\frac{E \cdot s_v^3 h^3}{\epsilon L^4}} \tag{4.8}$$

$$V_{si-CC} = \sqrt{11.9\frac{E \cdot s_v^3 h^3}{\epsilon L^4}} \tag{4.9}$$

In order to define the limit between allowed and forbidden devices (due to their possible stiction to the substrate), a theoretical study that has been performed by Tas [89] and Mastragelo [90] is now recovered. When the resonator surface touches the substrate, the total surface energy is lowered. The structure will permanently stick to the substrate if during peel-off the total energy of the system reaches a minimum. The total energy of the system consists of the elastic deformation energy and the surface energy. The critical length at which a c-f will collapse down to the substrate is given by the equation:

$$l_{critic} = \sqrt[4]{\frac{3}{8}\frac{Eh^3 s_v^2}{\gamma^s}} \tag{4.10}$$

where γ_s, the adhesion energy, is given by $\gamma_s = 100mJm^{-2}$ [89]. It shall be pointed that this critical length depends on the vertical gap distance (s_v).

	MET4		**POLY1-POLY2**	
	LBAC	**c-c beam**	**LBAC**	**c-c beam**
l_{critic}, (μm)	40	113	5.7	16
k_{critic}, (N/m)	0.19	0.54	2.74	7.8

Table 4.8: *Calculated critical length and elastic constant for the LBAC and c-c beam devices in MET4 and POLY1-POLY2 approaches.*

A elastic critical constant for a c-f beam at which the total energy will be minimum can be derived, taking into account equation 4.6:

$$k_{critic} = \frac{1}{4}\frac{Ebh^3}{\sqrt[4]{\left(\frac{3}{8}\frac{Eh^3 s_v^2}{\gamma_s}\right)^3}} \tag{4.11}$$

A similar theoretical approach has been developed for a c-c beam. The critical length and the equivalent critical elastic constant have been derived and are written as follows:

$$l_{critic} = \sqrt[4]{96\frac{Eh^3 s_v^2}{\gamma^s}} \tag{4.12}$$

$$k_{critic} = 16\frac{Ebh^3}{\sqrt[4]{\left(96\frac{Eh^3 s_v^2}{\gamma_s}\right)^3}} \tag{4.13}$$

Considering the values for the vertical gap distances previously described in sections 4.3 and 4.5, it has been calculated the critical spring constant and the critical length for the LBAC and c-c beam devices, and for the two approaches under consideration, MET4 (top metal in-plane approach) and POLY1-POLY2 (for in-plane resonators). Table 4.8 shows the calculations.

Figure 4.11 shows the collapse voltage for a LBAC and c-c beam devices versus frequency, in a range from $10MHz$ up to $400MHz$, implemented by the MET4 (in-plane top metal resonators) approach. Right axis and top axis are drawn to see the length and spring constant scale for both devices. Due to the log axis, the limit of the spring constant for LBAC and c-c beam devices seems to be the same. The dash line separates the allowed and the forbidden devices. From the calculations it will be impossible to fabricate devices with less than $50MHz$ in frequency with an LBAR design.

The same calculations have been performed to the POLY1-POLY2 approach. Results are plotted in figure 4.12. There, the limits for the LBAR devices, that should be shorter than $5.7\mu m$, limits the fabrication of resonators with less than $100MHz$ on frequency by the LBAR design. Furthermore, it is not possible to fabricate c-c beam with less than $20MHz$. For that frequency range, another approach will have to be used.

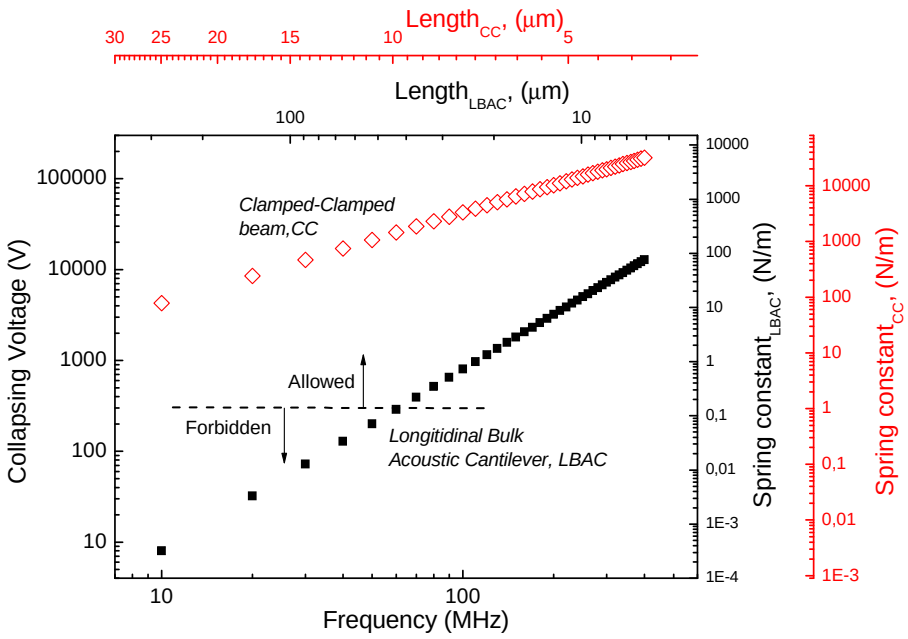


Figure 4.11: *Collapse voltage and spring constant versus frequency and device length for a LBAR and cc beams resonators implemented in the MET4 approach.*

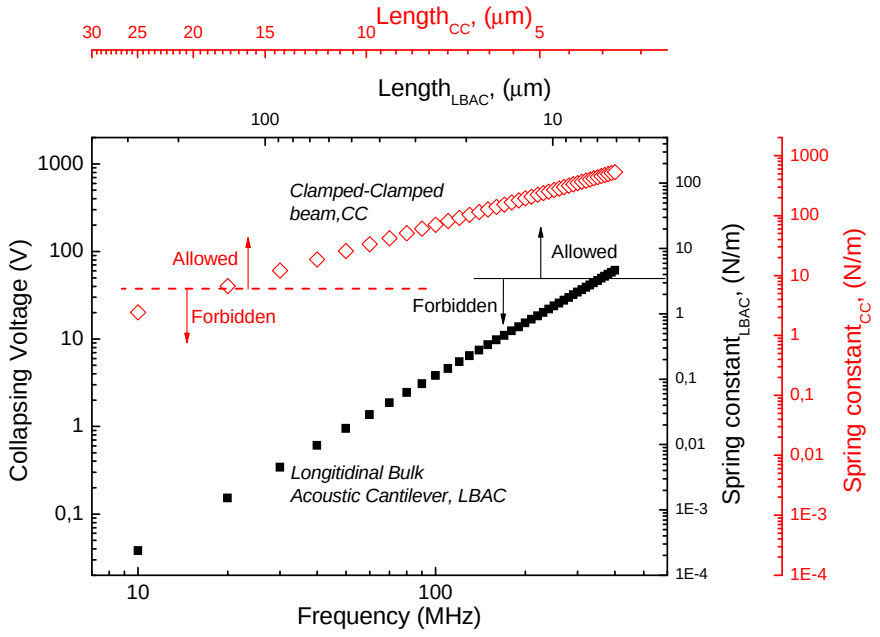


Figure 4.12: *Collapse voltage and spring constant versus frequency and device length for a LBAR and cc beams resonators implemented in the POLY1-POLY2 resonators approach.*

Up to now, it has been discussed which of the fabricated devices are forbidden by the possibility to collapse down to the substrate. However, and focusing in the POLY1-POLY2 approach, for an interval of frequency both kind of devices (above $100MHz$), LBAR and c-c beam are suitable from the design point of view. In order to predict which of them would provide better electrical properties, the motional resistance has to be calculated. In the chapter 2, it was introduced the normalized motional resistance, equation 2.25:

$$R = \frac{k}{2\pi f}\frac{s^4}{Q \cdot A^2 \epsilon_0^2} \tag{4.14}$$

The elastic constants (k) for the LBAR and c-c beam where deduced in previous chapter 2. Hereby are reproduced those equations 2.68 and 2.55:

$$k_{LBAR} = \frac{\pi^2}{8}\frac{Ehb}{L} \tag{4.15}$$

$$k_{cc} = 16\frac{E \cdot h \cdot b^3}{L^3} \tag{4.16}$$

The resonance frequencies for the LBAR and bridge in their fundamental modes are also reproduced:

$$f_{cc} = \frac{1}{2\pi}\frac{(2.365)^2}{\sqrt{192}}\sqrt{\frac{k_{cc}}{m_0}} \tag{4.17}$$

$$f_{LBAR} = \frac{1}{4L} \cdot \sqrt{\frac{E}{\rho\,(1-\sigma^2)}} \tag{4.18}$$

The variable s refers to the lateral gap distance in the POLY1-POLY2 approach, that is $40nm$. A is the coupling area between readout electrode and resonator. For the c-c beam, the coupling area is given by:

$$A_{c-c} = 0.8 \times L \times h \tag{4.19}$$

where 0.8 is a factor that corrects the real coupling between resonator and electrode. For the POLY1-POLY2 c-c beams resonators designed, this factor oscillates between 0.8 and 0.9.
For the LBAR cantilever, the lateral coupling is given by:

$$A_{LBAR} = 2 \times b \times h \tag{4.20}$$

where the factor 2 is due to the two arms coupling.

In order to predict the Q factor, it is supposed that the main loss mechanism is the anchor losses. From previous chapter 2, the anchor losses in a c-f and c-c beams are expressed as:

$$Q_{c-f}^{-1} = C_{c-f}\left(\frac{w}{L}\right)\left(\frac{h}{L}\right)^4 \tag{4.21}$$

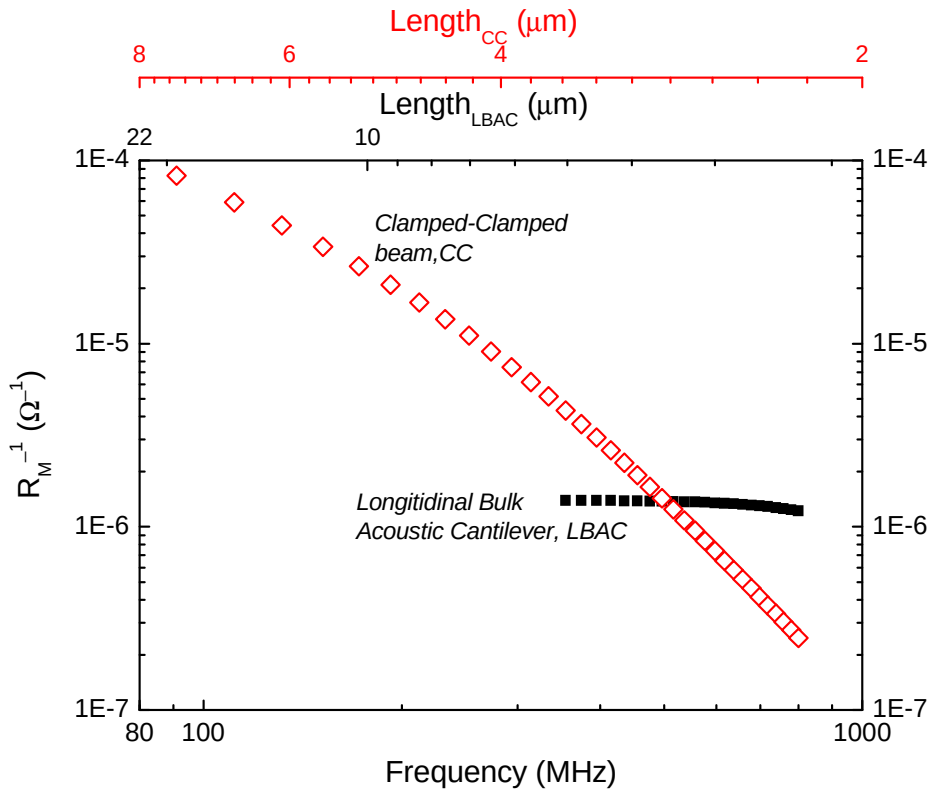


Figure 4.13: R_m^{-1} *as figure of merit, for POLY1-POLY2 resonators.*

where $C_{c-f} = 0.31$ is a numerical coefficient that depends weakly on the Poison's ratio σ and is 0.31 for $\sigma = 0.3 - 0.25$.

The losses fot he c-c beam are calculated by replacing C_{c-f} by C_{c-c}; in the fundamental mode, the relationship is:

$$C_{c-c} = 145.1 \cdot C_{c-f} \tag{4.22}$$

It shall be pointed that calculating the losses for the LBAR starting from the anchoring losses for a flexural c-f beam is just an approximation, and is justified in order to stablish a qualitative behavior in comparison to the c-c beam.

Anchoring losses are not the most important mechanism for lengths above $30\mu m$, hence for low frequencies, so more losses have to be considered in such cases. In order to evaluate the Q-factor of the resonators, it has been suposed that the main loss mechanism are due basically, to the resonator anchoring and to the surface losses. In order to modelize the

surface losses, it has been used an experimental result that will be given in the next chapter 5. It has been measured in vacuum, a quality factor of 3500 for a $4\mu m$-long c-c beam. From that experimental value, a dependence on the surface has been derived by the expression:

$$Q_{c-c}^{-1} = Q_{anchor_{c-c}}^{-1} + Q_{surface}^{-1} = Q_{anchor_{c-c}}^{-1} + \left(\gamma \frac{1}{d}\right) \tag{4.23}$$

where the surface losses are modelized by the factor $\left(\gamma \frac{1}{d}\right)$; γ is obtained by substituting the Q_{c-c} value for the measured value 3500 and the losses due to the anchor are calculated by the equations 4.22 and 4.21. It shall be pointed that all the resonator presents the same thickness, that is the POLY1 thickness, $282nm$. The value obtained for the γ parameter is $2.96 \cdot^{-11} m$. This value will be employed to calculate the quality factors for both the LBAR and c-c beams. Then, the quality factor is calculated by the equation:

$$Q_{\substack{c-c \\ c-f}}^{-1} = Q_{anchor_{\substack{c-c \\ c-f}}}^{-1} + Q_{surface}^{-1} \tag{4.24}$$

The DC voltages that can be applied to the resonator also conditionates the motional resistance. For that reason, and for each device, is calculated the vertical and lateral stiction voltages. For those values, the minimum voltage is the one that is used to compute the motional resistance. Based on the experience, another reestriction is imposed to the voltages that can be applied to the resonator; it has been observed that a voltage bigger than $30V$ breaks the inner oxide of the technology, yielding to the breakdown of the device. Then, the DC applied voltage to the resonator can not exceed the value of $30V$.

Taking into account those consideratons, the motional resistance for an LBAR and a c-c beam has been calculated by a frequency interval ranging from $10MHz$ up to $800MHz$ fabricated by the POLY1- POLY approach. The inverse of the motional resistance (R_m^{-1}), a parameter that wants to be as large as possible, is plotted versus the resonance frequency in figure 4.13. From previous calculations shown in figure 4.12, the devices that will collapse after releasing have been omitted; that is the reason why LBAR devices are not present in the $10MHz - 400MHz$ interval.

According to our calculations, in the VHF range the flexural c-c beam is the only possible choice, because of the reduced thickness of the field oxide layer, that will collapse the fabricated structures. But, in case that the releasing process would be possible, then the limitation will be related with the lower applied voltages that could be supported by those structures, hence limiting the minimum motional resistance. The R_m^{-1} for the c-c beams decreases continously versus frequency due to two main factors. The first one is the dependence on the quality factor versus the dimensions; when increasing the target resonance frequency, the resonator dimensions decreases, enhancing the mechanical losses due to the anchoring. The second factor is the coupling area, that is affected by the dimensions.

Around $500MHz$, and according to our calculations and hypothesis, is it observed that the

R_m^{-1} for the LBAR devices starts to be higher than for the c-c beams. So, there is a value for the frequency that from the design point of view, it is preferable to design LBAR than flexural c-c beams. For the LBAR, the quality factor in that frequency range is still limited by the surface effects, that is one of the reasons why the R_m^{-1} remains constant versus frequency in the interval, obtaining higher R_m^{-1} values than for c-c beam with the same resonance frequency.

Finally, it would be interesting to extend that analysis to another bulk acoustic resonators, for example the RBAR in order to compare and study the viability of fabricating those resonators, that present larger coupling areas, in the $100MHz - 1GHz$ range and discern if still the flexural c-c beams are the best option.

4.7 Summary

In this chapter, it has been studied and analyzed different fabrication approaches using the standard layers of the AMS-0.35μm commercial technology. The different alternatives have been discussed and the guidelines for the design have been stablished from previous characterization of the technology layers and processes. It has been demonstrated that the conformal deposition of the layers that conforms the CPOLY module favors the fabrication of in-plane resonators with a $40nm$ gap distances.

The limits for the integration of in-plane vibrating resonators (LBAR and c-c beam) have been analyzed based on two monolithic approaches, MET4 and POLY1-POLY2. For both cases, a limit of forbidden devices has been obtained, as well as a comparison between LBAR and c-c beam in terms of R_m^{-1} for the POLY1-POLY2 approach. According to our calculations, the starting frequency at which the LBAR devices begins to offer better performance than the flexural c-c beams is around $500MHz$.

CHAPTER 5

Results on RF-MEMS in the VHF band

In this chapter a detailed characterization for different microresonators fabricated by the hybrid and monolithic approach, and showing frequencies in the VHF range are presented. Results are divided into two categories, taking into account the nature of the fabrication process. Then, the first part of the chapter is dedicated to resonators obtained by hybrid fabrication processes, described in previous chapter 3, whereas the second part of the chapter is dedicated to resonators fabricated by the monolithic approach, presented in chapter 4. Resonators fabricated by the hybrid approach present air transducer gaps as well as solid dielectric gaps. Resonators integrated in AMS-0.35μm are divided according to the fabrication approach chosen. A section in this chapter is also dedicated to the CMOS integrated circuitry.

5.1 Hybrid resonators

Two different kind of resonators will be described in this section related with the fabrication processes presented in previous chapter 3. The purpose of both processes are different. Whereas in the first approach the main aim is to achieve a sub-100nm air gap resonators in single crystal silicon, the aim of the second one is to study the viability of incorporating solid dielectric gap materials on the fabrication process.

5.1.1 Air-gap resonators

Hereby are discussed the problems that raised while the technological process (see section 3.2) was being carried out, the proposed solutions to overcome such a limitations as well as a set of preliminary electrical characterizations performed on some devices.

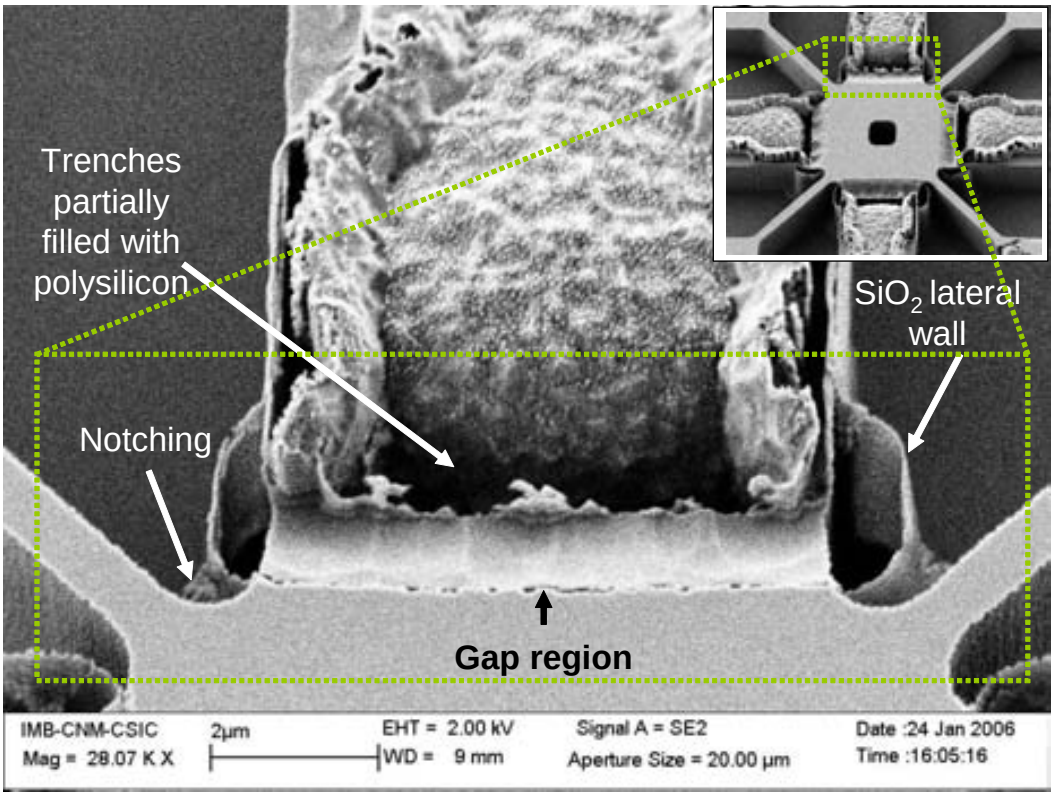


Figure 5.1: *Square shaped resonator fabricated by the process described in section 3.2. The image shows some problems encountered along the fabrication process.*

Characterization and optimization of the fabrication process

The technological process, that consisted in 3-mask, was described in previous chapter 3. The process starts with the definition of trenches openings by a DRIE process on a SOI wafer. On those trenches, a thin silicon dioxide is grown in order to define the gap lateral spacer that will be etched in the last step of the process sequence. Once the silicon oxide is etched, a polysilicon layer is deposited and patterned conforming the pads and the electrical electrodes. Finally, a DRIE process is necessary to pattern the resonator structure. The last step is the releasing of the resonators in a wet etching solution.

However, some problems appeared when carrying out the process. In figure 5.1 is shown a SEM image of a fabricated square shaped resonator. The complete square resonator can be seen in the inset of the figure. The figure shows in detail the gap region. From this figure some problems related with the fabrication problems have been deduced:

1. Trenches partially filled of polysilicon. In a first run it was observed that the deposited polysilicon of $1\mu m$ was not enough to completely fill the trenches area. The trivial solution to that problem was solved depositing a thicker layer of polysilicon.

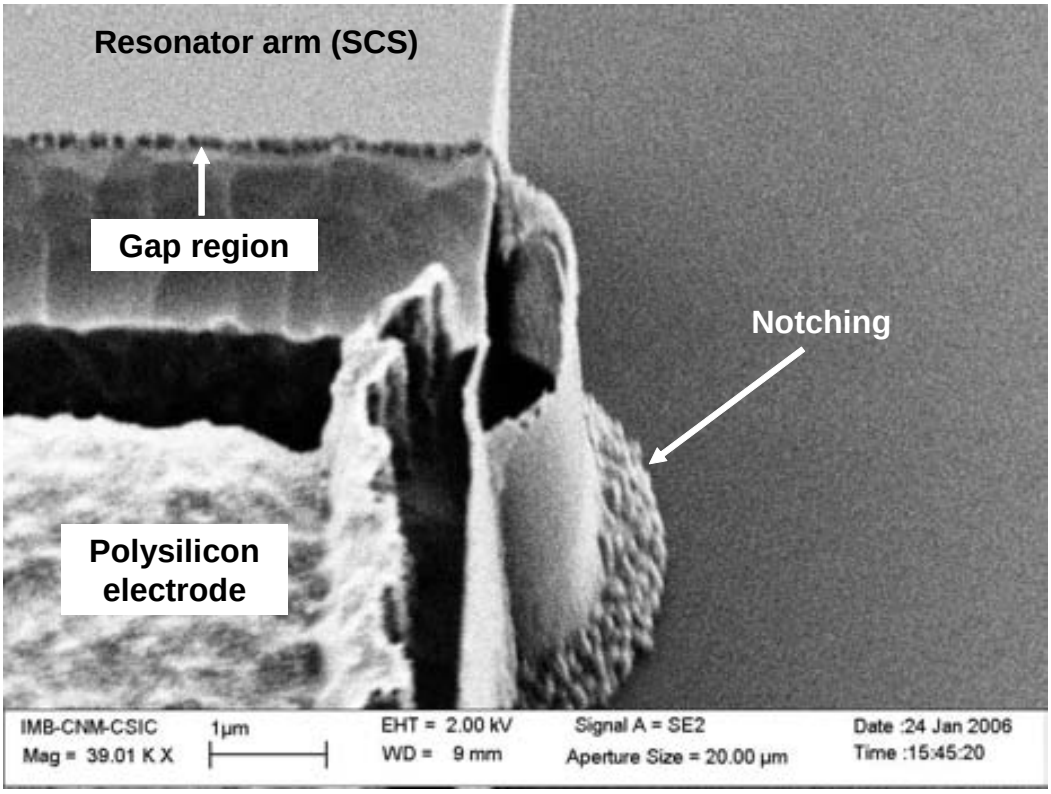


Figure 5.2: *The image shows the free end of a Longitudinal Bulk acoustic cantilever fabricated by the process sequence described in 3.2. The image shows the trench wider at the bottom, effect known as Notching.*

2. Figure 5.1 shows SiO_2 vertical walls surrounding resonator-to-electrode area. The presence of this walls have been associated to the growth with the gap spacer. After etching the trenches a thin layer of SiO_2 is grown in order to form the gap spacer. Instead of depositing it by LPCVD techniques, (like other works [75], [76]), the dry growth process in the silicon surface seemed the most suitable way to control the layer thickness of the gap spacer. Then, the oxidation process leaves a wall of silicon that is being oxidized and is not etched on the releasing process. The solution was to perform an isotropic wet etching of the SiO_2 following a short RIE isotropic etching of the SiO_2 following a short RIE isotropic attack.

3. In figures 5.1 and 5.2 it is shown how the trenches are wider at the bottom region, when the trench arrives to the buried oxide. This problem has been reported before and is known as *notching* [91]. The *notching* occurs when etching thicker and narrow trenches of silicon layers on top of buried oxides, and consists on the underetching of the silicon at the bottom regions. In narrow trenches, when all the silicon layer has been etched, the bottom oxide is exposed to the plasma and then charged; hence, the

ions are reflected to the bottom edge of the trench, destroying the protective polymer on the lowest part of the silicon sidewall, exposing the silicon to the plasma. Solutions to that problem imply the optimization of the DRIE process, adjusting the etching parameters.

4. Problems related with the resonator releasing have also appeared. Gap distances down to $60nm$ together with thicknesses of $5\mu m$, and planarless surface due to the DRIE process makes more difficult the releasing of such resonators, because derivate products of the wet reaction are not removed from the gap region. A solution that has been proposed is the use of additive TritonX (©) to the HF bath [92], [93] in order to reduce the surface tension of the liquid, facilitating the circulation of the etchant and avoiding the stiction of those particles in the gap region.

5. Figure 5.3 shows a profile of the gap region of a square resonator performed by FIB. When etching the trenches by the DRIE process, the cycles of passivation and etching makes the sidewalls of those trenches not vertical. This typical shape is observed in the profile of figure 5.3. A more planar and vertical sidewalls will facilitate the etching of the sacrificial gap spacer as well as the circulation of the subproducts derived from the chemical reaction.

Electrical characterization

After applying solutions to each of the problems above described, some devices could be electrically characterized. Electrical characterization based on one-port measurements (see appendix B) have been performed in such resonators.

Figure 5.4 shows a LBAR resonator and its electrical characterization. The side length of the resonator is $L = 36.2\mu m$. The resonator was designed to have a resonance frequency of $60MHz$, but the measured resonance frequency is around $35MHz$, below the expected value. It is suspected than the Young's modulus is smaller than predicted and the effect of the 'ears' could decrease even more the resonance frequency.

Figure 5.5 shows a square shaped resonator and its electrical characterization. The side length of the resonator is $L = 42.3\mu m$; the resonators are perforated in order to facilitate and reduce the etching time. The resonator was designed to have a resonance frequency of $100MHz$. Preliminary results shows a resonance frequency around $90.8MHz$, confirming that the expected Young's modulus was bigger than measured.

In a similar experiment, a circular shaped resonator with $R = 27.9\mu m$ has also been electrically measured. The expected resonance frequency for this disk in the *Wine Glass Mode*, is around $100MHz$. Figure 5.6 shows a SEM image of the device as well as the electrical characterization; the measured resonance frequency is around $78.5MHz$.

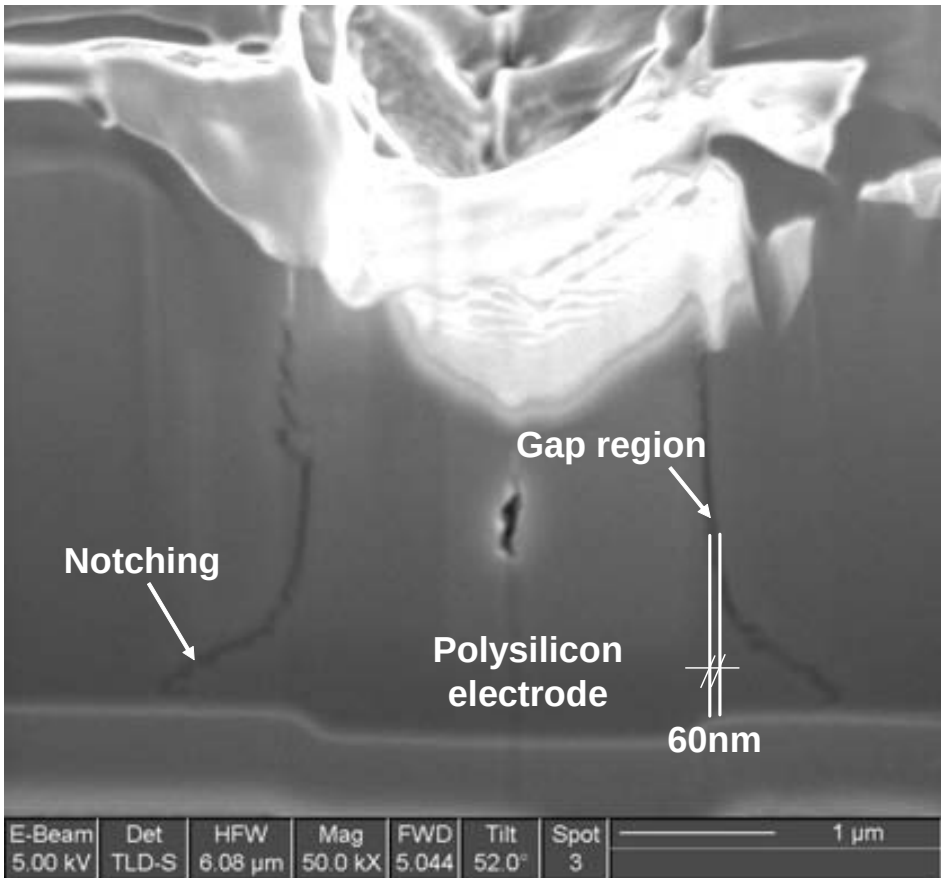
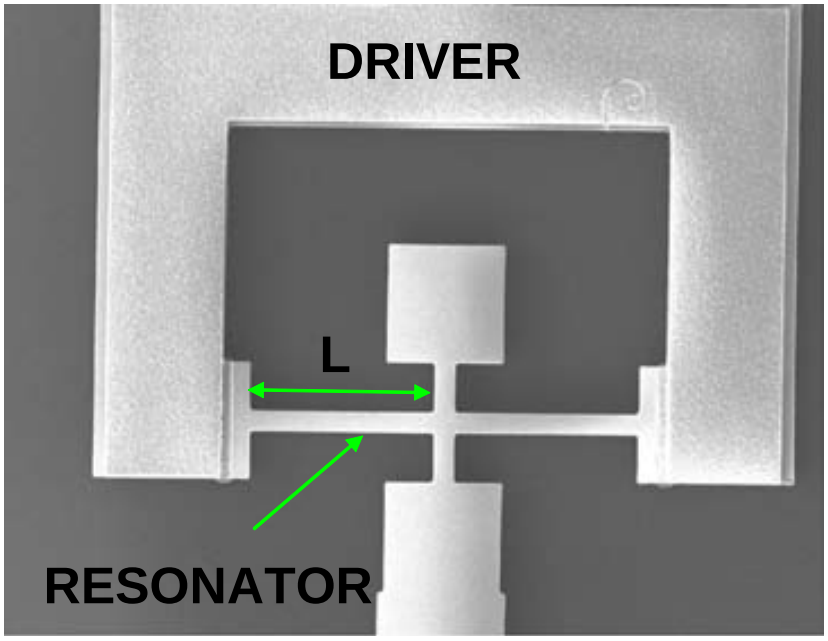
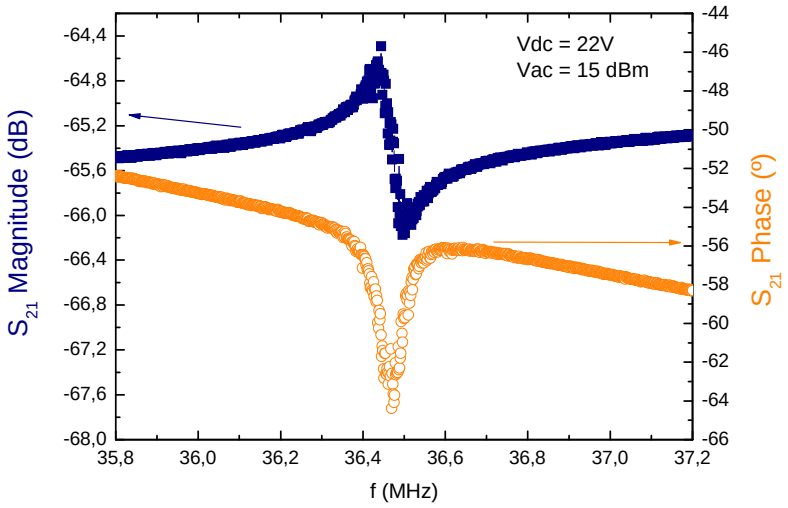


Figure 5.3: *SEM image showing a cross section performed by means of a FIB of a square shaped resonator in the gap region.*

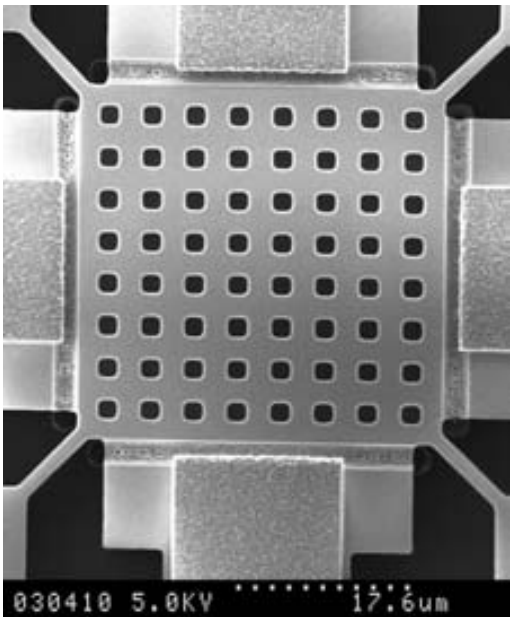


(a) SEM image of a LBAR resonator

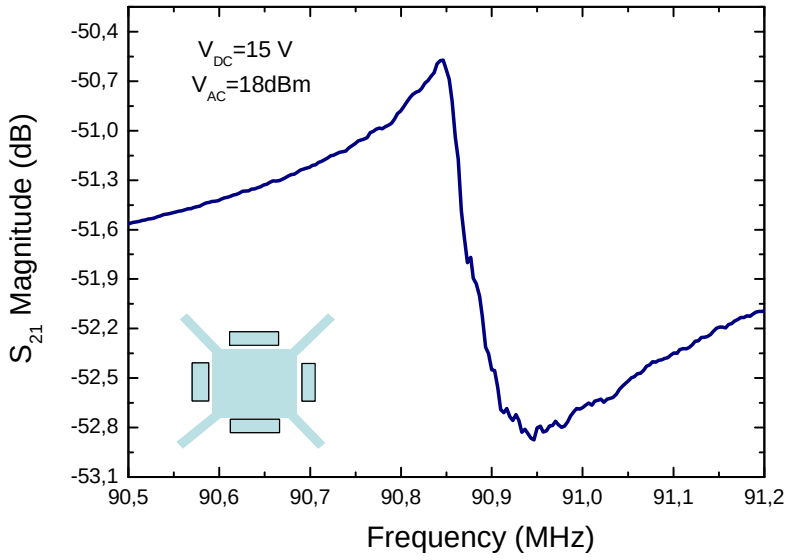


(b) Electrical characterization of the device

Figure 5.4: *SEM image of a LBAR resonator of* $L = 36.2\mu m$ *and its electrical characterization.*

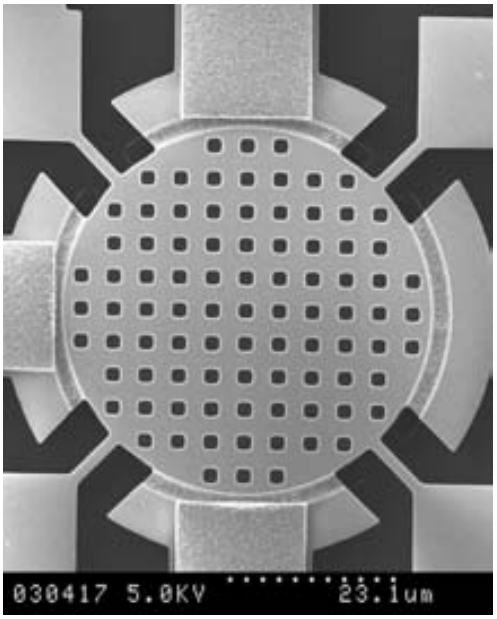


(a) SEM image of a square resonator

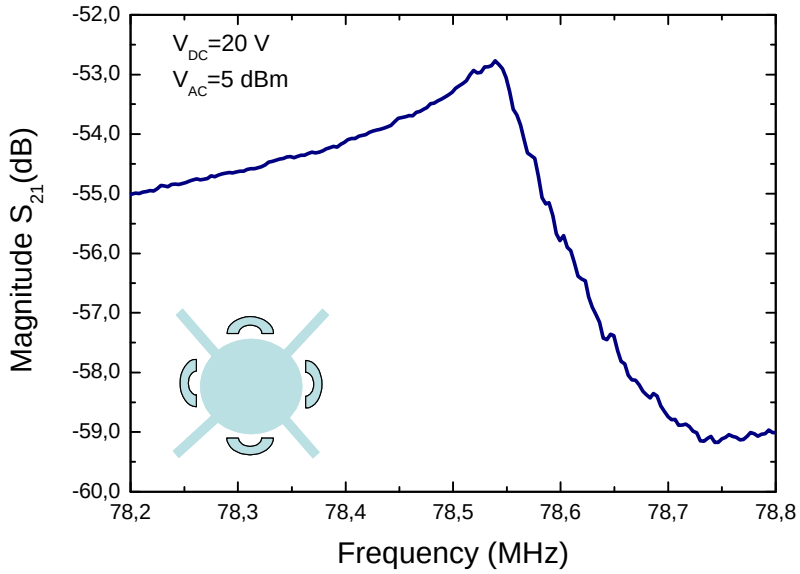


(b) Electrical characterization of the device

Figure 5.5: *SEM image of a square shaped resonator of* $L = 42.3\mu m$ *and its electrical characterization.*



(a) SEM image of a disk resonator



(b) Electrical characterization of the device

Figure 5.6: *SEM image of a disk shaped resonator of* $R = 27.9\mu m$ *5.6(a) and its electrical characterization 5.6(b).*

In both resonators, the magnitude of the peak not as large as expected, and is attributed to a reduced transduction in the gap regions. This limitation on the transduction is might be due to dirty gaps, where the etching of the gap spacer has been completed but subproducts of the chemical reaction are still trapped inside. More effort is needed in order to enhance the electrical response of such resonators. The addition of the component TritonX to the wet solution for releasing the resonators improved the electrical measurements, but still more research is needed in order to optimize the fabrication process.

5.1.2 Solid-gap resonators

The fabrication process, that was carried out at DANCHIP in collaboration with Dr. Z. Davis of the NSE-Nanoprobes group at MicroElectronic Centre (MIC), was depicted in previous chapter 3.3.

The fabrication process is partially determined by the gap material deposition. Furthermore, the process sequence is sensitive to the CMOS compatibility of the deposited gap material. Then, it makes sense to classify the solid gap materials in two different categories: CMOS-compatible and Non-CMOS-Compatible. CMOS- compatible solid gap materials that have been included in the process sequence are SiO_2 and Si_3N_4. Non-CMOS-Compatible material gaps are, aluminum nitride (AlN), boron nitride (BN) and carbonfluoroteflon, C_4F_8.

In next subsections, results on the fabrication of structures for the solid gap tests will be presented. Details of the dielectric material deposition conditions and the measured dielectric constant (ϵ_r) for all the proposed material will be reported. In order to test the dielectric properties of the gap material, specific and simplified runs that consisted on a fabrication on *test wafers* composed of two layers of aluminum and the solid gap in between, have been carried out. Polysilicon resonators are fabricated on *device wafers*.

Electrical measurements

An indirect method is used in order to measure the relative dielectric permitivity of the gap material deposited. The method consists on the measurement of a set of plane-parallel capacitances of known area. The capacitance is measured by means of a C-V meter. The value of the dielectric permitivity can be deduced if the thickness of the deposited material is also known:

$$C_{PP} = \epsilon_0 \epsilon_r \frac{A}{d} \tag{5.1}$$

where ϵ_0 and ϵ_r are the air and gap material permitivity, respectively. A is the coupling area between the two electrodes and d is the distance between them.

In order to measure the dielectric permitivity of the gap material, a set of test capacitances ($VCAP$ and $LCAP$) were included in the design (see section 3.3) and measured by means of

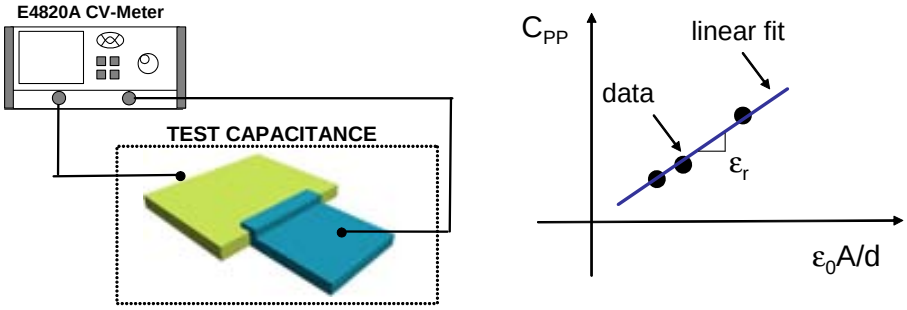


Figure 5.7: *Scheme of the experimental setup in order to measure the dielectric constant. Generic plot of the capacitance measurement that allows to extract the dielectric constant.*

a capacitance versus voltage meter [94]; figure 5.7 shows the experimental setup. The *VCAP* and *LCAP* capacitances consist on a set of vertical and lateral capacitances with different coupling length, and hence different area.

A graph, like the one shown in figure 5.7, allows to extract the dielectric permitivity for each material. The y axis will show the capacitance measured by the $C-Vmeter$ corresponding to the test capacitances.
The x axis will correspond to $\epsilon_0 \times A \times d^{-1}$. Then, the slope in graphs is adjusted to a linear fit, obtaining an experimental value of the ϵ_r.

CMOS-COMPATIBLE GAPS

In this section two different choices for solid gap materials will be described, SiO_2 growth by dry oxidation and Si_3N_4 deposited by LPCVD.
Furthermore, for device wafers, two approaches for fabricating device wafers have been designed. Tables A.2 and **??** (in the Appendix A) show those technological processes. The only difference between them is that in one approach a layer of SiO_2 is deposited on top of the structural material (polysilicon), adding a layer in order to protect the polysilicon in further steps of the process. Typically, the thickness layer of this oxide is $500nm$ and is deposited by a LPCVD furnace (LPCVD: TetraEthyl OrthoSilane (TEOS)). In the same step of photolithography (resist of $1.5\mu m$) the top SiO_2 and the structural polysilicon layers are etched. The SiO_2 layer is etched by means of the Advance Oxide Etcher (AOE) (is an equipment similar to the oxides and nitride as the DRIE is to silicon). With the recipe *base2a* only 2 min are needed for patterning the SiO_2 layer.
However, some runs have been performed without this SiO_2 on top of the polysilicon structural layer in order to measure the electrical properties by the vertical capacitances.
RUN06 wafers (named $r06\_9$, $r06\_8$ and $r06\_7$), do not have this SiO_2 layer on top of the polysilicon. Table 5.1 (in appendix A) shows the technological process sequence for these

Wafer Name	SiO_2 on top	Deposition time t, min	Deposited Thickness nm
$r03\_1$	$500nm$	4	10
$r06\_5$	NO	4	10
$r06\_3$	NO	8	20
$r03\_2$	$500nm$	8	20
$r03\_7$	$500nm$	8	20

Table 5.1: *Fabricated wafers with Si_3N_4 as gap material. Table shows thicknesses deposited in each wafer.*

three wafers.

Si_3N_4 as Solid Gap material

Table A.3 (in appendix A) shows the technological process for fabricating microresonators with Si_3N_4 as the dielectric solid material. In particular, the process depicted in table A.3 shows the sequence fabrication for a $50nm$-thick Si_3N_4 solid gap. The Si_3N_4 later is deposited on top of the first polysilicon. This has the advantage that vertical capacitances can be measured directly on the device wafer in order to extract the dielectric constant. However, the resonator polysilicon is only protected by a thin Si_3N_4 layer when patterning the polysilicon electrodes. So, the first polysilicon is etched while patterning the electrodes; two factors are responsible for that: the first factor is that only the thin Si_3N_4 layer was protecting the bottom polysilicon. The second factor is that an overetching is necessary in order to remove completely the second polysilicon. Then, this oxide layer prevents the first polysilicon to be etched while patterning and overetching the top (second) polysilicon.
Figure 5.8 shows a Si_3N_4 device on a wafer without SiO_2 layer on top. After the overetching of the second polysilicon, the gap material above the microresonator and the first polysilicon are removed. The Si_3N_4 on the walls is still there because the anisotropy of the etching process.
In a similar process, some wafers were fabricated by changing the deposition time of the Si_3N_4 layer. Then, different devices with different thicknesses of the solid gap were obtained. The relationship between deposition time and deposited thickness is shown in table 5.1. Si_3N_4 thicknesses have been measured by means of the *Filmtek* equipment.
For the silicon nitride different thicknesses were deposited in order to test resonators performance versus the solid gap distance. Figure 5.9 shows the extracted dielectric constant, obtaining typical values for this material, between 6.7 and 7. Frequency response have been measured on devices of these wafers, but no results have been obtained. The second polysilicon layer (that correspond to the electrodes) that surrounds the first polysilicon is thought to be the problem for not measuring the electrical response of any device.

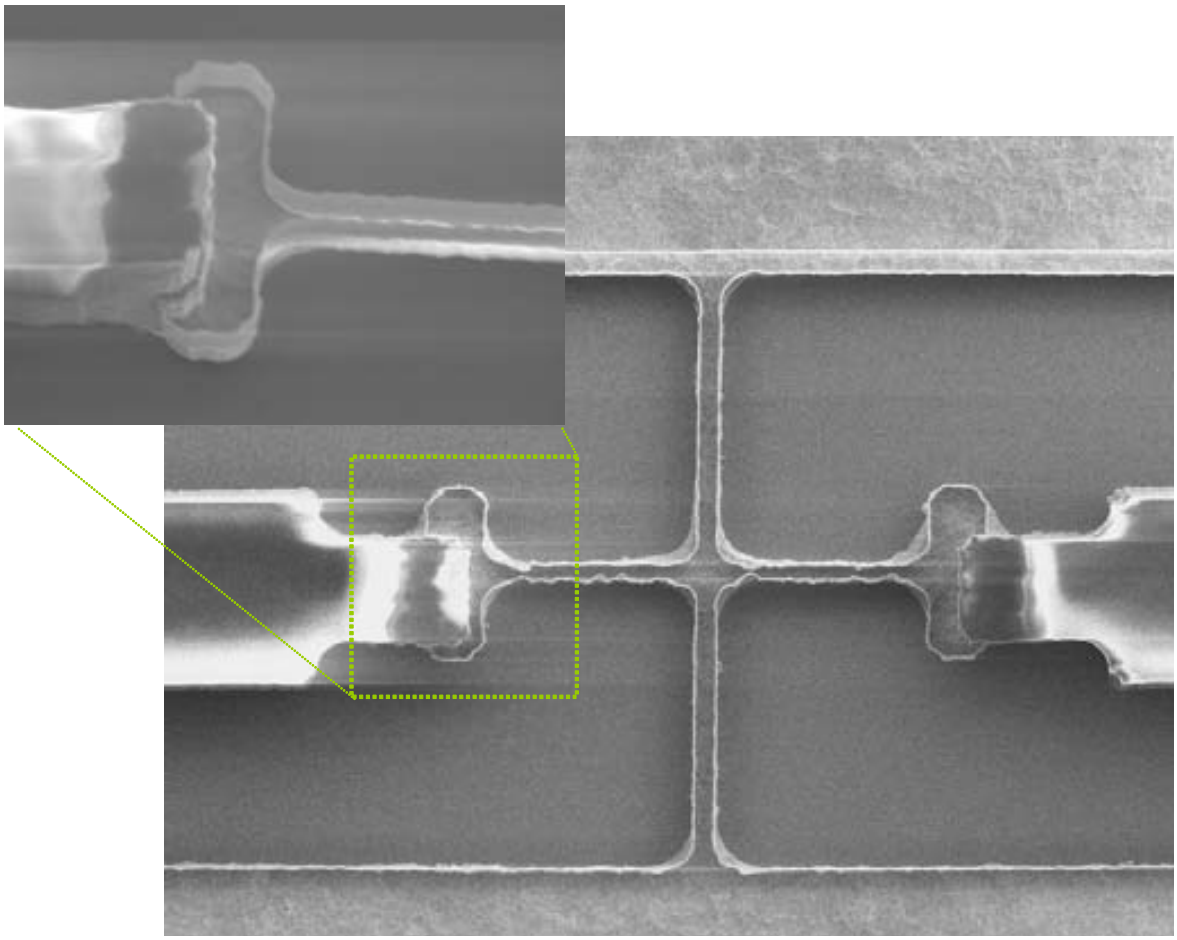


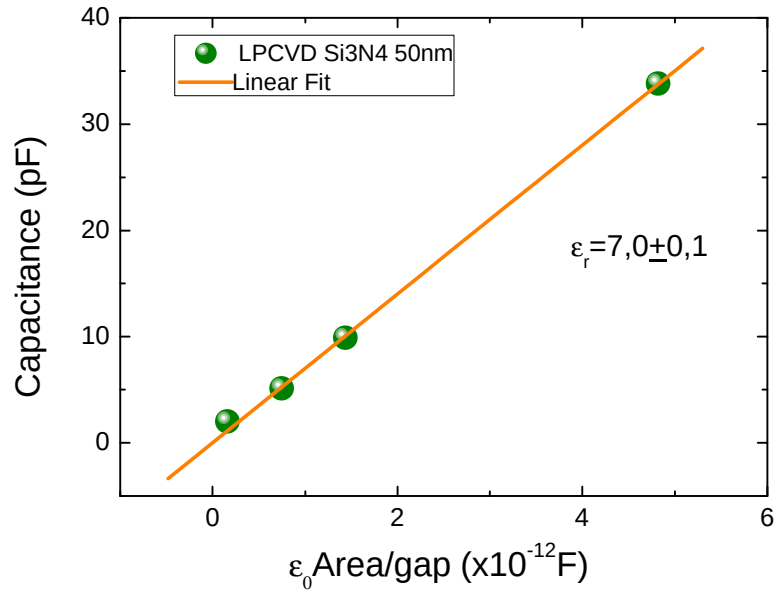
Figure 5.8: *SEM image showing a microresonator after patterning the top polysilicon. Above the first polysilicon is the Si_3N_4 thin layer, that is fast etched when overetching the second polysilicon.*

SiO_2 as Solid Gap material

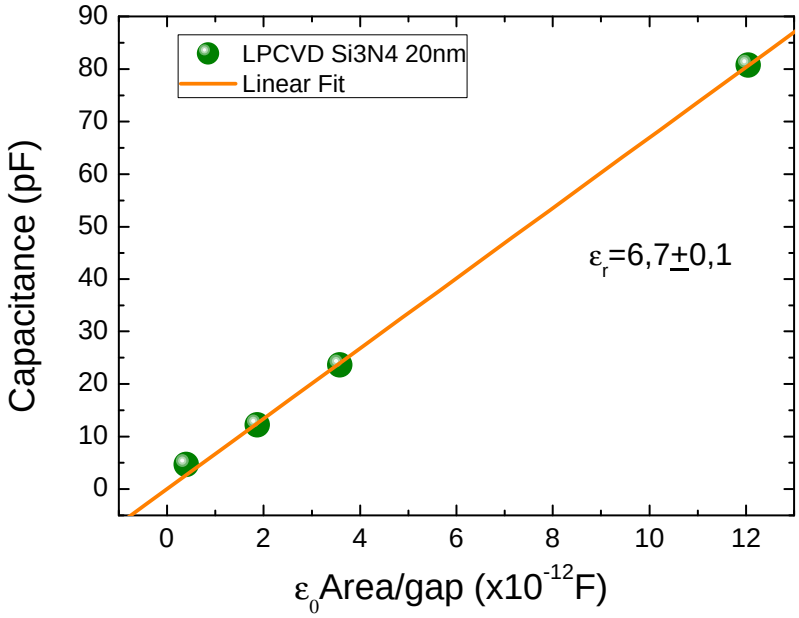
Table A.4 shows the technological process sequence in order to fabricate microresonators with dielectric solid gap based on SiO_2. For wafer $r03\_4$, the solid gap obtained is approximately $35nm$. It was necessary two dry oxidation processes (of $10min+$ $18min$) in order to achieve that value. The target gap distance was $40nm$. The polysilicon doping is not included in the process sequence but it was done a similar process as the one shown in table **??** or A.3.

After the RIE process to pattern the electrodes, a layer of resist of $9.5\mu m$ thick was spined in order to dice the wafer. 6 min in 40% HF solution are necessary in order to release the resonators.

Figure 5.10 shows the end arm of a LBAR fabricated device. The protecting SiO_2 layer on



(a) Si_3N_4 50nm-thick solid gap



(b) Si_3N_4 20nm-thick solid gap

Figure 5.9: *Extracted dielectric properties for two deposited* Si_3N_4 *layers,* 50nm *and* 20nm.

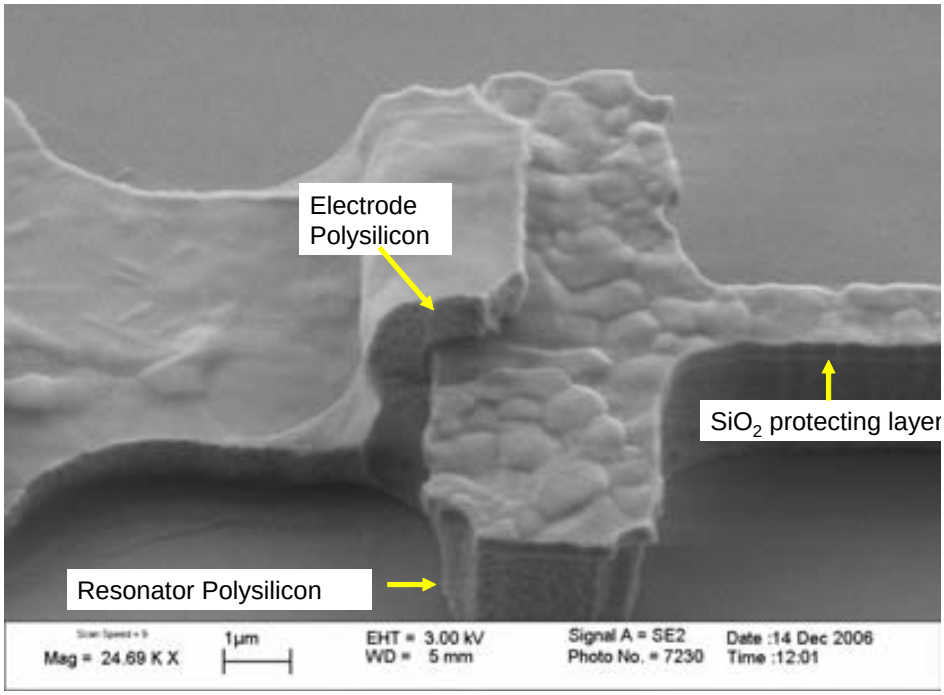
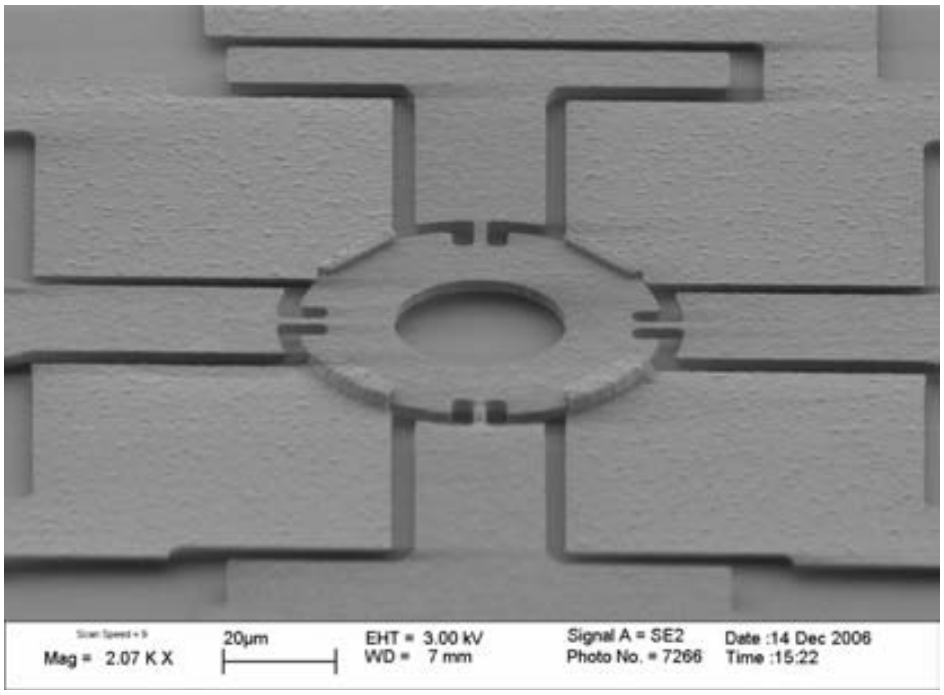
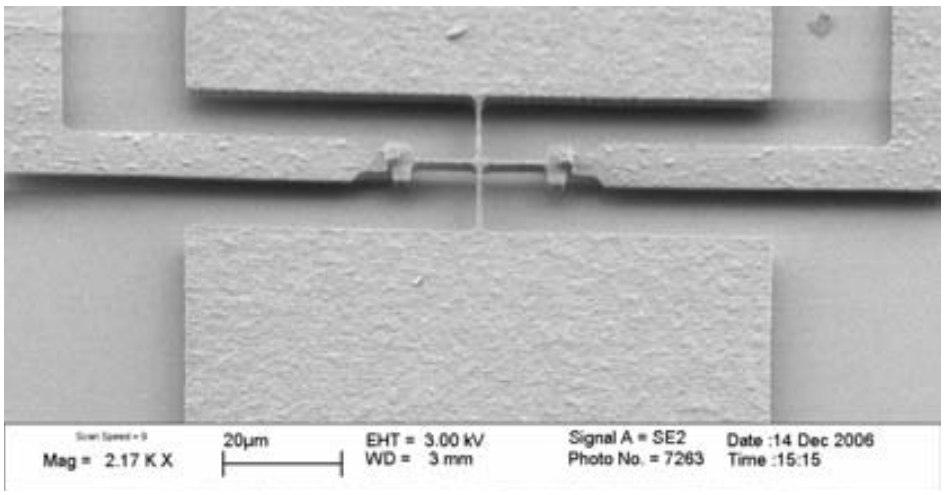


Figure 5.10: *SEM image showing the end of an LBAR. The top* SiO_2 500nm*-thick can be seen. The image was taken before releasing the resonators.*

top of the resonator arm can be observed. The thickness of this SiO_2 layer is 500nm, whereas the thickness of the structural polysilicon is 2.5μm and 1.5μm for the electrode polysilicon.
Figure 5.11 shows two different devices after the wet etch releasing process. For testing purposes, the longitudinal bulk acoustic cantilever is the most implemented resonator in the design. But, also some rings have been added in order to test the solid dielectric constants at higher frequencies. In order to release the resonators, the chip was submerged in a bath composed of HF at the 40%.
Figure 5.12 shows the corner of a RBAR device after the releasing process. Both sacrificial and protecting SiO_2 layers have been removed. It shall be pointed that the electrode polysilicon (second or top polysilicon) has not been completely removed. This is a problem that has to be solved in future designs, because it limits the operability of the device. This is the reason why sometimes no electrical signal is measured and when is measured, the signal is very low.
Figure 5.13 shows the dielectric properties for a SiO_2 layer, approximately 35nm thick,. Measurements correspond to wafer $r01\_9$, a similar wafer that run_03_4, but without SiO_2 layer on top. In fact, it is necessary not to have this SiO_2 on top in order to perform correctly this capacitance measurements. The technological process followed to fabricate this wafer is depicted in table A.4.
The dielectric permitivity extracted from the measurements was 3.6, a value close to the standard 3.9. In fact, the SiO_2 layer grown might be some nanometers thicker than measured,



(a) Ring bulk acoustic device, RBAR, with dimensions $r_i = 15\mu m$ and $r_o = 32.5\mu m$



(b) Longitudinal Bulk Acoustic resonator, LBAR, $L = 20\mu m$ long and $b = 2\mu m$ wide

Figure 5.11: *SEM images showing fabricated devices after* $6min$-40%-*HF solution wet etching.*

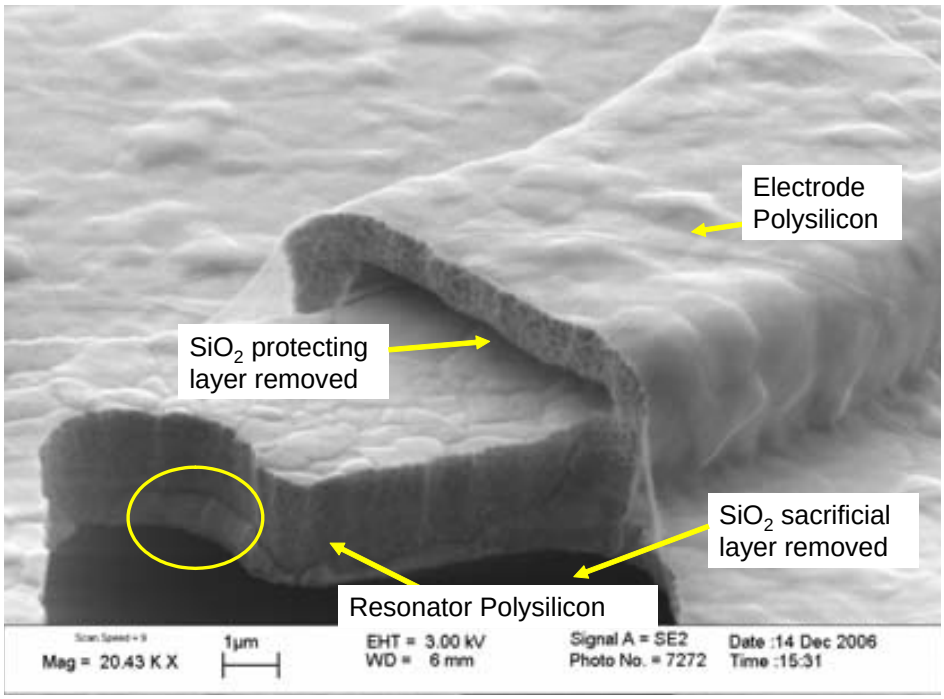


Figure 5.12: *SEM image showing corner of a RBAR fabricated and released device. The SiO_2-500nm thick protecting layer as well as the sacrificial oxide have been removed. A circle is showing electrode polysilicon that has not been completely removed.*

explaining this difference.
Figure 5.14 shows the frequency response near resonance for a LBAR device. In particular, the device is $30\mu m$ long and $4\mu m$ wide. In order to release the resonators, a wet etching based on HF at 40% has been performed during t=6min. For $V_{DC} = 3V$, a resonance peak is observed close to $31.5MHz$. In fact, the resonance frequency expected was $60MHz$. Some factors are reducing the resonance frequency. The polysilicon structural material is porous and hence, the Young modulus is lower than expected, yielding to a lower resonance frequency. In addition, the "ear" effect, consisting in widening the end of the resonators to increase the coupling area, decreases the resonance frequency.

NON-CMOS-COMPATIBLE GAPS

In this section, the fabrication process for three Non-Compatible CMOS materials will be described. The materials are: carbonfluoroteflon, C_4F_8, Aluminum Nitride AlN and Boron Nitride BN. The first problem to be faced was to establish the deposition conditions and the conformal behavior of the deposition process. Once that problem was solved, then the election of the electrode material became the second problem to face with.

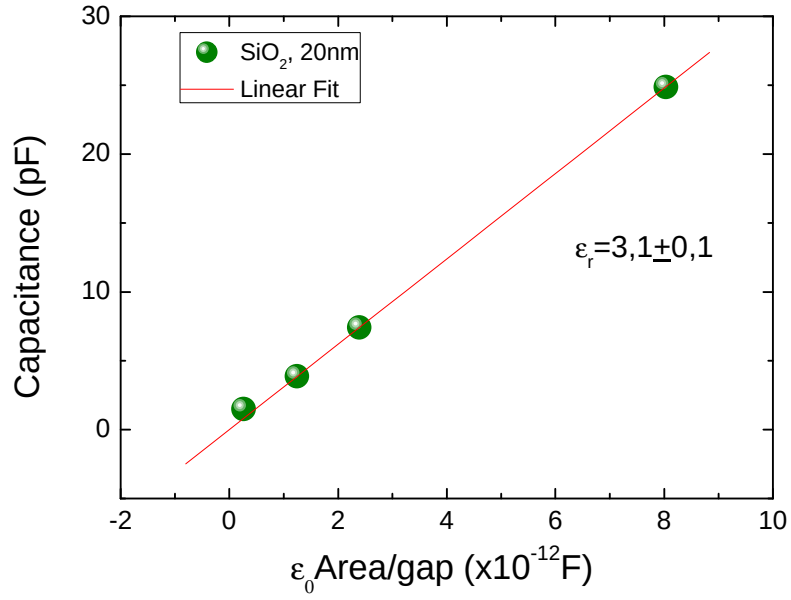


Figure 5.13: *Extracted dielectric properties for a* $35nm$*- *SiO_2* layer.*

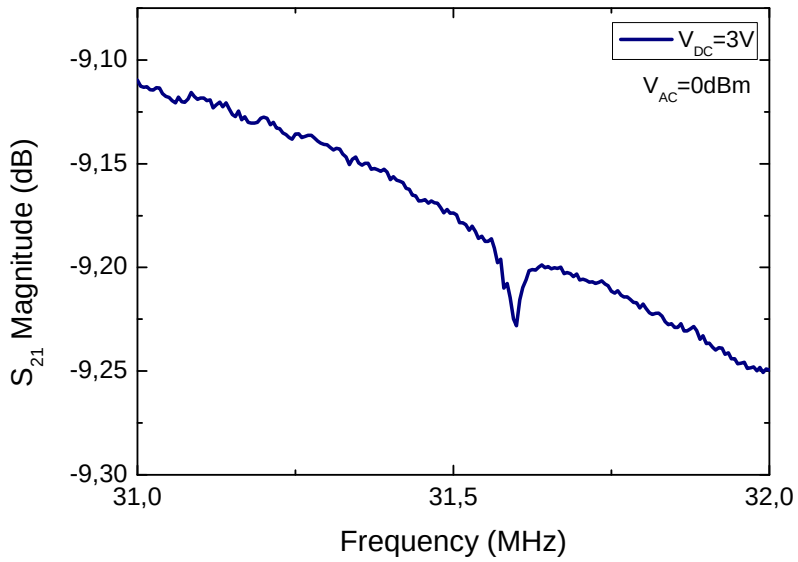


Figure 5.14: LBAR *frequency response near resonance. For* $V_{DC} = 3V$*, a (small) resonance peak is observed.*

Gap material	**Electrode Material**		
	Polysilicon	*Cr-Au Lift Off*	*Cr-Au and wet etching*
SiO_2	YES		
Si_3N_4	YES		
BN	NO, Dies in the RCA bath	YES, but stress problems appears	
AlN	NO, Dies in the RCA bath	AlN removed in the developer	YES
C_4F_8	NO, Dies in the RCA bath	YES	

Table 5.2: *Possibilities for the electrode material function of the solid gap material.*

Material Gap and Material Electrodes

Using materials as C_4F_8, AlN and BN arise new problems in terms of electrodes material selection. The non-CMOS compatibility of these materials implies the impossibility to use polysilicon as electrode material. The electrode material has to accomplish two different conditions: it has to be conductive and it has to be selective against the wet HF etch performed in order to release the resonator. In table 5.2 it is summarized the different possibilities offered at Danchip for depositing the electrodes material. For CMOS-compatible gaps, the best option is the deposition by LPCVD of polysilicon. However, for Non-CMOS-compatible gaps, the options are reduced to metal electrodes that are not etched in the releasing process. A stack of Cr-Au is thought to be the best option. A very thin Cr layer ($20nm$ or less) are previously deposited in order to reduce the surface stress of the gold layer. Two different ways have been tried in order to deposit the Cr-Au layers. The first one is to make a lift off process of the Cr-Au layers on top of the solid gap. The problem is that, when developing the resist, the AlN material is etched in the developer. The second option is to deposit the Cr-Au layers and then make photolithography and etch the Cr-Au layers for patterning electrodes and electrical pads.

Al Test wafers

Previously to the microresonators fabrication in $PolySi - SiO_2 - Si$ wafers, some test wafers were fabricated in order to test the dielectric properties of the gap material. These test wafers consist on a sandwich of Aluminum-Gap Material-Aluminum. The generic fabrication sequence of these wafers is depicted in table A.5 (see appendix A). The process consists on a lift-off in order to pattern the resonators and the bottom plate of the test capacitors. After the gap material is deposited, a layer on aluminum is deposited and patterned by chemical etching.

Carbonfluoroteflon, C_4F_8

The Carbonfluoroteflon, C_4F_8, is deposited by means of the Advance Silicon Etcher (ASE). The Teflon deposition recipe (named *jtedep*) is depicted in table 5.3.

The *jtetef* recipe is focused in order to achieve an isotropic deposition of the C_4F_8. Figure 5.16(a) shows the C_4F_8 deposited thickness versus the deposition time for short periods of time. The behavior of the deposition rate is non linear in the first seconds of the deposition cycle, but a deposition rate can be extracted in order to have a preliminary value for the deposition of the desired thickness. The extracted deposition rate value is $107nm/min$.

These measurements were performed in a dummy wafer. Each deposition cycle was preceded by an O_2 cleaning of $5min$.

However, due to the anti-adhesion behavior of the carbonfluoroteflon, a process sequence consisting on an isotropic deposition and followed by an anisotropic etching step was designed. Then, a C_4F_8 layer is expected to be only on the sidewalls, as shows figure 5.15.

The anisotropic C_4F_8 etching is based on the shallow process for the deep RIE etching of Silicon. The variables of the recipe *jteetch* are depicted in table 5.4.

Figure 5.16(b) shows the etching rate for the C_4F_8. The extracted etching rate is $286nm/min$.

In a similar way, the dielectric constant of a $50nm$-thick C_4F_8 layer was indirectly extracted from capacitance measurements. Figure 5.17 shows the results. The wafer used to extract the dielectric properties was an Al test wafer, composed of a $50nm$-thick C_4F_8 layer between two $300nm$-thick Al layers. The extracted dielectric constant is $\epsilon_r = 2.4$, which is among the values in literature. It shall be pointed that no capacitance was measured in the vertical

Teflon Deposition Recipe	
Pressure	APC Manual 15% Base Pressure $0.1mTorr$ Pressure Tip $94mTorr$
Gases	C_4F_8, $120sccm$, (Tolerance 5%)
RF	COIL
	$1000W$, (Tolerance 10%) Matching Auto: 30% LOAD, 60% TUNE
	PLATEN
	$0W$, (Tolerance 10%) Matching Auto: 45% LOAD, 60% TUNE
HBC Active	He Flow $9.8Torr$ 99% $40sccm$-$10sccm$

Table 5.3: *Teflon isotropic deposition recipe (*jtedep).

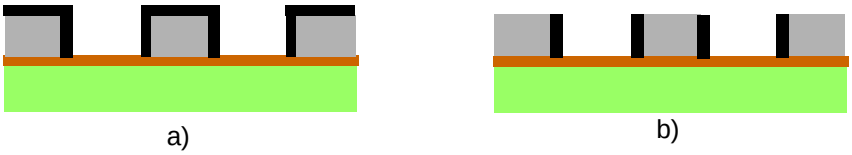


Figure 5.15: *Process sequence for removing the C_4F_8 on top of the layer; deposition cycle (a), followed by the anisotropic etching cycle (b), resulting in a thin C_4F_8 layer on the sidewalls.*

Teflon Etching Recipe	
Pressure	APC Manual 86.8% Base Pressure $0.1mTorr$ Pressure Tip $94mTorr$
Gases	SF_6, $260sccm$, (Tolerance 5%) O_6, $260sccm$, (Tolerance 5%)
RF	Coil
	$2800W$, (Tolerance 5%) Matching Auto: 45% LOAD, 60% TUNE
	Platen
	$20W$, (Tolerance 5%) Matching Auto: 40.5% LOAD, 61.6% TUNE
HBC Active	He Flow $9.8Torr$ 99% $40sccm$-$10sccm$

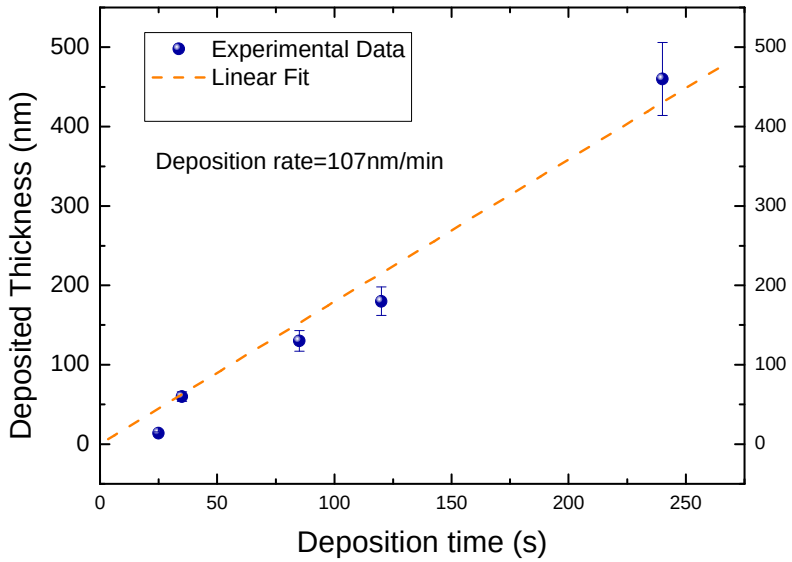
Table 5.4: *Teflon anisotropic etching recipe (*jteetch).

capacitances, i.e, the result obtained from those capacitances was the same as an open circuit. However, lateral capacitances exhibit a different behavior when measuring. Then, from the measurements, some stiction problems may be present on the vertical capacitances.

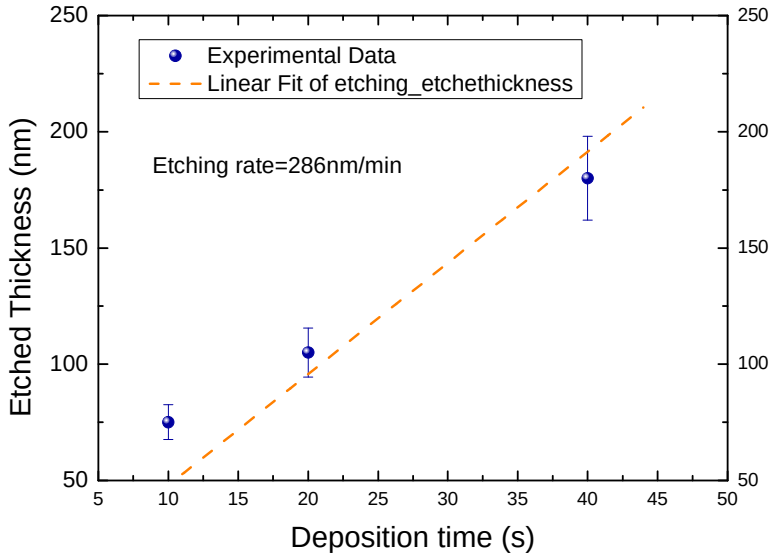
Aluminum Nitride, *AlN*

The *AlN* is deposited by means of a DC reactive sputtering technique, where *Al* is sputtered from the target and recombined in an atmosphere of nitrogen in order to form the *AlN* compound. The equipment used in order to deposit this *AlN* was the *Wondertec*. A new bottle of gas based on (Nitrogen-Argon), with a composition of (80%-20%, respectively) was acquired in order to perform this material deposition.

Because *AlN* is a non-conductive material, an *AlN* layer is also formed on the surface of the



(a) C_4F_8 deposited thickness versus deposition time for deposition conditions shown in table 5.3



(b) C_4F_8 etched thickness versus deposition time for deposition conditions shown in table 5.4

Figure 5.16: *Measurement of the deposition and etching rates of the* C_4F_8.

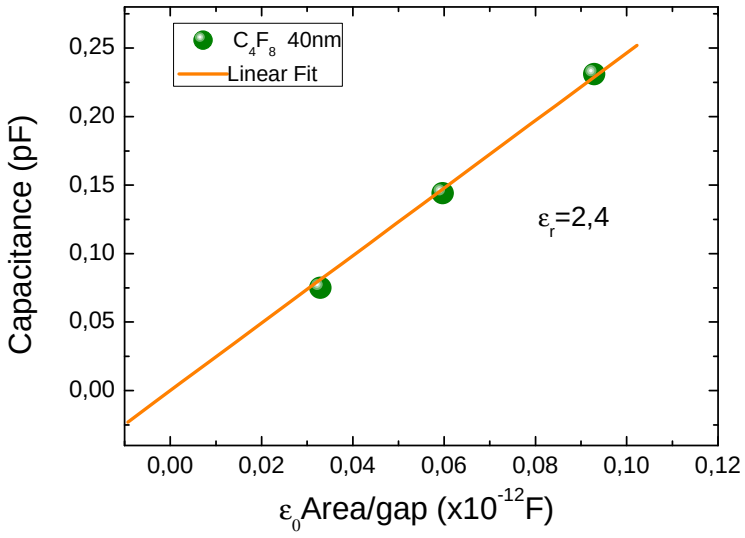


Figure 5.17: C_4F_8 *dielectric properties extracted from an* Al *wafer.*

target, needing a cleaning step of the surface in an Argon atmosphere. Table 5.5 shows this fact. After two deposition processes of 10min a cleaning on the target is needed in order to follow with the AlN deposition.

The deposition variables that control the deposition rate are: Deposition Time, Temperature, Power and Pressure [95]. The control of temperature in the *Wondertec* machine is not possible, so it is assumed that at the beginning of the deposition process the temperature is ambient; however, this temperature increases during the deposition process. During the cleaning process, the power is set to $300W$ in order to perform a good target cleaning. However, during the AlN deposition process, the maximum power oscillates between $220W$ and $255W$. The maximum current given by the power source is $1A$, and this criteria limits the maximum power that can be applied to the target. It has been observed that the deposition rate depends strongly on the maximum power. For power values $220W - 230W$ the deposition rate has been measured as $20nm/10min$, whereas if the power reaches values close or above $250W$, the deposition rate can be increased to $40nm/10min$.

The conditions for cleaning the target and depositing the AlN are:

1. **Cleaning**. In order to cleaning the target an Al deposition is performed on a dummy substrate for 10min and keeping constant the power source to $300W$ in an Ar atmosphere. A cleaning process is necessary before an AlN deposition and after two depositions of 10min.

2. AlN **deposition**. The AlN process deposition is performed in a $Ar - N_2$ atmosphere. For a $40nm$ layer thickness the estimated time is 10min. The power source is kept

Aluminun Nitride Deposition Recipe

Cycle	Process	Atmosphere	Deposition time t, min	Pressure μbar	Power W
1	Cleaning	$Argon$	10	8	300
2	AlN deposition	N_2/Ar	10	8	$247 - 257$
3	AlN deposition	N_2/Ar	10	8	$248 - 256$
4	Cleaning	$Argon$	10	8	300
5	AlN deposition	N_2/Ar	10	8	$241 - 254$
6	AlN deposition	N_2/Ar	10	8	$246 - 255$

Table 5.5: *Process sequence and deposition variables for depositing AlN.*

constant at the maximum value taking into account that the maximum current available from the source is $1A$.

After the AlN deposition, the electrode material is deposited. In table A.6 (appendix A) is shown the fabrication process for a wafer with AlN as a dielectric solid gap. The electrode material chosen is gold, due to its selectivity in the HF etching. In order to improve the adhesion with the AlN layer a thin layer of Cr is previously deposited. The Cr also shows selectivity in a HF bath. Au and Cr are deposited by *e-beam* in the *Wondertec* machine.

Figure 5.18 shows a Double Longitudinal Extensional Bulk Acoustic Resonator (DLBAR) after the electrode material deposition. A layer of Au $3.5\mu m$-thick has been deposited by *e-beam* deposition techniques. After that deposition, a shadow in the step region is observed. However electrical connectivity was measured between up and down. In the wet etching process of the Au and Cr, the electrode material is removed near those step regions. This fact can be seen in figure 5.19. For LBAR resonators the width of the electrodes was $10\mu m$ and are totally removed. For RBAR resonators, the electrodes are bigger, so they were not completely etched, see figure 5.20. But, looking in detail at the transducer gap, it seems that the gold has been removed yielding to an air gap.

A solution to overcome that problem could be the use of a dry etching of gold (performed in a Reactive Ion Beam Etch (RIBE)), but this equipment is not available at MIC. Another possible solution is using the electroplating technique in order to deposit the electrodes material. However, a seed layer for the electroplating with good step coverage is needed.

Wafers named $r06\_4$ and $r06\_2$ have been fabricated in a similar process like the one is detailed in table A.6. However, thickness of the electrode material are different. Table 5.6 shows the differences for these two wafers.

A set of capacitances were measured in order to extract the AlN dielectric constant. Results

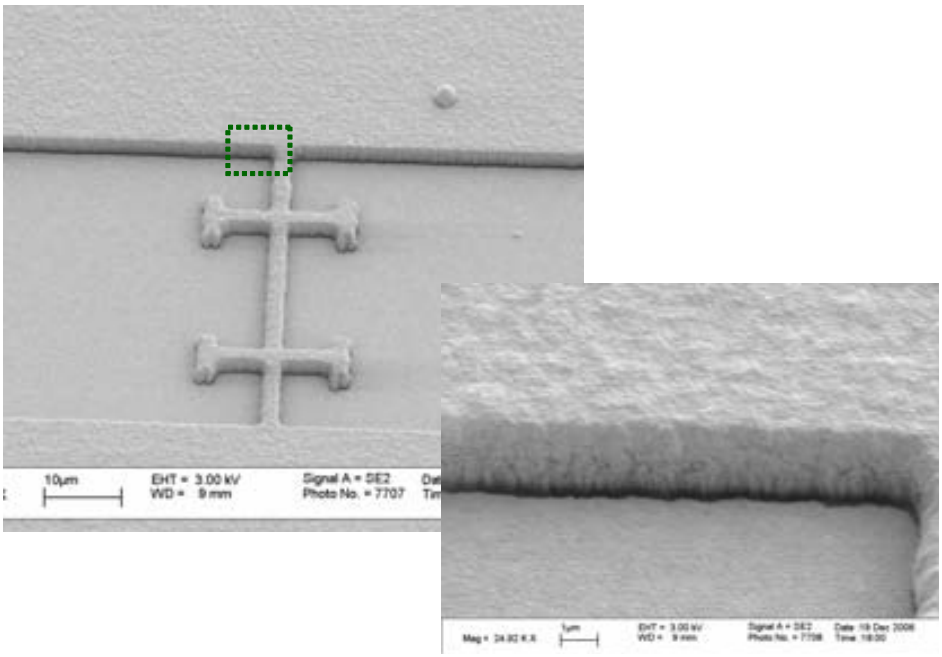


Figure 5.18: *SEM images showing a DLBAR resonator after the Au deposition, wafer r*06_6.

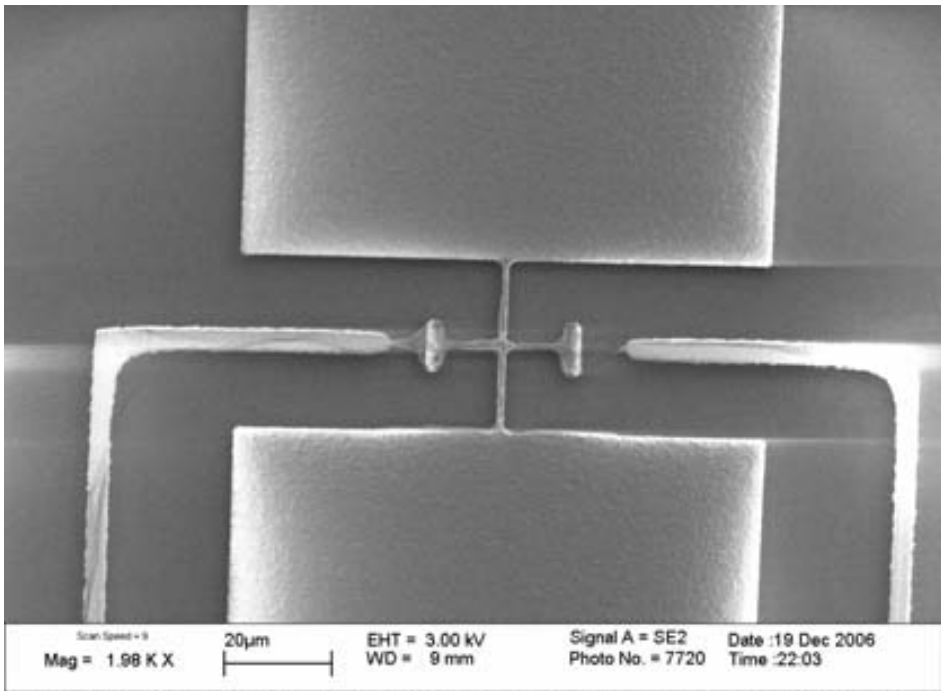


Figure 5.19: *SEM image of a LBAR device after performing the Au and Cr wet etching. Drivers have been partially removed.*

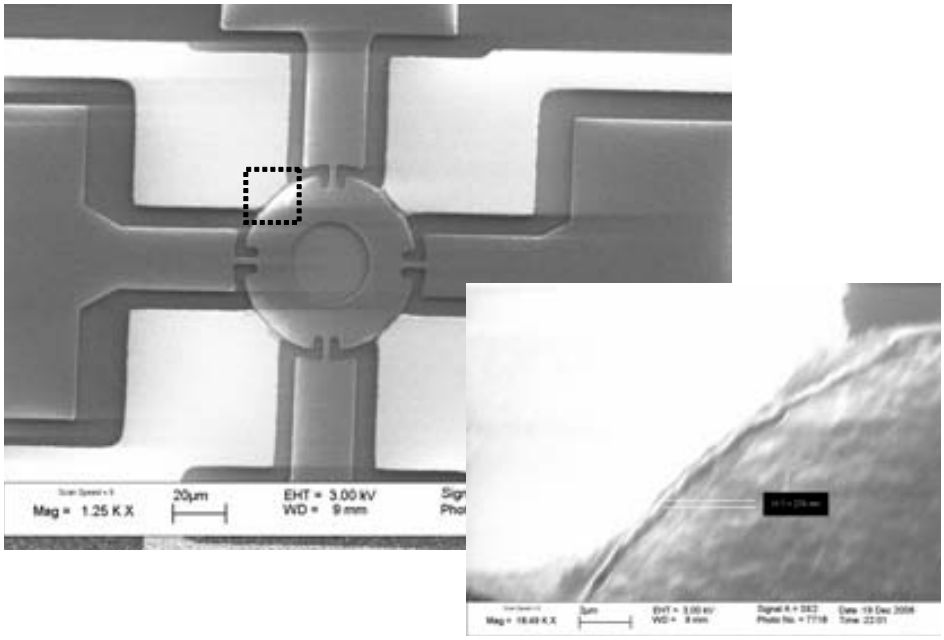


Figure 5.20: *SEM image of a RBAR device after performing the Au and Cr wet etching. Drivers have been partially removed. It seems that between driver and resonators an air gap of* $300nm$ *has been formed.*

Wafer name	AlN Deposition			
	Deposition time	Pressure	Power	Thickness
$r06\_4$	$10min$	$8\mu bar$	$241-254W$	$50nm$
$r06\_2$	$10min$	$8\mu bar$	$238-252W$	$40-50nm$
	Cr Deposition		Au Deposition	
	Thickness		Thickness	
$r06\_4$	$20nm$		$3.5\mu m$	
$r06\_2$	$200nm$		$500nm$	

Table 5.6: *Deposition variables for wafers* $r06\_4$ *and* $r06\_2$.

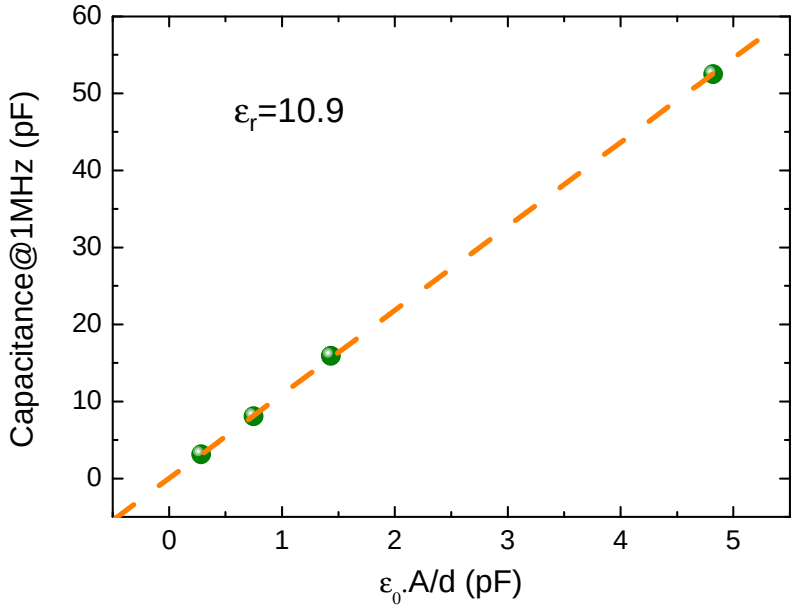


Figure 5.21: *AlN dielectric constant extracted from the capacitance measurements on Al (test) wafer.*

are shown in figure 5.21 and the extracted dielectric constant is 10.9.

5.2 Monolithic resonators

In this section, results showing the structural and electrical characterization for monolithically integrated resonators are presented. Devices are characterized by their technological approach, showing the structural layers for resonators and electrodes.

It shall be pointed that for each alternative, the structural material as well as the sacrificial layers corresponds only to the layers available in the technology. It shall be pointed that in some approaches the resonator and electrodes are designed and fabricated with different layers.

For each technological approach, a layout scheme of each structure is depicted, as well as the physical and electrical characterization. The chapter starts with the description of the readout circuitry fabricated monolithically with the resonator which function is to amplify and condition the signal coming out of the transducer.

5.2.1 CMOS readout circuitry

For MEMS devices, a read-out circuitry is necessary in order to enhance and improve the electrical signal generated by the resonator. In addition, the possibility to monolithically integrate a readout circuitry for on-chip resonators implies a drastic reduction of the parasitic capacitance between the readout electrode and the input of the circuit improving the readout signal.

The resonator is excited by means of an alternate voltage and supplied by a DC voltage and the output signal obtained from the read-out electrode is an alternate current, characterized to have tenths of microamperes of amplitude. This current is amplified to match further electronic blocks of 50Ω, which is very important, at least on the characterization stage.

From the circuitry design point of view, two different alternatives have been designed and implemented for testing the resonators performance. The first approach consists on the integration of the capacitive current generated by the vibrational movement of the resonator by using the intrinsic capacitance of a *CMOS* amplifier. The second approach is based on a TransImpedance Amplifier (TIA).
The total current generated at the driver-resonator system can be calculated as:

$$I_C(t) = \frac{d\,(C \times V)}{dt} = C\frac{dV}{dt} + V\frac{dC}{dt} \tag{5.2}$$

The first term is the parasitic current generated as a consequence of the alternate voltage applied to drive to resonance the resonator whereas the second term is the resonance current produced by the mechanical movement of the resonator. The first term masks the resonance current, affecting negatively to the resonance signal.

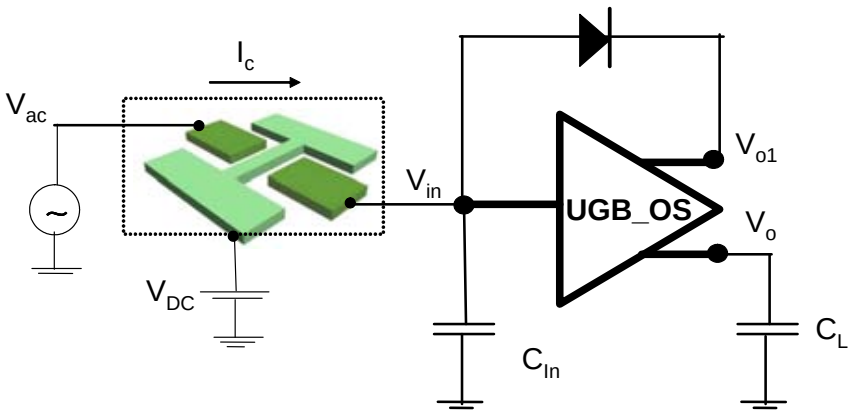


Figure 5.22: *Capacitive sensing scheme for a resonator electrostatically driven.*

Capacitive Detection

The purpose of the readout circuitry is to detect and amplify the capacitive current generated in the driver-resonator interface. The design of this circuitry has been carried out by J.Verd, and more detailed information about the circuitry design and performance can be found at [96]. In this approach, a capacitive detection method has been chosen in order to detect the displacement (or resonance) current. The principle of operation is based on the integration of the capacitive current I_C by using a capacitor (C_{IN}), and measuring the resulting voltage (V_o), as depicted in 5.22. Considering C_p the parasitic capacitance between excitation and read-out electrodes, and C_{In}, the input capacitance of the circuit, it can be demonstrated that the output voltage is proportional to [97]:

$$\frac{C_p}{C_p + C_{in}} G_{buffer} \tag{5.3}$$

From last equation, a low value of the total capacitance at the input node (C_{In}) is compulsory in order to maximize the sensitivity of the readout system. A value of C_{In} is achieved by designing monolithically the circuit following some rules:

- The intrinsic capacitance at node V_{In}, which represents the input capacitance of the circuit, cantilever-substrate capacitance and the contribution of the electrical connection from the readout driver to the circuit, is designed as an integrated capacitance.

- The buffer circuit is polarized by means of a DC bias diode (D_{bias}), connected between the sense node V_{In} and the node V_{o1} (see Figure 5.22). Since there is no DC current through the diode, it acts like an extremely high value impedance ($10^{15}\Omega$). This diode is laid out so that the parasitic well-substrate diode does not shunt C_{In}.

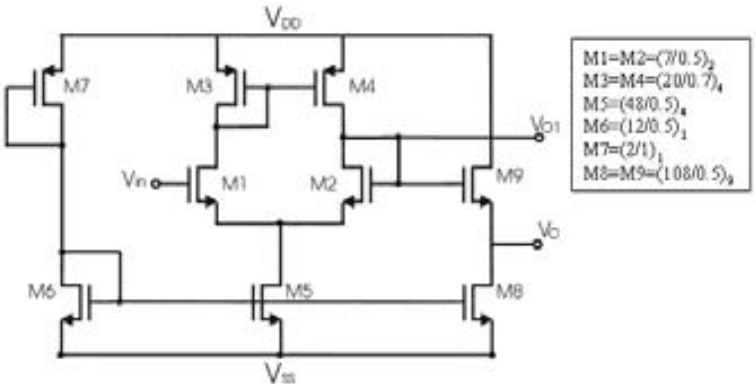


Figure 5.23: *Unity gain buffer with output stage (*UGB_OS*) circuit schematic. The dimensions of the transistors are in microns.*

- The bias diode, or other bias element, may limit the sensitivity of the readout system since its parasitic capacitance, on the same order of magnitude than C_{In} may increase C_{In} directly. In this design, this parasitic capacitance is strongly minimized by using a feedback configuration connecting the diode between V_{o1} and V_{In} nodes. Since the readout circuit is a unity gain buffer ($V_{o1}/V_{In} \approx 1$), the increment of C_{In} by Miller effect is very small.

The unity gain buffer scheme is depicted in figure 5.23. The electrical scheme is based on a threshold independent level-shifter topology (M1..M5) with a source follower output stage (M8 and M9). This circuit has low input capacitance ($7.37pF$) achieved by using the source-follower input stage. The circuit has two outputs: V_{o1} which has a gain of 0.974 with respect V_{In} and it is used for biasing V_{In} through a diode and V_o which has the capability of loading high capacitances ($30pF$) with a relative high bandwidth, ($47MHz$) that allows the circuit test measurements but with a gain of 0.782 with respect V_{In}.
The simulated frequency response of the circuit is represented in figure 5.24. The amplifier shows a gain of more than $90dB$ at $100MHz$. Althoug the gain decreases continuously with the frequency, a gain of $60dB$ is expected at $1GHz$.

TransImpedance Amplifier

This approach has been developed by A.Uranga. Further details of the circuitry design and performance are described in [98].
In this approach the readout circuitry is based on a transimpedance amplifier structure, (TIA). The circuit exhibits a bandwidth of $400MHz$, as shows figure 5.26, suitable for a lot of fabricated devices [98]. The structure of the transimpedance amplifier consists on an inverting transimpedance amplifier connected to a source-follower stage, in order to enhance the bandwidth of the full amplifier. An output matching buffer stage has been designed to drive the 50Ω input impedance of the network analyzer. In order to reduce power consumption

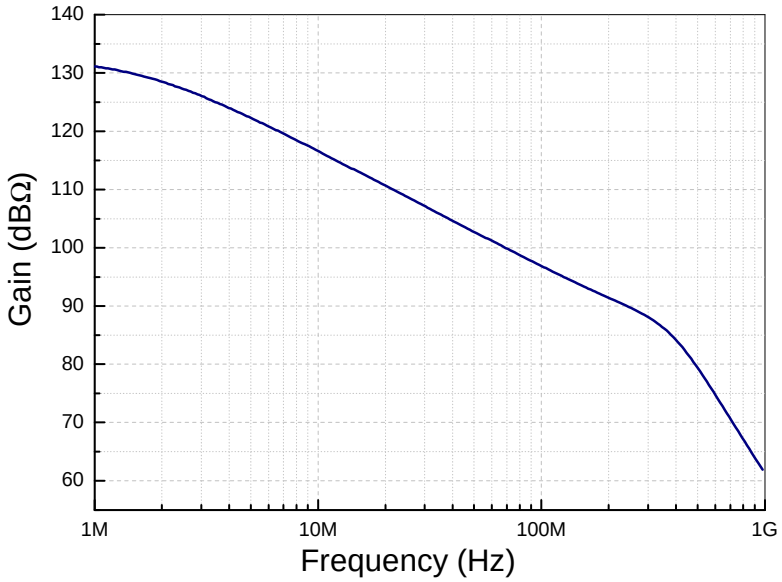


Figure 5.24: *Simulated frequency response of the amplifier depicted in figure 5.23.*

at the output stage, the full amplifier is AC coupled to the network analyzer by means of an external bias-T structure. This element provides an AC coupling (because of the capacitor) to the input impedance of the network analyzer. Connections between the *MEMS* structure and the circuit are performed by a short metal line in order to minimize the parasitic capacitance. Figure 5.25 shows the scheme and transistor dimensions that conforms the *TIA* amplifier. The current that comes from the resonator is labeled I_{In}. To polarize the circuit, a current

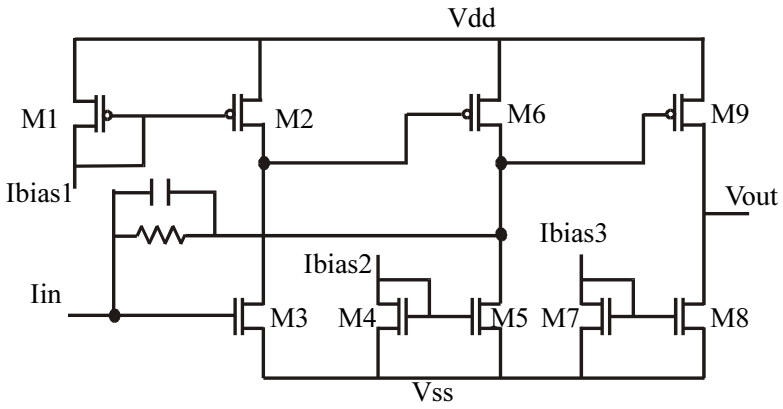


Figure 5.25: *Scheme of the implemented transimpedance amplifier in charge of amplifying the capacitive current generated by the resonator.*

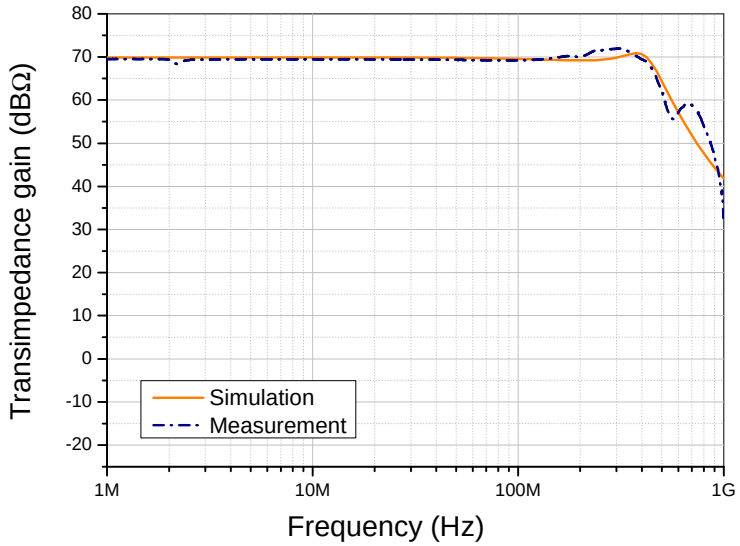


Figure 5.26: *Frequency response of the TIA amplifier depicted in figure 5.25.*

reference has been implemented. It consist on a bootstrap current reference that generates a fixed current, independent of the power supply. By mirroring this reference current, the different I_{bias} currents have been generated.

5.2.2 MET4 in-plane resonators

In this section, the design as well as the electrical characterization of a monolithically integrated metal clamped-clamped beam will be presented [99]. The selected approach will be based on choosing the top metal (MET4) as structural layer for in-plane resonator design, The section is divided into three parts, design, physical characterization and electrical characterization.

Design

The structure chosen to test the capabilities using this approach, explained in section 4.3, consisted on a clamped-clamped beam. Resonators and electrodes are fabricated choosing MET4 as structural material. The dimensions of the c-c beam are: $10\mu m$ long, $1.2\mu m$ wide and a lateral gap distance determined by the minimum distance between two MET4 adjacent lines of $s = 600nm$. The layout of the designed structure is depicted in figure 5.27(a). A pad window is drawn in order to define the resonator area. The resonator is surrounded by a n-well in order to reduce the parasitic signal produced by the circuitry.

The resonance frequency for the in-plane fundamental mode of a clamped-clamped beam was derived in previous chapter 2 and hereby is reproduced:

$$f_{c-c} = \frac{(2.365)^2}{\sqrt{3}\pi} \frac{b}{L^2} \sqrt{\frac{E}{\rho}} \tag{5.4}$$

The expected resonance frequency of the device is calculated using equation 5.4 and the Al mechanical properties depicted in table 5.7; the theoretical resonance frequency is $65.9MHz$.

The measured electrical performance of the resonator has been fit to the simulation curves (obtained by the electromechanical model developed in previous chapter 2), showing the final values for the mechanical and physical parameters.

Structural characterization

A SEM picture of the fabricated device is shown in figure 5.27(b). The resonator is surrounded by a window pad of $(15 \times 15)\mu m^2$, the minimum allowed by the technology, that removes the passivation layer from the resonator area.

The measured dimensions differs a little bit from the ones drawn at the layout. The measured length of the resonator is $10\mu m$, the width is $1.1\mu m$ and the gap distances are around $650nm$. Table 5.8 summarizes those values.

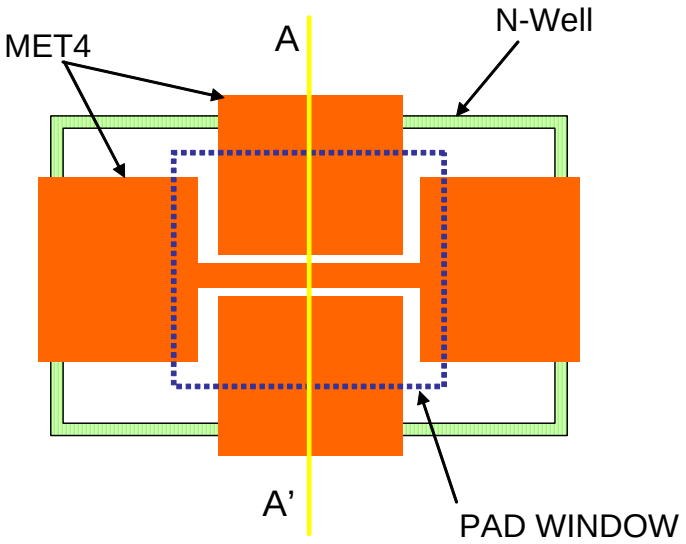
In order to release the mechanical structure, a maskless wet etching is performed. The area under the defined window is exposed during a short period of time to a solution based on *HF*, with an etching rate of approximately $200nm/min$. A postprocess of $4min$ is enough to release the MEMS, removing part of the sacrificial layer. The sacrificial layer on this approach is conformed by the inter-metal oxides IMD3, IMD2, IMD1 and by the oxides layers ILDFOX and FOX. The passivation layer protects the circuitry from the wet etching.

Material	E**,** GPa	ρ**,** kg/m^3
Aluminum	77	$2.70 \cdot 10^3$

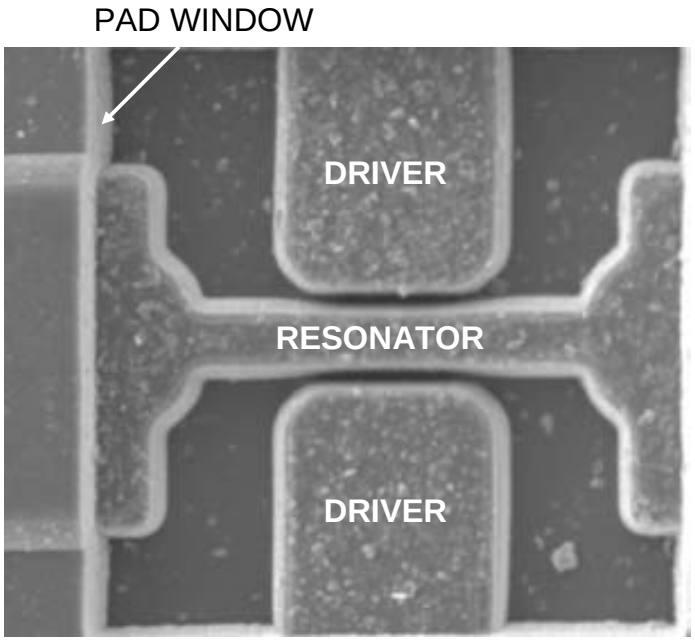
Table 5.7: *Material properties for MET4 layer.*

	Layout	**Simulated**	**Measured**
Width, b	$1.2\mu m$		$1.1\mu m$
Length, L	$10\mu m$		$10\mu m$
Gap distance, s	$600nm$		$650nm$
Resonance frequency ($V_{DC} = 0$)		$65.9MHz$	$60MHz$
Motional resistance			$3.5 \cdot 10^{12}\Omega$

Table 5.8: *Thickness for all the layers of the standard AMS* $0.35\mu m$ *technology [85].*



(a) Layout of the clamped-clamped beam designed using the top-metal of the technology



(b) SEM image of the fabricated device

Figure 5.27: *Layout and fabricated c-c beam by the top metal in-plane resonators approach.*

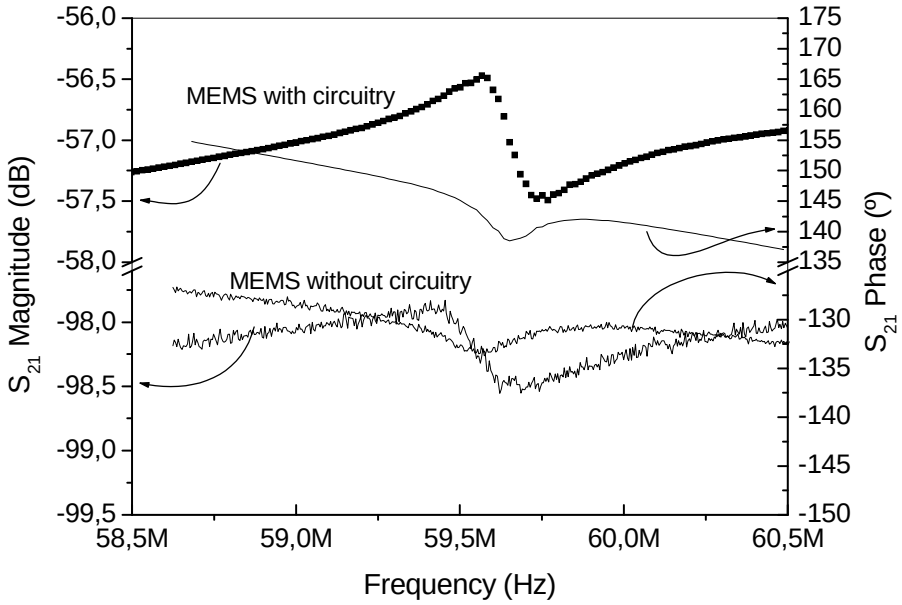


Figure 5.28: *S_{21} transmission curves, showing magnitude and phase for the MEMS device with and without readout circuitry.*

Electrical characterization

Electrical characterization of the bridge resonator has been performed using a network analyzer, as described in appendix B. As is there explained, the motional current generated by the *MEMS* has been measured using a two-port measurement. A DC voltage is applied to the bridge, an AC excitation voltage is applied to one driver and the readout current signal is acquired from the readout electrode.

Two different electrical characterizations of the bridge frequency response around the resonance have been done: 1) with an on-chip integrated *CMOS* amplifier and 2) directly connecting the readout electrode to a network analyzer. In this case, the *CMOS* circuitry employed is the one that is based on the integration of the capacitive current generated by the resonator, and explained in section 5.2.1. The total transimpedance gain of the readout circuit is $500k\Omega$ at $60MHz$.

Figure 5.28 represents the measured transmission spectrum S_{21} (magnitude and phase) for an $80V$ DC polarization of the bridge, with and without on-chip amplification. In both cases, a mechanical resonance of approximately $60MHz$ is observed, which is in accordance with the expected values provided by Coventor simulations. The experimental value of the resonance frequency, that is depicted in table 5.8, corresponds to the extrapolated value at $0V$, after measuring the resonance curves and the resonance frequencies for different DC

applied voltages. It shall be pointed out that this resonance frequency is slightly different than the mechanical resonance, and the natural frequency (in vacuum and without applying dissipative forces to the resonator), but for simplicity this will be the given value.

Two main differences can be highlighted from these results:

- On-chip circuitry reduces, as expected, the insertion loss of the *MEMS* device from 98 to 57dB.

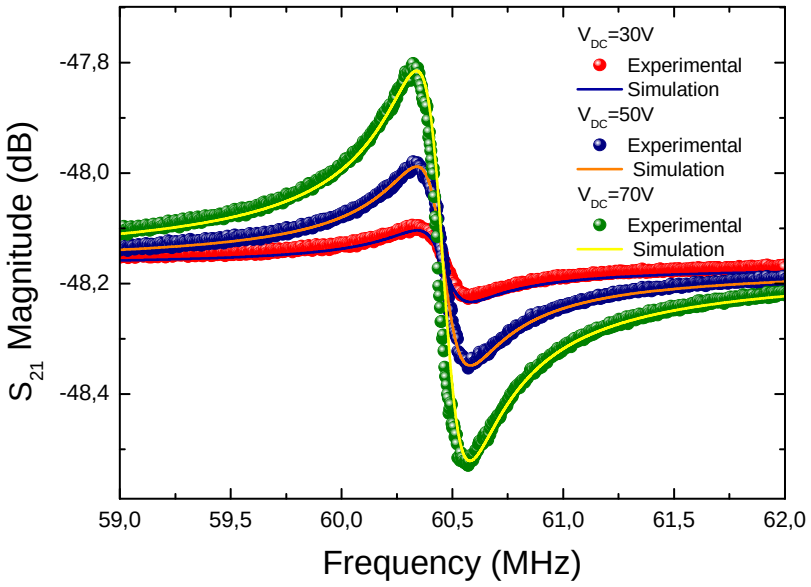
- Higher electrical Q-factor is deduced in the on-chip amplification scheme (from a Q-factor less than 10 to a Q-factor over 30). This improvement of the experimental Q-factor (at least by a factor 3) of the *MEMS* with on-chip amplification is due to the minimization of the Q-loading effect inherent to the method of electrical detection used. The use of the on-chip redout circuit reduces the value of the coupling capacitance between the excitation and readout electrodes (C_0) and because no electrical connections to any probe pad for the readout electrode are used. In this way, the Q factor is increased due to the reduction of the parasitic current (across the coupling capacitance) that masks the motional current. Higher Q factors are expected with low pressure measurements, as it has been demonstrated in previous works based on cantilevers [97].

Although using a *CMOS* circuitry to amplify the signal generated by the resonator and applying up to $80V$ to the bridge, small resonance peaks of $1.5dB$ or less are measured as a consequence of small values of resonance current generated. This is a consequence of the limitation of a fixed gap distance between resonator and electrode above $600nm$.

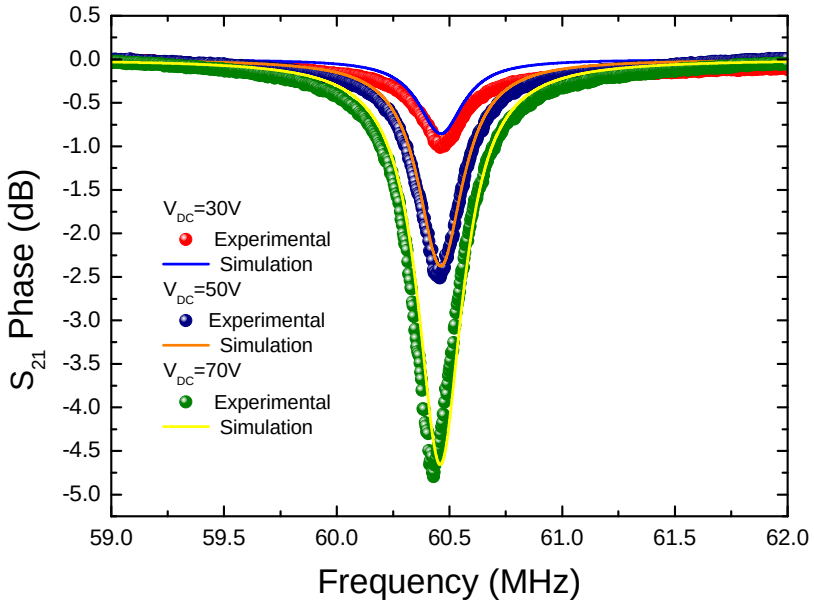
Model fitting

A similar device like the one depicted in figure 5.27, provided with an integrated CMOS circuitry was the basis of a modelization study whose main purpose was to fit the experimental curves with the PSPICE model (see chapter 2) of a clamped-clamped beam. Taking the advantage of the facilities to implement the equivalent electrical circuit of the capacitive readout circuitry and the input and output ports of the network analyzer, experimental curves measured in a two-port configuration were adjusted and fitted by accurately selecting the parameter models.

S_{21} transmission curves, magnitude and phase, for different voltages applied were fit by choosing accurately the input parameters of the model. Dimensions of the device were also adjusted in order to achieve an accurate fit of experimental and simulated curves. Figure 5.29 shows the fit of the experimental curves to the simulated ones for different applied voltages, both in magnitude and phase. The fit is done as expenses of adjusting the input parameter values, which are summarized in table 5.9. The adjusted value for the Young's modulus is $60GPa$, that is below the theoretical value for the aluminum.



(a) S_{21} magnitude, experimental and simulated



(b) S_{21} phase, experimental and simulated

Figure 5.29: *Experimental data versus simulated data for a c-c- beam like the one depicted in figure 5.27(b).*

Model Parameter	**Value**	Units
L	10	μm
w	1.15	μm
s	700	nm
h	1	μm
Q	250	
E	72.6	GPa
ρ	$2.70 \cdot 10^3$	kg/m^3
m_{eff}	$8.7 \cdot 10^{-15}$	kg
k	1.2	kN/m
f_{res}	60.4	MHz
V_{DC}	above $100V$	V
V_{AC}	18	dBm
R	3.5	$T\Omega$
L	2.3	MH
C	3.0	yF
C_{FF}	39	aF
C_{IN}	10	fF
$Responsivity$	0.3	Hz/ag

Table 5.9: *Parameter values used to fit the measured curves represented in figure 5.29.*

The transmission spectrum S_{21} (magnitude and phase), shown in figure 5.29, has been measured for different DC applied voltages showing the spring-softening effect due to the electrostatic excitation of the mechanical structure. An increase of the applied voltages gives, as a result, a shift in the resonant frequency to lower frequency values. This is a known effect in electrostatic driven resonators, [47].

5.2.3 MET1-POLY1 vertical resonators

It was studied in section 4.4 of the last chapter, the viability of integrating vertical resonators using a metal layer as structural material. The result of the study determined that the best option in terms of electrical response was the MET1-POLY1 approach, that consisted on using MET1 as resonator structural material and POLY1 as electrode structural material. Designs and results on this approach are reported in this section.

	Resonance mode	
	Translational	Torsional
Resonance Frequency	$12.7MHz$	$21.1MHz$
Young's modulus	**Poisson's ratio**	
$77GPa$	0.3	

Table 5.10: *FEM-Simulated resonance frequencies for the paddle shaped resonator shown in figure 5.30. The table also shows the material constants used for the simulation.*

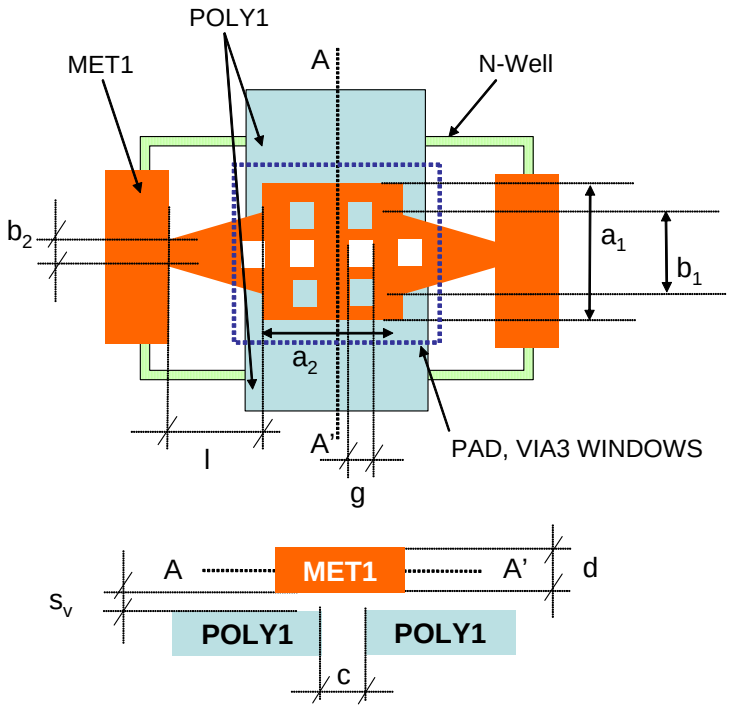
Design

The designed vertical structure is based on a paddle shaped structure. This structure presents a torsional vibrational mode, which is characterized to have a high quality factor value.

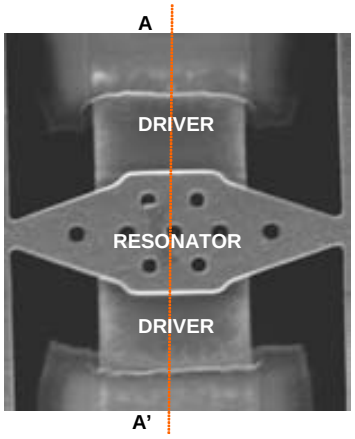
In figure 5.30(a) is depicted a layout of the designed structure. The arms of the paddles have been drawn in a triangular shape in order to increase the frequency of the torsional resonance mode versus the torsional mode. The dimension of the structures are shown in table 5.11. The distance between the two polysilicon electrodes is $450nm$, the minimum distance between two adjacent polysilicon lines. The vertical distance between resonator and electrodes is also determined by the ILDFOX thickness, that is the inter-POLY2-MET1 oxide and shows a typical thickness of $650nm$.

On top of the resonator, a PAD window layer in order to remove the passivation layers as well as VIA3 layer has been opened in order to remove partially the oxide thickness on top of the resonator and therefore fasten the wet etching releasing process. In figure 5.31(a) are reproduced the different layers of the design, showing the characteristic dimensions of the structures.

The triangular shaped arms imposed a different moment of inertia than the rectangular beam used for calculating an expression of the equivalent spring constant and the resonance frequency of a paddle in the torsional mode, that were depicted in previous chapter 2. The lack of equations to modelize the structure, explains in this case the use of a FEM tool [46] in order to predict and design the resonance frequency of such a device. Results from simulations are: $12.7MHz$ for the translational mode and $21.1MHz$ for the torsional resonant mode. Table 5.10 shows the results of the simulations as well as the material constants properties for the resonator structural layer.

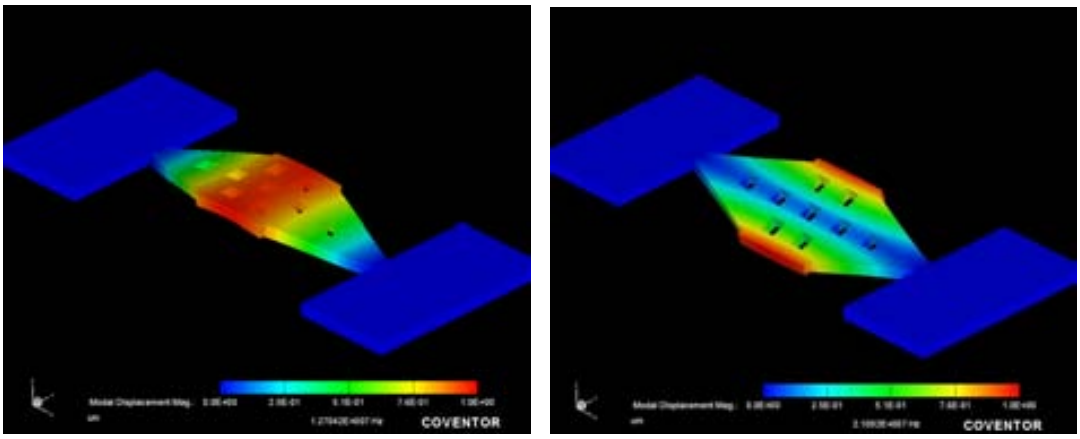


(a) Scheme of the vertical paddle resonator, showing its characteristic dimensions



(b) SEM image on top of the paddle shaped device

Figure 5.30: *Paddle shaped structure implemented by the MET1-POLY1 approach. In table 5.11 are shown the dimensions of the fabricated device.*



(a) Simulated translational mode (b) Simulated torsional mode

Figure 5.31: *Results obtained by the FEM simulation for the translational and torsional modes of vibration.*

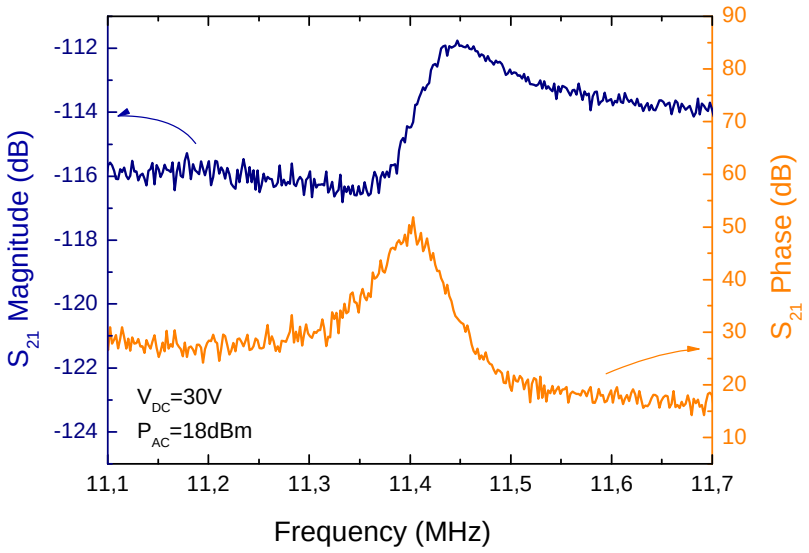
Structural characterization

The structures are designed with holes in order to facilitate and fasten the post-CMOS releasing process. A total time of $10 + 4min$ are necessary in order to remove the sacrificial layers surrounding the resonator, that are IMD2, IMD1 and IDLFOX.

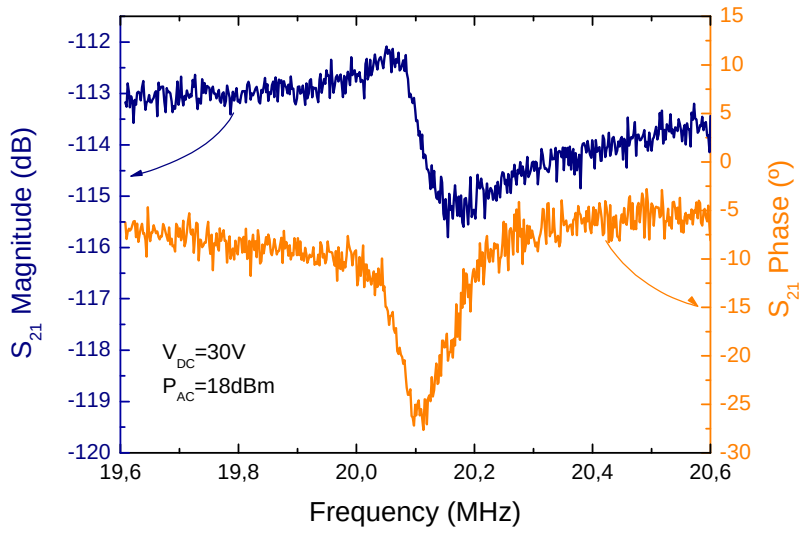
Figure 5.30 shows a fabricated device that has been released. Dimensions of the fabricated device are in concordance with the drawn dimensions; however, squared holes and corners seem to be rounded due to limited photolithography resolution.

Dimension	**Value**
a_1	$5\mu m$
a_2	$4\mu m$
l	$5\mu m$
b_1	$4.5\mu m$
b_2	$0.8\mu m$
g	$0.8\mu m$
s_v	$600nm$
c	$450nm$

Table 5.11: *Dimensions of the paddle shaped resonator depicted in figure 5.30.*



(a) S_{21} curves around the resonance peak for the translational mode



(b) S_{21} curves around the resonance peak for the torsional mode

Figure 5.32: *Electrical characterization of the paddle resonator shown in figure 5.30(b) for two resonances modes, translational and torsional.*

Electrical characterization

The electrical characterization has been performed by a two-port configuration, using the three electrical connections available on this device, driver, read-out and resonator electrodes.

Two different modes have been measured, corresponding to the translational and the torsional modes. Results are shown in figure 5.32. Because of the peaks heights are below $3dB$ it is not possible to measure the quality factor of the resonance modes, but it is deduced that the resonance peak of the torsional mode is bigger than the translational one, because of the width of the resonance peaks on the S_{21} spectrum. The measured resonance frequencies for the translational and torsional modes are: $11.4MHz$ and $20.1MHz$. Measured data are in agreement with the simulated resonance frequencies.

The translational mode exhibits a transmission spectrum near resonance different than previously observed; in that case, the behavior near resonance of the magnitude transmission spectrum, starts with an antiresonance peak and is followed by a resonance peak. Also, the phase transmission spectrum shows an upwards peak instead of the 'traditional' downwards peak. This behavior is related with the phase of the parasitic and resonance current. The translational mode determines the parasitic current to be in-phase with the resonance current, and the consequence is the inverted behavior in front of the 'traditional' out-phase readout.

5.2.4 POLY2-POLY1 vertical resonators

In the design of capacitively transduced resonators, the distance between electrodes and resonator (gap) becomes a relevant parameter and in most cases the fabrication process turns around the minimization of this parameter [76], [75]. However, for monolithically integrated resonators in a commercial technology using the standard layers of the technology, there is no possibility to modify the fabrication process parameters and the designer has fit the design with the available layers.

The electrical response of vertical resonators described in previous section were limited basically by the vertical gap distance between driver and resonators, as it is shown by the strong dependence on the motional resistance on the fourth power of the gap distance. A strategy to decrease the gap distance was described in previous chapter in section 4.5, where the $40nm$-thick inter-polysilicon oxide was presented as a gap spacer between two polysilicon that made the role of the structural material for resonator and electrodes.

Design

The vertical structure chosen to be implemented in the POLY1-POLY2 approach was a paddle shaped structure operating in the torsional mode, as shows figure 5.33(a). In order to promote the torsional mode, two electrodes (of POLY1) are situated symmetrically with respect the horizontal axis of the paddle. The minimum separation of both electrodes is determined by the technology rules, which is the minimum separation for two poly1 lines, i.e. $0.45\mu m$. The idea beyond that design was to extrapolate the MET1-POLY1 approach to the POLY1-POLY2 approach, enhancing the electrical response by decreasing the vertical gap

distance from $640nm$ down to $40nm$. The vertical distance between electrodes and resonator corresponds to the IOX oxide layer, that is $40nm$.

The device was designed to obtain a paddle shaped resonator vibrating in the torsional mode at $100MHz$; the mechanical properties of the POLY2 layers used in the design phase are depicted in table 5.12.

The dimensions of the fabricated device shown in figure 5.33(a) are depicted in table 5.13. Specifically, those dimensions corresponds to a resonance frequency of the torsional mode of $108MHz$.

Structural characterization

In figure 5.33(b) is depicted an optical image of the full system showing the micromechanical resonator integrated along with the CMOS circuitry. A wet etching of $18min$ on duration has been done in order to release the structure; the result is shown in figure 5.33(c). The etching time was not enough to release the structure, and a layer of oxide on top of the resonator is appreciated. However, the shape of the resonator can be envisaged; the PAD and VIA3 and VIA2 windows can be observed in the image.

Electrical characterization

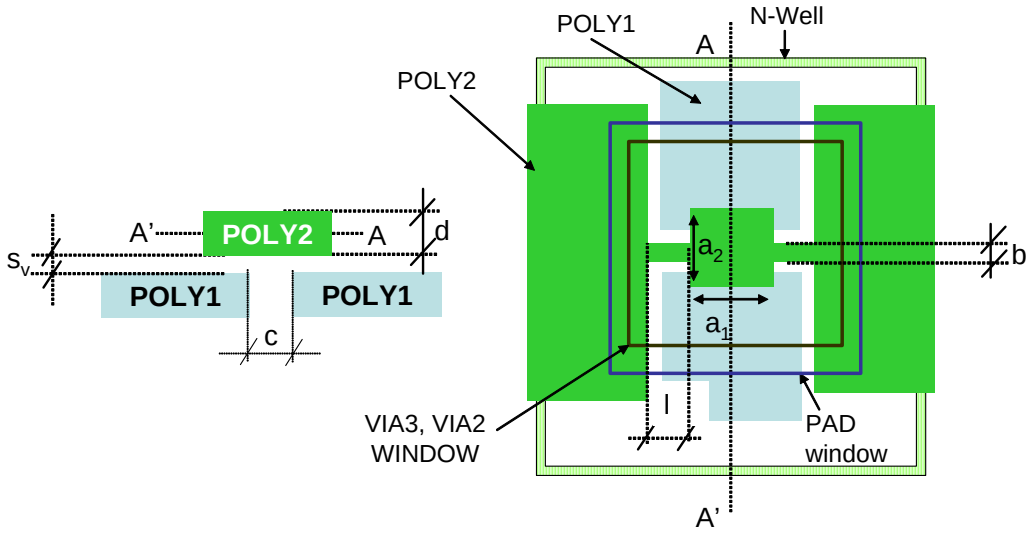
The transducer has been designed for a two-port operation. An alternate AC voltage (from the output port of the network analyzer) is applied to one driver whereas the DC signal is

Material	E, GPa	G^*, GPa	ρ, kg/m^3
Polysilicon	110	67	$2.23 \cdot 10^3$

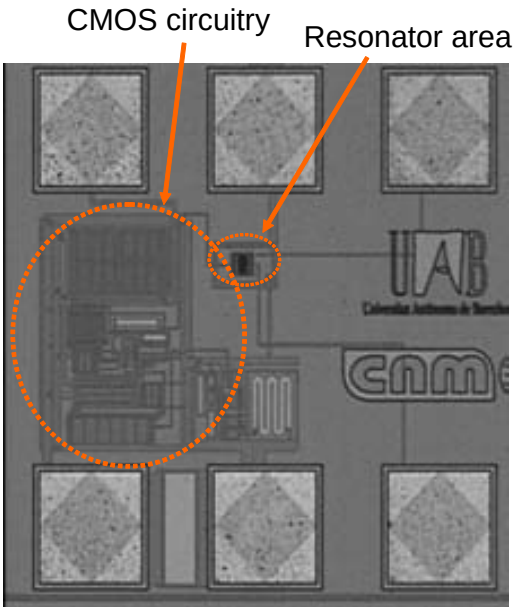
Table 5.12: *Material properties for the POLY2 layer,* $*$ *Shear Young's modulus.*

Dimension	**Value**
a_1	$3\mu m$
a_2	$3\mu m$
l	$3\mu m$
b	$1\mu m$
c	$450nm$
s_v	$40nm$
d	$200nm$

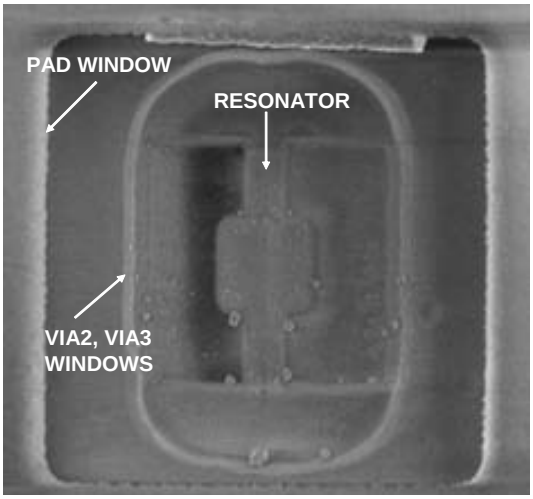
Table 5.13: *Dimensions of the paddle shaped resonator depicted in figure 5.33.*



(a) Scheme of the vertical paddle resonator, showing its characteristic dimensions

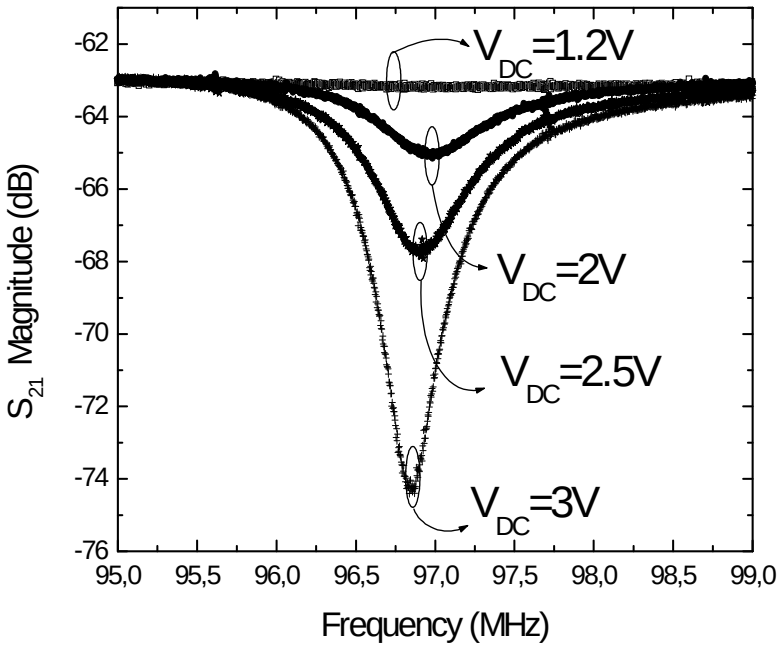


(b) Optical image of the MEMS

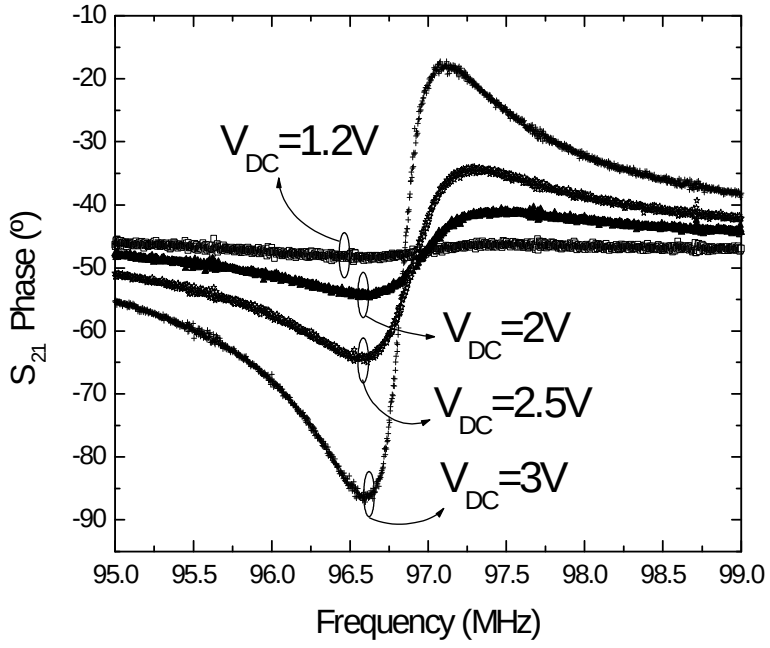


(c) SEM image of paddle shaped device

Figure 5.33: *Paddle shaped structure implemented by the POLY1-POLY2 approach. Optical image and SEM image of the fabricated MEMS and resonator, respectively.*



(a) Magnitude S_{21} curves around the resonance peak



(b) Phase S_{21} curves around the resonance peak

Figure 5.34: *Electrical characterization of the paddle resonator shown in figure 5.33 both in magnitude and phase.*

applied to resonator. The resonance current is collected by the other driver and amplified by the integrated transimpedance circuitry.
Figure 5.34 represents the transmission spectrum S_{21}, both magnitude and phase for $V_{DC} = 3V$ and $P_{AC} = 0dBm$. The resonance frequency is $97.02MHz$ for $V_{DC} = 2V$.
The magnitude of the measured S_{21} parameter shows an antiresonance peak for all the measured voltages. The absence of a resonance peak can be understood by the role of the parasitic current in this device. The large coupling area between two electrodes determines the high value of the parasitic current that reflects the absence of the resonance peak. The value for the parasitic capacitance is estimated by the value of the fringing capacitance between two poly1 lines that is available in the datasheet of the technology. The fringing capacitance is $0.041fF/m$, that results in $0.41fF$ for the $10\mu m$ electrodes long.

From analysis of the previous measurements, a quality factor higher than 300 is achieved at the antiresonance frequency with a low bias polarization voltage ($V_{DC} = 3V$) applied to the paddle. A higher value of the quality factor is expected under the vacuum conditions.

The limitation of this approach is given by low reliability of the releasing process. A vertical $40nm$ gap for this structure determines in high percentage the collapsing of the structures to the electrodes, in the releasing process or in the measurement step.

5.2.5 POLY1-POLY2 in-plane resonators

The low reliability exhibited by the vertical resonators shown in the above section and implemented by using the layers of the CPOLY module, force the new design of a new structure with high reliability. However, the IOX layer, with a thickness of $40nm$ is an excellent candidate to define the gap distance between resonator and electrode. The solution to combine high reliable resonators with the $40nm$-thick gap spacer arises from the figure 4.8. The good conformal behavior together with the vertical sidewalls definition of POLY2 with respect POLY1 focuses the design strategy to lateral in-plane resonators. On that case, one of the polysilicon layer acts as resonator structural material whereas the other one is selected as the electrode material. In this section, the two possibilities of design have been investigated, showing their advantages and drawbacks.

POLY2 as structural material

Design

In order to test the viability of the POLY1-POLY2 approach, a lateral c-c beam has been designed, defining a layout depicted in figure 5.35. In order to avoid the vertical collapse of the structure to the silicon substrate (as the resonator is released), a triangular shaped anchors for resonator as well for electrodes are designed.
In order to reduce the post-CMOS process time, a set of via layers are drawn to faster activate the releasing of the resonator in the wet etch solution. The drawn dimensions as well as the

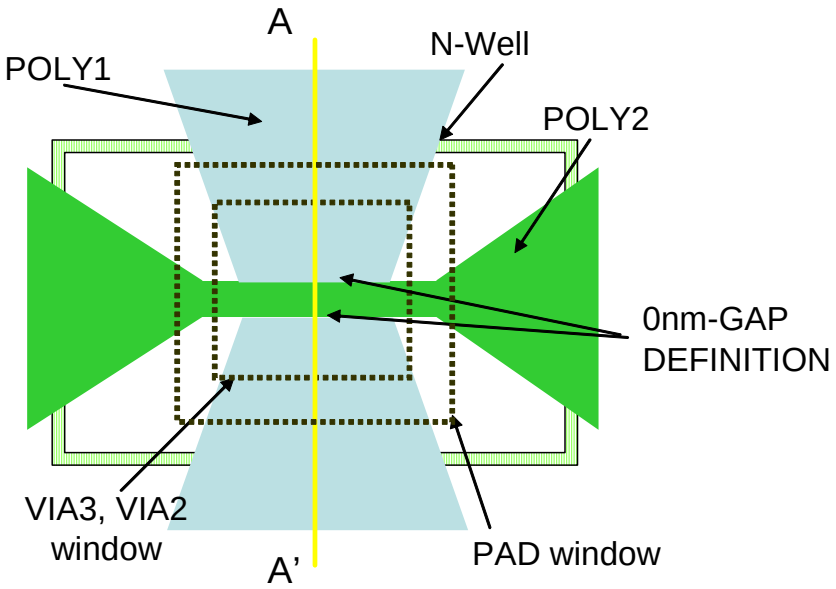


Figure 5.35: *Layout showing the CMOS technology layers used to design a lateral c-c beam by the POLY1-POLY2 approach. POLY2 is the resonator structural material.*

measured ones are depicted in table 5.14.

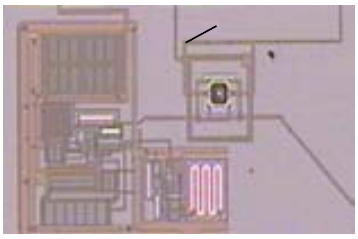
Physical characterization

Figure 5.36(a) is an optical image of the MEMS device showing the resonator monolithically integrated along with a CMOS buffer amplifier. From the resonator point of view, the structural material for electrodes and resonant structures were POLY1 and POLY2, respectively. Figure 5.36(b) shows the resonator area after the post-CMOS releasing process, and where the pad layer aperture limits the resonator area after the post-CMOS process.

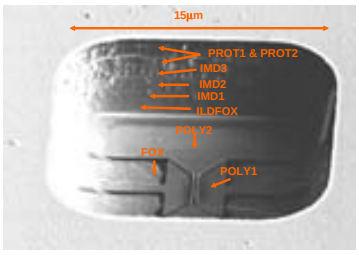
The fabricated device is $4\mu m$ long, $500nm$ wide and $200nm$ thick and lateral gap has apparent

	Layout	**Simulated**	**Measured**
Width, b	$650nm$		$500nm$
Length, L	$4\mu m$		$4\mu m$
Gap distance, s	$40nm$		$40nm$
Resonance frequency		$250MHz$	$200MHz$

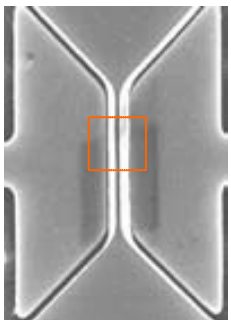
Table 5.14: *Layout versus fabricated dimensions. The table also shows the resonance frequency predicted and measured.*



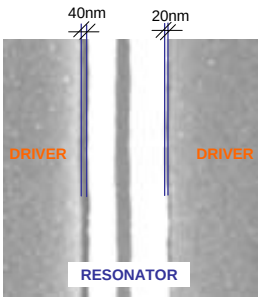
(a) Optical image of the MEMS device



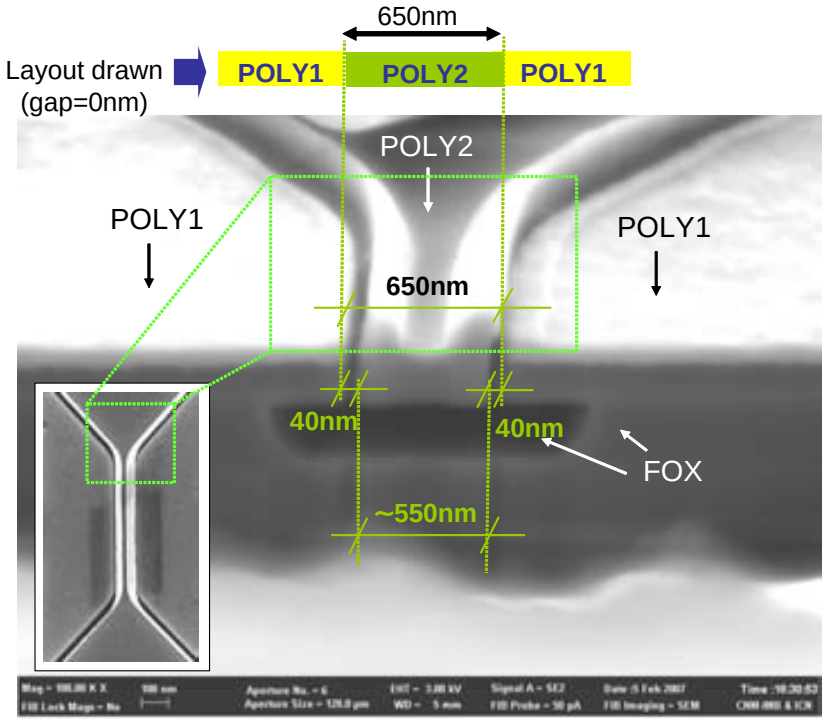
(b) SEM image of the c-c beam after releasing. The resonator area is defined by the PAD window



(c) SEM image showing the top view of the c-c beam



(d) Top view image of a c-c beam, showing an apparent asymmetry on the gap distances



(e) Sidewall profile of a c-c beam performed by means of a FIB

Figure 5.36: *Structural characterization of a c-c beam fabricated by the POLY1-POLY2 approach. POLY2 is the resonator structural material.*

values of $20nm$ and $40nm$, extracted from figures 5.36(c) and 5.36(d). Table 5.14 shows the measured versus the designed dimensions. The apparent asymmetry of gap distances are observed in figure 5.36(d), where a top view image is taken in the SEM microscope. Apparent measured gaps are $40nm$ and $20nm$, approximately.

In order to characterize the electrode-resonator area, a profile of the structure has been performed by means of a FIB. The result is shown in figure 5.36(e), where the two gaps are measured to be equals and defining a distance between resonator to electrode of $40nm$. The gap difference seen in the top view of the image are attributed to the optical misalignment of the technology. However, and independently of this misalignment the lateral gap is always $40nm$, i.e, the thickness of the IOX layer.

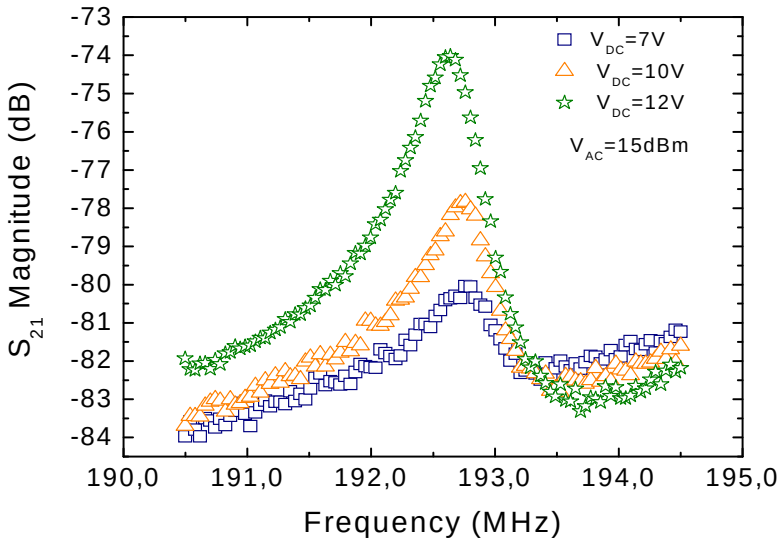
The observed width of the fabricated c-c beam is different than the width designed. Furthermore, the POLY2 losses the planar profile in the area closer to the driver.

Electrical characterization

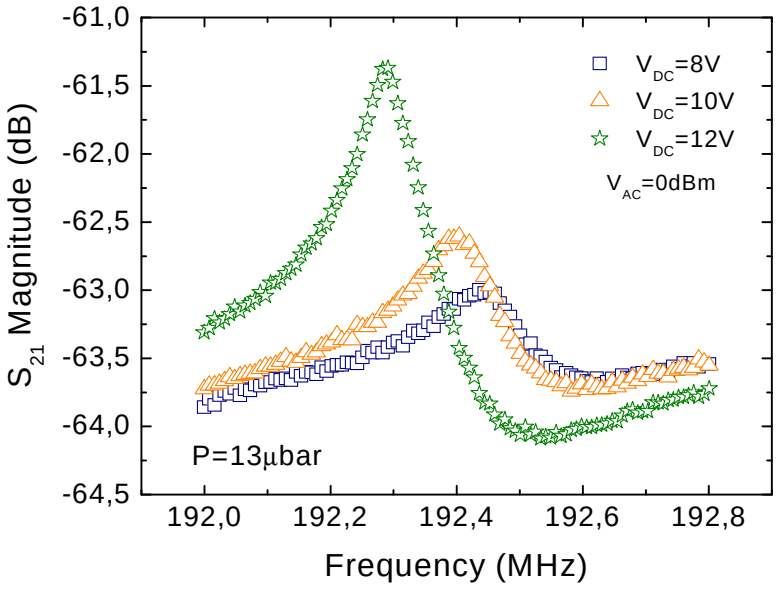
S_{21} transmission curves have been measured both in air and in vacuum using the experimental setup described in appendix B. Figures 5.37(a) and 5.37(b) show the transmission frequency response for different values of the DC voltage applied to the resonator for air and vacuum conditions, respectively. The typical DC values do not exceed the $20V$. The ac values for air measurements are $15dBm$ and for vacuum $0dBm$; a minimized effect of the noise in the measured signal is observed when increasing the ac power. The quality factor of the device operating in air and in vacuum are extracted from figures 5.37(a) and 5.37(b), obtaining $Q_{air} = 300$ and $Q_{air} = 1033$, respectively.

In order to extract a more accurate Q factor value with a minimized influence of the parasitic capacitances, mixing measurements have been performed for the device with the CMOS integrated circuitry. Performing the mixing setup shown in figure 5.38, a mixing measurement has been carried out with the MEMS device operated in vacuum ($13\mu bar$). The result for this experiment is shown in Figure 5.38. The measurement conditions where: for the RF signal applied at one electrode ac power, $P_{RF} = 15dBm$ and frequency centered at $f_{RF-c} = 182.2MHz$ with $\Delta f_{RF-s} = 1MHz$ of span; for the ac signal applied at the resonator $f_{LO} = 10MHz$ and $P_{LO} = 10dBm$ plus a DC voltage of $17V$. Then, an up-conversion mixing measurement was performed. From this measurement, the extracted Q is around 1000, obtaining a $f \times Q$ product of $2 \times 10^{11}Hz$, which represents an improvement from previous limits for monolithically *CMOS* integrated devices $f \times Q = 6 \times 10^{9}Hz$ [19].

These devices offer low controllability of the resonance frequency due to the triangular shape of the anchors. For this reason, a new design showing square anchor was performed. Results are presented in next section.

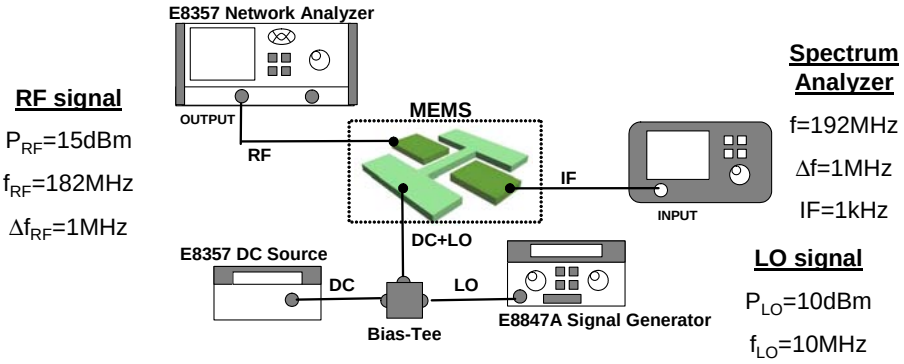


(a) S_{21} air measurements

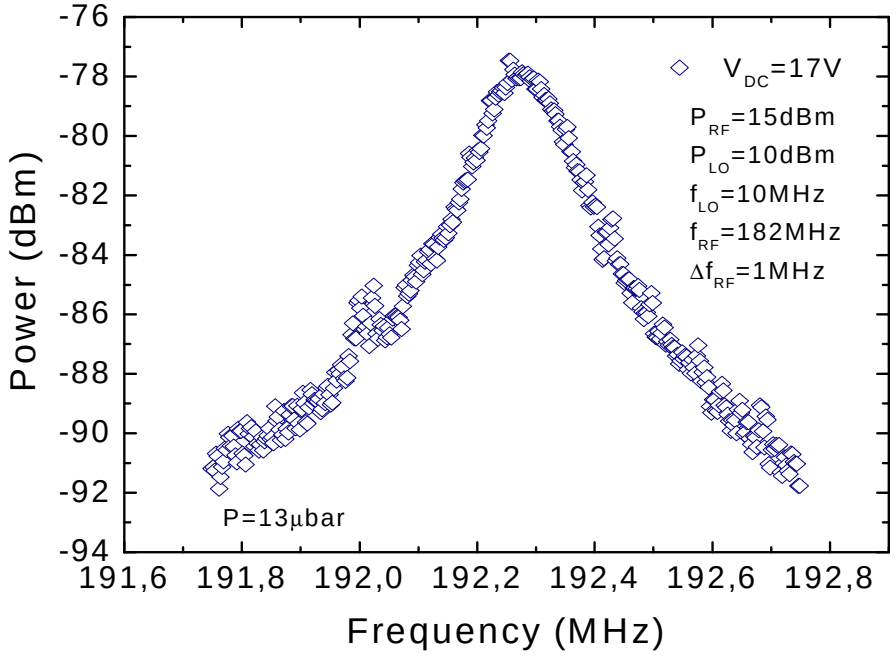


(b) S_{21} vacuum measurements

Figure 5.37: *S_{21} transmission curves in vacuum and in air for the device shown in figure 5.36.*



(a) Experimental setup and measurements conditions for the mixing measurement



(b) Mixing measurement of the c-c beam designed

Figure 5.38: *Signal measured at the input port of the spectrum analyzer when performing the mixing measurement above described.*

Drawn Length (μm)	Drawn Width (nm)	Thickness (nm)	Fabricated Length (μm)	Fabricated Width (nm)
4	650	282	4	710

Table 5.15: *Design and fabricated dimensions for device shown in figure 5.39 .*

5.2.6 POLY1 as structural layer. An improvement

Up to now, the clamped-clamped beam resonators fabricated using the capacitance module have been designed choosing polylisilicon2 as the structural material for the resonator. However, the election of this material as structural material is not the best choice due to the following factors:

- The main reason that limits the election of polysilicon2 as structural material for resonators is that the dimensions drawn on the layout do not corresponds to the final device. The designed width, that is defined typically as $0.65\mu m$ (because is the minimum distance of two lines of POLY1 in the capacitance module), results in a bridge width less than $0.5\mu m$. This is due to the fact that POLY2 does not lie in a planar surface but in a surface where previously POLY1 and the thin silicon oxide have been deposited. Figure 5.36 shows this fact, where differences between drawn layout and fabricated device can be observed. This differences can limit the design stage, giving different device's frequencies than those which were designed to. Furthermore, the crossection shape of the device also can vary the resonance frequency, making difficult the design step.

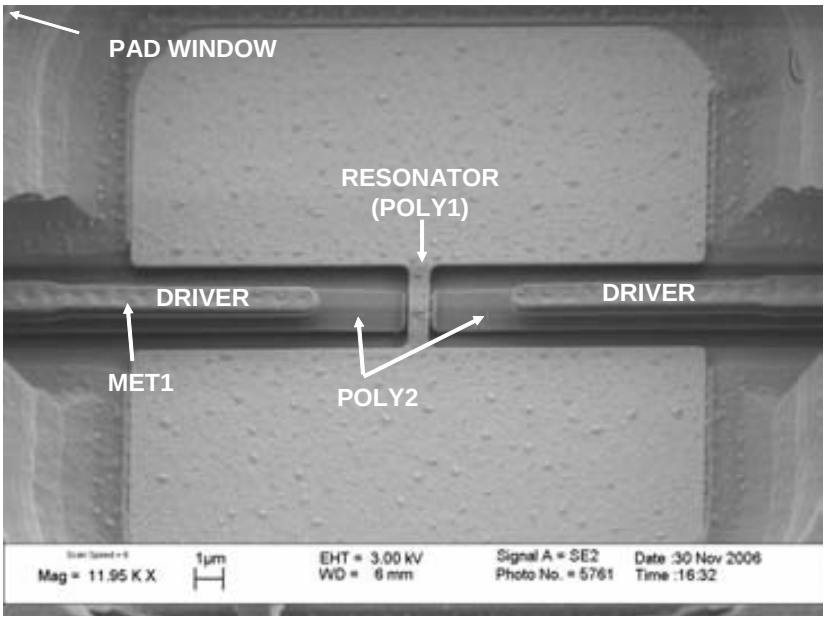
- In some published works [37], the thickness of the material is related with the maximum achievable Q. In this sense, POLY1 exhibits a nominal thickness of $282nm$, whereas the thickness of polysilicon2 is $200nm$.

Design

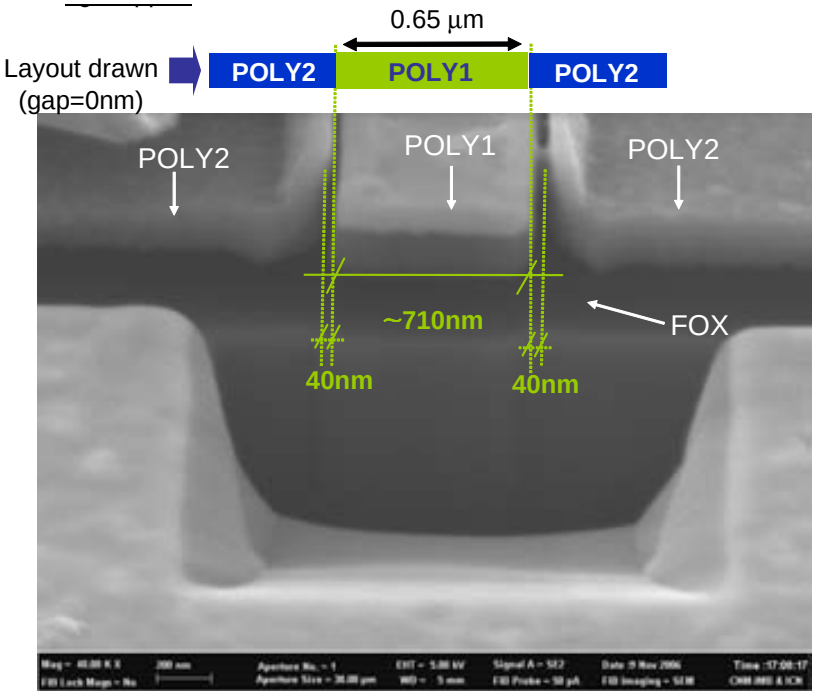
New generation of devices were designed and fabricated using POLY1 as structural material. Furthermore, a new design was employed to draw the clamped-clamped resonators. The new approach consists on drawing the anchors at straight angle with respect to the bridge. This is done in order to increase the frequency controllability of such devices.

Structural characterization

Figure 5.39 shows a SEM image of one of this new-generation fabricated device and table 5.15 its dimensions. The width of the fabricated device does not corresponds exactly with the drawn width, and the device is approximately $60nm$ wider than designed, which corresponds on $30nm$ by side. However, the deposited polysilicon seems to be planarized and without any cracks on the surface.



(a) SEM top view image of the MEMS device



(b) SEM image showing the profile performed by means of a FIB

Figure 5.39: *SEM image showing a clamped-clamped beam with right angle anchors.*

Electrical characterization

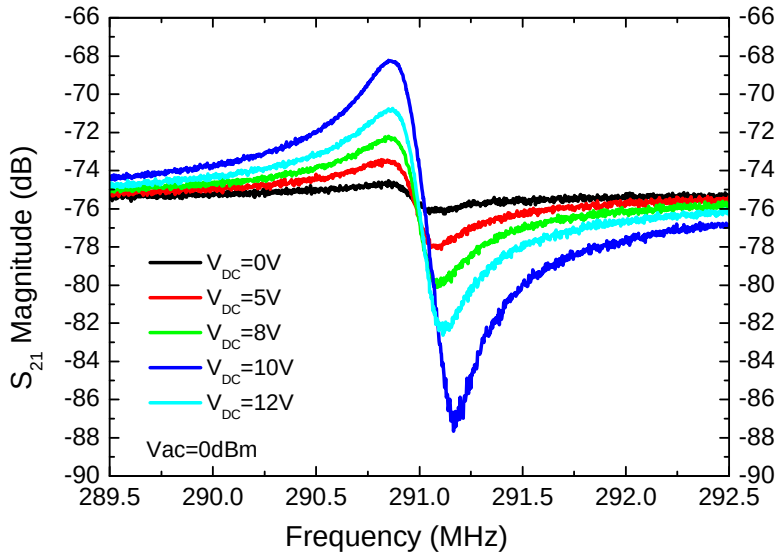
A similar device than depicted in figure 5.36, and with a transimpedance amplifier integrated circuitry has been characterized and tested both in air and in vacuum. The first measurements performed to the device are shown in figure 5.40. They correspond to a S_{21} measurements in air near resonance for different DC applied voltages in the range from $5V$ to $15V$. The measurement is split in magnitude and phase for the S_{21} transmission parameter. The electrical resonance frequency obtained is $290.8MHz$ for the maximum voltage applied, ($V_{DC} = 15V$). For that voltage, the resonance peak has an amplitude of $8dB$ and antiresonance peak of $12dB$. The shift on the phase is 90^o. The appearance of the antiresonance peak in the S_{21} magnitude plot reveals the effect of the parasitic current on the measurement. Due to the proximity of both electrodes, (less than $1\mu m$), the excitation voltage signal is coupled by means of fringing capacitances to the readout electrode. The measured quality factor in this plot is only $Q = 800$. However, the influence of the parasitic current is limiting the maximum value of the the resonance peak and then, the Q factor maximum value. In addition, the measured resonance frequency corresponds to the electrical resonance frequency that is different from the intrinsic mechanical resonance frequency.

For this reason, mixing measurements have been performed in this device both in air and in vacuum. For vacuum measurements, a wire-bonding was performed on the chip device connecting the electrical pads to a *PCB* specifically designed for high-frequency measurements. Results are shown in figure 5.41. Both measurements were performed under the same conditions, the same applied signal and electrical connections through the wires of the wire-bonding (except for the pressure conditions).

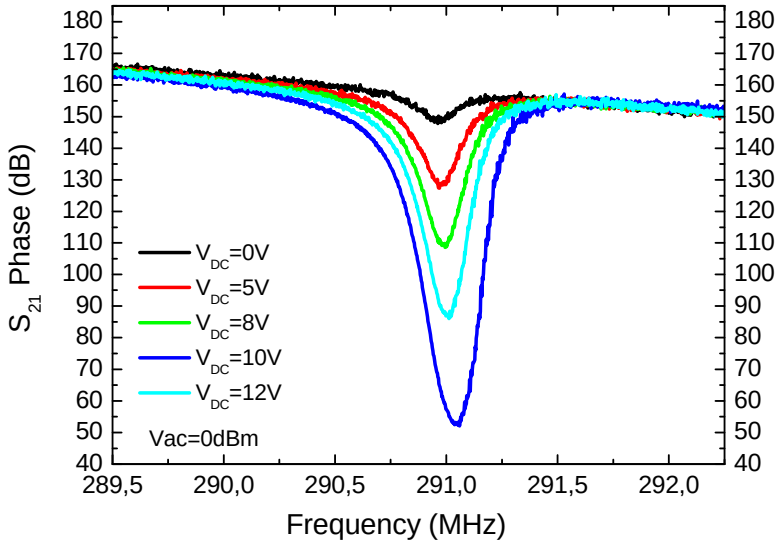
Experimental configuration to make mixing measurements is depicted in the appendix B. The values for the power applied, center frequency and span frequency are depicted in figure 5.41(a). The vacuum level for the measurement in vacuum was $20\mu bar$. The resonance frequency measured in air was $f_{RES-AIR} = 290.39MHz$ and in vacuum was $f_{RES-VAC} = 290.45MHz$. Resonance frequencies both in air and in vacuum are slightly different due to the influence of the Q factor on the mechanical resonance frequency by the equation $w = w_0\sqrt{1 - \frac{1}{2Q}}$. The extracted Q factor gives a value of 970 in air and 2836 in vacuum. The quality factor is multiplied in a factor by 3 just in a vacuum atmosphere. It shall be pointed that the previous value for the quality factor in air was only 800 (obtained from the S_{21} measurement) whereas in the mixing measurement a value of 970 is obtained. Then, the parasitic current limits the resonance peak, yielding a lower quality factor.

POLY1 Young's modulus extraction

The material properties of the resonator structural material, i.e. Young's modulus, can be indirectly derived by studying the mechanical resonance frequency versus the squared applied voltage, so that the natural resonance frequency can be obtained, $f_{res,0}$. In order to derive the

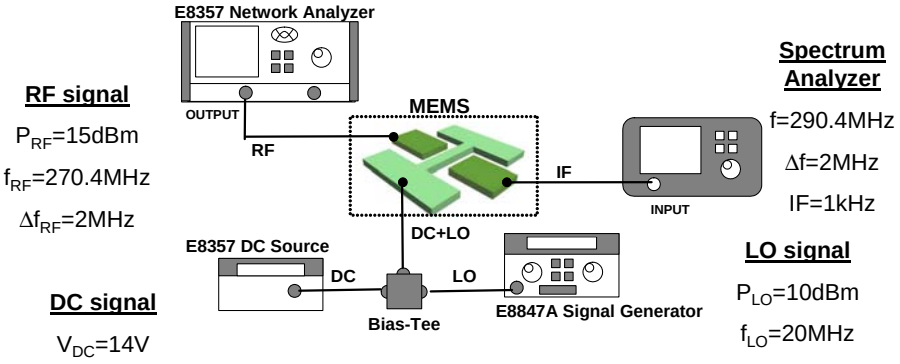


(a) Transmission measurement, magnitude

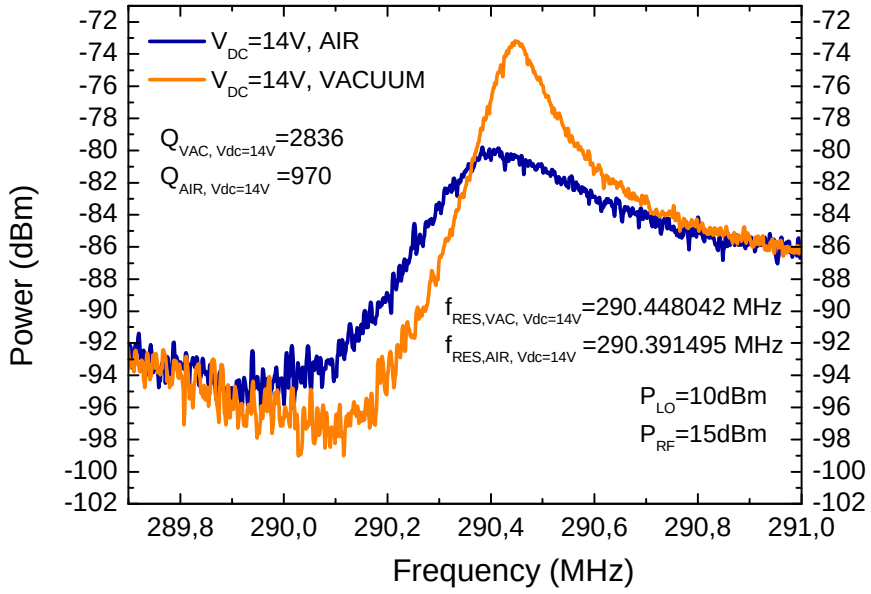


(b) Transmission measurement, phase

Figure 5.40: *Electrical response for measuring MEMS devices using the two-port configuration, perfmrmed in a similar device that the one depicted in figure 5.39(a).*



(a) Experimental setup and measurements conditions for the mixing measurement



(b) Mixing measurement of the c-c beam designed

Figure 5.41: *Mixing experimental setup and signal measured at the input port of the spectrum analyzer in air and in vacuum, for a similar device that the one depicted in figure 5.39(a).*

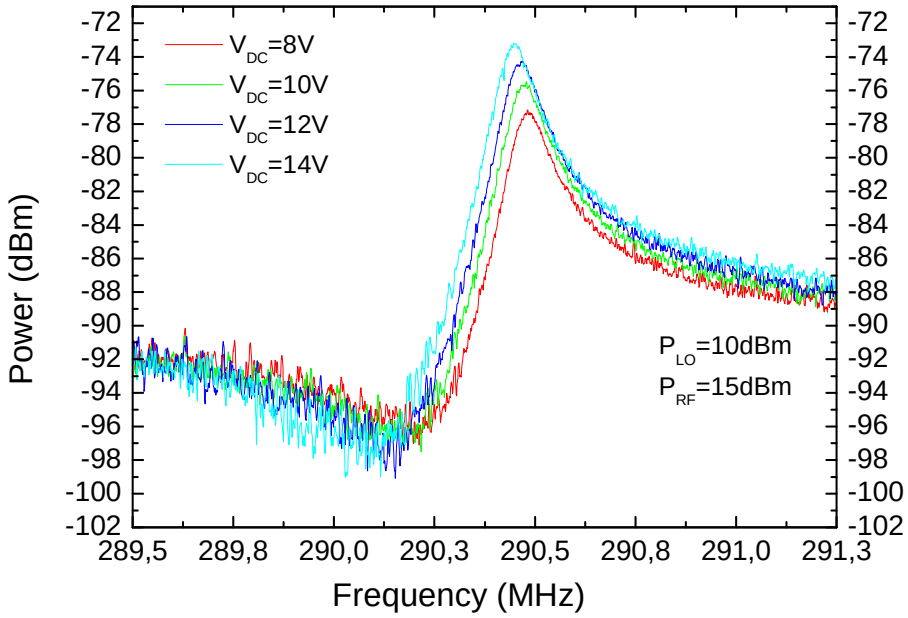


Figure 5.42: *Mixing measurements performed in vacuum, for different DC applied voltages, performed in a similar device that the one depicted in figure 5.39(a).*

relation $\frac{E}{\rho}$, different curves where obtained by mixing measurements performed at different applied voltages. Figure 5.42 shows resonance curves obtained applying the signals defined in figure 5.41(a), except for the DC applied voltage, that varied for each measurement, in the range from $5V$ to $15V$. The resonance frequency is measured for each curve and those values are plotted against the squared DC voltage, as shows figure 5.43. From the resonance frequency values a linear fit is performed in order to derivate the origin ordinate. The value corresponds to the mechanical resonance frequency in the absence of applied voltages. From this value, $f_{res,0} = 290.49MHz$, the relation $\frac{E}{\rho}$ is calculated by the analytical expression that relates the natural resonance frequency of a bridge with its dimensions. The resonance frequency of a c-c beam is given by this equation:

$$f_{res,0V} = \frac{(2.365)^2}{\sqrt{3}} \sqrt{\frac{E}{\rho}} \frac{b}{L^2} \tag{5.5}$$

The relation $\frac{E}{\rho}$ is derived from the above equation:

$$\frac{E}{\rho} = \left(\frac{1}{2 \times \pi \frac{2}{\sqrt{3}} (2.365)^2 \frac{1}{f_{res}} \frac{w}{L^2}} \right)^{-2} \tag{5.6}$$

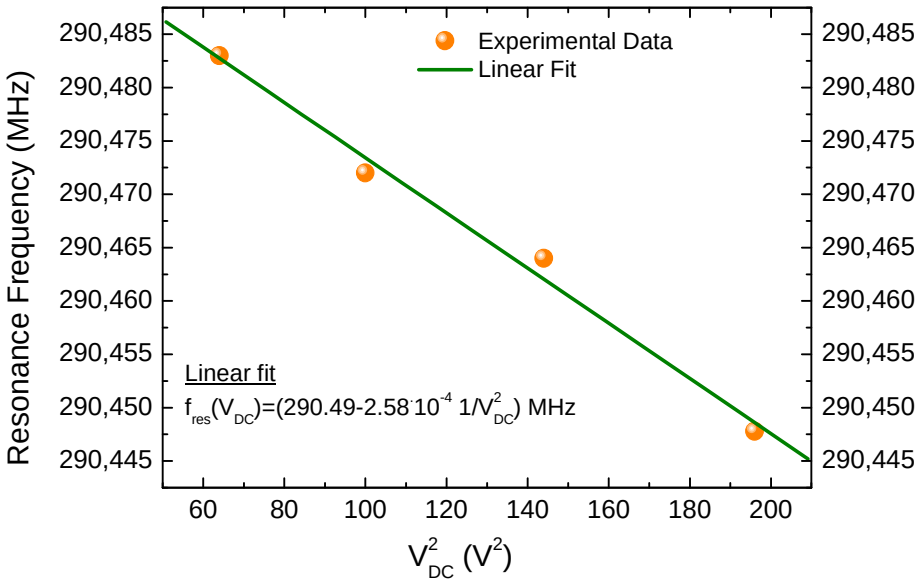


Figure 5.43: *Resonance frequency versus the squared DC voltage applied in mixing measurements in vacuum, extracted from measurements depicted in figure 5.42.*

From dimensions obtained from SEM images ($b = 710nm$ and $L = 4\mu m$) the calculated value for the relation $\frac{E}{\rho}$ is

$$\frac{E}{\rho} = 4.43 \cdot 10^7 \frac{Pa \cdot m^3}{kg} \tag{5.7}$$

For the polysilicon, the mass density is $\rho = 2.23 \cdot 10^3 kg/m^3$, then, the equivalent POLY Young's modulus is:

$$E = 100GPa \tag{5.8}$$

An unusual shape on the resonance curves measured by mixing techniques is observed in figure 5.42. The expected resonance peak is a symmetrical lorentzian curve, but the measured curves present an asymmetry with respect to the resonance frequency. This behavior is associated with the wire-bonding performed on those chips, necessary to measure them under vacuum conditions. This behavior has not been observed when measuring in air conditions with the RF-probes contacting directly to the electrical pads.

Circuitry performance

It is crucial to know which is the impact of integrating the circuitry along with the microresonator. At this level, the circuitry has been developed in order to amplify and adapt the mechanical current generated at the resonator. In future works, the circuitry will have the role of achieving the oscillator functionality.

A two-port measurement has been carried out in similar devices with and without CMOS circuitry in order to compare the advantages of incorporating an integrated amplifier. The device is a POLY1-POLY2 c-c beam, $5\mu m$-long with a resonance frequency around $180MHz$ and the circuit is a transimpedance amplifier. Two main differences in the transmission spectrum, shown in figure 5.44, can be deduced from the measurements. The first one is the level of the coupling signal, that for the device with the TIA attached is $-85dB$ and without the circuitry falls below the $-95dB$; this difference is due to the coupling between the resonator and the load impedance: for the device plus circuit, the load is the input impedance of the circuit; for the device alone, the load are the 50Ω of the network analyzer. The more demanding load is the input impedance of the network analyzer which presents a larger mismatch with the output impedance of the device.

The second different behavior is related with the shape of the electrical resonance. For the device without circuitry, no resonance peak is observed, i.e, the resonance peak is masked by the anti-resonance peak, that in this case is very sharp. The anti-resonance peak is associated with the effect of the parasitic current in the overall current. For the device with integrated circuitry, the effect of those parasitic current are lowered as expenses of dramatically reducing the distances from the resonator readout electrode to the electrical circuit.

A comparison between the two circuits has also been performed. The resonator, as before is a POLY1-POLY2 c-c beam but in that case is $4\mu m$-long, and with a natural resonance frequency around $290MHz$. The performance of both electrical circuits (transimpedance amplifier and capacitive readout) is shown in figure 5.45. In both curves, the effect of the parasitic capacitances is reduced due to the proximity of the readout circuitry. However, a substantial difference is observed in terms of the coupling levels in the transmission signal. For the capacitive readout, the coupling level is around $-50dB$ whereas for the TIA is $-75dB$. Those differences are associated to the impedance mismatch between the resonator and the electrical circuit. With those measurements, the device impedances can be extracted and the circuitry can be designed more precisely knowing the resonance frequencies and the electrical current.

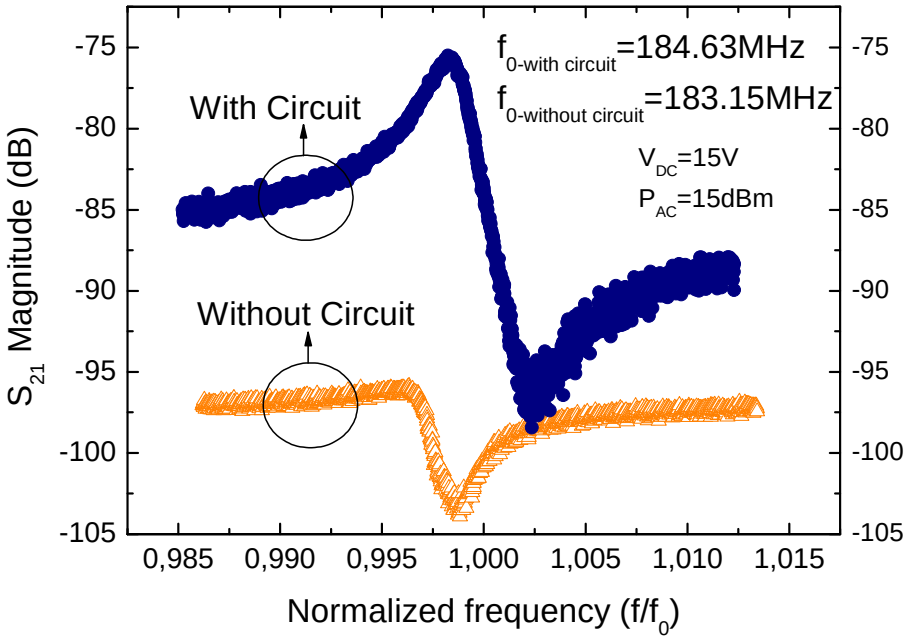


Figure 5.44: *Electrical response near frequency of a 5μm c-c beam, with and without integrated readout circuitry.*

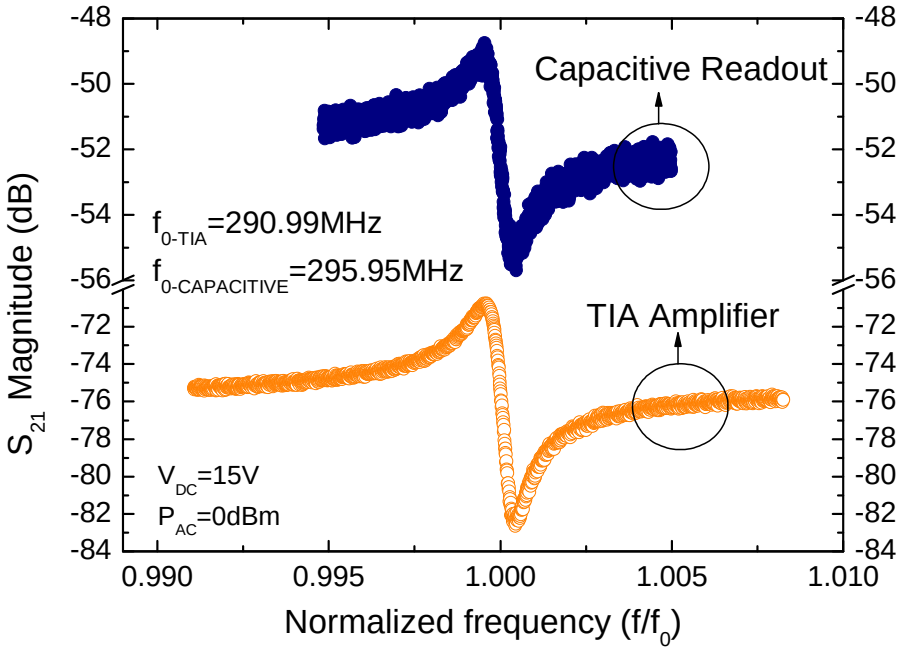


Figure 5.45: *Electrical response of a 4μm c-c beam, with two different readout circuits, the TIA and the capacitive readout.*

Structure	Dimensions	f_0
LBAR	$L = 72.4\mu m$	$34.5MHz$
	$s = 60nm$	
	$b_{end} = 10\mu m$	
Square-shaped	$L = 42.3\mu m$	$90.8MHz$
Disk-shaped	$R = 27.9\mu m$	$78.6MHz$

Table 5.16: *Summary of the tested devices fabricated by the air-gap fabrication process.*

CMOS compatible material

Material	Deposition technique	ϵ_r	Step coverage
SiO_2	LPCVD	3.1	Excellent
Si_3N_4	LPCVD	$6.7 - 7$	Excellent

Non-CMOS compatible material

Material	Deposition	ϵ_r	Step coverage
C_4F_8	Plasma	2.4	Excellent
AlN	Reactive Sputtering	10	Excellent

Table 5.17: *Dielectric constant for the material proposed as solid-gap resonators.*

5.3 Summary

Devices operating at resonance frequencies in the VHF range have been the core of this chapter. microresonators have been divided according to their fabrication process (hybrid or monolithic approach). The chapter started showing the air-gap resonators fabricated in SCS; a summary of the most relevant results is shown in table 5.16; among the demonstrated devices are the LBAR, square and circle shaped resonators.

For the solid-gap resonators, different recipes were developed in order to deposit the gap material, problems related with the technological process limited the electrical characterization. Table 5.17 summarizes the dielectric constant for the material proposed for the transducer gap.

Finally, operating devices for different technological approaches by using the standard AMS-$0.35\mu m$ CMOS layers, like the in-plane MET4 and POLY1-POLY2 resonators and vertical MET1-POLY1 and POLY2-POLY1 have been demonstrated. Among all those alternatives, the POLY1-POLY2 approach for fabricating in-plane resonators is the most promising alternative for monolithically integrated micro resonators in the VHF range. Table 5.18 summarizes and compares the results achieved for the monolithic devices.

Tech. Approach	Device	Dimensions	f_0 (MHz)	Q-factor Air	Q-factor $Vacuum$	$Q \times f_0$ (Hz) Air	$Q \times f_0$ (Hz) $Vacuum$
MET4	c-c beam	$L = 10\mu m$ $b = 1.1\mu m$ $s = 650nm$	$f_0 = 60.4$	3^* $30^\dagger$			
M1-P1	paddle	$a_1 = 5\mu m$ $l = 5\mu m$ $s_v = 600nm$ $b_2 = 0.8\mu m$ $b_1 = 4.5\mu m$ $a_2 = 4\mu m$	$f_{0-tra} = 11.4$ $f_{0-tor} = 20.1$				
P2-P1	paddle	$a_1 = 3\mu m$ $l = 3\mu m$ $a_2 = 3\mu m$ $b = 1\mu m$ $s_v = 40nm$	$f_{0-tor} = 96.7$				
P2-P1	c-c beam	$L = 4\mu m$ $b = 550nm$ $s_v = 40nm$	$f_0 = 192$	$300^\dagger$	$1000^\dagger$	$6 \cdot 10^{10}$	$2 \cdot 10^{11}$
P1-P2	c-c beam	$L = 4\mu m$ $b = 700nm$ $s_v = 40nm$	$f_0 = 290.5$	$1000^\dagger$	$3000^\dagger$	$3 \cdot 10^{11}$	$10 \cdot 10^{12}$

Table 5.18: *Summary for the integrated resonators in the AMS-0.35μm technology.* * *refers to devices without integrated readout circuitry;* † *refers to devices with integrated readout circuitry.*

CHAPTER 6

Results on RF-MEMS in the UHF band

The chapter describes the design and characterization of microresonators that present resonance frequencies in the UHF range, ($300MHz$-$3GHz$). The microresonators have been fabricated by the hybrid and monolithic approaches described in previous chapters 3 and 4. From the application point of view, the design and fabrication of microresonators in that frequency range is pursued due to their direct application in a front end transceiver whether as the mixer used to downconvert the RF frequencies or as local oscillator.

For designing resonating devices above the UHF range frequency, flexural modes are not suitable at all, because of having small coupling gap areas and low Q-factors. In that case, the design has to be focused to bulk resonance modes, that exhibit higher resonance frequencies than flexural resonators for the same characteristic dimensions.

6.1 Hydrid resonators in the UHF range

The fabrication process depicted in chapter 3 has the purpose of achieving SCS high frequency microresonators with gap distances below $100nm$. Designs of high frequency resonators, based on disks, squares and elliptic shaped resonators pointing out to frequencies in the UHF range, were introduced in the mask layout. Best results were obtained on the elliptical shaped resonator. In the next section the design and characterization of that resonator are reported.

6.1.1 The elliptical resonator

An elliptical shape resonator was included in the design of microresonators fabricated by the hybrid approach whose process sequence was presented in a previous chapter 3. The objective of the elliptical shape resonator design was to compare the performance with the disk shaped in terms of electrical response in the target frequency.

Design

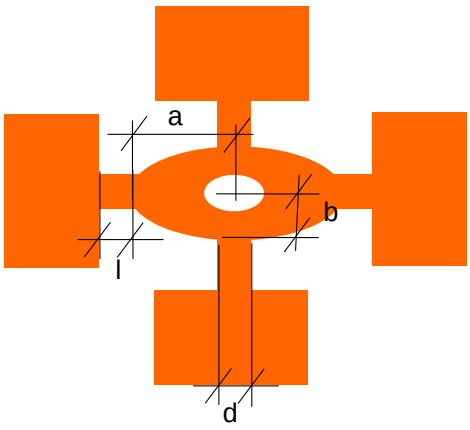
A scheme of an elliptical microresonator is depicted in figure 6.1(a). The ellipse is characterized by its minor and major axis and the length and width of the supporting beams. The ellipse is performed with a $(2 \times 2)\mu m^2$ hole in order to facilitate its releasing. All the dimensions of the designed elliptical resonator are depicted in table 6.1.

Analytic expressions for the resonance frequencies of bulk acoustic modes for an ellipse has not found in literature, so the frequency response of such a resonator has been calculated by a FEM tool. The design target frequency for the device is chosen to be $450MHz$.

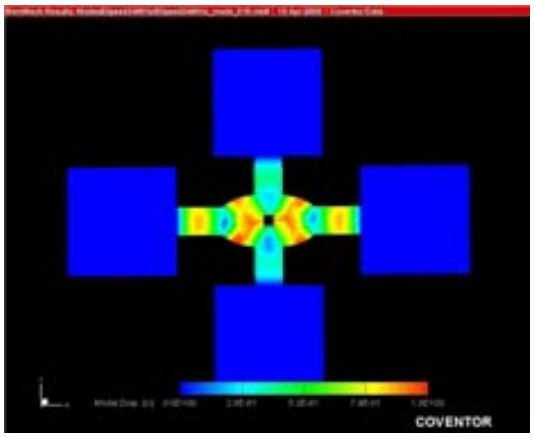
In order to achieve the correct dimensions, some simulations have been performed. The starting point was the known case of the disk. Figure 6.1(b) shows the first bulk radial acoustic mode; the simulated resonance frequency is $450MHz$ showing an effective mass of $1.38pg$.

Dimension	Value
a	$10.20\mu m$
b	$5\mu m$
d	$5\mu m$
l	$7\mu m$

Table 6.1: *Dimensions of the designed elliptical resonator.*



(a) Scheme of the elliptical shaped resonator



(b) Elliptical resonator in its first radial bulk acoustic mode. The simulated resonance frequency is $450MHz$ for the dimensions of table 6.1

Figure 6.1: *Elliptical shaped resonator showing their characteristic dimensions and its bulk radial resonance mode simulated with Coventor.*

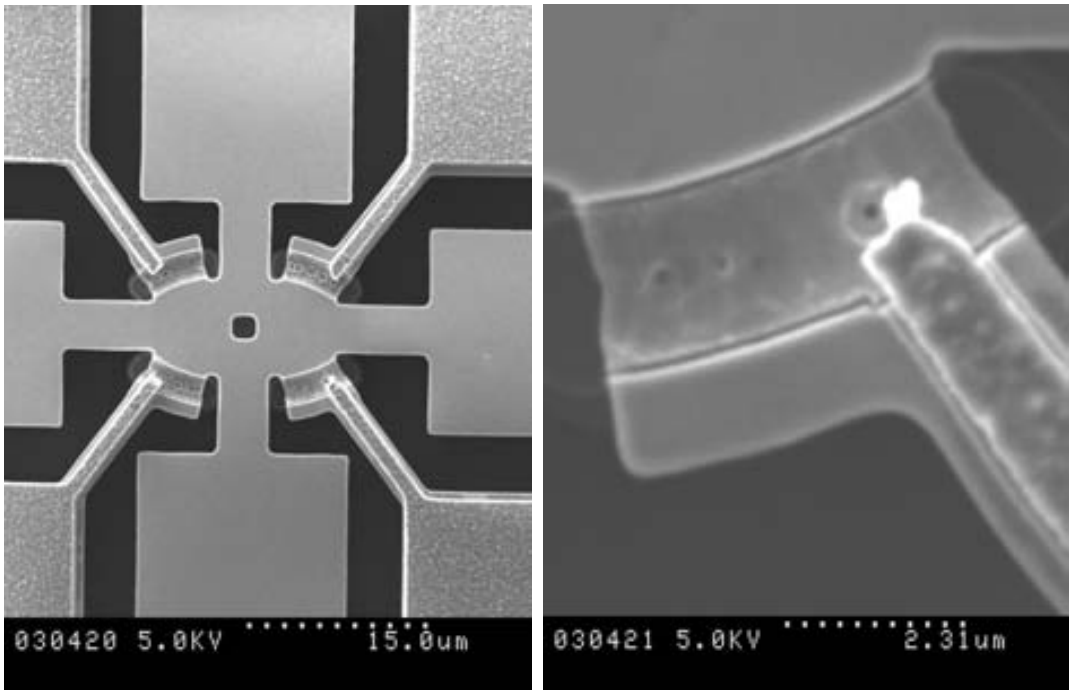
Structural characterization

The fabricated device is characterized by optical inspection by means of a SEM microscope. The most sensitive part of the device is the gap region, where planar and vertical sidewalls are desired in order to obtain a good performance of the device. Figure 6.2 shows a SEM image of a fabricated elliptical resonator. Measured dimensions are in concordance with the design values.

Electrical characterization

The electrical characterization of this device is obtained by the one-port measurement. This resonator is characterized to have only two terminals, resonator and the fourth electrodes connected at the same terminal. Then, the measurement consisted on applying a AC+DC voltages on the resonator and measuring the electrical current on the electrodes.

The result of the measurement is depicted in figure 6.3. The measurement was performed in air and the voltage applied was $30V$. The amplitude resonance peak is measured, showing good correlation between simulated and measured resonance frequencies. The amplitude of the peak is related with the non-optimal transduction in the resonator, which has to be



(a) SEM image showing the elliptical resonator designed in section 6.1.1

(b) Gap region of the elliptical resonator

Figure 6.2: *Physical characterization of the fabricated device.*

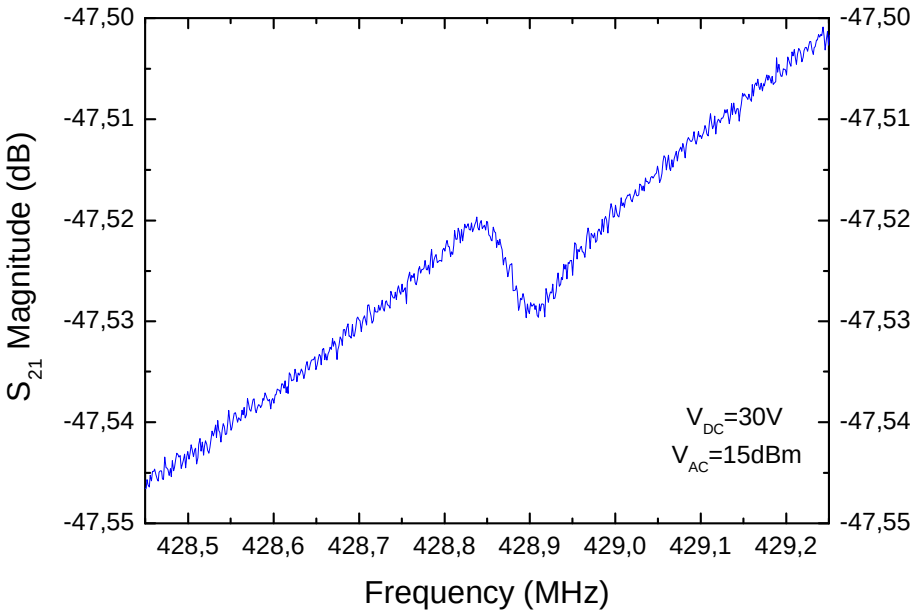


Figure 6.3: *Electrical characterization of the elliptical resonator.*

related to the gap region. The non-uniformity of the gap, may be with subproducts of the chemical reaction, together with non-vertical sidewalls might be the reason for this low signal.

6.2 Monolithic resonators in the UHF range

In previous chapter 4, technological approaches using the standard layers of the AMS-0.35μm technology were introduced as well as how to design flexural resonators, like c-c beams and paddles, by those approaches. Then, it was concluded that the best approach for high frequencies was the lateral POLY1-POLY2 approach, that takes advantage of the 40nm-thick oxide to delimitate the transducer gaps. In this section it will be shown that, with the same philosophy, this approach can be used to implement bulk acoustic resonators. Specifically, the bulk acoustic resonators that have been tested successfully corresponds to a longitudinal bulk acoustic resonator (LBAR) and to a ring annular shaped resonator (RBAR).

6.2.1 The Longitudinal Bulk Acoustic Resonator

The longitudinal bulk acoustic resonator represents one of the most typical devices which has been studied as bulk acoustic microresonator. In this section, the design, the structural and electrical characterization will be shown.

Design

The technological approach used for designing the LBAR device is based on the POLY1-POLY2 approach. The POLY1 and POLY2 layers are chosen to be the resonator and electrodes structural material, respectively. In the layout, both layers are drawn at $0nm$ gap in order to achieve a symmetrical gap distance on both sides.

The frequency of a LBAR microresonator in its first bulk acoustic mode is found when the quarter of the acoustic wavelength corresponds to the length of the arm. The equation for the frequency, then is given by:

$$f_{LBAR} = \frac{1}{4L} \cdot \sqrt{\frac{E}{\rho}} \tag{6.1}$$

The target resonance frequency for this resonator was $400MHz$. With the Young's modulus derived in previous chapter 5, the arm length of the LBAR that corresponds to that frequency is $4\mu m$. In figure 6.4 is depicted an scheme of the layout drawn for fabricating this device, and in table 6.2 are shown the dimensions.

In order to increase the capacitive coupling, the arm width is widen at the free end, giving the so called eared-LBAR. The width of each arm is $500nm$ and at the free end the width increases up to $1\mu m$. In order to investigate which are the consequences of the addition of the 'ears' to the resonator a simulation in the FEM tool Coventor was performed.

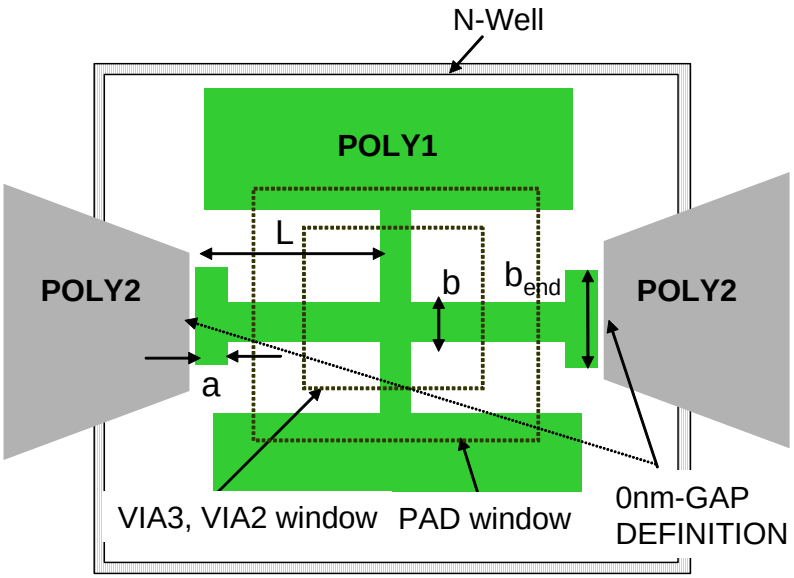
The results of the simulation are shown in figure 6.4(b). In appearance, the simulated resonance mode corresponds to the bulk acoustic mode; however, the resonance frequency has decreased below the expected value ($400MHz$) down to $361.9MHz$. Then, this solution to increase the coupling area introduces a change in the analytically found resonance frequency, that has to be considered in the design.

Structural characterization

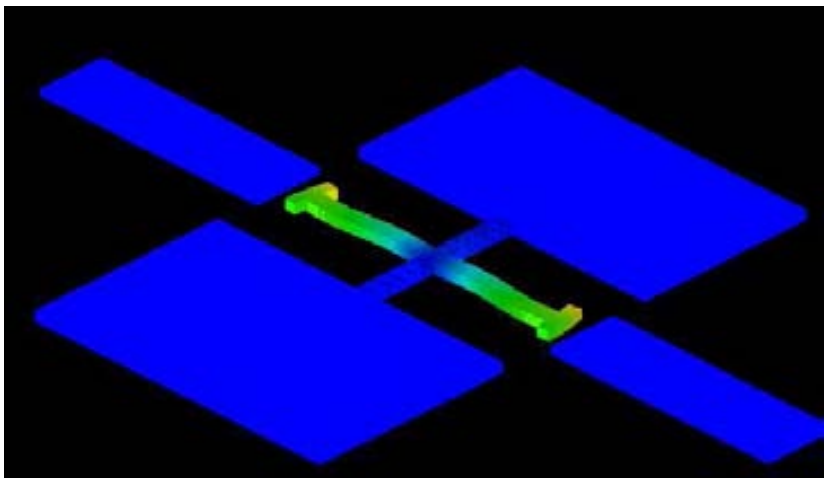
Figure 6.5 shows a SEM picture of a fabricated device. In the inset of the figure, it can be observed that the POLY2 (electrode material) tends to overlay the resonator; this same effect

Dimension	Value
L	$4\mu m$
a	$350nm$
b	$650nm$
b_{end}	$1\mu m$

Table 6.2: *Dimensions of the LBAR device implemented in the POLY1-POLY2 approach.*



(a) Layout for the LBAR device implemented in the POLY1-POLY2 approach



(b) Simulated bulk acoustic mode

Figure 6.4: *LBAR fabricated by the POLY1-POLY2 technological approach, showing the layout and the simulation of the first bulk acoustic mode.*

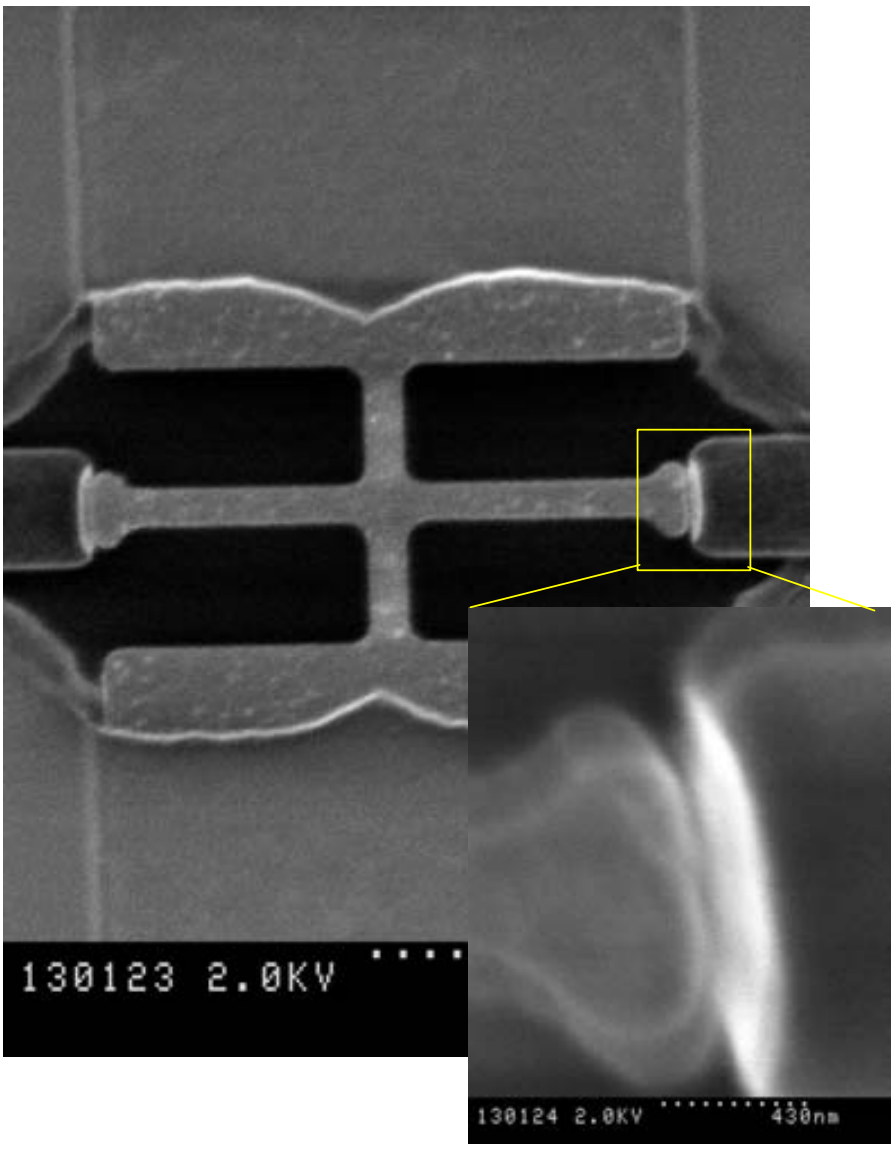


Figure 6.5: *SEM image of a LBAR fabricated by the POLY1-POLY2 approach. The length of the arm is* $L = 4\mu m$ *and the width is* $500nm$.

was observed in previous chapter when fabricating the c-c beams.

Alhtough the gap distances seem to be asymmetrical by the top view image (figure 6.5), it was demonstrated in last chapter that in the cross section the lateral gaps were perfectly defined to $40nm$. However, the resolution of the process limits the shape of the ears of the resonator. The free ends are drawn rectangular, but the fabricated shape presents a rounded free ends.

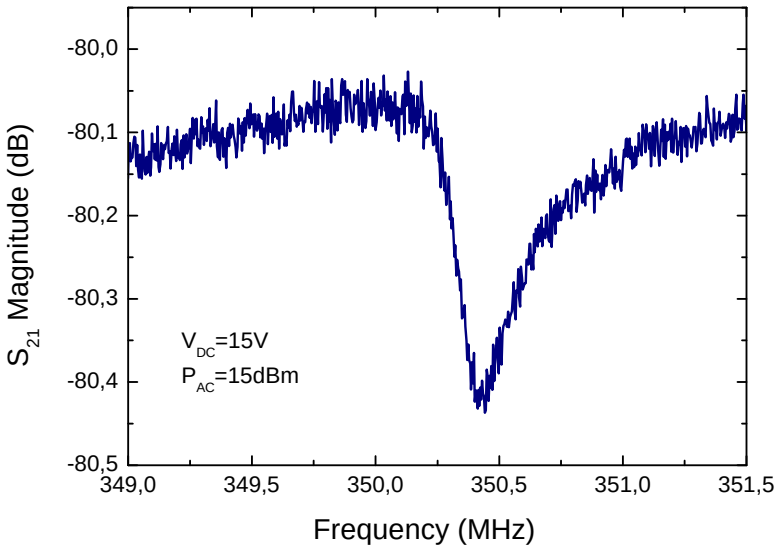


Figure 6.6: *Air measurement of a LBAR device like the one shown in figure 6.5.*

Electrical characterization

The LBAR resonator has typically only two terminals, so in most of the cases the electrical characterization is obtained by one-port measurement. The result of the characterization in air is shown in figure 6.6. The transmission spectrum near resonance presents a resonance peak at $350MHz$. However, the resonance curve does not present a peak, just the anti-resonance peak. This is due to the high component of the parasitic current that screens the resonance current.

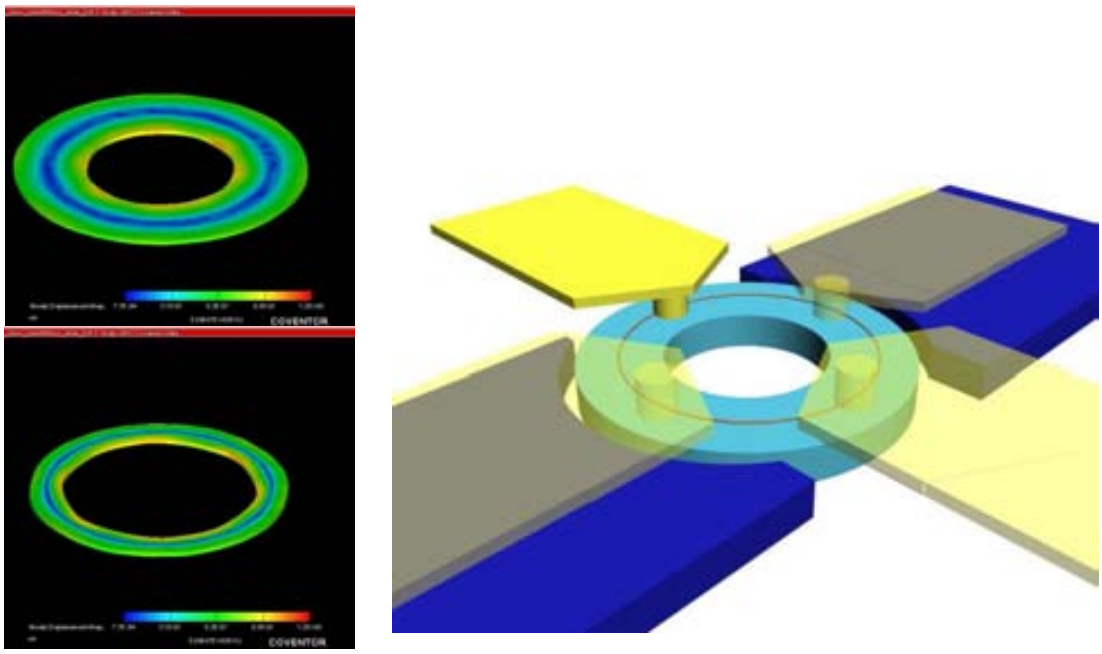
On that case, a DC voltage applied of $15V$ and a AC power of $15dBm$ in ambient conditions were applied to the resonator.

6.2.2 The annular ring

The LBAR resonator presents some limitations when increasing the target resonance frequency. One of this limitations comes from the fact that when increasing the resonance frequency the equivalent stiffness of the LBAR increases, the movement is smaller and the electrical signal becomes undetectable. In front of this situation, the ring shaped resonator presents more coupling area that increases the resonance current.

Design

An annular ring shaped resonator is chosen in order to achieve the target frequency of $1GHz$. The main advantage of choosing a ring shaped resonator is the absence of a trade-off between the coupling area and the high target frequency, because the resonance frequency of a ring



(a) First bulk acoustic mode for the RBAR

(b) Scheme of the polysilicon ring vertically anchored by metallic anchors at nodal line of the first resonant mode

Figure 6.7: *Ring Bulk Acoustic Resonator, showing the first bulk acoustic mode and the anchoring point.*

depends on the width, i.e $r_o - r_i$, but not in the absolute radius value as in a disk. For example, in the case of a resonating disk, a diameter of only $5\mu m$ is mandatory to achieve a resonating structure of $1GHz$ in its first bulk acoustic mode, limiting the coupling area with the electrodes and thus, lowering the resonance current. However, choosing the annular ring as resonating structure allows the compatibility of high resonance frequency with high coupling area, as recently published [82].

The inner diameter chosen was $10\mu m$, and solving equation 2.81 by numerical methods for the $f_0 = 1GHz$ target frequency, considering $E = 110GPa$ and $\sigma = 0.2$, the outer radius was $17.32\mu m$. The bulk acoustic mode was simulated by COVENTOR , obtaining the resonance mode depicted in figure 6.7(a). In table 6.3 are depicted the dimensions of the ring resonator, as well as the expected and measured resonance frequency.

The bulk resonance mode consists on the expansion and compression of the outer and inner surfaces of the ring whereas the center of the ring remains immovable defining a nodal line. For this reason, and in order to minimize the losses by the anchors, the structure is suspended and anchored vertically by 4 points of the nodal line, as shown in 6.7(b).

Furthermore, if the structure is anchored by a different material than the structural material

of the resonator, then losses are again minimized. This fact is due to the reflection of the transmitted wave produced between two different media. In our design, the structural material of the resonator is polysilicon whereas the material used for supporting the ring at nodal points is the metal of the CMOS technology, aluminum.

A way of quantifying the transmitted energy at the anchors can be done by expressing the reflection coefficient in terms of the resonator and stem material acoustic impedances. In this case, for standard values of both materials, the transmission coefficient is 0.9, giving a 90% of the transmitted wave energy, reducing anchor losses only a 10%, relative to the case of having anchors and resonators made of the same material.

The ring bulk acoustic resonator has been fabricated by the POLY1-POLY2 approach. Figure 6.8(a) shows the layout drawn that corresponds to the fabricated device. The resonator is defined by the layer POLY1 and electrodes by layer POLY2. The structure is vertically anchored by the aluminum of MET1 layer, as shows figure 6.8(b). The annular ring of $8.6\mu m$ of outer radius is supported by a metal vias in the nodal points of the structure, minimizing the anchor losses.

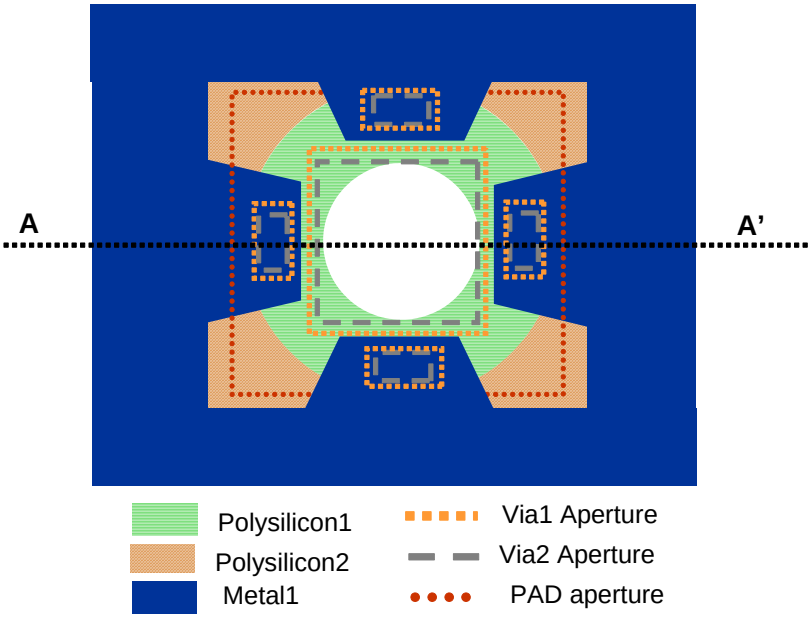
In order to reduce the post-CMOS process time, necessary to release the structure, a set of via layers are drawn in order to remove the oxide layers IMD2 and IMD3 oxides, thus activating the releasing of the resonator in the wet etch solution. In order to protect the POLY1 layer from posterior CMOS processes, IMD1 oxide is not removed by drawing VIA1 aperture. Field oxide (FOX), inter poly-metal oxide (ILDFOX), inter-metal oxide (IMD1) and the inter-polysilicon oxide are the sacrificial layers. Once all those oxides are etched the structure is released.

Structural characterization

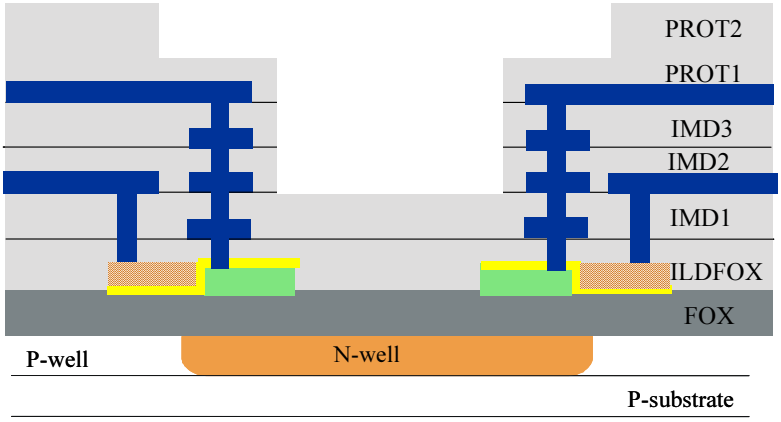
Figure 6.9 shows a SEM image of the annular ring shaped transducer after releasing. The wet-etching time necessary for the releasing was $18 + 10min$ in the HF-based solution. The resonator area is defined by the pad aperture, designed to remove the passivation layer and enabling the releasing process. The resonator is anchored by the MET1 and MET2 metal

Dimension	Value
r_i	$5\mu m$
r_o	$8.6\mu m$
f_{0-theo}	$1GHz$
f_{0-meas}	$1.04GHz$

Table 6.3: *Dimensions of the RBAR device showing the expected and measured resonance frequency.*



(a) Layout of the poly1-poly2 ring



(b) Cross section scheme of the released MEMS. The profile is made through the ring, from one anchor to the other, following the dotted line of figure 6.8(a)

Figure 6.8: *Layout and cross section scheme of the ring resonator fabricated in AMS-0.35μm.*

layers at four points of the structure, that coincides with the nodal line of the first bulk vibrating mode of the ring resonator, in order to minimize losses due to the anchoring. The resonator size is $r_i = 5\mu m$, $r_o = 8.6\mu m$. A gap of $40nm$ is measured between electrode and resonator, as can be seen in figure 6.9(b).

Electrical characterization

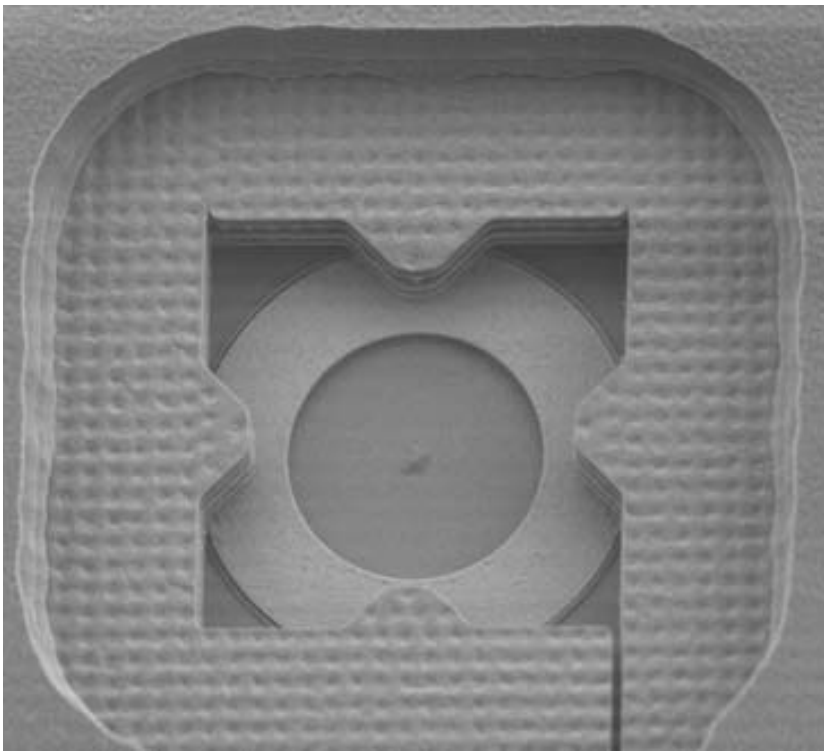
The resonator is designed in order to be excited electrostatically in a two-port configuration. By this configuration, the DC and AC voltages applied to the structures are applied separately. A DC voltage is applied directly to the annular ring and the electromechanical current produced by the movement of the resonator is collected in the read-out electrode.

Figure 6.10 shows the measured transmission spectrum S_{21}, (magnitude and phase) for $10VDC$ polarization voltage of the ring. It can be observed the transmission at $1.04GHz$, in accordance with the expected values provided by the numerical solution of equation 2.81 and with Coventor simulations. The anharmonic behavior of the curve shown in figure 6.10 is suspected to be due to the high AC signal applied, $P_{AC} = 15dBm$. The height of the peak is a little above $3dB$, so allows to extract the electrical Q factor from the measurement. The extracted Q factor in air is 400. An improvement of the electrical signal is expected when implementing monolithically a CMOS amplifier in order to condition the readout signal.

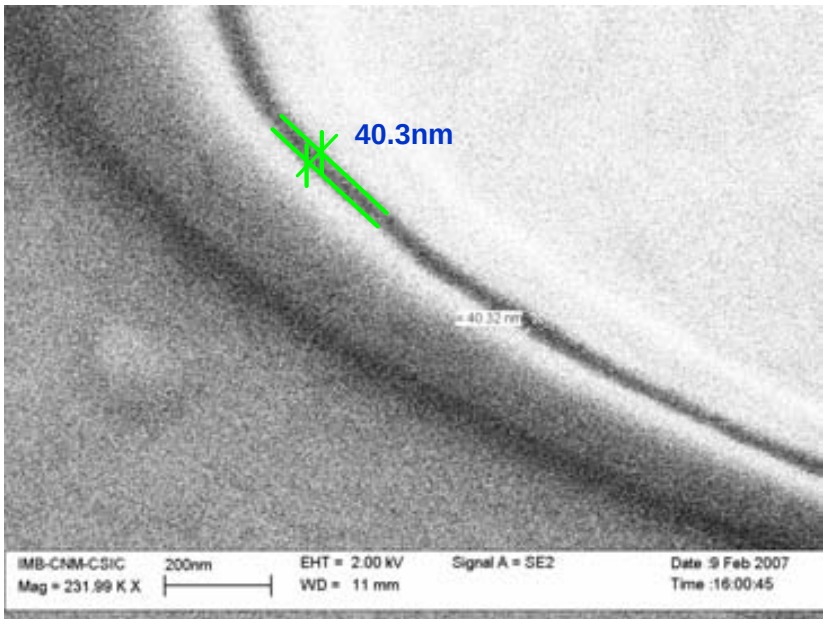
Although this last result at $1GHz$ corresponds to the first annular ring integrated in AMS-0.35, and consequently it is in some sense a preliminary result; it will allows us to estimate a figure of merit of $Q \times f_{res}$ bigger than $400 \times 1GHz$, which, up to now, defines a milestone on the state of the art of UHF monolithically integrated MEMS resonators.

6.3 Summary

In this chapter have been presented microresonators exhibiting bulk resonance frequencies in the UHF range have been presented. For the elliptical resonator fabricated by the hybrid approach it has been measured the resonance frequency, but still more effort in the fabrication process is needed in order to improve the capacitive transduction. Two different bulk acoustic resonators monolithically integrated have been fabricated and tested by the POLY1-POLY2 approach, taking advantage of the $40nm$ spacing between electrode and driver. For the LBAR, a resonance frequency of $360MHz$ has been measured in a one-port configuration technique. However, the most promising device operating in the UHF range, corresponds to the RBAR, that in preliminary test exhibits a resonance frequency of $1.04GHz$ and a Q factor in air of 400. This results defines a milestone on the state of the art of UHF monolithically integrated MEMS resonators. In table 6.4 are summarized all the characterized devices in the UHF range.



(a) SEM image of the annular ring shaped resonator



(b) Detail of the gap region, showing the 40nm distance

Figure 6.9: *SEM image of the Ring Bulk Acoustic Resonator, and a detail of the gap region.*

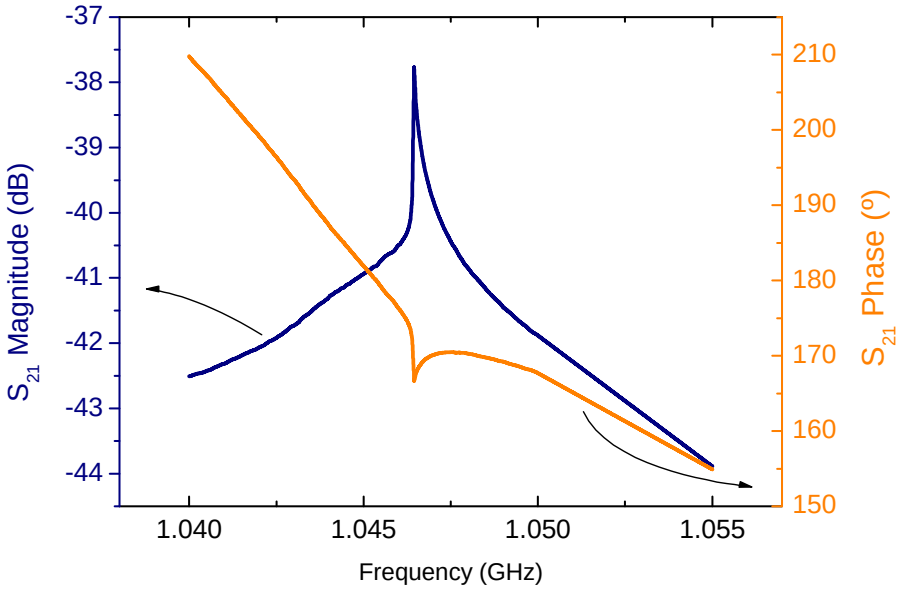


Figure 6.10: *Two-port transmission measurement (S21) near resonance; a DC voltage of* $10V$ *is applied directly to the annular ring and* $15dBm$ *to the input electrode.*

Structure	Fab. Process	Dimensions	f_0	Q_{air}	$f_{res} \times Q_{air}$
Ellipse	Hybrid	$a = 10.2\mu m$	$428.8MHz$		
		$a = 5\mu m$			
LBAR	CMOS-MEMS	$L = 4\mu m$	$350.2MHz$		
	POLY1-POLY2	$b = 650nm$			
RBAR	CMOS-MEMS	$r_i = 5\mu m$	$1.04GHz$	400	$4 \cdot 10^{11}Hz$
	POLY1-POLY2	$r_i = 8.6\mu m$			

Table 6.4: *Summary for the resonators measured in the UHF range.*

Conclusions

This phd thesis has been mainly focused on the fabrication of RF CMOS-MEMS resonators in a commercial CMOS $0.35\mu m$ technology by using its available standard layers, leaving the maskless post-CMOS process for only releasing the resonators.

In the first chapter, the most relevant parameters related with the RF MEMS were identified and presented. A summary of the most important technological processes, including hybrid and monolithical fabrication approaches, were described. The implementation of a super-hetorodyne architecture by using such resonators showing the advantages in terms of cost and size, as well as the present and future market for RF MEMS devices was also analyzed.

An non-linear electromechanical model, based on the real deflection profile of the resonators for accurately computing the transduction capacitance variation, has been implemented in Matlab and in the electrical simulation environment of SPICE. The basis for extending the model to bulk acoustic resonators has been described. Furthermore, a set of equations for designing different vibrating structures has been presented.

For resonators under the hybrid approach, a technological process for fabricating devices in Single Crystal Silicon (SCS) with lateral gaps distances below $100nm$ has been developed. A technological approach in order to explore the transduction by a solid dielectric gap has also been developed. For monolithic resonators, an exhaustive study of the different technological approaches allowed by the commercial technology was presented. Among all different approaches studied, it has been demonstrated that the most relevant consisted on using two polysilicon layers separated by a thin silicon oxide layer available in the capacitance standard module of the technology. By a smart new design strategy, lateral in-plane resonators showing symmetrical gap distances of only $40nm$ have been demonstrated.

Preliminary results on the electrical test for bulk acoustic resonators in SCS designed by the hybrid approach have been presented. Devices showing frequencies up to $430MHz$ have been

demonstrated although related problems in the gap region are still to be solved.

The designed technological process for testing and studying the electrical transduction by means of a solid and dielectric gap has been carried out, and preliminary tests results involving the dielectric material characterization have been presented. The dielectric gap materials proposed were: silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum nitride (AlN) and carbonfluoroteflon (C_4F_8). For all the alternatives a deposition process was studied and developed, emphasizing the last two materials. For the most promising alternative, the aluminum nitride, more effort is necessary in order to solve the problems related with the electrodes material deposition, although a recipe for the deposition was established.

For the monolithic fabrication approach on polysilicon with $40nm$ lateral gap transduction, lateral clamped-clamped beams with integrated readout circuitry showing frequencies from $50MHz$ up to $420MHz$ have been demonstrated. The highest quality factor measured was 3000 in vacuum for a c-c beam resonating at $280MHz$. Then, the highest quality factor per resonance frequency measured was $3000 \times 290MHz1 \simeq 9 \cdot 10^{11}Hz$. The same lateral polysilicon approach has been applied to design bulk resonant structures showing higher frequencies, like longitudinal bulk acoustic cantilevers and annular rings. The highest measured frequency was $1.04GHz$ for an annular ring in air, showing a quality factor of 400. The measured figure of merit $Q \times f$ at $1GHz$ was $4 \cdot 10^{11}Hz$.

Finally, the integration of lateral flexural resonating structures as well as bulk acoustic resonators in a commercial and standard CMOS technology, showing symmetrical transducing gap distances of only $40nm$ has been achieved. Operating devices showing a high reliability have been demonstrated based on a simple and maskless post-CMOS process. Tested resonators exhibited frequencies in the VHF and UHF range, establishing the basis for future monolithically integration of oscillators as well as filters or mixers in a new generation of front-end transceivers based on RF-MEMS devices.

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Abbreviations and Acronyms

ABM	Analog Building Blocks
AFM	Atomic Force Microscopy
AMS	Austria Micro Systems
AOE	Advance Oxide Etcher
ASE	Advance Silicon Etcher
BAW	Bulk Acoustic Wave
BHF	Buffered Hydrofluoric Acid
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BOX	Buried Oxide Layer
CMOS	Complemetary Metal Oxide Semiconductor
DLBAR	Double Longitudinal Extensional Bulk Acoustic Resonator
DLP	Digital Light Processor
DRIE	Deep Reactive Ion Etching
EBL	Electron Beam Lithography
FBAR	Film Bulk Acoustic Resonator
FEM	Finite Element Method
FIB	Focused Ion Beam

GaAs	Galium Arsenide
HARPSS	High Aspect-Ratio Combined Poly and Single-Crystal Silicon MEMS Technology
HF	Hydrofluoric Acid
HTO	High Temperature Oxide
IC	Integrated circuits
IMEC	Inter-universitary of Micro Electronics Centre
LBAR	Longitudinal Extensional Bulk Acoustic Resonator
LNA	Low Noise Amplifier
LPCVD	Low Pressure Chemical Vapour Deposition
MEMS	Micro Electro Mechanical Systems
MIC	MicroElectronic Centre
PECVD	Plasma Enhanced Chemical Vapor Deposition
PLL	Phase Locked Loop
RBAR	Ring Shaped Bulk Acoustic Resonator
RDM	Radial Disk Bulk Acoustic Mode
RF	Radio Frequency
RF-MEMS	Radio Frequency Micro Electro Mechanical Systems
RIBE	Reactive Ion Beam Etch
RIE	Reactive Ion Etching
SAW	Surface Acoustic Wave
SBAR	Square Shaped Bulk Acoustic Resonator
SCS	Single Crystal Silicon
SEM	Scanning Electron Microscopy
SiC	Silicon Carbide
SoC	Systems On Chip
SOI	Silicon On-Insulator

SSoC Sensing Systems On Chip

SSPA Solid State Power Amplifier

TED ThermoElastic Damping

TEOS TetraEthyl OrthoSilane

TIA TransImpedance Amplifier

UHF Ultra High Frequency

VHF Very High Frequency

WGDM Wine-Glass Disk Bulk Acoustic Mode

APPENDIX A

Technologycal Processes

The technological processes carried out for the solid-gap microresonantors fabrication, are described in this appendix. Specifically, processes for the fabrication process including SiO_2, Si_3N_4 and AlN as gap materials are depicted. Furthermore, the sequence for fabricating test wafers is also depicted, as well as the two options, corresponding to the addition of a SiO_2 layer on top of the resonators or not, for fabricating device wafers.

DEVICE WAFERS WITHOUT A SiO_2 LAYER ON TOP

Step	Equipment	Process	Recipe	Experimental Data
1	Furnace: PhosphorDriveIn	Si Thermal Oxidation	WETN4, T=1050°C, time=10h	
2	LCVD Furnace: Polysilicon	Polysilicon Deposition	Poly620, $T = 620°C$, $time = 3h40min$	Expected thickness=2.5μm
3	RIE1	Poly etch	Recipe zdaniso	Dektak measurement, Thickness=2.6μm
4	Furnace: Phos.PreDep	PolySi doping	WETN4, T=1000°C t=1h	
5	Furnace: Phos.DriveIn	PolySi doping	WETN4, T=1000°C t=5min+ 3h	$\rho = 0.7 \times 10^{-3}\Omega cm$
6	HMDS Oven	Surface preparation for photolitography	Recipe 4	
7	Track1 AZ5214E	Photoresist spinning and baking	$pr1\_5$	
8	KS Aligner	Mask1 exposure	8.5s exposure HARD contact	
9	Developer	Mask1 developing	New developer 60s	
10	RIE2	Polysilicon dry etching	jt_aniso t=10min	

Table A.1: *Technological process sequence for the fabrication of device wafers without SiO_2 layer on top.*

DEVICE WAFERS WITHOUT A SiO_2 LAYER ON TOP

Step	Equipment	Process	Recipe	Experimental Data
1	Furnace: PhosphorDriveIn	Si Thermal Oxidation	WETN4, T=1050°C, time=10h	
2	LCVD Furnace: Polysilicon	Polysilicon Deposition	Poly620, $T = 620°C$, $time = 3h40min$	Expected thickness=2.5μm
3	RIE1	Poly etch	Recipe zdaniso	Dektak measurement, Thickness=2.6μm
4	Furnace: Phos.PreDep	PolySi doping	WETN4, T=1000°C t=1h	
5	Furnace: Phos.DriveIn	PolySi doping	WETN4, T=1000°C t=5min+ 3h	$\rho = 0.7 \times 10^{-3}\Omega cm$
6	HMDS Oven	Surface preparation for photolitography	Recipe 4	
7	Track1 AZ5214E	Photoresist spinning and baking	$pr1\_5$	
8	KS Aligner	Mask1 exposure	8.5s exposure HARD contact	
9	Developer	Mask1 developing	New developer 60s	
10	RIE2	Polysilicon dry etching	jt_aniso t=10min	

Table A.2: *Technological process sequence for the fabrication of device wafers without SiO_2 layer on top.*

PROCESS SEQUENCE FOR Si_3N_4 NANOMETRIC SOLID GAP

Step	Equipment	Process	Recipe	Experimental Data
1	Furnace:PhosphorDriveIn	Si Thermal Oxidation	WETN4, T=1050°C, t=10h	
2	LCVD Poly	Poly Deposition	Poly620, $T = 620°C$, $3h40min$	Expected, 2.5μm
3	RIE1	Poly etch	Recipe, zdaniso	Dektak meas. 2.6μm
4	LPCVD Furnace: TEOS Oxide	SiO_2 Deposition	Recipe, $t = 40min$	Dektak measurement, Thickness=500nm
6	HMDS Oven	Surface preparation for photolitography	Recipe 4	
7	Track1 AZ5214E	Photoresist spinning and baking	$pr1\_5$	
8	KS Aligner	Mask1 exposure	8, 5s exposure, HARD	
9	Developer	Mask1 dev.	New developer, 60s	
10	AOE	SiO_2, dry etching	Base2a, t=2min	
11	RIE2	Polysilicon dry etching	jt_aniso, t=6min	
12	RCA Cleaning	Wafer cleaning		
13	LPCVD Furnace: SiliconNitride	Si_3N_4 as gap material	Dry, T=900°C time=4min	Filmtek mesurement Thickness=20nm
14	LCVD Furnace: Polysilicon	Polysilicon Deposition	Poly620, $T = 620°C$, $time = 3h40min$	Expected thickness=2.5μm
15	Track1, AZ5214E	Photoresist spin. and baking	$pr1\_5$	
16	KS Aligner	Mask1 exposure	8.5s exposure, HARD	
17	Developer	Mask1 developing	New developer, 60s	
18	RIE2	Polysilicon dry etching	jt_aniso, t=12min	

Table A.3: *Technological process sequence for the fabrication of microresonators with Si_3N_4 nanometric solid gap. The deposited thickness is* 50nm. *The wafer that followed this technological process was* r_03_2.

PROCESS SEQUENCE FOR SiO_2 NANOMETRIC SOLID GAP

Step	Equipment	Process	Recipe	Experimental Data
1	Furnace:	Si Thermal Oxidation	WETN4, T=1050°C, t=10h	
2	LCVD: Poly	Polysilicon Deposition	Poly620, $T = 620°C$, $t = 3h40min$	Expected, $2.5\mu m$
3	RIE1	Poly etch	Recipe, zdaniso	Dektak meas.,$2.6\mu m$
4	LPCVD: TEOS Oxide	SiO_2 Deposition	Recipe, TEOSPNE, $t = 40min$	Dektak meas.$500nm$
5	HMDS Oven	Surface preparation	Recipe 4,	
6	Track1 AZ5214E	Photoresist spinning and baking	$pr1\_5$	
7	KS Aligner	Mask1 exposure	8.5s, HARD	
8	Developer	Mask1 developing	New developer, $60s$	
9	AOE	SiO_2 dry etching	Base2a, t = 2min	
10	RIE2	Polysilicon dry etching	jt_aniso, $t = 6min$	
11	RCA Cleaning	Wafer cleaning		
12	Furnace: PhosphorDriveIn	Si Dry Oxidation for gap spacing	Dry, T=900°C, time=10min+20min	Filmtek mesurement Thickness=$8nm$
13	Furnace: PhosphorDriveIn	Si Dry Oxidation for gap spacing	Dry, T=1000°C, time=10min+20min	Filmtek mesurement Thickness=$28nm$
14	LCVD Furnace: Polysilicon	Polysilicon Deposition	Poly620, $T = 620°C$, $time = 3h40min$	Expected thickness=$2.5\mu m$
15	Track1 AZ5214E	Photoresist spinning and baking	$pr1\_5$	
16	KS Aligner	Mask1 exposure	8.5s, HARD	
17	Developer	Mask1 developing	New developer,60s	
18	RIE2	Polysilicon dry etching	jt_aniso, t=10min	

Table A.4: *Technological process sequence for the fabrication of microresonators with SiO_2 nanometric solid gap. The estimated gap thickness is $8nm + 28nm$. The wafer that followed this technological process was r_03_4.*

PROCESS SEQUENCE FOR Al TEST WAFERS FABRICATION				
Step	Equipment	Process	Recipe	Experimental Data
1	Furnace: PhosphorDriveIn	Si Thermal Oxidation	WETN4, T=1050^oC, time=3h20min	Deektak measurement=1μm
2	Track1 AZ5214E	Photoresist spinning and baking	$pr1\_5$	
3	KS Aligner	Mask1 exposure	4s exposure HARD contact	
4	Track2	Photoresist Baking	REV120 $t = 2min$, $T = 120^oC$	
5	KS Aligner	No mask	30s exposure HARD contact	
6	Developer	Developing	New developer 60s	
7	Alcatel	Aluminum Sputtering	$Ti1Al3$ thickness=300nm	
8		Gap material deposition		
9	Alcatel	Aluminum Sputtering	$Ti1Al3$ thickness=300nm	
10	Track1 AZ5214E	Photoresist spinning and baking	$pr1_5$	
11	KS Aligner	Mask2 alignment exposure	8.5s exposure HARD contact	
12	Developer	Developing	New developer, 60s	
13	Aluminum Etcher	Aluminum Wet Etching	New developer 200s	

Table A.5: *Technological process sequence for Al test wafers fabrication.*

PROCESS SEQUENCE FOR *AlN* NANOMETRIC SOLID GAP				
Date	Equipment	Process	Recipe	Experimental Data
1	Furnace: PhosphorDriveIn	Si Thermal Oxidation	WETN4, T=1050^oC, time=10h	
2	LCVD Furnace: Polysilicon	Polysilicon Deposition	Poly620, $T = 620^oC$, $time = 3h40min$	Expected thickness=2.5μm
3	HMDS Oven	Surface preparation for photolitography	Recipe 4,	
4	Track1 AZ5214E	Photoresist spinning and baking	$pr1\_5$	
5	KS Aligner	Mask1 exposure	8.5s exposure HARD contact	
6	Developer	Mask1 dev.	New developer, 60s	
7	RIE2	Polysilicon dry etching	jt_aniso, t=6min	
	RCA Cleaning	Wafer cleaning		
8	Wondertec	AlN as gap material	P=$241 - 254W$, P=8μbar N_2/Ar time=10min	Deektak Meas. Thickness=45nm
9	Wondertec	Cr deposition as electrode material	thickness=40nm	
10	Wondertec	Au deposition as electrode material	thickness=3.5μm	
11	Wondertec	Au wet etching		
12	Wondertec	Cr wet etching		

Table A.6: *Technological process sequence for the fabrication of microresonators with AlN nanometric solid gap. The wafer that followed this technological process was r_06_6.*

Dry etching of the silicon dioxide, *Base2a* recipe	
Pressure (mTorr)	
Base Pressure =5	Pressure Tip=0.4
Gases (sccm)	
$He = 500$	$C_4F_8 = 25$
RF power, $13.56MHz$, W	
$Coil = 1100$	$Platen = 430$
Etching Rate	
$400nm/min$	

Table A.7: *Base2a recipe for dry etching of silicon dioxide in the Advance Silicon Etcher, AOE.*

Dry etching of the silicon, *jt_aniso* recipe	
Pressure (mTorr)	
Base Pressure =80	
Gases (sccm)	
$SF_6 = 32$	$O_2 = 8$
RF power, $13.56MHz$, W	
30	
Etching Rate	
$500nm/min$	

Table A.8: *jt_aniso, recipe for dry anisotropic etching of silicon in the RIE.*

Dry etching of the silicon dioxide, *jt_oxide* recipe	
Pressure (mTorr)	
Base Pressure =100	
Gases (sccm)	
$CF_4 = 16$	$CHF_3 = 24$
RF power, $13.56MHz$, W	
60	
Etching Rate	
$50nm/min$	

Table A.9: *jt_oxide, recipe for dry anisotropic etching of silicon dioxide in the RIE.*

Recipe for the deposition of Si_3N_4 by LPCVD, *nitride* recipe	
Pressure (mTorr)	
Pressure =250	
Temperature (°C)	
Temperature=800°C	
Gases (sccm)	
$DCS = 25$	$NH_3 = 75$
Deposition Rate	
$5nm/min$	

Table A.10: *Recipe for the deposition of Si_3N_4 by LPCVD.*

Recipe for the deposition of polysilicon by LPCVD, *poly620* recipe
Pressure (mTorr)
Pressure =250
Temperature (°C)
Temperature=620°C
Gases (sccm)
$SiH_4 = 80$
Deposition Rate
$10nm/min$

Table A.11: *Recipe for the deposition of polysilicon by LPCVD.*

Recipe for the deposition of TEOS by LPCVD, *teospne* recipe	
Pressure (mTorr)	
Pressure =150	
Temperature (°C)	
Temperature=725°C	
Gases (sccm)	
$TEOS = 50$	$O_2 = 30$
Deposition Rate	
$10nm/min$	

Table A.12: *Recipe for the deposition of TEOS by LPCVD.*

APPENDIX B

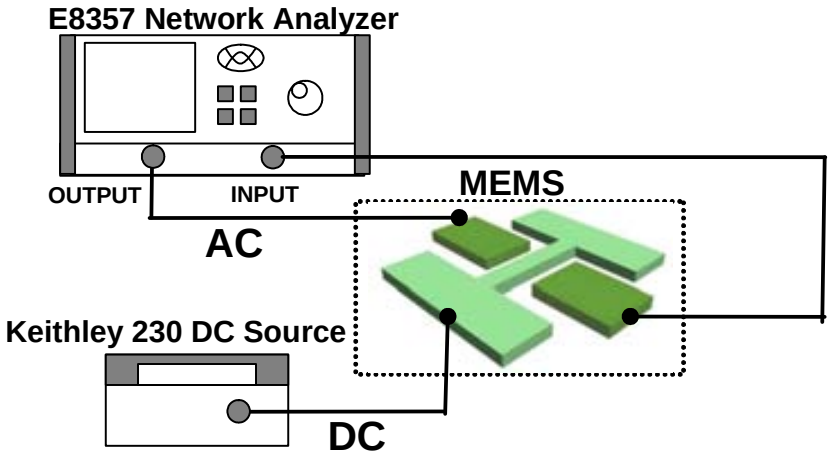
Measurement techniques

Electrical measurements have the finality of characterizing the electrical performance of the designed resonators. Quantities such as: resonance frequency, quality factor and transmission power have to be measured in order to have a fully characterized device.

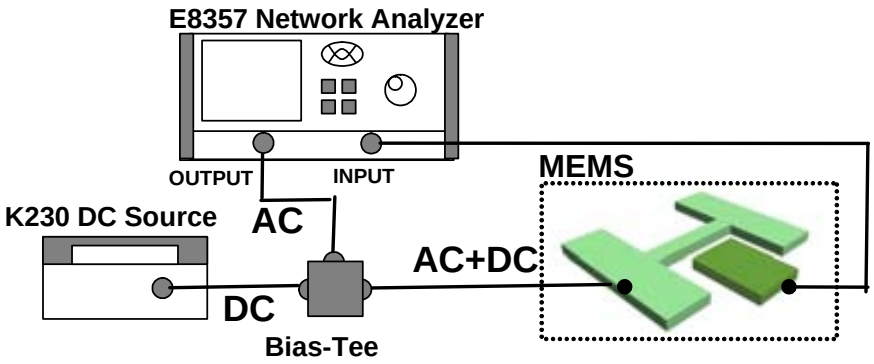
Electrical measurements based on measuring transmission curves or (S_{21} parameter) gives the electrical resonance frequency and a value of the quality factor (only if the resonance peak is above $3dB$). However, due to the influence of parasitic capacitances, sometimes is not possible to extract the value of the quality factor and a new experimental approach based on mixing properties of such resonators is employed in order to extract the quality factor as well as the mechanical resonance frequency.

For obtaining S_{21} transmission curves, two different configurations can be used. The first and simplest approach corresponds to the one-port measurement, as shows figure B.1(a), where the DC and AC signals are applied directly to the resonator port. On the other hand, in the two-port configuration only the DC signal is applied to the resonator whereas the AC signal is applied to another electrode. In this case, the parasitic capacitance is smaller that in the one-port measurement, obtaining a lower parasitic current. As can be seen in figure B.3 the parasitic capacitance for the one-port measurement is the capacitance C_2, whereas in the two-port measurement the parasitic capacitance is C_{12}, that corresponds to the fringing capacitance between both electrodes. For this reason, the two-port would be prefered against the one-port configuration. For both measurements, a network analyzer is used to obtain the transmission frequency response of the *MEMS* devices.

However, in most cases the presence of the parasitic current is so high that mixing measurements have to be performed in order to be able to measure the quality factor of the resonator. Figure B.2 shows the electrical configuration for mixing measurements. In that



(a) One port transmission measurement



(b) Two port transmission measurement

Figure B.1: *Figure showing the electrical connection for measuring* MEMS *devices using the one- or two-port configuration.*

case, an alternate signal, named RF, is applied to the excitation driver whereas at the resonator an excitation voltage named LO is added to the DC voltage applied in the two-port measurement.

To understand the mixing capabilities of such devices, consider the total electrical force applied to the resonator under these conditions:

$$F_e = \frac{\partial E}{\partial x} = \frac{\partial}{\partial x}\left(\frac{1}{2}C_1V_1^2 + \frac{1}{2}C_2V_2^2\right) \tag{B.1}$$

where E is the energy stored in the device and derivatives are respect to the displacement variable, x. Figure B.3 shows the electrical scheme for mixing measurements. Electrical

connection between driver1 and resonator is named port1, and electrical connection between driver2 and resonator is named port2. So, V_1 and V_2 in equation B.1 refer to voltages applied at those port1 and port2, respectively.

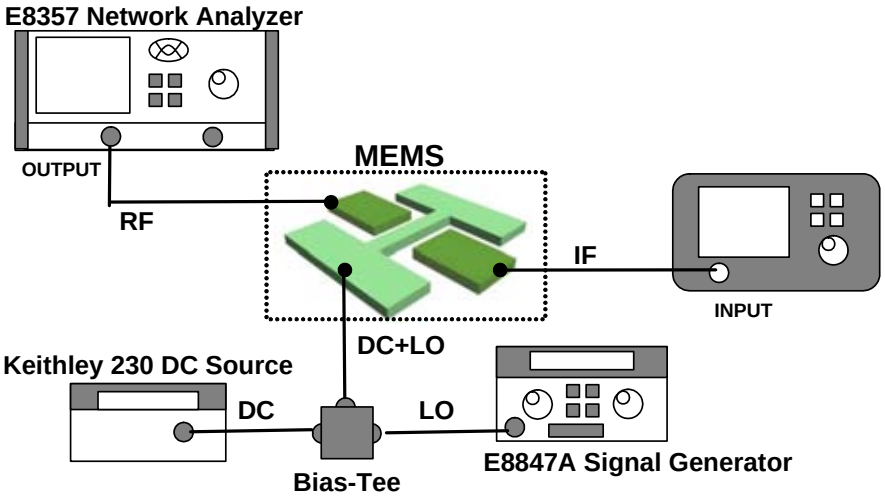


Figure B.2: *Electrical set-up for mixing measurements.*

Writing LO and RF signals as:

$$v_{LO} = V_{LO}\cos(\omega_{LO}t) \tag{B.2}$$

$$v_{RF} = V_{RF}\cos(\omega_{RF}t) \tag{B.3}$$

and derivating in eq. B.1:

$$\begin{aligned} F_e = \frac{1}{2}\frac{\partial C_1}{\partial x}\left(v_{RF}^2 + v_{LO}^2 + V_{DC}^2 + 2v_{DC}v_{LO} + 2v_{DC}v_{RF} + 2v_{RF}v_{LO}\right) \\ + \frac{1}{2}\frac{\partial C_2}{\partial x}\left(v_{LO}^2 + V_{DC}^2 + 2v_{LO}V_{DC}\right) \end{aligned} \tag{B.4}$$

Among all these terms, only the term represented by the product $v_{LO}v_{RF}$ is performing the mixing operation to the resonator:

$$F_e = ...\frac{\partial C_1}{\partial x}v_{LO}v_{RF}... \tag{B.5}$$

Equation B.5 can be rewritten considering eq. B.2, as:

$$F_e = ...\frac{1}{2}V_{LO}V_{RF}\frac{\partial C_1}{\partial x}\cos\left(\left(\omega_{RF} - \omega_{LO}\right)t\right)... \tag{B.6}$$

which indicates that the mixing of signals LO and RF drives the resonator to a force of frequency $\omega_{IF} = \omega_{RF} - \omega_{LO}$.

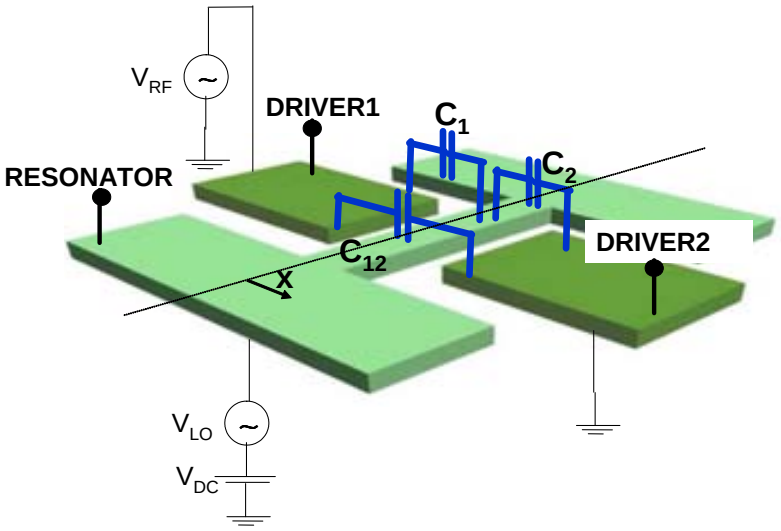


Figure B.3: *Configuration for performing mixing measurements.*

The idea beyond mixing measurements is to remove parasitic currents always present on transmission measurements. This current is generated due to two factors: i) the applied ac voltage (necessary to actuate the resonator) and ii) the intrinsic parasitic capacitances (due to the layout but also due to fringed fields) which are always present between the excitation and readout electrodes. This parasitic current screen the resonance current, which is the product of the time-variable capacitance between resonator and read-out electrode and the dc voltage applied. Taking advantage of the *MEMS* capabilities for mixing electrical signals, several techniques have been developed to perform such a measurement [100]. In this work, one of these measurement techniques based on *MEMS* mixing capabilities has been implemented [101].

In order to perform this measurement, two alternate signals have to be applied to the device. From one hand, an ac signal (named LO-local oscillator) is applied to the resonator electrode. This signal is added to the dc voltage applied to the resonator, as shows figure B.3. From the other hand, another ac signal (named RF) is applied to the input electrode. The resonator mixes these two ac signals giving an IF signal, which corresponds to the resonator's resonance frequency. In this case, the IF signal is measured by means of a spectrum analyzer. In our experiments, LO frequency is kept constant while the RF frequency is swept. The IF frequency signal measured, $w_{IF} = w_{LO} + w_{RF}$, at the spectrum analyzer corresponds to the resonator frequency response. The *MAX HOLD* option of the spectrum analyzer is activated in order to build up the resonance curve, measuring the IF signals for each RF frequency of the sweep.

A particular case of this mixing measurement occurs when the input RF frequency corresponds to the half of the resonance frequency of the device. In fact, this measurement consists on a two-port configuration (because an LO signal is not necessary) where the RF signal is the half of the IF frequency, $\omega_{RF} = \omega_{IF}/2$.
The electrical force in this case is:

$$F_e = \frac{1}{2}\frac{\partial C_1}{\partial x}\left(v_{RF}^2 + V_{DC}2 + 2v_{DC}v_{RF}\right) + \frac{1}{2}\frac{\partial C_2}{\partial x}V_{DC}^2 \tag{B.7}$$

and the relevant term that performs the mixing is given by v_{RF}^2:

$$\begin{aligned} F_e &= .....\frac{\partial C_1}{\partial x}v_{RF}^2... \\ F_e &= .....\frac{1}{2}V_{RF}\frac{\partial C_1}{\partial x}\cos\left(\left(2\omega_{RF}\right)t\right)... \end{aligned} \tag{B.8}$$

Due to the non-linearity of the electrical force, an harmonic signal at $2 \times \omega_{RF}$ is produced. Again, the purpose of exciting and reading at different frequencies is achieved. In both cases the electrical resonance current is:

$$I_2 = V_2\frac{\partial C_2}{\partial t} = V_2\frac{\partial C_2}{\partial x}\frac{\partial x}{\partial t} \tag{B.9}$$

APPENDIX C

List of publications

- **Articles**

"CMOS-MEMS 1GHz-Annular Ring Electrically Transduced by a 40nm Air-Gap", J.Teva, G.Abadal, A.Uranga, J.Verd, F.Torres, J. Ll. Lopez, J.Esteve, F. Pérez-Murano and N.Barniol. In preparation.

"CMOS-MEMS monolithically integrated paddle shaped resonator", J.Teva, G.Abadal, A.Uranga, J.Verd, F.Torres, J. Ll. Lopez, J.Esteve, F. Pérez-Murano and N.Barniol. In preparation.

"VHF clamped-clamped beam resonators monolithically integrated in a $0.35\mu m$ technology. Part I: Theoretical limits on the monolithically integration" J.Teva, G.Abadal, A.Uranga, J.Verd, F.Torres, J. Ll. Lopez, J.Esteve, F. Pérez-Murano and N.Barniol. In preparation.

"VHF clamped-clamped beam resonators monolithically integrated in a $0.35\mu m$ technology. Part II: Electrical characterization" J.Teva, G.Abadal, A.Uranga, J.Verd, F.Torres, J. Ll. Lopez, J.Esteve, F. Pérez-Murano and N.Barniol. In preparation.

"A femptogram resolution mass sensor platform, based on SOI electrostatically driven resonant cantilever. Part I: electromechanical model and parameter extraction". J. Teva, G. Abadal, F. Torres, J. Verd, F. Pérez-Murano, N. Barniol Ultramicroscopy, vol. 106 (8-9) pp.800-807, (2006).

"A femptogram resolution mass sensor platform, based on SOI electrostatically driven resonant cantilever. Part II: sensor calibration and glycerin evaporation rate measurement". J. Teva, G. Abadal, F. Torres, J. Verd, F. Pérez-Murano, N. Barniol Ultramicroscopy, vol. 106 (8-9) pp.808-814, (2006).

"Integrated CMOS-MEMS with on-chip readout electronics for high-frequency applications". J. Verd, A. Uranga, J. Teva, J. L. López, F. Torres, J. Esteve, G. Abadal, F. Pérez-Murano, and N. Barniol. IEEE Electron Device Letters, vol. 27 (6) pp.495-497, (2006).

"Design, fabrication and characterization of a sub-microelectromechanical resonator with monolithically integrated CMOS readout circuit". J. Verd, G. Abadal, J. Teva, M. Villarroya, A. Uranga, X. Borrisé, F. Campabadal, J. Esteve, E. Figueras, F. Pérez-Murano, Z. J. Davis, E. Forsén, A. Boisen, N. Barniol. IEEE Journal of MicroElectroMechanical Systems, vol. 14(3), pp. 508-519, (2005).

"Fully CMOS integrated low voltage 100MHz MEMS resonator". A. Uranga, J. Teva, J. Verd, J.L. López, F. Torres, J. Esteve, G. Abadal, F. Pérez-Murano and N. Barniol. Electronic Letters, vol. 41 (24), pp. 1327-1328, (2005).

"On the electromechanical modeling of a resonating nano-cantilever based transducer". J. Teva, G. Abadal, Z.J. Davis, J. Verd, X. Borrisé, A. Boisen, F. Pérez-Murano, N. Barniol. Ultramicroscopy , vol. 100 (2004) pp.225-232.

"Nanometer scale gaps for capacitive transduction improvement on RF-MEMS resonators". F. Torres, J. Teva, J.Ll. Lopez, A. Uranga, G. Abadal, N. Barniol, A. Sánchez-Amores, J. Montserrat, F. Pérez-Murano, J. Esteve. Microelectronic Engineering 84 (2007) 1384-1387.

- **Conference Proceedings**

"VHF CMOS-MEMS resonator monolithically integrated in a standard 0.35μm CMOS technology". J.Teva, G.Abadal, A.Uranga, J.Verd, F.Torres, J.L.Lopez, J.Esteve, F.Pérez-Murano, N.Barniol. Technical Digest of the 20th International Conference on Micro Electro Mechanical Systems 2007, MEMS 2007, pp.789-792 (2007).

"Resonant Metal Cantilever with Attogram/Hz Mass Sensitivity Fully Integrated in a Standard 0.35μm CMOS process". J. Verd, G. Abadal, J. Teva, A. Uranga, F. Pérez-Murano, J. Esteve, N. Barniol. Technical Digest of the 19th International Conference

on Micro Electro Mechanical Systems 2006, pp.638-641 (2006).

"Resonating cantilever mass sensor with mechanical on-plane excitation". J. Teva, G.Abadal, X. Jordà, X. Borrisé, Z.J. Davis, N.Barniol Proceedings of SPIE conference. Smart sensors, actuators and MEMS, vol. 5116, (2003), pp.353-363.

APPENDIX D

Experimental facilities

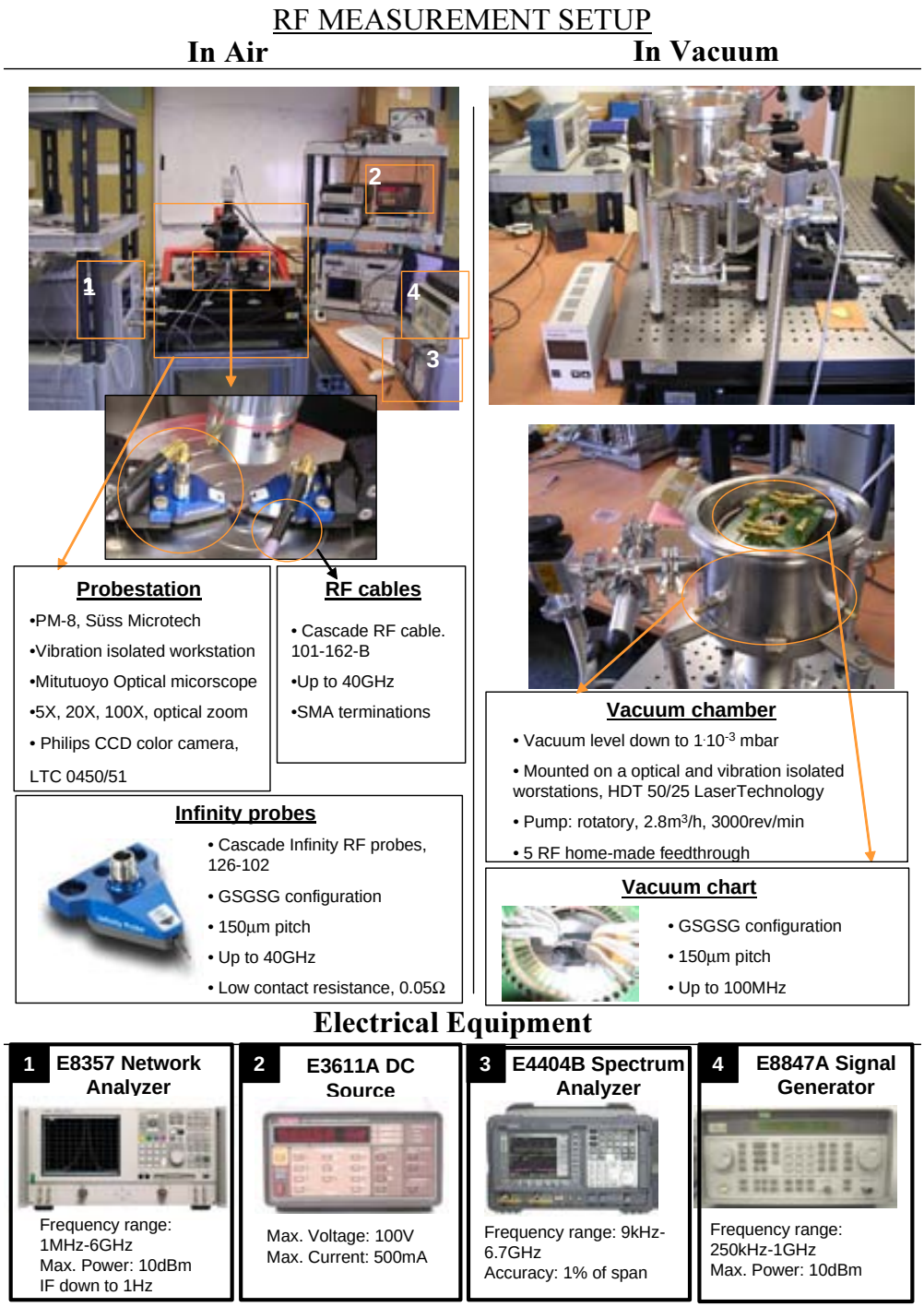


Figure D.1: *Photograph showing the experimental facilities at UAB. For the measurements in air, RF-probes are used. A vacuum chamber was designed in order to measure resonators in vacuum conditions.*