A CMOS PIXEL VERTEX DETECTOR FOR THE SUPER KEK-B EXPERIMENT SEMICONDUCTOR TRACKER

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By
María Elena Martín Albarrán

Dissertation Committee:

Prof. J. Aguiló, Chairperson
Dr. M. Lozano, Secretary
Prof. A. Diéguez
Dr. H.-G. Moser
Dr. G. Rizzo

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A CMOS PIXEL VERTEX DETECTOR FOR THE SUPER KEK-B EXPERIMENT SEMICONDUCTOR TRACKER

Dissertation presented to obtain the degree of Doctor of Philosophy in Electrical Engineering

Author: MARÍA ELENA MARTÍN ALBARRÁN

Directors : DR. GARY S. VARNER AND DR. CARLES FERRER I RAMIS

Dr. Gary S. Varner, Assistant Professor from the University of Hawai'i, Dr. Carles Ferrer i Ramis, Professor from the Universitat Autònoma de Barcelona

CERTIFY:

that the dissertation **"A CMOS pixel vertex detector for the Super KEK-B experiment semiconductor tracker "**, presented by Ms. María Elena Martín Albarrán to obtain the degree of Doctor of Philosophy in Electrical Engineering, has been done under their direction at the University of Hawaii and the Universitat Autònoma de Barcelona.

Barcelona, March 2008

Dr. Gary S. Varner　　　　Dr. Carles Ferrer i Ramis

Una de las lecciones más claras de la historia,
incluida la historia reciente, es que los derechos
no son graciosamente concedidos, sino conquistados.
Noam Chomsky

Aprendí que no se puede dar marcha atrás,
que la esencia de la vida es ir hacia adelante.
La vida, en realidad, es una calle de sentido único.
Agatha Christie

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ABSTRACT

This dissertation is entitled ***A CMOS pixel vertex detector for the super KEK-B experiment semiconductor tracker***. It will explain the research that has been done at the IDLab at the University of Hawai'i for the upgrade of the pixel detector. This summary will briefly explain the contents of each chapter that has been included.

Chapter 1 Introduction This chapter makes an overview of the fields that this dissertation has been developed. The first field is related to experimental particle physics and a brief description of the different kind of detectors that can be found in a complete detector environment, like a tracking detector. A tracking detector can be a semiconductor detector, which is the kind of detectors presented in this dissertation. From all the different possibilities, the option studied in this work is Monolithic (or Semi-Monolithic) Active Pixel Sensor (MAPS), that will be briefly introduced. The next aspect to be explained is a Belle experiment overview that explains the reason for the need for the upgrade of the vertex detector.

Chapter 2 Particle Detection and Tracking This chapter includes a technology review. This technology review describes drift and Charge-Coupled Device (CCD) detectors and their more successful applications in the field of high energy physics. The next kind of detectors explained include hybrid and monolithic (and semi-monolithic) detectors. The detectors that have been evaluated in this dissertation correspond to monolithic detectors: Complementary Metal Oxide Semiconductor (CMOS) with epitaxial layer and CMOS on Silicon on insulator (SOI). These two options are explained, specially the SOI technology, highlighting all the advantages and disadvantages presented by them. The next aspect that is explained in this chapter is how the detection is performed. The basis of all this semiconductor detectors are the p-n junction, where the junction capacitance, charge collection and signal formation are analyzed. The last aspect to be presented is the different pixel detector architectures, from the basic Passive Pixel Sensor (PPS) to the more complex

Active Pixel Sensor (APS). The most commonly used is the APS, because it includes amplification at pixel level. This approach has been evolving through the years, presenting a more complex architecture that will go from the basic 3 Transistor (3T) structure to the digitalization at pixel level.

Chapter 3 Principle of Detector Operation This chapter start listing the most important characteristics of the Silicon, that convert it as the most used material in pixel detector development and microelectronics digital/analog circuitry. The next aspect to be considered is the interaction of radiation with matter. There will be an analysis that includes the energy loss of heavy charged particles, and analyzing what are the fluctuations of loss. A similar analysis is performed for the energy loss by electrons and photons. The last aspects that are explained here include the energy for charge carrier generation in a semiconductor material and the multiple coulomb scattering.

Chapter 4 Belle Experiment Upgrade This chapter is used to introduce the environment where the pixel detector has to be working. To start this introduction basic particle physics and the Belle Experiment in Research Institute for High Energy Physics (KEK) are explained. The second explanation is related to B-Factories, specially to KEK. KEK is the accelerator where the Belle experiment is taking place. After this general introduction, the results obtained with the two first prototypes are introduced. Continuous Acquisition Pixel 1 (CAP1) is the first prototype, it consists of a basic 3T cell and irradiation studies and an analysis of the read-out speed is also presented. Continuous Acquisition Pixel 2 (CAP2) is the second prototype, it consists of a basic structure with 10 storage cells per pixel, that can be used to perform Correlated Double Sampling (CDS) read-out. As well as happened with CAP1, test beam results, irradiation studies and an analysis of the read-out speed is done.

Chapter 5 Continuous Acquisition Pixel 3 (CAP3) This chapter is used to explain the architecture of Continuous Acquisition Pixel 3 (CAP3) and to describe all the testing results obtained with the laser set-up. CAP3 was

developed using TSMC with a feature size of 0.25μm. The pixel architecture used here includes a double 8 group of storage cells per pixel. The laser spot was detected. But the output speed obtained with this chip was too slow, because the capacitance at the output lines were too high.

Chapter 6 Continuous Acquisition Pixel 4 (CAP4) This chapter is used to explain the architectures of Continuous Acquisition Pixel 4 (CAP4). In this chapter the laser testing set-up is explained with more detail. The Compound Operational Board Interface (COBI)/Particle Electronics Test & Readout Application Board (PETRA) board are introduced as a part of the new environment used for the development of the Continuous Acquisition Pixel (CAP) family. Then, the CAP4 architecture will be generally explained, to enter into more detail in the 2 architectures included in this chip: the Wilkinson and the Binary read-out. Wilkinson read-out prototype keeps studying the analog read-out kind of system. This architecture would include two main advantages. The use of a tree output structure to decrease the capacitance at the output node. And the inclusion of a comparator every few rows that would digitalized the signal obtained at pixel level The second option evaluated in this CAP4 was a more complex digitalization pixel structure. It analyzed the possibilities of using a pixel with circuitry that would take responsibility of the detection of a hit based on a general threshold signal. The main characteristic of this approach is the transmission pixel-by-pixel of the signal obtained for both sides, left and right. There were two different pixel layout included in the CAP4 layout. The main difference was the number of Positive-channel Metal-Oxide Semiconductor (PMOS) used. The approach with higher number of PMOS transistors showed results based in a read-out speed of 10Mhz.

Chapter 7 Continuous Acquisition Pixel 5 (CAP5) Continuous Acquisition Pixel 5 (CAP5) chapter analyzed the possibility of overcoming the limitation of PMOS transistor that appears in a CMOS with epilayer technology. The usage of a SOI process was available through a collaboration with KEK and OKI Electric Industry Co. Ltd. (OKI). This prototypes were fabricated using a second run of a 0.15μm SOI process. The pixel that were submitted for

this process included the same architectural approach as CAP4 binary. The basic read-out cell, with the reset transistor and source-follower was working according to our expectations, but the comparator and all the digital circuits showed a very poor performance. This chip was used to characterized the transistors and see the real effects of using the openings on the variation of the threshold voltage, showing results that were never reported before.

Chapter 8 Conclusions This section presents the main achievements presented in all the dissertation, they are novelty of the pixel architecture used, even though the experimental results obtained have not been as successful as expected. CAP6 prototype will also continue evaluating the Wilkinson architecture in the 0.35μm TSMC process was done in October 2007. CAP7 prototype will be evaluating the binary solution. This binary solution will be fabricated using a 0.20μm SOI process of OKI. This process has been developed for several years and has shown great performance. CAP7 submission was done in January 2008 with improved binary solution to correct the pixel chatter problem.

RESUMEN

Esta tesis doctoral se titula ***A CMOS pixel vertex detector for the Super KEK-B experiment semiconductor tracker***. Esta tesis explicará toda la investigación que se ha desarrollado en el laboratorio IDLab, que se encuentra en la University of Hawai'i, y que corresponde al *upgrade* del detector de pixel. Este resumen explicará brevemente los contenidos de cada capítulo presente en esta memoria.

Capítulo 1 Introducción Este capítulo presenta una revisión de algunos de los campos de conocimientos en los cuales se desarrolla esta tesis. El primer campo que se menciona está relacionado con física experimental de partículas y introduce brevemente los diferentes tipos de detectores que pueden ser encontrados en el entorno de un detector a nivel general, como podría ser un detector de *tracking*. Un ejemplo de detector de *tracking* es el detector basado en semiconductores, que es el tipo de detectores que es presentado y desarrollado en esta tesis. De todas las diferentes opciones, el tipo de tecnología escogida para desarrollar en est tesis corresponde a MAPS, que también será presentado. El siguiente aspecto que se explicará es una visión general del experimento Belle y que explicará las razones que han llevado a la necesidad de la actualización del *vertex detector*.

Capítulo 2 Detección y Rastreo de Partículas Este capítulo presenta una revisión tecnológica. Esta revisión describe brevemente a los detectores de *drift* y basados en CCD y tambien sus aplicaciones más exitosas en el campo de la física de altas energías. El siguiente tipo de detectores que se explican incluyen los detectores híbridos y monolíticos (y semi-monolíticos). Los detectores que han sido evaluados en esta tesis corresponden a detectores monolíticos (o MAPS) en dos de sus modalidades: CMOS con capa epitaxial y CMOS con tecnología SOI. Estas dos opciones tecnológicas son explicadas detalladamente, especialmente la tecnología SOI, y se procede a resaltar las ventajas y desventajas más importantes presentes en ambas tecnologías. El siguiente aspecto que se explica en este capítulo es como se realiza la detección

de las partículas. La base de todos los detectores es la unión pn, y se hace un análisis detallado de la capacidad de unión presente, la carga capturada y como se realiza la creación de la señal que será posteriormente detectada. El último aspecto que se presenta aquí es un análisis de las diferentes arquitecturas a nivel de pixel, que iran desde la bàsica PPS a la más compleja APS. La mayormente utilizada es la APS, debido a la amplificación que se incluye en cada pixel presente. Esta arquitectura ha ido evolucionando a lo largo de los años, presentado una arquitectura que se encuentra desde la estructura básica llamada 3T a la que incluye una digitalización a nivel de pixel.

Capítulo 3 Principos de Operación para un Detector Este capítulo se inicia con un listado de las características más importantes del silicio, que lo convierten en el material más usado en el desarrollo de detectores de píxel y en la tradional circuitería digital o analógica que se desarrolla en el campo de la microelectrónica. El siguiente aspecto considerado es la interacción de la radiación con la materia. Se presenta un análisis que incluye las pérdidas de energía de partículas cargadas pesadas y también se analizan las fluctuaciones que aparecen en las pérdidas. Un análisis similar se produce tambien para las pérdidas de energia producida por electrones y fotones. Los últimos aspectos que se explican aquí incluyen la energía por generación de portadores en un material semiconductor y el *multiple coulomb scattering*.

Capítulo 4 Upgrade del Experimento Belle Este capítulo se utiliza para introducir el entorno donde el detector de pixel tiene que acabar trabajando. Para empezar esta introdución se hará una descripción de conceptos básicos de física de partículas, del experimento Belle, y también de KEK. La segunda explicación es una descripción de las características más importantes de las *B-Factories* y especialmente sobre KEK. KEK es el acelerador donde el experimento Belle tiene lugar. Despué de esta introducción general, se presentan los resultados obtenidos con los dos primeros prototipos. CAP1 es el primer prototipo, consiste de una celda 3T básica, con el cual se presentan los resultados de la radiació a la que el prototipo ha sido expuesto, a parte de estos resultados se hace un análisis de la velocidad de lectura obtenida. CAP2 es

el segundo prototipo, y presenta una estructura básica que contiene 10 celdas de almacenaje por pixel. Estas 10 celdas pueden ser utilizadas para hacer una lecture con CDS. Tal y como se hizo anteriormente con CAP1, los resultados de la irradiación a la que el prototipo ha sido expuesto se presentan, y también se realizará un análisis de la velocidad de lectura obtenida.

Capítulo 5 ***Continous Acquisition Pixel 3 (CAP3)*** Este capítulo se utiliza para explicar la arquitectura de CAP3 y para describir todos los resultados de test obtenidos con el *set-up* del laser. CAP3 se fabricó utilizando el proceso de TSMC de 0.25μm. La arquitectura de pixel usada aquí incluye un grupo doble de 8 celdas de almacenaje por pixel. El laser infrarrojo era detectado claramente, pero la velocidad de lectura que se obtenía con este chip era muy baja, en parte, debido a que las capacidades que se encontraron en las líneas de salida eran muy altas.

Capítulo 6 ***Continous Acquisition Pixel 4 (CAP4)*** Este capítulo se utiliza para explicar las arquitecturas que se utilizan en CAP4. En este capítulo se describirá con mayor detalle el *set-up* de test del laser. Las placas COBI/PETRA son presentadas como partes del nuevo entorno que se usara para el desarrollo de la familia CAP. Después de esto, la arquitectura del CAP4 se explicará de un manera general, para despues entrar en detalle en las dos arquitecturas presentes en este chip: *Wilkinson* y *Binary*. El prototipo con lectura de salida tipo *Wilkinson* es la continuación del estudio del tipo de lecturas de salida tipo analógico. Esta arquitectura presenta dos ventajas. La primera es la utilización de una estructura tipo árbol para disminuir la capacidad del nodo de salida. La inclusión de un comparador cada 3-4 filas permiten la digitalización de la señal obtenida a nivel de pixel. La segunda opción evaluada en el CAP4 era una estructura que realiza una mucho más compleja digitalización a nivel de pixel. Esta opción analiza la posibilidad de utilizar un pixel con gran número de circuitería que se encargaría de la detección de un *hit* dependiendo de una señal humbral. La característica más importante de esta aproximación es la transmisión de la información de pixel a pixel, hacia la derecha y hacia la izquierda. Esta arquitectura presenta dos

tipos diferentes de *layout*, que difieren en el número de transistores PMOS utilizados. El *layout* que presentaba mayor número de transistores PMOS presentó resultados para velocidades de lectura de 10Mhz.

Capítulo 7 ***Continous Acquisition Pixel 5 (CAP5)*** El capítulo que describe CAP5 estudia la posibilidad de evitar las limitaciones del número de transistores PMOS utilizados, que aparece en la utilización de CMOS con capa epitexial. La utilización de un proceso SOI es posible gracias a una colaboración de KEK con la empresa OKI. Estos prototipos se fabricaron utilizando un *run* del proceso 0.15μm de SOI. El pixel que se envió a fabricar seguía la misma arquitectura que en el *CAP4 binary*. La celda de lectura básica, con el transistor de *reset* y con la estructura de *source-follower* funcionaron de acuerdo con las expectativas, pero el comparador y toda la circuitería digital mostró un funcionamiento muy pobres. Este chip se utilizó para caracterizar los transistores y comprobar los efectos de utilizar las aberturas para las implantaciones en las variaciones de tensión humbral, mostrando resultados que no se habían mostrado antes.

Capítulo 8 Conclusiones Este capítulo presenta los mayor logros conseguidos a lo largo de esta tesis. Entre ellos esta la presentación de una arquitectura a nivel pixel (*binary*) que nunca antes había sido utilizada, aunque los resultados experimentales no son tan exitosos como era de esperar. Se presentará al prototipo de CAP6 que continuará evaluando la arquitectura de Wilkinson con un proceso de TSMC de 0.35μm que se envió a fabricar en Octubre de 2007. El prototipo de CAP7 continuará evaluando la solución *binary*. Esta solución se fabricará utilizando el proceso de SOI de 0.20μm de OKI. Este proceso se ha desarrollado y utilizado durante años y ha mostrado un funcionamiento excelente. La fabricación de CAP7 se realizó en Enero del 2008 incluyendo una solución *binary* donde el problema de *chattering* presente en CAP4 se intenta evitar.

SUMARI

Aquesta tesi doctoral es titula***A CMOS pixel vertex detector for the Super KEK-B experiment semiconductor tracker***. Aquesta tesi explicarà tota la investigació que s'ha desenvolupat en el laboratorio IDLab, que es trobas a la University of Hawai'i, i que correspon a l'*upgrade* del detector de pixel. Aquest resum explicarà breument els continguts de cada capítol present en aquesta memòria.

Capítol 1 Introducció Aquest capítol presenta una revisió d'alguns dels camps de coneixement en els quals es desenvolupa aquesta tesi. El primer camp que es menciona està relacionat amb la física experimental de partícules i introdueix breument els diferent tipus de detectors que es poden trobar en l'entorn d'un detector en termes molt generals, com podria ser un detector de *tracking*. Un exemple de detector de *tracking* és el detector bast en semiconductors, que és el tipus de detector presentat i desenvolupat en aquest tesi. De totes les diferents opcions, el tipus de tecnologia escollida per desenvolupar en aquesta tesi correspon a MAPS, que també serà presentat. El següent aspecte que s'explicarà és una visió general de l'experiment Belle i que explicarà les raons que han portat a la necesitat d'actualització del *vertex detector*.

Capítol 2 Detecció i *Tracking* de Partícules Aquest capítol presenta una revisió tecnològica. Aquesta revisió descriu breument els detectors de *drift* i basats en CCD i també les seves aplicacions més exitoses en el camp de la física d'altes energies. El següent tipus de detectors que s'expliquen inclouen els detectors híbrids i monolítics (i semi-monolítics). Els detectors que s'han evaluat en aquesta tesi corresponen a detectors monolítics (o MAPS) en dos de les modalitats possibles: CMOS amb capa epitaxial i CMOS amb tecnologia SOI. Aquestes dues opciones tecnològiques són explicades detalladament, especialment la tecnologia SOI, i es procedeix a resaltar les avantatges i desvantatges més importants presents en ambdues tecnologies. El següent aspecte que s'explica en aquest capítol és com es realitza la detecció de les partícules. La base de tots els detectors és la unió pn, i es fa una anàlisis detallat de la

capacitat d'unió present, la càrrega capturada i com es realitza la creació de la senyal que será posteriorment detectada. L' últim aspecte que es presenta aquí és un anàlisi de les diferents arquitectures a nivell de pixel, que aniran desde la bàsica PPS a la més complexa APS. La majorment utilitzada és la APS, degut a l'amplificació que s'inclou en cada pixel present. Aquesta arquitectura ha anat evolucionant al llarg dels anys, presentant una arquitectura que es troba desde l'estructura bàsica que es diu de 3T a la que inclou una digitalització a nivell de pixel.

Capítol 3 Principis d'Operació per un Detector Aquest capítol s'inicia amb un llistat de les característiques més importants del silici, que el converteixen en el material més utilitzat en el desenvolupament de detectores de píxel i en la tradional circuitería digital o analògica que es desenvolupa en el camp de la microelectrònica. El següent aspecte considerat és la interacció de la radiació amb la materia. Es presenta un análisi que inclou les pèrdues d'energía de partícules carregades pesades i també s'analitzen les fluctuacions que apareixen en les pèrdues. Un anàlisi similar es produeix també per les pèrdues d'energia produïda per electrons i fotons. Els últims aspectes que s'explican aquí inclouen l'energía per generació de portadors en un material semiconductor i el *multiple coulomb scattering.*

Capítol 4 Upgrade de l'Experiment Belle Aquest capítol s'utilitza per introduir l'entorn on el detector de pixel ha d'acabar treballant. Per començar aquesta introducció es farà una descripció de conceptes bàsics de física de partícules, l'experiment Belle, i de KEK. La segona explicació és una descripció de les característiques més importants de les *B-Factories* i especialment sobre KEK. KEK és l'accelerador on l'experiment Belle té lloc. Després d'aquesta introducció general, es presenten els resultats obtinguts amb els dos primers prototips. CAP1 és el primer prototipus, consisteix en una cel·la 3T bàsica, per la qual es presenten els resultats per la radiació a la qual el prototipus ha esta exposat, a part d'aquests results es fa un anàlisi de la velocitat de lectura obtinguda. CAP2 és el segon prototipus, i presenta una estructura bàsica que conté 10 cel·les d' emmagatzament per pixel. Aquestes cel· poden

ser utilitzades per fer lectures amb CDS. De la mateixa maner que es va fer amb CAP1, els resultats de la radiació a la que el prototipus ha estat exposat es presenten, i també es realizarà un anàlisi de la velocitat de lectura obtinguda.

Capítol 5 ***Continous Acquisition Pixel 3 (CAP3)*** Aquest capítol s'utiltza per explicar l'arquitectura de CAP3 i per descriure tots els resultats de test obtinguts amb el *set-up* del laser. CAP3 es va fabricar utilitzant el procés de TSMC de 0.25μm. L'arquitectura de pixel utilitzada aquí inclou un grup doble de 8 cel·les d'emmagatzament per pixel. El laser infraroig era detectat clarament, pero la velocitat de lectura que s'obtenia amb aquest chip era molt baixa, en part, degut a que les capacitats que es trobaben a les línees de sortida eren molt altes.

Capítol 6 ***Continous Acquisition Pixel 4 (CAP4)*** Aquest capítol s'utiliza per explicar les arquitectures que s'utilizan en CAP4. En aquest capítol es descriurà amb més detall el *set-up* de test del laser. Les plaques COBI/PETRA són presentades com a parts del nou entorn que s'utilitzarà pel desenvolupament de la familia CAP. Després d'això, l'arquitectura del CAP4 s'explicarà d'una manera general, per després entrar en detall en les dues arquitectures presents en aquest xip: *Wilkinson* i *Binary*. El prototipus amb lectura de sortida tipus *Wilkinson* és la continuació de l'estudi del tipus de lecturas de sortida tipus analògic. Aquesta arquitectura presenta dues aventatges. La primera és la utilizació d'una estructura tipus arbre per disminuir la capacitat del node de sortida. La inclusió d'un comparador cada 3-4 files permet la digitalització de la senyal obtinguda a nivell de pixel. La segona opció evaluada en el CAP4 era una estructura que realitza una molt més complexa digitalització a nivell de pixel. Aquest opció analitza la posibilitat d'utilizar un pixel amb gran nombre de circuiteria que s'encargaria de la detecció d'un *hit* depenent d'una senyal llindar. La característica més important d'aquesta aproximació és la transmisió de la informació de pixel a pixel, cap a la dreta i cap a l'esquerra. Aquesta arquitectura presenta dos tipus diferents de *layout*, que difereixen en el número de transistors PMOS utilitzats. El *layout*

que presentava més número de transistors PMOS va presentar resultats per velocitats de lectura de 10Mhz.

Capítol 7 ***Continous Acquisition Pixel 5 (CAP5)*** El capítol que descriu CAP5 estudia la posibilitat d'evitar les limitacions del número de transistors PMOS utilizats, que apareixen en la utilització de CMOS amb capa epitexial. La utilizació d'un procés SOI és possible gràcies a una colaboració de KEK amb l'empresa OKI. Aquests prototipus es van fabricar utilitzant un *run* del procés 0.15μm de SOI. El pixel que es va enviar a fabricar seguia la mateixa arquitectura que en el *CAP4 binary*. La cel·la de lectura bàsica, amb el transistor de *reset* i amb l'estructura de *source-follower* van funcionant d'acord amb les expectatives, però el comparador i tota la circuiteria digital va mostrar un funcionament molt pobres. Aquest xip es va utilitzar per caracteritzar els transistors i comprovar els efectes d'utilizar les obertures per les implantacions en les variacions de tensió llindar, mostrant resultats que no s'havien mostrat abans.

Capítol 8 Conclusions Aquest capítol presenta els majors assoliments aconseguits al llarg d'aquesta tesi. Un d'ells és la presentació d'una arquitectura a nivell pixel (*binary*) que mai abans habia estat utilitzada, encara que els resultats experimentals no són tan exitosos como era d'esperar. Es presentarà al prototipus de CAP6 que continuarà evaluant l'arquitectura de Wilkinson amb un procés de TSMC de 0.35μm que s'ha enviat a fabricar en Octubre de 2007. El prototipus de CAP7 continuarà evaluant la solució *binary*. Aquesta solució es fabricarà utilitzant el procés de SOI de 0.20μm de OKI. Aquest procés s'ha desenvolupat i utilitzat durant anys i ha mostrat un funcionament excel·ent. La fabricació de CAP7 es va realitzà al Gener del 2008 incloent una solució *binary* on el problema de *chattering* present en CAP4 s'ha intentat evitar.

Glossary

3T 3 Transistor. x, xiv, xviii, 10, 11, 50, 79, 122, 123, 134, 168, 170, 171, 175–177, 182, 185, 188

ACC Aerogel threshold Cherenkov Counters. 67

ADC Analog-to-Digital Converter. 69, 70, 76, 97, 108, 109, 114, 116, 125, 127, 190

ALICE A Large Ion Collider Experiment. 15, 17

AMS Austria MicroSystems. 115, 165, 190

APS Active Pixel Sensor. ix, xiv, xviii, 11, 49

ASIC Application-Specific Integrated Circuit. 20

ATLAS A Toroidal LHC ApparatuS. 17, 18

BABAR B/B-bar. 18

BE Back-End. 76

BESOI Bonded and Etched-Back Silicon-On-Insulator. 19, 27

BJT Bipolar Junction Transistor. 21

BOX Buried Oxide Layer. 25, 27–29, 33, 37, 152, 154, 156

BTev BlueTrait Event Viewer. 17

CAP Continuous Acquisition Pixel. xi, xv, xix, 10, 12, 50, 65, 69, 71, 75, 113, 116, 121, 124, 142, 147, 164, 165, 168, 189

CAP1 Continuous Acquisition Pixel 1. x, xiv, xviii, 10, 68–71, 73, 75, 76, 78, 116, 125, 128

CAP2 Continuous Acquisition Pixel 2. x, xiv, xviii, 10, 70, 71, 73, 75, 76, 78, 116, 125, 128, 187

CAP3 Continuous Acquisition Pixel 3. x, xv, xix, 10, 73, 75, 76, 78, 79, 83, 86, 91, 110, 111, 116, 122, 125, 128, 187

CAP4 Continuous Acquisition Pixel 4. xi, xv, xvi, xix, xx, 10, 111, 114, 115, 131, 144, 145, 147, 165, 168, 170, 188, 189

CAP5 Continuous Acquisition Pixel 5. xi, xvi, xix, 161, 165, 167, 168, 175, 182, 188

CCD Charge-Coupled Device. ix, xiii, xvii, 7, 9, 13–16, 49, 63, 190

CDC Central Drift Chamber. 67

CDS Correlated Double Sampling. x, xiv, xviii, 19, 49, 70, 75, 76, 78, 79, 83, 102, 104

CERN Centre Européenne pour la Recherche Nucléaire. 15–19, 114

CMOS Complementary Metal Oxide Semiconductor. ix, xi, xiii, xvi, xvii, xix, 7, 9, 11, 13, 19–22, 25, 29, 33, 49, 51, 63, 116, 131, 134, 136–140, 147, 148, 152, 164, 188–190

CMS Compact Muon Solenoid. 17, 18

COBI Compound Operational Board Interface. xi, xv, xix, 12, 113, 144, 173, 174, 187

CP Charge conjugation Parity. 8, 9, 67

CVD Chemical Vapour Deposition. 14, 18

CW Continuous Wave. 112, 113

DAC Digital-to-Analog Converter. 11, 182–185

DEPFET DEpleted P-channel Field Effect Transistor. 7, 20

DSSD Double Sided Silicon Detector. 8, 76

EFC Extreme Forward Calorimeter. 67

ENC Equivalent Noise Charge. 24

FAPS Flexible Active Pixel Sensor. 50

FD-SOI Fully-Depleted Silicon-On-Insulator. 29, 32–35, 37, 39, 148

FE Front-End. 17, 70, 76, 113

FET Field Effect Transistor. 14

FPGA Field Programmable Gate Array. 10, 113, 139, 189

FPN Fixed-Pattern Noise. 49, 78

FWHM Full Width at Half Maximum. 58

HAPS Hybrid Active Pixel Sensor. 7, 14, 17

HEP High Energy Physics. 3, 13, 14, 49, 65, 114

HV High Voltage. 173–176, 182, 183, 185, 190

IC Integrated Circuit. 21, 22

IGFET Insulated-Gate Field-Effect Transistor. 25

IHXCP Imaging Hard X-Ray Compton Polarimeter. 179

ILC International Linear Collider. 21, 50

IR Infrared. 79, 112, 113, 144

ITOX Internal Oxidation. 27

JAXA/ISAS Japan Aerospace Exploration Agency /Institute of Space and Astronautical Science. 151

KEK Research Institute for High Energy Physics. x, xi, xiv, xvi, xviii, xx, 8, 10, 20, 50, 65, 69, 70, 147, 148, 151, 158, 188, 189

LBNL Lawrence Berkeley National Laboratory. 151

LHC Large Hadron Collider. 15, 17, 18

LHCb Large Hadron Collider beauty. 17

LV Low Voltage. 164, 173, 174

LVDS Low-voltage differential signaling. 69, 70

MAPS Monolithic (or Semi-Monolithic) Active Pixel Sensor. ix, xiii, xvii, 7, 9, 10, 14, 16, 22, 28, 50, 67, 68, 131

MCM Multi-Chip Module. 7, 17

MIMOSA Minimum Ionising Particle MOS Active Pixel Sensor. 24, 50

MIP Minimum Ionizing Particle. 18, 19, 24, 56, 57, 62

MOS Metal Oxide Semiconductor. 19, 20, 28, 29, 48, 49

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor. 19, 25, 29, 32, 33, 35, 37

MPW MultiProject Wafer. 151

MWPC Multi-Wire Proportional Chamber. 6

NMOS Negative-channel Metal-Oxide Semiconductor. 116, 131, 134–138, 154, 156, 158, 159, 162, 165, 170, 188

OKI OKI Electric Industry Co. Ltd.. xi, xii, xvi, xx, 10, 12, 20, 33, 147, 148, 158, 159, 161, 164, 188–190

PAW Physics Analysis Workstation. 114

PD-SOI Partially-Depleted Silicon-On-Insulator. 29, 34, 35

PETRA Particle Electronics Test & Readout Application Board. xi, xv, xix, 12, 114, 144, 187

PMOS Positive-channel Metal-Oxide Semiconductor. xi, xv, xvi, xix, 131, 134–137, 145, 154, 158, 159, 165, 170, 182, 188

PPS Passive Pixel Sensor. ix, xiv, xviii

PUC Pixel Unit Cell. 117, 122, 123, 128, 132

PVD Pixel Vertex Detector. 75

RHIC Relativistic Heavy Ion Collider. 15

SDD Silicon Drift Detectors. 14, 15

SEE Single Events Effects. 25

SER Soft Error Rate. 30

SIMOX Separation by IMplantation of OXygen. 19, 25, 27

SLC Stanford Linear Collider. 16

SNR Signal-to-Noise Ratio. 16, 39, 44, 69, 70

SOI Silicon on insulator. ix, xi–xiii, xvi, xvii, xx, 7, 10–13, 19, 24, 25, 27–35, 43, 51, 147, 148, 151, 152, 158, 164, 178, 181, 188–190

SOITEC Silicon on Insulator Technologies. 19

SPS Super Proton Synchroton. 15

SVD Silicon Vertex Detector. 8, 9, 67, 189

TCAD Technology Computer Aided Design. 12, 147, 154

TEG Test Element Group. 11, 12, 158

TEM Transmission Electronic Microscopy. 151, 154

TESLA Tera-electronvolt Energy Superconducting Linear Accelerator. 17, 20

TID Total Ionizing Dose. 33

TOF Time-of-Flight. 67

TPC Time Projection Chamber. 6

TRISTAN Tri Ring Intersecting STorage Accelerators at Nippon. 65

ZMR Zone-Melting Recrystallization. 19

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Chapter 1

Introduction

1.1 Particle Physics and Experimental Methods

Human nature has determined the advances of our society. The main force that is driving these advances is the curiosity of human beings. Curiosity makes a person ask the reason for a thing to happen. Curiosity then drives humans to mathematically describe nature. In order to satisfy this curiosity, new inventions are required for further refine these mathematical laws.

One of the first tools used to relate to our environment was the eye, which can be considered **the first particle detector**. The eye shows high sensitivity to photons, with good spatial resolution, and a large dynamic range. It shows wavelength discrimination, being sensitive to the region of the electromagnetic spectrum known as the visible region(see Fig. 1.1). The answer of what is the best description of matter in terms of fundamental constituents has been evolving through time. Until the 19th century, atoms were considered the smallest building block. In the 20th century electrons, protons and neutrons were discovered, now there is proof that these particles have substructure (quarks and gluons). Now it is known that hadrons are not fundamental and are composed of finer building blocks.

These days, the smallest constituents of matter (see Fig. 1.2) and the fundamental forces between them are being studied by a branch of science called High Energy Physics (HEP). This field has a theoretical and an experimental component. HEP experiments study the interaction of particles by the scattering of particles on another particles. The results of these interactions show a change in the direction, energy and/or momentum of the original particles, and the production of new

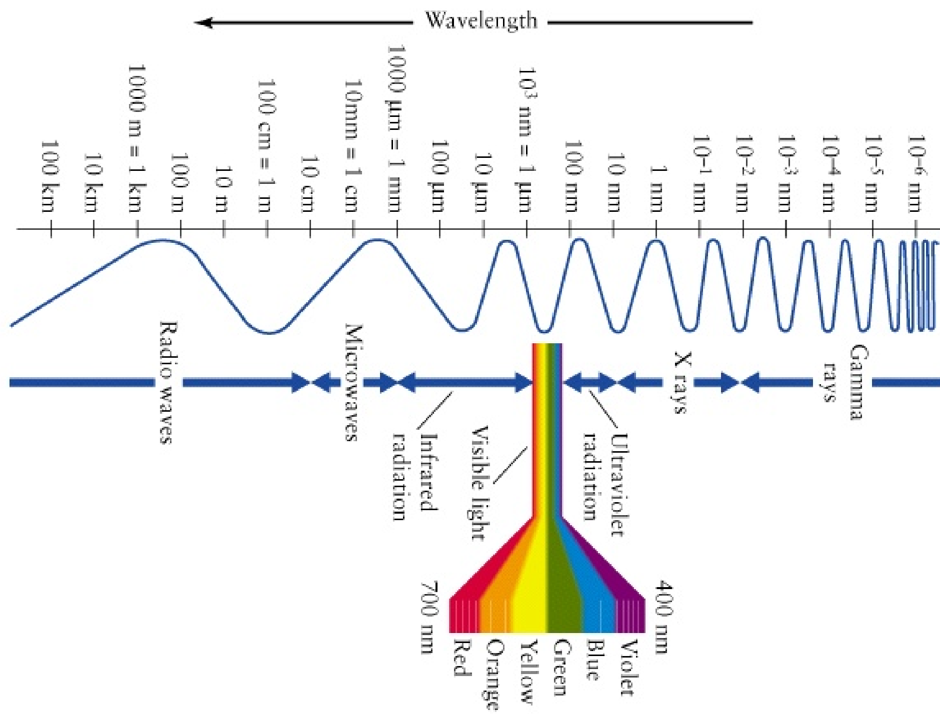


Figure 1.1: Electromagnetic Spectrum

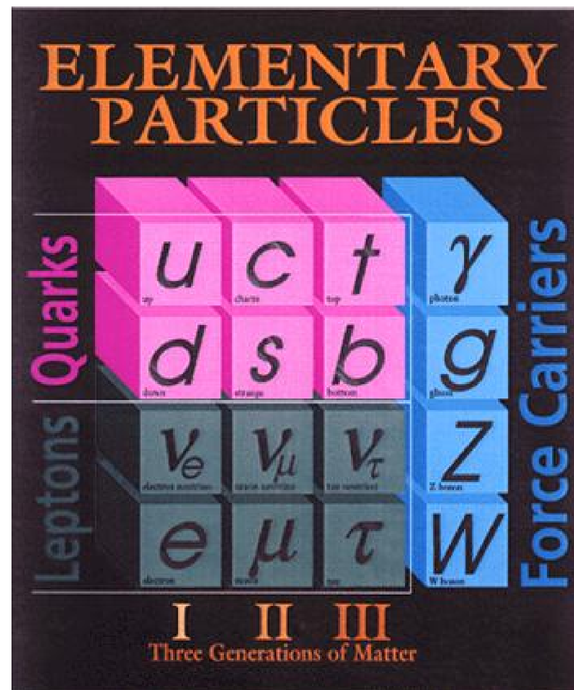


Figure 1.2: Elementary particles according to the Standard Model

particles. The interactions happen in accelerators, where electric fields are used to accelerate particles. Accelerators types includes the synchrotron, fixed target or colliding beams. A particle detector should provide the coverage of full solid angle with a fine segmentation and measure the momentum/energy of the particles. The detector must detect, track, and identify all of the particles with a fast response time, often with no dead-time. These characteristics require the detector to be located very close to, and surround, the interaction point.

To measure the energy of a particle a calorimeter is used. To measure the momentum of a particle a magnetic spectrometer along with tracking detectors are required. Time of flight or Cerenkov radiation detectors are used to determine the particle velocity. Many effects such as multiple scattering (when undergoing through a thick material layer) must be taken into account to obtain a correct value of the particle's momentum. The detection of charged particles is based on their loss of energy that happens with discrete collisions with atomic electrons that could end up into ionization, nuclear collisions, Cerenkov radiation, transition radiation (between two media), bremsstrahlung, e^--e^+ pair production, electromagnetic shower or hadron production. In the case of the interaction of photons with matter, the loss of energy can come from the photoelectric effect, Compton scattering or pair production.

The major part of energy loss of a traversing heavy particle is due to the inelastic collision with the electrons in the medium. The energy is transferred from the traversing particle to the electrons in the atoms. If enough energy is transferred the atom is ionized. When a particle traverses a medium it usually encounters many electrons. The loss of energy by ionization is given by the Bethe-Bloch formula. The Bethe-Bloch formula gives results accurate to within a few percent for traversing particles down to $\beta \sim 0.1$.

When the interaction takes place in thin layers there are few collisions that presents large fluctuations, known as Landau tails. For thick layers there are many collisions and the measurement of energy loss will present a Gaussian shape distribution. The particles that can be detected are divided in two groups: charged particles (e^-, e^+, protons, $\pi^{\pm}$, $K^{\pm}$, $\mu^{\pm}$) and neutral particles (γ, n, K^0, ν).

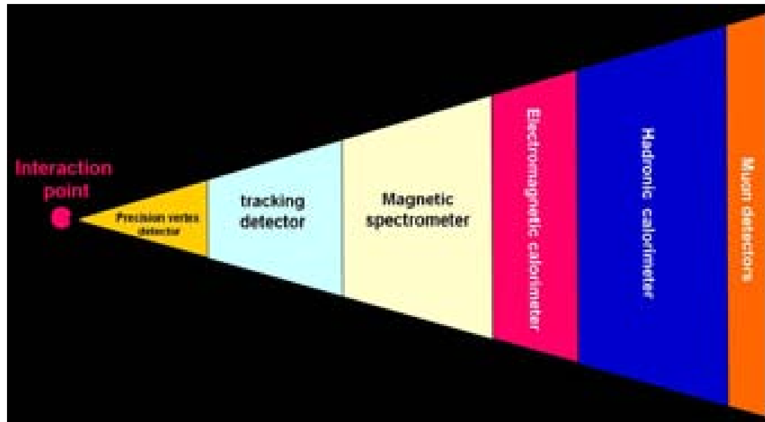


Figure 1.3: Detector Concept, showing different architectures

All these particles interact differently with matter, therefore one detector system will combine different technologies or detector types, as shown in Fig. 1.3. Tracking detectors measure the tracks and allow for reconstruction of the measured space points of the flight path, and enable an extraction of information on the momentum. These detectors record an ionization signal or are based on the produced scintillation light. Ionization signals can be measured with Geiger-Müller counters, Multi-Wire Proportional Chambers (MWPCs), Time Projection Chambers (TPCs), Bubble chambers or **Silicon detectors**.

1.2 Semiconductor Detectors and MAPS

A complete particle detector is composed of different sensors, integrated electronics, and tools for data processing and storage, as seen in Fig. 1.4. This

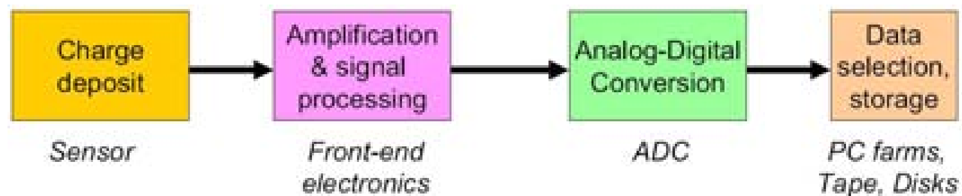


Figure 1.4: Simplified block diagram of a typical particle detector

basic structure can have variations, like amplification and signal processing at the sensor level. Semiconductor sensors have been developed based on the evolution of microelectronics. The use of Silicon as the most common material in semiconductor sensors is because of its well known properties and the existence of production

techniques for high quality substrates. A historical review of Silicon Pixel Detectors starts with drift and CCD pixel detectors. In recent years, these detectors have been joined by two different technology approaches: Hybrid sensor and MAPSs. The main difference between Hybrid sensor and MAPS is that Hybrid sensor presents a sensor and a Front-End chip that are connected using bump bonding flip-chip technology. This additional technology to put both chips together increases costs and can lead to pixel sizes larger than MAPS case. In the case of MAPS, the amplifying, logic and the sensor are integrated in one entity. MAPS can therefore have smaller pixel sizes. Both technological approaches are being actively researched. For a Hybrid sensor the most interesting approaches are Hybrid Active Pixel Sensors (HAPSs), Multi-Chip Modules (MCMs) Technology on Silicon, Active edge 3-D Silicon and Diamond pixel detectors. For MAPS the most interesting approaches are CMOS on high resistivity bulk, CMOS with epi-layer, CMOS on SOI, Amorphous Silicon on CMOS, DEpleted P-channel Field Effect Transistor (DEPFET) in high resistivity bulk and Deep n-well sensor. The technology for both approaches is rapidly advancing. Once advance particularly interesting is 3D packaging. 3D packaging consists of different layers that are connected with vertical interconnection. Each layer can perform a different task and can belong to a different technology, like CMOS on SOI for the detector layer, digital circuitry in CMOS, analog circuitry in CMOS and Opto Electronics and/or regulation in CMOS, each of these layers can be fabricated in a specific technology approach.

Some of the most attactive MAPS options consist of CMOS with an epitaxial layer and SOI with CMOS. CMOS with an epilayer is an available commercial process, which has been widely researched and used with many feature sizes. Many prototypes developed with this technology are actively studied. SOI with CMOS has only been available for scientific applications for a few years. SOI was developed for the digital electronics market and not for high energy sensor research. There are some collaborations that are studying the performance, radiation hardness, with a real possibility of using SOI for particle detectors.

1.3 Belle Experiment

The Belle Experiment is a particle physics experiment conducted by the Belle Collaboration that investigates Charge conjugation Parity (CP)-violation ef-

fects at the KEK Laboratory in Tsukuba, Japan. Among the Belle experiment relevant results include the 1st observation of CP violation outside of the kaon system and observations of a number of new particles including the $X(3872)$. The Belle experiment operates at the KEKB accelerator, the world's highest luminosity particle collider. The instantaneous luminosity exceeds $1.7 \times 10^{34}\text{cm}^{-2}\text{sec}^{-1}$. The integrated luminosity is greater than 700fb^{-1} (In excess of 600 million $B\bar{B}$ meson pairs). Most data is recorded on the $Upsilon(4S)$ resonance, which decays to pairs of B mesons (particles containing b-quarks). About 10% of the data is recorded below the Upsilon(4S) resonance in order to study backgrounds. In addition, Belle has carried out special short runs at the $Upsilon(5S)$ resonance to study B_s mesons (particles with a b quark and s anti-quark) as well as on the $Upsilon(3S)$ resonance.

1.4 Motivation for the Upgrade of the Belle Experiment using MAPS

The KEKB accelerator started operation in 1999 at KEK. The Belle experiment is one of the two e^+-e^- B-factories, the other being located at SLAC. To obtain the important results mentioned above, the silicon vertex detector has played an important role. During the summer of 2003, the Belle Silicon Vertex Detectors (SVDs) was upgraded to a second generation one, SVD 2, to obtain improved performance and radiation hardness. In order to search for physics beyond the standard model in rare B decays, 100 times or higher luminosity is required.

	SVD1	**SVD2**
Number of layers	3 (30-60 mm)	4 (20-88 mm)
Number of channels	~82k	~110k
Coverage	23°-139°	17°-150°
Silicon	102 DSSD, 0.2m^2	246 Double Sided Silicon Detector (DSSD), 0.5m^2
Readout	VA1chip	VA1TA chip

Table 1.1: The most important characteristics of the SVD of the Belle Experiment.

A Super KEKB factory, running at the luminosity of $5{\times}10^{35}\text{cm}^{-2}\text{s}^{-1}$, is the next goal. In this case, the accelerator has be to modified substantially, increasing backgrounds in the interaction point region. Therefore, upgrade plans are being considered for the vertex detector.

KEKB vertex detector performance can benefit from the use of a pixel detector in its innermost layer because of the high levels of occupancy, and the current SVD will not work at the higher luminosity. The levels of occupancy of SVD2 are on the order of ∼10% (200Krad·yr^{-1}) for the first layer. The nominal current luminosity is L∼1.5×10^{34}cm^{-2}s^{-1} but the luminosity is expected to increase up to L∼5×10^{35}cm^{-2}s^{-1}. With a luminosity of 5×10^{35}cm^{-2}s^{-1}, a background level 20-50 times higher than that currently seen has been estimated. SVD3 should also have good vertexing performance under such high background conditions.

Although the interesting physics trigger rate will be around 1 kHz, the Level-1 trigger rate is estimated to be 30 kHz due to background particles. The SVD3[1] readout system should operate with small deadtime under such high trigger rates. This will increase the occupancy and the radiation dose received by the SVD, making a conventional solution with Si strips no longer work. Since the improvement in vertexing is not mandatory for observing CP-violation in the gold-plated $J/\psi K_S$ mode, it was not aggressively pursued. An improved vertexing will give better continuum suppression thereby improving the background analysis. To improve the B-factory vertexing measurement the key point are move closer to the beampipe and to reduce the sensor material, discarding the usage of hybrid pixels as they are not compact nor thin enough.

Radiation damage is a major problem because of the proximity to the interaction point. Radiation hardness is one of the reasons that CCD technology is not a viable option for the Super-B factory. MAPS presents better radiation hardness than CCD s detectors. MAPS technology is based on commercial CMOS technology, that is the basis for the development shown by, among others, digital cameras.

The total requirements of our system are the following: low occupancy (that defined the technology choice to MAPS), fast read-out speed, Mega-Gray (multy Mega-Rad) radiation hardness, thin sensor and maintain good noise performance for a full-sized detector. The evolution of the prototypes presented in this dissertation are the following. CAP1 was a proof of concept, where the basic functionality of the 3T cell was tested. In CAP2 the speed was improved by introducing a pipelined read-out (introducing various storage cells per pixel), with a 10μs frame

[1] SVD2.5 introduced striplets, although it was never built. SVD3 is going to be SVD5.

acquisition speed. CAP3 took the risk of trying to proof the performance of a full-size detector with 5-deep double pipeline per pixel. CAP3 showed various design flaws, like high capacitive bus lines which slowed down the output signal to an undesirable low rate. CAP3 was tested with a laser set-up and was able to detect the laser location. After further investigation, the noise levels and speed limitations indicated this architecture approach would be unable to meet all the requiref speed specifications.

Up until CAP3, the design approach was simple and well stablished by literature. In CAP4, it was decided to work with new technological approaches. The first challenge was to include digital and analog circuitry into a pixel of small dimension. As example, the binary architecture had a pixel size of $30\times25\mu m^2$, electrode area of $3\times3\mu m^2$, and a total transistor count of 50. This Binary design is able to compare, at a pixel level, the signal from the electrode to a threshold value. Whenever a rising edge signal is detected, a digital output signal is generated and transfered to left and right neighboring pixels. Once the signal is transferred along the row of pixels, it is sent to an Field Programmable Gate Array (FPGA) which sends the data to the computer for processing, recording and display. This architecture for the pixel design is new and novel, having never been presented previously, and the results from this dissertation show the possibility of using this new approach with an epitaxial layer for very high occupancy rates. The other two designs included in the prototypes were not successful, and they presented design flaws that did not allow to obtain any valid data.

The next prototype, CAP 5, was fabricated using SOI technology. This technology was available through an R&D collaboration with KEK and OKI. The results presented were obtained with two prototypes that were designed at the Instrument Development Laboratory at the University of Hawaii - Manoa. A third set of results are from a test structure fabricated by Prof. Arai's group at KEK. The results obtained from Prof. Arai's results show limitations with the technology as fabricated. Unfortunately the threshold variation of the transistors used in the design was too high, the run was considered valid with a variation of 50%, and that made the behaviour of the analog circuits included in the design not work properly. The core of each pixel includes a comparator, registers, and basic digital cells. The final results from the comparator showed it failed for two reasons: threshold

variation and back gate effect. These results are also seen for the prototype X-ray detector. This X-ray prototype is based on a traditional APS architecture with a programmable threshold voltage comparator (with 5bit Digital-to-Analog Converter (DAC)) and four double storage cells. This structure work for the basic 3T structure, but the analog-digital circuitry does not work properly. All these results can also been seen for the results measured from the chip Test Element Groups (TEGs), designed and fabricated by Prof. Arai, where the values obtained for the threshold voltages show high variations.

1.5 Description of the organization of the dissertation

The organization of this dissertation is the following:

- **Chapter 2** should be read with 3 different objectives. The first objectives is to become familiar with the technologies available, as well as how they have been used and will be used in a particle physics environment. This introduction can be used also to obtain an historical background of the pixel detector field and see the most important technological approaches in the coming years (see Section 2.1, Section 2.2 and Section 2.3). There are two Sections dedicated to the technologies used for the work developed in this dissertation, they are Section 2.4 that explains the details of CMOS technology with epitaxial layer, the other is found at Section 2.5 that explains the details of SOI technology[2].

- **Chapter 3** describes the most important physical processes that are involved in the interaction of radiation with matter in Section 3.2 (in the case of detectors, silicon is the material that is used to develop the detectors, and Section 3.1 includes its characteristics more relevant). The interactions of radiation will be explained for different cases: for heavy charged particles in Section 3.3, electrons in Section 3.4 and photons in Section 3.5. The next physical aspects to analyze are the energy needed for charge carrier generation in Section 3.7 and multiple Coulomb scattering in Section 3.8.

- **Chapter 4** describes the environment and characteristics at the KEKB as well as the main characteristics of the B-Factories in Section 4.1. After this

[2]This Section explains with great detail the electrical characteristics of the SOI technology/process. This detail is not given about the CMOS with epitaxial layer because the characteristics are basically the same as typical CMOS technology/process

introduction the description and results obtained with both CAP 1 (in Section 4.2) and CAP 2 (in Section 4.3 are included.

- The next 3 chapters will describe 3 members of the family that have been added in the last years. **Chapter 5** is used to explain the architecture of CAP 3 (in Section 5.1 and to describe all the testing results obtained with the laser set-up (in Section 5.2 and Section 5.3). **Chapter 6** is used to explain the architectures of CAP 4. In this chapter the laser testing set-up (in Section 6.1 is explained with more detail. The COBI/PETRA board are introduced in Section 6.2, as a part of the new environment used for the development of the CAP family. Then, the CAP 4 architecture will be explained generally in Section 6.3, to enter into more detail about the 2 architectures included in this chip: the Wilkinson in Section 6.4 and the Binary read-out in Section 6.6. The last chapter, **Chapter 7** describes CAP 5 related results. It starts describing the OKI SOI process used in Section 7.1, including the Technology Computer Aided Designs (TCADs) simulations perfomed for this process in Section 7.2. The first results are found in Section 7.3, where the chip TEG is used to characterize the transistors available with this process at different Back Gate Voltages. The last two Sections, describe the results obtained for CAP 5 in Section 7.4 and the X-ray prototype in Section 7.5. The X-Ray detector is included here to show all the results obtained for the SOI process, which were worse than expected because of process parameter spread.

Chapter 2

Particle Detection and Tracking

Chapter 2 describes the basics of Particle Detection and Tracking. This chapter includes three parts divided in five sections. The first part is a technology review and it includes the first three Sections. The first Section is a technology review which gives a review of the technological approaches that have been used to detect and track particles in the HEP field. This technological review section includes historical technologies to give an understanding evolution of the field, and put current technologies in a historical context. The most common technologies used today, the hybrid and monolithic (and semi-monolithic) detector technologies are explained in detail. The next sections detail the manufacturing process used in modern detector construction, that is CMOS with epitaxial layer and CMOS on SOI. The next section explains the principles of detector physics from a semiconductor view and describe how the detector works. This description includes an explanation of the p-n diode, generation and detection of charge, along with sources of noise. The last part provides a brief summary of the different pixel detector architectures that are being used in monolithic detectors. This section is a good summary of what have been the new and best approach in the detector research to overcome the limitations of speed and noise that can be present in a collider environment.

2.1 Technology review

Particle detectors used for HEP applications are based on the same principles that allow for the operation of imaging applications with pixel detectors, which are described in section Section 2.6. High energy physics detectors are based on the same principles as imaging applications with pixel detectors, wich were briefly described in Section 2.6.2. The first silicon pixel devices for HEP s were built using drift detector and CCD technology. They have been joined by two new technologies

[2]: MAPS and HAPS. The main difference between MAPS and HAPS are the design requirements and operation conditions, which are detailed in the corresponding sections. Particle detectors used in HEP demand strict spatial resolution and timing constraints, primarly defined and constrained by the need for other detector structures present around the detector device. HEP assume typical charges collected, even after high radiation doses, of a few thousand electrons for very thin devices. For typical silicon strip sensors, that have a 300μm thickness on average, the charge collected is assumed to be about 23,000 electrons. Spatial resolution can go from few μm in the best case to pixels about 100μm. In vertex detectors, the need of very thin detectors is mandatory to obtain highly specific momentum/Energy information. To develop these detectors, silicon is the material of choice, which makes design easier as silicon is well studied and understood. Silicon is a good material due to the ability to shape internal electric fields dependant upon the dopant concentration defined. In the case of a high radiation environment, a different material or approach is needed, like Chemical Vapour Deposition (CVD)-diamond or silicon with a radiation hardened design.

CCD s pixel detectors present an active collection depth 15μm, which provides a small charge signal shifted to an edge of the device. The readout presents challenges to achieving low noise. Low temperatures must be maintained, as well as slow clocking speed to avoid increasing noise. These disadvantages make CCD s unsuitable for high rate applications. CCD s are used ideally in lower rate applications, such as some fixed target experiments. HAPS are a strip sensor with the strips segmented into pixels. To read-out the collected charge, the read-out chip will have the same structure as the sensor. MAPS use the same thin active layer as CCD (the epitaxial layer) but instead of shifting the signal, the charge is collected and processed at the pixel level.

2.1.1 Drift Detectors

Silicon Drift Detectors (SDD) were proposed in 1983 by Gatti and Rehak [3]. A SDD consists of a thin cylinder of fully depleted silicon in which an electric field, parallel to the surface, drives electrons towards the anode situated at the center. The field is created by many concentric ring electrodes and the anode is directly connected to an integrated Field Effect Transistor (FET) acting as a current

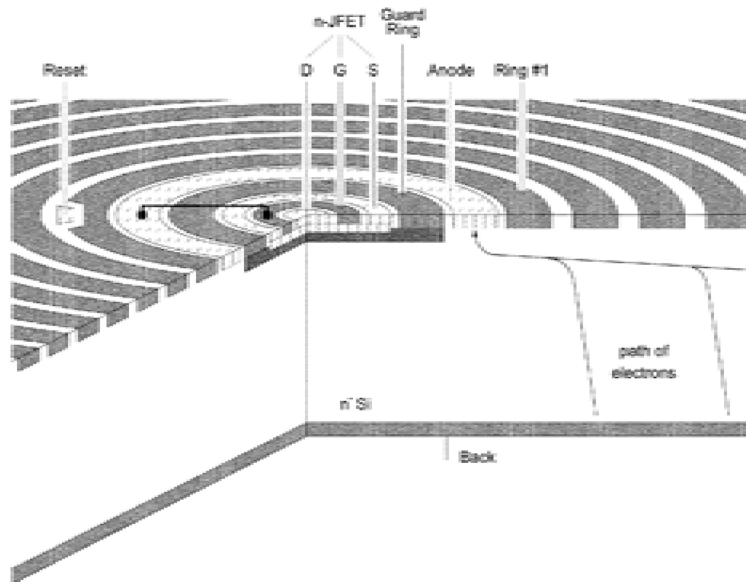


Figure 2.1: Geometry of a radial silicon drift detector.

preamplifier. SDD s have a small anode capacitance which is practically independent of the total area of the device. This characteristic allows shorter rise time and large amplitudes of the output signal for a given amount of collected electrons. Due to their high position resolution, SDD s are used as tracking and charged particle detectors. SDD have been developed in different geometries depending upon their desired implementation. SDD were used in the past at the NA45 (CERES) experiment at the Super Proton Synchroton (SPS) at Centre Européenne pour la Recherche Nucléaire (CERN) [4] (with 3" and 4" cylindrical detectors). They have been designed and built for the Star experiment at Relativistic Heavy Ion Collider (RHIC) at BNL[5] and for A Large Ion Collider Experiment (ALICE) experiment at the Large Hadron Collider (LHC) at CERN [6], and are the subject of intense research. SDD have been used for X-Ray applications [7] as well, showing their versatility and usefulness.

2.1.2 CCD Detectors

In 1969 Smith & Boyle, working at Bell-Labs, described the basic structure and principles of operation of the CCD when they invented the buried channel in 1974 [8]. These developements lead to the fabrication of the first solid-state video camera with suitable quality for broadcast television in 1985. CCD s made its appereance in the astronomy field at 1983, when the first CCD was mounted on a

telescope. CCD s are used in the Hubble Space Telescope [5] and continue to be actively researched.

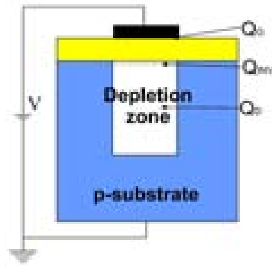


Figure 2.2: CCD structure.

Figure 2.3: Three phase CCD structure.

The operational principle of CCD s is to store the information as electrical charge in potential wells created by overlaying electrodes separated from the semiconductor by a thin insulating layer (see Fig. 2.2). Under the control of external voltages applied to the electrodes, the charges associated with a given storage cell can be shifted through the semiconductor. The most conventional scheme to move these charge packets is the three phase clock process; three clocks with identical shapes and different phases (see Fig. 2.3). Scientific CCD s have been used extensively in ground and space-based astronomy because of their high detection efficiency, low noise, good spatial resolution, low dark current, and high charge transfer efficiency. CCD s are fabricated in a low-resistivity substrate and use the same detection principle as MAPS (see Section 2.3), leading to a similar Signal-to-Noise Ratio (SNR) and spatial resolution factors. CCD s however show poor radiation resistance when compared to MAPS [9]. The first CCD-based vertex detectors were used for studies of charm production at CERN in 1984 (NA32 experiment [10]). They were also used at the VXD2 vertex detector at the Stanford Linear Collider (SLC) (1992) [11], and at the VXD3 upgrade vertex detector. The VXD3 used 96 large CCD s, which included 307 Million pixels (1996) [12].

2.2 Hybrid Detectors

A Hybrid Detector is formed by a sensor and a Front-Ends (FEs) chip, which are connected through various techniques, such as bump bonding and flip-chip technology). This detector architecture is used in all LHC-collider-detectors (AL-

ICE [13], A Toroidal LHC ApparatuS (ATLAS) [14], and Compact Muon Solenoid (CMS) [15] and Large Hadron Collider beauty (LHCb) [16]) and in some fixed target experiments (NA60 [17] at CERN and BlueTrait Event Viewer (BTev) [18] at Fermilab) using pixel areas that range from 50μm $\times$ 400μm for ATLAS [19] or 100μm $\times$ 150μm for CMS [20]. The design of the front-end pixel electronics has the following requirements: low power ($< 50\mu$W per pixel), low noise and threshold dispersion (together < 200e), zero suppression in every pixel, on-chip hit buffering, and small time-walk to be able to assign the hits to their respective LHC bunch crossing. These requirements have been fulfilled using deep submicron technologies [18]. Different ideas and projects are evaluating using Hybrid Pixels, like HAPS, MCM Sensor, Active edge 3-D Silicon or Diamond Pixel Sensor.

HAPS HAPS have been used, among others, in the CMS and the ATLAS experiment. The ATLAS experiment [21] uses a pixel size of $50{\times}400\mu$m. HAPS were proposed for the Tera-electronvolt Energy Superconducting Linear Accelerator (TESLA) linear collider [22], [23]. In the TESLA application[1], capacitive coupling between pixels is used to obtain smaller pixel cells, with a larger readout pitch resulting in interleaved pixels and a resolution of 10μm with pixel readout pitch of 200μm.

MCM Technology deposited on Si-substrate (MCM-D) A multiconductor layer structure is built up on the silicon sensor. MCM-D can use bump-bonding for all connections, making final modules robust. This option was used for the R&D work for the ATLAS pixel detector project, although not chosen for the final design [24] [25]. The R&D sensor for ATLAS has a sensor cell size of $422.25{\times}52.25\mu$m with 2880 read-out channels and a total area of 16.4×60.4mm^2.

Active edge 3-D silicon was proposed [26] for applications which require a large active/inactive area ratio. An active edge 3-D detector is obtained by processing the n+ and p+ electrodes into the detector bulk. Charge carriers drift inside the bulk parallel to the detector surface over a short drift distance of 50μm. The main advantages come from the fact the electrode distance is short (50μm) in comparison to conventional planar devices at the same total charge, resulting in a fast (1-2 ns) collection time, low (< 10V) depletion voltage and a large active/inactive area ratio

[1] TESLA linear collider is no an active project, which have been cancelled.

of the device, but the major advantage is its radiation hardness. 3-D detectors are being analyzed for the upgrade of the LHC [27], [28], [29], where the luminosity will be increased by a factor of 10. This upgrade will reduce the bunch crossing time to 12.5ns and increase the proton intensity, forcing the detector radiation tolerance to be proportionally scaled upward.

Diamond pixel detectors are a potentially very radiation hard material that has been explored in the framework of the R&D collaboration RD42 at CERN. This development was applied to the ATLAS pixel detector R&D and it was operated as single-chip modules in testbeams [30]. A spatial resolution of 22μm has been measured with 50μm pixel pitch, compared to about 12μm with Si pixel detectors of the same geometry and using the same electronics. Finally, the fast response and radiation tolerance of polycrystalline CVD material has also proven ideal for beam background monitors. B/B-bar (BABAR), Belle, ATLAS and CMS experiments are developing their own diamond-based beam condition monitors.

2.3 Monolithic and Semi-Monolithic Pixel Detectors

Monolithic pixel detectors include amplifying, logic and the detecting sensor as one entity. The main characteristics are very low material per detector layer, small pixel sizes ($<20\mu\text{m}\times20\mu\text{m}$) and a good rate handling capability (80 hits/mm^2/ms). Among the developments of monolithic or semi-monolithic pixel devices the following classifying list is presented.

Non-standard CMOS on high resistivity bulk The first monolithic pixel detector successfully operated in a particle beam [31] used a high resistivity p-type bulk p-i-n detector. The junction was created by a n-type diffusion layer, but the technology is nonstandard and non-commercial. This approach has been used recently in *Mimosa4* (4 arrays of 64×64 pixels with a pitch of 20μm) and *Successor2* (4 arrays of 32×32 pixels with pitch of 40μm)[32] obtaining Minimum Ionizing Particle (MIP) detection efficiency >99.5% for *Mimosa4* with lifetime limit close to 10^{12} n/cm^2 and at least several hundreds of kRad for total ionizing dose absorption. The main advantage is based on the fact that a relatively thick depletion

region can be obtained, a large charge signal is generated and signal-to-noise ratio in excess of 100 can be obtained [9].

CMOS technology with charge collection in epi-layer Commercial (and cheap) CMOS technologies use low resistivity silicon (thin layer, $\sim 10\mu$m, of lightly doped silicon) with an epitaxial silicon layer (heavily p++ doped thick, $\sim 500\mu$m, supporting structure)[33], [34], [9]. The generated charge is kept in the epi-layer by potential wells at the boundary and reaches an n-well collection diode by thermal diffusion. The signal charge is tipically small (<1000e) and therefore low noise electronics are needed. Full CMOS circuitry in the active area is not available (only nMetal Oxide Semiconductor (MOS)) to keep fill factor 100%.

CMOS on SOI Pixel sensors with full CMOS circuitry have been developed using the SOIs technology. This option allows high resistivity bulk material (there have been approaches using low resistivity substrate in applications such us active pixel light sensors [35]), connecting the bulk by vias, and allowing full charge collection with CMOS electronics. The SOI approach was pursued by the CERN RD19 collaboration [36] using Separation by IMplantation of OXygen (SIMOX) and a Zone-Melting Recrystallization (ZMR) process, although it presented problems related to the kink non-linearity and back-gate effect on the top layer Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET). References [37], [38] used Bonded and Etched-Back Silicon-On-Insulator (BESOI) technique and back-illuminating the sensor to reach the active volume, although the cell pitch was rather large, 100μm, and the cells used a classical serial analog organization, without including a common readout amplifier nor shift register. It showed the sensitivity of the direct charge carrier generation with a pulsed infrared laser. Reference [39] uses a SIMOX process to develop a matrix of 8×8 diodes, with a cell dimension of $140\times122\mu\text{m}^2$. The readout is based on the rolling shutter technique, where rows are both reset and read-out one by one in the same sequence and at the same speed thereby allowing external CDSs. This structure was tested with an infrared laser, showing a linear response for a range up to 45MIP s and with a ^{90}Sr beta source. Reference [40] shows the results obtained by Silicon on Insulator Technologies (SOITEC) process, showing fine segmentation, low material thickness, good radiation hardness and low power consumption, for pixels $20\times20\ \mu\text{m}^2$ size. This collaboration provided additional results [41], [42], [43] that will be further detailed in this dissertation,

including the effect of irradiation on the different threshold voltage values. This work was made possible thanks to a R&D collaboration between KEK and OKI Semiconductor.

Amorphous silicon on standard CMOS ASICs Hydrogenated amorphous-Silicon (a-Si:H) is deposited as a film on top of CMOS Application-Specific Integrated Circuit (ASIC) electronics, acting as the sensor material [44], [45]. The signal charge collected in the $<30\mu$m thick film is in the range of 500-1500 electrons. The radiation hardness of these detectors appears to be very high $>10^{15}$cm^{-2} due to the defect tolerance and defect reversing ability of the amorphous structure and the larger band gap (1.8 eV). The carrier mobility is very low and only electrons contribute to the signal. The potential advantages are small thickness, radiation hardness, and low cost. The main disadvantage is that the leakage current at high reverse biases turns out to be an important parameter limiting the performance. This is based on the quality of the deposition of the a-Si:H layers with minimal defect density [46].

Amplification transistor implanted in high resistivity bulk, *DEPFET* pixel sensors The DEPFET combines detection and amplification within one device [47][2]. It is based on the sideward depletion as used in the semiconductor drift chambers [48]. Intrinsic advantages of the DEPFET device are the amplification of the signal charge at the position of its generation thus avoiding any charge transfer where losses could occur. The entire bulk is depleted and sensitive to incident radiation. The main advantage of the device is its very small input capacitance that provides a very low noise operation even at room temperature. DEPFET pixels was one option being studied for the TESLA Linear Collider [49].

Deep n-well sensor The SLIM5 Collaboration has proposed the use of the triple well option of a commercial CMOS process [50] to improve the readout speed of these devices while also increasing the sensitive element area. This allows for the complete signal processing chain at pixel level (charge preamplifier, shaper, discrim-

[2] A MOS is integrated onto a detector substrate, below the transistor a potential minimum for electrons is created underneath ($\pm 1\mu$m) the transistor channel, it can be considered an internal gate of the transistor. A particle entering the detector creates e-hole pairs in the fully depleted silicon substrate. The holes drift into the rear contact of the detector. Electrons are collected in the internal gate where they are stored. The signal charge leads to a change in the potential of the internal gate, resulting in a modulation of the channel current of the transistor.

inator and a latch). The deep n-well (DNW) of the triple well process is used as a charge collecting electrode and also contains part of the front-end stage. This is physically overlapped with the area of the sensitive element, allowing more complex in-pixel readout electronics. Furthermore, since the voltage gain is now determined by the feedback capacitance of the charge preamplifier, the size of the collecting electrode can be increased (up to about 900 μm^2 in a pixel cell with a 50 μm pitch).

The second generation of the chips, APSEL2, shows good sensitivity to electrons from a ^{90}Sr source, as well as improved pixel noise and threshold dispersion with respect to the previous prototype chips. APSEL3 has improved noise figures, power consumption and charge collection efficiency. Residual crosstalk has been reduced to the level of the pixel noise using one of the metal layers as a shield between the digital lines and the sensor underneath. This approach is very promising to develop a thin pixel system with a fast sparsified readout for applications in silicon vertex trackers at future colliders as the SuperB Factory or the International Linear Collider (ILC).

One particular innovative approach is ***3D packaging*** of sensors and different layers of electronic circuits, connected through vertical interconnects [51]. The 3D stacks can be built using wafer-to-wafer or die-to-wafer bonding with the technology of each layer being optimized for its function. This approach is not likely to be practical in the near term.

2.4 Epitaxial Substrate in IC designs

An epitaxial layer is a semiconductor layer having the same crystalline orientation as the substrate on which it is grown. It is used in silicon-based manufacturing processes for Bipolar Junction Transistor (BJT) s and modern CMOS, but it is particularly important for compound semiconductors such as gallium arsenide. Manufacturing issues include controlling the amount and uniformity of the deposition's resistivity and thickness, the cleanliness and purity of the surface and the chamber atmosphere, the prevention of the typically much more highly doped substrate wafer's diffusion of dopant to the new layers, imperfections of the growth process, and protecting the surfaces during the manufacture and handling.

Epitaxial substrate starting material is preferred because these wafers permit Integrated Circuit (IC) designs that are significantly more robust against latch-up than designs using bulk silicon wafers. On the other hand, analog designs require good isolation between circuits to achieve low noise performance. A bulk substrate, with its high bulk resistivity, acts as a filter to attenuate high frequency noise, rapidly minimizing coupling to surrounding circuitry. Epitaxial substrates have a low bulk resistivity material underneath the epitaxial layer which is able to couple noise more efficiently to nearby circuits. The epitaxial substrate will cause spiral inductors to have lower Q due to the close proximity of the lower resistivity bulk substrate. As a result of these design issues, most foundries that advertise mixed signal IC fabrication will offer either epitaxial wafers or bulk wafers as options to please both digital designers and analog designers.

2.4.1 Use of epitaxial layer in particle detectors

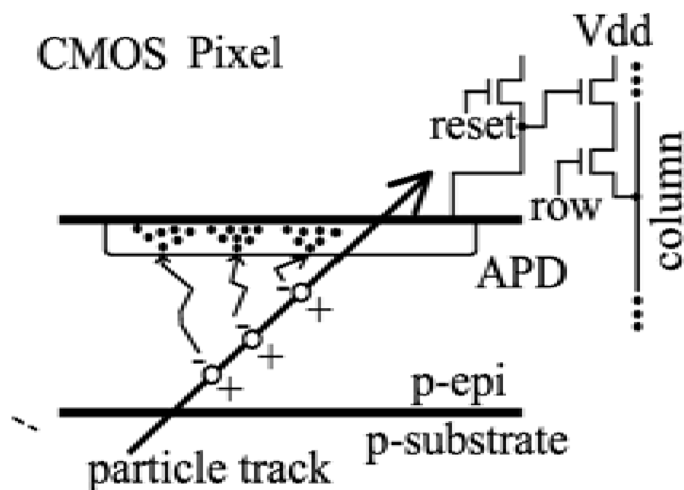


Figure 2.4: Charge generation from an incident high-energy particle.

CMOS MAPS are charged particle tracking devices (see 2.4), integrating on the same silicon substrate radiation sensitive detector elements with front-end readout electronics. In this substrate, a thin ($\sim 10\mu$m) lightly p- doped silicon epitaxial layer is grown on heavily p^{++} doped thick ($\sim$500μm) supporting structure. On top of epitaxial layer, structures of n^{+} and p^{+} wells are formed, providing a surface for CMOS transistor implantation (Fig 2.5).

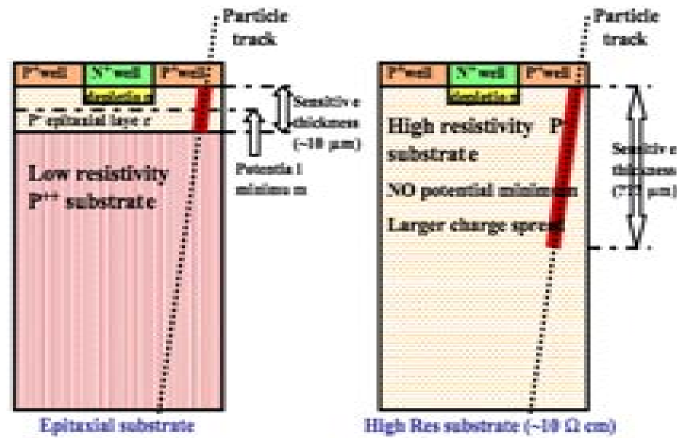


Figure 2.5: Cross section of silicon wafers used for the fabrication of CMOS monolithic pixel sensors. On the left, structure of epitaxial type wafer is shown. On the right non-epitaxial, high resistivity wafer is presented. [32]

The epitaxial layer is used as a detector radiation sensitive volume, with a diode N_{well}/P_{epi} working as a charge collecting element. The detector is only partially depleted in the vicinity of the Nwell/Pepi junction (1-2 μm in depth), and the charge is collected mainly through thermal diffusion. However, due to the particular doping profile ($P_{++substrate}$ - P_{-epi} - P_{+well}), there is a potential minimum in the middle of epitaxy, limiting volume spread of diffusing electrons created. The height of the potential barriers is of the order [9],

$$V = \frac{kT}{q} ln \frac{N_{sub}}{N_{epi}} \tag{2.4.1}$$

where k is the Boltzmann constant, q is the electron charge, T is the absolute temperature and N_{sub} and N_{epi} are, respectively, the doping of the substrate and the epitaxial layer. These generated electrons may move only along the plane parallel to the surface and are rapidly collected when passing close to the collecting diode junction, with a typical collection time of the order of 100 ns. The detector active volume is limited in depth to the epitaxy layer only, because of the short lifetime of charge carriers inside a p++ substrate[3]. Therefore, a total amount of available charge created by an impinging minimum ionizing particle amounts to a few hundreds electrons only, for a typical epitaxy thickness on the order of 10μm.

[3]The substrate is formed of *low-quality* silicon. The recombination time is relatively short, which explains way just a small fraction of the charge created may be able to drift towards the epitaxial layer and be seen by the electrodes.

In [52], [9] a spatial resolution of 1.5μm, a detection efficiency close to 100% and a signal-to-noise ratio >30 was obtained with the Minimum Ionising Particle MOS Active Pixel Sensor (MIMOSA) family (MIMOSAI and MIMOSAII). Radiation studies were performed showing an increase of leakage current with proton, neutrons and soft X-ray irradiation. For example, MIMOSAI showed an individual pixel noise Equivalent Noise Charge (ENC) below 20e$^-$ and the Signal-to-Noise ratio for 5.9keV X-ray and MIP of the order of 30[4].

2.5 SOI Technology

From all the monolithic solutions, the one chosen for the work presented here, is the SOI technology. The SOI concept is very old, although the commercialization of this technology is new and growing because of high-speed and low-power applications. SOI technology becomes an attractive option because of the fundamental physical limits of bulk-Si technologies (decreasing carrier mobility due to impurity scattering, increasing tunnel current as gate insulator is thinner, and increasing leakage p-n as junction is shallower) that make conventional scaling less feasible. These disadvantages are generally forcing the operating voltage to be set higher than was expected to achieve desired speed performance.

SOI technology has lower capacitance, which enables a lower supply voltage to be used. Moreover, it also shows good radiation hardness, ability to withstand high temperatures and handle high voltages. On top of that, it is a very flexible technology that allows the designer to define the properties of the substrate independently from the device layer thanks to the presence of the insulator. SOI technology became a feasible technology with the appeareance of high-quality bonded SOI wafers in the late 1990s.

SOI wafer technology consists of a silicon film over an insulator layer (Buried Oxide Layer (BOX)) on a silicon substrate. In standard integrated circuits, the top silicon film (or device layer) is used for manufacturing of electronic devices, while the bottom silicon substrate (or support or handle wafer) acts only as a mechanical support (see Fig. 2.10 for a schematic). In detector applications, the substrate is intended to have high resistivity and act as a particle sensor, be fully

[4] These results were for a temperature of -20°C, not room temperature.

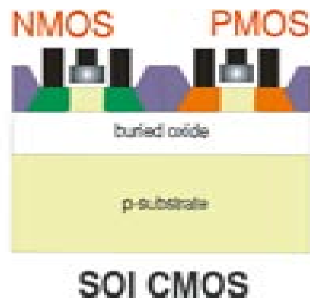


Figure 2.6: Conventional integrated circuit done in SOI technology.

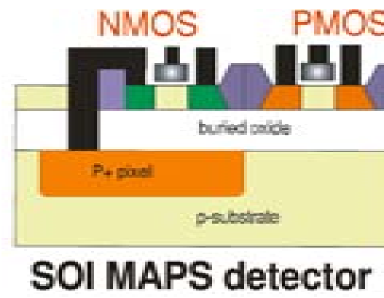


Figure 2.7: Radiation detector produced in SOI technology

depleted and monolithically coupled to the readout electronics integrated in the silicon film over the buried oxide. The readout electronics immunity to Single Events Effects (SEE) is expected to benefit from the reduction of ionizing path length in the active layer over the BOX. The detector is realized in a thick, high resistivity wafer and has a conventional p-n junction and the readout is created in the thin low resistivity active layer.

2.5.1 History and Description of Wafers using SOI Technology

The idea of developing semiconductor devices in a thin silicon film that were mechanically supported by an insulating substrate has been around for several decades. In fact, the first description of an Insulated-Gate Field-Effect Transistor (IGFET) appears in a patent from Lilienfield at 1926 [53], that would become the silicon MOSFET. The MOSFET transistor consists of structure very similar to an SOI device. The technology at that time was unable to produce operating devices and was temporary forgotten with the success of the discovery of the bipolar transistor at 1947.

It was in 1998, with the IBM's development of the Power PC MPU, that mass production of SOI chips was finally undertaken.

The first SOI wafers for integrated circuits were produced using SIMOX in 1978 [54]. This method provides high quality SOI wafers, but the wafer cost is relatively high due to the necessity of large oxygen implantation doses. Another method, called Smart-Cut [55], is based on wafer bonding. An SOI wafer fabricated using the Smart-Cut method is called a UNIBOND wafer, by a process that is described in Fig. 2.8. The SOI devices use the upper Si layer for circuit implementation and the bottom wafer as a mechanical support structure. Using the UNIBOND

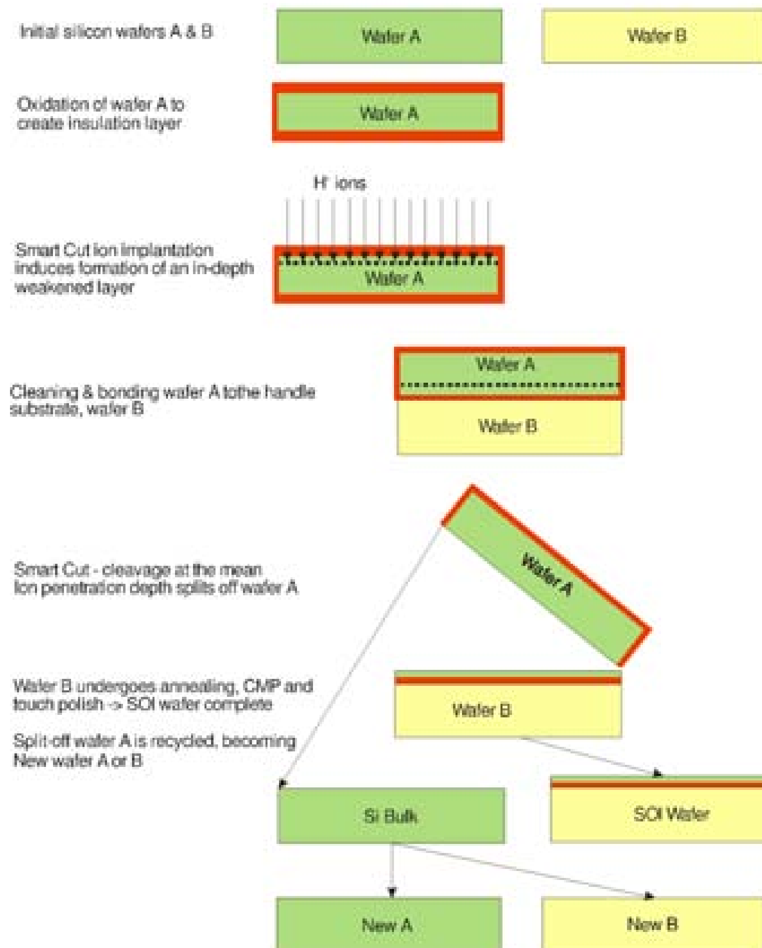


Figure 2.8: Process description for the wafer fabrication using the Smart-Cut method.

method it is easy to bond a low-resistivity Si wafer (for CMOS implementation) with a high-resistivity Si wafer (for the radiation sensor).

SIMOX is a mature and well established method of the SOI wafer production based on the implantation of oxygen ions below the surface of a silicon wafer at the temperature of 500°C to 600°C. The oxygen implantation is followed by high temperature annealing, which leads to the formation of a BOX and heals most of the silicon crystalline damages caused by the implantation. In modern SIMOX techniques, multiple implantation and annealing steps are usually performed and BOX growing is fulfilled by Internal Oxidation (ITOX) [56]. The major challenges in the SIMOX process are formation of the BOX layers with adequate dielectric characteristics and preservation of the single crystalline nature of the silicon film. The development of low dose SIMOX processes permit achieving high quality device layers with low dislocation densities resulting in formation of thin buried oxide layers (typically 100nm to 150nm), which may not be sufficient for the realization of the proposed monolithic active pixel detectors due to possible cross-talk between the readout electronics and the detector active volume. Another problem associated with the SIMOX process is the risk of formation of silicon pipes in the buried oxide. Silicon pipes are continuous regions of silicon extending through the BOX layer. They may cause an undesirable electrical short between the device and support layers of the SOI wafer.

Wafer-bonding is an alternative method of SOI wafer production. During this process, a thermally oxidized silicon wafer is bonded to another oxidized or bare silicon wafer. At room temperature, the flat and smooth surfaces of the wafers are mainly connected by Van der Waals forces or hydrogen bonds and water molecules. To obtain better mechanical strength, the bonded pair is subsequently annealed at elevated temperatures, up to 300°C, and the water initially trapped between the bonded surfaces diffuses through the oxides to the silicon-oxide interfaces and an additional thin oxide layer is produced. Further heating up to 800°C removes any remaining water from the bond interface. As the temperature increases to 1100°C, the complete closure of the wafer interfaces occurs. After the fusion process, one of the bonded wafers is thinned down to form the thin silicon film in which the electronic devices can be produced.

The most common methods are: grinding and chemical-mechanical polishing, back-etching (BESOI), plasma assisted chemical etching, bond and selective etching of porous silicon (e.g. ELTRAN ® process) or implant enhanced wafer splitting (e.g. Smart Cut ® technique). Since in the wafer-bonded substrates, the device layer and the support layer originate from two separate silicon wafers, specific resistivity of the latter can be used, taking into account the specific aspects of the radiation detector implementation. The same materials for hybrid detector production can be used as the handle wafers, making the wafer-bonding technique especially attractive for manufacturing of MAPS realized in this SOI technology. The bonding method is responsible for the more flexibility in the choice of the desired buried oxide and silicon film thicknesses.

2.5.2 Comparison of Bulk CMOS *vs.* SOI CMOS technology

Fig. 2.9 and Fig. 2.10 can be used to compare the 2 silicon wafer technologies, bulk and SOI). It can be seen that in bulk technology each transistor is isolated by reverse-biased p-n junctions in a well structure. In SOI technology, each transistor is completely isolated by the oxide insulator, decreasing the parasitic effects in the SOI transistors. The presence of the BOX layer gives the SOI devices

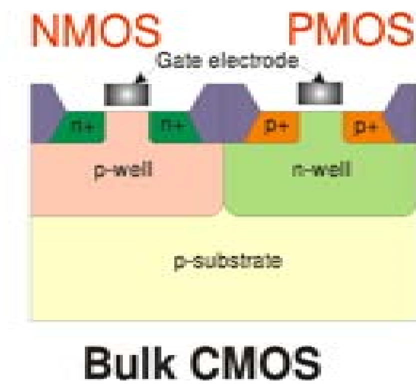


Figure 2.9: Cross section of bulk CMOS transistors.

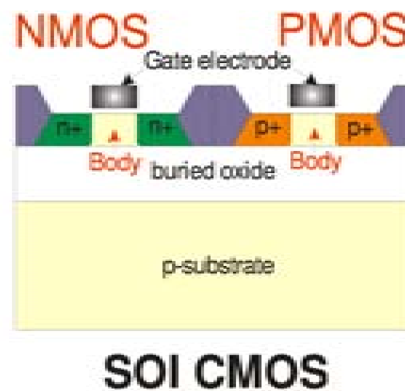


Figure 2.10: Cross section of SOI CMOS transistors.

advantages over the bulk-Si. A summary of the advantages of SOI over bulk-Si is:

1. **Negligible drain-to-substrate capacitance** because of the high dielectric constant of SiO_2, switching speeds are improved. In bulk MOS, the parasitic drain/source-to-substrate has two capacitance components: capacitance be-

tween drain and substrate and capacitance between drain and channel-stop implant under field oxide. In SOI devices, the junction capacitance has only one component: the buried oxide and the underlying silicon substrate, and is lower than the junction capacitance of a bulk MOSFET. The drain capacitance of an SOI MOSFET can be obtained from the MOS capacitor theory and is given at Equation 2.5.1

$$C = \frac{C_{BOX}}{\sqrt{1 + \frac{2C_{BOX}^2}{qN_a\varepsilon_{Si}}}} \tag{2.5.1}$$

2. **Small body effects (fast stacked gates)** because it is possible to independently bias the body. This fact allows a lower threshold voltage for stacked transistors.

3. **No latch-up**, the parasitic PNPN (or NPNP) structure found in bulk CMOS (see Fig. 2.11) may turn on, limiting the maximum operating voltage. This structure is not found in a SOI device [57]. In SOI technology, there is just a parasitic bipolar effect found in Partially-Depleted Silicon-On-Insulator (PD-SOI), which might reduce drain breakdown voltage [58] (see Fig. 2.12). This effect is very small in Fully-Depleted Silicon-On-Insulator (FD-SOI).

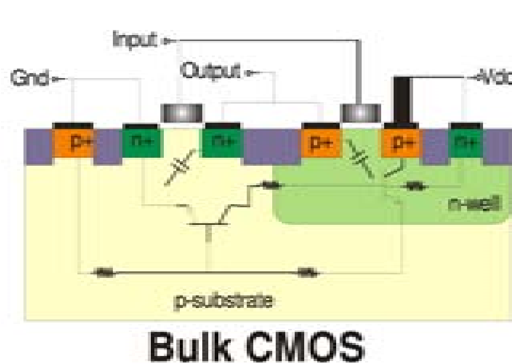


Figure 2.11: Parasitic PNPN structure in bulk CMOS structure.

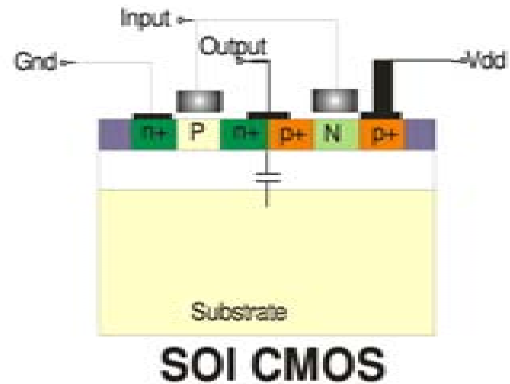
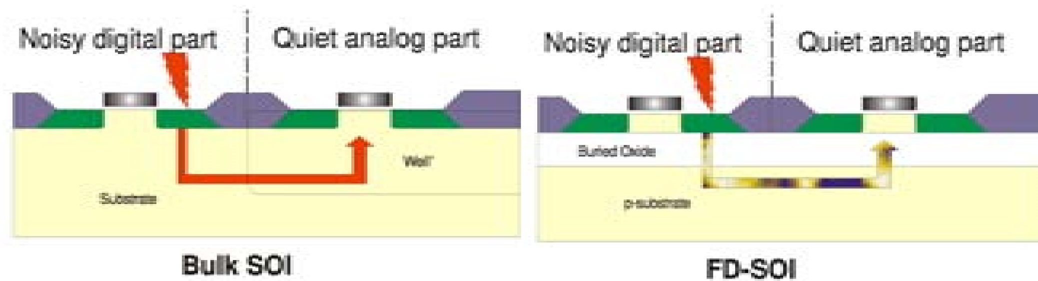


Figure 2.12: Parasitic structure in SOI CMOS structure.

4. **Simple device isolation, smaller area** in SOI technology, each transistor is laterally isolated by an insulator film and vertically isolated from the substrate by the BOX, representing better isolation than bulk technology (see Fig. 2.13 and Fig. 2.14 for an schematic). The fact that no well for isolation is needed



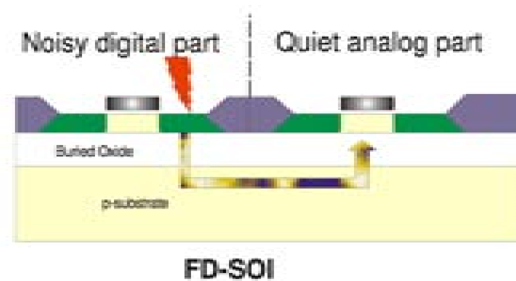
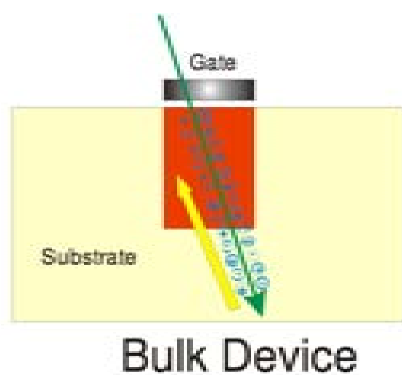


Figure 2.13: Noise travelling path in bulk devices.

Figure 2.14: Noise travelling path in SOI devices.

in a SOI device allows for the development of a more compact layout(see Fig. 2.12).

5. **Excellent radiation hardness** SOI shows excellent radiation hardness to alpha particles, neutrons and other particles. As an example, an alpha particle with an energy of 5 MeV can penetrate about 25μm in Si, generating many electron-hole pairs, which results in charges of around 10fC per μm. Considering the thickness of the active Si, the number of generated charges in the active area is very small, compared to bulk transistors. The Soft Error Rates (SERs) in SOI becomes a function of the SOI thickness.



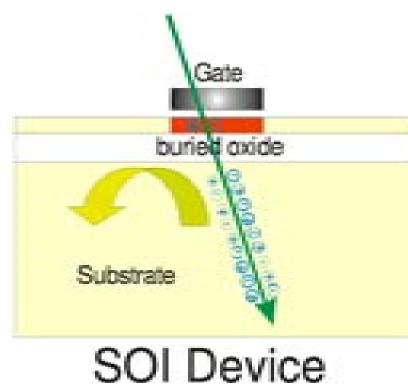


Figure 2.15: Soft error immunity in bulk devices.

Figure 2.16: Soft error immunity in SOI devices.

6. **Small junction leakage current** in SOI, because the impurities in n^+ and p^+ regions diffuse deeply into the thin Si film, leaving a p-n junction only at the sidewall of the diffused area.

2.5.3 SOI Characteristics

Some of the electrical performace characteristics of the SOI technology that can be summarized in the following way:

Threshold Voltage If considering a thick film in SOI ($t_{Si}>2x_{dmax}$), there will be no interaction between front and back depletion zones.

$$x_{dmax} = \sqrt{\frac{4\varepsilon_{Si}\Phi_F}{qN_a}} \tag{2.5.2}$$

where Φ_F is the Fermi potential and is equal to $\Phi_F=\frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right)$. In this case, the threshold voltage expression is similar to the bulk expression and is given by:

$$V_{th} = V_{FB} + 2\Phi_F + \frac{qN_a x_{dmax}}{C_{ox}} \tag{2.5.3}$$

where V_{FB} is the flat band voltage, Φ_B is the Fermi potential and x_{dmax} is the maximum depletion width.

The threshold voltage of a thin film, fully depleted, enhancement mode, n-channel SOI device is obtained from solving the Poisson equation and is solved to be[5]:

$$\phi(x) = \frac{qN_a}{2\varepsilon_{Si}}x^2 + \left(\frac{\phi_{s2}-\phi_{s1}}{t_{Si}}\right)x + \phi_{s1} \tag{2.5.4}$$

where ϕ_{s1} and ϕ_{s2} are the potentials at the front and back Si/Oxide interfaces. The doping concentration N_a is assumed to be constant. The equation that describes the front-gate voltage is given by:

$$V_{G1} = \phi_{MS1} - \frac{Q_{ox1}}{C_{ox2}} + \left(1+\frac{C_{Si}}{C_{ox2}}\right)\phi_{s2} - \frac{C_{Si}}{C_{ox2}}\phi_{s1} - \frac{\frac{1}{2}Q_{dep1}+Q_{s2}}{C_{ox2}} \tag{2.5.5}$$

where, $C_{Si}=\varepsilon/t_{Si}$, Q_{dep1} is the total depletion charge in silicon film, Φ_{MS1} is the front work function difference, Q_{ox1} is the fixed charge density at the front Si-SiO_2

[5]See Section 2.5.6 for a description of the single/dual gate structure

interface, Q_{inv} is the front channel inversion charge and C_{ox1} is the front gate oxide capacitance. Similarly the expression for the back-gate voltage is given by:

$$V_{G2} = \phi_{MS2} - \frac{Q_{ox2}}{C_{ox1}} + \left(1 + \frac{C_{Si}}{C_{ox1}}\right)\phi_{s1} - \frac{C_{Si}}{C_{ox1}}\phi_{s2} - \frac{\frac{1}{2}Q_{dep2} + Q_{s1}}{C_{ox1}} \tag{2.5.6}$$

Equation 2.5.5 and Equation 2.5.6 can be combined to obtain the dependence of the front threshold voltage on back gate vias voltage.

If the back surface is **accumulated**, Φ_{s2} is pinned to approximately 0V. The threshold voltage is calculated at Φ_{s2}=0, Q_{inv1}=0 and $\Phi_{s1} = 2\Phi_F$, giving the expression,

$$V_{th1,acc2} = V_{G1} = \phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + \left(1 + \frac{C_{Si}}{C_{ox1}}\right) - \frac{Q_{dep1}}{2C_{ox1}} \tag{2.5.7}$$

If the back surface is **inverted**, Φ_{s2} is pinned to approximately $2\Phi_F$. The threshold voltage is calculated at Φ_{s2}=$2\Phi_F$, Q_{inv1}=0 and $\Phi_{s1} = 2\Phi_F$, giving the expression,

$$V_{th1,inv2} = V_{G1} = \phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + 2\phi_F - \frac{Q_{dep1}}{2C_{ox1}} \tag{2.5.8}$$

If the back surface is **depleted**, Φ_{s2} depends on the back gate voltage, V_{G2}. Where V_{G2} can range from 0 to $2\Phi_F$, or $V_{G2,acc} < V_{G2} < V_{G2,inv}$ the front threshold voltage can be obtained, considering $\Phi_{s1} = 2\Phi_F$ and $Q_{inv1} = Q_{s2} = 0$, giving the expression,

$$V_{th1,depl2} = V_{Vth1,acc2} - \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})}(V_{G2} - V_{G2,acc}) \tag{2.5.9}$$

Body Effect For an SOI transistor, the body effect is defined as the dependence of the threshold voltage on the back gate bias. Although it can be neglected in thick-film SOI devices, this does not happen in thin-film FD-SOI devices, where the body-effect is derived from Equation 2.5.9,

$$\frac{dV_{th1}}{dV_{G2}} = -\frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})} = -\frac{-\varepsilon C_{ox2}}{C_{ox1}(t_{Si}C_{ox2} + \varepsilon_{Si})} = \gamma \tag{2.5.10}$$

In most cases the following approximation can be made, $\gamma \cong -\frac{t_{ox1}}{t_{ox2}}$.

Short Channel Effects In an ideal case, the MOSFET should behave like a switch and there should be minimal leakage in the device when it is off. As the dimensions are reduced, it's very difficult to maintain this perfect switch characteristic. The primary effect of the short channel is to increase the leakage current when the devices are off. This leakage effect is smaller than in bulk devices.

I-V Characteristics The expression for thick-film SOI is identical to bulk MOSFET. For the case of thin-film FD-SOI, the saturation current in strong inversion is:

$$I_{Dsat} \cong \frac{W\mu_n C_{ox1}}{2L(1+\alpha)}(V_{G1} - V_{th})^2 \tag{2.5.11}$$

where $\alpha = C_{Si}/C_{ox1}$ in a fully depleted device with accumulation at the back interface, and $\alpha = \frac{C_{Si}C_{ox2}}{C_{ox1}(C_{Si} + C_{ox2})}$ in a fully depleted transistor with depleted back interface. The high saturation current in thin film fully depleted SOI MOSFET increases its current drive capacity and gives excellent speed performance.

Transconductance is a measure of the effectiveness of the control of the drain current by the gate voltage. In a thin-film FD-SOI MOSFET, the transconductance can be expressed as:

$$g_m = \frac{dI_{Dsat}}{DV_{G1}} = \frac{W\mu_n C_{ox1}}{L(1+\alpha)}(V_{G1} - Vth) \tag{2.5.12}$$

This value is rather higher in FD-SOI compared to bulk or back accumulated device.

Mobility The mobility of the electrons within the inversion layer of an n-channel MOSFET is a function of the vertical field below the gate oxide, and can be approximated to:

$$\mu_n(y) = \mu_{max}[E_c - E_{eff}(y)],\ for\ E_{eff}(y)\ E_c \tag{2.5.13}$$

where μ_{max}, E_c and c are fitting parameters depending on the gate oxidation process [59] [60].

SubThreshold Slope The subthreshold swing (or inverse subthreshold slope) is the inverse of the slope of the $I_D(V_G)$, that is expressed as:

$$S = \frac{dV_G}{d(logI_D)} \tag{2.5.14}$$

The inverse subthreshold slope has the lowest value in a FD-SOI device, allowing lower threshold values to be used than bulk, without increasing the leakage current.

High-Temperature operation It is a consequence of the immunity to latch-up. The high-temperature leakage currents are decreased because of the small junction area of FD-SOI devices (up to 3 to 4 orders of magnitude smaller compared to bulk CMOS). This means that threshold voltage variation with temperature can be 2 to 3 times smaller than bulk devices.

Total Ionizing Dose The presence of many Si-SiO_2 interfaces make an SOI device more sensitive to Total Ionizing Doses (TIDs). The process provided by OKI 0.15 μm shows radiation tolerance up to a few hundred kRad [1]. At higher doses, the holes are trapped at Si-BOX interfaces and the threshold voltage shifts due to back gate bias, although it can be compensated for by biasing the substrate [61].

2.5.4 Comparison of PD-SOI and FD-SOI

There are two kind of SOI devices, PD-SOI and FD-SOI. The main difference is the Si active layer thickness which in PD-SOI can reach 100-200 nm, while in FD-SOI the active thickness is less than 50nm (see Fig. 2.17 and Fig. 2.18 for comparison).

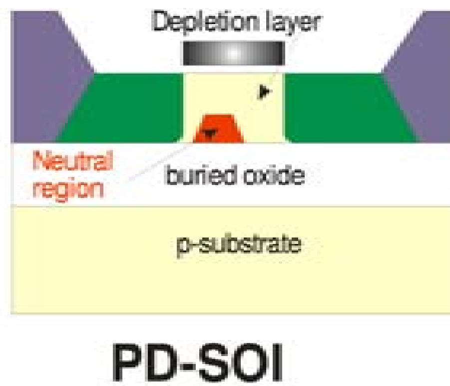


Figure 2.17: Cross section of bulk CMOS transistors.

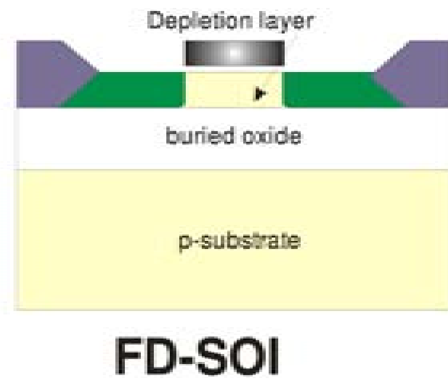


Figure 2.18: Cross section of SOI CMOS transistors.

In **PD-SOI** , there is a neutral region in the body that causes floating body effects (the body potential varies with the number of holes that accumulate in the body and with the voltage at the electrodes), which modifies the threshold voltage. Floating body effects are, among others, history and kink effects. Hysteresis makes simulation of the circuits difficult and the kink effects increases the drivability; useful for high-speed digital circuits but detrimental for analog circuits.

In **FD-SOI** , the body under the gate is depleted, and body floating effects are reduced. In these transistors, the gate voltage is used to deplete the body region, so the sub-threshold slopes are steep. That makes it possible to lower the

threshold voltage and encourages FD-SOI s use in low power applications.

A comparison of the energy bands (see Fig. 2.19) of both SOI devices show that the potential barrier to holes between body and source is lower in FD-SOI type (hardly any holes accumulate in FD-SOI, mitigating floating body effects [62]). Since the gate potential provides good control of the channel potential, the subthreshold slope is steeper than in PD-SOI-type making low-voltage operation possible.

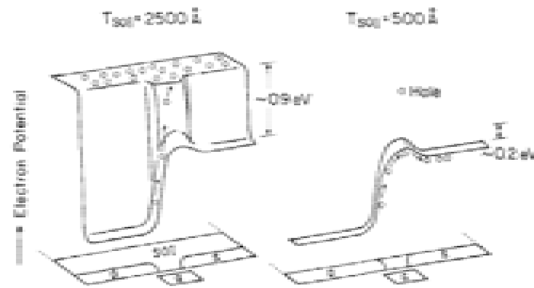


Figure 2.19: Two-dimensional electron potential in PD- and FD-SOI MOSFET [63]

Operation Modes of PD- and FD-SOI MOSFETs. In a FD-SOI device, the body is depleted for *on* and *off* states, because of the thinner body region. A PD-SOI device has an undepleted neutral region at the bottom of the body region, creating a potential difference between the top and bottom of the body region larger than in FD-SOI devices. The number of accumulated holes (generated by impact ionization near the drain) at the body depend on the barrier height. Because of the higher barrier height in PD-SOI, more holes accumulate at the bottom. These holes generate all kind of floating-body effects: kink at the drain current-voltage characteristics, shallow subthreshold characteristics and instability of dynamic characteristics.

Kink effect in PD-SOI Fig. 2.21 show the effect so-called *kink effect*, which does not exist for the equivalent MOSFET device manufactered in FD-SOI, as seen in Fig. 2.20. Fig. 2.21 shows the *kink*, a sharp rise in drain current as drain voltage increases at a fixed gate voltage. The reason for that is the higher potential barrier for holes in the PD-SOI devices. When a large number of holes accumulate, the potential of the body rises to a positive value and it causes the threshold voltage to drop (increasing the drain current).

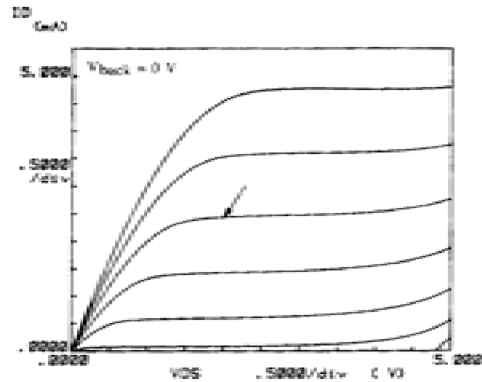


Figure 2.20: I_{ds} V_{ds} characteristics of a FD-SOI nMOSFET [57].

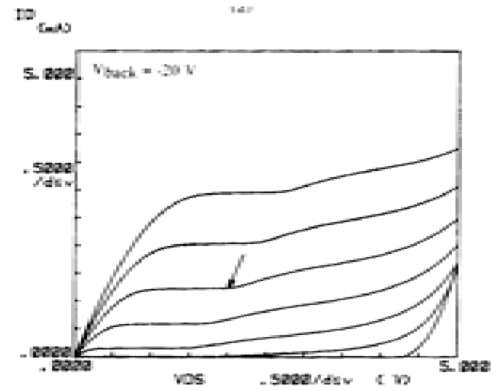


Figure 2.21: I_{ds} V_{ds} characteristics of a PD-SOI nMOSFET [57].

2.5.5 SOI MOSFET layout

The layout of a SOI transistor can be a regular (active area, gate and contact hole) device or an edgeless device. An edgeless device will avoid edge leakage problems, such as when devices are exposed to ionizing radiation, where the generation of oxide charge develops in the field oxide. **Body contact** can be used for applications where the kink effect or parasitic lateral bipolar effects need to be avoided. It consists of a p^+ diffusion contact with the p-type silicon underneath the gate (called I-gate, see Fig. 2.22 [57]). There are two variations: the T-gate design and the H-gate design. The T-gate (see Fig. 2.23) design is used for large gate width, where more than a single body contact is used to suppress the kink effect. The H-gate (see Fig. 2.24) design is the next version, including body contacts at both ends of the channel. The last and more compact body contact is where the p^+

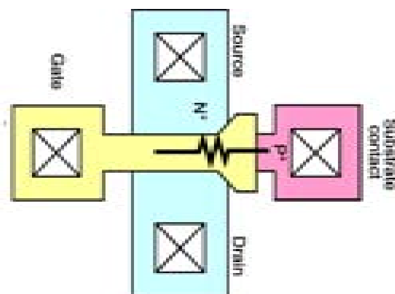


Figure 2.22: I-gate device schematic.

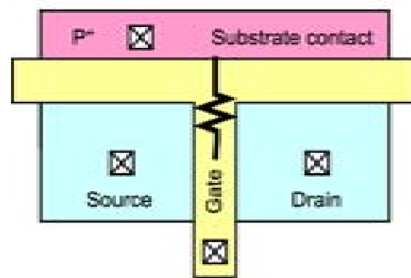


Figure 2.23: T-gate device schematic.

body ties are created on the side of the n^+ source diffusion. It is an asymmetrical

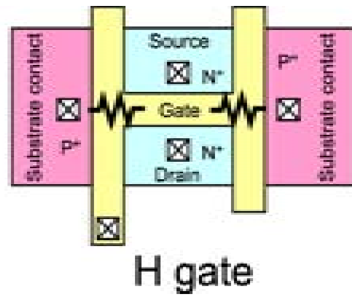


Figure 2.24: H-gate device schematic.

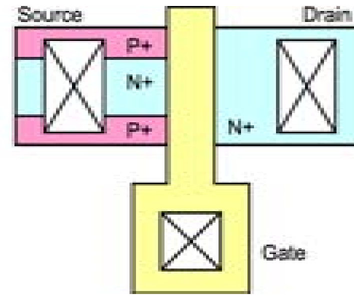


Figure 2.25: N-channel transistor with source body ties.

design and the effective channel width that is smaller than the width of the active area.

2.5.6 Single/Dual Gate Operation for the FD-SOI

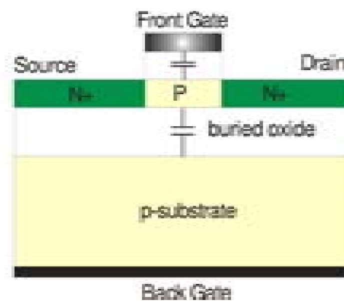


Figure 2.26: Schematic illustration of FD-SOI cross-section.

An FD-SOI MOSFET enables the control of the channel from the front-gate and the back-gate. The **dual gate operation** enables control and optimization of threshold voltage, subthreshold voltage swing and small signal transconductance. The front-gate corresponds to the conventional gate terminal, and the voltages applied (V_{FG}) to it are used to modulate the carrier concentration of the Si film. Unlike bulk-Si, there is a backside contact to the device, which can also be used as a gate. Voltages applied (V_{BG}) to the back-gate are applied across the BOX to modulate the energy bands and carrier concentration of the Si film.

An applied back-gate voltage will affect the value of the threshold voltage (V_t). Fig. 2.27 shows the I_{ds} versus V_{FG-s} and clearly shows how the V_{th} can be modulated using V_{FG-s}. The evolution of V_{th} can also be seen in Fig. 2.29. This fact is explained by charge control [65].

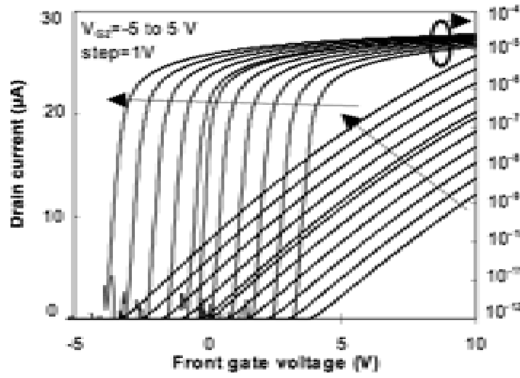


Figure 2.27: Drain current versus front gate bias in a 3nm thick transistor with L=30μm and W=100μm [64].

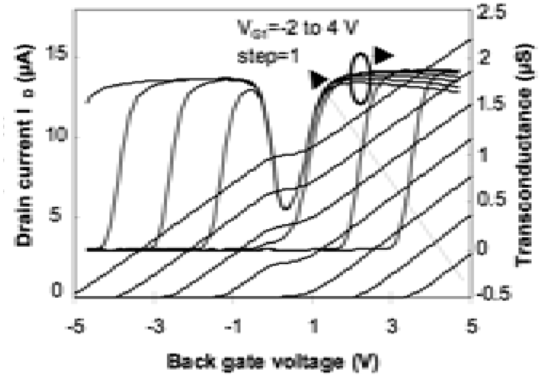


Figure 2.28: Drain current and transconductance versus back gate bias (3nm thick transistor) [64].

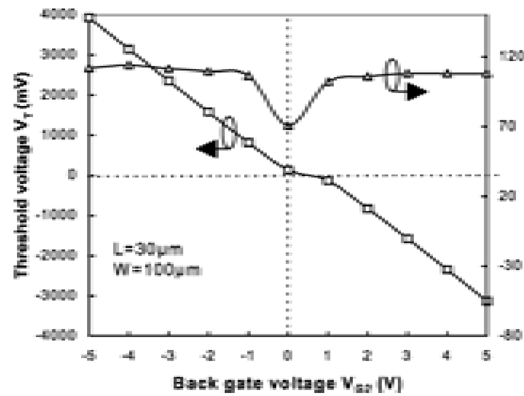


Figure 2.29: Threshold voltage and subthreshold swing versus back gate bias in a 3nm thick MOSFET [64].

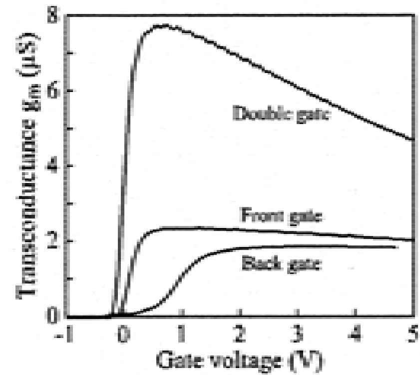


Figure 2.30: Transconductance versus gate voltage in a 3-nm-thick SOI MOSFET operated in dual-gate mode (V_{BG}=0.8V) and single-gate modes (front channel with V_{FG} = 0, back channel with V_{BG} =0V, L = 30 μm, V = 50 mV, T =300 K) [66].

Applying an inverting V_{BG} will increase the off-state leakage current (I_d at V_{FG}=0V) between drain and source, which also will increase the static power consumption. If V_{BG} depletes the back channel a steeper subthreshold curve is obtained, which is desired for optimizing power and performance. When the FD-SOI body is depleted by V_{BG} both carrier and electric fields from drain and source are modulated, causing the subthreshold swing to be minimized with depleted V_{BG}. The depletion mode operation will increase small signal transconductance in strong inversion.

2.6 Introduction to Detection

Quanta of radiation can be observed on a very small scale of time as well as space. Radiation detectors are developed to detect these quanta of radiation and were initially developed for detecting radiation in atomic, nuclear and elementary particle physic experiments. Now they are used in many fields of science and everyday life. The progress that comes from science is not just directly related to the relation between science and experiment. Now it is also driven by breakthroughs in instrumentation. Modern detectors convert the absorbed energy into an electrical signal and the sensitivity of the detector will depend on the choice of either the detector or the electronics used for the read-out. To maximize sensitivity, there are many factors to be considered: signal formation, coupling of the detector to the electronics and noise fluctuations in the electronics.

Radiation impinges on a sensor creating an electric signal, the signal level is low and it must be amplified to allow digitization and storage. The detection limit is determined by the SNR. SNR can be optimized, thereby increasing the signal and reducing the noise. A detector system is designed to perform specific and basic functions, including:

- Radiation deposits energy while traversing a detector medium; so detection should be done without affecting the trajectory of the particle by minimizing the energy loss and particle scattering.
- Radiation energy is converted into an electric signal (pulse of electric charge) in the detector medium. This can be done by direct conversion. Direct conversion involves ionization by the incident radiation in the absorber that creates mobile

charges. The energy absorbed is proportional to the primary signal charge. The signal charge created is not available instantaneously, leading to a typical pulse duration of 1ns-10μs.

- The electrical signal is amplified (by an electronic circuit or by secondary multiplication) introducing random fluctuations (noise).
- Digitization of a signal amplitude (Analog-to-Digital Conversion(ADC)) or time difference between detected signal and a reference signal (Time-to-Digital Conversion (TDC)).

2.6.1 Silicon Detector as a p-n Junction

The collecting element used to explain the collection of charge, and therefore signal formation, is a semiconductor diode (for a more detailed description see [67]). A depleted diode is an ionization chamber because it presents a detection volume with an electric field. When energy is deposited in the diode volume e^{-}-h^{+} pairs are created. If these pairs are moving in an electric field an electrical signal, is thus generated. Semiconductor devices with diode detectors can be used to perform energy measurements and position sensing of particles passing through the detector medium. The resolution of the measurement is determined by the patterning and quality of the detector.

The first Subsection 2.6.2 considers how the signal is extracted. In order to form a current that can be measured with external circuits, the signal charge carriers must be brought into motion. This is done by establishing a field in the detection volume. Increasing this field will sweep the charge more rapidly from the detection volume.

2.6.2 High-Field Region and the Diode

The diode is the simplest bipolar semiconductor device and the basis for all solid state particle detectors. It is formed by a p-type and a n-type semiconductor brought together. A depletion layer (or space charge layer) is built up at the junction as a result of the diffusion caused by the carrier concentration gradients. The holes diffuse from the p-side into the n-side, while electrons diffuse from the n-side to the p-side. An electric potential barrier, ξ, builds up, creating a drift current which

opposes the diffusion flow. The electric field is a maximum at the junction and zero at the depletion layer edges. The zero external bias, built-in, junction potential is given by,

$$V_{bi} = \frac{kT_j}{q} ln \frac{N_A N_D}{n_i^2} \tag{2.6.1}$$

where q is the electron charge (1.6 10^{-19}C), k is the Boltzmann's constant (1.38 10^{-23}J/K) and T_j is the junction temperature (in K). The pn junction can be reversed biased; p-region is negatively biased with respect the n-region. In that case the depletion zone widens. As this happens, the peak electric field ξ_m at the junction increases creating a wider depletion region. The only current flowing is the leakage current due to carriers generated in the depletion zone that diffuse to the junction and are collected.

Electric Field and Electrostatic Potential for the Diode To define the equations of the diode, it is useful to start by evaluating the electrical neutrality considering that the charge on either side of the junction is equal to:

$$qN_D x_n = -qN_A x_p \tag{2.6.2}$$

where q is the charge of the electron (1.60 $\times$ 10^{19} C), N_D is the concentration of donors in the n-type semiconductor, and N_A is the concentration of acceptors in the p-type semiconductor. x_n is the distance over which the donor atoms have a positive charge (because they have lost their free electron) and x_p is the distance which the acceptors atoms have a negative charge (because they have lost their free holes). These two last quantities define the depletion region, as the region which is depleted of free carriers

$$x_d = x_n - x_p \tag{2.6.3}$$

The general analysis starts by invoking Poisson's equation (2.6.4) to start calculating the electric potential. This permits calculation of the electrical field from the integral, imposing that the electric field at the end of the depletion field is zero, resulting in

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\partial E}{\partial x} = \frac{\rho}{\varepsilon_S} \tag{2.6.4}$$

where the electric field results in

$$E(x) = \begin{cases} -\dfrac{qN_A}{\varepsilon_S}(x + w_p) & -w_p \le x \le 0 \\ \dfrac{qN_D}{\varepsilon_S}(x - w_n) & 0 \le x \le w_n \end{cases} \tag{2.6.5}$$

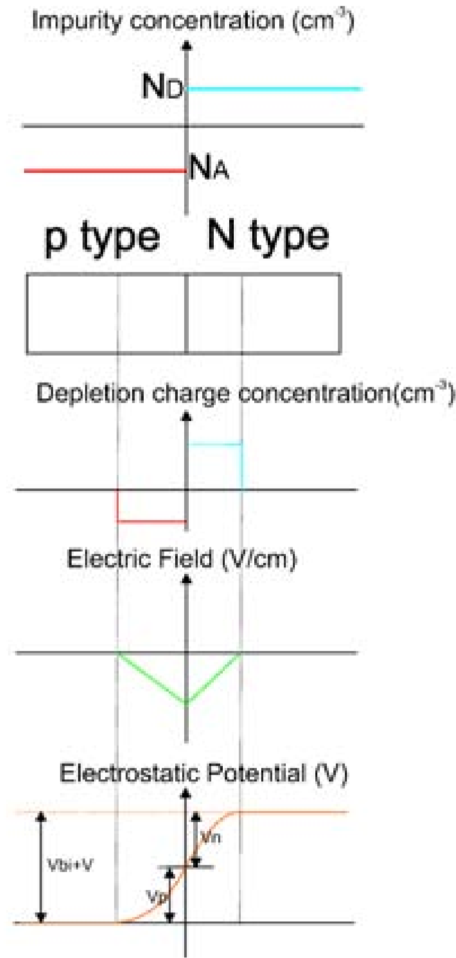


Figure 2.31: A p-n junction: a) cross-section for the initial impurity concentration, an schematic of the p-n type zone definition, the depletion charge concentration, the electric field and electrostatic potential that can be found.

where ε_S is silicon permittivity (1.0359×10^{-12} F/cm). The second integration of 2.6.4 gives the expression of the electrostatic potential, with conditions V(-w_p)=0 and V(w_n)=V, giving

$$V(x) = \begin{cases} -\dfrac{qN_A}{2\varepsilon_S}(x+w_p)^2 & -w_p \leq x \leq 0 \\ \dfrac{qN_D}{2\varepsilon_S}(x-w_n)^2 + V & 0 \leq x \leq w_n \end{cases} \tag{2.6.6}$$

The values obtained from 2.6.6 will also give the potential barriers at the junction as,

$$V_p = \frac{qN_A w_p^2}{2\varepsilon_S} \tag{2.6.7}$$

$$V_n = \frac{qN_D w_n^2}{2\varepsilon_S} \tag{2.6.8}$$

The equations 2.6.7 and 2.6.9 can be summed to produce the total potential difference at the junction, as

$$V_{bi} + V = V_p + V_n = \frac{q}{2\varepsilon_S}(N_A w_p^2) \tag{2.6.9}$$

where V_{bi} is the built-in potential 2.6.1. This expression can be used to give an equation defining the total width of the depleted zone as

$$w_d = w_p + w_n = \sqrt{\frac{2\varepsilon_S(V_{bi} + V)(N_D + N_A)}{qN_D N_A}} \tag{2.6.10}$$

This expression can be simplified based on the real architecture of the detectors. Detector diodes are usually asymmetrically doped. The starting material (bulk) is lightly doped and will occupy most of the depleted zone. Considering the case of an epitaxial layer with a p-substrate and an n implant, which is the case of a typical commercial technology, the equation will be,

$$w_d \approx \sqrt{\frac{2\varepsilon(V_{bi} + V)}{qN_A}} \tag{2.6.11}$$

In the case of a SOI technology, where a n-substrate can be used with a highly doped p implant the equation is,

$$w_d \approx \sqrt{\frac{2\varepsilon(V_{bi} + V)}{qN_D}} \tag{2.6.12}$$

The doping concentration can also be expressed in terms of resistivity

$$\rho = (\mu q_e N)^{-1} \tag{2.6.13}$$

where μ describes the relation between the applied field and the carrier velocity, now the depletion width can be expressed as:

$$w_d = \sqrt{2\varepsilon\mu_n\rho_n V_b} \tag{2.6.14}$$

The detector bulk will be completed depleted when w_d=d (thickness of the bulk). If the bias voltages increase beyond this value, it will add a uniform field with a distribution:

$$E(x) = \frac{2V_{di}}{W}\left(1 - \frac{x}{W}\right) + \frac{V_b - V_{di}}{W} \tag{2.6.15}$$

where $V_{di}=V_d+V_{bi}$ is the internal depletion voltage. When considering a partially depleted detector ($V_b < V_d$), the field can also be expressed as,

$$E(x) = -\frac{q_e N_d}{\varepsilon}(W - x) \equiv E_o(W - x) \tag{2.6.16}$$

where the local velocity of a charge carrier is defined as,

$$v(x) = \mu E(x) = \mu E_o(W - x) \tag{2.6.17}$$

2.6.3 Junction Capacitance

Junction Capacitance The voltage dependent depletion region capacitance C_j, which is dominant under reverse bias, involves the zero bias junction potential voltage ϕ and the zero bias junction capacitance C_{jo}

$$C_{jo} = \left| \frac{dQ}{dV} \right| = A\sqrt{\frac{q\varepsilon_S}{2(V_{bi}+V)} \frac{N_D N_A}{N_D+N_A}} = \frac{\varepsilon_S A}{w_d} \quad (2.6.18)$$

$$C_j = C_{jo}(1 - \frac{V}{V_{bi}})^{-\frac{1}{2}} \quad (2.6.19)$$

where V_{bi} is the junction potential (as defined in Equation 2.6.1), A is the cross-sectional area of the junction and w_d is the width of the depletion region. The permittivity of the silicon is often expressed as:

$$\varepsilon_S = K_S \varepsilon_o \quad (2.6.20)$$

where K_S is the dielectric constant of silicon and ε_o is the permittivity of free space (8.86 10^{-14}F/cm). Equation 2.6.18 can be approximated in the case of an asymmetric junction to Equation 2.6.21 and in the case of p substrate and highly doped n (Equation 2.6.11.

$$C_j = \sqrt{\frac{q\varepsilon_S N_A}{2(V_{bi}+V)}} \quad (2.6.21)$$

For the case of n substrate and highly doped n (Equation 2.6.12), the Equation 2.6.22 is obtained

$$C_j = \sqrt{\frac{q\varepsilon_S N_D}{2(V_{bi}+V)}} \quad (2.6.22)$$

Leakage Current is the second parameter for a diode detector, because it directly affects the SNR value. The leakage current comes from the thermal generation of the electron-hole pairs in the material. It consists of 2 components: generation current and diffusion current. The **generation current** appears because of the generation process at the depletion region of the detector, where the presence of the electric field separates the charges and they cannot recombine. The charges drift under the influence of the electric field and give rise to the leakage current, the Equation that describes it is [68],

$$j_{jen} = \frac{q n_i W_d}{\tau_g} \quad (2.6.23)$$

where τ_g is the generation time, which is dependent upon the substrate quality. The generation current depends on the reverse bias voltage and should increase linearly

with the $\sqrt{V}$ (see Equation 2.6.12) until full depletion and then remain constant. The **diffusion current** is related to the generation process in undepleted regions. If the e-hole pairs are generated close to the space charge region and have a chance to diffuse into the space charge region before recombination, they create a diffusion current, the density of which is approximated as [69],

$$j_{diff} \approx n_i^2 \left(\frac{1}{N_A} \sqrt{\frac{D_n}{\tau_n}} + \frac{1}{N_D} \sqrt{\frac{D_p}{\tau_p}} \right) \tag{2.6.24}$$

where D_p (D_n) is the electron (hole) diffusion constant τ_n (τ_p) is the electron (hole) lifetime. For an asymmetric junction, Equation 2.6.24 becomes,

$$j_{diff} \approx q \frac{n_i^2}{N_D} \sqrt{\frac{D_p}{\tau_p}} \tag{2.6.25}$$

Under normal operation, detectors are fully depleted and the leakage current is determined by generation current (Equation 2.6.23).

2.6.4 Charge Collection

Mobile electrons and holes move under the influence of the electric field in the p-n junction. Although electrons and holes move in opposite directions, their contribution to the signal current is of the same polarity. The time required for a charge carrier to traverse the sensitive volume is the collection time. This time for a charge originating at x_o to reach x is

$$t(x) = -\frac{1}{\mu E_o} ln \frac{W - x}{W - x_o} = \frac{\varepsilon}{\mu q_e N_d} ln \frac{W - x}{W - x_o} \tag{2.6.26}$$

Considering a hole drifting toward a high-field region and collected at the p-electrode (x=0), Equation 2.6.26 becomes

$$t(x_o) = \tau_p ln \frac{W}{W - x_o} \tag{2.6.27}$$

where τ_p is defined as the characteristic time. For the electrons drifiting to the low-field electrode (x=W), the corresponding Equation 2.6.27 can be expressed as

$$x(t) = W - (W - x_o) e^{-\frac{t}{\tau_n}} \tag{2.6.28}$$

where τ_n is the characteristic time for electrons. For electrons in $3\tau_n$ the carrier will have traversed 95% of the detector.

The collection time can be reduced by operating the detector at bias voltages exceeding the depletion voltage and Equation 2.6.16 can be expressed as,

$$E(x) = E_o\left(1 - \frac{x}{W}\right) + E_1 \tag{2.6.29}$$

considering the drift time for the holes originating at x_o=W and drifting to x=0 is,

$$t_{cp} = \frac{W}{\mu_p E_o} ln\left(1 + \frac{E_o}{E_1}\right) \tag{2.6.30}$$

corresponding equation for electrons is

$$t_{cn} = \frac{W}{\mu_n E_o} ln\left(1 + \frac{E_o}{E_1}\right) \tag{2.6.31}$$

and for the case of large over bias $E_1 \gg E_o$, Equation 2.6.30 becomes

$$t_{cp} = \frac{W}{\mu_p E_1} \tag{2.6.32}$$

2.6.5 Signal Formation

The signal (current) generation has a time dependence for detection. The signal current begins when the charge begins to move. When a charge pair is created, both the positive and negative charges couple to the electrode and induce mirror charges of equal magnitude. As a charge traverses the space between two plates the induced charge changes continuously, so current flows in the external circuit as soon as the charges begin to move. Mathematically, it can be analyzed using the Ramo's theorem [70].

Induced Charge and Ramo's Theorem Considering a mobile charge in the presence of any number of grounded electrodes, if the charge q moves in direction x, the current on electrode A is

$$i_A = \frac{dQ_A}{dt} = q\frac{dV_{q1}}{dt} = q\left(\frac{\partial V_{q1}}{\partial x}\frac{dx}{dt}\right) \tag{2.6.33}$$

can also be expressed as

$$i_A = qv_x\frac{\partial V_{q1}}{\partial x} \tag{2.6.34}$$

where v_x is the velocity of motion, and V_{q1} is the weighting potential that describes the coupling of a charge at any position to electrode A. In general, if a moving charge does not terminate on the signal electrode, the signal current is induced on other electrodes but the current changes sign and integrates to zero. The current

cancellation on non-collecting electrodes relies on the motion of both electrons and holes. Usually the weighting potential is strongly peaked near the signal electrode, thus most of the charge is induced when the moving charge gets near or terminates on the signal electrode.

In the case of a partially depleted detector, the depletion zones due to each charge collection diode can be very shallow and separated on the same substrate. Electric fields are also separated, and the non-depleted region can be considered as a constant potential volume. The charges originating in the non-depleted region may diffuse until they reach the region with electric field of one of the collecting electrodes. The signal weighting potential and the electric field become the same, the signal is only induced on the electrode on which the charge terminates.

2.6.6 Noise in Detectors

A detector system is defined by its resolution and presence of noise. These two characteristics will permit spectral contrast and determine the sensitivity ratio of the signal to background noise. The mechanism that generates noise can be understood by considering the simple case of the presence of n carriers of charge e moving with a velocity v through a sample of length l. The induced current i at the end of the sample is,

$$i = \frac{nev}{l} \tag{2.6.35}$$

and the fluctuation of this current is given by the total differential,

$$\langle di \rangle^2 = \left(\frac{ne}{l}\langle dv \rangle\right)^2 + \left(\frac{ev}{l}\langle dn \rangle\right)^2 \tag{2.6.36}$$

where the two terms are added in quadrature since they are statistically uncorrelated. There are thus two contribution to noise (see Equation 2.6.36): velocity fluctuations (such as thermal noise) and number fluctuations (such as shot noise and excess of 1/f noise). Thermal and shot noise are white noise sources with a constant power per unit bandwidth

$$\frac{dV_{noise}^2}{df} = const. \equiv e_n^2 \tag{2.6.37}$$

whereas 1/f noisehas a frequency depence given by

$$\frac{dP_{noise}}{df} = \frac{1}{f^\alpha} \tag{2.6.38}$$

here α is typically 0.5-2.0.

Shot noise occurs whenever carriers are injected into a sample volume independently of one another, like the current flow in a **diode**, where the spectral noise current density can be expressed as,

$$i_n^2 = 2q_e I \tag{2.6.39}$$

where q_e is the electronic charge and I is the DC current. Shot noise does not occur in ohmic conductors, however they do suffer from Nyquist or Johnson (or thermal) noise. Since the number of available charges is not limited, the fields caused by local fluctuations in the charge density draw in additional carriers to equalize the total number of carriers.

The other dominant source of noise if 1/f noise due to bias current. Diodes are operated under reverse bias and the noise results from the dark current. Under exposure to light or radiation source additional noise i_{ph} of generated charge carriers have to be taken into account. The two sources are statically independent and are expressed as [71],

$$i_{shot}^2(f) = 2q(i_{ph} + i_{dc}) \tag{2.6.40}$$

$$i_{1/f}^2(f) = a\frac{i_{dc}^c}{f} \tag{2.6.41}$$

where a is a constant that depends on the physical characteristics of the diode and i_{dc} is the constant bias current of the diode. 1/f (or Flicker) noise is caused by fluctuations in the surface recombination velocity and bulk carriers mobility. This flicker noise is proportional to the density of surface states, and in reverse biased diodes, only dark currents generate this noise. The total current, including thermal noise and 1/f, generates the shot noise.

The noise of a **MOS transistor** is more complicated. For a MOS biased in strong inversion, the transistor channel is resistive, and the dominant source of noise is thermal noise. In the weak inversion region, the dominant source is shot noise. In addition to these noises, it also presents 1/f noise sources. The noise can be modeled as two statistically independent current sources, connected in parallel with the drain current. The thermal or shot noise power spectral density is,

$$i_{d,th,sat}^2(f) = 4kTn\gamma g_m \tag{2.6.42}$$

$$i^2_{d,th,lin}(f) = 4kTng_{ds,lin} \quad (2.6.43)$$

The flicker noise power spectral density is,

$$i^2_{d,1/f,sat} = \frac{K_F g^1_m}{C_{ox}WL}\frac{1}{f} \quad (2.6.44)$$

$$i^2_{d,1/f,lin}(f) = \mu^2_{n,p}\frac{K_F W}{L^3}V^2_{DS}\frac{1}{f} \quad (2.6.45)$$

where first (Equation 2.6.42 and Equation 2.6.44), and second (Equation 2.6.43 and Equation 2.6.45) represent the MOS transistor in saturation and linear region. g_m and g_{ds} are the small signal transistor channel transconductance and conductance parameters, n is a parameter combining small-signal gate and bulk transconductances, proportional to the inverse of the subthreshold slope log (I_{ds}) vs V_{GS}, γ is a function of the basic transistor parameters and bias conditions and K_F is a flicker noise coefficient.

2.7 Pixel Detector Architectures

CMOS pixel sensors used in the field of high energy physics for particle detectors are based on developments related to CMOS image sensors[72]. High energy physics initially used CCD s for detection and read-out of the charge generated by particles and photons. The enhanced sensitivity and increased functionality of CMOS pixel sensors have made CCD technology less commonly used. An image sensor consists of an array of pixels that are typically selected one row at a time, using a shift register or a decoder. The read-out of the vertical column bus is normally done using a bank of analog signal processors (APS[6]) There are two predominant approaches to implement the basic architecture in CMOS for HEP: passive pixels and active pixels. The main difference is that the APS contains an active amplifier.

Passive Pixel Consists of a photodiode and a pass transistor. When the transistor is activated, the photodiode is connected to a vertical column bus. After being accessed, the photo diode is reset and the charge is converted to voltage.

[6]APS can perform functions as charge integration, gain, sample and hold, CDS, and Fixed-Pattern Noise (FPN) suppression

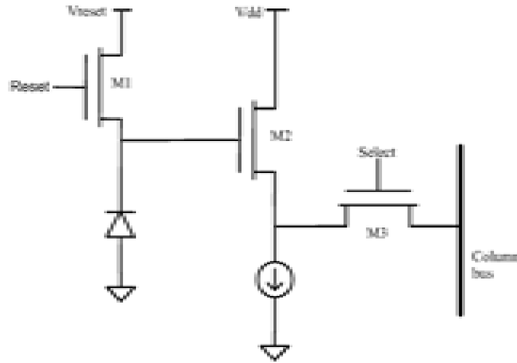


Figure 2.32: Active pixel schematic. The voltage at the electrode is buffered by a source follower to the column bus.

Active Pixel Includes an active amplifier within each pixel, see Fig. 2.32. Since the amplifier is activated only during the readout, power dissipation is kept to a minimum. The architecture shown at Fig. 2.32 is also known as a 3T pixel structure. M1 acts as a switch to reset the floating node corresponding to the electrode contact. M3 acts as a switch to select the pixel for readout, and M2 is the source follower with current source located outside the pixel and common to all the pixels in the column. The 3T structure has been widely used in the first designs for particle physics [33], [73], [74], with feature sizes that ranged from 0.18μm to 0.6μm.

The 3T structure by itself is limited in speed, which is a serious drawback for applications like the B-factory upgrade at KEK, where higher speed is needed. For these higher speed applications, pipeline architectures have begun to appear as the next step in pixel evolution. CAP was the proposal done for the Belle project upgrade at the KEK B-factory [75], [76], [77]. This approach was also used for the ILC, with the Flexible Active Pixel Sensors (FAPSs) [74] [78], [79]. The idea used in the CAP approach is to include different storage cells per pixel. The data can be stored at a high speed and subsequently read-out at a slower speed.

Digital MAPS is another option that is being analyzed in the MIMOSA series (where the data uses an on-chip discriminator to provide a binary output [80], [81]). Digital MAPS is also the option chosen for the Apsel series [82], where every pixel includes sparsification logic that includes a time stamp register to freeze the register when a pixel is hit.

2.8 Conclusions

This chapter has provided an introduction to most of the different technologies available and has pointed the main advantages and disadvantages present in the technologies chosen in the research done for the Belle Upgrade. These technology options are being widely researched and an increasing number of projects are using them (specially CMOS with epitaxial layer and CMOS on SOI) as the best option to develop new detectors.

The other goals in this chapter have been two-fold. First has been to introduce the relation between electronics and physics, providing all the tools needed to be able to understand how the charge is detected by the pixel circuitry. The second goal has been to introduce the different design solutions that have been used until now, and the new approaches that are being actively researched. These new approaches are going to be used to provide a more detailed and precise (in time and analog value) description of the events that are captured with a pixel detector.

Chapter 3

Principle of Detector Operation

The next section provides a brief explanation of how particles interact in a detector and the mechanisms for energy deposition. These explanations are needed to undestand the challenging nature of the particle physics experiments applications. In addition, the important characteristics which make Silicon such an interesting material for particle detectors are explained. The second section describes the different interactions of radiation with matter. Two kinds of particles are described: heavy particles and light particles. Both particle types interact with matter with different processes and these processes are explained. For the case of heavy charged particles, the Bethe-Block equation for energy loss is introduced, as well as the maximum kinetic energy and the cut-off energy. The straggling function, also known as the Landau function, corresponds to the energy loss for thin materials is also explained, to be able to introduce energy loss fluctuations. For light particles a brief analysis of both electrons and photons is presented. In these cases the radiation length is one of the characteristics of the processes. Multiple Coulomb Scattering is also introduced to explain how deflections in trajectory can happen due to interaction with materials. Table 3.1 has been included to summarize the variables used in this section.

3.1 Silicon as the Detector Material

Silicon is one of the most commonly used materials in semiconductor detectors. Some important properties of silicon from the point of view of effective particle detection are summarized in Table 3.2, with high density and low energy required for the generation of an electron-hole pair as the most important characteristics. This high density leads to a large energy loss per traversed length of ionizing

Symbol	Definition	Units of Value
β	v/c	
γ	$(1-(v^2/c^2))^{-1/2}$	
M	Incident particle mass	Mev/c^2
E	Incident particle energy γMc^2	MeV
T	Kinetic Energy	MeV
$m_e c^2$	Electron mass $\times$ c^2	0.5510998918(44)MeV
z_e	Charge of incident particle	
Z	Atomic number of absorber	
A	Atomic mass of absorber	g mol^{-1}
K/A	$4\pi N_A r_e^2 m_e c^2/A$	0.307075 MeV g^{-1} cm^2 for A=1 g mol^{-1}
δ $(\beta\gamma)$	Density effect correction to ionization energy loss	
-	$4\alpha r_e^2 N_A/A$	(716.408 g cm^{-2})$^{-1}$ for A=1 g mol^{-1}
X_0	Radiation length	g cm^{-2}
E_c	Critical energy for electrons	MeV

Table 3.1: Summary of physical constants used in this section [83].

Property	Value
Atomic number Z	14
Atomic mass A	28.0855
Density ρ [g cm^3]	2.33
Band gap energy E_g [eV]	1.12
Energy per electron-hole pair E_{e-h} [eV]	3.6
Intrinsic carrier concentration n_i [cm^3]	1.45×10^{10}
Electron mobility μ_e [cm$^2 V^{-1} s^{-1}$]	1350
Hole mobility μ_h [cm$^2 V^{-1} s^{-1}$]	450

Table 3.2: Silicon properties at 300 K [83], [67].

particle. The energy loss allows measurable signals even for thin detectors. Low electron-hole pair energy threshold ensures good energy resolution and a large number of charge carriers generated. Despite the high density of silicon, the electron and hole mobilities for this material are still quite high, which translates into relatively short collection times.

3.2 Interaction of Radiation with Matter

A fast, relativistic charged particle traversing matter loses energy in discrete amounts in independent, stochastic single collisions. The particle interacts with the electrons and the nuclei of atoms. The two main characteristics of this interaction are the loss of energy by the particle and the deflection of the particle from its incident direction. Different processes share the energy lost by the incident particle depending on the nature of the incident particles. The total energy loss is calculated as a sum of all contributions. Inelastic collisions with orbital electrons are almost exclusively responsible for the energy loss of **heavy particle** in matter. Energy is transferred from the particle to the atom causing an ionization by releasing the electrons, light emission or heat in the material. For **light charged particles** (like electrons and positrons), there are two main processes contributing to the continuous energy loss: ionization and bremsstrahlung. Bremsstrahlung is the term used for radiation caused by deceleration when passing through the field of atomic nuclei.

3.3 Energy Loss of Heavy Charged Particles

Charged particles, other than electrons, lose energy in matter by ionization if the energy transferred to the atomic electrons is large enough. The fluctuations in the total energy loss are small and a commonly used quantity is the average energy loss per unit track length -dE/dx [MeV/(g/cm^2)], where the negative sign indicates that the moving particle losses energy. The **mean energy loss** (or *stopping power*) can be derived using a full quantum mechanical treatment based on the momentum transfer, giving the equation commonly known as **Bethe-Block** equation [83]:

$$-\frac{dE}{dx} = Kz_e^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}ln\left(\frac{2m_ec^2\beta^2\gamma^2T_{max}}{I^2}\right) - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right] \quad (3.3.1)$$

where $\mathbf{T}_{max}$(see Equation 3.3.2) is the maximum kinetic energy which can be imparted to a free electron in a single collision and the other variables are defined at Table 3.1.

$$T_{max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma \frac{m_e}{M} + (\frac{m_e}{M})^2} \tag{3.3.2}$$

The energy loss rate will depend on the incident particle charge (see Equation 3.3.1) and slightly on its mass (according to Equation 3.3.2).

The created charge contributing to the sensed signal will depend on the energy deposited along the particle track. This energy is carried away by a few high-energy knock-on electrons produced[1], by fluorescence photons emitted by atoms along with the photons and phonons[2] radiated by the incident particles or, to a lesser extent, Čerenkov radiation. Therefore, practical detectors measure the energy that is deposited along to the particle track, not the total energy lost. The Bethe-Bloch equation does not include energy loss due to radiation. However, when energy is carried off by energetic knock-on electrons, it is more appropriate to consider the mean energy loss excluding greater energy transfers than some cut-off energy T_{cut}, where T_{cut}≈140 keV for silicon, to obtain a restricted energy loss that smoothly joins the energy loss given by the normal Bethe-Bloch function for $T_{cut}>T_{max}$, and this will be called the restricted energy loss rate, which can be expressed as,

$$-\frac{d\bar{E}}{dx}_{restr.} = K z_e^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2} ln\left(\frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2}\right) - \frac{\beta^2}{2}\left(1 + \frac{T_{upper}}{T_{max}}\right) - \frac{\delta(\beta\gamma)}{2}\right] \tag{3.3.3}$$

where T_{upper}=min(T_{cut}, T_{max}) [83]. Equation 3.3.3 is the mean rate of the energy deposited along the particle track [84], see Fig. 3.1 for the mean ionizing energy loss rates in silicon for pions. The stopping power in each medium decreases inversally proportional to β^2 for particle velocities $\gamma\beta<1$. The mean energy loss shows a minimum at $\gamma\beta \approx 3$. Particles with this minimum amount of the energy loss are called **MIP** .

The detection of charged particles is based on the specific energy loss in matter and the obtained signal is proportional to this **specific energy loss** and the **thickness of the detector**. Fig. 3.2 shows the energy loss in Cu as a function

[1] Knock-on electrons or delta rays may have enough energy to produce, themselves, fresh ions in traversing the medium (generating a secondary ionization).

[2] Which are not completely negligible.

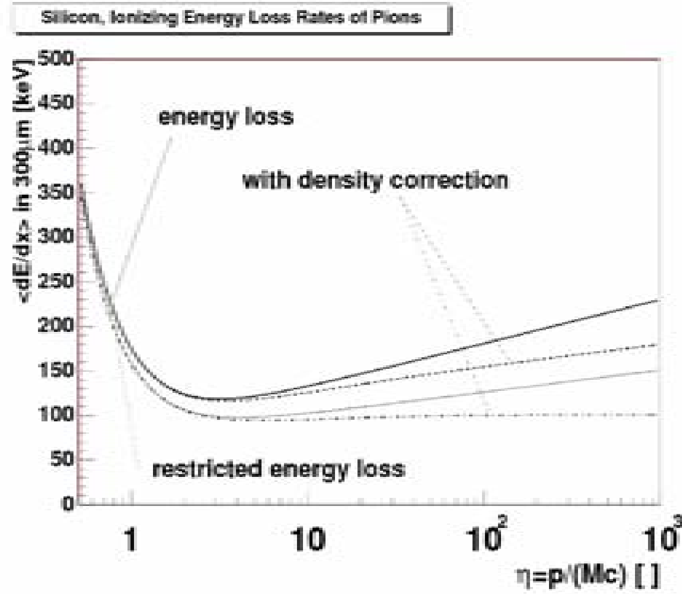


Figure 3.1: Energy loss rate and restricted energy loss rate as a function of η in Silicon, considering density corrections and without density correction (see Table 3.1, Equation 3.3.1 and Equation 3.3.3 for more detail in the expression of $\delta(\beta\gamma)$). Here the restricted energy loss is calculated using T_{cut}=140keV in silicon. The restricted energy loss smoothly joins the energy loss for $T_{cut}>T_{max}$. It shows a restricted energy loss rate of 97 keV/300 μm for silicon with a η=3 with density correction[84].

of particle momentum p [83]. In these units and as a function of $\gamma\beta$, the curve is approximately universal for all materials for particles with the same charge. Three regions are worth emphasizing: the low energy range with $0.05<\beta\gamma<1$, where the energy loss is proportional to $1/p2$, and thus can be used to measure the particle momentum. The region of minimum ionization with $1<\beta\gamma<100$, where a MIP deposits about 1.5 MeV/(g/cm^2), and the radiation region $\beta\gamma>5{,}000$, where most of the energy loss occurs via radiation.

3.3.1 Fluctuations in Energy Loss

The quantity (dE/dx)δx represents the mean energy loss via interaction with electrons in a layer of the medium characterized by the thickness δx. For finite δx , there are fluctuations in the actual energy loss, depending of the amount of energy transferred in a single collision and the number of collisions. The number of collisions involving large energy transfer is very small and the single-collision spec-

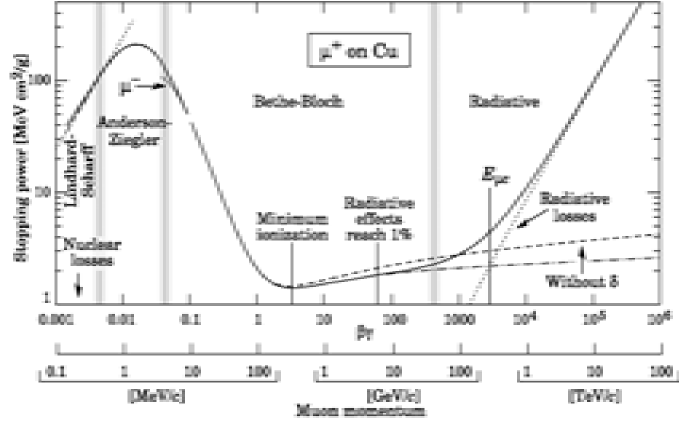


Figure 3.2: Stopping power ($= \mathrm{h}\langle E/dx \rangle$) for positive muons in copper as a function of $\beta\gamma$=p/Mc over nine orders of magnitude in momentum (12 orders of magnitude in kinetic energy), indicating that at high enough energies, all particles radiate and at low energies, the momentum of the particle can be determined from the energy loss.

trum becomes very asymmetric. Fluctuations follow a Poisson distribution and are inversely proportional to $\sqrt{N}$, where N is the number of collisions. The distribution of energy loss for a thick layer has a nearly gaussian form, called the *straggling function* (see [85] for a more detailed explanation). This distribution is skewed towards high values, with a long tail in the direction of high values of energy depositions. The first description of the probability distribution function (*pdf*) was given by Landau [86], making the assumption that the mean energy loss is small compared to the maximum energy transferred per single interaction T_{max}, which can be expressed by:

$$\rho K z^2 \frac{Z}{A} \frac{1}{\beta^2} x \ll T_{max} \tag{3.3.4}$$

The Landau function is approximated by the following normalized distribution:

$$\Phi(\lambda) = \int_{-\infty}^{\lambda} \phi(\tau) \tag{3.3.5}$$

also known as Moyal equation, where

$$\phi(\tau) = \frac{1}{2\pi i} \int_{-i\infty}^{+i\infty} e^{\lambda s + s\mathbf{ln}s} ds \tag{3.3.6}$$

and

$$\lambda = \frac{(N_{gen} - N_{mp})}{\Delta_{FWHM}} q \tag{3.3.7}$$

$\Phi(\lambda)$ is the distribution integral function of $\phi(\tau)$, which refers to the probability density of having a particular amount of charge generated, and the parameter λ is

a dimensionless number proportional to the energy deposited. The measured values for the most probable amount of charge generated $N_{mp}q$ and the width (Full Width at Half Maximum (FWHM))Δ_{FWHM} of the Landau distribution are used to derive the distribution of signals. Figure 3.3 shows some example Landau distributions for different thicknesses of a thin absorber.

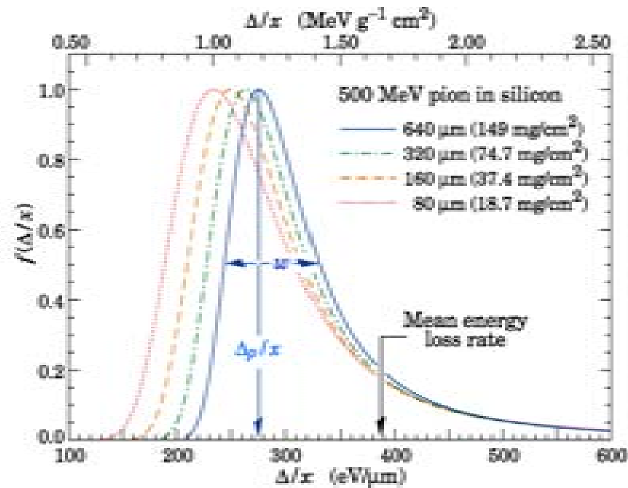


Figure 3.3: Straggling functions in silicon for 500 MeV pions, normalized to unity at the most probable value δ/x. The width w is the full width at half maximum [83].

The mean energy loss does not correspond to the peak, but is displaced because of the presence of the high-energy tail. When the mean energy required for charge carrier generation in a given material is known, the most probable energy loss allows a determination of the most probable number of charge carriers generated along the particle track per unit length (or e-hole pairs generated in a semiconductor material).

3.4 Energy Loss by Electrons

Light charged particles include electrons and positrons. At low energies light charged particles lose energy primary by ionization, but at high energies bremsstrahlung process becomes dominant. This difference in the character of the ionization energy loss results from the small mass of this particles [83], and modifies the Bethe-Block equation (see Equation 3.3.1), assuming the maximum energy

which is transferred during collision. This energy is equal to half of the kinetic energy of the incident particle. The contribution of the ionization and bremsstrahlung loss rate to the total energy loss rate of a light particle traversing the detector material depends on the energy of the particle. The ionization loss rate rises logarithmically with energy, while the bremsstrahlung loss rate rises nearly linearly with energy. For this reason, at certain incoming particle energy E_c, the two loss rates are equal. This value of energy is called critical energy and, for solid materials, may be approximated by Equation 3.4.1 [87]:

$$Ec = \frac{610MeV}{Z + 1.24} \tag{3.4.1}$$

According to the above formula, the critical energy E_c for silicon is of order 40 MeV.

3.5 Energy Loss by Photons

When a photon traverses the detector active volume, it may loss energy or change direction through such processes as: photoelectric effect, Compton or Rayleigh scattering (coherent) and electron-positron pair production. The probability of particular processes strongly depends up on the incident photon energy E_γ.

In low energy photons (for silicon up to several dozen keV), the dominate process is the photoelectric effect, although Compton and Rayleigh scattering also contribute. The photoelectric effect relies on the absorption of a photon by an atomic electron followed by the subsequent ejection of the electron from the atom. The absorption coefficient of this process is characterized by a discontinuity coming from the thresholds for photoionization of various atomic levels. If the kinetic energy of the photoelectron is high enough, the electron may cause a secondary ionization along its trajectory. The probability of the photoelectric effect decreases like $1/E_\gamma^{3.5}$ [88] with the increasing photon energy and Compton scattering becomes dominant in silicon detectors above 100 keV. Compton scattering originates from elastic scattering of the incoming photon off a quasi-free atomic electron. The photon changes direction and transfers part of its energy to the electron. In a given material, the probability of Compton scattering is proportional to $\ln E_\gamma / E_\gamma$. Another process that contributes at low energies is the Rayleigh scattering. The photon continues traversing the detector substrate, but its direction changes. At energies higher than about 1.022 MeV, the process of photon conversion into an electron-positron pair in the

Coulomb field of the nucleus may occur. This interaction is always accompanied by the atomic nucleus recoil, which allows simultaneous conservation of energy and momentum.

IR Laser A photon detector is a device (or a material) that detects light by a direct interaction of the radiation with the material. The efficiency of converting a photon to an electron is defined as quantum efficiency (η), normally expressed in percent. η takes into account reflectance, absorptance, scattering, and electron recombination. The electron-hole generation rate can be described as a function of distance into the detector as [89]:

$$g(x) = (1 - r)E_q a e^{-ax} \tag{3.5.1}$$

where r is the Fresnel reflectance, E_q is the photon irradiance and a is the absorption coefficient. The absorption coefficient is a strong function of wavelength [90]. Fresnel reflectance, which varies because the index of refraction is a function of wavelength, usually affects short wavelength response. Long wavelength photons tend to be transmitted causing a loss in quantum efficiency. In any case, there is always a cutoff wavelength that will define the minimum photon energy (hν) that can cause an electron in the valence band to be released into the conduction band and be detected[91].

3.6 Radiation Length

High-energy electrons predominantly lose energy in matter by bremsstrahlung, and high-energy photons by e^+-e^- pair production. The characteristic amount of matter traversed for these related interactions is called the radiation length X_0, which is usually measured in g$\cdot$cm^{-2}. The radiation length is a mean distance over which a high-energy electron losses all but 1/e of its energy by bremsstrahlung and the probability for a e^+-e^- pair to be created by a high-energy photon equals to 7/9. The value of radiation length depends on the atomic number Z of the material. A useful approximation of the radiation length, providing 2.5% agreement with more accurate and advanced estimations, is given by

$$X_0 = \frac{716.4 \cdot g \cdot cm^{-2} \cdot A}{Z \cdot (Z+1) \cdot ln(287/\sqrt{Z})} \tag{3.6.1}$$

3.7 Energy for Charge Carrier Generation in Semiconductor Material

The energy W required to create an e-hole pair in a semiconductor by a fast charged particle traversing the medium depends on the band gap energy E_g of the material and slightly on the temperature. The energy for charge carrier generation is always higher than the band gap energy due to the possible additional excitation of phonon and plasmon states. Phonon excitation transfers energy to the lattice, and the energy transferred appears finally as heat in the detector. W is the mean energy to create an e-hole pair, and it has been calculated and measured in experiments including high-energy charged particles and X-ray photons ([92], [93]). The mean energy W required to create an e-hole pair in silicon is equal to 3.68 ± 0.07 eV [94]. For the most probable energy deposition corresponding to a MIP, the most probable number of charge carriers of about 23,000 pairs in a 300μm thick detector.

3.8 Multiple Coulomb Scattering

The useful thickness of the silicon detector is limited by the desire to keep the depletion voltage low, and more importantly, by the need to limit the effect of multiple scattering of the particle. While passing through material, the particle will undergo multiple Coulomb interactions, which results in a deflection from the original direction. The multiple scattering angle θ_o (see Equation 3.8.1) depends linearly on the inverse of the momentum p and on the square root of the material thickness t in units of a material constant given by the radiation length X_o. For many applications it is sufficient to use θ_0 to capture 98% of the projected angular distribution.

$$\theta_o \approx \frac{13.6MeV}{\beta \cdot \rho} \cdot \sqrt{t/X_o} \tag{3.8.1}$$

Either very thin detectors or high energy particles (or both) are required to obtain good position resolution. The typical silicon detector thickness of 300μm amounts to 0.3% Xo.

3.9 Conclusions

When describing in more detail a silicon detector, silicon is a semiconductor with a moderate band gap of 1.12 eV, which compared with thermal energy levels (kT=1/40eV) allows a low noise detector at room temperature. The energy to create an e-hole pair is 3.6 eV, compared to the ionization energy of 15 eV in Argon gas, leading to an ionization yield for MIP s of about 80 electron-hole (e-hole) pairs per micron. Thus about 23,000 e-hole pairs are produced in the customary detector thickness of 300μm, and collected in about less than 30ns without a gain stage.

Materials other than Si (such as diamond) have been studied to replace silicon as the semi-conductor of choice in tracking devices, but have not been as successful [95], [96]. One reason for the uniqueness of silicon is its wide scientific and commercial development and study, and it has helped to spawn the use of pixel detectors (hybrids, CCD's, CMOS detectors), which has been explained in the previous chapter.

Chapter 4

Belle Experiment Upgrade

Particle physics is the branch of physics that studies the elementary constituents of matter and radiation, and the interactions between them. It is also called HEP, because many elementary particles do not occur under normal circumstances in nature, rather they can be created and detected during energetic collisions of other particles. This chapter is meant to introduce the experimental environment at KEK, which is the facility where the Belle experiment is taking place. The different components of the Belle Detector are detailed. The following sections describe the efforts undertaken with the first two versions of the CAP series of detectors.

4.1 B-Factories and KEK

The KEKB B-factory is an electron-positron energy-asymmetric double-ring collider for B physics. It consists of an 8-GeV electron ring (HER), a 3.5-GeV positron ring (LER) and an injector (J-Linac), as shown in Figure 4.1. Both rings are placed side-by-side in the tunnel originally constructed for Tri Ring Intersecting STorage Accelerators at Nippon (TRISTAN). As of this writing, KEK is the world's accelerator with the highest luminosity. Collisions are observed by the Belle detector located at a single interaction point located in the Tsukuba experimental hall. Construction of KEKB started in 1994 and the first event was observed by Belle in June 1999. After four years of operation, the peak luminosity (as a measure of the collision rate) exceeded the design value of 10/nb/s ($=10^{34}\text{cm}^{-2}\text{s}^{-1}$).

The detector is configured (see Figure 4.2) around a 1.5 T superconducting solenoid and iron structure surrounding the KEKB beams at the Tsukuba interaction region. The beam crossing angle is ± 11mr. B-meson decay vertices are measured by

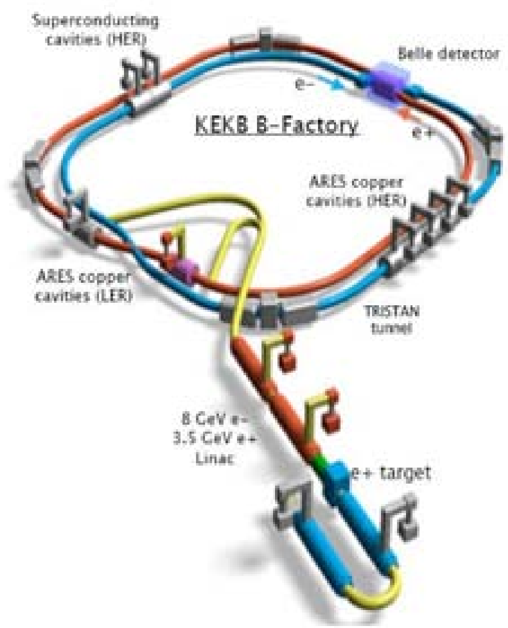


Figure 4.1: General schematic Layout of KEKB, with the Belle detector located in the upper right.

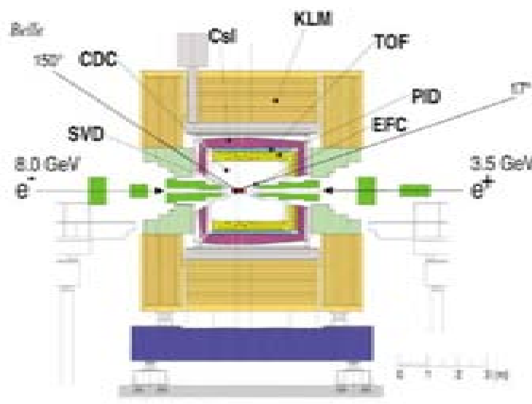


Figure 4.2: Side View of the Belle Detector.

a SVD situated just outside a cylindrical beryllium beam pipe (vacuum chamber). Charge particle tracking is provided by a gaseous wire drift chamber (Central Drift Chamber (CDC)). Particle identification is provided by dE/dx measurements in the CDC, Aerogel threshold Cherenkov Counterss (ACCs) and Time-of-Flights (TOFs), situated radially outside of the CDC. Electromagnetic showers are detected in an array of CsI (T1) crystals located inside the solenoid coil. Muons and K_L mesons are identified by arrays of resistive plate counters interspersed in the iron yoke. The detector covers the polar angle (θ) region extending from 17° to 150°. A part of the otherwise uncovered small-angle region is instrumented with a pair of BGO crystal arrays (Extreme Forward Calorimeter (EFC)) placed on the surfaces of the QCS (superconducting final focus quadrupole magnet) cryostats in the forward and backward directions.

A primary goal of the Belle experiment is to observe time-dependent CP asymmetries in the decays of B mesons. Doing so, requires the measurement of the difference in z-vertex positions for B meson pairs with a precision of $\sim$100μm. In addition, the vertex detector is useful for identifying and measuring the decay vertices of D and τ particles. It also contributes to the tracking. Since most particles of interest in Belle have momenta of 1GeV/c or less, the vertex resolution is dominated by multiple-Coulomb scattering.

4.2 CAP1

A MAPS can provide a detector of fine spatial granularity with information at the pixel level. Charge is collected by diffusion in a region $\sim 10\mu m$ thick. These detectors can be thinned to become a better match in the context of a Super-B factory, where particles are of relatively low momentum. As the electron-positron bunches collide with as little as 2ns temporal separation, the beam is almost DC in terms of the timing structure observed in the detector. Multiple ampere currents in each beam lead to severe radiation doses for operation close to the beam pipe (about 200 kRad/yr-2kGy/yr- recorded in innermost layer of the current Belle Vertex Detector). In contrast with a hadron machine, the bulk damage effects are usually negligible. Occupancy in the innermost silicon layer of the current vertex detector is now 10%. Projections of 20 times higher backgrounds, at planned increased luminosities, will render such a device unusable. Earlier efforts to develop a

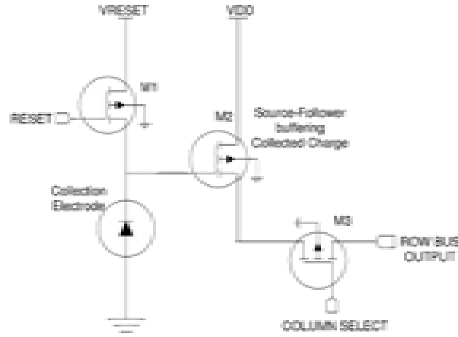


Figure 4.3: Simple three-transistor cell, which is the basis of the CAP1 detector.

hybrid pixel detector for lower luminosity operation, based upon bump bonding of a thinned detector, with thin readout electronics [97], were abandoned.

The first MAPS prototype developed for the Super-B factory upgrade was developed to decrease the high levels of occupancy and also present good signal-to-noise levels even after severe radiation damage. This first prototype was designated CAP1, and uses the basic three-transistor pixel cell, as can be seen in Fig. 4.3. When the gate of transistor M2 is held at a positive voltage relative to the surrounding well and substrate, electrons created in the sensor are collected and induce a voltage change on the gate of M2. As irreducible leakage current in the sensor eventually causes the collection potential to be lost due to negative charging; therefore a periodic reset must be applied to M1 to restore this collection capability. M3 is used as an output select to allow pixel multiplexing onto a readout bus row.

This is the basis of the 6336 pixel cell prototype, organized in 132 columns and 48 rows, with a 0.35μm feature size and a pixel size of 22.5 x 22.5μm^2. The 48 common row output bus line are multiplexed by 4 onto 12 parallel analog outputs. Internal calibration is done by varying the sense transistor gate voltage of a test pixel, thereby calibrating the gain. Noise in CAP1 detector was determined to about 16 e$^-$rms. The leakage current of the unirradiated detector is approximately 320 pA$\cdot$ cm^{-2} with all the measurements at room temperature.

The readout system includes a front-end board with multiplexers, 10-bit Analog-to-Digital Converter (ADC) and serializers. From the serializer, the signals

are converted to Low-voltage differential signaling (LVDS). Custom software was developed to handle data acquisition and readout. This software performs correlated double sampling and leakage substraction, and provides a SNR for each pixel of each CAP detector.

4.2.1 Test Beam Results, Irradiation Studies and Read Out Speed

A first beam test of CAP1 was done in KEK in June 2004 with over 10 days of data collection. The beam consisted of pions of momentum ranging from hundreds of MeV/c to 2-4GeV/c. In this measurement, charged particle tracks recorded by all 4 detectors were used to self-align and determine the hit resolution of the CAP sensor. A Gaussian fit to the residuals exhibits a standard deviation of about 11μm, which gives an upper limit on the hit resolution. Other measurements to study the charge spread in CAP sensor were performed. When a particle crosses the CAP sensor, electron-hole pairs are generated in the $\sim$10μm-thick epitaxial layer, and electrons are collected in 100-200 ns. These measurements are needed to develop efficient clustering algorithms, since they show that the percentage of the charge collected seems to saturate when including 6 pixels or more.

To work in the harsh Super-B factory environment, a detector must be radiation hard. MeV γ irradiation (^{60}Co) was performed for the following doses: 200 kRad, 2 MRad, 3 MRad and 20 MRad. Measurements [98], [75]performed at room temperature show that the CAP1 leakage current is less than 320 pA$\cdot cm^{-2}$ before irradiation, and increases by factors $\sim$8, $\sim$4200, $\sim$4800 and $\sim$22500 for 200 kRad, 2 MRad, 3 MRad, and 20 MRad, respectively, before annealing.

It is important to note that up to 20 MRad the detectors were shown to function properly. It is not clear if the saturation of the leakage current observed by other groups[98] above a couple of MRad was reproduced or not. It should be emphasized that the reduced SNR due to the increase of noise after irradiation could be shown to be acceptable, even for the 20 MRad irradiated detector. The primary concern is the degradation of the charge collection due to the creation of trapping sites in the irradiated sensor.

4.2.2 CAP1 Read-Out Speed and Concept

In the CAP1 prototype, to be able to perform CDS, the pixels must be continuously read out, disregarding the presence of a trigger. Reading out the full-frame pixel data is a time-consuming process, which was further exacerbated by the fact that the pixel data were analyzed *on the fly*, to be recorded only if the SNR of a pixel exceeded a tunable threshold (self-triggered recording mode). For an 8ms integration time, the live time of the CAP1 detector array was on the order of 16%.

4.3 CAP2

The basic CAP1 design is quite simplistic and does not have sufficient frame rate capability to handle the occupancy of the Super-Belle vertex interaction region. Even pushing the readout to its maximum, the latency for acquiring a pair of frames is excessive. To improve this situation, a miniature pipeline can be used inside each pixel. This decouples the frame sampling rate from the readout rate and thus reduces the required raw transfer rate off chip by the ratio of the sampling rate to the trigger rate. Maintaining a 100 kHz sampling rate (10μs integration time) for occupancy reasons, storing data and transferring at a level 1 trigger rate of 10 kHz represents one order of magnitude reduction in data transfer speed.

The layout of this 8-deep pipeline in CAP2 is shown in Fig 4.4. The pixel size (22.5 $\times$ 22.5 μm^2) is kept identical to the CAP1 dimensions. To perform this test, a 2 card scheme was developed. A 10-bit ADC and analog support electronics is included on the FE board (F2). F2 is interfaced to a compact PCI back-end board (B2) via standard Category 5 Ethernet cables. Power and control are provided over RJ-45 cables and data is broadcast via high-speed LVDS serial link (operating at 400 Mb/s). Four F2 are read out into one B2 board. Event acquisition rate for full frame pairs from 4 detectors, including 8 ms integration time, was measured to be approximately 30 Hz (limited by computer processing).

4.3.1 Test Beam Results, Irradiation Studies and Read Out Speed

Test of an array of 4 CAP2 detectors in the KEK pi2 beam line was made during the beginning of June 2004. An example of a self-triggered 4-layer event is seen in Fig 4.5. Irradiation of a couple of CAP devices has been performed with a

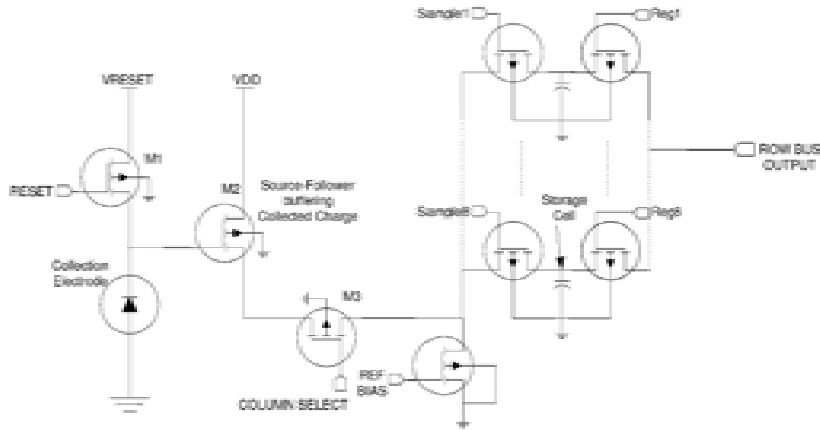


Figure 4.4: Schematic of a CAP2 pixel. Eight storage cells are available for each pixel with decoupled write and read selects.

^{60}Co irradiator. The leakage current values have been compared to [98], which have demonstrated survival to 30 Mrad. As can be seen in Fig 4.6, for dose rates above about 5 Mrad, the leakage current seems to saturate with proper annealing [76].

4.3.2 CAP2 Read-Out Speed and Concept

CAP2 was designed in order to enhance the live time of the CAP by recording data in an eight-deep pipeline in each pixel cell. The trigger can then be externally provided, the integration time can be drastically reduced, and the live time of the detector depends only on the trigger frequency, taking into account that about 1 ms is needed to read out each frame. A 15μ s frame acquisition time has been used with CAP2. The CAP2 prototype shows an increased noise (30 electrons noise measured) compared to CAP1. The mini-pipeline output level dispersion is quite large within the pixels, which requires eight separate lookup tables for the eight possible buffer transitions.

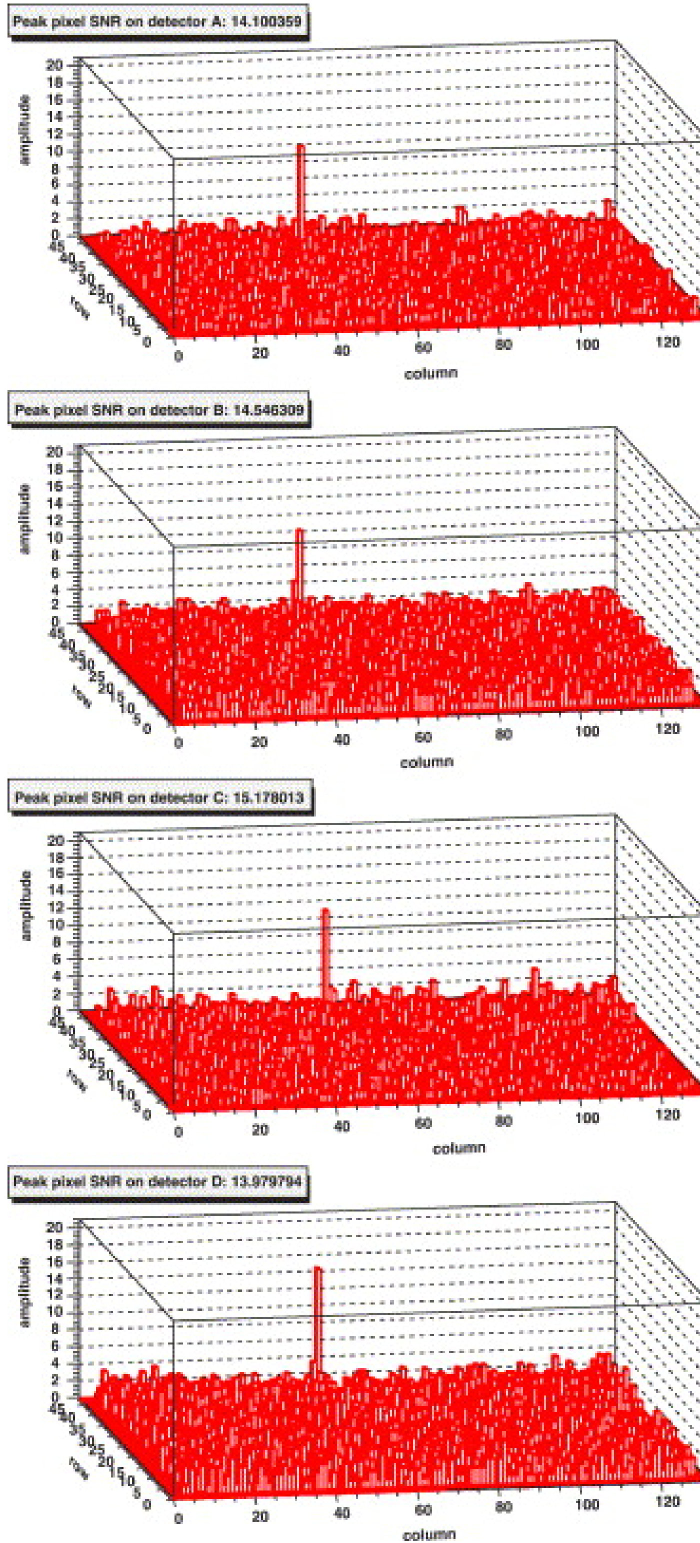


Figure 4.5: A sample thoughgoing 4GeV/c pion track in the 4 layer detector configuration of the pi-2 beam test.

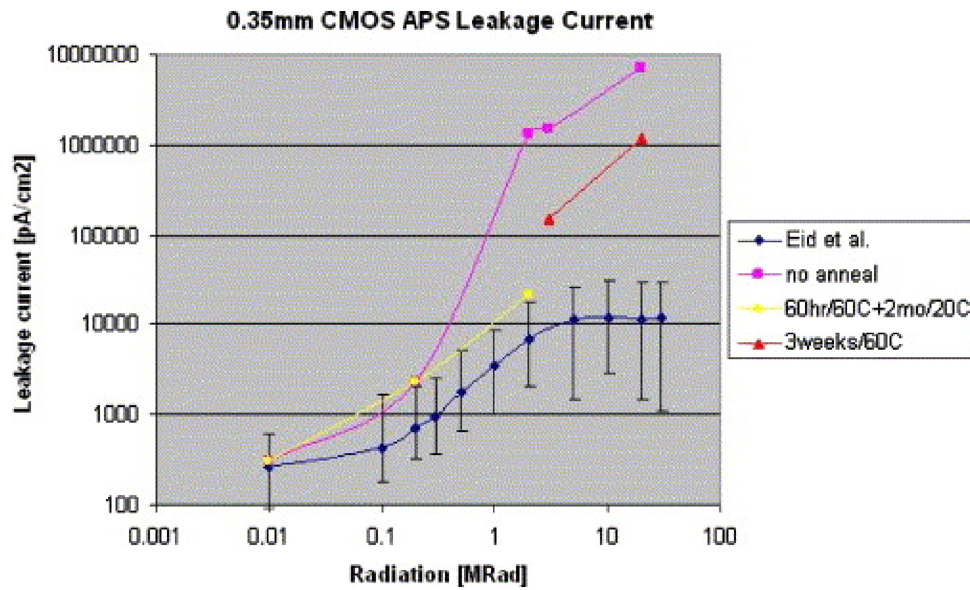


Figure 4.6: Measured leakage current versus MeV gamma irradiation dose.

4.4 Conclusions

The promising results obtained, with both CAP1 and CAP2, encouraged the team to make a step forward in the design and development of the CAP3 prototype. The next aspect to test was to reliability of the next prototype detector (that could be obtained with the architecture and technology previously used) to work in a more realistic environment. To perform such test, a detector size prototype was needed to make sure that the needs in data processing speed were accomplished. The next chapter describes the characteristics of CAP3, as well as the results obtained.

Chapter 5

Continuous Acquisition Pixel 3 *(CAP3)*

Based upon the results obtained with CAP1 and CAP2, the next member of the CAP family was designed and tested with expectations for improvement over the performance already obtained. CAP3 is a full-size detector prototype (21mm$\times$3mm) that evaluates critically the CDS structure used before in terms of speed and signal quality. The first section describes the architecture used and a brief overview of the timing and signals used for the read-out. The next section will describe the testing results obtained. The experimental results includes all the tests performed. These tests start from the most basic testing where the transfer curve and the noise in saturation are obtained. The next tests exposed are a more complex analysis, where the laser is used. This extensive test includes more noise analysis, optimization of the laser spot and analysis of the unformity in x-y axis. The last study is about the spill-over and pipeline.

5.1 Description of CAP3

Based on the successful operation of CAP1 and CAP2 prototypes, design concept studies and plans for the next stages of R&D [99] towards a full-size Pixel Vertex Detector (PVD) were undertaken and the third generation of CAP prototypes was developed. The CAP3 was designed and fabricated in the TSMC 0.25μm process. Fabrication cost of a chip increases considerably at larger die sizes and for the case of CAP3 was limited to 21$\times$3mm^2. CAP3 prototype was designed as array of a 928$\times$128 pixels at 22.5μm pitch, with a 5 deep sample pair pipeline in

each pixel. While these could be treated as 10 independent samples, they have been treated as 5 pairs of CDS for operational convenience (see Figure 5.4 for a detailed schematic). The $\sim 120\times 10^3$ pixels of a single CAP3 chip corresponds roughly to the total number of the read-out channels of the present entire DSSD based SVD2 [100]. The critical point for making a read-out system practical is the ability to handle the enormous amount of data intrinsic to such a finely segmented detector.

As with the CAP2 prototype, the decoupling of the sampling frequency from the read-out frequency makes it possible to reduce the required data flow from CAP3, which would nevertheless at a 10 kHz trigger rate still correspond to about 1.2×10^9 sample pairs per second per detector. Data are transferred via 32 signal channels, with rates of about 100MHz, to meet latency requirements. The CAP3 readout follows the two-card scheme developed for previous CAP1-CAP2 prototypes, with the necessary modifications of the FE board (see Fig. 5.1) so that it can accommodate the new detector (see Fig 5.2). The FE board includes a 16-bit ADC and the analog support electronics. To have maximal flexibility in the testing of the sensors, CAP3 is wire-bonded to a separate carrier board, which is pluggable into the FE board. Four 60-pin connectors on the FE board allow for mechanically stable stacking of boards and bring the power supply voltages from a separate power board at the bottom of the stack. Each FE board is connected to a compact PCI Back-End (BE) board (see Fig 5.3) via two standard CAT5 Ethernet cables: one transferring the control signals and the other transferring data at approximately 400 Mb/s. Four FE boards can be read out into a single BE board to simplify event synchronization when operating with an array of up to four detectors. The data from the BE board is read out by an embedded CPU running a Linux OS via a PCI interface.

5.2 Testing Results

The basic testing started (see Fig 5.4) allowing the transfer of information through one storage cell (closing $S0$ and $SS0$) and with fixed readout switches (CPS0 closed). The other switches are opened. This exercise show us the transfer curve of the complete structure in static conditions, as can be seen in Fig. 5.5.

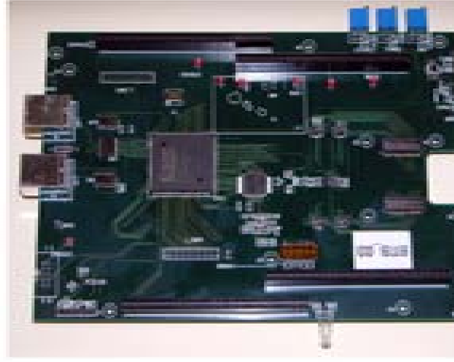


Figure 5.1: Front-End board (FE) with ADC converter, analog support electronics and connectors.

Figure 5.2: CAP3 prototype bonded to a separate board for use with the FE board.

Figure 5.3: Back-End board (BE) ready to be used with 4 FE boards.

The cell-to-cell readout has also been studied. Looking at different storage cells in the same operation conditions, differences as high as 500mV are obtained. These differences are coming from transistor mismatch that affects the smallest transistor geometry transistors (M2), producing leakage current variation and introducing layout dependence to the storage. An analysis of the pre-sample and post-sample (S0 and S1) also show a systematic difference of ~500mV, where the pre-sample is higher than the post-sample. Considering a pixel capacitance of ~3fF, the leakage current can be measured directly by applying A_{reset}=0V, where A_{reset} is the voltage applied to the gate of the reset transistor (M1 at Fig. 5.4). A leakage current of 1.5fA is obtained at V_{DD}=2.5V. This value shows a strong dependence on V_{DD}. The leakage current increases by a factor of 3, when using a V_{DD} of 2.7V. If the V_{DD} is decreased down to 2.3V, the value of the leakage current will decrease

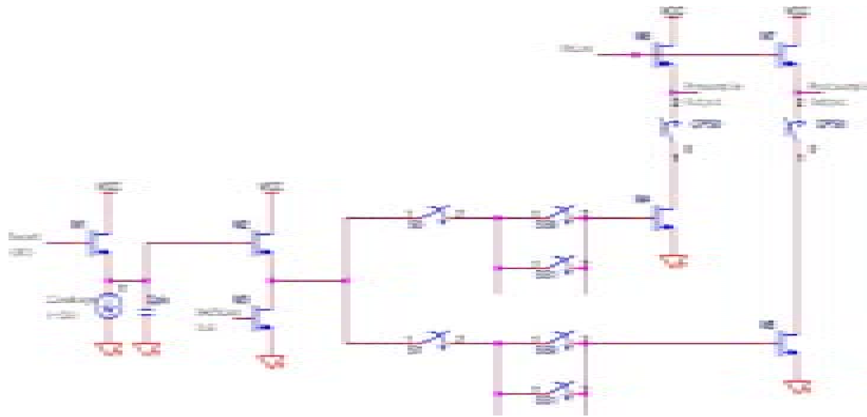


Figure 5.4: Schematic used for CAP3 testing.

by a factor of 3.

5.2.1 Noise Measurement

The next measurement was a noise measurement as seen in Fig 5.6. It was found that the increase of a storage cell number did not lead to a large increase of the noise for CAP3, in saturation ($<25e^{-}$), compared with the results for the CAP1 (< 16 e^{-}) and CAP2 (< 35 e^{-}). The read-out technique is CDS, where sample pairs are used. This technique was already used in CAP2. The improved noise is partially attributable to the reduction in FPN due to the differential readout of the two sample pairs, coincident in time. This result confirmed that the differential readout scheme successfully reduced the system noise pick-up.

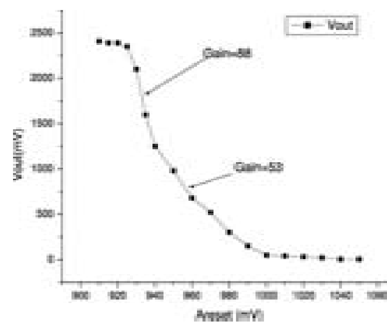


Figure 5.5: Transfer function obtained from CAP3 testing.

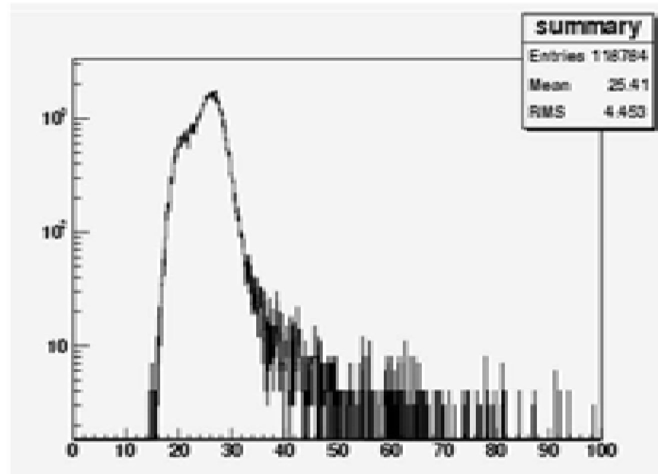


Figure 5.6: Noise distribution for the 118,784 pixels of a CAP3 sensor. The mean noise is around 25e^{-}.

5.3 Laser Testing

Tests of the detector response and performance of the CDS pipelined read-out were made using a laser test bench. As the front of the CAP3 is covered with 5 metal layers to accommodate the connections between the 3T cells and storage cells, which reflect light, the sensors had to be back-plane illuminated with an Infrared (IR) laser (960 nm) which can penetrate through 250 μm of the Si bulk.

5.3.1 DC initial results

Initial results were obtained with the Laser Setup used in a DC configuration. The laser set-up configuration can be: DC and pulsed mode. Two schematics of the different configuration are explained in Fig. 5.7 and in Fig. 5.8.

Figures 5.9 and 5.10 show the analog values corresponding to one pad. In this configuration every pad is responsible for the read-out of 8 different rows and the read out speed corresponds to 40kHz (25μs time frame per value). The readout sequence is done column by column, and then shifting the results through the row, going from the pads to the end of the sensor. Good sensitivity to a laser dc signal is obtained, showing beam spread of ~1.3mm and good x-axis sensitivity results (moving the laser in the reading out row is clearly seen on the oscilloscope, showing a linear relation with motor movement and pixel distance). When adjusting the

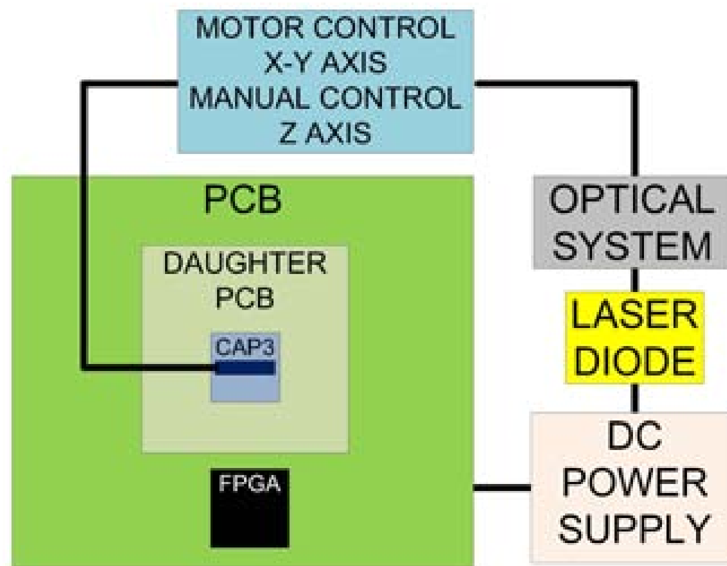


Figure 5.7: Schematic of the DC Laser set-up configuration. This configuration includes the two PCBs, the one that contains all the circuitry needed (including the FPGA) and the one that holds the CAP3. This board is biased using a Power Supply, which also supplies the laser diode directly. Light output is modulated by controlling the amount of current provided to the laser diode. The signal generated at the laser diode is adjusted using an optical system that focuses the signal at the input of a fiber cable. The end of the fiber cable position (on top of the CAP3) is controlled in x-y-z axis by a stage that can be control manually in all axes and be optionally controlled from a computer for the x-y axis.

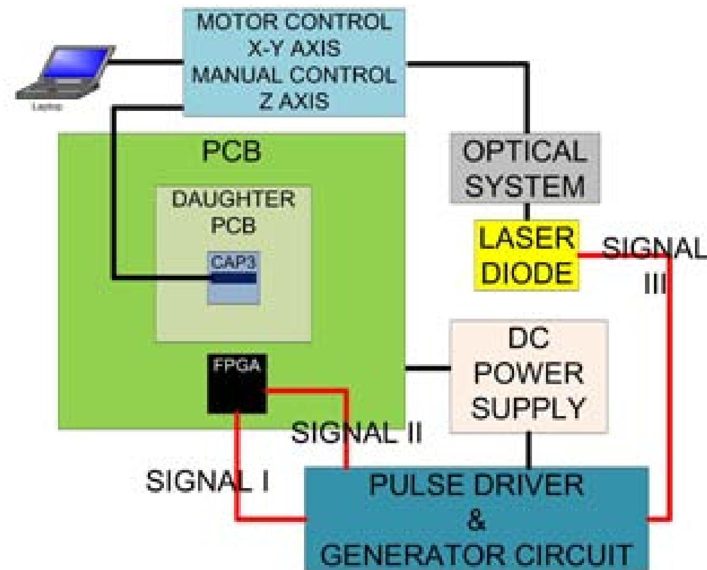


Figure 5.8: Schematic of the Pulsed-Mode Laser set-up configuration. This configuration includes the two PCBs, the one that contains all the circuitry needed (including the FPGA) and the one that holds the CAP3. This board is biased by the Power Supply. The Power Supply also biases the Pulse Drive & the Generator Circuit. The FPGA generates a trigger signal (that can optionally provided by function generator) that is sent to the Generator Circuit as Signal I. The amount of current provided to the laser driver must be controlled, as well as the pulse width of the laser. This control signal is adjusted to voltage levels, now is called Signal II, and it can be detected by the FPGA. The same signal with no voltage level adjustment is used to drive the laser diode. This configuration is extremely safe because the current provided to the laser diode is limited by the Generator circuit. The signal generated at the laser diode is adjusted using an optical system that focuses the signal at the input of a fiber cable. The end of the fiber cable position (on top of the CAP3) is controlled in x-y-z axis by a stage that can be controll manually in all axis and optionally controlled from a computer for the x-y axis.

laser diode operation to $V_{applied}$=1.69V, ΔV= 0.67V is obtained, showing a high dependence on the ambient light and forcing to work in tight light conditions.

Figure 5.9: Measured pad output results when the PCB is covered, no lab light and a DC signal is applied to the laser diode. Left side of the Figure shows a lower noise level compared to the right side (far from the bonding pads).

Figure 5.10: Measured output results when the Printed Circuit Board (PCB) is uncovered, lab lights on and a DC signal is applied to the laser diode.

These initial measurements show a bump width of 1.3mm for the laser and the shifting of the laser signal through the pixel array using the motor[1] a distance of 45mm results in a shift of the signal in 4.2 ms (equivalent of 21 cells).

5.3.2 Noise analysis of the 16 Output PADS

The next test performed was to analyze the different behavior between output pads. There are 16 output pads and, as can be seen in Fig. 5.11 and Fig. 5.12, different mean values are found on each of them when doing a DC measurements without any laser signal applied. Every output pad displays the information for 8 rows, and one pixel located in the middle of the chip has been selected to perform the read-out test. Apart from initial analysis, a comparison for the different storage cell values [2] can be seen (for these measurements all oscilloscope probes were

[1] The configuration used at the laser set-up is by two stepping motors for the x-y axis and a manual translation screw for the z axis. It also includes a 980 nm laser with 5 mm diameter and an output power 15 mW. More details can be found at Chapter 6

[2] The configuration of CAP3 is used to perform a CDS read-out with 5 different pairs of samples, the storage cell number mention here correspond to the number of pair samples, that will go from 1 to 5

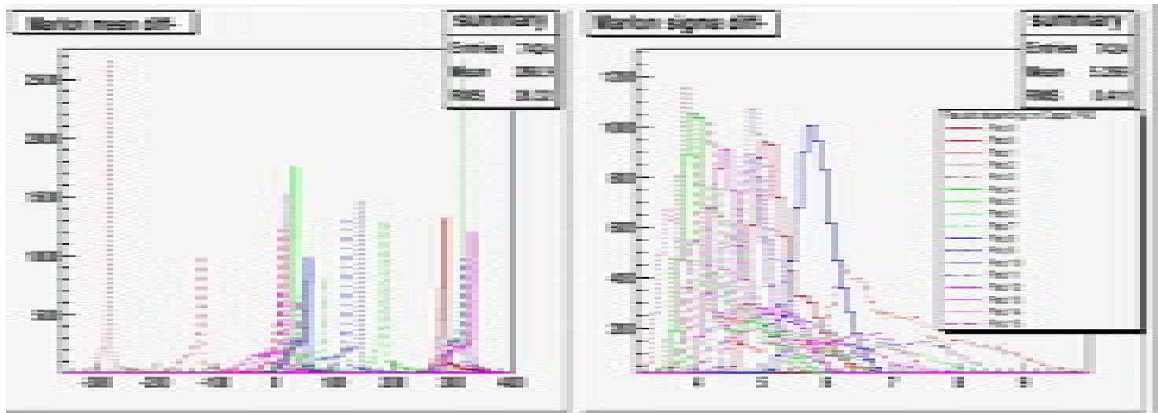


Figure 5.11: Analysis of the output pad amplifier offsets when using storage cell number 1 for the read out for a pixel located in the middle of the CAP3 array.

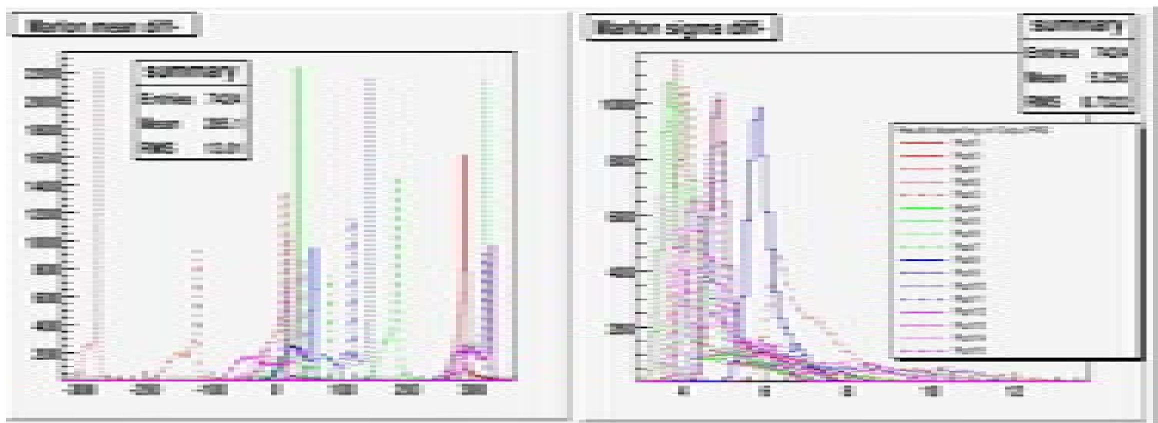


Figure 5.12: Analysis of the pad performance when using storage cell number 3 for the read out for a pixel located in the middle of the CAP3.

removed, their presence was determined to add to the observed noise sigma value). Fig. 5.11 shows the results obtained for the storage cell number 1 and Fig. 5.12 for storage cell number 3. For each output pad in both figures, similar behavior is seen, though it is not exactly the same. This can be seen by looking at pad8; in Fig. 5.11 the sigma shows more dispersion in comparison to Fig. 5.12, although both of them are centered around the same mean value.

Initial results for the analysis of a single event when a DC laser signal is applied can be seen in the following pictures lego plot representations (see Fig. 5.13) and a 2D cut (see Fig. 5.14). The lego representation shows that the peaks observed before (Fig. 5.11 and 5.12), did not actually have a high impact in the representation

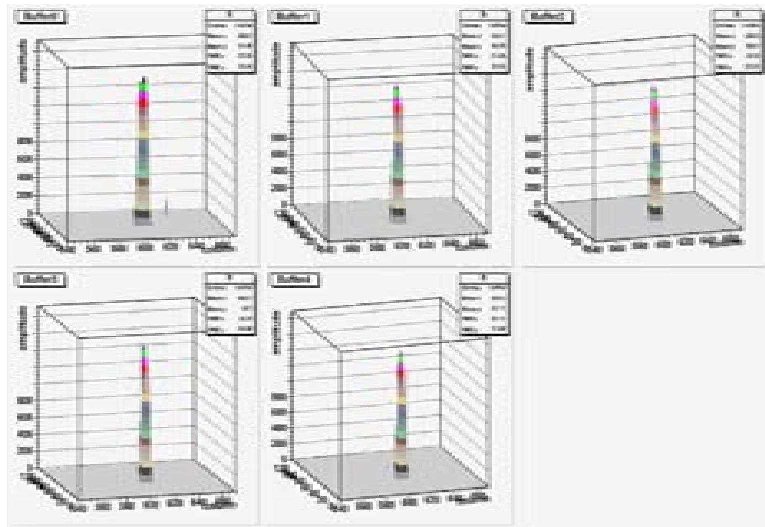


Figure 5.13: Lego plot representation of a single event with a DC laser signal.

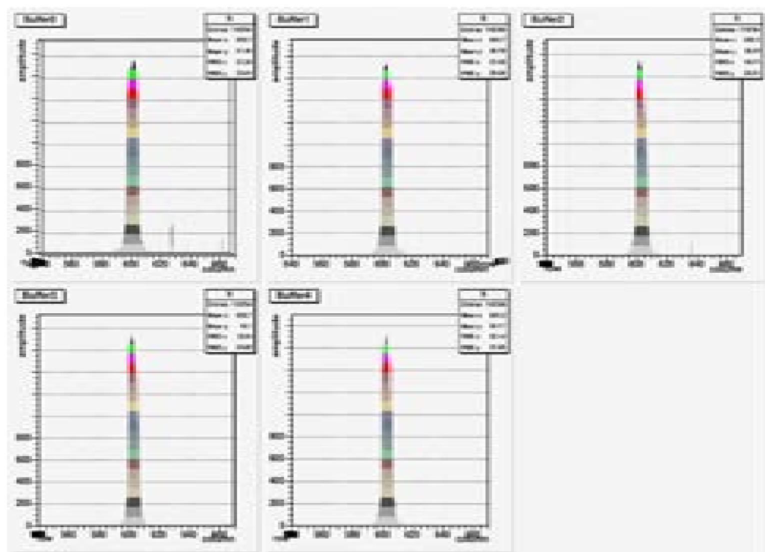


Figure 5.14: 2D representation of a single event with a DC laser signal.

of a DC signal. The plots also show an equal response for the 5 storage cells for this case.

5.3.3 Noise analysis of 9 pixels

A new study was done considering 300 events for 9 specific pixels. The results obtained here are shown in Fig. 5.15. Every color represents a different storage cell response. It does not show a similar response for the nine pixels selected. It seems to present a repetitive shift to higher values for storage cell 0. This fact

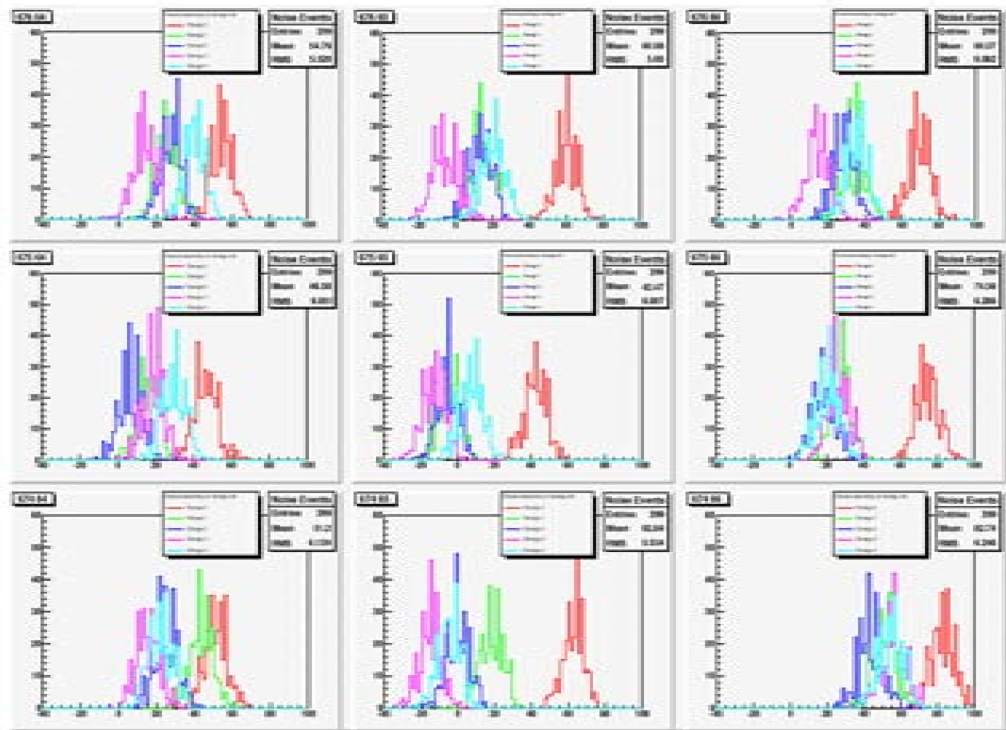


Figure 5.15: Analysis of the noise for 9 pixels (see top left corner at each plot for corresponding location, with the top left location of (676, 64) and bottom right location of (674,66)) depending on the storage cell (SC) used (0 to 4) to perform read out.

seemed initially to be pure coincidence, but indeed, looking more closely at the data for buffers 0 to 4 in Section5.3.2 it seems it is not a coincidence. In Fig 5.11 and Fig 5.12 the mean for buffer 0 (about 304) is displaced from the other 4 means (between 280 and 290). So not only is this shift there for 9 pixels out of 120000, but in the bigger picture, it is a systematic effect. The most probable reason for this is *common-mode* noise and the effects specific to the layout of this design.

5.3.4 Z scan

Fig. 5.16 shows the scan performed (from top left to 2nd plot bottom right), by steps of 2 turns of the high precision Mitutoyo z translation screw, where 1 turn is ∼0.6-0.7mm. Only a reduced portion of the pixel array is shown to improve the image quality of the laser spot. These curves show a minimum around position *10*, of less than 35 pixels. Unfortunately, more careful observation of the beam spot

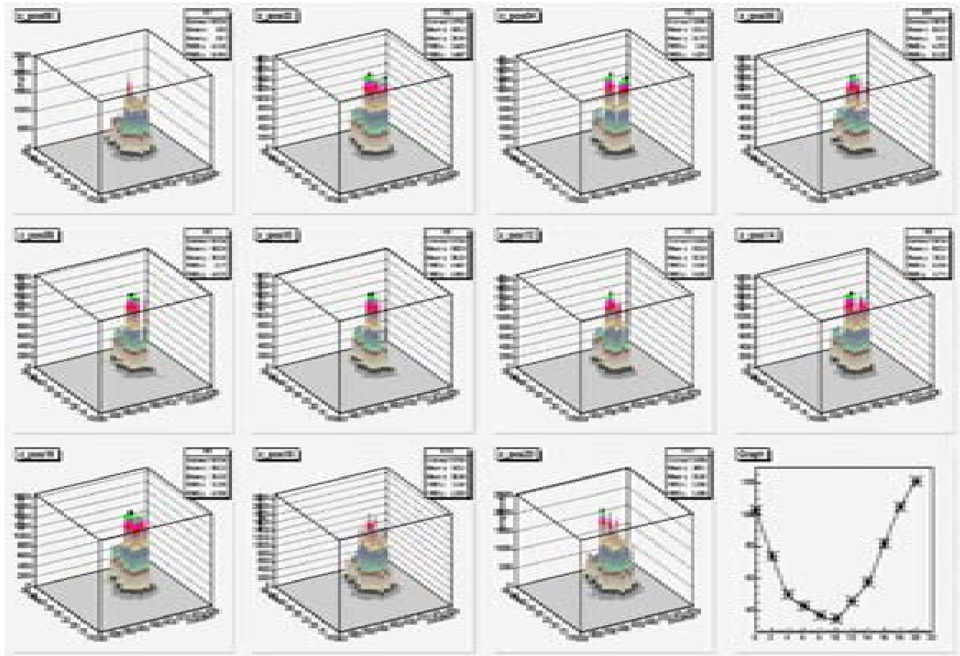


Figure 5.16: Z-scan results using a DC laser signal to minimize the size of the laser spot. Bottom right plot is a representation of the number of pixel above a significance of 50.

(Fig. 5.17) around this position shows that there is quite a bit of structure in the spot detected. Fig. 5.18 clearly shows some *ring* structure appearing for z position 02 to 14. The origin of this ring structure is mostly due to diffraction of the laser light [3]. The laser fiber core is 50μm, the wavelength of the laser diode is 980nm and the distance from the last focusing lens to the detector is about 3mm. It shows a distance between minimums of diffraction of $\sim$70μm, this number agrees with the x-axis ($\sim$150μm) and y-axis ($\sim$200μm) distances between minimums. The other reason for this ring pattern is the non-uniformity of the chip, which impacts the results by taking some of the pixels to saturation high or low. This effect explains some of the non-smooth figures obtained, but not the ring pattern.

5.3.5 CAP3 Uniformity

The next aspect to analyze was the uniformity through the pixel array. Trying to perform a uniform laser illumination of the pixel array is difficult, so a different approach has been chosen. The alternative approach is based on the se-

[3]The interaction with particles of dust on the top layer of the detector is the second possible cause, although it was impossible to proof with a *completely clean* CAP3

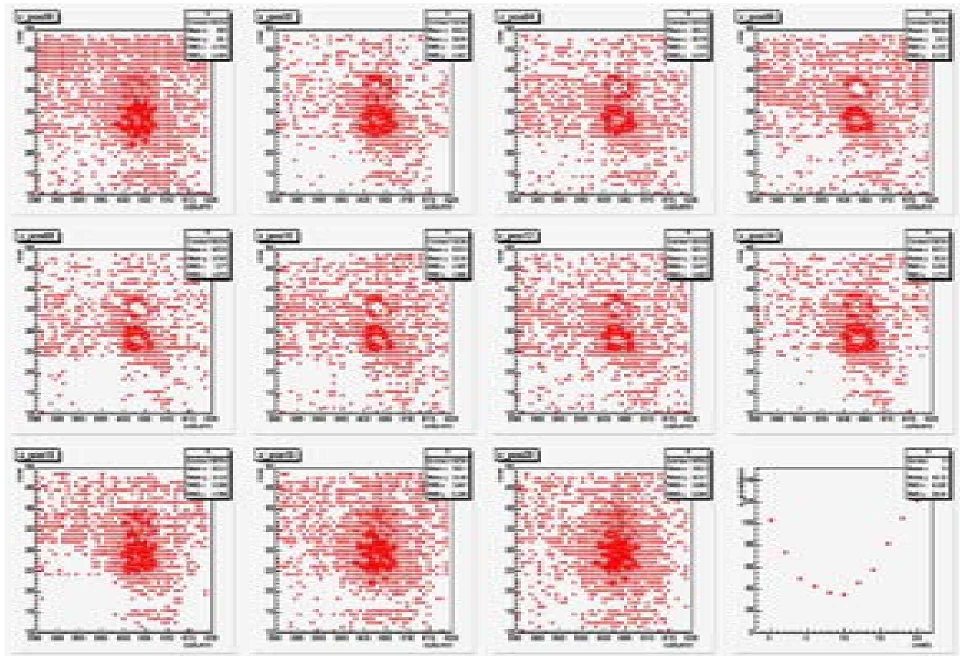


Figure 5.17: Intensity plot of the z-scan results. A ring structure can be seen from pos02 to pos12.

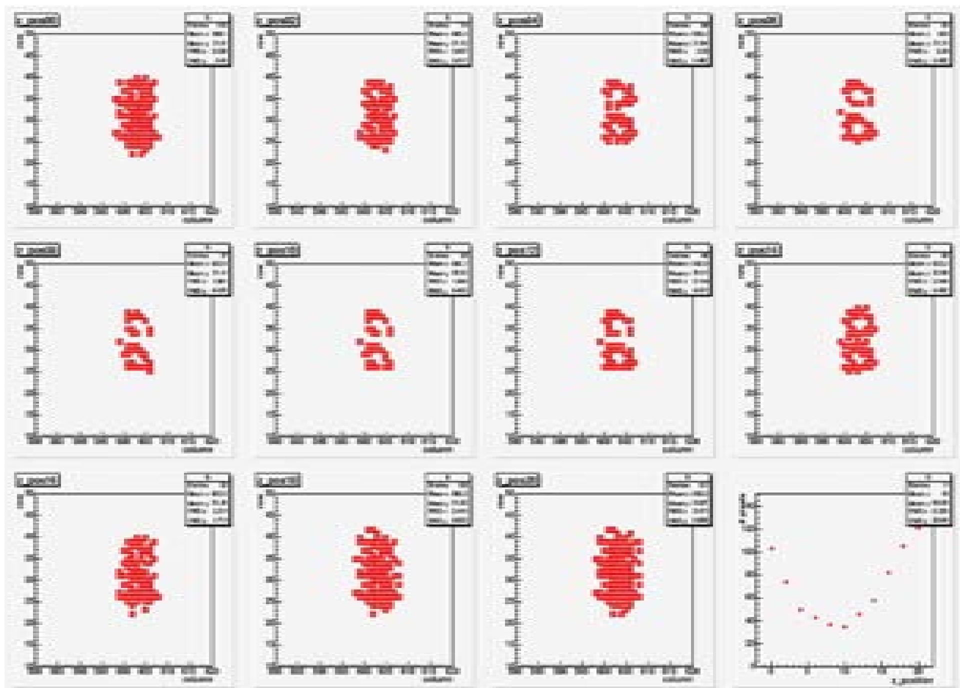


Figure 5.18: Intensity plot of the z-scan results, with an arbitrary normalization to one of the points. A ring structure can be seen from pos02 to pos12.

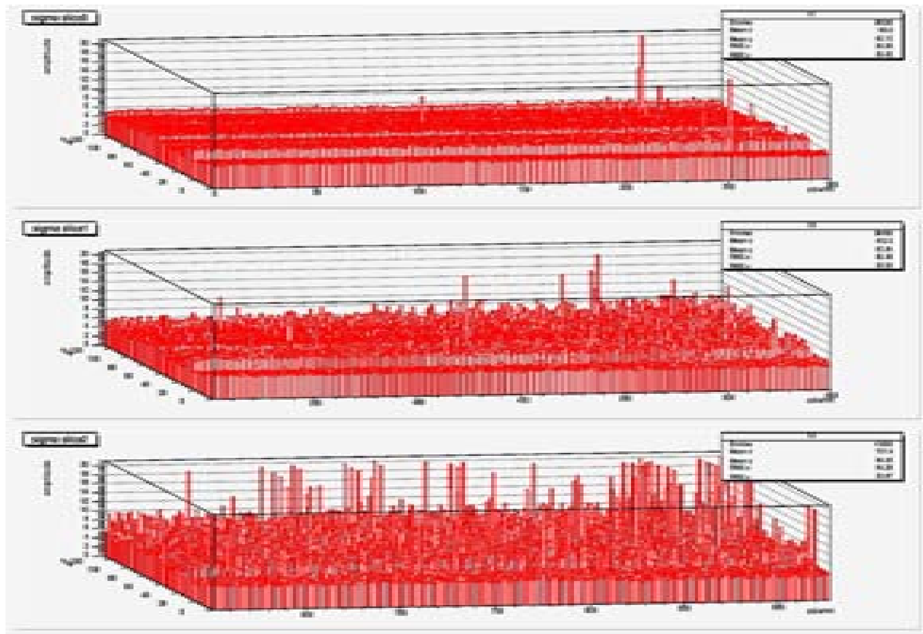


Figure 5.19: Noise map of the complete CAP3.

lection of an operation point that will give room for signal detection. That means that some pixels will be in saturation. They will be considered to be saturated *low* when they show a low output voltage, they will show a very low sensitivy to an input signal. As well, if these pixels are too high (with a high output voltage), they might be a saturation high and again a part of the sensitivity at the detector will be lost. To summarize, this loss of sensitivity at low and high saturation might seem to have a very little effect, but when using a laser input signal will clearly not help to obtain a sensitivity map of the sensor.

A clearer picture can be obtained by mapping the σ/noise of the pixels throughout the pixel array. This is also difficult to show because of the high number of pixels, but here are a few plots that show the complete CAP3 pixel noise map (see at Fig. 5.19). The CAP3 pixel array is sliced in three pieces in these plots, from column 0 to 300, from column 301 to 600, and from column 601 to 927 (all rows shown). Note that the *amplitude* axis is always kept at 20 to allow direct comparison. One can very clearly see the 16-fold structure (*8-row multiplexing* effect) and also the increase of noise when going from slice 0 (small column number) to slice 2 (high

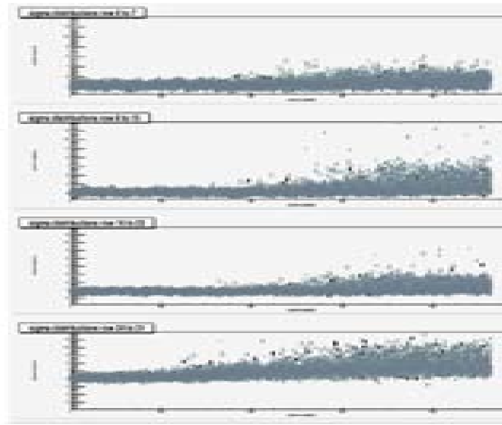


Figure 5.20: Noise map of CAP3 rows 0-31.

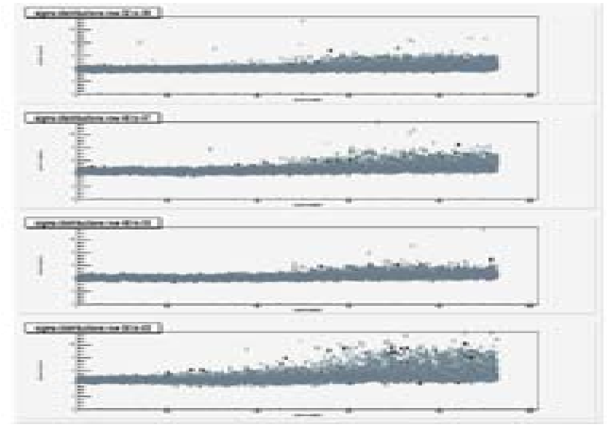


Figure 5.21: Noise map of CAP3 rows 32-63.

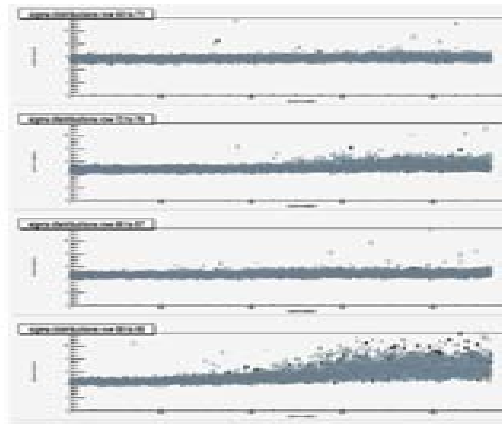


Figure 5.22: Noise map of CAP3 rows 64-95.

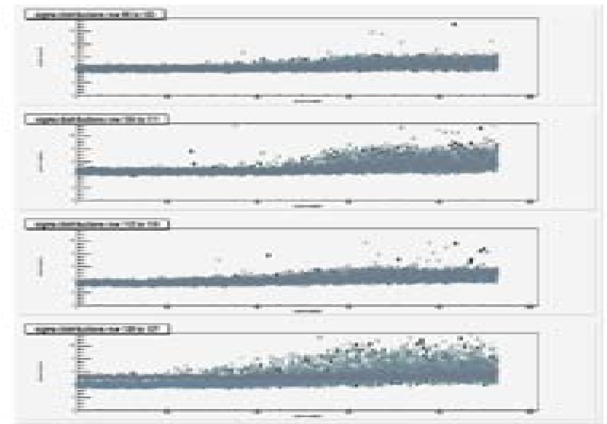


Figure 5.23: Noise map of CAP3 rows 95-127.

column number). Pixels in slice 0 are more in saturation (low voltage out) than pixels in slice 2 (higher voltage out).

Another way to show these data is by showing the noise row by row: see row 0-31 (see Fig. 5.20, row 32-63 (see Fig. 5.21, row 64-95 (see Fig. 5.22, and row 96-127 (see Fig. 5.23). In each of the plots, 8 adjacent rows are shown in the same graph. The increase of noise as a function of column number can be seen.

The result of the scan in the y axis of the pixel array when the laser is operated in DC mode is shown as a sequence of images, each one of them representing the movement in 8 pixel steps. See SectionA.1 for a complete sequence. Several features can be observed. At low row number (beginning of the sequence of images), there is a strange coupling appearing as peaks at high row number (to see a good example look at Fig. A.2). A few hypotheses were given, from data scrambling, light reflection (due to the overlay of the PCB and the sensor) to some noise coupling. These hypotheses have not been confirmed and are hard to understand. Data scrambling can not be the only reason, because the height of the generated peak is not as high as the standard laser (see Fig. A.2). The light reflection cannot also be the only reason because this effect seems to appear in the last 8 rows. This last fact seems to encourage the idea of a noise source, although it could not be proven. When the laser spot reaches the other side of the pixel array (high row number), there are some rings appearing. It initially seemed an optical effect due to the overlay PCB/sensor, but a closer look at Fig. A.11 seems to make this idea not valid. The ring structures are structured row-wise, in groups of 4 (and each 4 belonging to the same pad output). There was no reasonable explanation for this behavior.

5.3.6 X scan with CAP3

A scan in the X axis with the laser was performed, from column 928 to column ∼420 (maximum range for the X stage). A partial sequence of the X scan can be found at A.2. For these images, the laser was operated in DC mode. The bottom plot shows the signal recorded (the plotted signal is the result of the difference between the event data and the mean value) whereas the top plot shows a hit for each pixel above a significance of 4.5 (the significance is defined as the difference between the event data and the mean value divided by the sigma of the corresponding pixel). The main features observed are that there is detection of some pixels that are always noisy, like the one located at column 790, row 120. There are also some fluctuations in the overall level of noise observed throughout the array. This might very well be linked to fluctuations of the baseline (linked to a light leak, or to some noise coupling). It can be checked that a choice of a higher significance cut diminishes the number of noisy pixels, see A.2 to see results for a significance of 10. The 8-row multiplexing effect (this is because 8 adjacent rows share the same

data path) is here very visible in the amplitude of the signal that is recorded. Some calibration of the detector has been provided for fluctuations of the baseline as well as to compensate for the variations due to the 8-row multiplexing effect.

5.3.7 Calibration Coefficients for CAP3

The read-out scheme of CAP3 is based on 16 output amplifiers and 16 output pads. Each of these pads transfers the information corresponding to 8 different rows. The read-out speed has been decreased to be able to overcome any delay that could be introduced by the long output bus lines present in CAP3. The fact that there are 8 different rows to read-out also affects the way they are transmitted by the analog multiplexer included in the design. This kind of behavior will distort the image that is being analyzed, introducing an artifact. That kind of distorsion is very clear in the vertical axis of the image and can be treated as a factor in the aspect ratio of each one of the pads.

A set of calibration coefficients for each of the 16 by 8-row multiplexors has been calculated from the noise value of the Y-scan. The details of this calculation are based on a sum over all the amplitudes and number of the noise pixels, with the requirement that the mean subtracted amplitude should be greater than zero for column numbers between 650 and 928 (based on a physical limitation). Then a calculation of the mean noise for each multiplexer as the amplitude sum divided by the number is done. Finally the coefficient for each multiplexer is proportional to the inverse of the mean noise. Here are the comparison for the calibrated and original laser plot for different events in the total of the Y-scan: 60 (see Figure 5.24 for original versus 5.25 for the calibrated), 120 (see Figure 5.26 for original versus 5.27 for the calibrated), 180 (see Figure 5.28 for original versus 5.29 for the calibrated). The small amplitude region in the upper (larger row number) spot is thought to be a laser reflection, which migrates from multiplexer output 10(row 80-87) for event 60, to multiplexer output 9(row 72-79) in event 180. The scale factors for the 16 multiplexers used in the previous Figures are (from 0 to 15) = {1.25, 1.09, 1.15, 0.68, 1.24, 1.08, 1.21, 0.80, 1.84, 1.20, 1.69, 0.69, 1.28, 0.80, 0.92, 0.63}

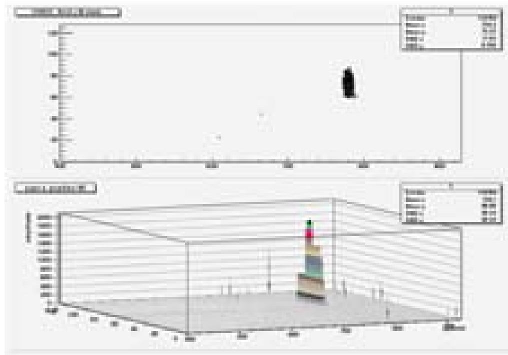


Figure 5.24: Laser Signal for event 60.

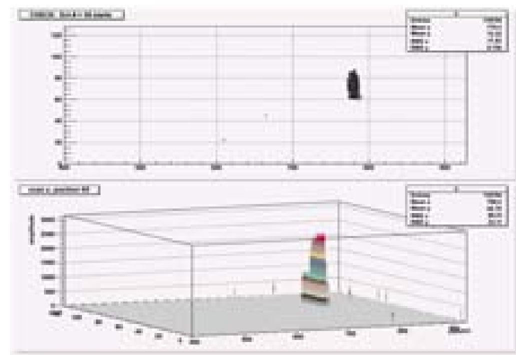


Figure 5.25: Laser Signal calibrated for event 60.

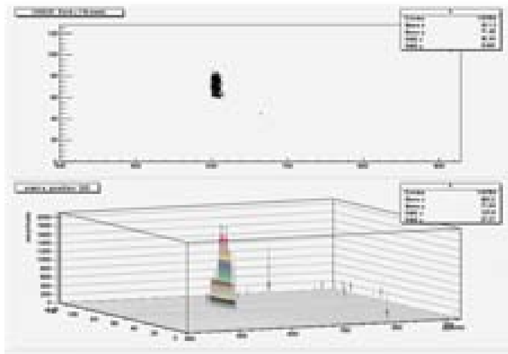


Figure 5.26: Laser Signal for event 120.

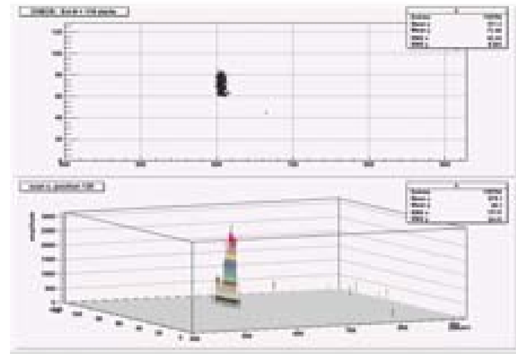


Figure 5.27: Laser Signal calibrated for event 120.

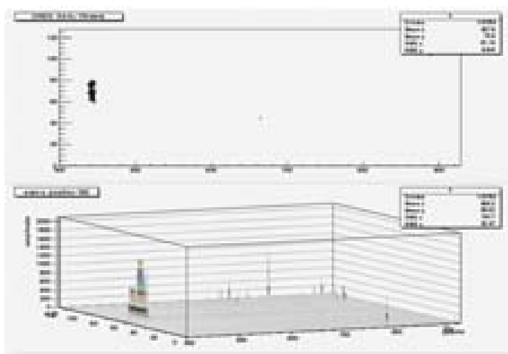


Figure 5.28: Laser Signal for event 180.

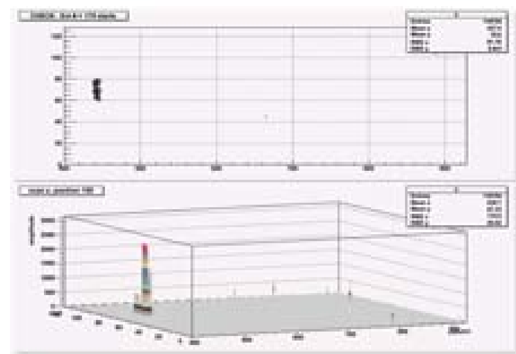


Figure 5.29: Laser Signal calibrated for event 180.

5.3.8 Laser spot and noise value plot for X scan

The following plots are a representation of the mean laser spot column and row number for the laser spot for each event. They are obtained by getting the pixels where the laser is on, by picking the pixels with a big significance and value for the signal amplitude in/around the laser spot, and then calculate the mean and error for the chosen pixels in the dimension x(col) and y(row) for each event. The bottom two plots are for the average noise level of each event with the laser spot region excluded. Left figure is for the whole X-scan region and right figure is for the region with (col >650). The excluded region in the noise calculation for the laser spot is shown for Event 60 at Figure 5.31, Event 120 at Figure 5.32 and Event 180 at Figure 5.33, as a red box in the upper plot.

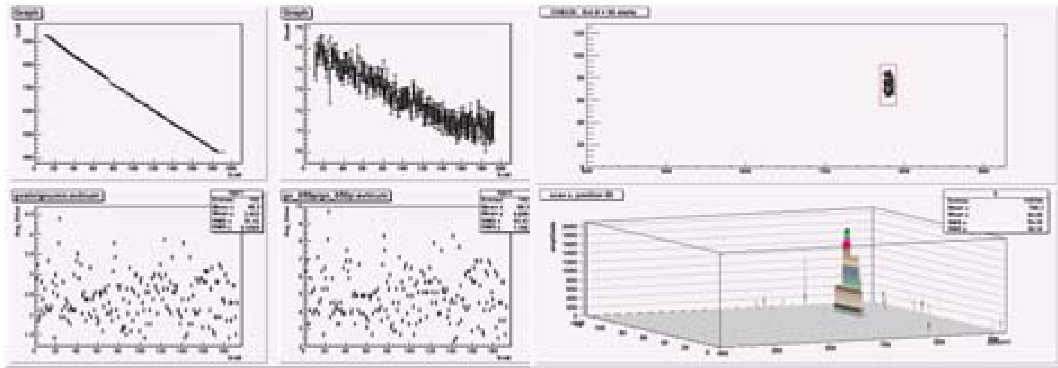


Figure 5.30: Spot column and row number for the X scan.

Figure 5.31: Excluded region for Event 60.

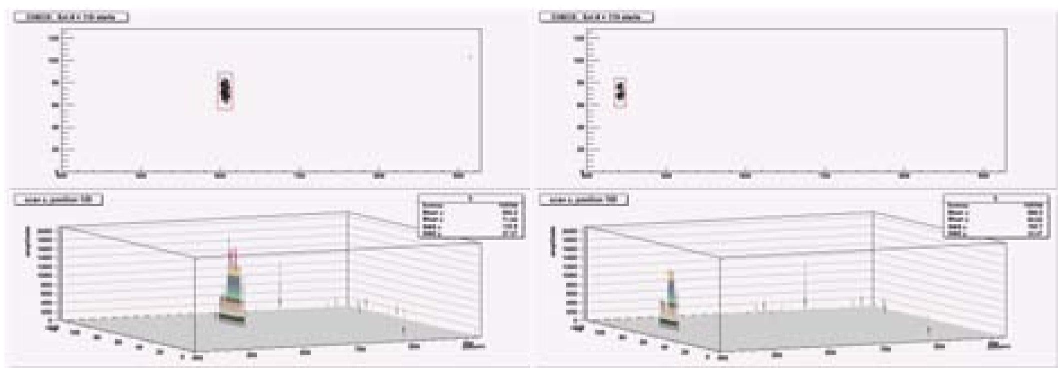


Figure 5.32: Excluded region for Event 120.

Figure 5.33: Excluded region for Event 180.

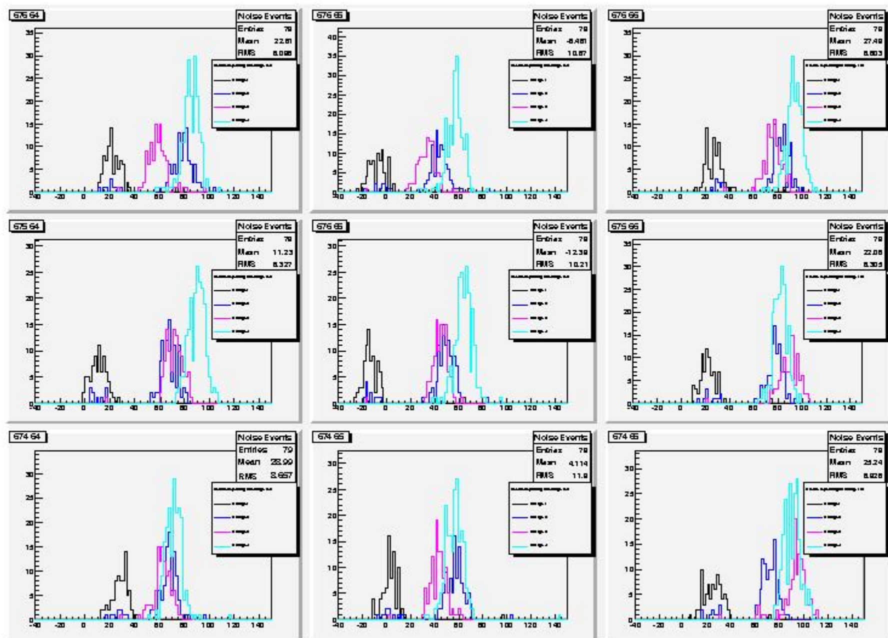


Figure 5.34: 9 cells noise acquisition results.

5.3.9 Pipeline Preliminary test results: noise measurement

In order to start working with pipelined data and to obtain information from any of the storage cells, a number of different noise studies have been performed. Initially similar results to Section 5.3.3 are found as can be seen at Figure 5.34 where the noise acquisition results for 9 cells are presented. The other results obtained correspond to the noise measurement when measuring 500 events for the different storage cells: for storage cell 1 see Figure 5.35, for storage cell 2 see Figure 5.36, for storage cell 3 see Figure 5.37, for storage cell 4 see Figure 5.38 and for storage cell 5 see Figure 5.39.

5.3.10 Pipeline/Pulsed laser preliminary test results: laser $_{pulsewidth}$ vs recorded signal

When using the Pulsed laser (see Fig. 5.7 and in Fig. 5.8 for an schematic of this mode in comparison of the DC mode) there were two kind of problems found at the output signal. The first one is that depending on pulse width, the trigger out and the laser pulse become asynchronous: see 10μs laser pulse (see Figure 5.40) and

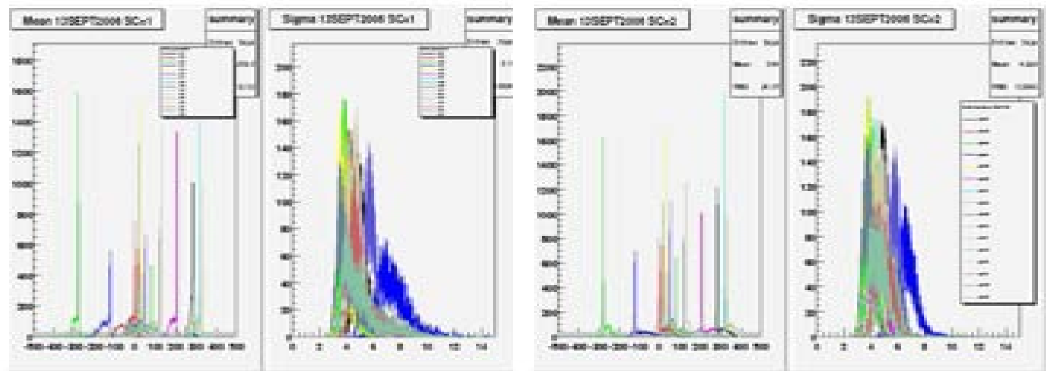


Figure 5.35: Noise results for pipeline data for storage cell 1.

Figure 5.36: Noise results for pipeline data for storage cell 2.

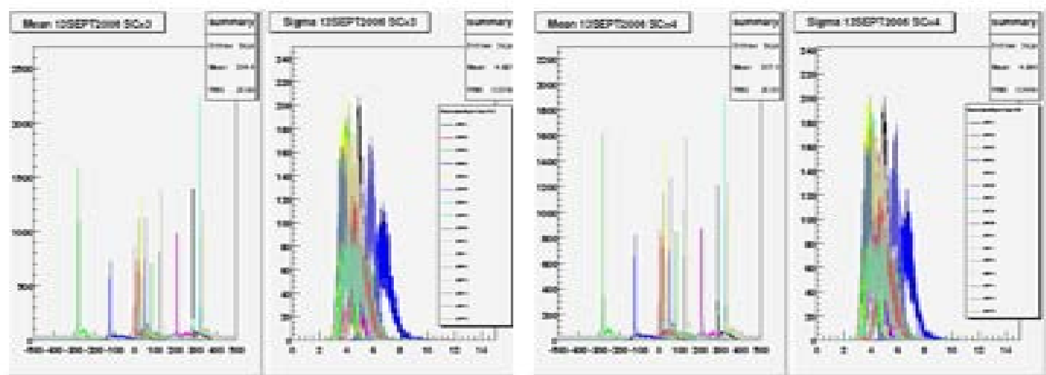


Figure 5.37: Noise results for pipeline data for storage cell 3.

Figure 5.38: Noise results for pipeline data for storage cell 4.

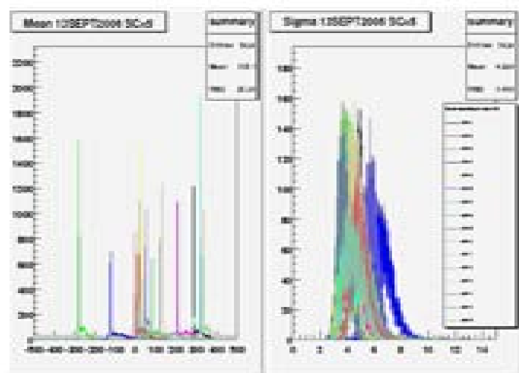


Figure 5.39: Noise results for pipeline data for storage cell 5.

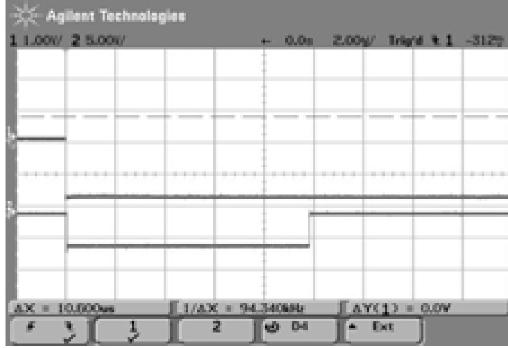


Figure 5.40: Asynchronous trigger and laser for a 10μs laser pulse.

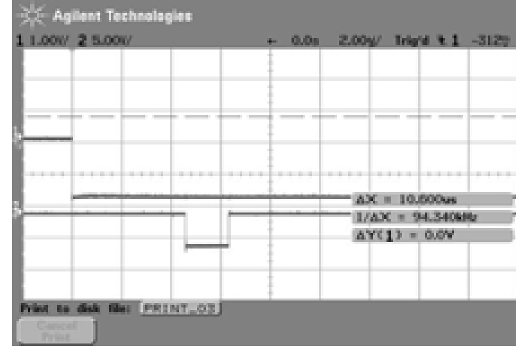


Figure 5.41: Asynchronous trigger and laser for a 2μs laser pulse.

2μs laser pulse (see Figure 5.41). The laser output is on channel 2 and the trigger output on 1. A shift of these two edges is observed for width $\lesssim$10us. The second problem is that is not possible to sweep values of the laser pulse width between about 40ns and about 380ns. For the testing, the first problem was compensated by a smaller/tuned *trigger accept* window to be sure that a trigger matches the acquisition window (between 2 samples) corresponds to a pulse entirely contained in one and only one window. The second problem was avoided by not recording data with a laser pulse width between 40ns and 500ns. Here are the plots generated to see the influence of the laser pulse width on the signal recorded. Four events were recorded each time. The different conditions the laser has been operated for this testing for the event1, event2, event3 and event4 have been: laser operated DC, with 10us pulse, with 6us pulse, with 3us pulse, with 1us pulse, with 500ns pulse and with 40ns pulse. A summary of the data recorded, obtained through the previous measurements is shown in the next 3 Figures 5.42, 5.43 and 5.44. In these plots, the x axis is the laser pulse width given in ns. The error bars are standard deviations (but note the very small number of events treated, 4 events per point only). Finally, DC data are plotted as a function of time for 1,000,000 ns points. A very strong decrease in the signal detected was observed when the laser pulse becomes shorter. Nothing is detected for a pulse width below 1μs. The signal detected in each pixel still stays at around 600 (ADC bit) down to a width of 1us. Below that, it reaches about 300-400, but the influence of noisy pixels (just above significance threshold) might be felt quite strongly at that point. One could think that the pixels providing a high output level still show a pretty strong signal, but that somehow the laser

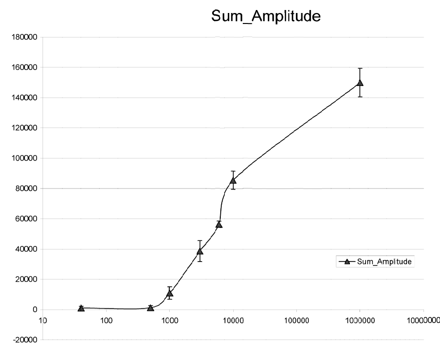


Figure 5.42: Evolution of the total signal recorded as a function of the laser pulse width.

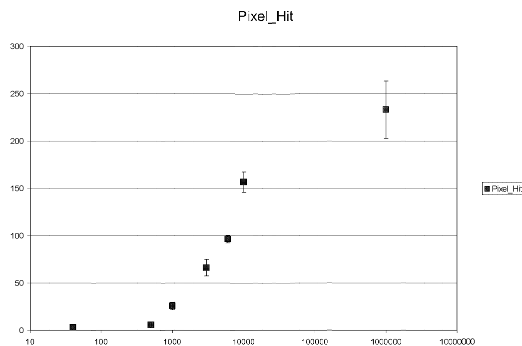


Figure 5.43: Evolution of the number of pixels over the significance cut (10) as a function of the laser pulse width.

spot size decreases. It should be strongly underlined that it is hard to disentangle several possible effects and so we can only conjecture the possible reason.

5.3.11 Laser$_{pulsewidth}$ vs signal recorded for column 420

Another measurement at a lower column number was also performed. This is done to test if changing the region of operation (considering the different gains of the pixels involved) change the results obtained. The laser position was moved from column 700 to column 420. There are some differences in the characteristics of the pixel response as a function of the column number (see Section 5.3.5), and

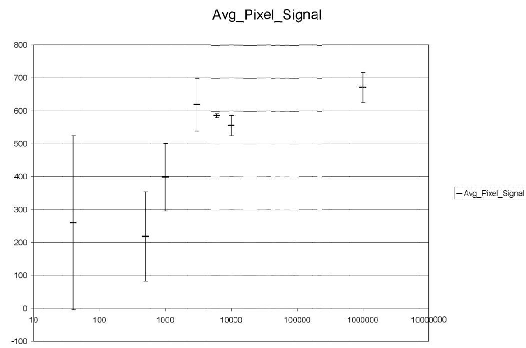


Figure 5.44: Average signal recorded as a function of the laser pulse width.

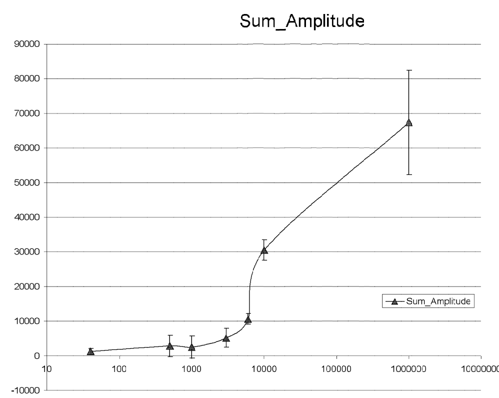


Figure 5.45: Evolution of the total signal recorded as a function of the laser pulse width.

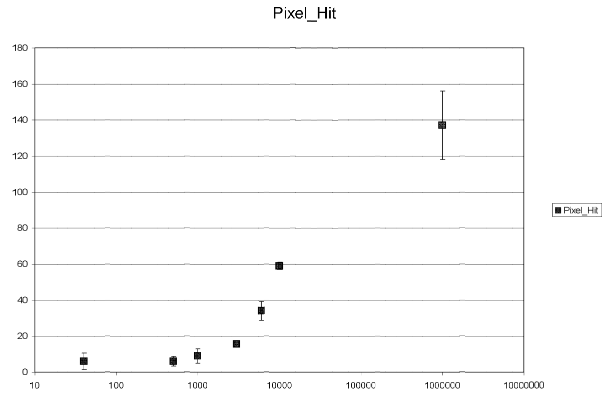


Figure 5.46: Evolution of the number of pixels passing the significance cut (10) as a function of the laser pulse width.

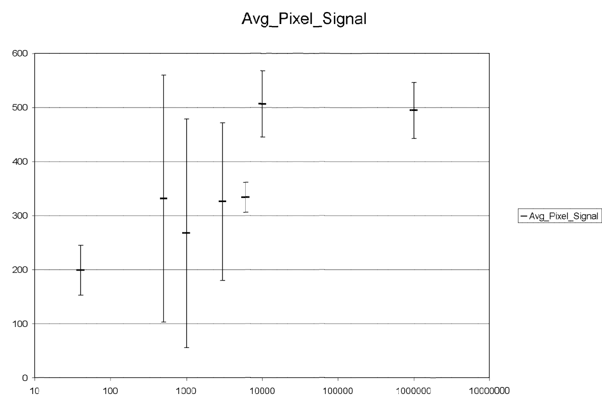


Figure 5.47: Average signal recorded in each firing pixel as a function of the laser pulse width.

because of that the operation of the laser was done in the same conditions as measurements presented before (Section 5.3.10). The output signal was generated to see the influence of the laser pulse width. Four events were recorded each time for each new position. The different conditions the laser has been operated in for this test for event1, event2, event3 and event4 have been: Laser operated DC, with a 10μs pulse, with a 6μs pulse, with a 3μs pulse, with a 1μs pulse, with a 500ns pulse and with a 40ns pulse. A summary of the data recorded, obtained through the previous measurements is shown in Figures 5.45, 5.46 5.47. In these plots, the x axis is the laser pulse width given in ns. The error bars are standard deviations (but note the very small number of events treated, 4 events per point only). Finally, DC data are plotted out to 1,000,000 ns points. Comparing the results showed in Section 5.3.10 with the ones showed here, the influence of moving to a lower column number manifests as a lost of signal. Although this effect was expected, it is stronger than desirable for this kind of detector.

5.3.12 Spill-over and pipeline

Explanation of the data acquisition in the Front-End board Fig. 5.48 shows the signals from the Front-End board. A description of the signals is the following:

- **D0** is the trigger as received from Back-End board.
- **D1** is the reset as received from the Back-End board, with ~75μs period and ~2μs width.
- **D2** is the trigger as passed to the rest of Front-End board logic, the only difference with **D0** is that we wait for an extra Sample to be generated in the Back-End (and received in the Front-End).
- **D3** is S0 switch and controls the recording to the 1st of the buffer pair ("pre-sample").
- **D4** is the S1 switch and controls the recording to the 2nd of the buffer pair ("post-sample"), **D5** is the clean signal.
- **D6, D7, D8** and **D10** are SSx (1-4) switches to control to which buffer pair is written to and to define which integration window is the current one.
- **D11**, **D12**, **D13**, **D14** or **D15** are not relevant.

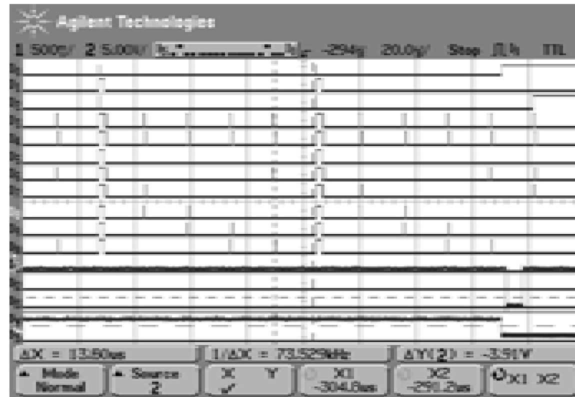


Figure 5.48: Snapshot of current operating conditions for 1st tests of the buffer pipeline and spillover.

- The Analog 2 signal is the actual laser pulse and shows $\sim 6\mu$s wide, Analog 1 is not relevant.

A *sampling window* is defined as the time between two successive ticks of the SS0-4, or the time between a coincidence of SSx and S0 and the same SSx and S1 It has been chosen to be around 15us. Doing that, information is recorded successively on buffer cell accessed by SSx and S0 and the one accessed with the same SSx and S1. The 2 different trigger shown come from the fact that to do CDS an extra sample is waited when a trigger is received and allow to finish at the end of the acquisition window (which means wait for the next coincidence between S1 and the current SSx).

Simple Test and Problems The idea was to start with a simple test. The acquisition cycle is based on received input trigger that stops the acquisition cycle after the next SSx/S1 coincidence. In this particular case, instead of generating the corresponding CPSx (to switch on the readout from the buffer cell corresponding to the generated trigger), the readout is done from a fixed buffer. The test has been done with buffer 2, buffer 3 and buffer 4. The operating conditions are based on a laser pulse well contained inside a single window with a laser spot 6μs wide. On the x axis for all plots, this is the window number in which a trigger was recorded.

Results from the Read-Out from Buffer 2 Figure 5.49 shows the sum of the signals recorded if the pixel shows a significance greater than 10 (fixed rather arbitrarily). Each time, CDS is performed and noise is subtracted. Figure 5.50 shows the total number of pixels above the significance cut of 10. Figure 5.51

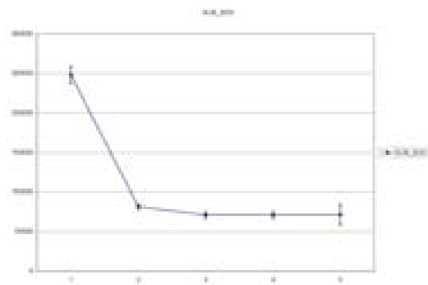


Figure 5.49: Sum of signal for Buffer 2 with significance greater than 10.

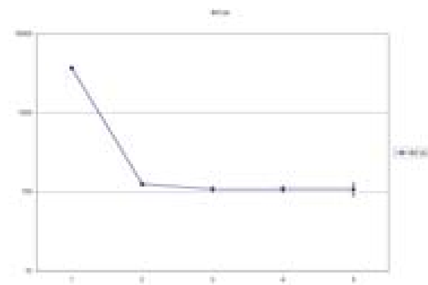


Figure 5.50: Pixel with significance above 10 for Buffer 2.

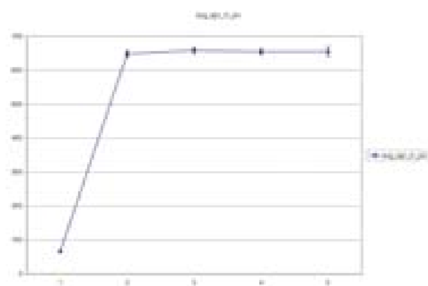


Figure 5.51: Average signal recorded in a pixel above the significance value of 10 for Buffer 2.

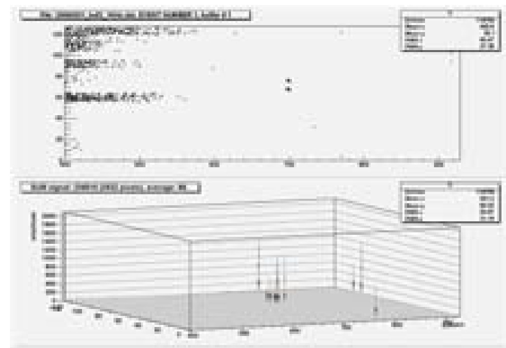


Figure 5.52: Buffer 2 read out although trigger was in window 1.

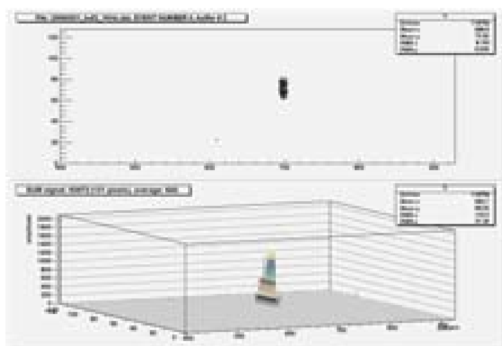


Figure 5.53: Buffer 2 read out although trigger was in window 2.

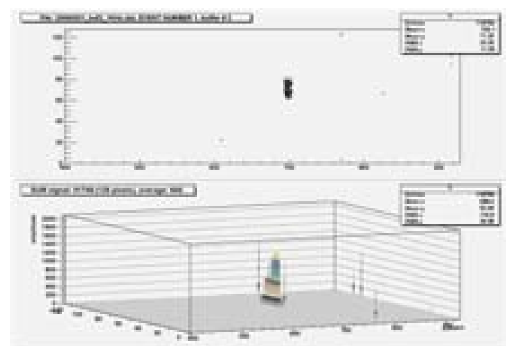


Figure 5.54: Buffer 2 read out although trigger was in window 3.

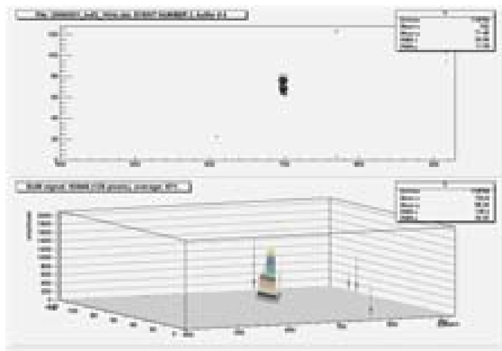


Figure 5.55: Buffer 2 read out although trigger was in window 4.

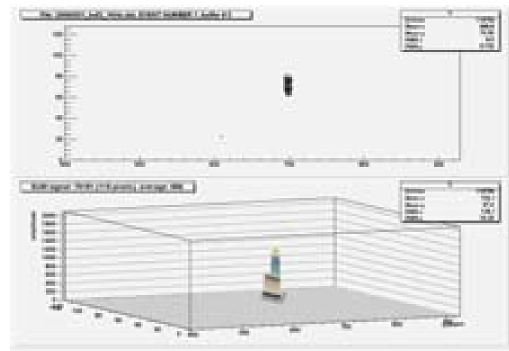


Figure 5.56: Buffer 2 read out although trigger was in window 5.

shows the average signal recorded in a pixel above the significance cut chosen. Finally, here is a representative sample of the data recorded: at Figure 5.52 buffer 2 does the read out although trigger was in window 1, the meaning for Fig. 5.53, Fig. 5.54, Fig. 5.55 and Fig. 5.56 is the same, just varying the window chosen. The results obtained for Buffer2 are showing surprising results. When the trigger happens at the window 1, the system does not record the pre and the post-sample after the trigger. The only difference between them is the noise generated since the reset. It should be very similar as can be seen, in Fig. 5.52, although the profile of the laser position can be presumed with the presence of 2 dots in the middle of the photograph. When the trigger happens in window 2, Fig. 5.53, shows a clear image that corresponds with the expected results. When the trigger happens in window 3, Fig. 5.54, it shows a clear location of the laser. This fact is strange, because the pre-sample should show nothing and the post-sample should show the event at the moment of the trigger. This means that an inverted signal is expected. Instead of an inverted signal, a positive signal is obtained. Fig. 5.55 and Fig. 5.56 show 2 peaks where the recording of the events take place way before the laser signal is applied. These Figures show a clear signal located at the position of the laser, but they should be showing the values recorded when performing the reset.

Results from the Read-Out from Buffer 3 Figure 5.57 shows the sum of the signals recorded if the pixel shows a significance greater than 10 (fixed rather arbitrarily). Each time, CDS is performed and noise is subtracted. Figure 5.58 shows the total number of pixel above the significance cut chosen of 10. Figure 5.59 shows the average signal recorded in a pixel above the significance cut

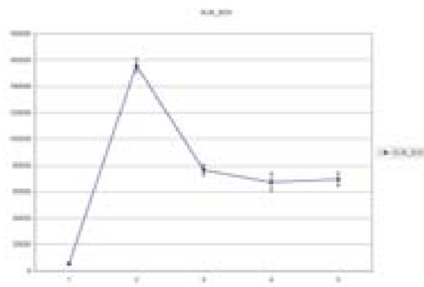


Figure 5.57: Sum of signal for Buffer 3 with significance greater than 10.

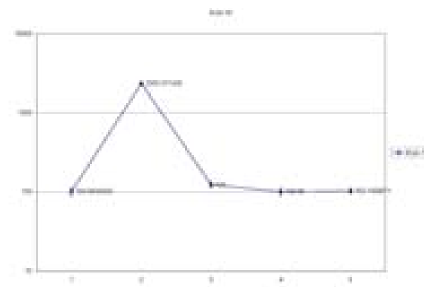


Figure 5.58: Pixel with significance above 10 for Buffer 3.

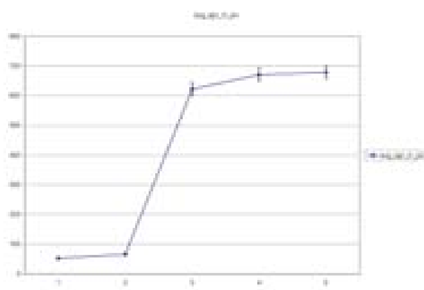


Figure 5.59: Average signal recorded in a pixel above the significance value of 10 for Buffer 3.

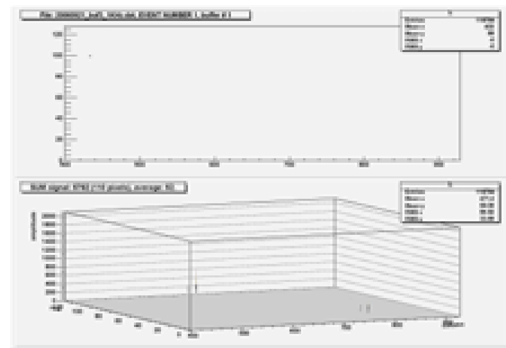


Figure 5.60: Buffer 3 read out although trigger was in window 1.

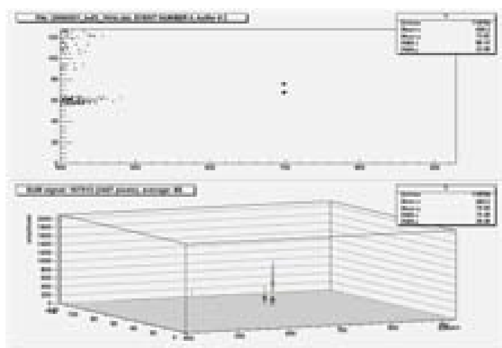


Figure 5.61: Buffer 3 read out although trigger was in window 2.

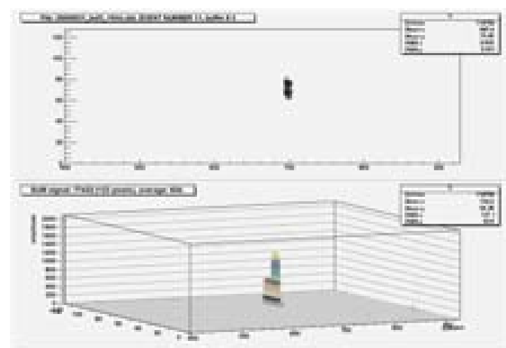


Figure 5.62: Buffer 3 read out although trigger was in window 3.

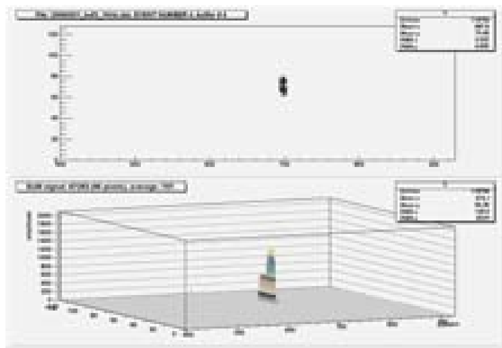


Figure 5.63: Buffer 3 read out although trigger was in window 4.

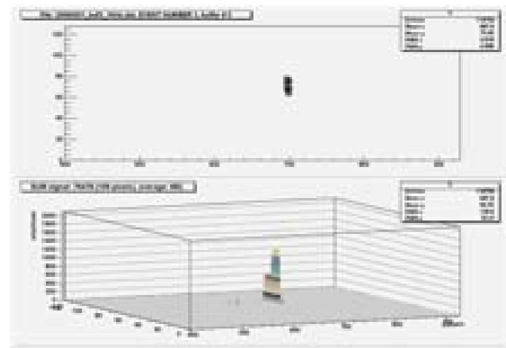


Figure 5.64: Buffer 3 read out although trigger was in window 5.

chosen. Finally, here is a representative sample of the data recorded: at Figure 5.60 buffer 2 does the read out although trigger was in window 1, the meaning for Fig. 5.61, Fig. 5.62, Fig. 5.63 and Fig. 5.64 is the same, just varying the window chosen. The results obtained for Buffer3, are also showing unexpected results. When the trigger happens at the window 1 or 2, the system do not record any signal and should be showing the reset values. The only difference between them is the noise generated because of the different output timing. It should be very similar as can be seen, in Fig. 5.60 for window1 and Fig. 5.61 for window2. A similar fact as for Buffer2 (in window1 then) happens here, for window2. Fig. 5.62 shows the presence of 2 peaks that are located where the laser is pointing. When the trigger happens at window 4, Fig. 5.63, it shows a clear location of the laser. This fact is strange, because the pre-sample should show nothing and the post-sample should show the event at the moment of the trigger. This means that an inverted signal is expected. Instead of an inverted signal, a positive signal is obtained. Fig. 5.64 show an image where the recording of the events take place way before the laser signal is applied. These Figures show a clear signal located at the position of the laser.

Results from the Read-Out from Buffer 4 Figure 5.65 shows the sum of the signals recorded if the pixel shows a significance greater than 10 (fixed rather arbitrarily). Figure 5.66 shows the total number of pixel above the significance cut of 10. Figure 5.67 shows the average signal recorded in a pixel above the significance cut chosen. Finally, here is a representative sample of the data recorded: at Fig. 5.70 buffer 4 does the read out although trigger was in window 3, the meaning for Fig. 5.71 and Fig. 5.72 is the same, just varying the window chosen. The

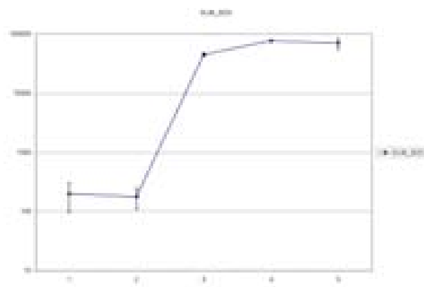


Figure 5.65: Sum of signal for Buffer 4 with significance greater than 10.

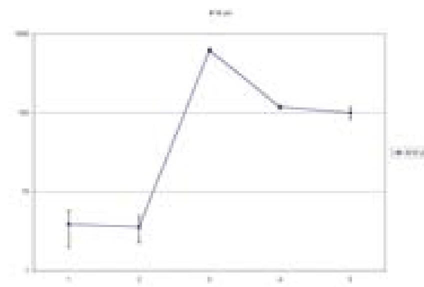


Figure 5.66: Pixel with significance above 10 for Buffer 4.

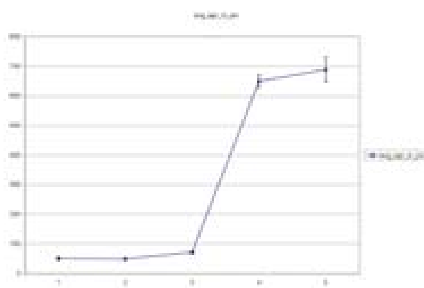


Figure 5.67: Average signal recorded in a pixel above the significance value of 10 for Buffer 4.

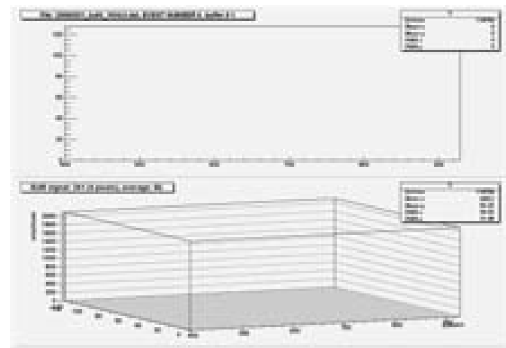


Figure 5.68: Buffer 4 read out although trigger was in window 1.

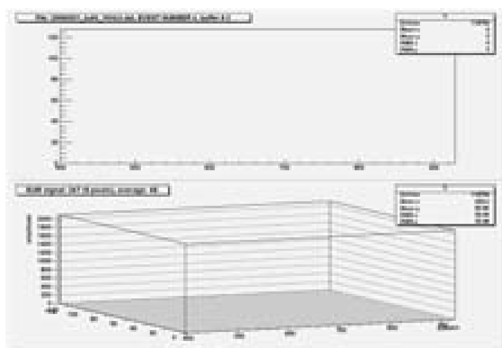


Figure 5.69: Buffer 4 read out although trigger was in window 2.

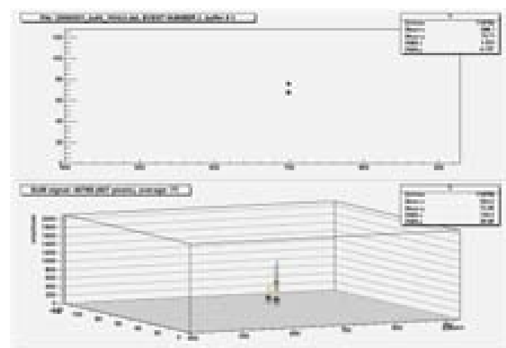


Figure 5.70: Buffer 4 read out although trigger was in window 3.

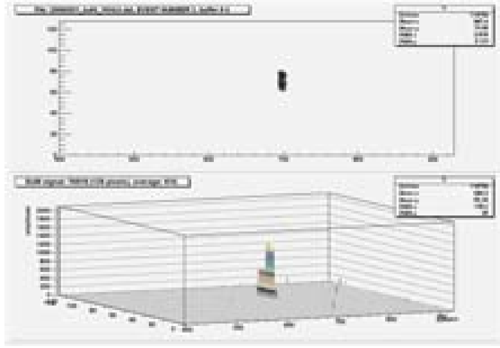


Figure 5.71: Buffer 4 read out although trigger was in window 4.

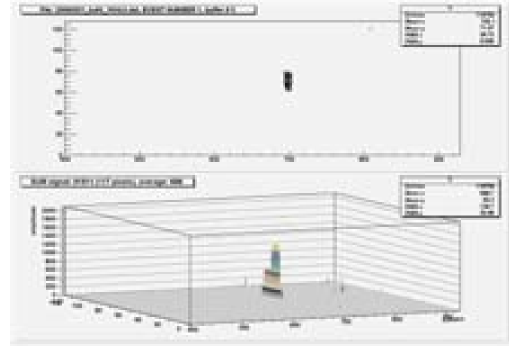


Figure 5.72: Buffer 4 read out although trigger was in window 5.

results obtained for Buffer4 show no results for the case the trigger is at window1 or window2, working as expected. If the trigger is found at window3, there are 2 peaks located close to the location of the real laser. The Fig. 5.71 shows the results obtained when the trigger is at window 4 and the results correspond to the expected. Fig. 5.72 corresponds to the fact that the pre-sample is after the trigger and the post-sample is a few μs later, the clear image obtained does not correspond to the expectations.

When a trigger is recorded in the specific buffer we are reading out, things seem to work properly. It is possible to see a very well defined laser spot, and sometime a few other noisy pixels. On average, the total signal recorded is about 80,000 (given in ADC counts), the number of pixels hit is around 100-150, and the average signal recorded in the pixels is around 600-700.

But taking a look at the readout obtained at buffer 4, when the trigger belongs to window 1 or window 2, no significant signal is recorded (see Fig. 5.73 for a visual help for the timing signals). On average, the total signal recorded is about 200-300 (given in ADC counts), the number of pixels hit is around 5, and the average signal recorded is around 50, that is noise. Taking a look at readout buffer3, the same behavior can be observed, but when the trigger is observed at window 1, there are many more pixels showing this characteristic noise.

Going back to the results obtained at buffer 4, when the trigger belongs to window 3, a small signal is recorded at the place where we would expect the laser

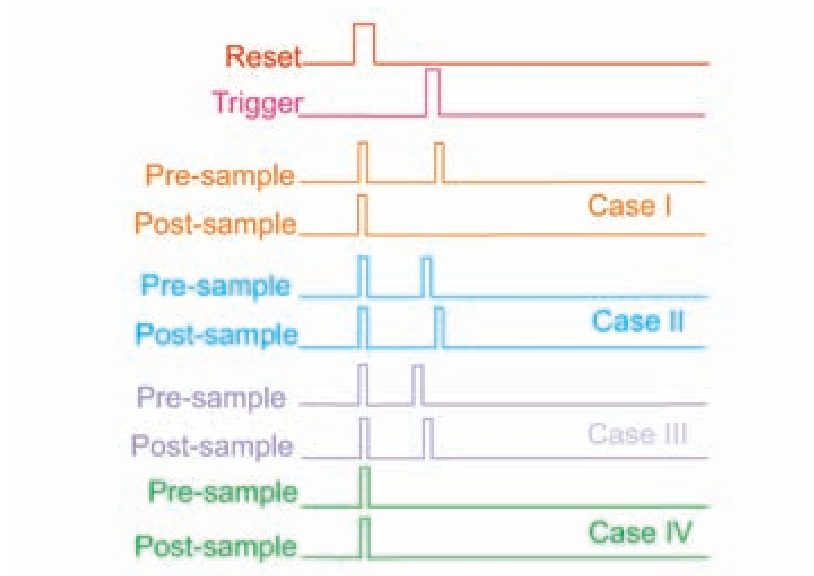


Figure 5.73: Schematic representation of the signal depending on the trigger and the window this is happening. **Case I** corresponds to the case that the trigger happens in the previous window, the system records the pre-sample, but the post-sample keeps the value stored at reset. **Case II** corresponds to the case that the trigger happens at the window that is being read-out, the system will record the pre- and the post-sample properly. **Case III** corresponds to the case that the system records the post-sample at the moment of the trigger, and the pre-sample has been recorded before the trigger (signal generation) took place, this means that the system should be storing a similar value to the reset. **Case IV** corresponds to the case the trigger happens more than 1 window event before, in this case no pre- or post-sample will be recorded.

spot to be. At first sight, that seems alright, and we are just witnessing spill-over, or the fact that it takes time for charges to diffuse, but this is not true. When we receive a trigger, we freeze the data acquisition with the next coincidence of S1 and SSx -in our case SS3. For the buffer of interest, we will do the *pre-sample* (with the next coincidence of S0 and SS4) but never the *post-sample* (no coincidence of S1 and SS4 afterwards). Information recorded on the second buffer of the buffer pair belonging to window 4 should basically stay at reset level (the last time we recorded something on this specific buffer was with the reset). So if we are recording anything, since the *pre-sample* of window 4 was performed but the *post-sample* was not done, this should be not a *laser bump*, but a *laser hole*. Taking a close look for the other buffers (2 and 3) similar effects are found.

The obvious hypothesis there are the following ones: when the trigger is received the acquisition is not frozen (has been checked with the oscilloscope) or the fact that the data is converted at its absolute value (not probable because the both the ADC decoding and linearity of the ADC have been positively studied).

Taking also a closer look to buffer 2, more surprising effects are observed. When we read out this buffer and the trigger happens in window 3, window 4 or window 5, we see a very clear laser spot, and the sum of the signals recorded, the number of pixel hits or the average signal in a pixel all are about the same as when the triggers happen during window 2. So now, yes, the pre-sample and post-sample were done correctly for window 2, but the thing is that there was nothing to record at that time: the laser pulse took place later in time.

After these two examples of the effects found, a few more hypothesis were raised. The storage of data is being done in multiple storage cells, but this hypothesis was not seen in the data sent to the prototype. The fact of reading a different buffer as is thought to be done. The last and the final reason found is leakage of charge and coupling between storage cells, due to layout problems. Although this seems to be the best explanation, the same coupling could not be found in the opposite direction, e.g. the pulse is not seen in buffer 4 when it takes place at 2.

The other aspect that was observed with these results were the patterns of noise observed at the left side of the read-out. There is a banding effect that

affects specially in the case of reading out the posterior Buffer corresponding to the specific window where the trigger happens, in this case the storage-cell will record the pre-sample of the trigger, but the post-sample should be kept at reset level. The cases are: read-out of Buffer2 when the trigger happens in window1 (Fig. 5.52) or Buffer3 when the trigger happens in window2 (Fig. 5.61. In any case, it should be mentioned that this bands are present, but show much lower value than the signal that was described in previous paragraphs (it can be 100 times less).

5.4 Conclusions

A surface scan of the sensor was performed. In different measurements the data was read out from all five storage buffers, one pair per event cyclically, to confirm the functionality of the internal storage pipeline. With the scans we discovered that 16 groups of rows connected to different readout multiplexers behave differently in terms of noise, and a systematic shift in transfer curve response column-wise was also found, so that a gain correction has to be performed.

However electronics tests, however, showed that CAP3 design suffers from additional flaws. These are limited dynamic range across the entire chip for a common set of bias parameters, poor choice of reset transistor control for the basic three transistor pixel cell and excessively long settling times on the highly capacitive bus lines running the entire length (2 cm) of the sensor [101].

Chapter 6

Continuous Acquisition Pixel 4 *(CAP4)*

Based upon the lessons learned from the CAP1, CAP2 and CAP3 prototypes, the next member of the CAP family was developed. In parallel, an overhaul of the test hardware, software and firmware environment was undertaken. This environment was changed because of the limitation of data processing speed and software. In this chapter the new evaluation environment is presented in detail, as well, as the CAP4 chip description and results. Section 6.1 describes the laser set-up environment used and developed in the lab, which includes not just the laser diode, but the alignment system and the dark box that was designed and fabricated. Section 6.2 introduces the new hardware environment developed. This section include a complete description of the new PCB environment, the USB connection and the software development used in this CAP4 version. Section 6.3 introduces the general details of the CAP4 technology, where the 2 different architectures are briefly explained. A detailed description and results obtained are described in Section 6.4, Section 6.5 and Section 6.6.

6.1 Laser Set-Up

The laser set-up used for the testing of CAP3 and CAP4 has been developed to allow the testing of a particle detector in light-tight conditions. CAP3 was used to prepare the set-up for use with CAP4. The experimental requirements are a small spot size, small enough to fit inside any of pixels used in every design, with the best alignment possible (highest output power). In the case of CAP4, due to the metal layers on the top of the sensors, the pixels must be illuminated from the

back side, and the light must travel through the 450 μm of Si bulk. Because of this back illumination, an IR laser is used.

In order to achieve a sufficiently small and round beam profile with homogeneous intensity from the laser diode output, it is coupled to a single-mode fiber patch cable (2m length with λ=980nm and FC/PC connectors with 5.8 μm diameter of the optical core) via a single mode fiber coupler device equipped with corresponding aspheric lenses for collimation and focusing of the divergent diode light into the fiber. Theoretically, 45% of the diode power can be transmitted into the optical core of the fiber. For testing the fiber output, an IR card and an IR camera with a microscope has been used to measure the quality and size of the beam spot. Also included in the set-up, the optical table has an automated XY stage, to allow the movement for the laser fiber cable. Furthermore, to allow the possibility of working at different wavelengths (like visual light), additional diodes and the corresponding fiber are present, including a visible laser that is used during the alignment process.

The components of the IR set up consist of the following. A **laser diode (IR)** with a typical wavelength of 980nm. In Continuous Wave (CW), the laser diode emits a typical optical output power of 100mW, at a typical threshold current of 50mA and an operating voltage of 2.0V. It also includes a **single-mode launch fiber (with lenses)** (see Fig. 6.1 and Fig. 6.2), which is a system specially designed to couple the output from a laser diode into a fiber optic cable terminated with FC connectors. To compensate for variations in the mechanical emission point of the laser, a manual XY positioner is used to mount the laser package. The collimating lens for the laser is mounted in a cage plate that allows the laser output to be collimated. The lens is used to focus the collimated beam onto the fiber optic core mounted on the XY translation stage. The final component is a Z translator that accepts the FC or SMA terminated fiber optic cable. The **automated stage** used is composed of a motorized XY axis travel stage, which includes two motors and two single-channel USB DC servo controller/drivers. To allow automated PC control, a full software control suite (APT^{TM} System Software) is used. **A powermeter and a photodetector** are used to measure the light conditions inside of the box. A powermeter is used to check the strength of the laser at the end of the fiber cable. A light tight, **black box and optical table** house the entire set up. The optical table provides stability to the system, and the Black Box keeps it

light-tight. A **laser pulse driver and generator circuit** is used to apply a pulse laser signal, rather than a CW illumination. The pulse circuit is current limiting (50 mA) which will prevent the laser diode from being over driven. For the case of the IR laser diode the threshold current is 35mA, ensuring a safe operation region.

Figure 6.1: Side view photograph of the laser set-up used and described in this section.

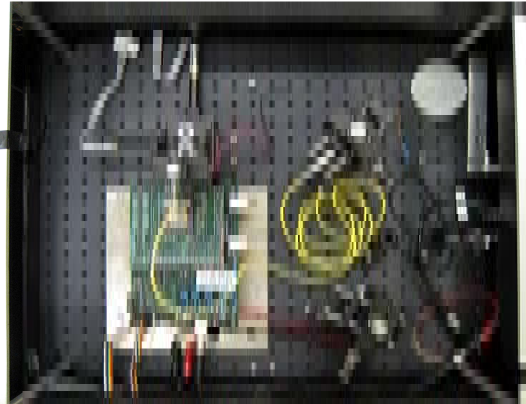


Figure 6.2: Top view photograph of the laser set-up used and described in this section.

The **laser set-up** can be used in CW mode or in Pulsed mode. CW mode is quite useful to start testing basic functionality of the detector, such as sensitivity to signal and noise. Pulsed mode is used to study the laser signal spill-over and dynamic noise/effects introduced by a pulsed source. The driver output negative pulses and the current provided is limited to 50mA or less. The driver also produces a TTL *trigger out* signal, either clocked with an internal clock or by a TTL level *trigger in*. The TTL level output *trigger out* from the laser driver then goes into a level converter, which makes the correct level signal for the COBI[1] board (TTL to 0-2.5 level, which matches the FPGA). The delay from the trigger output to optical output should be less than 10 ns, and is typically 8ns. The maximum external trigger frequency must be less than $\frac{1}{5t_{pw}}$. To maintain the pulse width, a potentiometer is used. Higher frequency operation distort and shorten the pulse width. The potentiometer is only minimally sensitive to temperature, about 1-2% for every 10K.

[1]For a description of the COBI board go to Section 6.2

6.2 Description of the COBI Board

Previous CAP prototypes used a complicated read-out and processing architecture. The chip and the FPGA (at the FE Board) transmitted the digitized values generated by the ADC over two standard CAT5 Ethernet cables to the compact PCI Back-End Board usign a high-speed, custom serial protocol. One goal of the CAP4 prototype test station was to develop a more simple and versatile evaluation infrastructure. The new solution will allow for a more portable solution (where just one computer would be used) as well as a faster and easier to troubleshoot solution. The previous solution was very complicated in terms of signal control and troubleshooting. The goal was to develop a compact, single board read-out solution using USB communication to transmit the data to the computer that would be in charge of the reception, processing and graphical representation.

Another aspect that was changed in this new system was the replacement of the two-card scheme used in previous versions. In one previous version, four 60-pin connectors were used to accommodate the detector board. The connector provides mechanical stability and allows for easy exchange of detector chips to have a more complete test without the problem of having to de-solder the chip every time a new chip has to be studied. The option chosen for CAP4 was a two stacked board scheme. In this case three 120-pin Q Strip® Samtec connectors were used to be able to increase the transmission data rate to 4 GHz. This change of connector increased the number of I/O signals by 2 without degrading the signal quality. The daughter board that is used in CAP4 has been called PETRA.

The software was also changed to *so-called* standard programs used in the HEP environment. In previous versions Physics Analysis Workstation (PAW) was used for the data analysis and representation. PAW was developed by the CERN laboratory in Geneva, to be used in particle physics experiments and their data analysis. PAW is described as a Fortran based system. A major limitation with PAW is that is limited to 50000 columns (memory allocation static) and presents a limited number of data types. That means that an event, which is a mixture of data types, is moved and manipulated *by hand* and the handling of data means that the code can corrupt the data. The environment chosen to be used in the CAP4 read-out is an Object Oriented(OO)/C++ based system. Root is a library of rou-

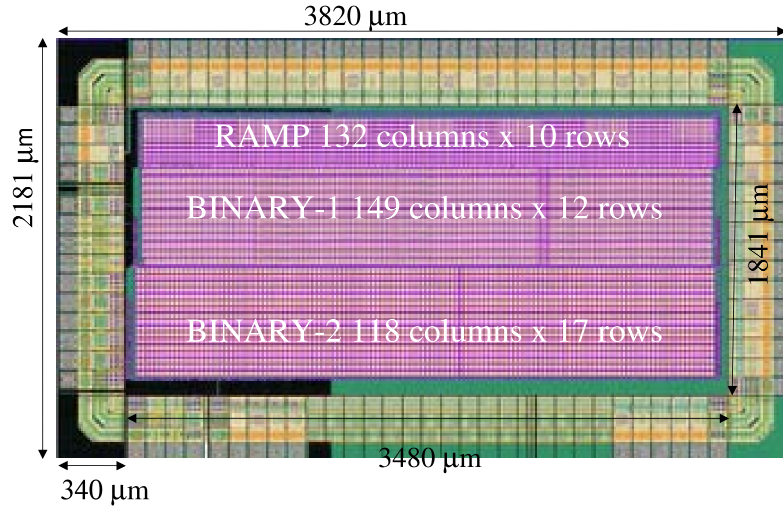


Figure 6.3: Schematic view of CAP4 Layout submitted for fabrication using the AMS 0.35μm process, containing an improved analog design MAPS (denoted as RAMP) and two new digital designs for continuous readout (denoted as BINARY-1 and BINARY-2.

tines that takes the successful features of PAW and adds the data handling and the OO advantages of C++. The Root framework allows the use of one language for reconstruction, analysis and display. The program developed using Root can take care of the reception of the USB data, processing and visualization.

6.3 General Characteristics of CAP4

The CAP4 prototype was made in the Austria MicroSystems (AMS) 0.35μm Opto process, with a 14 μm epitaxial layer. CAP4 chip contains three separate sensor prototypes, following two conceptually different designs, one *analog* and two different *binary* schemes (see Fig 6.3). The first design aims to develop further the analog CAP architecture, which is based on the already implemented CAP designs (CAP1, CAP2 and CAP3 versions). The binary design has been developed to test basic functionality of a new digital readout concept, which is, by contrast to the analog readout, not trigger rate independent.

The external dimensions correspond to 3820×2181$\mu m$with an active area used of 3480×1841 μm. The three different detector versions included in CAP4

Figure 6.4: Photograph of the CAP4 in theAMS 0.35μm process.

(see Fig 6.4) also occupy different areas. The **Wilkinson ADC** uses an overall size of is 3035 $\times 300\mu m$, and the pixel size is $21.9\times 25.3\mu m$ with 132 columns and and 10 rows. The **Negative-channel Metal-Oxide Semiconductor (NMOS) Binary** array has an overall size of 3035 $\times 565\mu m$, and each pixel size is 20.5×42.7 μm arranged in 149 columns and 12 rows. The **CMOS Binary** array has an overall size of $3035\times 570\mu m$, with each pixel 25.5×30.9 μm, arrayed as 118 columns by 17 rows.

6.3.1 CMOS-Opto 0.35μm AustriaMicroSystems Process

The process used to fabricate this chip has a minimum feature size of 0.35μm with an epitaxial layer. The CMOS-Opto process has a 4 metal layers and 3 poly layers. The nominal V_{DD} supply voltage is 3.3V and this process uses a wafer with a 14μm epitaxial layer, as can be seen in Fig. 6.5. The main features of the Opto process are a $I_{Darkcurrent}$ <200 nA/mm^2 for the standard base material and a $I_{Darkcurrent}$ <10 nA/mm^2 for the epi base material. The Cut-off frequency is >20 MHz, a responsitivity at 550 nm: 290 mA/W, a responsitivity at 850 nm: 330 mA/W and a cut-off frequency of photodiode: 20 MHz. Fig. 6.6 shows the responsitivity for a wavelength from 400nm to 1000nm, where a comparison between a wafer with a epitaxial layer and another with no epitaxial layer.

Figure 6.5: Wafer Cross Section of the CMOS-Opto 0.35μm process of AustriaMicroSystems.

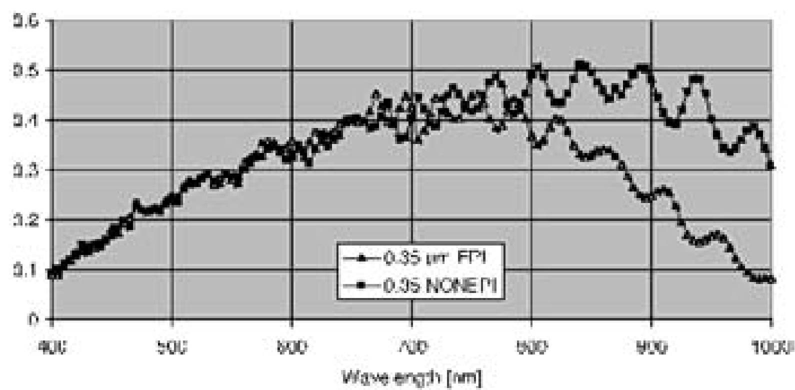


Figure 6.6: Responsitivity of the CMOS-Opto 0.35μm process of AustriaMicroSystems.

6.3.2 Calculation of charge deposition for CAP4 using the IR Laser in the Wilkinson Configuration

The Set up used for the testing includes an IR Laser ($\lambda_{Wavelength}$=980nm) that has a measured incident power of 15 μW, with an approximated beam size spot diameter of 50μm (Area of 2.356 10^{-9} m^2 if considering a magnification of 1.2 considering the microscope used for measuring). The energy for the 980nm wavelength light is:

$$E_\gamma = \frac{hc}{\lambda} = \frac{4.135 \cdot 10^{-15} \times 2.998 \cdot 10^{17} eVnm}{980nm} = 1.265eV/\gamma = 2.027 \cdot 10^{-19} J/\gamma \tag{6.3.1}$$

This gives the number of incident photons at 1.234 10^{12}. The Pixel Unit Cell (PUC) characteristics are a height of 25.3μm and a width of 21.9μm, giving an area of 5.5407 10^{-10}m^2, therefore 3.54 pixels. The number of e-hole pairs generated by the incident photons depends on the Silicon characteristics. The general characteristics of the Silicon chip are a bulk thickness of 436μm with an epi thickness of 14μm, giving a total thickness of 450μm. There are many effects that need to be considered to calculate how many electrons will be generated by the diode laser. Backside illumination is used in this case.

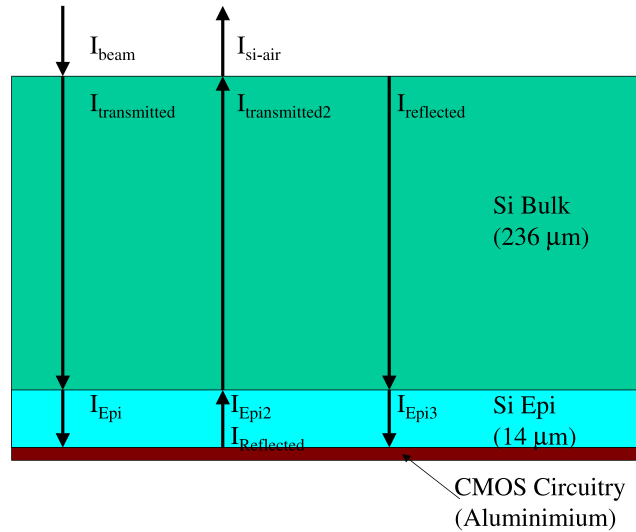


Figure 6.7: Detailed schematic for the calculation of the charge deposition for the Wilkinson array case.

The first effect that is considered is described according to the **Fresnel Equations**[2]. The Cauchy formula is used for the air index of refraction, obtaining a n=1.000274 [102]. The silicon index of refraction is n=3.72540 ([103],[104]). Calculations using this Fresnel equation give an R=0.33254 and a T=0.66746.

The second effect to consider is the **Photoelectric Effect** [3]. The value of the absorption coefficient at 300K is 73.04μm [90]. Within the Si bulk, the attenuation of photon due to the photoelectric effect is:

$$I_{Bulk} = I_{\text{Transmitted}} e^{-\frac{t_{BulkSi}}{LengthAbsorption}} = 0.66746 I_o e^{-\frac{436.00\mu m}{73.04\mu m}} = 0.001741 I_o \quad (6.3.5)$$

Once the number of photons arriving at the epitaxial layer is known, the deposition at this layer can be calculated:

$$I_{Epi} = I_{Bulk} e^{-\frac{t_{Epi}}{LengthAbsorption}} = 0.001741 I_o e^{-\frac{14.00\mu m}{73.04\mu m}} = 0.00141 I_o \quad (6.3.6)$$

The number of photons deposited corresponds to:

$$I_{1deposited} = I_{Bulk} - I_{Epi} = (0.02637 - 0.02177) I_o = 2.96 \cdot 10^{-4} I_o \quad (6.3.7)$$

The beam will strike the aluminium of the CMOS circuitry and will be reflected at 98% [105] of its original value. If a non-specular correction factor for the aluminium layer of 0.8 is considered, the reflected intensity is:

$$I_{reflected} = I_{Epi} \cdot \text{Reflection}_{coef} \cdot Factor_{non-spec} = 0.00141 I_o (0.95)(0.80) = 1.072 \cdot 10^{-3} I_o \quad (6.3.8)$$

[2]Fresnel equations describe the behavior of light when moving between media of different refractive indexes. The fraction of the intensity of incident light that is reflected is given by the reflection coefficient **R**, and the fraction refracted by the transmission coefficient **T**. Fresnell equations, can be used to calculate R and T, when considering both mediums as non-magnetic. These calculations can be simplified when considering that light is at near-normal incidence to the surface, reduced to the expressions:

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2 \quad (6.3.2)$$

$$T = \frac{4 n_1 n_2}{(n_1 + n_2)^2} \quad (6.3.3)$$

[3]Photons are absorbed in a solid through a process called the photoelectric effect, where a photon interacts with an electron by giving all its energy to the electron. The mathematical description for the visible and x-ray spectrum corresponds to the exponential decay law. Using the absorption coefficient α, the intensity of light as a function of depth t, I(t), and I_0 as the incident light intensity, then I(t) is described as:

$$I(t) = I_o e^{\alpha t} \quad (6.3.4)$$

If consider the photoelectric effect at the epitaxial layer deposition, a second amount of photon intensity is deposited as:

$$I_{2deposited} = I_{reflected} - I_{epi-2} = 2.739 \cdot 10^{-6} I_o - 2.261 \cdot 10^{-6} I_o = 0.478 \cdot 10^{-6} I_o \quad (6.3.9)$$

If considering a third contribution to the photon deposition it will come from the reflection of the reflected photons previously calculated. Considering a geometric spread of 0.25, the calculations show that the third deposition is shown to be negligible, because it gives less than 0.01% of the total number of deposited photons. A good approximation for the number of deposited photons in the epitaxial layer is $2.965 \cdot 10^{-4} I_o$.

To finish the calculation and assuming that every photon will generate one electron, the total signal per pixel is expected to be:

$$Signal_{pixel} = \frac{(totalgamma/s)(\gamma_{deposited})}{hit_{pixels}} = 5.52 \cdot 10^9 \frac{e^-}{pixels} \quad (6.3.10)$$

This means that when applying a 10μs width laser signal pulse, 55,200e^- will be generated per pixel.

6.3.3 Calculation of pixel capacitance and noise values for CAP4

One of the key calculations to perform is the capacitance seen by every pixel electrode. The calculation, using values provided for the AMS 0.35μm epitaxial process are the following.

When using an epitaxial process the main contributor is the diode formed by the implantation at the electrode. The diode contribution considering an area of 3μm by 3μm is: $C_{AreaJunction}$[4]=0.72fF, $C_{Metal1-WellContribution}$[5]=0.27fF, C_{Area}[6]=0.24fF and $C_{Perimeter}$[7]=0.528fF. The total capacitance is then 1.518fF. After doing the layout and extracting the parasitics, the value associated to the electrode node with respect to ground is higher, $C_{electrode}$=2.11fF.

The variation of signal at the electrode node is defined as:

$$\Delta V = \frac{\Delta Q}{C_{electrode}} \quad (6.3.11)$$

[4] CJNW=0.08fF/μm^2
[5] MET1-active=0.030fF/μm^2
[6] CMDIFF=0.030fF/μm^2
[7] CMDIFF=0.044fF/μm^2

Considering a 10μs, 980nm laser signal incident on a Wilkinson cell, it would create 118e^{-}. The equivalent change in voltage value should be 8.8mV. Because of the small capacitance involved in this pixel detector, there is an associated noise added by the electrode and also by the storage cell (at the Wilkinson) of:

$$v_{noiseElectrode} = \sqrt{\frac{kT}{C_{electrode}}} = \sqrt{\frac{1.3810^{-23}298.15}{2.1110^{-15}}} = 1.396mV \qquad (6.3.12)$$

For the storage cell, the gate capacitance value is determined by the t$_{ox}$=7.575 $10^{-3}\mu$m and an area of 1.5 μm by 0.5 μm, resulting in a capacitance of 3.478fF.

$$v_{noiseStorageCell} = \sqrt{\frac{kT}{C_{StorageCell}}} = \sqrt{\frac{1.3810^{-23}298.15}{3.47810^{-15}}} = 1.088mV \qquad (6.3.13)$$

The variation of the signal at the electrode node due to the leakage current is:

$$\Delta V = \frac{\Delta t \times I_{leakage}}{C_{electrode}} = \frac{10^{-6} \times 9 \times 2.8\ 10^{-15}}{2.11 \times 10^{-15}} = 1.194\ 10^{-02}mV \qquad (6.3.14)$$

6.3.4 Analysis of CAP4

A simple program has been developed to evaluate the position resolution sensitivity of the Belle CAP (sensors) as a function of the n-well size and geometry. The processing steps are the following: generation of the impact point, calculation of Landau fluctuations of signal, diffusion of the charges, co-addition of noise, calculation of center of gravity (at trigger threshold crossing) and accumulation of statistics.

In the generation of simulations with this program, a few parameters have been choosen: V$_{emax}$=2.3 10^{5} m/s (maximum velocity at charge transport) and T$_{step}$=400 $10^{-15}m$ (modified distance m at collision). The first step is to define the electrode and n-well positions. The impact position calculation is then followed by the Landau calculation (see Equation 3.3.4) using Moyal approximation (see Equation 3.3.5), which is used to calculate the approximate energy loss and the equivalent number of e-hole pairs created. After this initial settings, the calculations can start and each electron is analyzed to see if it has been reflected from bottom (bulk Silicon) or top (circuitry layer), has been lost at bottom or has recombined at the surface. If the electron has not reflected or recombined, the following may be occuring: the electron is still diffusing or has already been captures, either by an electrode or by a parasitic n-well.

The simulations have been done considering different levels of noise, from 1 to 30e$^-$. In all cases 100 events have been the maximum event number calculated. These simulations also use the different geometrical parameters used for each of the architectures. For the case of the Wilkinson architecture a pixel with an electrode of 3$\times$3μm was included in a matrix of 8$\times$8 pixels of 22$\times$25μ.

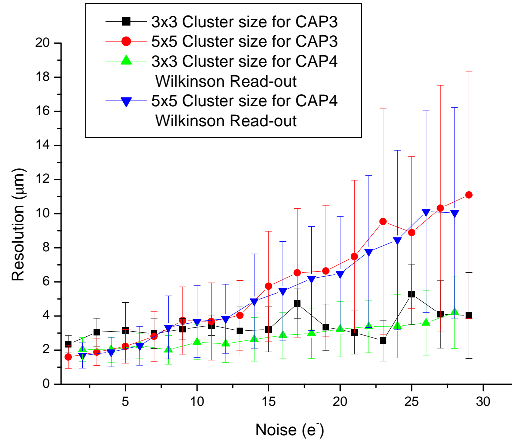


Figure 6.8: Resolution simulation for different cluster sizes for the case of the analog output read-out.

The simulations performed for the Wilkinson architecture show that the results obtained present similar resolution results to the CAP3 simulations. The resolution is not affected as the absence of symmetry is increased in the pixel layout. The simulation shows a resolution of 10μm for a noise of 30e$^-$ for a cluster size of 5x5 for the Wilkinson architecture, and a resolution of 4μm for a 3$\times$3 CAP3 cluster size. This value decrease for lower noise values, down to 2μm for the case of 1e$^-$ noise.

6.4 Wilkinson Solution

The analog part of CAP4 consists of 132 columns $\times$ 10 rows of pixels, and the size of each PUC is 22 μm by 25 μm (see Fig 6.21 for the layout image). The pixels use the previously mentioned 3T cells with a redesigned reset transistor control. A new bus architecture based on a **tree-readout** has been used inside each row to reduce the capacitive loads of the long output bus lines that run across the

columns, and, thus, speed up the data output capability. Streaming of the data from the chip is facilitated by encoding the analog signal level into time intervals using **the basic Wilkinson type ADC encoding**, where the high-speed clocking is performed outside the CAP4. This allows the use of stronger, digital output buffers and improves the output drive strength. The analog Wilkinson was designed to obtain better parameter uniformity throughout the pixel array and higher data output speeds compared to the previous CAP prototypes.

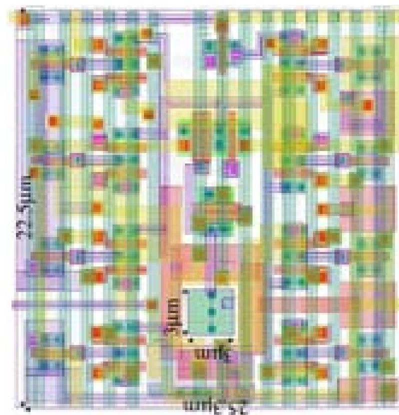


Figure 6.9: Detailed layout for the Wilkinson Pixel Cell, including dimensions.

6.4.1 Architecture for the Wilkinson Solution

Pixel Unit Cell Description Every PUC presents a 3T structure to measure the input signal and 10 storage cells that are controlled by 2 different types of signals (S_i, for store and C_i, for transferring to the output, where i is 0-9). All the storage cells are connected to the same puc output. See Fig. 6.23 for more details.

Row Output Organization Description In order to minimize the capacitance at the output node, the pixels are grouped in 10s with a last group consisting of only 2 pixels (for a total of 132). To make an initial selection of the cells, an additional signal is used: SW_L_i, which decreases the number of outputs per row to 14. There is a third level to select the output using 4 additional signals SW_i, giving a

total of 10 outputs, each one corresponding to each row. After that, a 4×1 analog multiplexer is used to reduce the 10 outputs to 3. In this case, the signals MUX0 and MUX1 are used.

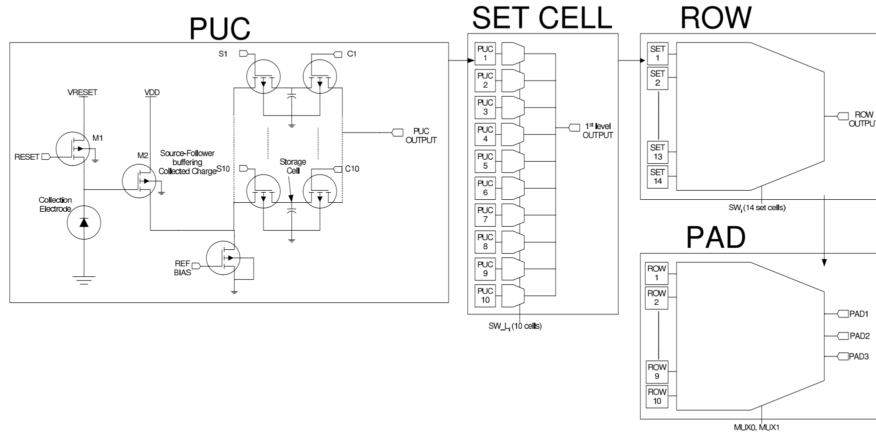


Figure 6.10: Detailed schematic of the Wilkinson readout circuitry from the Pixel Unit Cell to the PAD level.

Additional analog values which are required to be set include: Sensor (Tunable, used to set the value at electrode at testing PUC), V_{reset} (Tunable, initially set to 3.3V, determines the drain voltage of the reset transistor at the 3T structure), $V_{source3T}$ (0.55V, determines the voltage for the current source used after the source follower structure), and $V_{sourceComparator}$ (2.75V, determines the voltage to set the current source used at the comparator). The following additional digital signals are needed: Ramp Strobe of 4MHz period (used to generate the ramp signal that is used at the comparator) and Reset (initially set to 3.3V, but tunable to control the drive strength of the reset architecture by decreasing its value).

6.4.2 Wilkinson Test Results

The results obtained with this part were limited due to oversights and flaws in the design. However , some new ideas have come from these lessons and have led to the design of a new CAP prototype, which will continue evaluating the Wilkinson

architecture.

The storage cells did omitted an high impedance transistor in the readout path of the electrode voltage value. This limits the possibility of using this architecture used in this configuration. The presence of multiple switches introduced a drop of voltage through the output path, resulting in the impossibility of detecting small voltage variations(due to particle/laser), on the other hand, the capacitance per row has been decrease and now it is possible to work at a higher speed (between 1MHz and 4MHz) than with previous prototypes (CAP1, CAP2 and CAP3).

6.4.3 Constant Reset with no Laser Applied

To start testing the Wilkinson structure, the value of the gate reset voltage has been changed to see how the sensor behaves and to determine what is the valid operation region. The following Figures correspond to 100 samples results, for different reset voltages. Fig. 6.11 show the results for a reset voltage of 3.3V, Fig. 6.12 for a reset voltage of 2.3V and Fig. 6.13 for a reset voltage of 1.3V.

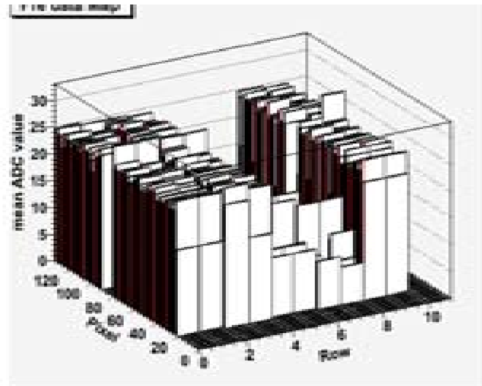


Figure 6.11: 3.3V Reset Results.

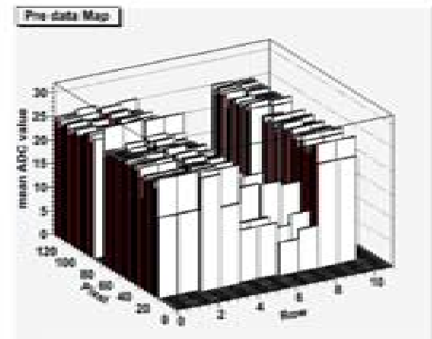


Figure 6.12: 2.3V Reset Results.

The next example is the number of ADC counts found for a specific pixel (position row=2 and column=60) and for a given applied reset voltage of 2.6V. The results obtained for this specific pixel are representative of all pixels at a voltage higher than 1.3V. Fig. 6.14 shows the ADC counts distribution that is measured. To do these measurements the digital signal obtained from the output pads is quantized using a 200MHz clock, corresponding to 1.44ns least count precision. Fig. 6.15 is

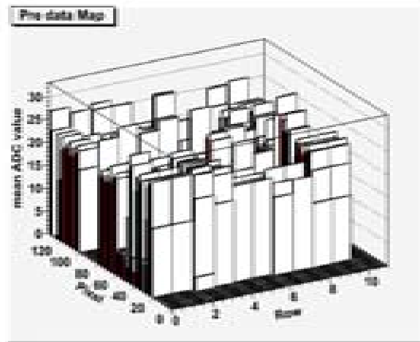


Figure 6.13: 1.3V Reset Results.

a representation of the transfer function obtained, where the electrode voltage is a function of the ADC counts measured in the FPGA.

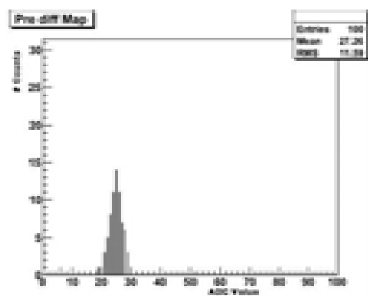


Figure 6.14: Voltage distribution in ADC counts at 2.6V at Reset.

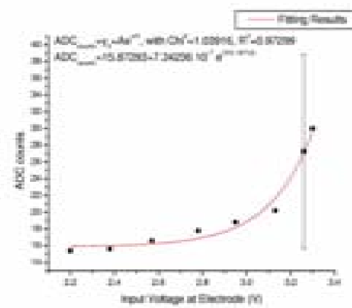


Figure 6.15: Pixel Voltage Correspondence for ADC counts.

The signal distribution Fig. 6.14 shows that the value of the reference pixel is 27.26 ± 11.59 counts. The equivalent voltage value at the electrode is found at Fig. 6.15, where the mean value corresponds to 2.6V, but the σ puts the error bar input voltage out of scale. This behavior has also been observed for signal in the range of 1.6V to 3.3V, showing slight changes that do not correspond with the expected ADC counts. For input Reset values below 1.6V but higher than 1.1V, the results seem to be not stable, showing two kinds of outputs (0 and similar count values to the previous case). These behaviour is due to comparator instability. For any value below 1.1V the output is always 0.

Another drawback to the switching approach used in the design is the tree structure (see Fig. 6.16), used to decrease the capacitance on the output bus, before the comparison, also presents some behaviors not desirable for the pixel performance.

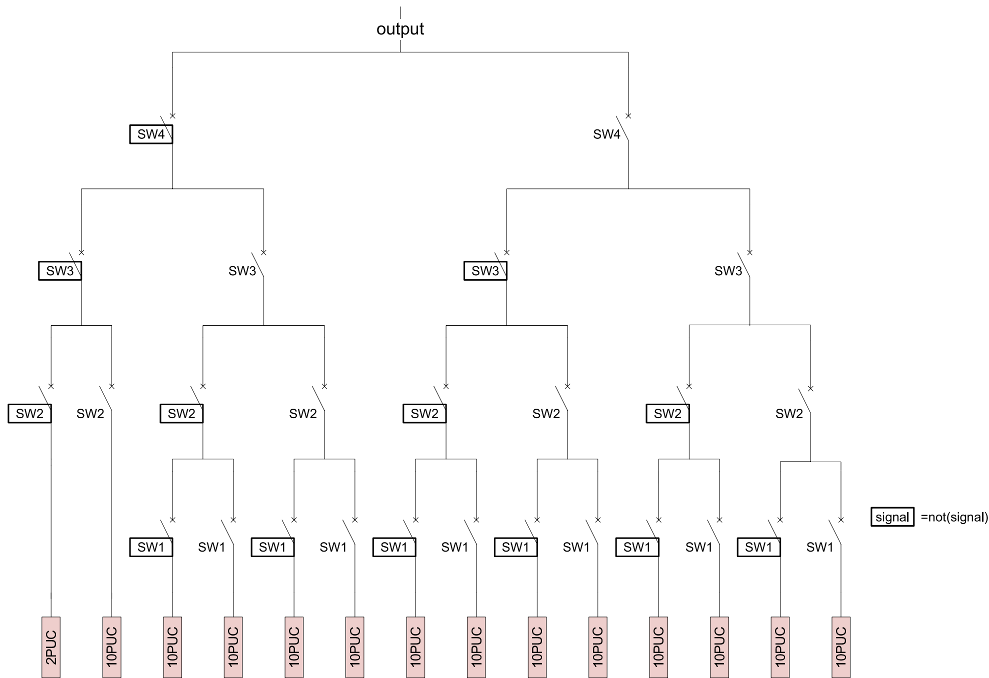


Figure 6.16: Tree structure used for capacitor control at Wilkinson.

The pixels structure can be divided in 80 + 52 pixels per row. The first 20 pixels of each of each sub-divisions created per row provides a constant 0 ADC count, clearly incorrect. This problem was initially linked to speed readout, but after decreasing the readout speed from the initial 4 MHz, down to 400KHz, no noticeable change was observed. This indicated a problem in the layout of the tree structure, further optimization is required for the use of a tree structure for voltage output readout.

6.4.4 Test Results

The test results obtained for the Wilkinson have not been successful. The main reason for the failure whas been a design flaw not including an high impedance output transistor (in a common source amplifier configuration) at the storage cells to readout the electrode's voltage value. On the other hand, the layout has not been optimized for the tree structure, resulting in the loss of information of some of the

columns during a readout of the complete structure.

The design must be improved due to limited range. A new approach will be used in CAP6 prototype, which will continue evaluating the Wilkinson architecture.

6.5 Binary Approach Theory

A new digital readout has been developed and introduced to test basic functionality of a new digital concept. The new digital architecture approach is trigger rate independent. The PUC is based on measuring thec hargeduring each clocked comparator interval (100ns). When this charge is above a set threshold, the local digital buffer is set to binary 1. At the next clock interval the information is shifted to both left and right adjacent pixels in the same row. After every shift, the information is OR'ed with the potential hit occurring in the next clock interval. The hit information is transferred from PUC to PUC in both directions (see Fig 6.17), until it reaches either end of the row. On the readout side, output drivers broadcast the data out of the chip.

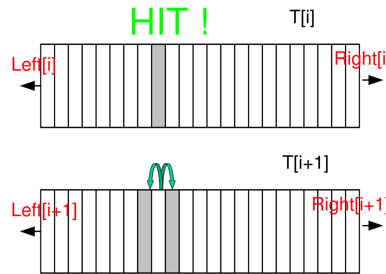


Figure 6.17: Simple example of temporal behavior of a signal in the Binary architecture.

With this readout scheme, we should benefit from working with digital signals, driving the bus across the chip will no longer be a problem and noise pickup will be reduced except for the 10MHz clock noise. Requirements for speed should also be easier to fulfill. The quantity of broadcasted data would also be reduced compared to the analog architecture used in CAP1, CAP2 and CAP3. The reason for using both outputs, and not just one, is to have extra information that will allow us to do the data processing that will decide when and where a hit has taken place. A simplified example for 6 cells of how the processing is done is the following. If

CELL POSITION	Left Out	Right Out
1	j+1	j+6
2	j+2	j+5
3	j+3	j+4
4	j+4	j+3
5	j+5	j+2
6	j+6	j+1

Table 6.1: Timing example for Left and Right Output signals.

a hit happens in PUC2 in T[i]. The result will come out from the left at T[i+2] and from the right at T[i+5]. If this data is analyzed, for a T[j] the hit left/right timing expected is found in Table 6.1 and finding hits becomes a simple task that can be done by a simple recursive C program. Once the processing is done, it can be plotted using ROOT. A few examples with the 6 PUC structures are the following:

1 Hit If one hit occurs in the System, the calculations are defined by Table 6.1, providing the time and location of the hit (see Figure 6.18).

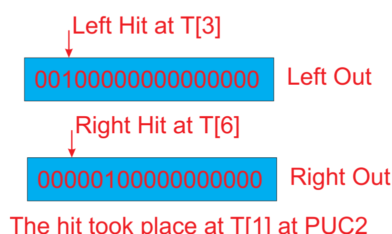


Figure 6.18: Example for the calculation of 1 hit with 6 PUC.

2 Hits: Case A If two single hits occurs in the System, the calculations are also defined by Table 6.1, providing the time and location of the hit per every left event, giving a total of 2 independent events (see Figure 6.19) .

2 Hits: Case B If two possible hits occurs in the System, the calculations are also defined by Table 6.1, providing the time and location of the hit showing that 1 left hit signal can proceed from more than one hit (see Figure 6.20).

The difference between case a and b is seen coming from the calculation. As can be seen from Table 6.1, the calculation is based on the delay difference between the left and right stream of data. The difference between a left hit and a right

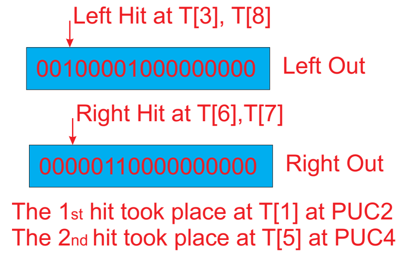


Figure 6.19: Example for the calculation of two hits with 6 PUC.

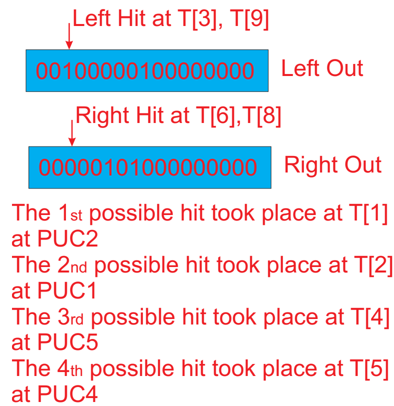


Figure 6.20: Example for the calculation of two hits with 6 PUC with possible error.

hit is always an odd numbers, which simplifies the hit determination, and an even difference is immediately thrown out. Case a is an example of the hit data clearly indicating only one hit in the row. Case b is more complicated, as each hit from the left output could potentially have two origins. Both origins in this case are marked as potential hit candidates. For a given trigger time, only one of these combinations should be allowed. This decision is acceptable based on the expected occupancy at the Belle detector, about 1%. If 120k pixels are used, 1.2k should be firing at the same time. The reconstruction software will take this number into account when reconstructing hits. This does leave room for false hits, but the expected false positives are low and will be more closely examined in a full sized detector.

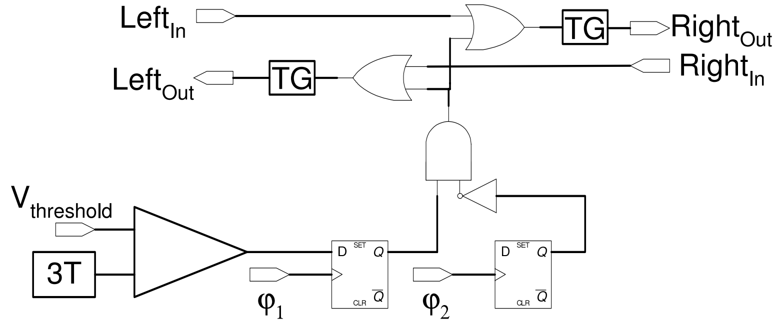


Figure 6.21: Schematic of the Binary architecture, including the 3 transistor structure, comparator, registers, and gate, or gate and transmission gate (TG).

6.6 Binary Solution

Two digital readout sensors are included in the CAP4 chip with arrays of: a primarly NMOS design with 149×12 pixels (also called Binary1) and a CMOS 118×17 pixels (also called Binary2). Both designs follow the same basic conceptual design. Binary2 is designed using CMOS architectures, whereas in Binary1 has been designed to reduce the number of PMOS transistors used. The use of PMOS in MAPS should be avoided because of parasitic charge collection by the extra N-wells. By examining both we will try to establish the functionality of a new readout concept, where the data is being *continuously* streamed out of the sensor without any trigger rate limitation.

The PUC is based on the same 3-transistor structure as with the analog CAP4, however, the analog signal from the charge collected at the electrode of each PUC in one clock interval (100 ns) is fed directly into a comparator, which produces digital information. In every clock interval, this digital bit of information is shifted to both left and right adjacent pixels in the same row, until the bit reaches the end of the row, when it is shifted off chip. For more details on the Binary see Figure 6.21 for an schematic or Section 6.5 for more theory details.

As the digital PUC size can in principle be reduced to about a half of the analog CAP PUC size (only one internal digital buffer is used instead of a large analog pipeline), the digital design would still provide excellent intrinsic resolution of around ~3-4μm.

6.6.1 NMOS Mostly Solution

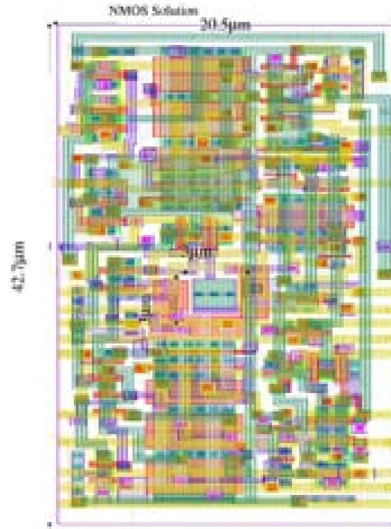


Figure 6.22: Detailed layout for the NMOS Binary Pixel Cell, including dimensions.

In the case of the NMOS solution, we have included 149 columns and 12 rows (see Fig 6.22 for PUC layout). Due to the architecture and layout, there will be 12 signals on each side of the detector requiring read out. There is a pad limitation in the design, therefore only 6 pads are available and the 24 output signlas are multiplex together. In addition, the left and right data for each row is not read out synchronously, and the data must be aligned off chip[8].

.

Additional values needing to be tuned include : Sensor (Tunable, used to set the value at electrode at testing PUC), Vreset (Tunable, initially set to 3.3V determines the drain voltage of the reset transistor at the 3T structure), $V_{source3T}$ (0.574V, determines the voltage for the current source used after the source follower), $V_{sourceComparator}$ (0.595V, determines the voltage to set the current source used at the comparator), $V_{threshold}$ (1.46V, sets the threshold level at the comparator,

[8] For the ROW0, the Right Output will come from PAD3 when MUX0&MUX1==0, but the Left OUtput will come out from PAD8 when MUX0&MUX1==1.

referred to the electrode) and V_{preamp} (2.28V, determines the top voltage used to avoid the use of PMOS transistor at the comparator). The additional digital signals needed are: PHI1, PHI2, Clock1 and Clock2 (used to synchronize the transfer of the information, see Figure 6.23 for representative timing details) and Reset (Tunable, initially set to 3.3V, but with a high level voltage tunable obtain highest gain).

Figure 6.23: Detailed timing scheme for the digital signals that have to be applied to the Binary (both NMOS and CMOS) different structures.

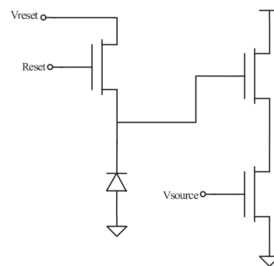


Figure 6.24: 3T structure schematic.

Test Results for NMOS Binary and Discussion

The NMOS Binary desiign was initially thought the more likely of the designs to work successfully. The reason for this idea was based on the use of a minimum area for the PMOS transistors (parasitic nwell), with their parasitic n-wells. This optimism was unfounded due to the fact that the reduced PMOS transistors were inadequate for proper circuit operation.

The primary changes included compared to the CMOS design was the elimination of as many PMOS transistors as possible. The simulation data showed the design should work, but experimentally the NMOS did not work correctly. The common components used for both NMOS and CMOS implementations are:

3T structure The same 3T structure has been used, including a Reset Transistor (with a drain and gate tunable voltage), a source follower (with the drain connected to V_{DD}) and a current source (see Figure 6.24).

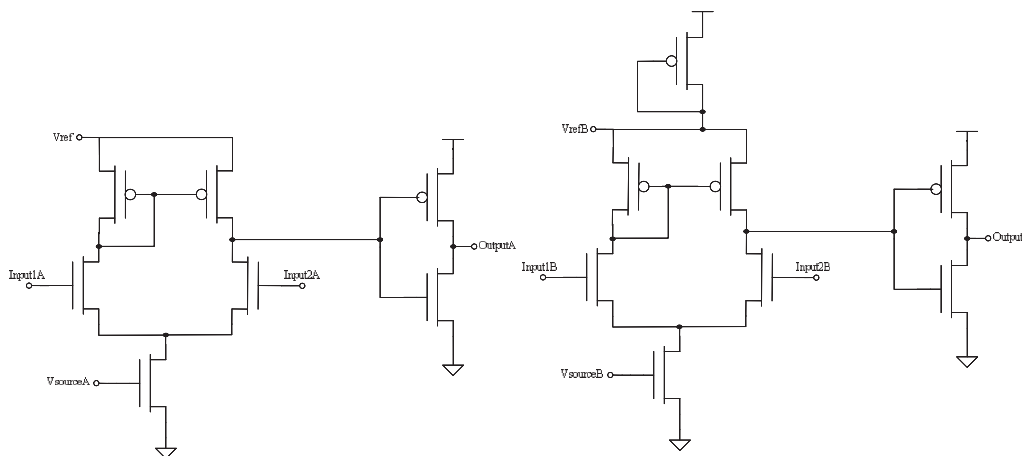


Figure 6.25: Comparator schematic for NMOS (left) and CMOS (right).

Comparator The comparator is one of the structures differs substantially. Here a differential pair with an output buffer is used. The difference between both of them is the presence of a PMOS used in diode configuration as an active load at the CMOS architecture (see Figure 6.25).

AutoZero Circuit The auto-zero circuit is another structure that differs. There are three components comprising the circuit: two transparent latches with one AND gate. The transparent latches are used as a D Flip-Flop (see Fig. 6.27). The AND gate has one input inverted (see Fig. 6.28). In both designs, the

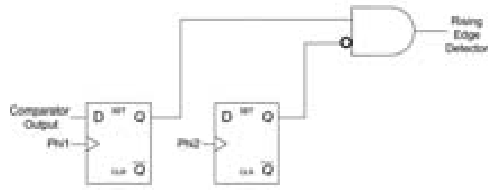


Figure 6.26: Rising Edge detector schematic.

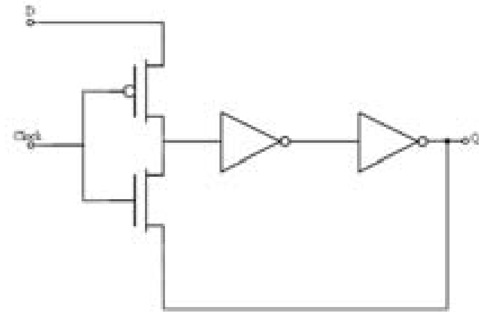


Figure 6.27: Register schematic.

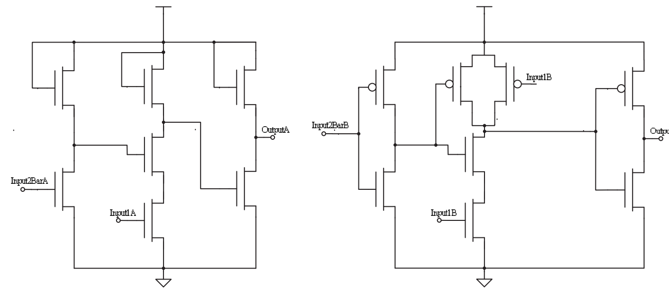


Figure 6.28: AND Gate with 1 inverter input schematic for NMOS (left) and CMOS (right).

transparent latches are identical, the AND meanwhile has NMOS transistors used in a diode configuration instead of PMOS transitors, in the case of the NMOS design.

OR Gate also has a different structure, where again the difference is used of NMOS as active load instead of PMOS (see Figure 6.29).

Transmission Gate (TG): The transmission gate is the same between both designs. The transmission gate includes two storage-transmission structures, with an inverter and a NMOS switch (see Fig. 6.30).

All the mentioned components were throroughly simulated, individually as well as a collection. Each simulation passed and worked as expected. A brief

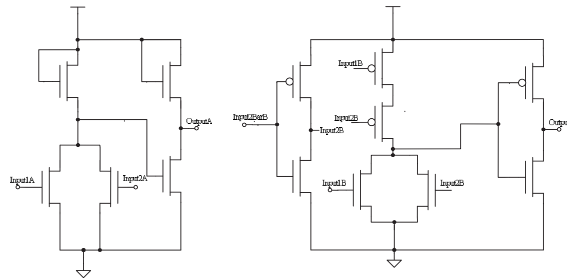


Figure 6.29: OR Gate schematic for NMOS (left) and CMOS (right).

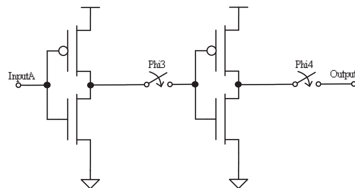


Figure 6.30: Transmission Gate schematic for NMOS and CMOS.

analysis describing the differences in the compononets follows.

The comparator structure only difference is the voltage found at the differential pair top node. In the case of the CMOS architecture a diode is used to set that to the desired voltage, in the case of the NMOS this voltage is set directly by an independent voltage pin.

The AndX gate is the next circuit presenting a difference between the two designs. The NMOS design includes all NMOS transistors in diode configurations. The CMOS design includes PMOS transistors. In the NMOS inverter design, the configuration becomes a Common Source Amplifier with an diode connected load. The analysis of thie inverter circuit is the following, for low V_{in} the common source transistor is in the Cut-off region and the diode connected load is in saturation, giving a maximum output voltage of V_{MAX}=V_{DD}-V_{THN}. When the input voltage starts increasing, common source transistor is taken out of the Cut-Off region and it enters in saturation until it generates enough current to allow the decrease of the

output voltage until the linear region is achieved.

The modifications to the NMOS AND gated consists of a diode connected load for two parallel PMOS transistors. In this configurations, the analysis of the circuit is very similar to the analysis performed above. The current at the bottom transistors the two of them need to be active (high). In the case of having any of them low, the voltage found at the output will be determined by V_{DD}-V_{THN} and only in case both of them are high we will make that both transistor conduct current. Depending on the order of switching states the order of modes for each case is determined.

The OR gate is the last circuit containing a difference between the two designs. The analysis is very similar to the AndX (for the inverter), the part that includes the NOR gate is also very similar to the AND gate. The NOR gate has been modified and a diode connected load has been used instead of the serial PMOS transistors. In any low-to-high transition on the input occur, the analysis is the same as for the common source case. The situation is similar when both input signals transition from high-to-low or both inputs are low.

This technique to minimize the number of PMOS is rooted in the processes which had no PMOS transistors available. The design approach is based on a top NMOS-diode. The NMOS-diode is found always on saturation, and the a primarly difference compared to a CMOS process is the highest logic level is not V_{dd}, but a lower logic level.

After a careful analysis of the circuit and a comparison with the results obtained from the CMOS architecture (see Section 6.6.2) the following conclusions were reached. The comparator should be working correctly, based on the idea the CMOS comparator is working correctly. Both use the same differential pair principle and simulations were successful for both designs. The digital parts of the circuit raise the most concert. The NMOS-diode is going to be conducting current almost always for the AndX and the OR gate, which lead to increasing current consumption and heating of the circuit.

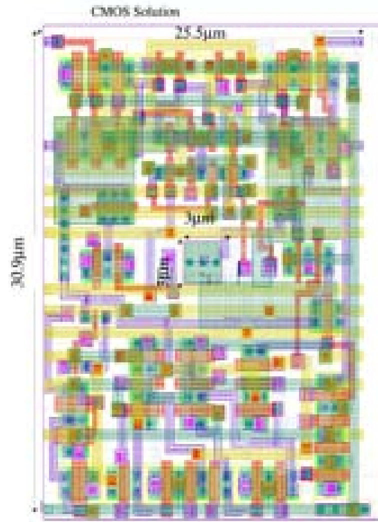


Figure 6.31: Detailed layout for the CMOS Binary Pixel Cell, including dimensions.

6.6.2 CMOS Solution

The CMOS design includes an array of 118 columns by 17 rows (see Fig 6.31 for PUC layout). The outputs are 17 signals from the right and 17 signals from the left. In this case, 6 pads have been assigned, and new control signals are used for multiplexing. As in the case of the NMOS desgin, the left and right output for a row will not come out synchronously, rather the data must be aligned off chip. Analog values neeeding to be tuned include: Sensor (Tunable, used to set the value at electrode at testing PUC), Vreset (Tunable, initially set to 3.3V determines the drain voltage of the reset transistor at the 3T structure), $V_{source3T}$ (0.574V, determines the voltage for the current source used after the source follower), $V_{sourceComparator}$ (0.595V, determines the voltage to set the current source used at the comparator), $V_{threshold}$ (1.46V, determines the quantity setting of the threshold at the comparator, referred to the electrode). The additional digital values needed are: PHI_1, PHI_2, $Clock_1$ and $Clock_2$ (used to synchronize the transfer of the information, see Figure 6.23 for all the timing details) and Reset (Tunable, initially set to 3.3V, but with a high level voltage tunable to obtain highest gain).

General Description The CMOS Binary design provides an output generated as a digital signal. The output signal is the result of shifting each pixel's digital

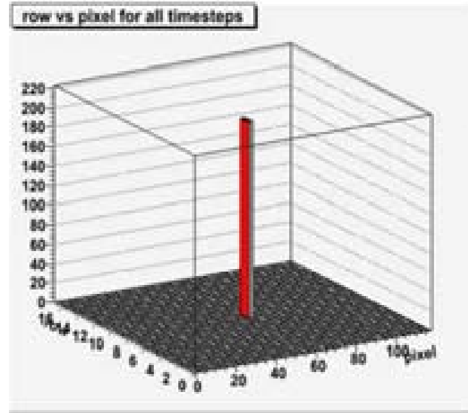


Figure 6.32: Plot obtained for 1 Hit in the CMOS Pixel architecture.

hit signal to each adjacent pixel. The timing of the arriving signals at the left and right side of the row defines the position of origin within the row. After the shifting of the signal (to left and right from each pixel) the resulting signal is multiplexed from 6 rows to one output pad. The signal coming from the pad is then sent to the FPGA which will rearrange the data into the proper format for later processing in software. The primary processed signal is then sent to the computer via USB. The data received via the USB interface is processed using custom software developed using ROOT. The ROOT software enviroment is able to handle the USB connection, as well as data processing and plotting of the results. The results appear as a 2D histogram, which each reconstructed hit is displayed on the histogram corresponding to the specific pixel reporting the hit. It is also possible in the reconstruction to calculate the hit time, from the timing of the left and right signals.

Initially the results obtained from the CMOS design were discouraging. No signal was obtained from the chip with the initially supplied tunable values. After modification to the clock signals (PHI_1, PHI_2, $Clock_1$ and $Clock_2$), it was observed the clock signals did not have time to propagate through out the entire chip. The clock speeds were lowered from the initial 10MHz to 2MHz. The signals were modified from the original specification (Fig. 6.23) to delay the comparator readout ($Clock_1$) to give additional time for the comparision. The last change, is related to the transfer cell timing signals. The clock signal PHI_1 is active while $Clock_2$ is active. In this case, PHI_1 transitions low before $Clock_2$, which will avoid problems with instabilities. PHI_2 will transition high with a delay respective to PHI_1, as well

as extending the time PHI_1 is low.

The sensitivity of the detector was also a concern with a powerful laser. With a high output power on the laser, charge generation was spreading into multiple collection diodes. This was creating a large number of hits, swamping the readout and reconstruction. A second problem was the threshold voltage being set too sensitive (low), creating every pixel on. In this situation, the pixel would never reset back to logic '0' That produced a set of information that was useless because all the output pads were providing a constant 1.

To overcome these difficulties the reset was pulsed for a longer time period (as well as being set higher compared to the threshold voltage). The laser on pulse was decreased to inject less charge as well as decreasing the output of the diode by diadjusting all the laser alignemnt. Fig. 6.32 shows the results obtained after including all the modifications that have already been described above. As can be seen, the results are focused on a single pixel with the other pixels OFF. That precision is obtained by a high threshold with longer reset time (allowing more integration time). The next step in testing the CMOS architecture was determine the X and Y sensitivies of the array, sensitivity to radiation sources, noise measurements, and linearity of threshold. From these measurements, some new design flaws became evident,such as the impossibility of working at a threshold close to minimum will be explained later on this section.

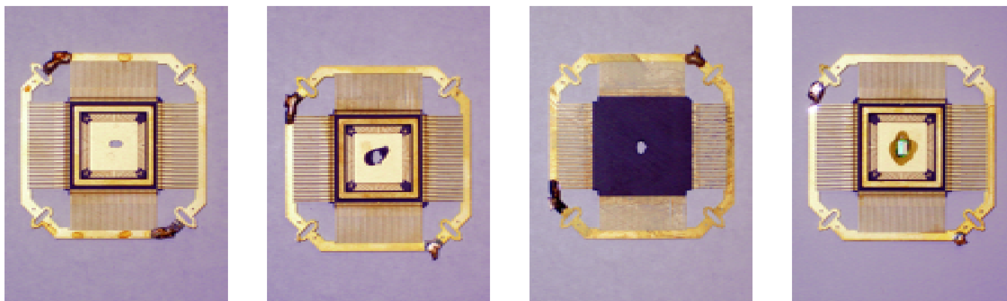


Figure 6.33: Top View of Package

Figure 6.34: Top View of Bad Package

Figure 6.35: Bottom View of Bad Package

Figure 6.36: Top View of epoxied Package

Sensitivity of the X-Y axis An X-Y motor was used to step through all the pixels in the chip. The chip had to be back-illuminated due to the metal present on the top layers. Therefore an opening in the chip packages was created. The chip was then epoxied over the hole so allow laser illumination on the back of the substrate. The task of creating the holes in the package was quite difficult and Fig. 6.34 and 6.35 shows examples of damaged packages. Fig. 6.33 shows an example of a correct hole. To use the damaged packages, a plastic mold was created to fill the damaged parts with epoxy. Once the epoxy was dry, the chip could lay flat on top of the package (see Fig. 6.36) and the wire bonding could be done. One scanning test was a zig-zag pattern, that rastered the laser across the pixel array, as shown in Fig. 6.37. The chip was tuned to minimize the number of hit pixels. The result of the Zig-Zag test show fluctuations with the number of hits detected, showing the highest number of hits at the corners of the trajectory with respect the straight lines that are between the corners. The reason for for this effect is the non-uniform speed of the laser which is controlled by a computer program. The read-out characteristics for this test was a speed of 2MHz, that becomes 20MHz read-out speed after considering the output multiplexing.

Chattering Pixels and Filtering The problems found with the response of this chip can be summarize as the presence of chattering pixels and the fact that the architecture implementation has a problem when more than one hit appears in an output sequence.

- Chattering pixels appear because of the use of a transparent latch instead of a flip-flop in the design of the comparator. The reason for including the latch was the minimization of the area per pixel, the latch had only six transistor which allowed the use keep the area minimum.
- The algorithm to reconstruct the hits that are sent by USB presents the problem in that extra hits are generated when more than one hit happens. False hits generate an incorrect image and mislead the user into what is happening with the detector.

Chattering pixels generate what has been called ghost hits. Ghost hits appear in two differerent situations: for charge signals near threshold that take the comparator to a situation where it will keep generating hit signals, or a situation of charge sharing.

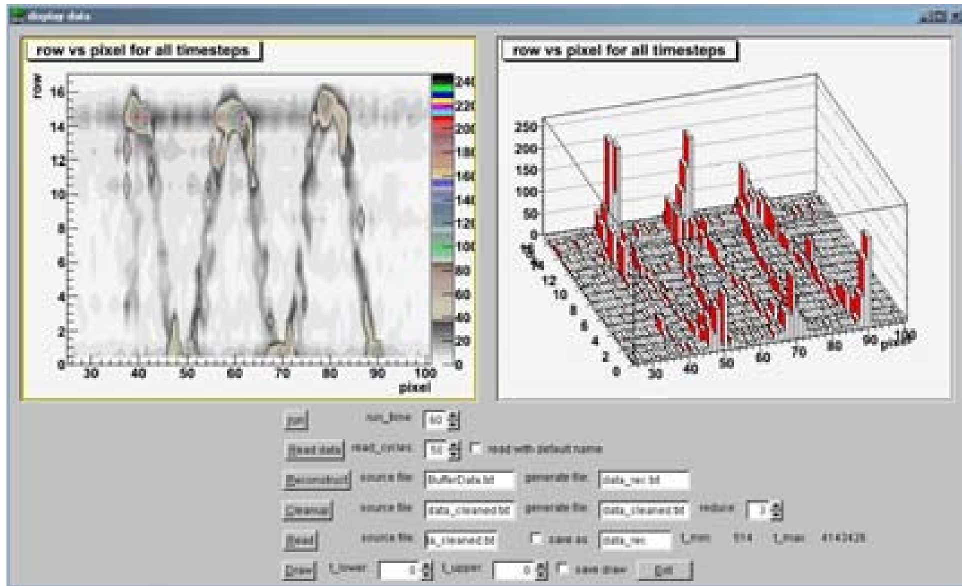


Figure 6.37: Zig-zag test performed with CMOS Binary.

The charge sharing will appear for higher threshold voltage values, but will generate the extra hits because of the design algorithm flaw. For solving the algorithm problem, the solution would be to use a 3 channel pixel, where the information would go come from 3 different sources to do the comparison (like an hexagon). This solution may be implemented in the next versions of the CAP family if the area can be kept small enough to follow the specifications of minimum size of $\sim 10\mu$. The second solution happens when the ambiguity is removed by checking for pixel correlations at a fixed time after the laser is fired. In this design the solution was to implement a chatter filter in the reconstruction software. This chatter filter distinguishes the real pixels hitting at a specific time. Fig. 6.39 shows the reconstructed results after the anti-chatter filter. The reconstruction after the anti-chatter filter shows a good improvement. Fig. 6.38 shows a typical image where all the variables have been tuned but chatter has been generated. The image is clearly improved and the laser raster becomes distinct, and without significant tails. The reconstruction software is based on a comparison of the timing of the arriving signal and a fixed laser pulse latency.

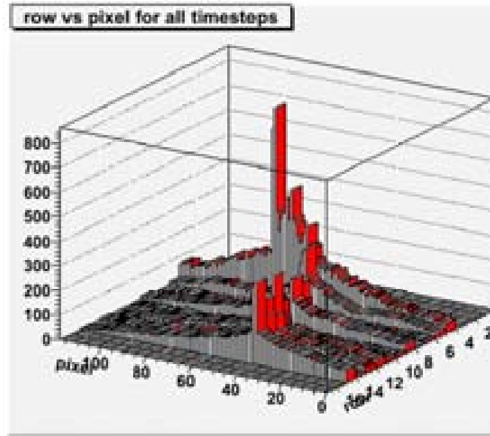


Figure 6.38: Pre-filter image obtained.

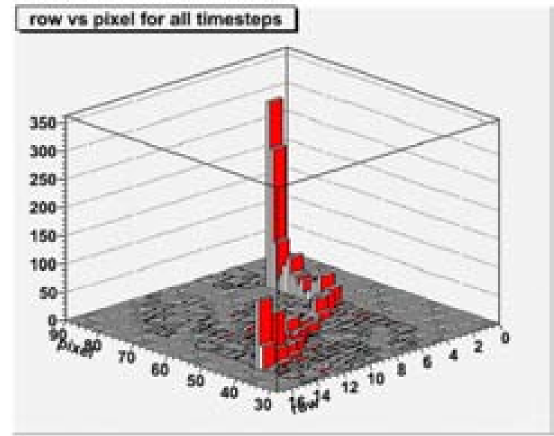


Figure 6.39: Post-filter image obtained.

Electronic Noise Measurement (ENM)is one of the more important parameters to define in a detector. To measure the ENM, it is neccessary to measure the turn-on curve for the pixels. The fact that the chattering does not allow us measurement of a reliable threshold makes such a statistical evaluation of the pixel response impossible. For the same reason, the detector was exposed to a radioactive source for a long period of time (1 day) and the same chattering problems were observed. The need for using long acquisition times between reset ended up making itimpossible to obtain a read-out usable with a radiation source, where all the pixels seem to be providing signal any time anything was recorded.

Linearity of maximum threshold and laser pulse length The last test done with the detector was to vary the length of the laser pulse applied and see corresponding change in onset threshold value. The amount of charge created on the pixel by the IR laser is proportional to the laser pulse length. According to that simple rule, the longer the pulse the higher the threshold can be set on the pixel to still detect the laser. For the corresponding charge generated at the pixel (see Fig. 6.40) a pixel input capacitance of 2.11 fF was used. This value was obtained from the calculation based on the physical parameters of the detector and the specific architecture used in this case. Fig. 6.40 shows that for a laser pulse length that varies from 40ns to 15μs the threshold valued used to detect will also go from a few mV for the shortest laser pulse to about 1.20V for the longest laser pulse. The equivalent calculations

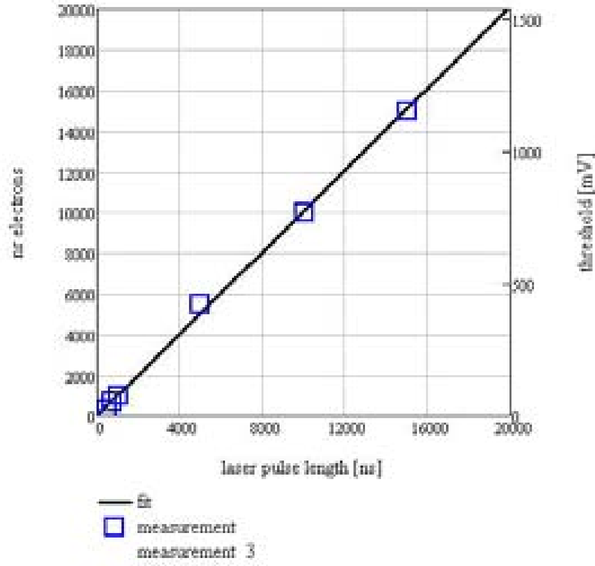


Figure 6.40: Threshold Value vs Laser pulse length.

of charge that has been detected per pixel gives a maximum value of 15000e$^-$ for the case of a pulse that is 15μs. Fig. 6.40 calculations are based on two different values that are measured. The first one is what has been called *threshold high*; it consists of the measure of the threshold when the first pixel fires. The second value is the *threshold low*; it consists of the threshold value when other pixels start firing as well, due to noise. The charge is calculated as (*threshold high* - *threshold low*)$\times$capacitance. This curve does not go through zero, but the offset of a linear curve fit is substracted. This representation change dramatically if the charge is shared with other pixels, with a much slower rising curve, as seen in Fig. 6.41.

6.7 Conclusions

The results obtained with CAP4 have been both exciting and interesting. This CAP4 prototype has taken the development of the test set-up to a new challenging situation. The laser set-up has been upgraded to allow a more accurate testing with an IR laser. The second new work that has been developed in parallel has been the fabrication of a versatile hardware set-up. This set-up mainly consists of two new boards (COBI and PETRA). COBI has been develop to enable USB communication with a computer, as well as, incorporate all the analog and digital circuitry that may be needed. PETRA is the board that contains the tested CAP4.

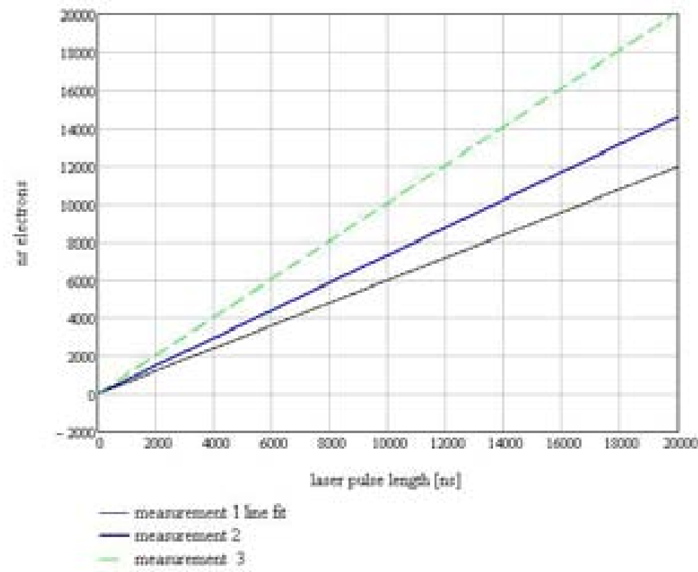


Figure 6.41: Threshold Value vs Laser pulse length for different positions of the fiber. It can be observed that the measured charge decreases as the it its shared by neighboring pixels.

CAP4 prototype includes two kinds of architectures. The first architecture is based on a Wilkinson readout. This part of the prototype had a design flaw that did not give any valid data. The second architecture is an innovative digital pixel architecture, called Binary read-out. The binary readout presented to approaches, that would differ in the number of PMOS transistors included. The approach that included less did not work properly, but the one that used the most traditional CMOS design approach showed a good performance, although also including some design flaw due to the minimum pixel size needed.

Chapter 7

Continuous Acquisition Pixel 5 *(CAP5)*

After the results obtained with the first four members of the CAP family, the fifth member was designed using a different technological approach. The possibility of using a SOI process appeared in the form of a collaboration provided by OKI and KEK. This collaboration was based on the use of a 0.15μm technology provided by the Japanese company OKI through KEK. This run included two different designs of pixels and the chips were tested during the second half of 2007 at the Instrument Development Labratory in Hawaii. The results of the testing are presented in this chapter. Section 7.1 introduces the SOI characteristics of the process provided by OKI, including the wafer characteristics from the first run. To analyze the different characteristics of the process, some TCAD studies were performed (in Section 7.2), including an analysis of the back gate effect and circuit-to-sensor cross talk. Section 7.3 shows the characterization of the transistors provided by the process. This characterization was needed in order to evaluate the effect of the Back Gate contact voltage (back gate effect) on the transistor and the possible consequences for the more complex circuits. Section 7.4 presents the results obtained from the chip. CAP used the same architecture described for the CAP4 Binary CMOS. The last Section 7.5 describes the results obtained from an X-Ray telescope pixel architecture included in the submission to OKI.

7.1 SOI Pixels using OKI Process

A highly resistive Si must be used to develop a particle detector using SOI technology. The highly resistive Si is used to make a thick depletion layer, to achieve

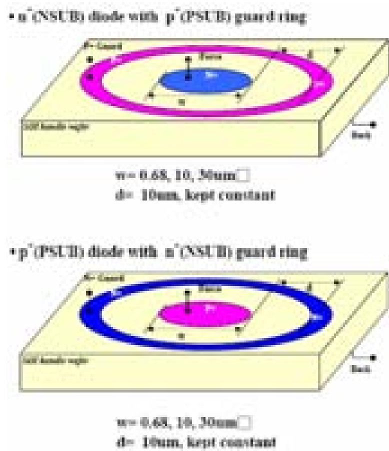


Figure 7.1: Two different diode structures analyzed to test the handle wafer.

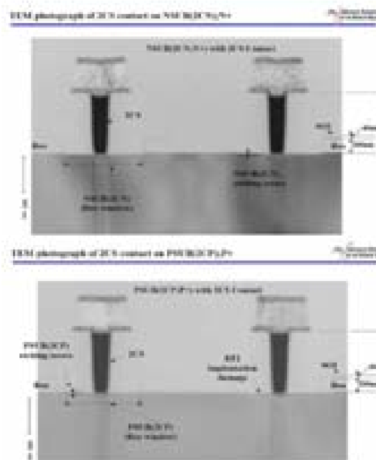


Figure 7.2: TEM photographs of the contacts and implants of the handle wafer.

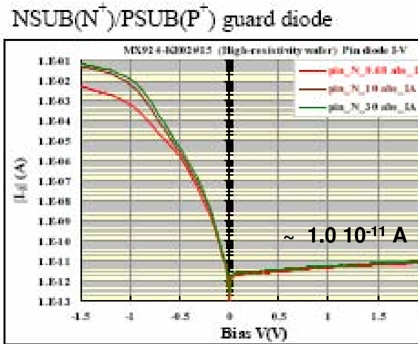
high-speed signal collection and to achieve high radiation detection efficiency. A low resistivity Si is needed for the LSI circuit to control the transistor parameters.

OKI started a R&D collaboration with KEK to allow the development of a SOI pixel detector in summer 2005 [40], [106], [107]. OKI is known as the world's first supplier of FD-SOI products. The basic technology to fabricate the pixel detector is the OKI's 0.15μm FD-SOI CMOS process. Additional processing steps (to create substrate implants and contact formation) were developed by this collaboration.

Two submissions with the OKI process have been done and were completed in spring 2006 (FY05 run) and January 2007 (FY06 run). The FY05 run was a MultiProject Wafer that obtained initial results. The FY05 run performed the measurements to characterise the handle wafer(see Fig. 7.1 to Fig. 7.6) and to analyze the process variations. Fig. 7.1 shows the two diode schematics analyzed, assuming a n-substrate handle wafer with $\sim$700Ωcm. The first diagram considers the structure formed by the n+ implantation, with a guard-ring formed by p+ implants. The second diagram considers the implantation as p+ and and the guard-ring is n+ implant. These 2 structures can be seen in Fig. 7.2 with two Transmission Electronic Microscopy (TEM) photographs showing the actual contacts. The measured results

Typical diode I-V curve

NSUB(N^+)/PSUB(P^+) guard diode



PSUB(P^+)/NSUB(N^-) guard diode

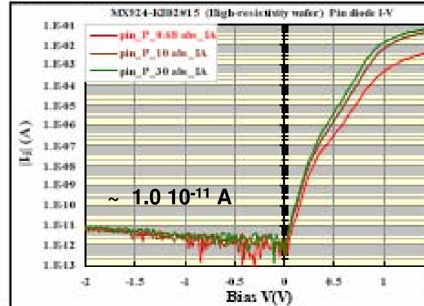
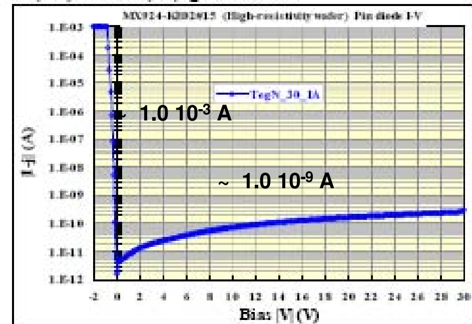


Figure 7.3: Typical diode I-V curve for the n-substrate ~700Ωcm ~6 10^{12}cm^{-3} doping concetration, for the two different diode structures described at Fig. 7.1.

Typical reverse I-V curve of a diode

NSUB(N^-)/PSUB(P^+) guard diode



PSUB(P^+)/NSUB(N^+) guard diode

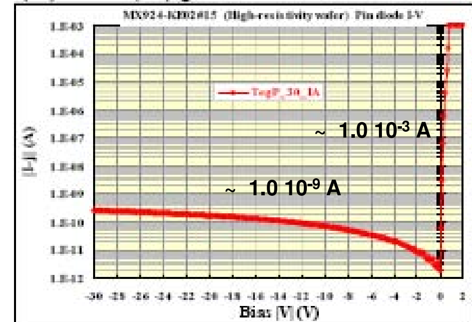
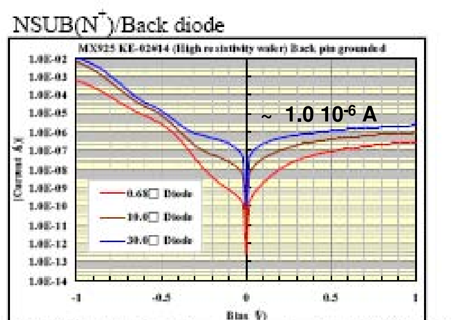


Figure 7.4: Typical reverse I-V curve for the n-substrate ~700Ωcm ~6 10^{12}cm^{-3} doping concentration, for the two different diode structures described at Fig. 7.1.



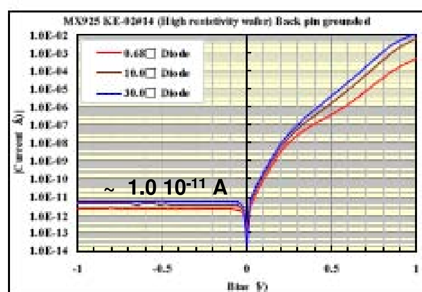
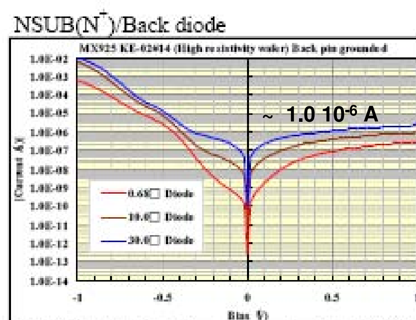


Figure 7.5: Typical diode I-V curve for the n-substrate ~700Ωcm ~6 10^{12}cm^{-3} doping concentration, for the diode structure described at Fig. 7.1 but considering the back gate contact, instead of the guard ring gate.



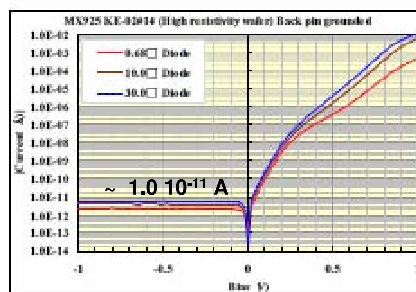


Figure 7.6: Typical diode C-V curve for the n-substrate ~700Ωcm ~6 10^{12}cm^{-3} doping concentration, for the diode structure described at Fig. 7.1 but considering the back gate contact, instead of the guard ring gate.

can be found in Fig. 7.3 for the typical diode curves, and Fig. 7.4 for the reverse curve of the same diodes. When considering high back voltage applied, the value for the leakage current is 1nA in both cases.

The next measurements are also done for a diode structure, but in this case, instead of considering the guard-ring as one of the terminals of the diode, the back-gate contact is used as the terminal to measure the output current and these measurements are plotted in Fig. 7.5. The last measurements done to test the handle wafer is the C-V curve for the structure, and the results can be found at Fig. 7.6.

The FY06 run was a MultiProject Wafer (MPW) with 17 user designs. The wafer was 6 inch diameter and the mask size was 20.8 $\times$ 20.8 mm^2. The wafer includes submissions from Osaka University, Tokyo University, University of Hawaii, Japan Aerospace Exploration Agency /Institute of Space and Astronautical Science (JAXA/ISAS), Fermilab, Lawrence Berkeley National Laboratory (LBNL) and KEK.

Process	0.15μ FD-SOI CMOS process 1 poly and 5 metal layers
SOI wafer	Diameter: 150 mm ϕ (SOITEC) Top Si: Cz, $\sim$ 18 Ω-cm, p-type, $\sim$40nm thick Buried Oxide: 200nm thick Handle wafer: Cz, 700Ω-cm, 650μm thick
Backside	Thinned to 350μ and plated with Al (200nm)
Supply Voltage	Core 1V, I/O $\sim$1.8V
Transistors	High Voltage Tr(I/O), High Threshold Tr, Low Threshold Tr, Floating body and body tight Tr.

Table 7.1: Process characteristics of the OKI SOI process

The characteristics of the process are summarized in Table 7.1. The SOI wafer is a low resistivity p-type Si on top with a high resistivity (700Ω-cm) n-type substrate on the bottom. The process flow of the SOI pixel is described using Fig. 7.7, Fig. 7.8, Fig. 7.9, Fig. 7.10, Fig. 7.11, Fig. 7.12 and Fig. 7.13. The implantation of p+/n+ to the substrate is performed after cutting the BOX layer. The FY05 run had the substrate implants done under the same conditions as the drain/source implants ($\sim$0.1μm). In the FY06 run the implants were deeper, tar-

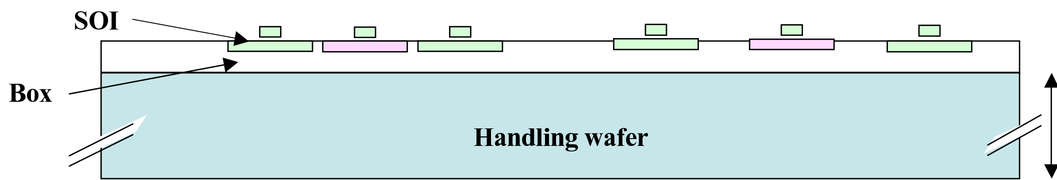


Figure 7.7: After Gate formation for CMOS processing the stack formation takes place (with extension and sidewall formations). The dimensions at this point are thickness of handling wafer 650μm, thickness of BOX 200nm and thickness of implants for SOI active circuitry implants of 50nm.

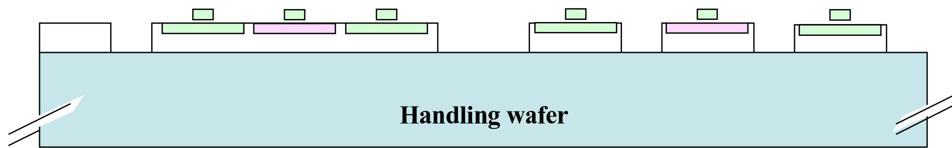


Figure 7.8: Photolithography and etching

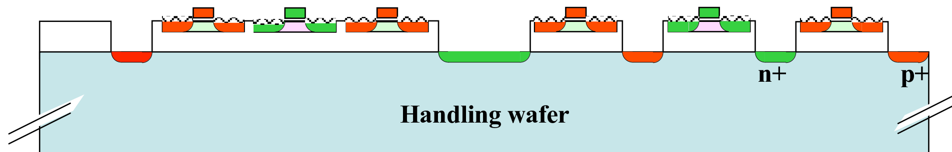


Figure 7.9: S/D Implantation followed by S/D annealing and Salicidation

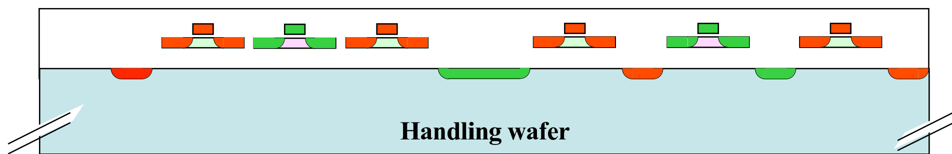


Figure 7.10: 1st ILD filling and CMP planarization (after Salicide formation)

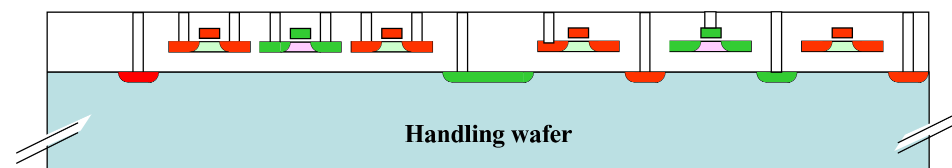


Figure 7.11: Contact etching (for gate of transistor and for substrate)

geting a ∼4.7 times deeper implant profile. After forming contacts between p+/n+ implants and the 1st metal layer, normal SOI CMOS processing is performed. After wafer processing, the wafer backside is ground mechanically to ∼350μm, then plated with 200nm of aluminium. Detector voltage can be applied both from bottom and top pads, which are connected to a high voltage n+ implant ring.

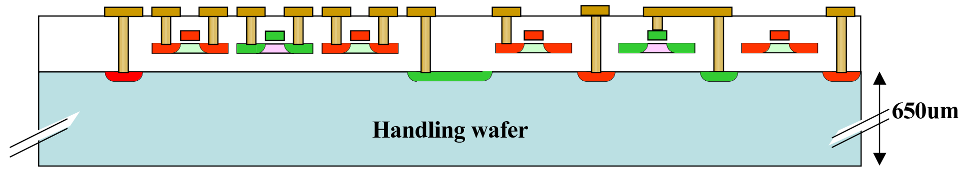


Figure 7.12: Contact plug filling and 1st Metal formation

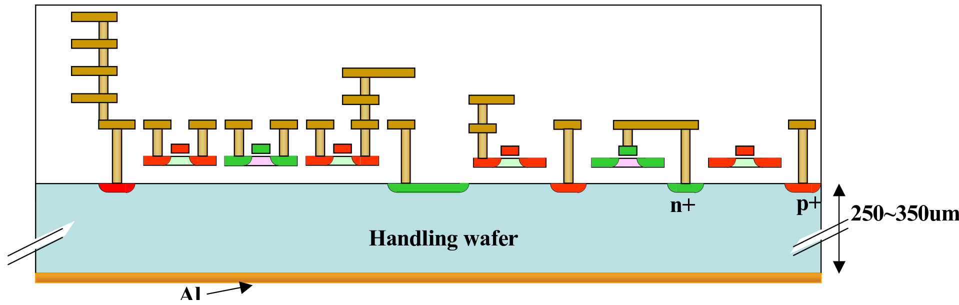


Figure 7.13: 5 Metal layer formation followed by Backside polishing and Au coating

Fig. 7.14 shows a TEM photograph of the cross section of the p+ implant to the substrate and contact to the 1st metal later. Sheet resistance[1] of the p+(n+) implant is measured to be 136(33)Ω/□, and the resistance of the 0.16×0.16μm contact to the p+(n+) implant is 218(87)Ω.

7.2 TCAD studies

TCAD is used to simulate the process device operation. ENEXSS is the software used, which has been developed by SELETE [108]. The results obtained are an extraction from a very small scale simulation.

Back Gate Effect Analysis The potential under the BOX acts as a back gate of the transistors in the top Si. As the back gate voltage is increased, the NMOS transistor threshold voltage is decreased and the PMOS transistor threshold voltage is increased until finally the circuit stops working for excessive back gate voltage [40]. This is confirmed in test chips by observing an input-output signal of the I/O buffers

[1] Sheet resistance is a measure of resistance of thin films that have a uniform thickness and it is measured in ohms/square (Ω/□). The resistance is written as:

$$R = \frac{\rho}{t}\frac{L}{W} = R_s\frac{L}{W} \qquad (7.1.1)$$

R_s is then the sheet resistance. The term ohms/□ is used because it gives the resistance in ohms of current passing from one side of a square region to the opposite side, regardless of the size of the square.

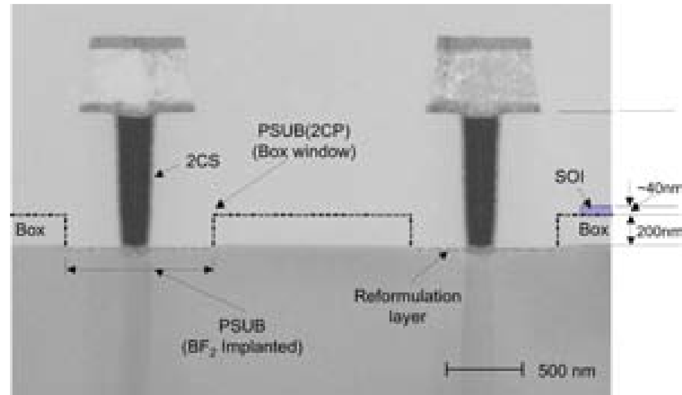


Figure 7.14: TEM photograph of the p^+ implant and contact cross section.

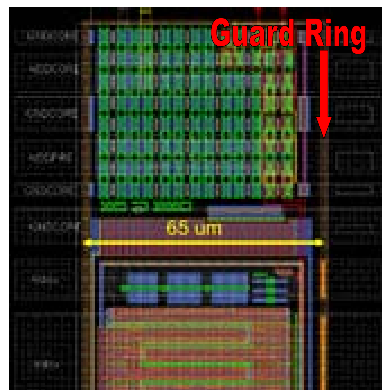


Figure 7.15: I/O buffer layout, improved with Guard Ring consisting of a p+ implantation.

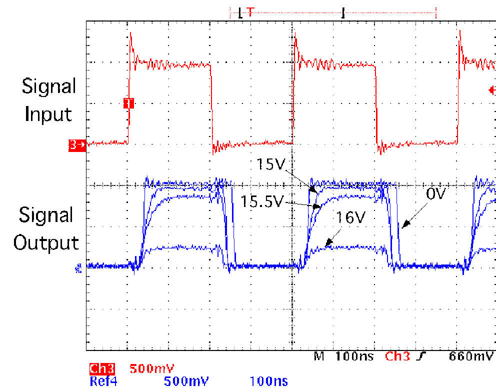


Figure 7.16: Signal obtained with the buffer, with no p+ implantation, it is almost undetectable for $V_{back-gate} >$ 15V.

Figure 7.17: Buffer signal, with p+ implantation, detectable for V_{bg}~10V.

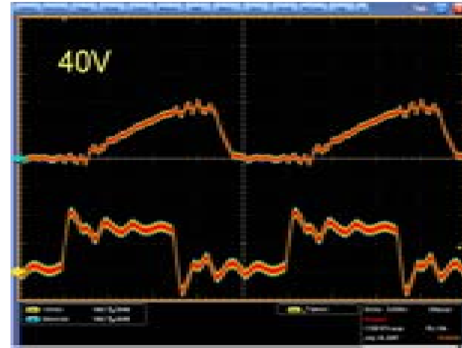


Figure 7.18: Buffer signal, with p+ implantation, detectable for V_{bg}~40V.

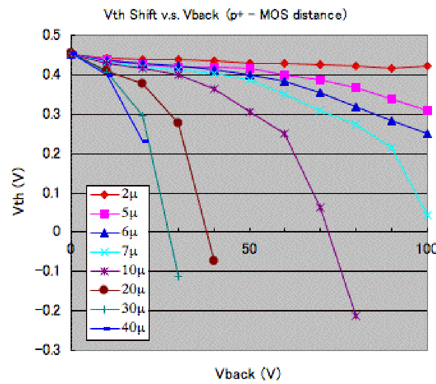


Figure 7.19: $V_{nmos-threshold}$(simulation) vs. $V_{back-gate}$.

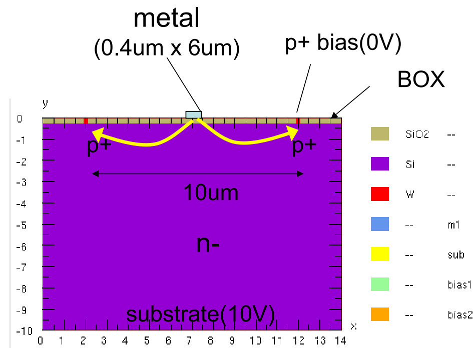


Figure 7.20: Schematic of the structure used to analyze the cross-talk.

where no p+ exists, so the detector voltage is almost directly applied to the back of the I/O buffers (see Fig. 7.16). In this case, the output signal becomes very small when the back voltage exceeds 15V. This back gate voltage can be reduced by placing a p+ implant near transistors and connecting it to ground voltage (see Fig. 7.15 for the layout), obtaining a threshold voltage shift reduced to 100mV at a back voltage of 40V (see Fig. 7.17 and Fig. 7.18 for the different output signals obtained for back-gate voltage of 10V and 40V). This is confirmed with ENEXSS simulations as seen in Fig. 7.19, where each curve corresponds to the distance between the NMOS and the p+ implant. By placing p+ implants within 10μm of the transistors, the threshold voltage shift can be reduced to less than 100mV at a back voltage of 40V [1].

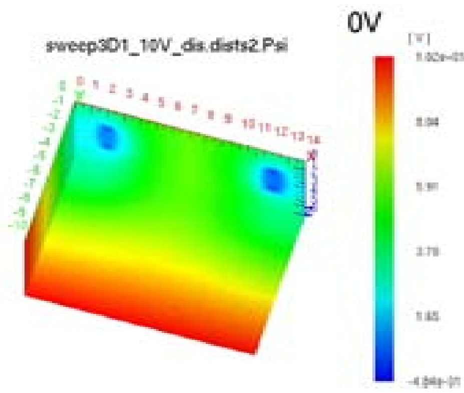


Figure 7.21: Potential distribution around a p+ sensor node simulated using ENEXSS[1].

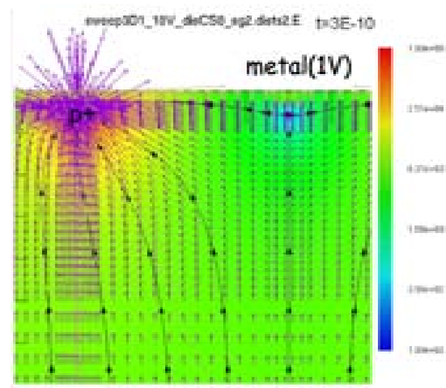


Figure 7.22: Electric field map and lines of electric force around a p+ sensor node simulated using ENEXSS[1].

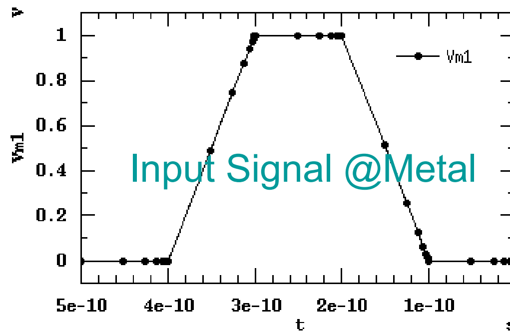


Figure 7.23: Input voltage signal applied to top metal layer, corresponding to structure of Fig. 7.20.

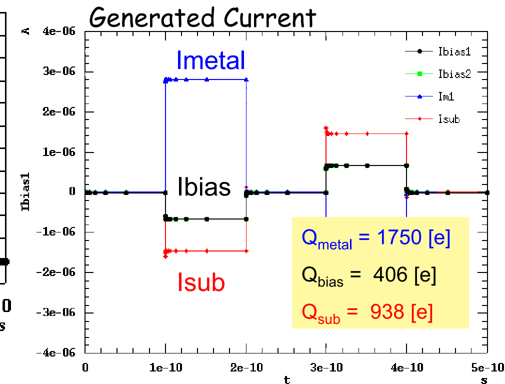


Figure 7.24: Output current (and charge injection) result obtained from the input of Fig. 7.23.

Circuit to Sensor cross talk The electronics and sensor are separated by a BOX layer, with a 200nm thickness. Although good isolation is expected between circuit elements, cross talk studies between circuitry and sensor have been performed. Fig. 7.20 shows the selected geometry being analyzed, where two p+ implants are located 10μm from the top centered metal layer. Fig. 7.21 and Fig. 7.22 show the simulated electric field and lines of electric force. There is a p+ implant in the upper left and a metal signal line at the upper right. Voltage change in the metal line disturbs the electric field, so some amount of charge is induced through capacitive coupling, and in some cases cannot be negligible. Lastly, Fig. 7.23 and 7.24 show the results obtained when considering an input pulse at metal 1 of 1V for 0.1ns. The results of this simulation are found in Fig. 7.24 where a current of $\sim$1.5μA (938e$^-$)

is injected into the substrate, considering an initial injection of electrons generating the initial signal of $1750e^{-}$.

7.3 Test Element Group Test

A test chip named TEG, developed by Prof. Arai at KEK, was used to characterize the transistors used in the SOI design. TEG 1 was fabricated with the FY05 run from OKI and TEG 2 was fabricated with the second run FY06. TEG 2 includes three different test structures: bare transistors (n-type, p-type, psubs-type), a transistor matrix and a ring oscillator. The **ring oscillator** is a 47 stage ring oscillator composed of NAND gates. It uses an input enable signal and provides an output oscillator signal.

The **transistor matrix** is also called **TEG** is a matrix of 32 NMOS (see Fig. 7.25) and 32 PMOS (see Fig. 7.26) transistors to extract the DC characteristics. Each transistor is selected by 3-bit column and 3-bit row decoders and NOR and NAND gates. It presents have of the rows with body-tie transistors and the rest with floating-body transistors. This matrix includes the 3 types of transistors available in the OKI process: I/O transistors (IO) with 5nm thick gate oxide layer, and high-VT (threshold) transistors for logic circuits and low-VT (threshold) transistors for analog circuits with 2.5nm thick gate oxide layer. The voltage tolerances are 1.8V for I/O circuits and 1V for core circuits. The buried oxide is 200nm thick. The backside of the wafer was ground mechanically to 350μm thickness and plated with 200nm of aluminium, used for back-gate biasing. The design for this structures does

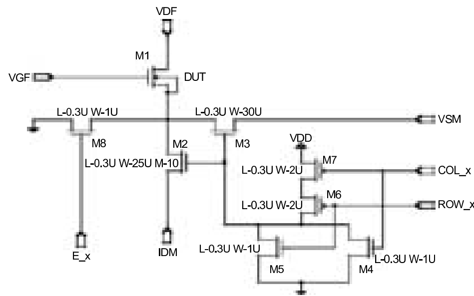


Figure 7.25: NMOS transistor circuit.

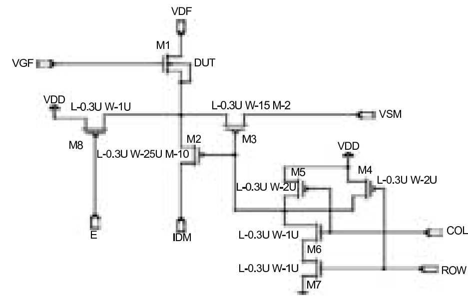


Figure 7.26: PMOS transistor circuit.

not allow the individual measurements because a design flaw. Every terminal will have connected for transistors (2 floating, 2 body-tie) and the measurements done

will be a sum of 4 transistors connected in parallel.

This structure was used to do irradiation measurements [61] with the NMOS and PMOS transistors. In both cases the threshold voltage decreased after irradiation. The NMOS low-VT with floating-body showed an increasing drain current after irradiation for the same V_{gs}. It seems to be already saturated at lowest fluence, with an increase in leakage current of 0.1mA in the sub-threshold region, with values of 10^{-8}A at V_{gs}=0V. For the case of the PMOS low-VT with floating-body also showed a decreasing threshold voltage after irradiation, with a decreasing drain current. In this case no increase at leakage current is observed. The threshold voltage shifts for a I_d of 500μA, after and before irradiation, are found to be about -0.1V for NMOS/PMOS low-VT and PMOS high-VT, -0.2V for NMOS high-VT and -0.35V for NMOS/PMOS I/O transistors. The highest shift for the I/O transistors is explained by the presence of a thicker gate oxide layer.

These results also evaluate the possibility of using a back-gate voltage to compensate for the variation in the threshold values. These experiments show the threshold shift is recovered for a value of -20V for the NMOS low-VT, -25V for the NMOS I/O and PMOS low-VT and high-VT, and finally a value of -30V is used to compensate for the NMOS high-VT and PMOS I/O.

7.3.1 BareN Cell results

The **Bare transistor cells** are the last test structure. This chip subsection presents three types of transistors for analysis: NMOS type, PMOS type and sub type (where the NMOS/PMOS types are surrounded by 0.7μm psub). The transistors found in this **BareN Cell (nmos type)** are divided in 2 types: body floating type and body tie type (see Table 7.2 for more detail). The transistors characteristics of the BareN structure are obtained for a V_{drain} = 1 V (or 0.1V for threshold measurement), V_{source} = 0 V and sweeping of V_{gate}. There are two kind of measurement done, with and without HV, with any other signal floating.

HV floating results The first measurement of the drain-source current with the chip was performed keeping a floating back-gate contact. The results obtained are shown in Fig. 7.27, Fig. 7.28 and Fig. 7.29. The transistors parameters

Body Float Type				Body Tie Type			
Tr	**l(μm)**	**w(μm)**	**Transistor Type**	**Tr**	**l(μm)**	**w(μm)**	**Transistor Type**
M1	0.14	280	High Threshold	M9	0.14	280	High Threshold
M2	0.14	280	Low Threshold	M10	0.14	280	Low Threshold
M3	0.30	600	High Threshold	M11	0.30	600	High Threshold
M4	0.30	600	Low Threshold	M12	0.30	600	Low Threshold
M5	0.30	600	High Voltage	M13	0.30	600	High Voltage
M6	0.50	1000	High Threshold	M14	0.50	1000	High Threshold
M7	0.50	1000	Low Threshold	M15	0.50	1000	Low Threshold
M8	0.50	1000	High Voltage	M16	0.50	1000	High Voltage

Table 7.2: BareN Cell transistor description.

Transistor type	**high-VT basic logic**	**low-VT analog circuits**	**I/O (high-VT)**
Voltage tolerance(V)	1.0	1.0	1.8
Gate oxide thickness(nm)	2.5	2.5	2.5
Minimum gate length(μm)	0.14	0.14	0.30
Threshold voltage(V)	0.4V	0.2	0.5

Table 7.3: Transistor parameters for SOI process.

provided by OKI can be found in Table 7.3 and the $V_{threshold}$ obtained can be found at Table 7.4. The values obtained here are not extremely significant, because the high voltgate is floating. The measurements can however give an estimate as to the accuracy the threshold measurements are as provided by OKI in their documentation. This comparison show that the values found in this particular go from a 25% to a 200%.

Body Float Type				Body Tie Type			
Tr	**$V_{threshold}$ (V)**	**Tr**	**$V_{threshold}$ (V)**	**Tr**	**$V_{threshold}$ (V)**	**Tr**	**$V_{threshold}$ (V)**
M1	0.506	M5	0.787	M9	0.562	M13	1.443
M2	0.389	M6	0.866	M10	Non-Available	M14	1.120
M3	0.510	M7	0.617	M11	0.601	M15	0.387
M4	0.388	M8	0.387	M12	0.383	M16	0.879

Table 7.4: BareN Cell transistor threshold measurement obtained with HV floating.

Back Gate Effect in OKI SOI transistor Fig. 7.30 and Fig. 7.31 show the analysis of the effect of the back-gate high voltage on the drain current,

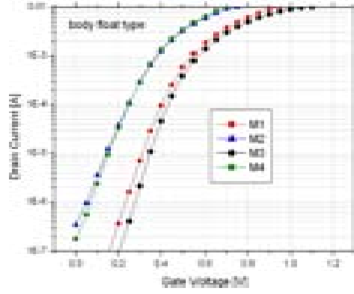


Figure 7.27: I_{drain} for M_1-M_4, Table 7.2 for details.

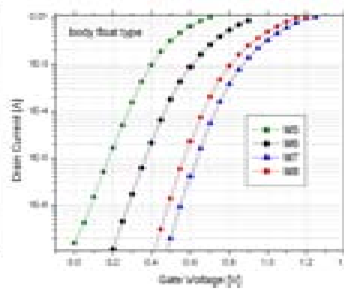


Figure 7.28: I_{drain} for M_5-M_8, Table 7.2 for details.

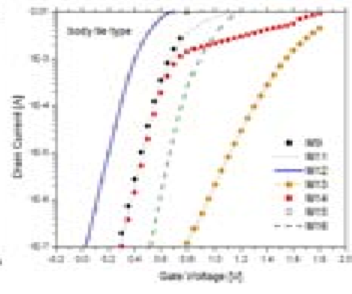


Figure 7.29: I_{drain} fpr M_9-M_{16}, Table 7.2 for details.

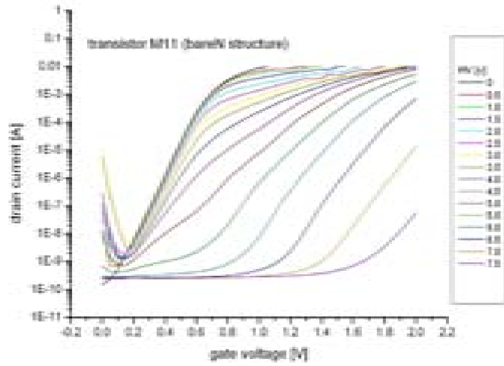


Figure 7.30: I_{ds} versus V_{gs} for different HV applied, for the case of V_{ds}=1.0V for transistor M11.

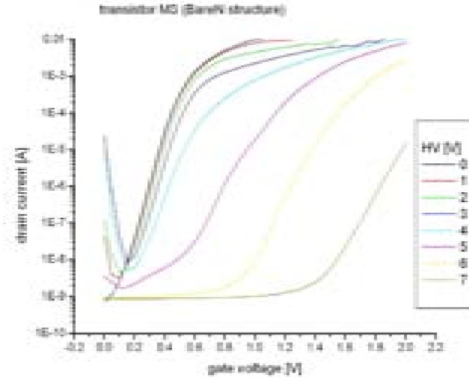


Figure 7.31: I_{ds} *vs* V_{gs} for different HV applied, for the case of V_{ds}=1.0V for transistor M3.

for a fixed V_{ds} = 1.0V. The two transistors analyzed are M3 (high-VT for body float type) and M11 (high-VT for body tie type). These transistors are used to develop the logical circuitry that is included in the design (i.e. flip-flop at the CAP5). As was mentioned in Table 7.3 the threshold voltage expected for this transistor is 0.4V. The results obtained show that the threshold voltage increases with the applied back-gate voltage in both cases: floating body and body tie. For the case of body tie (M11, see Fig. 7.30) the initial $V_{th-HV=0V}$=0.66V increases to a maximum of $V_{th-HV=7.5V}$=1.84V, with and increase of three times the initial value. Attempting to maintain a maximum V_{th} of 1.0V requires a HV value between 4.5V and 5.0V. For values higher than 5.0V the threshold voltage becomes higher than the tolerance voltage given by OKI. The value corresponding to the threshold factor also varies from the 88.14mV/dec at HV=0V that increases to 238.87mV/dec

when the HV applied is 7.5V. For the case of floating body (M3, see Fig. 7.31) initial $V_{th-HV=0V}$=0.54V, achieving a maximum value of $V_{th-HV=7V}$=1.90V. The HV value that gives a V_{th} closer to 1.0V, is between 4.0V and 5.0V. For HV values larger than 5.0V, the threshold value (V_{th}) is higher than the tolerance voltage stated by the manufacturer. The values for the threshold vary between 74.29mV/dec at HV=0V to 142.74mV/dec at HV=5.0V. The threshold values obtained for the body-float transistors are close to the values obtained in [109] with HV=0V, giving a value of 78mV/dec for the NMOS High Threshold voltage transistor.

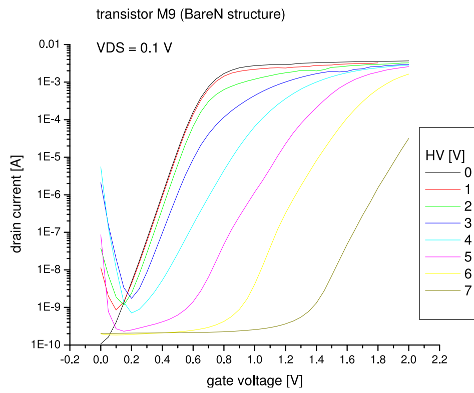


Figure 7.32: I_{ds} versus V_{gs} for different HV applied, for the case of V_{ds}=0.1V for transistor M9.

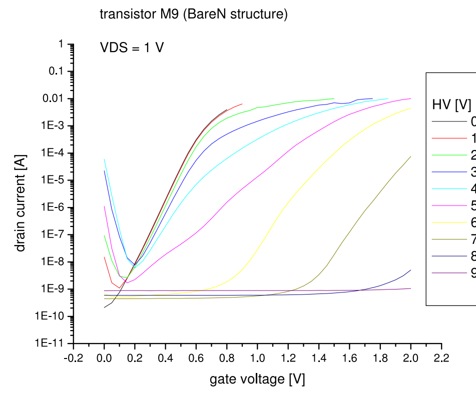


Figure 7.33: I_{ds} versus V_{gs} for different HV applied, for the case of V_{ds}=1.0V for transistor M9.

Backgate for M9 Similar measurements of the I_{ds} were performed for the transistor M9 (body tie high-VT transistor). The measurements performed are shown in Fig. 7.32 and Fig. 7.33. For V_{ds}=0.1V the results obtained show a $V_{th-HV=0V}$=0.56V with a maximum value of $V_{th-HV=7V}$=1.90V. A HV value between 4.0V and 5.0V gives a threshold voltage approximately equal to 1.0V. The threshold favtor varies from 92mV at HV=0V to 136mV for an HV=7.0V. In the case of V_{ds}=1.0V, the results obtained are a $V_{th-HV=0V}$=0.641V with a maximum value of $V_{th-HV=7V}$=1.810V. The HV value that is closer to 1.0V, which is the voltage tolerance for these transistors, is between 4.0V and 5.0V. The value corresponding to the threshold factor also varies from the 98.79mV/dec at HV=0V that increases to 139.09mV/dec when the HV applied is 7.0V.

A comparison between the results obtained between M9 and M11, allows us to compare how valid are the results obtained for V_{ds}=1.0V. The measurements obtained for M9 at V_{ds}=0.1V give a threshold of 0.56V for HV=0V, with a $\Delta V_{ds=1V}$=14.5%. For the case of M11, this $\Delta V_{ds=1V}$ value becomes 17.9% and the case of M3 yields $\Delta V_{ds=1V}$ = 3.6%. With HV=7V, the results for M9 presents a $\Delta V_{ds} = 1V$=4.7V, a M11 $\Delta V_{ds=1V}$=0.1% and M3 $\Delta V_{ds=1V}$=3.6%. The analysis of the threshold factor shows that the $\Delta S_{ds=1V}$=7.4%, this value becomes for the case of M11 $\Delta S_{ds=1V}$=4.2% and it becomes for M3 $\Delta S_{ds=1V}$=24.8. Considering the case of HV=7V, the results are the following, a $\Delta S_{ds=1V}$=2.2%, the comparison of M11 $\Delta S_{ds=1V}$=75.7%, and for M3 the value is $\Delta S_{ds=1V}$=2.6%. In this case, the values found are much higher than the ones presented at [109], where errors are $\Delta S_{ds=1.0V}$=26.9% for High threshold voltage transistor when HV=0.

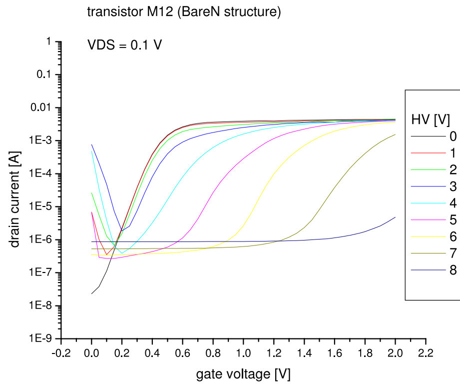


Figure 7.34: I_{ds} versus V_{gs} for different HV applied, for the case of V_{ds}=0.1V for transistor M12

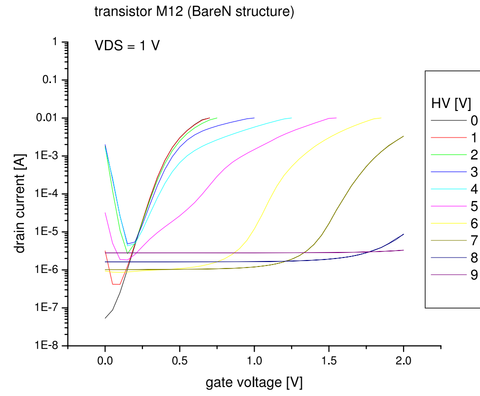


Figure 7.35: I_{ds} versus V_{gs} for different HV applied, for the case of V_{ds}=1.0V for transistor M12.

Backgate for M12 The next measurements performed were to characterize the M12 transistor (corresponding to low-VT body tie type). The measurements performed are shown in Fig. 7.34 and Fig. 7.35. For V_{ds}=0.1V the results obtained show a $V_{th-HV=0V}$=0.35V with a maximum value of $V_{th-HV=7V}$=1.70V. The HV value that is closer to 1.0V, which is the voltage tolerance for these transistors, is between 5.0V and 6.0V. The value corresponding to the threshold factor also varies from the 106.25mV/dec at HV=0V that increases to 218.90mV/dec when the HV applied is 7.0V. In the case of V_{ds}=1.0V, the results obtained are a $V_{th-HV=0V}$=0.37V with a maximum value of $V_{th-HV=7V}$=1.65V. The HV value

that is closer to 1.0V, which is the voltage tolerance for these transistors, is between 5.0V and 6.0V. The value corresponding to the threshold factor also varies from the 119.51mV/dec at HV=0V that increases to 208.27mV/dec when the HV applied is 7.0V. In this case, the values found are much higher than the ones presented at [109], where errors are $\Delta S_{ds=1.0V}$=45.5% for High threshold voltage transistor when HV=0.

The results obtained are very discouraging. As can be seen in both Figures 7.34 and 7.35 the values for both threshold voltage and factor changes dramatically when applying a backgate voltage. On top of that, it was found that some of the initial measurement. The high I_{ds} was solved by taking slow measurements, with each point taking 6 seconds to measure. Such a long readout time clearly impractical for a real system.

7.4 CAP5 test results

The fifth-generation CAP prototype has been fabricated in the OKI SOI 0.15 μm technology, and is targeted for the vertex detector of a Super-B factory. It uses a *Low Voltage (LV) CMOS Binary* architecture, based on a novel approach also employed in the fourth generation CAP device. This scheme provides binary readout in a space-time correlated manner that removes ambiguities otherwise present in continuous rolling acquisition. This readout approach provides higher readout speed and decreases problems associated with highly capacitive bus lines encountered in previous CAP versions.

This most recent generation of the CAP family is the evolution towards a binary readout design. The idea of using a Wilkinson readout with multi-pipelines per pixel have been explored in the previous CAP versions. CAP4 represented a breaking point in order to evaluate new possibilities to address the problem of highly capacitive bus lines and low transfer data rates. In CAP4, an improved Wilkinson readout was developed and a new architecture was proposed. The architecture proposed is a *Binary* architecture. The main disadvantage of this Binary readout is the technology used, because the architecture forced the use of PMOS as well as NMOS. AMS 0.35μm opto technology was used for the CAP4 design.

Calculations of charge deposition for SOI OKI chip using IR Laser Due to area and submission limitations, CAP5 includes a second detector prototype that is discussed in Section 7.5. The main difference between the sensor prototypes are the primary applications. The binary sensor has been designed for the Belle experiment upgrade while the X-Ray detector has been designed for the development of a gamma-ray telescope.

The calculations performed on the CAP5 chip are very similar to those carried out on CAP4. One difference is the dimensions of the pixels. CAP5 binary has a pixel area of 28.7×32μ with an opening to the diode contact of 5.4×5.4μm, giving a total area of 29μm^2. The X-Ray has a pixel area of 200×200μm with an open area of 100×100μm, giving a total area of 40,000μm^2. These area values are affected by a reduction correction factor of 5 due to the presence of a metal layer over the electrode area.

The Setup used for the testing includes an IR Laser ($\lambda_{Wavelength}$=980nm, P$_{in}$=0.250μW with a beam diameter of 0.5mm (Area=2.356 10-7m with a magnification of 1.2, with an energy of E=1.265eV). These factors lead to the number of incident photons of 1.21 10$^{12}\gamma/s$. Due to the beam size, the laser will hit 252.6 pixels for the case of the CAP5 prototype, and 5.89 pixels for the case of the X-Ray prototype.

When using the 980nm laser diode, the laser will be absorbed in the depletion layer. The pixel detector is formed over a 350μm n substrate with a doping concentration of N$_D$=6 10^{12}cm^{-3}, the p implant that creates the diode has a doping concentration of N$_A$=5 10^{15}cm^{-3}. The calculations for the built-in potentials is:

$$\Psi_o = V_T ln \frac{N_A N_D}{n_i^2} = 249.45mV \tag{7.4.1}$$

The built-in potential is then used to calculate the width of the depletion layer:

$$W_2 \approx \sqrt{\frac{2\varepsilon(\Psi_o + V_R)}{qN_D(1 + \frac{N_A}{N_D})}} = 47.11\mu m \tag{7.4.2}$$

For a laser pulse of 10μs, the number of photons reaching the top surface of the detector will be 9500γ for the binary detector and 41 10$^3\gamma$ for the X-Ray detector.

Calculations of per-pixel capacitance and noise values for CAP5 The number of electron-holes generated by the incident photons depends on the silicon characteristics. Considering frontside illumination with electron-holes generated in the depletion area of the junction, the absorption of the photons becomes:

$$I_{DepletionArea} = I_{Incident} e^{-\frac{t_{Depletion}}{LengthAbsorption}} = 0.5165 I_o \tag{7.4.3}$$

$$I_{Aluminium} = I_{Incident} e^{-\frac{t_{BulkSi}}{LengthAbsorption}} = 0.00829 I_o \tag{7.4.4}$$

where Equation 7.4.3 considers the case of the incident photons going through only the depletion zone, Equation 7.4.4 describes the illumination found at the aluminum-bulk junction before relfection. Calculations show less than 1% of the incident light reaches the aluminum layer, therefore reflected light can be neglected in further calculations. The deposited photons is calculated to be 0.4835·Io, which for the binary yields 570γ and for the X-Ray 20000γ, in the case of a laser width of 10μs.

The value of the electrode capacitance, capacitance is calculated for two different situations. In the binary detector the p-n junction capacitance can be neglected since the depletion depth is very large compared to a very small depletion depth capacitance of 0.625aF. The largest contributors to the capacitance are from the metal layers found over the active area and the gate capacitance of the source follower. This yields a C_{ele}=6.87fF[2]. The X-Ray p-n junction capacitance is not negligible however with a value of 21.55fF. For the X-Ray the total capacitance is C_{ele}=53.8fF.

To calculate the voltage variation expected at the electrode node: equation is used:

$$\Delta V_{electrode} = \frac{\Delta Q_{deposited}}{C_{electrode}} \tag{7.4.5}$$

This calcuation performed for the binary detector yields a ΔV of 13.3mV. For the X-Ray detector the ΔV becomes 59.5mV. The noise at the electodes are expected to be $v_{noise-CAP5}$=0.773mV and $v_{noise-X-Ray}$=0.277mV.

[2] $C_{electrode} = \sum_{i=1}^{5} C_{Mi} + C_{g-sf} + C_{d/s-reset} + C_{junction} \approx \sum_{i=1}^{5} C_{Mi} + C_{g-sf} + C_{d/s-reset} = 6.87fF$

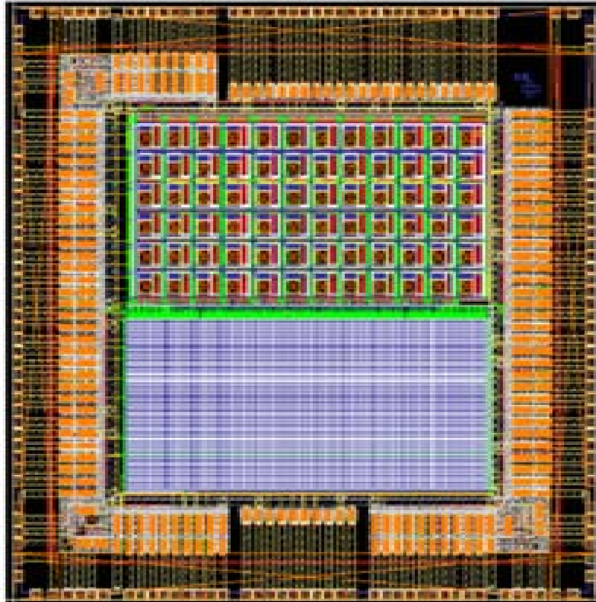


Figure 7.36: General Layout submitted for fabrication using process OKI 0.15μm.

7.4.1 CAP5 OKI chip submission

The general layout characteristics of the CAP5 chip are summarised in this section. The external dimensions correspond to 5000×5000 μm. Each pad separation distance is 100μm and the total area needed for the pad input/output circuitry circuitry corresponds to 800μm^2. The active area used for the detector is 4200×4200μm. The guard ring dimensions, which occuply a large portion of the area, correspond to the dimensions seen in Figure 7.37. As can be seen there a substrate type n is assumed.

The architecture used in CAP5 is based on the generation of a **Binary Hit** signal that is transferred from pixel to pixel until it is buffered out of the chip (in both directions, right/left). Every pixel uses a 3T structure to read the voltage at the electrode. The output of the 3T is buffered through a source-follower and compared to a threshold voltage. If the threshold voltage is passed by the 3T value, a logic '1' is generated and considered a Hit signal. That hit signal will be OR'ed with the previous period's clock information from the contiguous left/right pixel(see Fig 7.38).

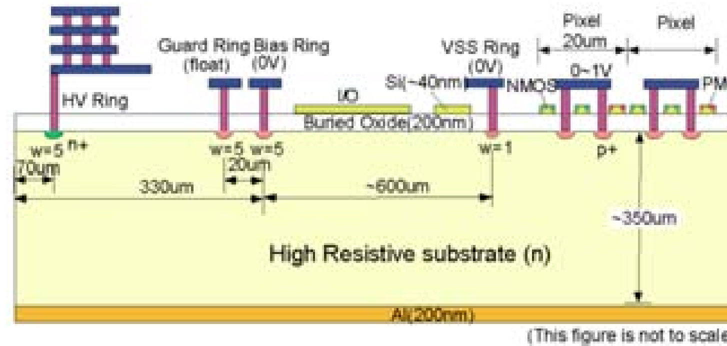


Figure 7.37: Dimension schematic corresponding to the Guard Ring present in the SOI chip.

The main characteristics of of the binary detector are a pixel size of $28.7\times32.5\mu m$ organized into 108 columns and 44 rows. Compared to previous CAP designs, there are less input and outputs due to pad count limitations. Instead of multiplexing rows as was done in CAP4, rows are interconnected, creating longer rows. A connection between rows has been the way of decreasing the number of rows. The design connects 5 rows together which dereases the number of outputs from 2×40 to only 2×4, with interconnected rows having a total of 540 pixels. This leaves 4 rows with 108 pixels each, not connected together. These unconnected rows allow for testing of the readout.

Whereas connecting rows helps with the layout and pad limitations, post-processing of the data becomes more difficult due to the larger row size. The first images of the chip are Fig. 7.39 and Fig. 7.40.

7.4.2 Simulations for CAP5 binary

3T Structure and cut-off current for PMOS and NMOS transistors The 3T structure has been slightly modified (Fig. 7.41) in order to compensate for the cut-off current of the NMOS transistors once a reset has been completed. The presence of a diode will be used as a current discharger in case the current injected from the pixel electrode is too large, such as $V_{BackGate}$ set too large. Simulations

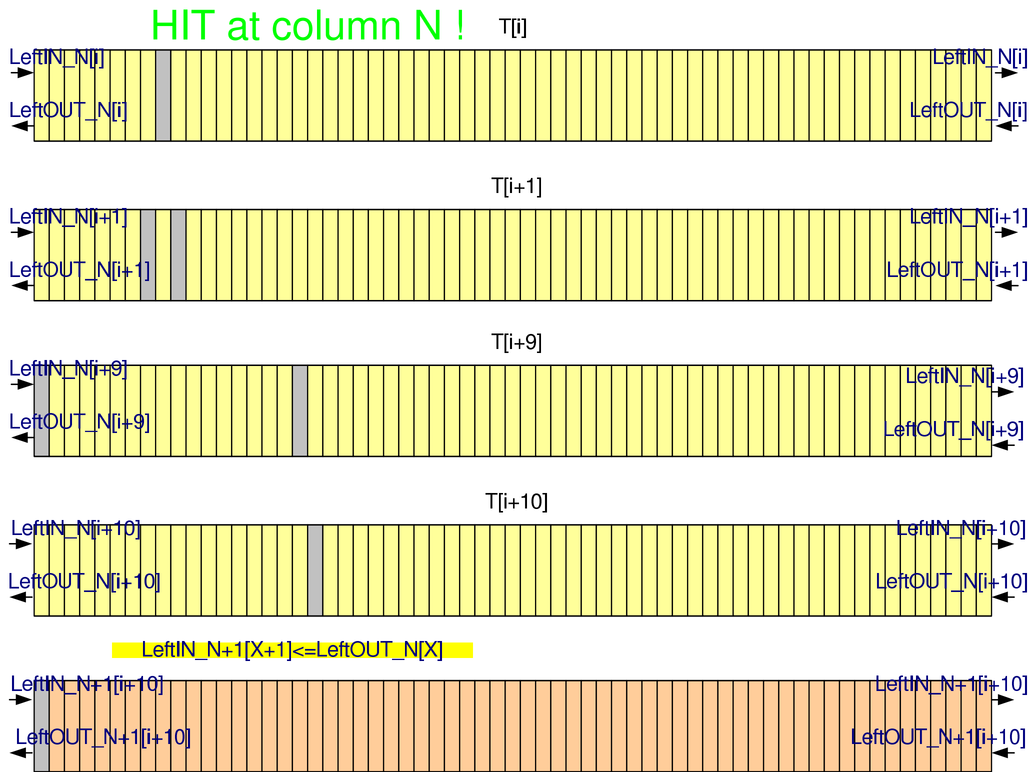


Figure 7.38: Example of Hit signal transmission through the pixel detector.

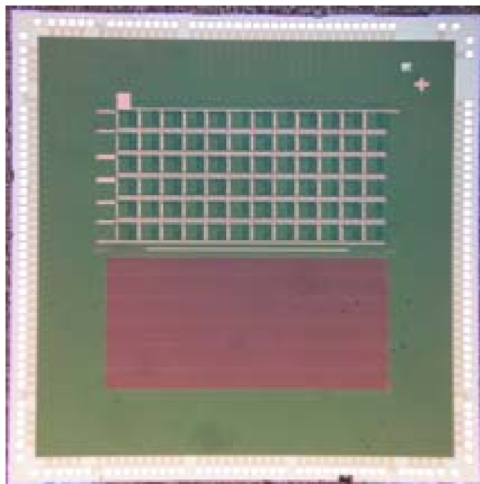


Figure 7.39: General micrograph of the SOI chip.

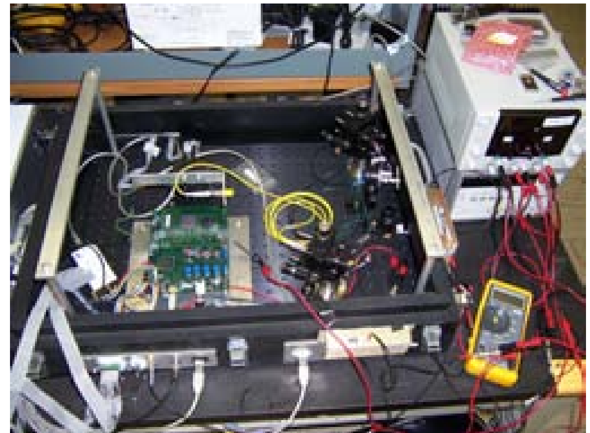


Figure 7.40: General photograph of the SOI chip setup.

of this simple structure show what are the levels of leakage current acceptable for the 3T structure. Fig. 7.42 shows the result of the simulation for a leakage current from 1fA to 100fA. This leakage current level becomes unacceptably high for 10pA.

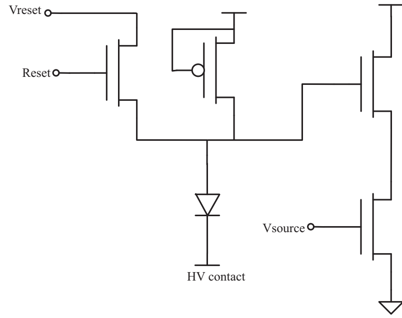


Figure 7.41: Modified 3T transistor structure used in CAP5.

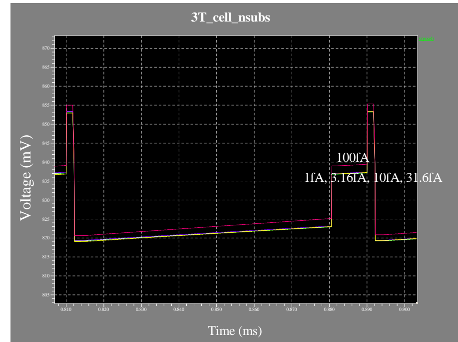


Figure 7.42: Simulation of the electrode at different leakage current.

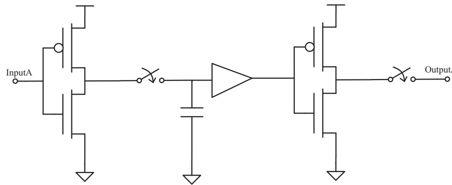


Figure 7.43: Schematic for the Transfer Cell.

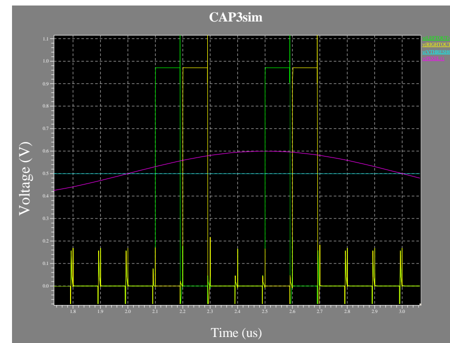


Figure 7.44: 6 Cell Tanner schematic simulation. The input signals compared here are the pink signal (as the $V_{electrode}$) and the blue signal (as the $V_{threshold}$). The output signals are green signal (which is the left signal from Fig. 7.45) and the yellow (which is the right signal from Fig. 7.45).

At this level the pixel becomes saturated, achieving voltage levels higher than the 1V supply voltage of the chip. At the level of leakage just mentioned, the pixel will not work and will not provide any useful information.

Transfer Cell The transfer cell is composed of two identical input/output switches, a capacitor, and a buffer (Fig. 7.43). The capacitance used to store and afterwards, transfer, is the one formed by a transistor used as a capacitor and the input capacitance of the buffer. The buffer is W/L=2/0.3 for the PMOS and NMOS, and the capacitor is formed by an W/L=5/1 NMOS transistor, giving a total capacitance of 15.43 fF.

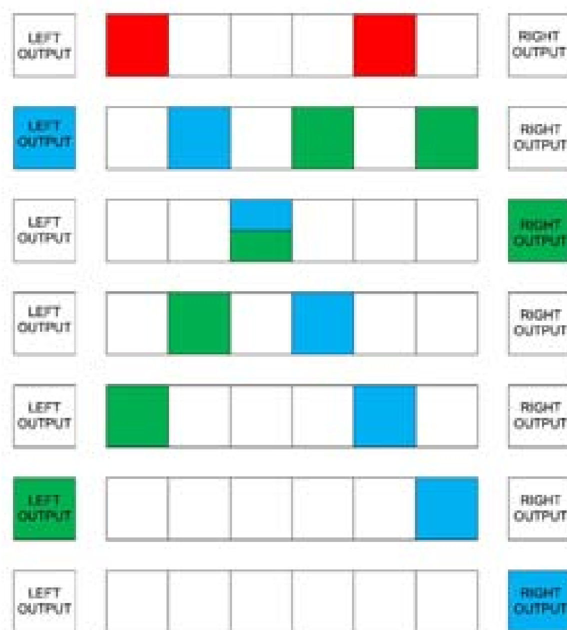


Figure 7.45: 6 Cell schematic simulation.

Simulation of 6 cells The signal used for the shifting and transfer is 10MHz, which was the speed used for CAP4. The output load used for both RightOut and LeftOut is 300KΩ. The simulation schematic found in Fig. 7.45 correspond to the real simulation performed with T-Spice, part of the Tanner Tools design suite. The simulations have been done with 6 complete pixels, the signals have been generated individually in two of them and the output obtained here, correspond to the results of Fig. 7.44. This image shows the two outputs (yellow and green) corresponding to the left and right output, correspondly, and the pattern shown at Fig. 7.45 can be found at Fig. 7.44.

7.4.3 CAP5 testing

Testing of the binary detector on the readout boards was unsuccessful. All binary outputs were observed either high or low (in more cases high than low) but constant and not changing regardless of the settings for all operating parameters such as reset, threshold, current supply for source follower or comparator. To test basic features of the pixel architecture several chips were mounted on packages with only the essential signals and powers bonded out to the test pads on the package. Four probes connected to a probe station were used to measure test outputs after the 3T cell and after the comparator and to provide thresholds and current sources. All other necessary grounds and powers were supplied via cables soldered to the package.

Leakage Current Measurements Leakage current measurements were performed in two different implant chips, where the different implant conditions correspond to the substrate.

The n-type parameters of the standard implant are: use of phosphorus, with an energy of 25keV and a dose of $5{\cdot}10^{15}$cm^{-2}. The p-type parameters are: use of boron fluoride (BF_2), with an energy of 40keV and a dose of $4{\cdot}10^{15}$cm^{-2}. The n-type parameters of the high-energy implant are: use of phosphorus, with an energy of 70keV and a dose of $5{\cdot}10^{15}$cm^{-2}. The p-type parameters are: use of boron , with an energy of 40keV and a dose of $4{\cdot}10^{15}$cm^{-2}. The measurement were carried out on a probe station on bare chip with only High Voltage (HV) contacts connected and the different implants show different breakdown behavior (see Fig. 7.46).

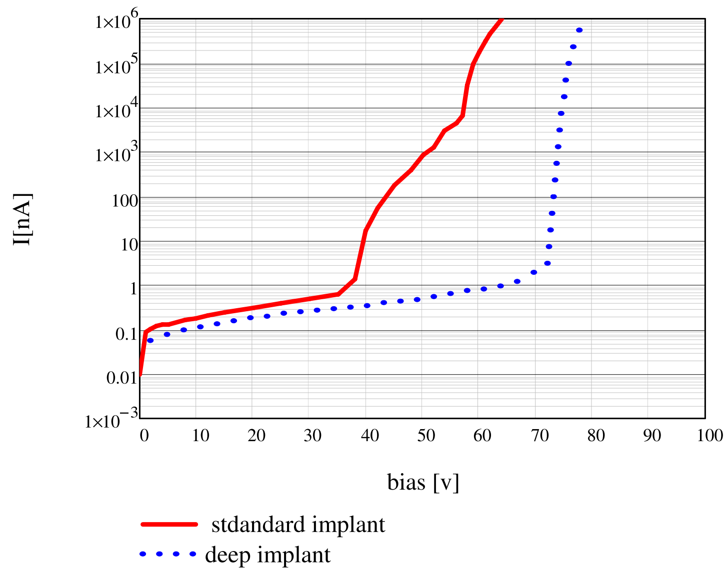


Figure 7.46: Leakage current measurement comparison for 2 different implants.

The measurements of the leakage current present problems because the values obtained initially for the standard implant were higher than expected. The initial measurement are based on the measurement for the High Voltage pins (see HV Ring and HV Bias (or HV Ground) Fig. 7.37). These pins are located on each corner, for ground and the HV connection, and also using the back HV connection. The initial measurements were performed using a COBI board and grounding the LV power lines, that supply the I/O pad ring. This measurement showed the leakage current as being too high ((see Fig. 7.47). After more examination, it was determined the leakage was due to measuring additional pixel leakage current and coupling between the HV ground and LV ground. After this initial measurements, more detailed measurements were performed (see Fig. 7.48) to determine the best leakage current.

Fig. 7.48 shows the results of leakage measurements for case I, the bare die is measured with the HV connected (the lowest value possible). Case II measures the bare die with all the possible supply pins connected to the corresponding values (1.8V and 1.0V). This case shows an increase of one order of magnitude with respect the just the HV connected. Case III is using the board for the same measurement but isolating the LV ground and providing this value with a separate pin that is not

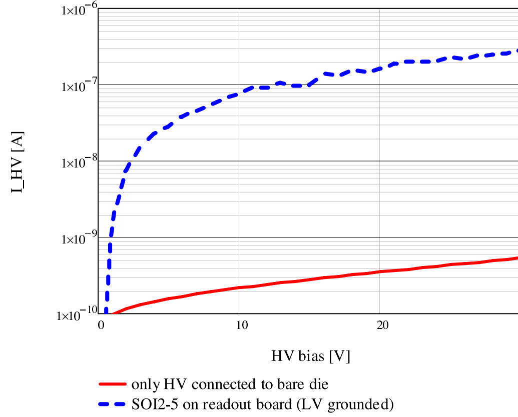


Figure 7.47: Measurement for the leakage current for the standard implant attaching the LV to ground or floating.

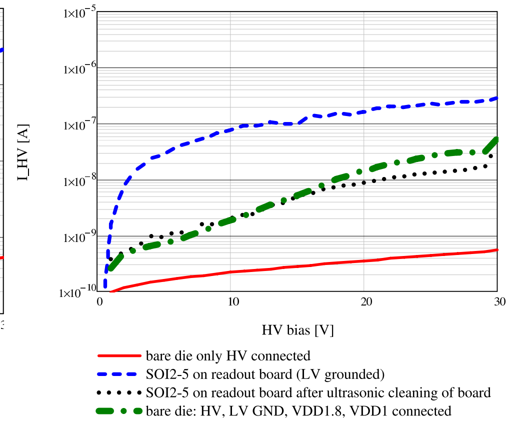


Figure 7.48: Measurement for the leakage current for the standard implant for different conditions.

going through the board[3] , this value is almost the same than the one using just the bare die and everything connected. Case IV measurement is done using the board but grounding the LV with the pins provided by the board. This last case shows that there is an increase of 2 orders of magnitude with respect the first initial value.

The measurements presented here show the initial idea of coupling is not responsible, as the COBI board has been done correctly. The board was still presenting a coupling problem that would increase the leakage, as seen in case III, but the major problem of coupling is overcome by applying the HV ground by a separate path. The initial measurements were done in the case IV situation and the leakage was too high to be able to obtain any valid measurement. The expected leakage current at the pixel level was 5 orders of magnitude less than the tested, and presented, values. The leakage currents presented correspond to the total chip current. This area includes the HV guard ring, the diodes of X-ray detector part and the diodes of the CAP5 part[4].

Testing of the 3T cell The next aspect to analyze was the 3T cell functionality. The signal $V_{AfterPixel}$ was obtained from a test output immediately after the source follower. This measurement was done for one pixel that was used

[3]the board has been cleaned using a ultrasonic bath to discard the presence of any flux

[4]Total leakage current should be multiplied by 3.3 10^{-5} to get an estimate for the current on a single pixel

as a test structure.

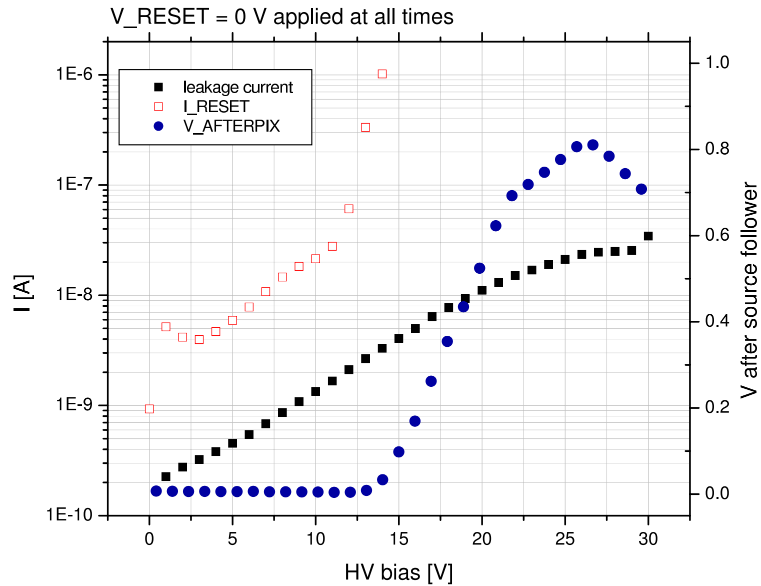


Figure 7.49: $V_{AfterPixel}$ after the source follower goes high for HV>13 V regardless of the constant reset.

Fig. 7.49 shows the current as a function of HV obtained from the 3T structrure present in the test pixel. There is a constant reset voltage applied (0V) and the measurements performed correspond to the leakage current for this case and the voltage at the source-follower. It shows that the leakage current increases in an almost linear way for a logarithmic scale, going from the initial 0.2·nA to the final 20nA for the highest HV of 30V. The output voltage shows that for a HV >13V the output of the structure is saturated and the output goes to the max voltage level of the chip. The fact that the reset would have to be done too fast to reset the complete chip forces the highest level of HV applied to be less than 13V.

Transfer curve of the source follower The next measurement was obtained at a HV of 2 V, and was the transfer curve of the source follower. Fig. 7.50 shows the voltage at the source-follower when the reset voltage level was swept from 0 to 1 V . Fig. 7.50 shows that the 3T cell correctly transfers the V_{reset}. Fig. 7.51 shows the signal after the source-follower for a slow pulsed reset. Considering these results, the estimated input capacitance obtained from the leakage current (300 pA) provides a $C_{pixel} \sim 0.3$ fF

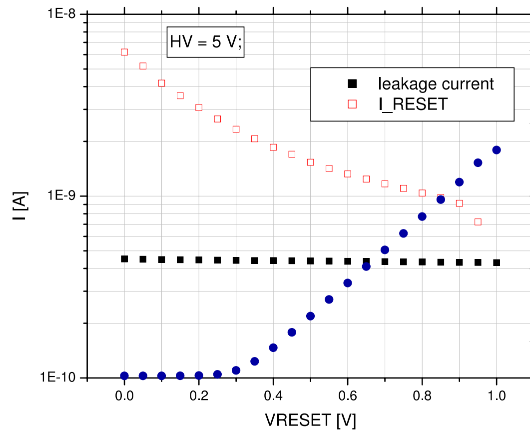


Figure 7.50: $V_{AfterPixel}$ after the source follower with a sweep over reset level.

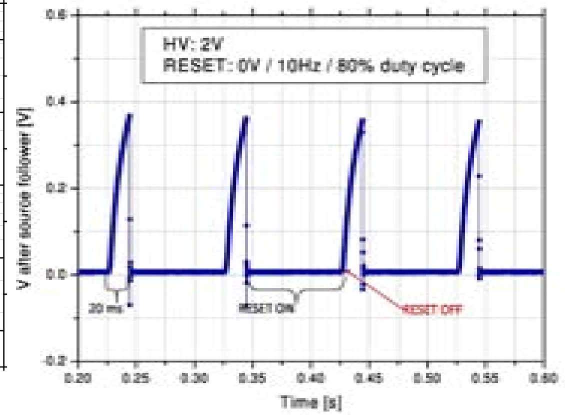


Figure 7.51: Signal after source follower for a slow pulsed reset.

Test of 3T cell and comparator The next test show the signal after the 3T as well as the signal after the comparator, for a pulsed reset. The chosen reset frequency was 1 Hz. HV was tied to VDD 1.8 V. Fig. 7.52 shows that the signal after the 3T cell (= the input of the comparator) goes from 0 to 600mV whenever the reset was not applied. The test output after the comparator did not follow, it stayed low at a few mV at all times. This behavior did not change for different values of the comparator threshold or current source, neither for different applied HV values. The current drawn from the comparator current source (ICOMP) was found to be rather high. The tests were repeated with a different chip and great care was taken to avoid any systematic sources of leakage currents (i.e. between neighboring bonding pads). The models showed much lower currents for a given voltage applied to the current source.

Fig. 7.52 For a pulsed reset the signal after the 3T cell starts increasing whenever the reset is off. The test signal plotted is found after the comparator output. The behavior was the same for various settings of threshold voltage and comparator current supply. Fig. 7.53 shows another measurement that was done to make sure the problem was not coming from a wrong current source voltage value. Here there are three values plotted, the first one is the current. Initial high power consumption was found and a sweep of the current was done. The complete power consumption was found to go from nearly 0mA at 0.1V to 800mV at 0.7V. Taking both extremes for analysis as the value of the source-follower, it can be seen the

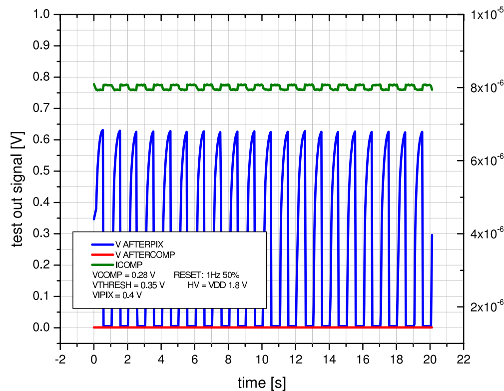


Figure 7.52: Comparator output with a pulsed reset signal of 1 Hz.

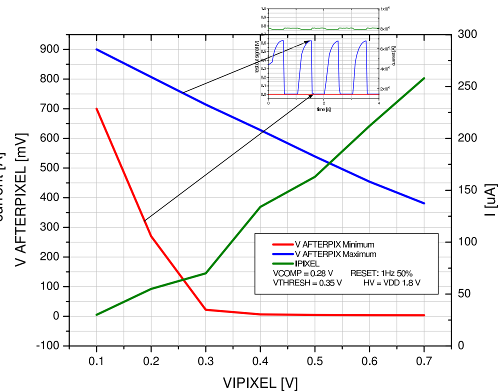


Figure 7.53: Detail of Fig. 7.52 with same conditions.

voltage swings from 400mV to 700mV.

This results, and the simulations show that the models used were not correct. In the operating conditions for the comparator, the signal output of the comparator should be rail-to-rail, instead of what is obtained.

7.5 X-ray telescope

The X-ray and γ-ray bands have been an important window for exploring the energetic universe. In these bands, non-thermal emission, primarily due to accelerated high-energy particles, becomes dominant. The study of the soft X-ray band has been revolutionizing our understanding of the high-energy universe. These studies have focused on the soft X-ray band due to XMM-Newton and Chandra satellites observations. However, the instrument experimental sensitivities for the hard X-ray band are low and have not been dramatically improved in the last decade. The improved sensibility for this hard X-ray can stimulate further understanding of our universe.

Polarization measurements are used to study particle acceleration mechanisms in supernovae remnants, pulsars and black holes. The main processes of photon creation are synchrotron radiation, Compton scattering and bremsstrahlung and they produce distinct photon polarization features. An imaging polarimeter enables detailed polarization mapping of these sources of photon emission and allows

the localization of these particle acceleration sites. Furthermore, measurement of polarization features caused by General Relativity effects around Kerr black holes would provide *the definitive proof of the existence of the black hole.*

A hard X-ray Compton polarimeter is based on a Compton telescope. The Compton telescope consists of 2 detectors that measure the scattering angle and energy loss and use these kinematic constraints to reconstruct an image of the sky [110]. The same idea can be used to develop a semiconductor Compton telescope, using a stack of position sensitive detectors made of semiconductor materials. The upper layers work as scatterers and the lower layers work as absorbers. An approach to this telescope can include silicon detectors. To obtain an improved sensitivity a prototype has been developed.

This prototype has been fabricated using a new 0.15μm low voltage SOI technology. The chip has been designed to detect xray and read-out the corresponding analog value corresponding to its energy deposition. This first prototype consists of an array of 16 sensor cells. Due to non-uniformities in fabrication, an independent threshold voltage is tunable for each cell. To control and extract the data obtained, a circuit board and user interface have been developed

7.5.1 Hard X-Ray Sensor Principles

An X-ray is a quantum of electromagnetic radiation with energy that is about 1000 times greater than optical photons. Traditionally, the soft X-ray band is defined as the energy range 0.5-12 keV, the hard X-ray extends to approximately 50 keV and the energy range beyond it to a few MeV is regarded as soft gamma rays, although this classification is not strict. High-energy physics and astronomy study this electromagnetic spectrum.

The fundamental physical mechanisms which can give rise to high energy emissions from a thermalised distribution of matter are limited: thermal black body radiation, bremsstrahlung and Compton scattering. However in supernova remnants, non-thermal processes play a key role in high-energy emission, apart from bremsstrahlung, Compton scattering and synchrotron emission. This non-thermal emission is best observed in accreting black holes and neutron star systems [111].

A more detailed explanation about the sources of these non-thermal emissions and questions regarding these mechanisms are found in [112]. A comparison of soft X-ray sensitivity with the hard X-ray and γ-ray sensitivities shows the existence of a gap for these energy bands. The so-called *sensitivity gap* [113] between 10 keV and 100 MeV includes the non-thermal emission, mostly due to accelerated high-energy particles.

7.5.2 X-Ray Telescope Background

The Imaging Hard X-Ray Compton Polarimeter (IHXCP) will consist of a hard X-ray mirror and a focal plane detector. The basic IHXCP focal plane detector module's design is based on a Compton kinematics telescope [110], [114] . The hybrid design of this module, illustrated in Fig. 7.54, incorporates both silicon detectors and pixelated CdTe detectors. The silicon layers are required to cause at least one Compton scattering before a photo-absorption and also improves the angular resolution because of the smaller effect of the finite momentum of the Compton-scattering electrons (Doppler broadening) than CdTe (see Fig. 7.55). The Compton telescope consists of 10∼20 layers of silicon detectors (double-sided silicon strip detectors or silicon monolithic pixel detectors) and 2 layers of thin CdTe pixelated detectors surrounded by 5 mm thick CdTe pixelated detectors. The telescope is surrounded by a BGO ($Bi_4Ge_3O_{12}$) shield units to reject backgrounds. The width of silicon strip or pixel depends on the requirement on the point spread function of the X-ray mirror. For a typical hard X-ray mirror, 0.5 arcminutes or better can be expected. It is required each IHXCP event to interact twice in the stacked detector, once by Compton scattering in the Si or thin CdTe part, and then by photo-absorption in the CdTe part. Once the locations and energies of the two interactions are measured as shown in Fig. 7.54, the Compton kinematics allows us to calculate the angle between the telescope axis and the incident direction of the event using the next Equation

$$cos\theta = 1 + \frac{m_e c^2}{E_2 + E_1} - \frac{m_e c^2}{E_2} \tag{7.5.1}$$

where θ is the polar angle of the Compton scattering, and E_1 and E_2 are the energy deposited in each photon interaction. The direction of the incident photon can be confined to be on the surface of a cone determined from θ and the two interaction positions. The fine energy resolution of the Si and CdTe devices help reduce the width of these *Compton rings*. We can determine the location of point

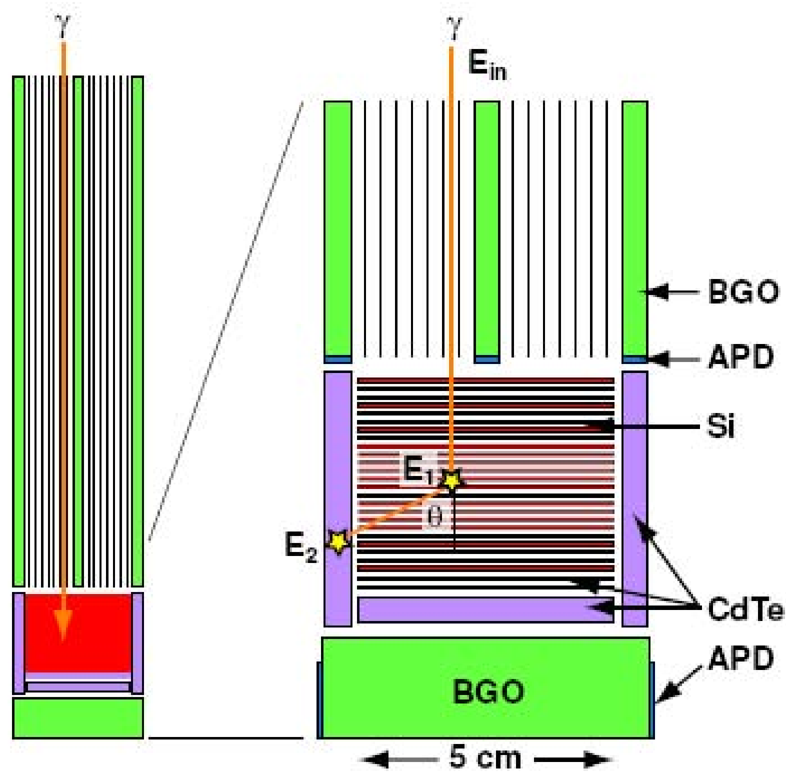


Figure 7.54: The Imaging Hard X-ray Compton Polarimeter (IHXCP) concept.

sources as intersections of multiple rings. The angular resolution is limited to $\sim 8^o$ at 100 keV due to the finite momentum of the Compton-scattering electrons, which is comparable to the FOV of the BGO collimators. Although the order of the events can be uncertain, we can use the relation that the energy deposition by Compton scattering is always smaller than that of the photo absorption for energies below E_γ = 256 keV (E_γ= $mec^2/2$). The polarization can be measured by an azimuth scattering angle distribution as shown in Fig. 7.56.

In order to maximize the energy resolution, a low noise pixel sensor is a natural choice. It is also the desire to minimize the power and to provide a low-noise, data-driven measurement of the Compton energy deposition.

7.5.3 General Characteristics of SOI X-ray

The area used for the SOI X-Ray detector corresponds to 3250×1500 μm^2. The pixel architecture used here corresponds to the same used in Figure 7.57. This option has been chosen because of the advantages that can be found by using SOI technology.

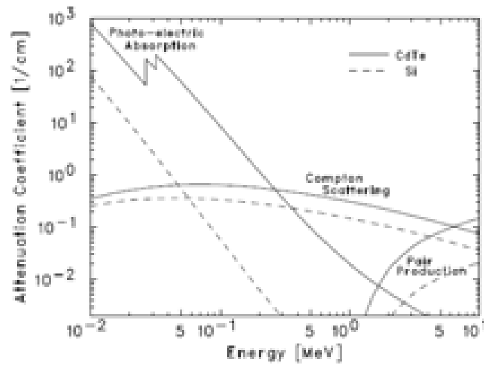


Figure 7.55: Linear attenuation coefficients for photo-electric absorption, Compton scattering and pair production in Si and CdTe. [115]

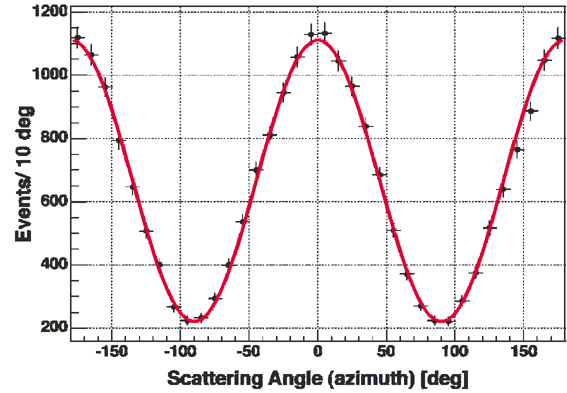


Figure 7.56: An example of polarization determination as a function of scattering angle.

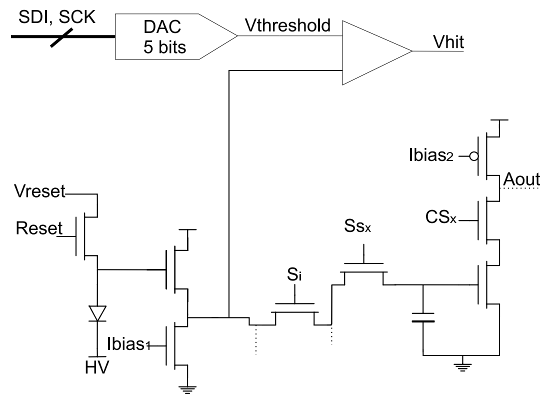


Figure 7.57: Schematic of the n-type substrate sensor architecture.

The SOI X-Ray main characteristics are a pixel of $200{\times}200\mu m$, with a spacing between pixels of 50μm and a detector area of $100{\times}100\mu m$, with a number of columns 12 and rows 6. Every pixel presents 8 storage cells, which have been separated in 2, depending on the pre-event storage(depends on S0) or post-event storage (depends on S1). After the event storage stage are four capacitors to store the value if the correspondent SS_i (i from 0 to 3) is activated. The output is done with the signal CS_i (i form 0 to 3).The final value is obtained after a common-source with triode load configuration. The analog output is multiplexed from the initial 32 signals to 6 signals connected to pad. Every pixel has a comparator that generates a $ComparatorR_i$ signal per row (OR-signal of the Hit per every pixel), that will decide to read-out the analog value. Once that this signal is generated, there is

a read-out enable signal, called Rienable (with i from 0 to 5). The Vthreshold that is set at the comparator to generate the hit signal is send through the DataIn data (MSB enters first) like serial data ($5 \times 6 \times 11$ bits total) and goes out like DataOut. An independent DataIn path has been included for the testing structure, called DataTest as input and OUT_i as output. There is a general clock signal used to transfer the information with a frequency of 2.4kHz.

7.5.4 XRAY testing

Each pixel has a 3T structure, 8 storage cells with a common source transistor as an output and a programmable comparator.

3T structure The 3T structure also includes the storage cells and common source output transistor. A pull-up PMOS transistor has been included. The first measurement realized was the measurement of the transfer curve, where one storage cell was always active. To perform this measurement a HV of 3.0 V has been applied. According to the measurement of leakage current, the leakage is on the order of 0.3nA (whole chip, including CAP5). According to simulation, a current of 390 nA was needed at the last pull-up stage. It has been observed that a pull up of 390nA was not sufficient and this value has been increased by one order of magnitude. The results can be seen at Fig. 7.58. An effect of 200mV difference has been observed between the two outputs.

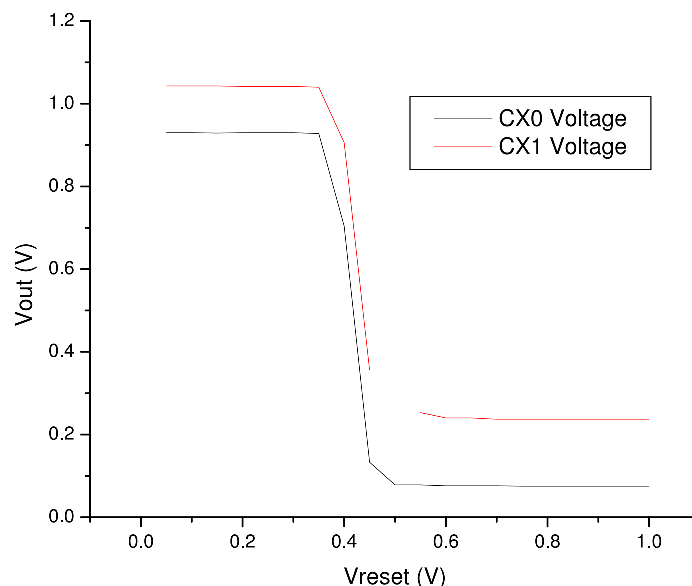


Figure 7.58: Transfer curve obtained for the XRAY testing structure.

Register The Comparator presents a programmable input threshold that is set using a group of registers and a DAC. The registers are used to transfer the bit information from pixel to pixel and once the information has been transferred through all the pixels, the clock is stopped and the information is transferred to the DAC, so the voltage (5 bit precision) can be set at the input. After the basic performance was tested, the registers were analyzed. Initially HV was set to 3.0 V. The idea of this test was to have a clock and an input signal at the input. Once the information is transferred through all the pixel structures the previous incoming data should be outcomming data. Unfortunately, nothing could be seen.

Simulation showed that for a frequency of 10 KHz, the transmission should be happening. After this discouraging results, a few more modifications of the input characteristics of the frequency, as well as the input signal were tried. None of them were positive. The last thing we tried was looking at the dependence of our output on HV. The results were highly surprising. When working at low HV no results were observed at the output, but when increasing it up to 7V the output started coming out. The transfer worked for voltages between 7 and 10 V. See Fig. 7.59, 7.60, 7.61, 7.62, 7.63, 7.64 for the results obtained at the register. First signal is the input signal, second signal is the output register signal and the third signal is the clock used to transfer the data from pixel to pixel.

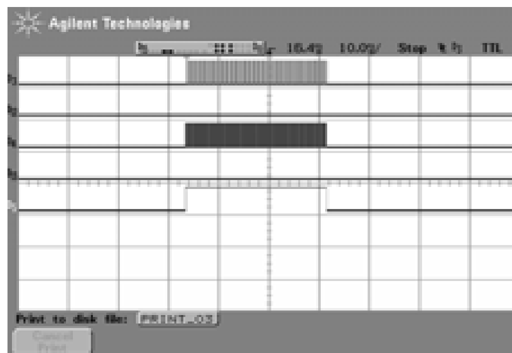


Figure 7.59: Register results for HV=3V.

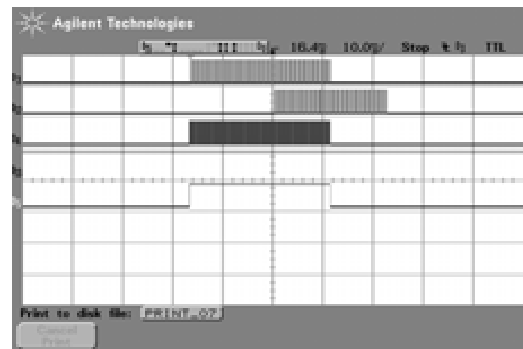


Figure 7.60: Register results for HV=7V.

Comparator After the registers, the comparator was analyzed. To set the voltage at the input of the comparator one of the inputs is provided by the source-follower

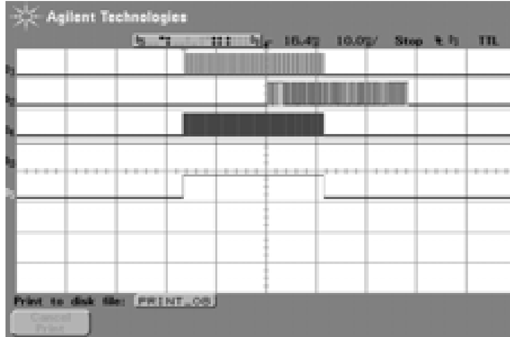


Figure 7.61: Register results for HV=8V.

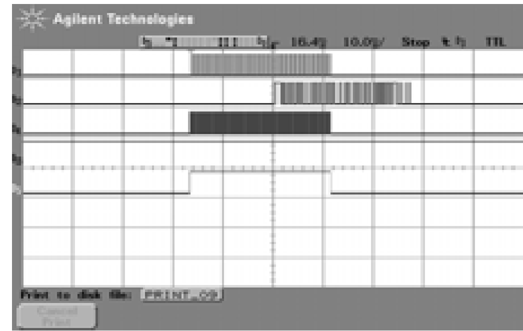


Figure 7.62: Register results for HV=9V.

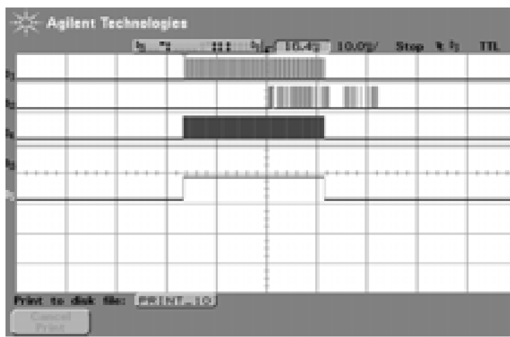


Figure 7.63: Register results for HV=10V.

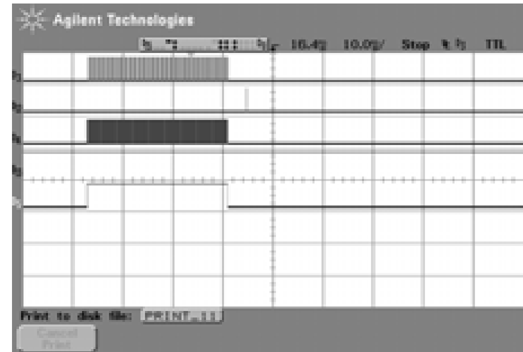


Figure 7.64: Register results for HV=11V.

and the other by the DAC, which is set by the values transferred by the register. To perform this test, the Reset transistor is always turned on and we vary the Vreset (at the drain) to be able to control the voltage at the pixel, as well as the voltage after the source-follower applied to the comparator input. The comparator was designed to work around 0.5 V so any change around this value is detected. The input voltage range used is 0.3 to 0.7 V. Here more troubles were found: The results found show that the comparator works, but not as expected. The DAC (based in resistors) seems not to be working according the simulations. The reason for this is that the comparator seems to be turning on and off but not following the expected threshold value, i.e. the DAC seems not to be setting the correct Vthreshold. The

DAC is not setting the value received from the register. Simulation were simple and straight forward and did not show any similar behavior.

Conclusions The models provided by the manufacturer for the 0.15μm process do not seem to follow the behavior observed in our device. The only fully working structure for the X-Ray prototype is the analog output. The digital reset signal generated by the comparator will probably not be useful. To use the digital comparator, reset and DAC, a HV of 7V has to be applied, which can be affecting the performance of the 3T structure. The DAC, comparator do not seem to present a high dependence on this value, as far as has been tested. The 3T structure shows that the output range shrinks by half when increasing the HV to 7V

Chapter 8

Conclusions

The conclusions of the research work developed in this dissertation have been provided in each chapter. The most important contributions presented are linked to the 3 separate members of the CAP family that have been introduced in great detail in previous chapters. Highlights of these developments of summarized below.

8.1 Contributions to the CAP development

The work presented in this dissertation show the research performed in support of the Belle experiment pixel detector upgrade. The main achievement presented here is the novelty of the pixel architecture explored, even though the experimental results obtained have not been as successful as had been hoped.

CAP3 was developed using well-established technology, provided by TSMC with a feature size of 0.25μm. The pixel architecture used here includes a group of 8 storage cells per pixel. This approach was initially used in CAP2, and provided excellent results. The approach of including these storage cells has not been used before, because of the increase of noise from the continuous sampling and because the output speed did not need to be dramatically increased. The main challenge for this prototype was to see what results could be obtained from a full-size detector prototype. A high-speed measurement set-up was developed. This measurement set-up was based on a laser scanning set-up and a read-out environment, which also had to be upgraded from a previous version (creation of COBI and PETRA board). Results obtained with this CAP3 prototype were encouraging. The laser spot was clearly detected, but many challanges appeared. The output speed obtained with

this chip was too slow since the capacitance on the output bus lines was too high.

After many discussions, there were two main approaches to address these problems. The first one would imply keep analyzing the analog read-out system. This option cannot be considered valid for a detector-size prototype with the architecture implemented before (because of the speed and noise limitations). In order to overcome these problems, an advanced architecture was proposed, a Wilkinson-based architecture. This architecture has two important advantages: the use of a tree output structure to decrease the capacitance at the output nodes and the inclusion of a comparator every few rows that would digitize the signal obtained at pixel level. This first option was called the Wilkinson CAP4 architecture. The results obtained here show that the read-out scheme, as developed contained a design flaw. This mistake made it impossible to read-out the prototype with valid data. The second option evaluated in this CAP4 was a more complex pixel encoding structure. This pixel structure is called binary structure and evaluates the possibility of using a pixel with circuitry that provides detection of a hit based on a general threshold signal. The main characteristic of this approach is the transmission pixel-by-pixel of the signal obtained for both sides, left and right. There were two different pixel layout included in the CAP4 layout. The use of a large number of complex circuits at high frequency (10MHz), decided the main differences of circuitry between the two binary approaches. The first one was called NMOS and the second one CMOS. The main difference was the number of PMOS used. For the NMOS case the number of PMOS was minimized, and specific design techniques were used. The CMOS design would not limit the number of PMOS transistors used in the design. The CMOS Binary showed results based in a read-out speed of 10MHz. This approach proved a very fast approach, which, as far as our group is aware, was never proposed before. The NMOS Binary was not successful, although simulations of the system showed positive results.

CAP5 was the possibility of overcoming the limitation of PMOS transistor that appears in a CMOS with epilayer technology. The usage of a SOI process was available through a collaboration with KEK and OKI. These prototypes were fabricated using the second run of a 0.15μm SOI process. The first run showed very positive results, and very simple 3T architectures with openings between the circuitry and the substrate were used. More complicated circuitry was tested, but it

did not use openings or back gate voltage applied. The pixel that was submitted for this process included the same architectural approach as with CAP4 binary. The inclusion of so much circuitry with the presence of the opening made the variation of threshold voltage depending on back gate voltage become very evident. On top of that the process fabrication did not follow very strict rules and process variations of 50% on the threshold voltage value were accepted by OKI. The results of these spreads led to a chip that was not working properly for any complex circuitry. The basic read-out cell, with a reset transistor and a source-follower was working according to our expectations, but the comparator showed a very poor performance. This chip was used to characterized the transistors and see the real effects of using the openings on the variation of the threshold voltage, results that have not been reported before.

8.2 Future Developments

Development of the CAP has been within the research that takes place in IDLab, at the University of Hawaii at Manoa, under the leadership of Prof. Varner. The last members of the CAP family have been the result of multiple discussions over the best options offered by technology and analog and digital processing for the upgrade that will take place at KEK for the Belle experiment. The experimental results obtained until now do not offer a final solution for the architecture or technology process to be used for a final design of the SVD. These results are guiding the IDLab team to ward the best option to be used in the next prototypes. After the work presented in this dissertation, the next members of the CAP family either are in preparation or have been submitted for fabrication.

A CAP6 prototype will continue evaluation of the Wilkinson architecture. In this approach, a differential pair will be used per pixel, and the time-encoded digital result of the comparison between a threshold voltage and the pixel obtained voltage will the transmitted as a digital signal. This temporal encoding of the voltage signal can be measured directly by an FPGA. This version has been implemented using a regular CMOS process. The main goal with this prototype is to analyze the viability of this design approach for a detector-size prototype. Submission of CAP6 prototype in the 0.35 mm TSMC process will be made in April 2008..

A CAP7 prototype will continue to scrutinize the binary solution using an SOI implementation. The new process used for this submission is slightly different from the 0.15μm process used before; a 0.20μm SOI process of OKI. This process has been developed for several years and has shown great performance. Results for the diode detector structures have, yet, to be analyzed, but the expectations are extremely positive. CAP7 submission in the 0.2 mm SOI OKI process was done in January 2008 with an improved binary solution, correcting the pixel chatter problem.

The IDLab and Prof. Varner also have many other projects in which I had the great opportunity to collaborate. Some of them are officially completed, while others will continue well into the future. As an example, a High Voltage Chip should be mentioned. The CMOS Interface Device for HV (CID HV) is a chip that has been developed using the 0.35μm HV process from AMS. The main purpose of this chip is to provide the appropriate voltage signal translation from the low-voltage logic STARGRASP readout system and the MOTA chip. As a new device, logic monitoring output signals were provided and high-capacitance clock line driving was evaluated. Some additional test structures were included to evaluate future ADC additions for a next version of the chip. This High Voltage Chip was developed and successfully tested in the lab. A new version of this chip, where this digitization circuitry could be integrated directly with the CCD is being studied.

Appendix A

CAP3 Testing Results

A.1 Y Axis Scan

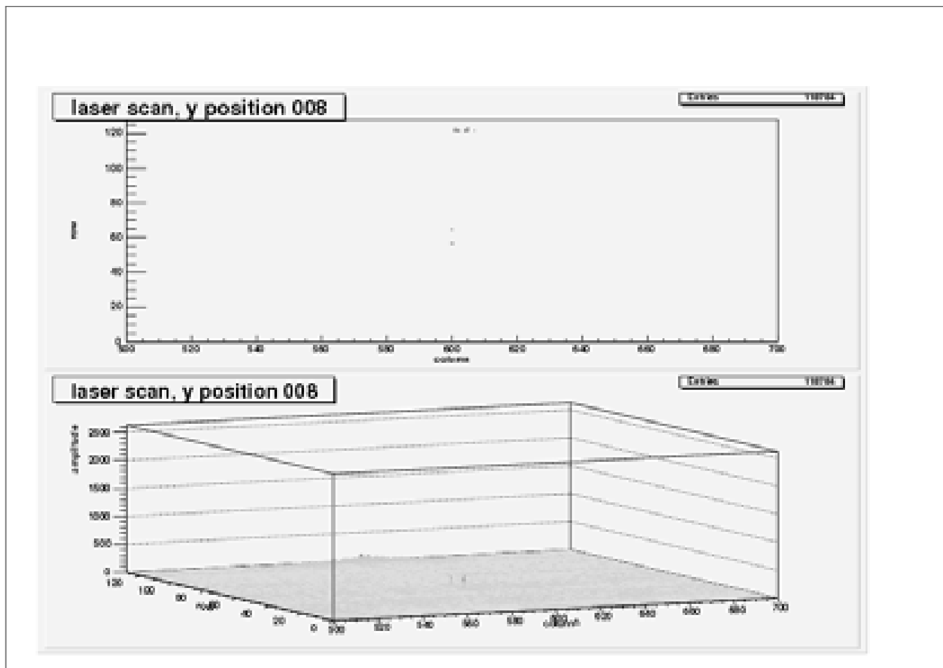


Figure A.1: Pos 008 of y axis scan.

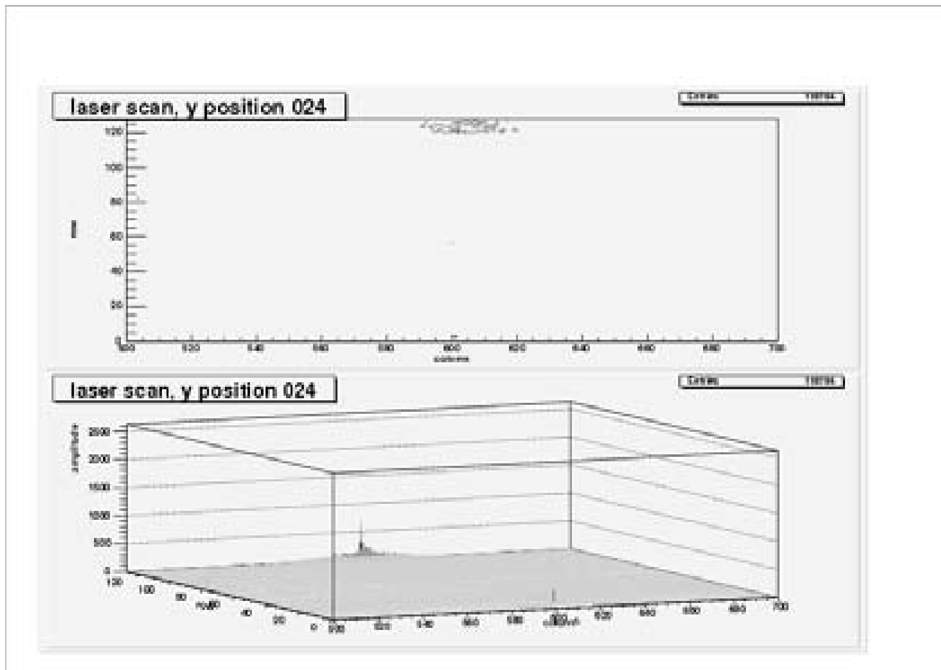


Figure A.2: Pos 024 of y axis scan.

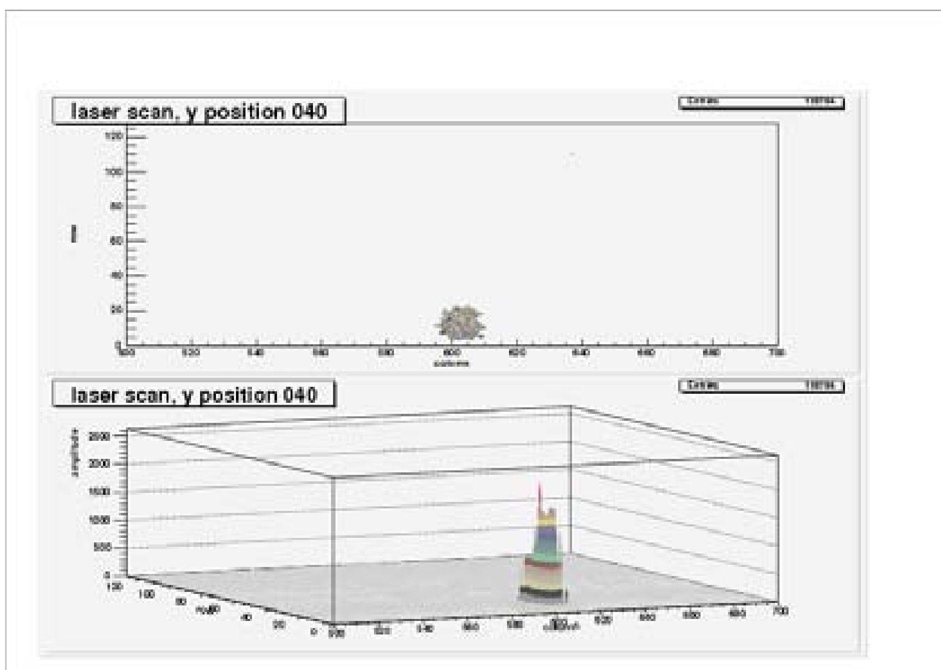


Figure A.3: Pos 000 of y axis scan.

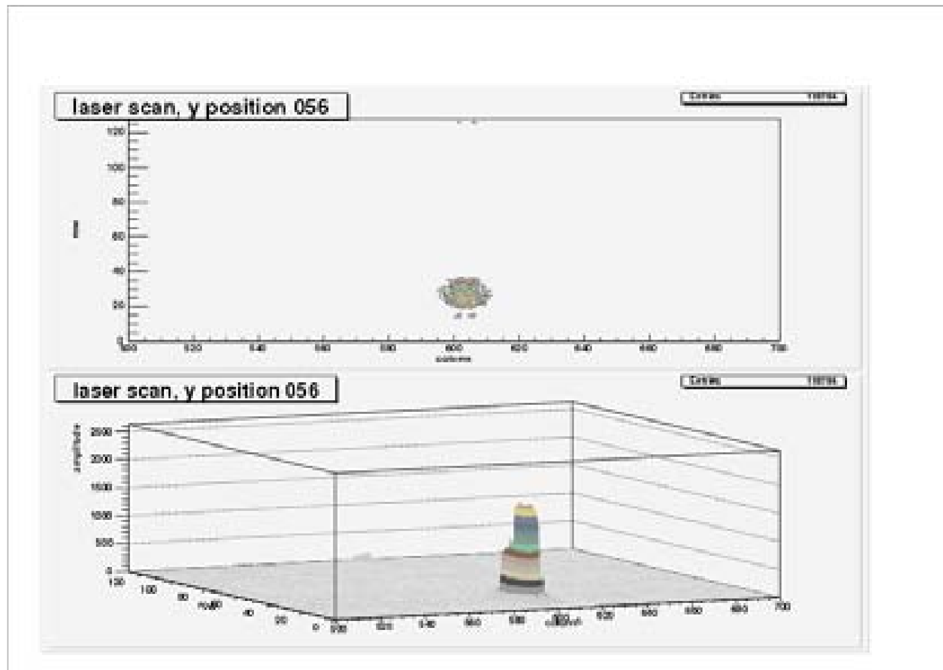


Figure A.4: Pos 056 of y axis scan.

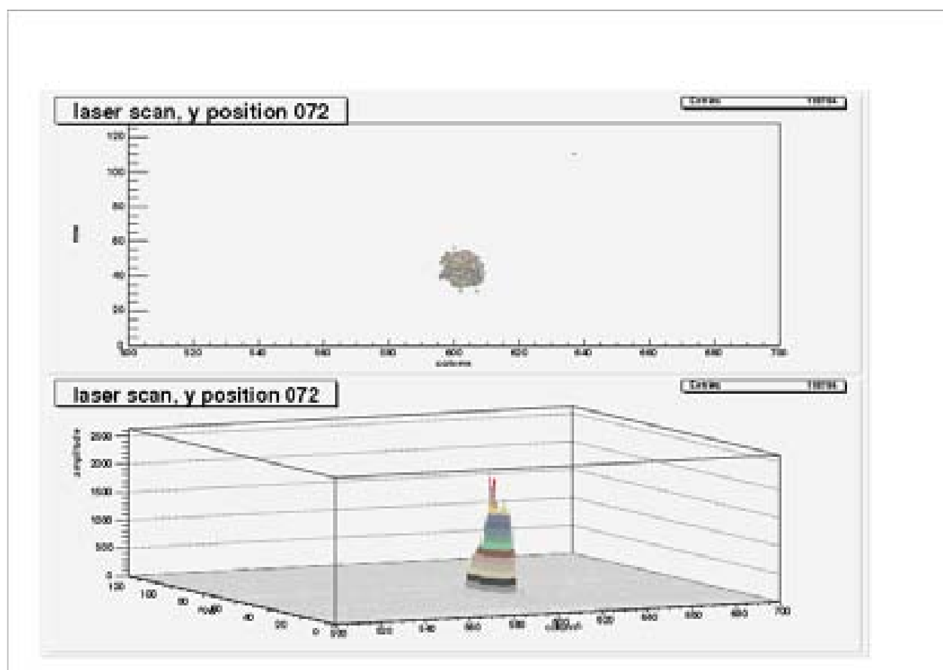


Figure A.5: Pos 072 of y axis scan.

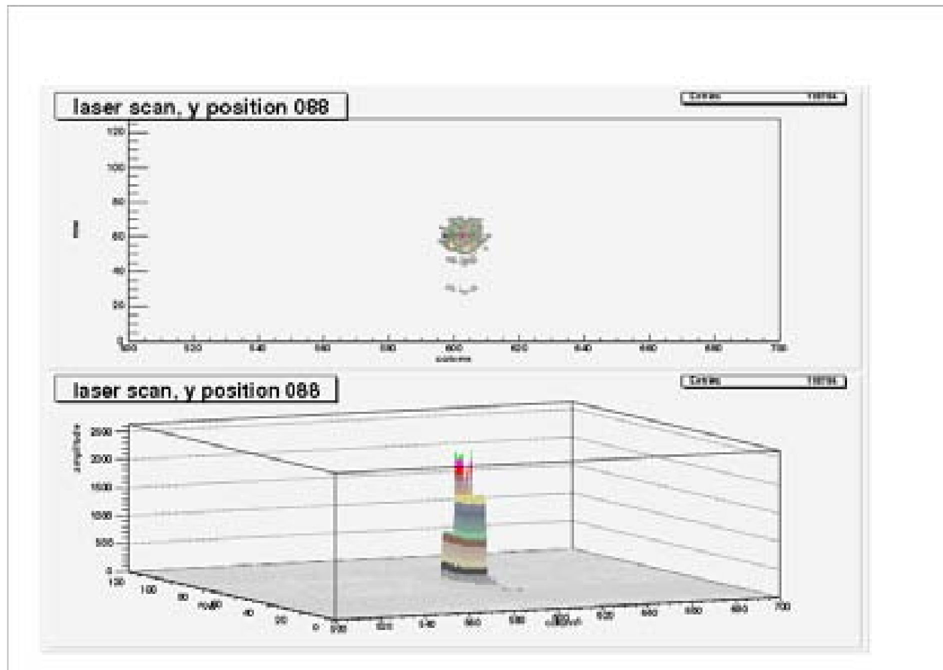


Figure A.6: Pos 088 of y axis scan.

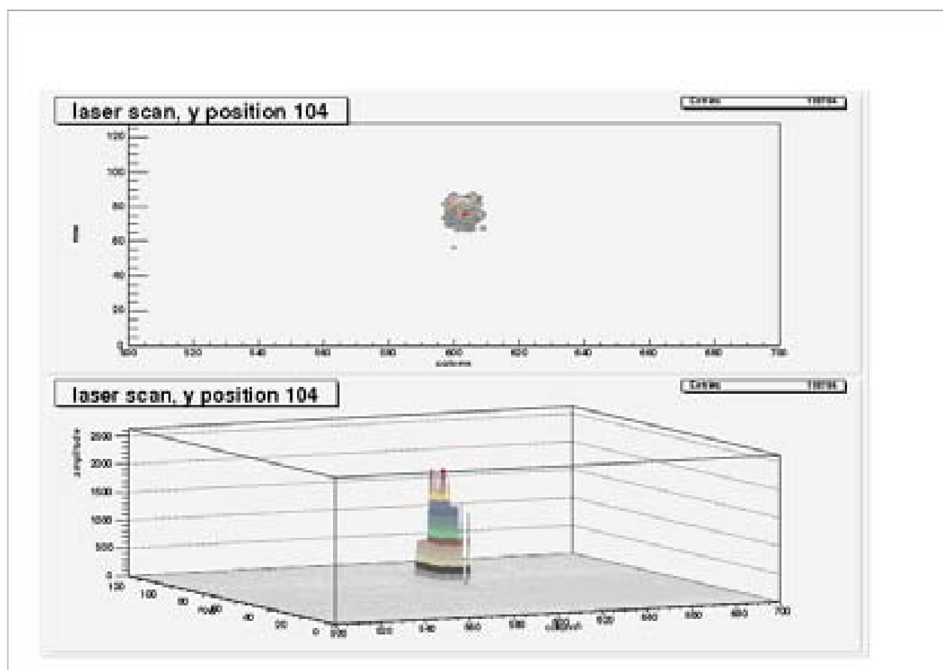


Figure A.7: Pos 104 of y axis scan.

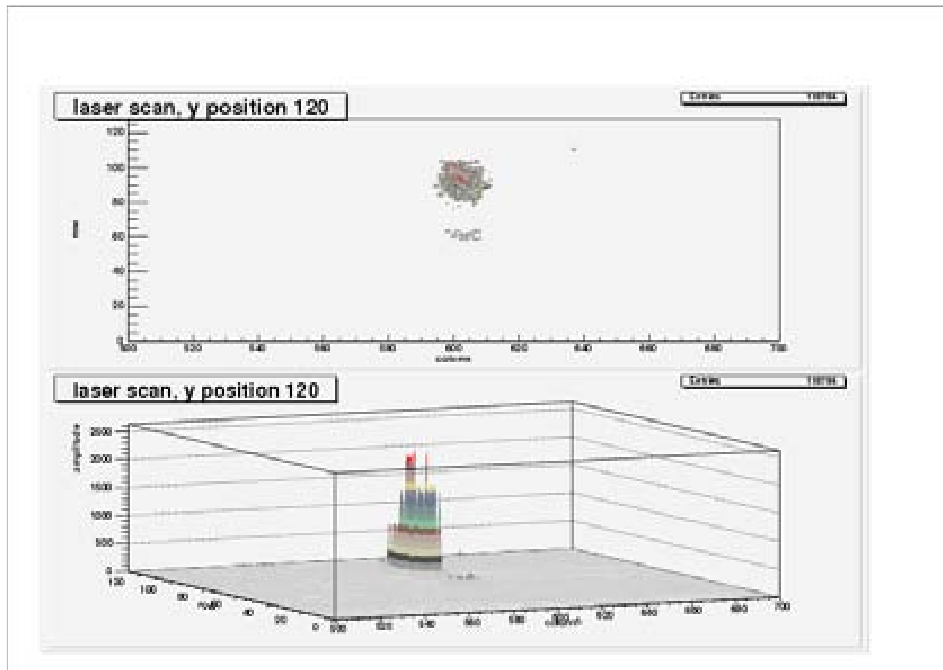


Figure A.8: Pos 120 of y axis scan.

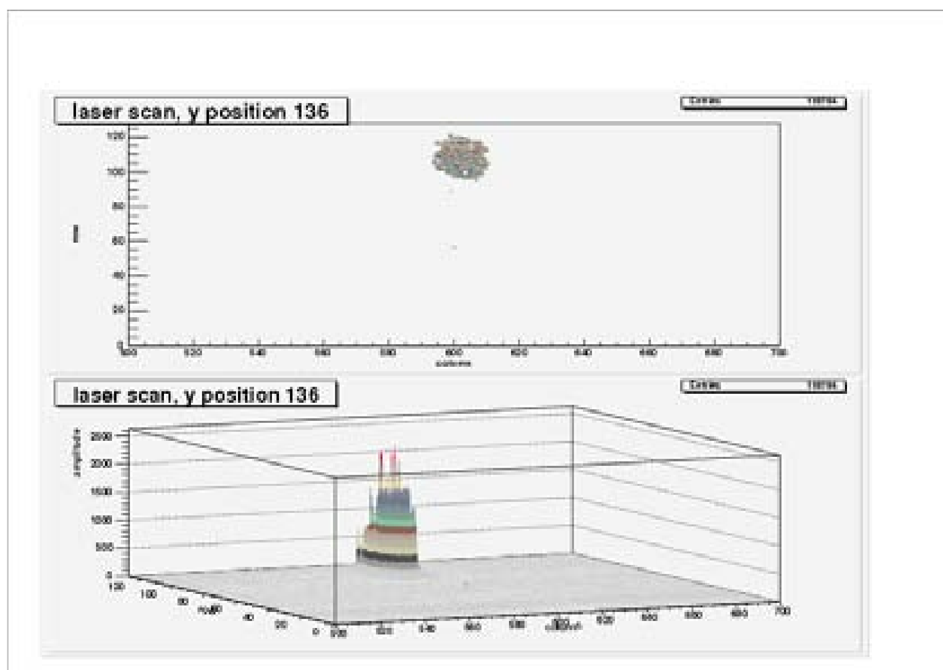


Figure A.9: Pos 136 of y axis scan.

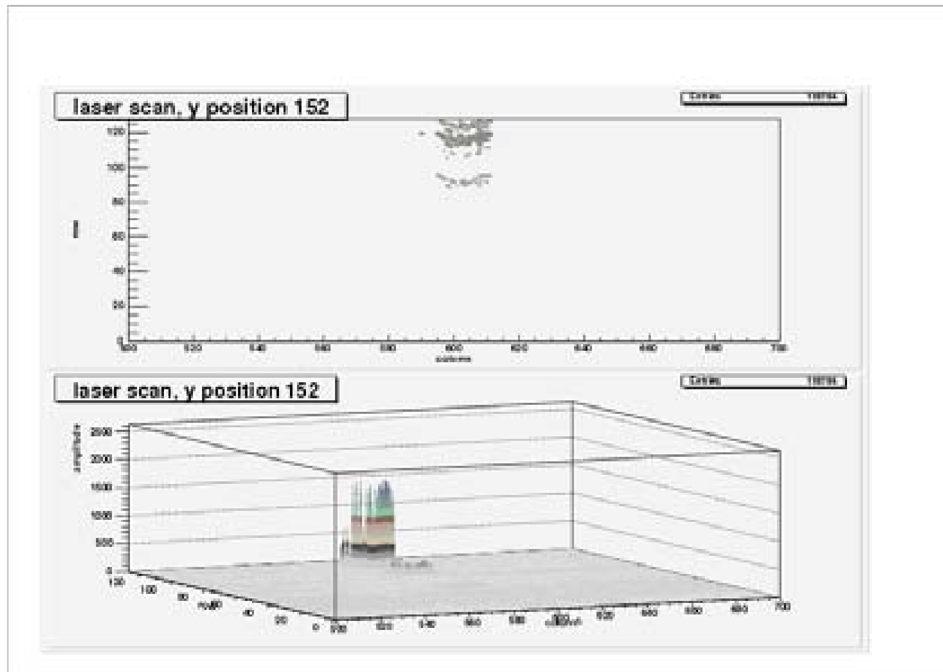


Figure A.10: Pos 152 of y axis scan.

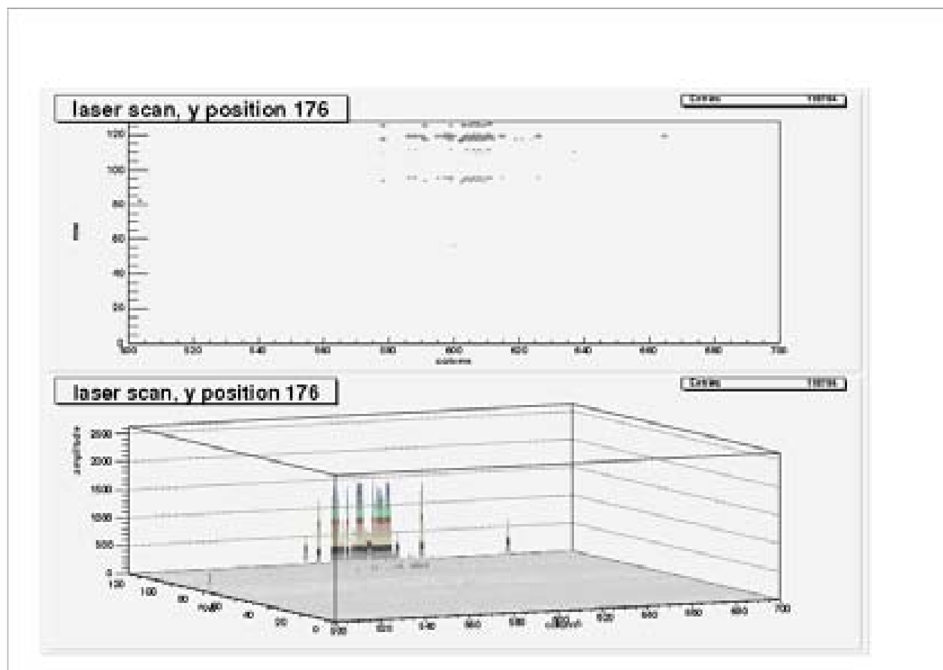


Figure A.11: Pos 176 of y axis scan.

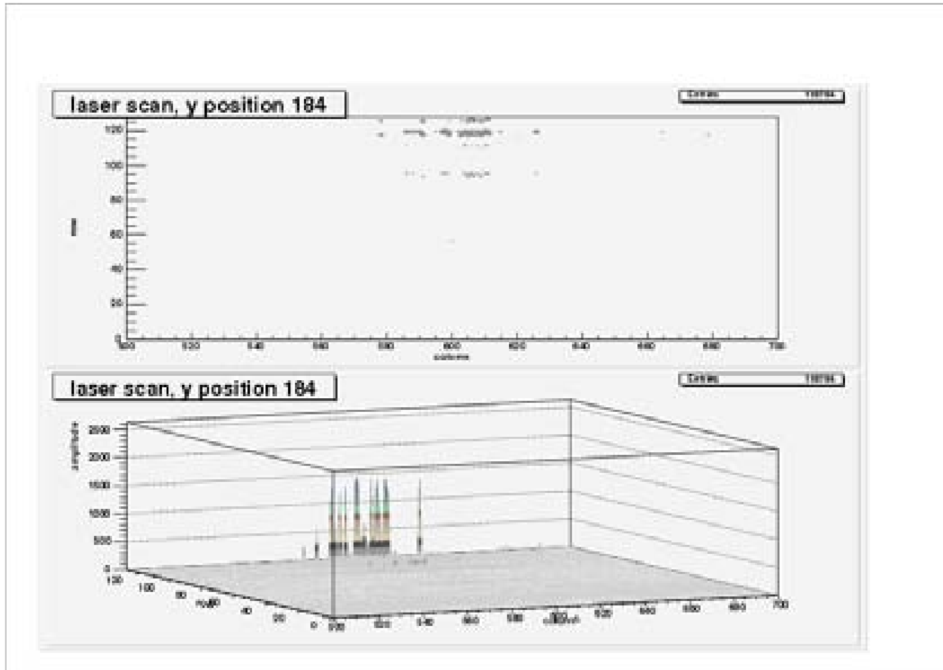


Figure A.12: Pos 184 of y axis scan.

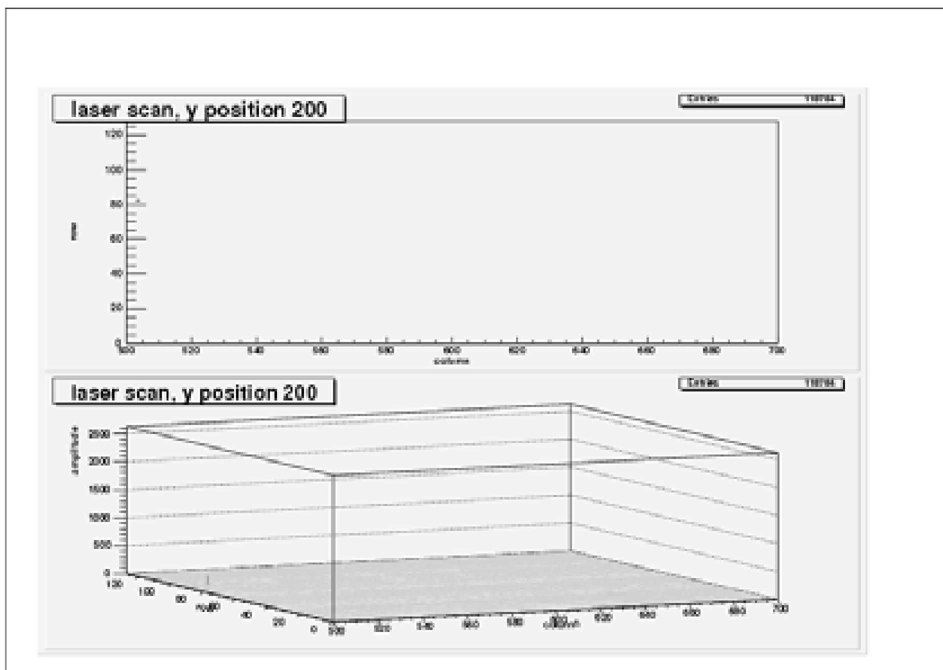


Figure A.13: Pos 200 of y axis scan.

A.2 X Axis Scan

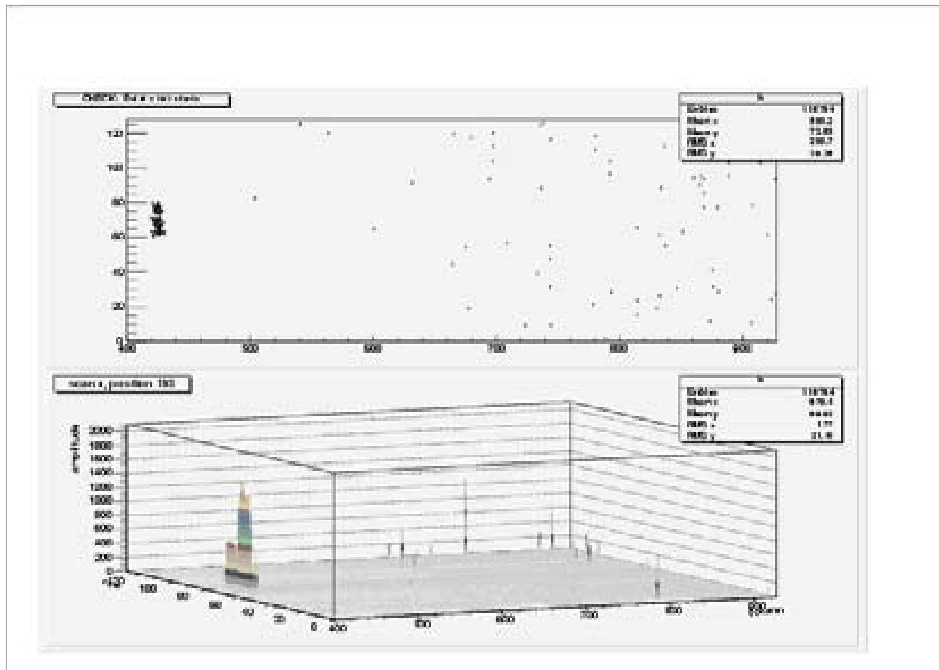


Figure A.14: Pos 193 of x axis scan.

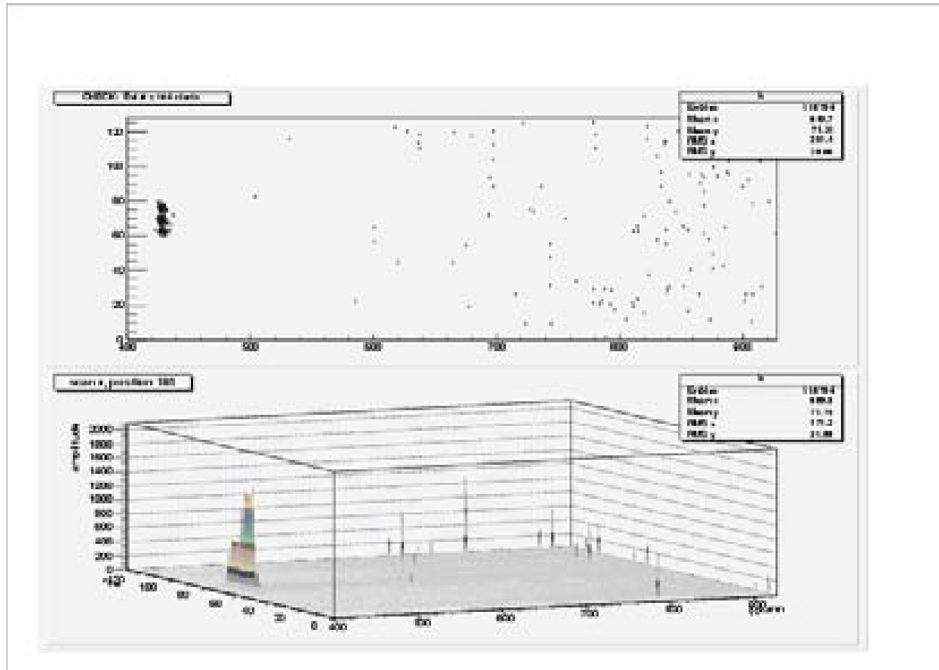


Figure A.15: Pos 185 of x axis scan.

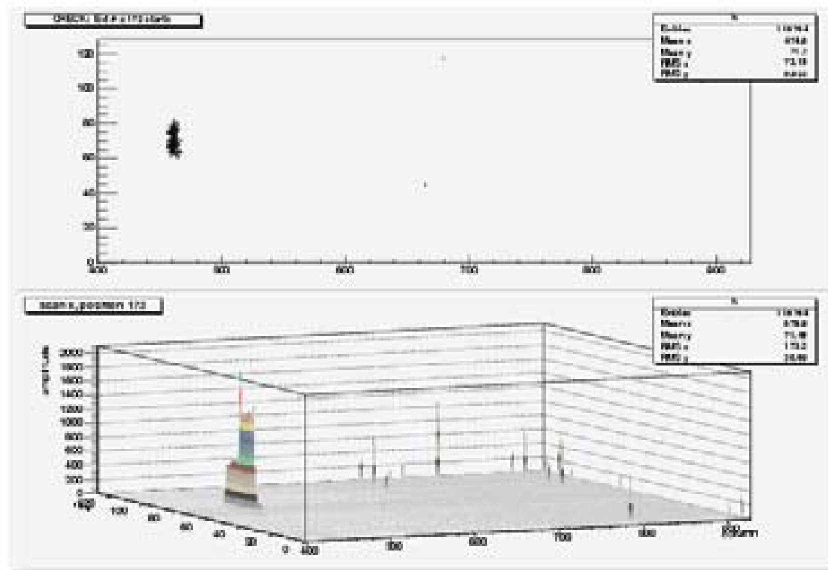


Figure A.16: Pos 173 of x axis scan.

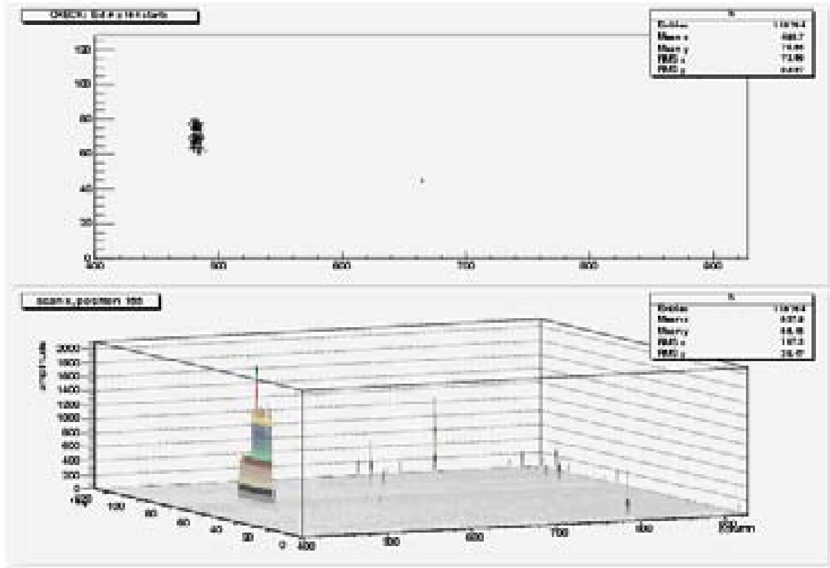


Figure A.17: Pos 165 of x axis scan.

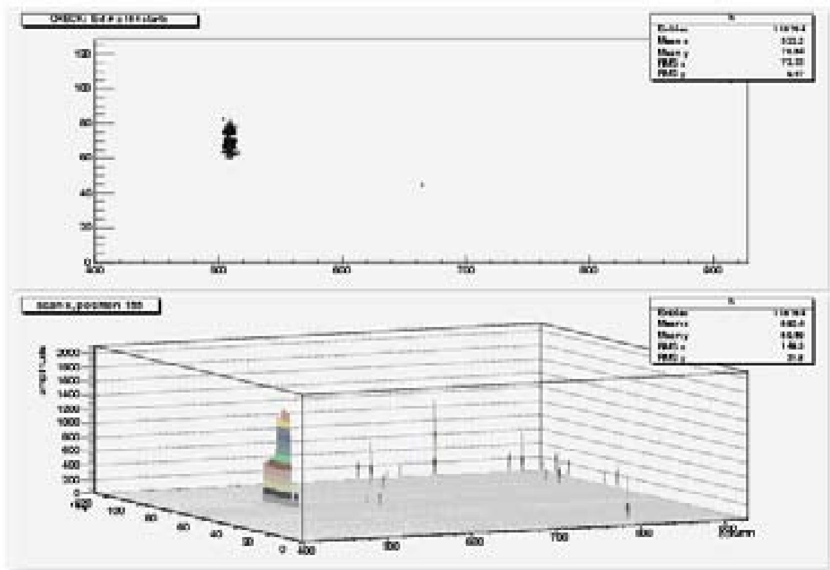


Figure A.18: Pos 155 of x axis scan.

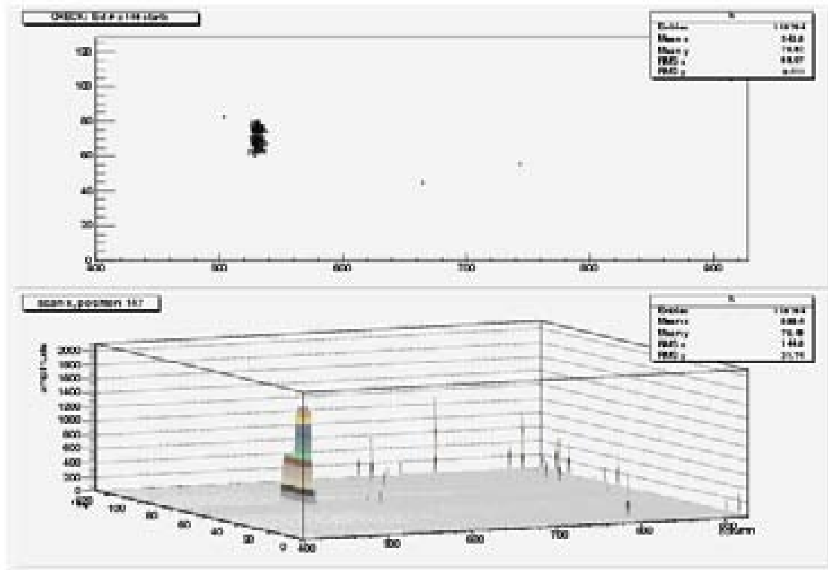


Figure A.19: Pos 147 of x axis scan.

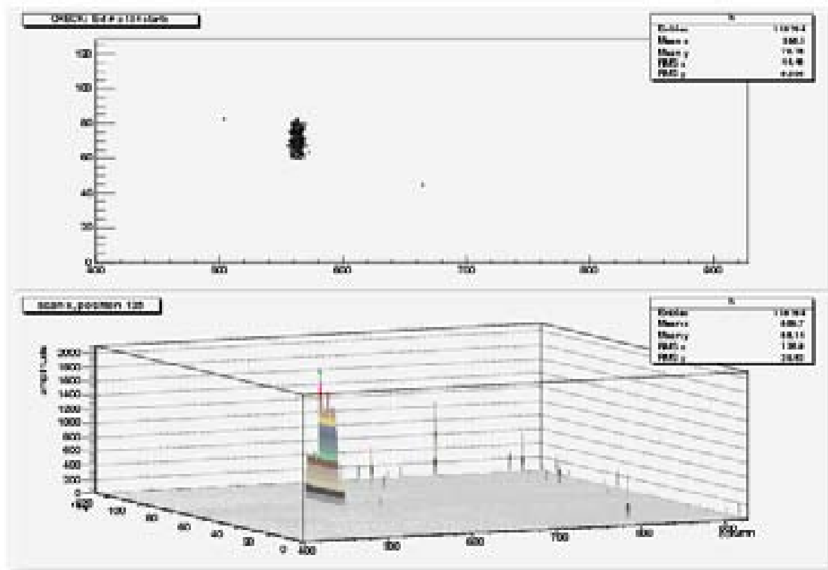


Figure A.20: Pos 135 of x axis scan.

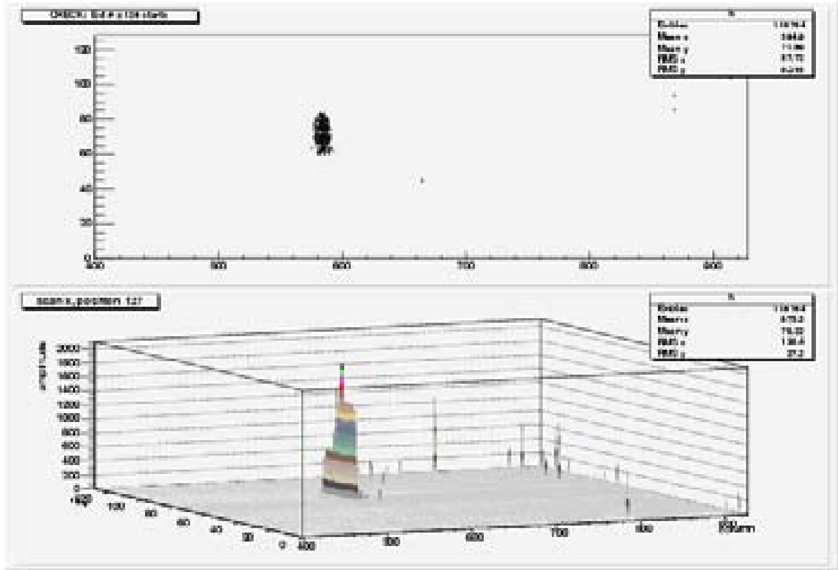


Figure A.21: Pos 127 of x axis scan.

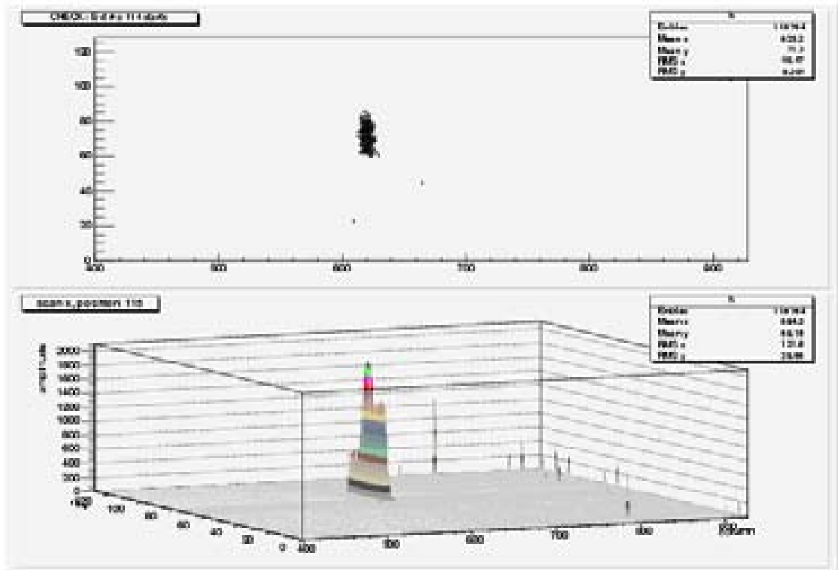


Figure A.22: Pos 115 of x axis scan.

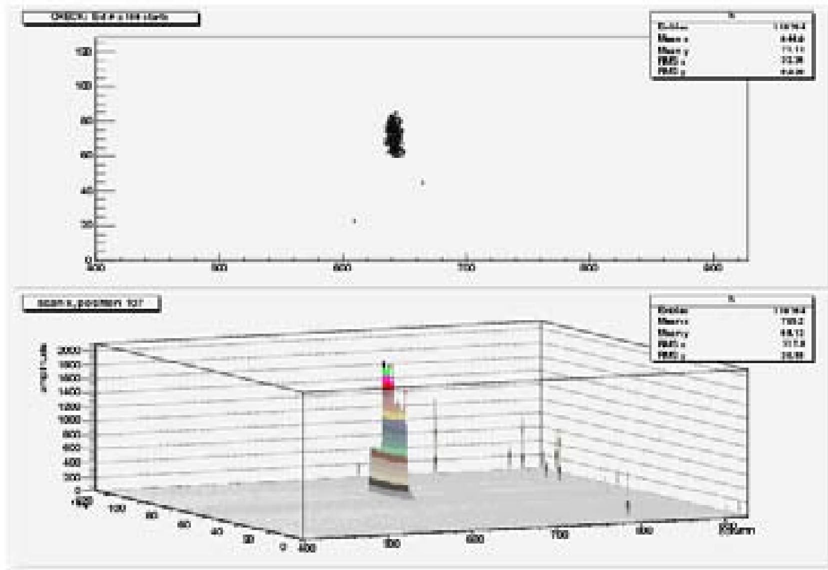


Figure A.23: Pos 107 of x axis scan.

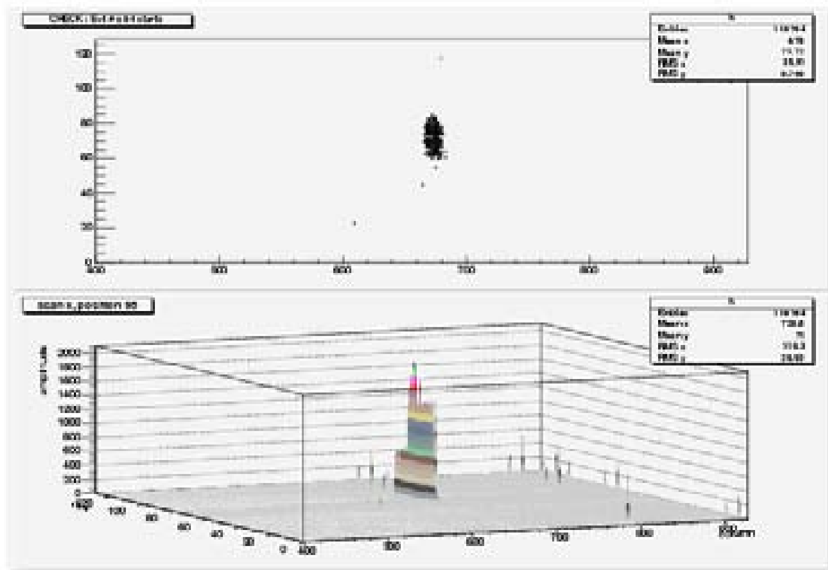


Figure A.24: Pos 095 of x axis scan.

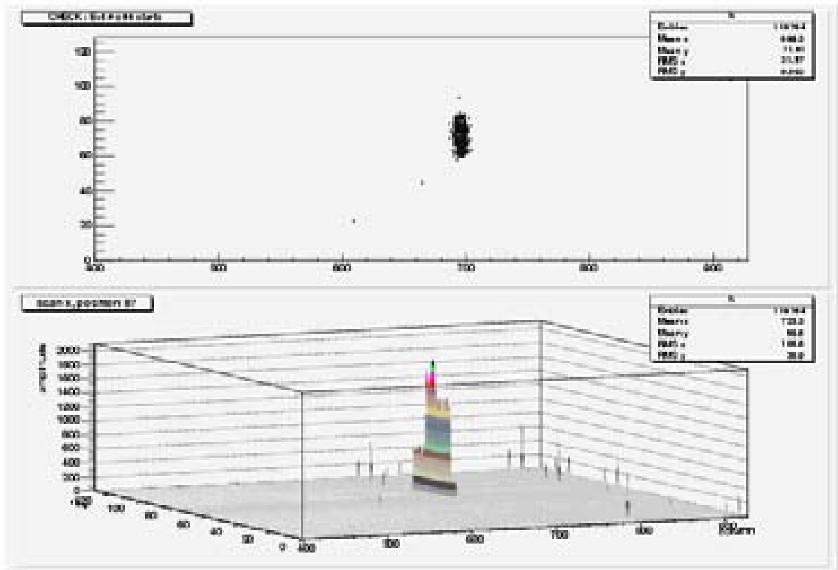


Figure A.25: Pos 087 of x axis scan.

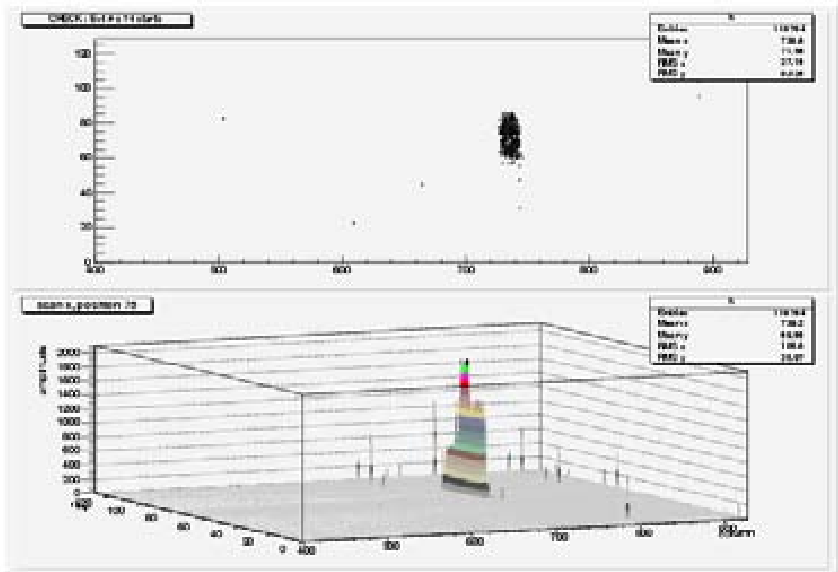


Figure A.26: Pos 075 of x axis scan.

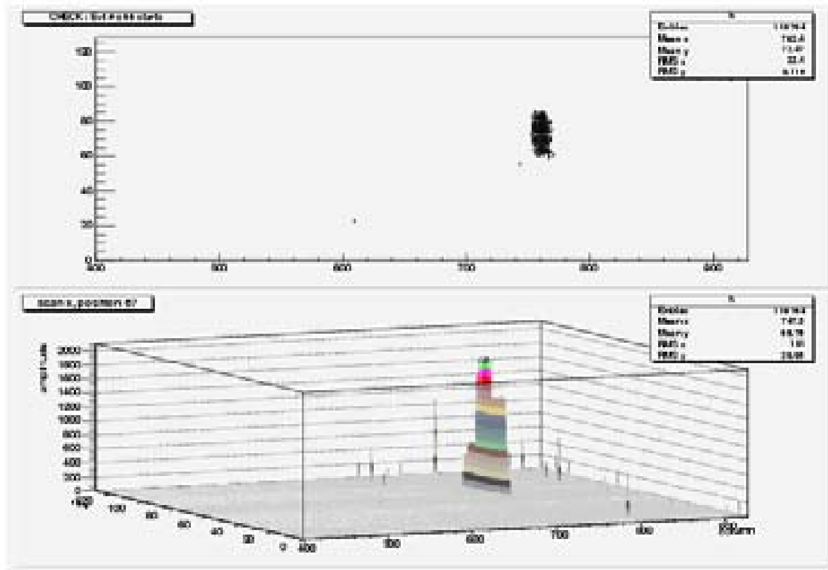


Figure A.27: Pos 067 of x axis scan.

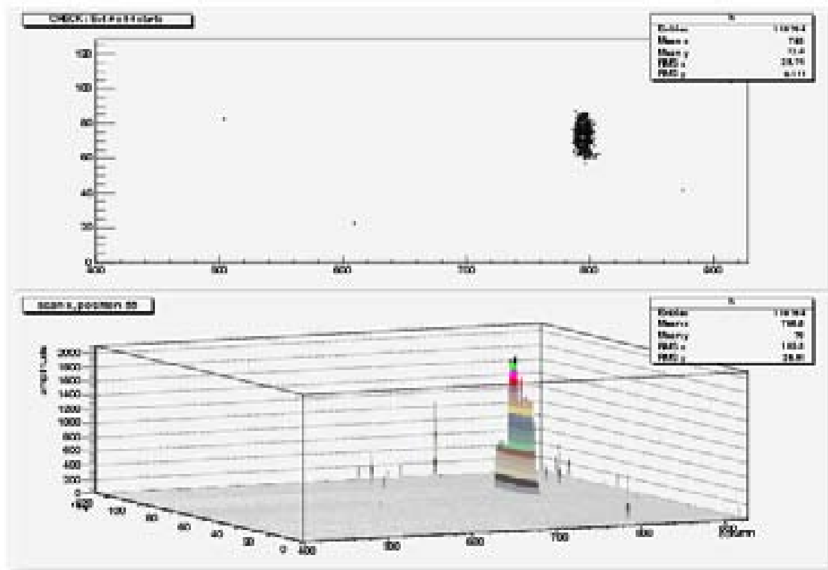


Figure A.28: Pos 055 of x axis scan.

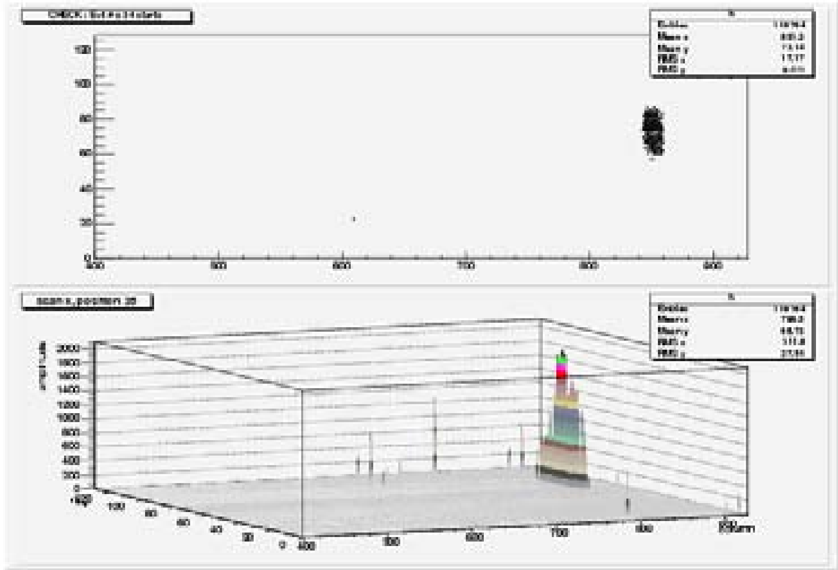


Figure A.29: Pos 035 of x axis scan.

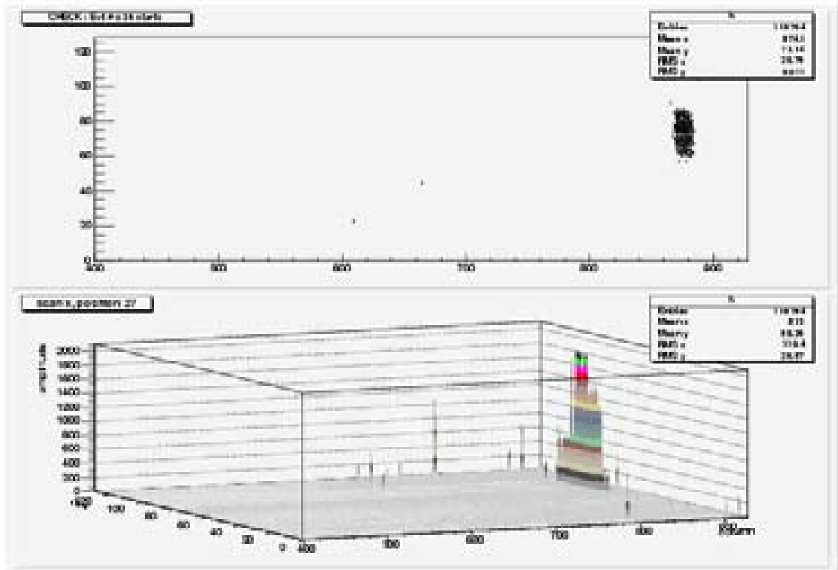


Figure A.30: Pos 027 of x axis scan.

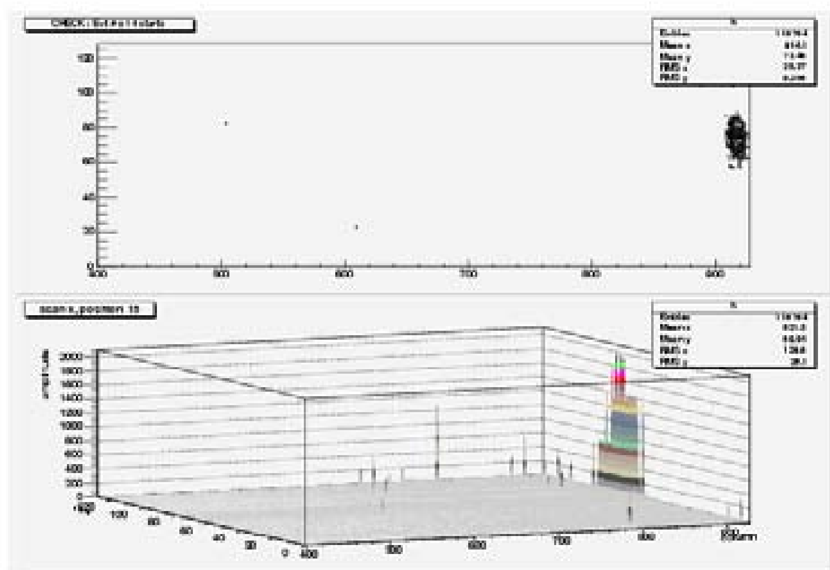


Figure A.31: Pos 015 of x axis scan.

Appendix B

Programing Files Sample for CAP4

```
/*
CAP4_sim1.c:

A simple program to evaluate the position resolution sensitivity of
the Belle Continuous Acquisition Pixel (CAP) sensors as a function of
N-well size and geometry, including binary simplification.


Processing steps:

1) generate impact point
2) Landau fluctuations of signal
3) diffuse charge
4) add noise
5) center of gravity calculation ==> trigger threshold crossing
6) accumulate statistics

7-APR-06/GSV

*/

#include <stdlib.h>
#include <stdio.h>
#include <math.h>
#include <fcntl.h>
#include <unistd.h>

#define SIGNOIZ  40  /* e- noise as starting place */
#define NOIZMAX  100  /* e- noise ending place */
#define SNR 10       /* SNR starting point -- as defined in the central pixel ma
#define SNRSTEP 1    /* SNR step size */
#define SNRMAX 11    /* SNR max */

#define EVTMAX 100   /* Number of sample events */

/* Array of 32 pixels (8 x 4), which is the minimalist lattic */

#define PINDEX 32    /* number of pixels */
                     /* 0-8 = -90 - -45 um; 4-7 0um - 90um; 90um - 180um */

#define NXELEC 8   /* number of electrodes in x */
#define NYELEC 4   /* number of electrodes in x */
#define NWELLX 9   /* number of electrodes in x */
#define NWELLY 5   /* number of electrodes in x */
#define LATXMIN -90.0  /* lower left corner of the array */
#define LATYMIN -90.0  /* lower left corner of the array */
#define CEOFFSETX 11.25   /* Collection Electrode offset lower left corner */
#define CEOFFSETY 22.5   /* Collection Electrode offset lower left corner */
double PIXX[PINDEX];
double PIXY[PINDEX];
double NWELLX[PINDEX];
double NWELLY[PINDEX];
int PIX[PINDEX][PINDEX];
int NWELL[PINDEX][PINDEX];
double PIXA[PINDEX][PINDEX];      /* analog stored values */

/* Energy loss values */

#define Zeta 0.178        /* Simplified Landau spread parameter [keV] */
#define Emp 3.733         /* Energy loss most probable [keV] */
```

```
#define Ctwopi 0.3989     /* 1/SQRT(2pi) */
#define Eholep 0.00362    /* keV/e-hole pair */

/* charge transport values */

#define Vemax 2.3e5       /* m/s velocity  */
//#define Tstep 40e-15      /* m between collisions atomic collisions */
#define Tstep 400e-15      /* modified for speed between collisions */
#define TSTEPMAX 500000  /* max number of diffusion steps */
#define DIMN 4            /* diffusion in 3-D lattice, 4th dim status */
#define ZSTEPMAX 10000    /* maximum number of charges to track */

double q[ZSTEPMAX][DIMN]; /* charges to transport */

/* charge collection */

int peakx;
int peaky;

/* noise contribution */

#define SYSNOIZ 8  /* 16 e- equiv. noise */

/* in order to log statistics, the following counters are defined: */

double pxsq[EVTMAX];   /* square of value */

/* end prelim -- function calls */

double moyal()
{
  /* returns Landau approximated energy loss  */
  double Etry,dice,ratio,normalize;
  double lambda, Omega, accept;

  do {
    normalize = RAND_MAX;
    dice = rand();
    Etry = 10.0 * (dice / normalize);

    //    printf("E try = %f\n", Etry);

    lambda = (Etry - Emp)/Zeta;
    Omega = Ctwopi*exp(-0.5*(lambda+exp(-lambda)));

    normalize = RAND_MAX;
    dice = rand();
    accept = (dice / normalize);
  } while (accept > Omega);
  //    printf("Eloss = %f, Omega = %f, accept = %f\n", Etry, Omega, accept);

  return Etry;
}

double gfluct()
{
/* returns gaussian with zero mean unit variance */
        static int iset=0;
        static double gset;
    double dice,normalize;
```

```
    double ratio;
        double fac,r,v1,v2;
    //       double drand48();

    normalize = RAND_MAX;
        if  (iset == 0) {
      do {
        dice = rand();
        ratio = dice/normalize;
        v1=2.0*(ratio)-1.0;
            //      printf("dice,ratio,normalize = %f %f %f\n",dice,ratio,normal
        dice = rand();
        ratio = dice/normalize;
        v2=2.0*(ratio)-1.0;
        //             printf("v1,v2 = %f %f\n",v1,v2);
                      r=v1*v1+v2*v2;
                } while (r >= 1.0);
                fac=sqrt(-2.0*log(r)/r);
                gset=v1*fac;
                iset=1;
                return v2*fac;
        } else {
                iset=0;
                return gset;
        }
}

/*>>>>>>>>>>>>>>>>>>>  start main <<<<<<<<<<<<<<<<<<<<<<<<<*/

main(int argc,char **argv)
{
  int isnr,ievt,qstep, idim, ehpairs, tstep, zstep, inoiz, i;
  int ipix, ipixx, ipixy, freeq, lostq, recombq, captq, garbage;
  int inwx,inwy;
  double crud, gfluct(), moyal();
  double roll,normal,rto,csnr;
  double ipx, ipy, zsep, step, ffree, fcaptq;
  double stepmax, latticepx, latticepy, peak, fract, xpos, ypos, ampl;
  double deltx, delty, resol, resolsum, runresol;
  double pxsqsum, pxsqavg, signif;

  FILE *Fstats,*Fsum, *fopen();
  char *wname, *sname;

/*___________________________end of declarations__________________________*/

  wname = "full_array.dat";
  sname = "full_summary.dat";
  Fstats = fopen(wname, "w");
  Fsum = fopen(sname, "w");

  normal = RAND_MAX;

/* --------------start the main sequence on timing loop HERE ----------- */

  printf("Starting simulation...\n");
  stepmax = Vemax * Tstep * 1e6; // um/sec
  printf("Stepmax = %f um\n", stepmax);
  fprintf(Fstats,"Starting simulation...\n");
  fprintf(Fsum,"Starting simulation...\n");
```

```
fclose(Fsum);

    /* define lattice electrode positions */

for(ipix=0;ipix<PINDEX;ipix++)
  {
    latticepx = LATXMIN + (ipix%8)*22.5 + 11.25;  //22.5um pitch
    latticepy = LATYMIN + (ipix/8)*45.0 + 22.5;  //45um pitch
    PIXX[ipix] = latticepx;
    PIXY[ipix] = latticepy;
    //      printf("Electrode = %d, x-coord = %f, y-coord = %f \n", ipix, latt
  }

    /* define N-well positions */

for(ipix=0;ipix<PINDEX+13;ipix++)
  {
    latticepx = LATXMIN + (ipix%9)*22.5;  //22.5um pitch
    latticepy = LATYMIN + (ipix/9)*45.0;  //45um pitch
    NWELLX[ipix] = latticepx;
    NWELLY[ipix] = latticepy;
    //      printf("Nwell = %d, x-coord = %f, y-coord = %f \n", ipix, latticep
  }

for(inoiz=SIGNOIZ;inoiz<NOIZMAX;inoiz=inoiz+10)
  {
    resolsum = 0.0; // zero stats for new noise point
    pxsqsum = 0.0; // zero stats for new noise point
    for(ievt=0;ievt<EVTMAX;ievt++)
  {

    /* calculate impact position */

    roll = rand();
    rto = roll/normal;
    ipx = 90.0* rto;
    roll = rand();
    rto = roll/normal;
    ipy = 90.0* rto;
    //      printf("ievt = %d, Impact position (x,y) = %2.1f,%2.1f um\n", ievt

    /* Landau fluctuation calculation  using Moyal approx.*/

    ehpairs = (moyal()/(Eholep));
    printf("# of e-hole pairs = %d \n", ehpairs);

    /* Distribute and randomize charge */

    zsep = 10.0/ehpairs;

    // clear charges

    for(zstep=0;zstep<ZSTEPMAX;zstep++)
      {
        for(idim=0;idim<DIMN;idim++)
      {
        q[zstep][idim] = -100.0;
      }
      }
```

```
// clear electrodes

for(ipixx=0;ipixx<NXELEC;ipixx++)
  {
    for(ipixy=0;ipixy<NYELEC;ipixy++)
  {
    PIX[ipixx][ipixy] = 0;
  }
  }

// clear N-wells

for(ipixx=0;ipixx<NWELLX;ipixx++)
  {
    for(ipixy=0;ipixy<NWELLY;ipixy++)
  {
    NWELL[ipixx][ipixy] = 0;
  }
  }

for(zstep=0;zstep<ehpairs;zstep++)
  {
    q[zstep][0] = ipx;
    q[zstep][1] = ipy;
    q[zstep][2] = -zstep*zsep;   // distribute uniformly along z
    q[zstep][3] = 1.0;          // available to diffuse, -100.0 = no exist
    //randomize z distibution
    roll = rand();
    rto = roll/normal;
    q[zstep][2] = q[zstep][2] + (rto-0.5)*zsep;
    if(q[zstep][2] < -14.0) {
  q[zstep][2] = q[zstep][2] + zsep; // reflect from bottom
    }
    if(q[zstep][2] > 0.0) {
  q[zstep][2] = q[zstep][2] - zsep; // reflect from top
    }
  }

/* Diffuse, collect & recombine charge */

for(tstep=0;tstep<TSTEPMAX;tstep++)
  {
for(qstep=0;qstep<ehpairs;qstep++)
  {
    if(q[qstep][3] > 0) {  //check if wandering charge
    for(idim=0;idim<DIMN-1;idim++)
    {
  roll = rand();
  rto = roll/normal;
  step = (rto-0.500)*2*stepmax;
  q[qstep][idim] = q[qstep][idim] + step;
  if(idim == 2) {
    if(q[qstep][2] < -14.0) {
      q[qstep][2] = q[qstep][2] - 2*step; // reflect from bottom
      roll = rand();
      rto = roll/normal;
      if(rto > 0.999)
        {
        q[qstep][3] = -2.0; // lost to substrate
        //      printf("q %d lost to substrate in z = %f2.1 @ timestep = %
```

```
                }
      }
      if(q[qstep][2] > 0.0) {
        q[qstep][2] = q[qstep][2] - 2*step; // reflect from top
        roll = rand();
        rto = roll/normal;
        if(rto > 0.995)
          {
          q[qstep][3] = -3.0; // lost to surface recombination
          //      printf("q %d lost to surf recomb in z = %f2.1 @ timestep =
          }
      }
    }
      }
      }
    }
  //      printf("timestep = %d\n", tstep);
          if((tstep % 10000) == 0) {
        freeq = 0;
        captq = 0;
        for(qstep=0;qstep<ehpairs;qstep++)
          {
        if(q[qstep][3] > 0) {  //check if wandering charge
          freeq = freeq + 1;
        }
        if( (q[qstep][3] > -1.5) && (q[qstep][3] < -0.5) ) {  //check if cap
          captq = captq + 1;
        }
          }
        ffree = freeq;
        fract = 100* ffree/ehpairs;
printf("Timestep = %d, # free = %d, # captured = %d, Percent free = %2.1f\n"
      }
  //  }

  //check if collected

  for(qstep=0;qstep<ehpairs;qstep++)
    {
      if(q[qstep][3] > 0) {  //check if wandering charge
    // test for electrode capture
      if(q[qstep][2] > -1.0) // speed up by confirming in electrode collecti
    {
      for(ipixx=0;ipixx<NXELEC; ipixx++)
        {
          for(ipixy=0;ipixy<NYELEC; ipixy++)
        {
          ipix = ipixx + 8*ipixy;
          if( (abs(q[qstep][0]-PIXX[ipix]) <3.0) && (abs(q[qstep][1]-PIXY[ip
            q[qstep][3] = -1.0;  // captured
            PIX[ipixx][ipixy] = PIX[ipixx][ipixy] + 1;
            printf("ipixx = %d, ipixy = %d\n", ipixx,ipixy);
            printf("Electrode capture of q %d @ (x,y,z) position at step %d

          }
        }
          }
        }
    }
    // test for N-well capture        if(q[qstep][2] > -1.0) // speed up by
```

```
  {
    for(ipixx=0;ipixx<NWELLX;ipixx++)
      {
        for(ipixy=0;ipixy<NWELLY;ipixy++)
        {
        ipix = ipixx + 9*ipixy;
          if( (abs(q[qstep][0]-NWELLX[ipixx])<9.5) && ((abs(q[qstep][1]-NW
            q[qstep][3] = -4.0;  // N-well captured
            //                PIX[ipixx][ipixy] = PIX[ipixx][ipixy] + 1;
          printf("ipixx = %d, ipixy = %d\n", ipixx,ipixy);
          printf("N-well capture of q %d @ (x,y,z) position at step %d = (
          //  printf("q %d captured @ ipixx = %d  ipixy = %d, timestep = %
          }
        }
        }
      }
  }

    }
  }
if(freeq == 0) {
  tstep = TSTEPMAX;
}
  }  // end of tstep loop for diffusion

freeq = 0;
lostq = 0;
recombq = 0;
captq = 0;
for(qstep=0;qstep<ehpairs;qstep++)
  {
    if(q[qstep][3] > 0) {  //check if wandering charge
  freeq = freeq + 1;
    }
    if( (q[qstep][3] > -1.5) && (q[qstep][3] < -0.5) ) {  //check if captu
  captq = captq + 1;
    }
    if( (q[qstep][3] > -2.5) && (q[qstep][3] < -1.5) ) {  //check if subst
  lostq = lostq + 1;
    }
    if( (q[qstep][3] > -3.5) && (q[qstep][3] < -2.5) ) {  //check if recom
  recombq = recombq + 1;
    }
    if( (q[qstep][3] > -4.5) && (q[qstep][3] < -3.5) ) {  //check if N-wel
  recombq = recombq + 1;
    }
    if(q[qstep][3] < -4.5 ) {  //check if lost to N-well
  garbage = garbage + 1;
    }
  }
printf("# of free charges at end of diffusion = %d\n", freeq);
printf("# of captured charges at end of diffusion = %d\n", captq);
printf("# of substrate lost charges at end of diffusion = %d\n", lostq);
printf("# of recombination lost charges at end of diffusion = %d\n", recom
fprintf(Fstats,"# of free charges at end of diffusion = %d\n", freeq);
fprintf(Fstats,"# of captured charges at end of diffusion = %d\n", captq);

for(ipixy=0;ipixy<PINDEX;ipixy++)
  {
    for(ipixx=0;ipixx<PINDEX;ipixx++)
```

```
  {
    printf("%4d ",  PIX[ipixx][ipixy]);
    fprintf(Fstats,"%4d ",  PIX[ipixx][ipixy]);
  }
    printf("\n");
    fprintf(Fstats,"\n");
  }


//      printf("first q (x,y,z) position at step %d = (%2.3f, %2.3f, %2.3f

/* add noise */

printf("noise statististics\n");
for(ipixy=0;ipixy<PINDEX;ipixy++)
  {
    for(ipixx=0;ipixx<PINDEX;ipixx++)
  {
    PIXA[ipixx][ipixy] = PIX[ipixx][ipixy] + inoiz * gfluct();
    printf("%5.1f ",  PIXA[ipixx][ipixy]);
    fprintf(Fstats,"%5.1f ",  PIXA[ipixx][ipixy]);
  }
    printf("\n");
    fprintf(Fstats,"\n");
  }

/* peak detect */

peak = 0;
for(ipixy=0;ipixy<PINDEX;ipixy++)
  {
    for(ipixx=0;ipixx<PINDEX;ipixx++)
  {
    if(PIXA[ipixx][ipixy] > peak) {
      peakx = ipixx;
      peaky = ipixy;
      peak = PIXA[ipixx][ipixy];
    }
  }
  }
printf("Peak pixel @ x = %d, y = %d\n",peakx,peaky);

/* center of gravity calculation -- 3 x 3 */

xpos = 0.0;
ypos = 0.0;
ampl = 0.0;
for(ipixy=peaky-1;ipixy<peaky+2;ipixy++)
  {
    for(ipixx=peakx-1;ipixx<peakx+2;ipixx++)
  {
    xpos = xpos + (PIXA[ipixx][ipixy] * PIXX[ipixx]);
    ypos = ypos + (PIXA[ipixx][ipixy] * PIXY[ipixy]);
    ampl = ampl + PIXA[ipixx][ipixy];
    //          printf("PIXX[ipixx] = %f \n",PIXA[ipixx][ipixy]);
    //          printf("PIXA[ipixx][ipixy] = %f \n",PIXA[ipixx][ipixy]);
    //          printf("PIXA[ipixx][ipixy] = %f \n",PIXA[ipixx][ipixy]);
    //          printf("xpos = %f, ypos = %f, ampl = %f\n",xpos,ypos,ampl)
  }
  }
```

```
      xpos = xpos / ampl;  // cog
      ypos = ypos / ampl;  // cog
      csnr = PIXA[peakx][peaky] / inoiz;
      printf("peak SNR = %2.1f for noise = %d e-\n",csnr,inoiz);
      printf("c.o.g. peak @ x = %2.3f, y = %2.3f um\n",xpos,ypos);
      printf("M.C.   peak @ x = %2.3f, y = %2.3f um\n",ipx,ipy);
      fprintf(Fstats,"c.o.g. peak @ x = %2.3f, y = %2.3f\n",xpos,ypos);
      fprintf(Fstats,"M.C.   peak @ x = %2.3f, y = %2.3f\n",ipx,ipy);
      deltx = fabs(xpos - ipx);
      delty = fabs(ypos - ipy);
      printf("Delta residuals x = %2.3f, y = %2.3f\n\n",deltx,delty);
      fprintf(Fstats,"Delta residuals x = %2.3f, y = %2.3f\n\n",deltx,delty);
      resol = sqrt( deltx*deltx + delty*delty);
      printf("Resolution = %2.3f um\n\n",resol);
      fprintf(Fstats,"Resolution = %2.3f um\n\n",resol);
      resolsum = resolsum + resol;
      runresol = resolsum / (ievt+1);
      pxsq[ievt] = resol * resol;
      pxsqsum = pxsqsum + pxsq[ievt];
      pxsqavg = pxsqsum / (ievt+1);
      //      printf("pxsq = %2.3f, pxsqsum = %2.3f \n",pxsq[ievt],pxsqsum);
      //      printf("pxsqavg = %2.3f \n\n",pxsq[ievt],pxsqsum);
      signif = sqrt(pxsqavg - runresol*runresol);
  printf("Running Resolution = %2.3f +/- %2.3f um   for %d events \n\n",runresol
    }
      Fsum = fopen(sname, "a");
      fprintf(Fsum,"%3d %2.3f %2.3f \n",inoiz, runresol, signif);
      fclose(Fsum);
      inoiz++;
    }  // inoiz loop

   /*%%%%%%%%%%%%%%%%%%%%%%% print out summary statistics %%%%%%%%%%%%%%%%%%%%%%%%

      /*

  //  printf("tstep, tmult = %f, %f\n", tstep, tmult);

  Fstat = fopen(wname, "a");

  tsum = 0;
  fprintf(Fstat," %2.1f", tthresh);
  printf("\n");
  rate = tsum * tmult;
  statsig = sqrt(tsum) * tmult;
  printf("Total Trigger rate = %5.1f +/- %5.1f Hz\n", rate,statsig);
  fprintf(Fstat," %5.1f %5.1f \n", rate, statsig);

      */

  fclose(Fstats);


  /* >>>>>>>>>>>>>>>>>> end main <<<<<<<<<<<<<<<<<<<<<<<<<<<<<*/
}
```

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