Chapter 5.

FEEDFORWARD SPACE-VECTOR PWM

5.1. Introduction

The modulation techniques applied to the three-level converter in Chapter 3 assume balanced voltages in the capacitors. In fact, these voltages cannot be maintained equal, not only due to the PWM modulation ripple (switching frequency), but also because the system is unable to achieve an NP current averaging zero over a modulation period [A32]. This problem arises for high modulation indices, mainly when low-power-factor loads are connected. As a result, a low-frequency ripple appears in the NP potential, the frequency of which is three times that of the output voltages. If the SV-PWM strategy does not take into account this imbalance, the obtained output line-to-line voltages will contain low-frequency harmonics (Fig. 5.1). Obviously, these harmonics will degrade the performance of the load; this is an important consideration for some applications, such as AC motor drives or applications in which the converter is connected to the electrical grid. A solution has been proposed for SPWM [A33], but this modulation does not offer the benefits of SV-PWM, such as larger output voltages and reduced switching frequency of the devices. An SV-PWM approach for obtaining balanced AC-output voltages when the DC-link capacitors have a permanent voltage imbalance is presented in another work [A34]. That approach requires four vectors for each modulation period, and their duty cycles are corrected after being calculated in a balanced SV diagram.

In this chapter, the proposed modulation method is based on obtaining duty cycles directly from the unbalanced SV diagram, and therefore requires no subsequent corrections. This process takes advantage of symmetry in the unbalanced diagram to

simplify long operations so that the approach can be implemented in a real-time digital processor. Additionally, since only three vectors are used during each modulation period, the switching frequencies of the devices are reduced.

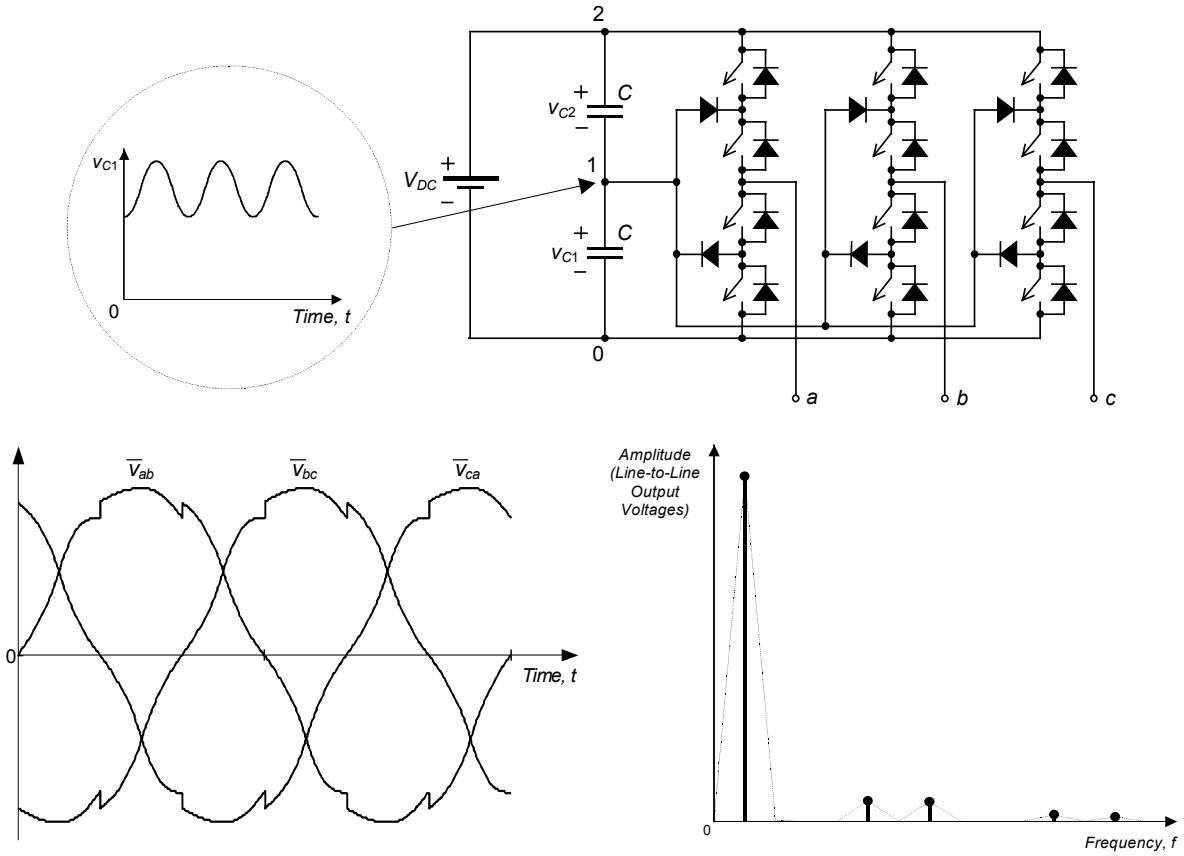


Fig. 5.1. *Distortion in the line-to-line output voltages due to low-frequency oscillation in the NP.*

5.2. SV Diagram Under Unbalanced Conditions

Several vectors of the SV diagram are affected when the voltages of the DC-link capacitors are not equal (Fig. 5.2). The short double vectors are split, and can therefore no longer be considered as only one voltage vector: one becomes smaller and the other larger, according to the direction of the imbalance, while the sum of the vectors remains constant. On the other hand, the medium vectors not only change in length but also in phase, so that their tips follow the boundary of the external hexagon.

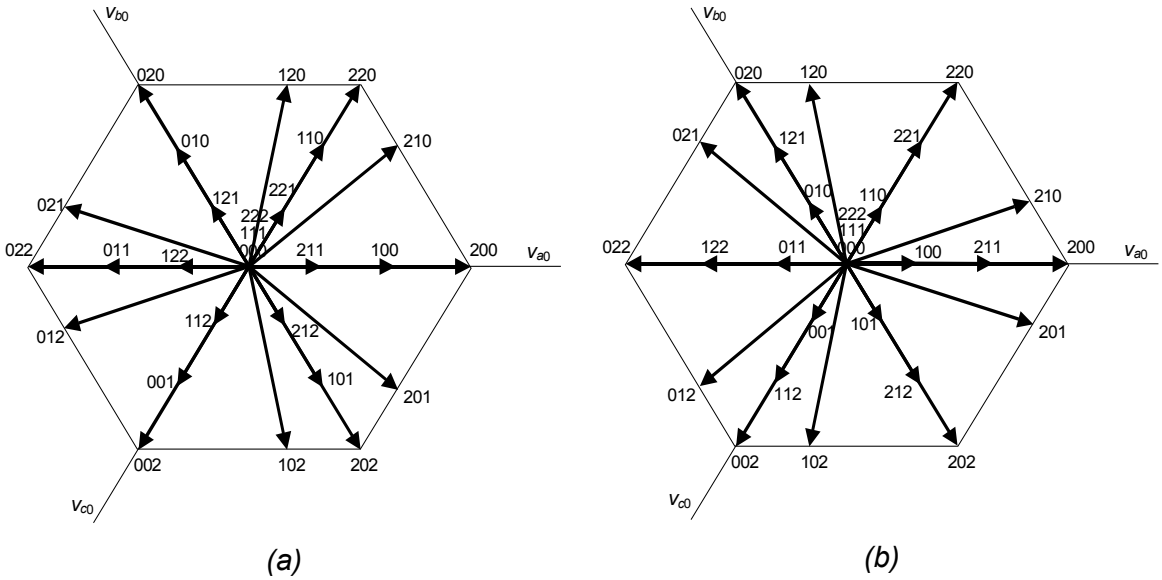


Fig. 5.2. *Vector diagram in the case of unbalanced voltages in the DC-link capacitors: (a) $v_{C1}>v_{C2}$ and (b) $v_{C1}<v_{C2}$.*

All these changes must be taken into account when an accurate reference vector is required; thus, the modulation stage must sense both voltages from the capacitors in order to establish a proper feedforward control. Table 5.1 shows the dependences of the vectors of the first sextant versus the voltages of the capacitors.

Components m'_1 and m'_2 are the non-normalized components of the vectors in the stationary coordinate axes located at zero and sixty degrees. Their values can be deduced from (3.22) as follows:

$$m'_1 = v_\alpha - \frac{1}{\sqrt{3}} v_\beta \quad \text{and} \quad m'_2 = \frac{2}{\sqrt{3}} v_\beta \ . \tag{5.1}$$

They are respectively related to the normalized components m_1 and m_2 by the coefficient $(v_{C1}+v_{C2})/2 = V_{DC}/2$.

Table 5.1. *Dependence of vectors in the first sextant with the voltages of the DC-link capacitors.*

	Components		Components	
Vector	*Alpha* (v_α)	*Beta* (v_β)	m'_1	m'_2
211	v_{C2}	0	v_{C2}	0
100	v_{C1}	0	v_{C1}	0
200	V_{DC}	0	V_{DC}	0
210	$\frac{v_{C1}}{2}+v_{C2}$	$\frac{\sqrt{3}}{2}v_{C1}$	v_{C2}	v_{C1}
221	$\frac{v_{C2}}{2}$	$\frac{\sqrt{3}}{2}v_{C2}$	0	v_{C2}
110	$\frac{v_{C1}}{2}$	$\frac{\sqrt{3}}{2}v_{C1}$	0	v_{C1}
220	$\frac{V_{DC}}{2}$	$\frac{\sqrt{3}}{2}V_{DC}$	0	V_{DC}

5.3. The Feedforward SV-PWM

5.3.1. Bases of the Method

The feedforward modulation will consider only three vectors per modulation period; therefore, from each pair of short vectors only one will be chosen. This selection will be made in order to balance the voltages of the capacitors, according to the method revealed for NTV modulation in Table 3.4.

The duty cycles of the vectors can be calculated by solving any of the equation systems in Section 3.1.4; however, this is not a practical solution for implementation in a DSP. The new fast feedforward modulation algorithm approach is based on the method of duty-cycle calculation from projections of the reference vector, as discussed in Section 3.1.5.

Parameters γ_1 and γ_2 are defined to reveal the modulation process under unbalanced conditions:

$$\gamma_1 = \frac{v_{C1}}{V_{DC}/2} \qquad \text{and} \qquad \gamma_2 = \frac{v_{C2}}{V_{DC}/2}\ , \tag{5.2}$$

which can be related to each other as

$$\gamma_1 + \gamma_2 = \frac{v_{C1} + v_{C2}}{V_{DC}/2} = \frac{V_{DC}}{V_{DC}/2} = 2\,. \tag{5.3}$$

Fig. 5.3 shows a representation of the normalized first sextant when v_{C1} is greater than v_{C2} (this sign of imbalance will henceforth be used). Despite the imbalance, the shape of this sextant still remains a regular triangle; additionally, the changes produced in the vectors are not at random, but instead follow symmetries.

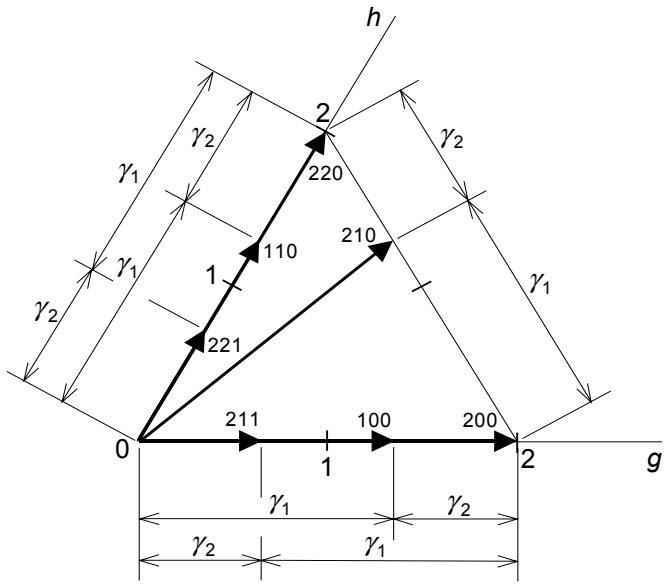


Fig. 5.3. *Symmetries in the first sextant in the case of unbalanced voltages in the DC-link capacitors (v_{C1}>v_{C2}).*

The complicating factor is that the regions change their shapes, and are also dependent on which short vectors are selected for each modulation cycle. Fig. 5.4 shows the four possibilities.

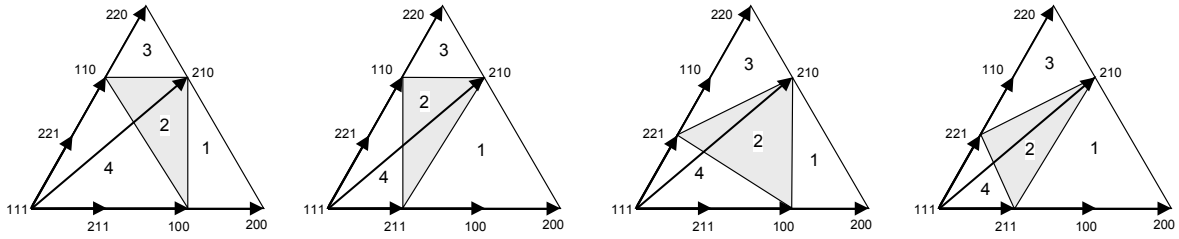


Fig. 5.4. *Shape of the regions depends on which short vectors are selected.*

It seems quite difficult to determine not only the region in which the extreme of the reference vector will be found, but also to work out the duty cycles for the vectors. Nevertheless, as all the regions still keep at least one 60º angle, the components m_1 and m_2 will be very useful for both processes. However, first, it is necessary to define a new variable m_{12} that depends on them, as follows:

$$m_{12} = 2 - m_1 - m_2 \,. \tag{5.4}$$

Graphically, these parameters can be represented in the normalized first sextant (Fig. 5.5).

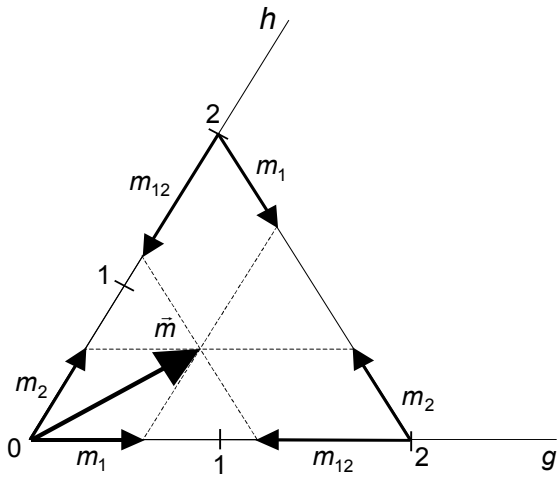
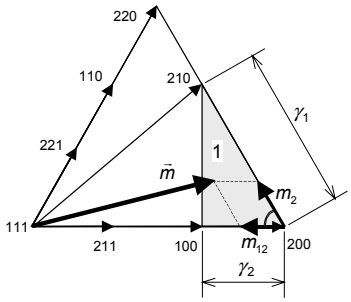
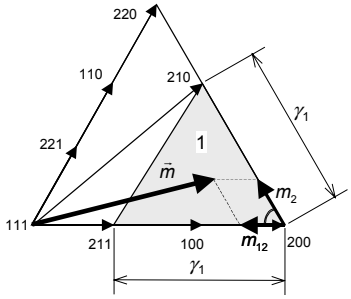
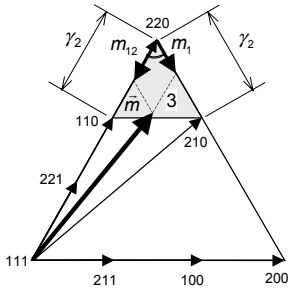
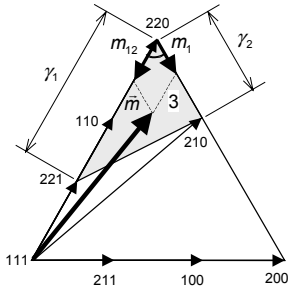
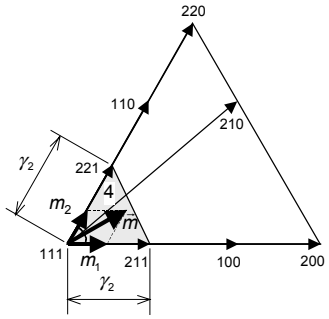
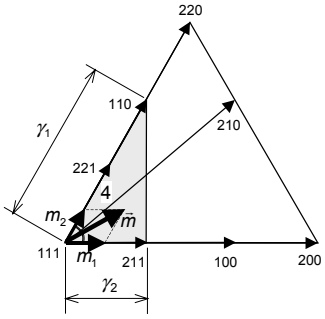


Fig. 5.5. *Different projections of the reference vector in the normalized first sextant.*

Table 5.2 shows all possible cases, as well as duty cycles, which have been calculated by the method of projections. There are 12 cases that have been grouped into four sets, in accordance with the regions defined in the first sextant. For example, since Region 1 uses only one short vector, there are two cases for this region, “Region 1 (100)” and “Region 1 (211),” depending on the selected short vector. For Region 3, the situation is similar with vectors 110 and 221. On the other hand, as Regions 2 and 4 use two short vectors, each has four cases. Once the short vectors are selected according to the balance requirements, the modulation process deals with only one case per region and therefore, only four cases must be considered for any modulation cycle.

Table 5.2. *Region set condition and duty-cycle calculation.*

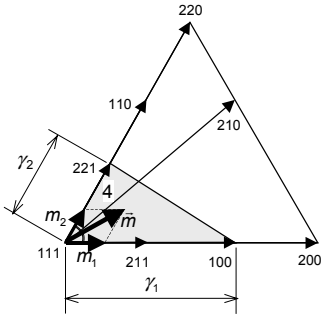
	Region 1 (100) $d_{100} = \frac{m_{12}}{\gamma_2} \qquad d_{210} = \frac{m_2}{\gamma_1} \qquad d_{200} = 1 - \frac{m_{12}}{\gamma_2} - \frac{m_2}{\gamma_1}$ Region Set Condition: $d_{200} = 1 - \frac{m_{12}}{\gamma_2} - \frac{m_2}{\gamma_1} \geq 0$
	Region 1 (211) $d_{211} = \frac{m_{12}}{\gamma_1} \qquad d_{210} = \frac{m_2}{\gamma_1} \qquad d_{200} = 1 - \frac{m_{12}}{\gamma_1} - \frac{m_2}{\gamma_1}$ Region Set Condition: $d_{200} = 1 - \frac{m_{12}}{\gamma_1} - \frac{m_2}{\gamma_1} \geq 0$
	Region 3 (110) $d_{110} = \frac{m_{12}}{\gamma_2} \qquad d_{210} = \frac{m_1}{\gamma_2} \qquad d_{220} = 1 - \frac{m_{12}}{\gamma_2} - \frac{m_1}{\gamma_2}$ Region Set Condition: $d_{220} = 1 - \frac{m_{12}}{\gamma_2} - \frac{m_1}{\gamma_2} \geq 0$
	Region 3 (221) $d_{221} = \frac{m_{12}}{\gamma_1} \qquad d_{210} = \frac{m_1}{\gamma_2} \qquad d_{220} = 1 - \frac{m_{12}}{\gamma_1} - \frac{m_1}{\gamma_2}$ Region Set Condition: $d_{220} = 1 - \frac{m_{12}}{\gamma_1} - \frac{m_1}{\gamma_2} \geq 0$
	Region 4 (211-221) $d_{211} = \frac{m_1}{\gamma_2} \qquad d_{221} = \frac{m_2}{\gamma_2} \qquad d_{111} = 1 - \frac{m_1}{\gamma_2} - \frac{m_2}{\gamma_2}$ Region Set Condition: $d_{111} = 1 - \frac{m_1}{\gamma_2} - \frac{m_2}{\gamma_2} \geq 0$



Region 4 (110-211)

$$d_{211} = \frac{m_1}{\gamma_2} \qquad d_{110} = \frac{m_2}{\gamma_1} \qquad d_{111} = 1 - \frac{m_1}{\gamma_2} - \frac{m_2}{\gamma_1}$$

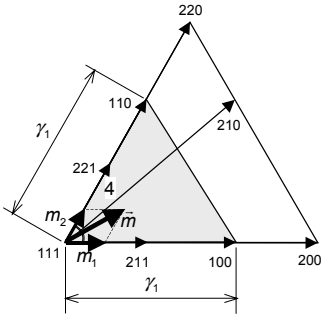
Region Set Condition: $d_{111} = 1 - \frac{m_1}{\gamma_2} - \frac{m_2}{\gamma_1} \geq 0$



Region 4 (100-221)

$$d_{100} = \frac{m_1}{\gamma_1} \qquad d_{221} = \frac{m_2}{\gamma_2} \qquad d_{111} = 1 - \frac{m_1}{\gamma_1} - \frac{m_2}{\gamma_2}$$

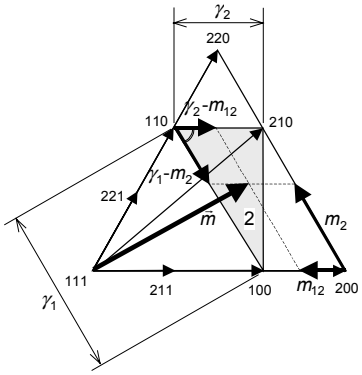
Region Set Condition: $d_{111} = 1 - \frac{m_1}{\gamma_1} - \frac{m_2}{\gamma_2} \geq 0$



Region 4 (100-110)

$$d_{100} = \frac{m_1}{\gamma_1} \qquad d_{110} = \frac{m_2}{\gamma_1} \qquad d_{111} = 1 - \frac{m_1}{\gamma_1} - \frac{m_2}{\gamma_1}$$

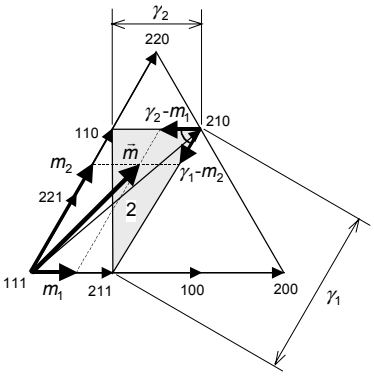
Region Set Condition: $d_{111} = 1 - \frac{m_1}{\gamma_1} - \frac{m_2}{\gamma_1} \geq 0$



Region 2 (100-110)

$$d_{100} = \frac{\gamma_1 - m_2}{\gamma_1} = 1 - \frac{m_2}{\gamma_1} \qquad d_{210} = \frac{\gamma_2 - m_{12}}{\gamma_2} = 1 - \frac{m_{12}}{\gamma_2}$$

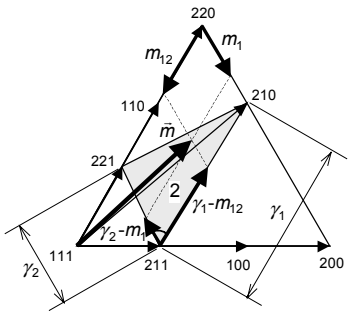
$$d_{110} = \frac{m_2}{\gamma_1} + \frac{m_{12}}{\gamma_2} - 1$$



Region 2 (110-211)

$$d_{110} = \frac{\gamma_2 - m_1}{\gamma_2} = 1 - \frac{m_1}{\gamma_2} \qquad d_{211} = \frac{\gamma_1 - m_2}{\gamma_1} = 1 - \frac{m_2}{\gamma_1}$$

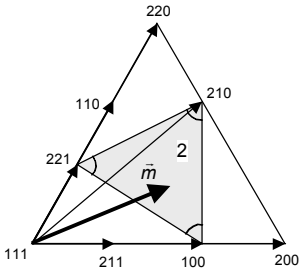
$$d_{210} = \frac{m_1}{\gamma_2} + \frac{m_2}{\gamma_1} - 1$$



Region 2 (211-221)

$$d_{210} = \frac{\gamma_1 - m_{12}}{\gamma_1} = 1 - \frac{m_{12}}{\gamma_1} \qquad d_{221} = \frac{\gamma_2 - m_1}{\gamma_2} = 1 - \frac{m_1}{\gamma_2}$$

$$d_{211} = \frac{m_{12}}{\gamma_1} + \frac{m_1}{\gamma_2} - 1$$



Region 2 (100-221)

$$d_{100} = \frac{1}{\Delta}\left(\frac{m_1}{\gamma_2} + \frac{m_{12}}{\gamma_1} - 1\right) \qquad d_{210} = \frac{1}{\Delta}\left(\frac{m_1}{\gamma_1} + \frac{m_2}{\gamma_2} - 1\right)$$

$$d_{221} = \frac{1}{\Delta}\left(\frac{m_2}{\gamma_1} + \frac{m_{12}}{\gamma_2} - 1\right) \qquad \text{with:} \quad \Delta = \frac{\gamma_1}{\gamma_2} + \frac{\gamma_2}{\gamma_1} - 1$$

It is important to mention the following points:

- Although the shapes of the regions are not equilateral triangles, each still retains at least one 60º angle that is used as a center for vector decomposition.

- Regions 1, 3 and 4 are activated when the only duty cycle that is potentially able to be negative is instead positive. The activation of Region 2 hinges on the non-activation of the others. Therefore, only at most three simple comparison operations must be done to determinate the appropriate region.

- The case “Region 2 (100-221)” cannot be analyzed by symmetries. Therefore, it has been calculated analytically. Since this case and the case “Region 4 (100-221)” will require more switching steps for the switches of the converter, they could be ignored in the modulation. Instead, either to replace vector 100 with 211 or vector 221 with 110 can be considered. For example, if vector 100 is substituted for vector 211, the case “Region 2 (100-221)” becomes the case “Region 2 (211-221).” The process is similar for Region 4. Nevertheless, in order to not lose much control for the NP balance, the expressions $\left(1-\left|1-m_1\right|\right)\cdot\left|i_a'\right|$ and $\left(1-\left|1-m_2\right|\right)\cdot\left|i_c'\right|$ would be helpful in deciding which change should be done, such the highest value reveals which vector has more influence on the balance (100 or 221, respectively). These expressions are reasoned from the standpoint that the closer m_1 and m_2 are to the unity value, the higher will be the control of the NP voltage. Obviously, the phase current levels also directly affect the control.

- For a DSP to more quickly process the values given in Table 5.2, parameters $1/\gamma_1$ and $1/\gamma_2$ can be calculated previously by a division algorithm, so that the only product operations remain to be applied.

After determining which sequence best enables the vectors in the first sextant to achieve low switching frequency, the next and final step is to apply the calculated duty cycles to the corresponding vectors. This task requires knowledge of the real sextant in which the reference vector lies, and it can be performed by simply interchanging the states of the output phases in accordance with the equivalences given in Table 3.3.

5.3.2. Simulated Results

Some simulated results are obtained from Matlab-Simulink. For this example, the converter is supplied by a DC source V_{DC}=1800 V and the output currents are provided by a balanced set of three-phase current sources with an RMS value I_{RMS}=220 A and a frequency f=50 Hz. The DC-link capacitors are C=550 μF and the modulation index m=1 (amplitude of the normalized reference vector $m_n = \sqrt{3}$), which is the worst case for producing voltage oscillations in the NP. None of the possible cases listed in Table 5.2 have been excluded from the modulation process.

The results shown in Fig. 5.6 include the voltage of the lower capacitor (v_{C1}) as well as the AC output line-to-line voltages; all of these are local averaged variables in order to show the quality of the waves obtained by the proposed modulation. Different load current angles (φ) have been considered for the simulations. For the noncompensated method, the parameters γ_1 and γ_2 are defined to be unity; hence, a balanced SV diagram is assumed for the calculation of duty cycles. The selection of the short vectors for the NP voltage balance compensation is also applied (Table 3.4). Low-frequency distortion appears in the output voltages for these cases when the amplitude of the NP voltage ripple becomes significant. In contrast, the output voltages obtained by the feedforward modulation are perfectly balanced and have no distortion.

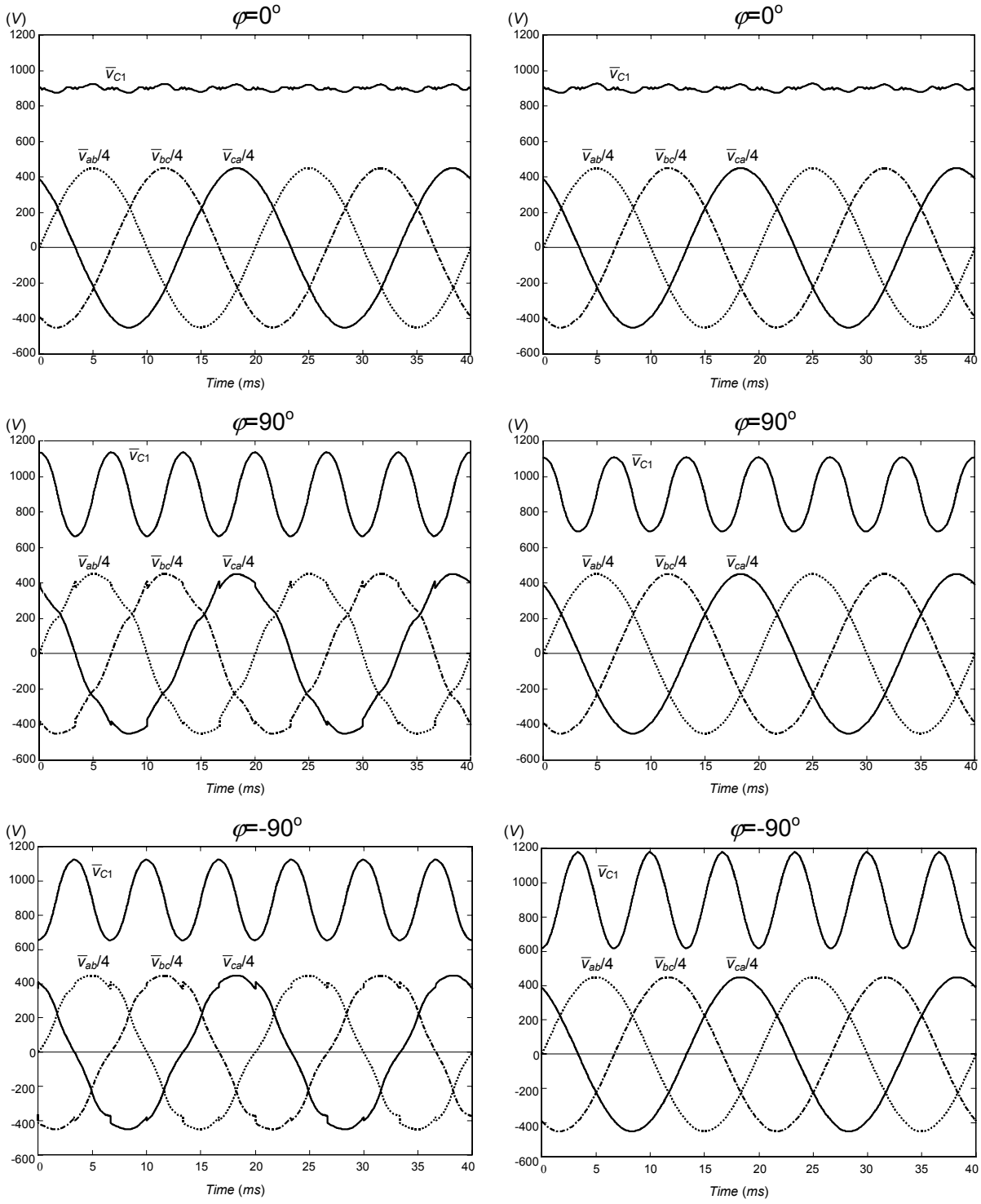


Fig. 5.6. *Simulated results. Averaged variables for different load current angles (φ).*
Left graphics: without feedforward compensation.
Right graphics: with feedforward compensation.

The amplitude of the NP voltage ripple for phase current angles $\varphi \in [0°, 180°]$ is smaller for the feedforward modulation algorithm. However, this voltage amplitude is bigger for load angles $\varphi \in [-180°, 0°]$.

The NP peak-to-peak voltage ripple is graphically quantified in Fig. 5.7 ($\Delta V_{NP}/V_{DC}$), in which all the curves illustrated are for constant values of the nondimensional parameter β, which is defined as follows:

$$\beta = \frac{I_{RMS}}{f\,C V_{DC}}. \tag{5.5}$$

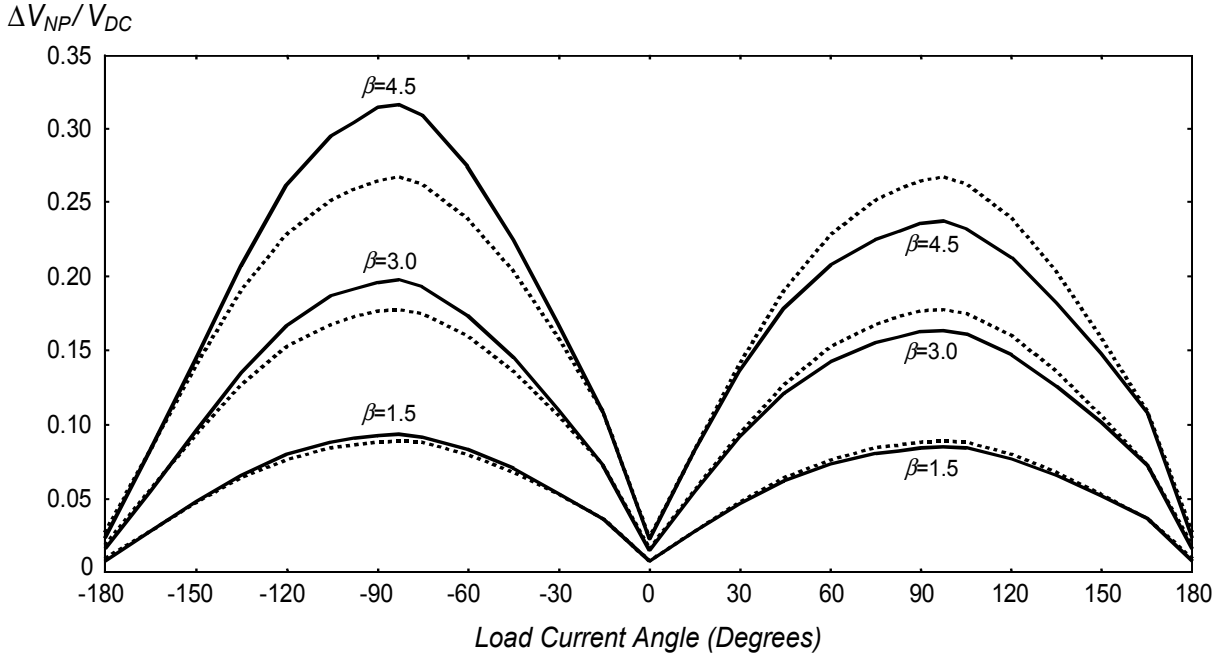


Fig. 5.7. *Voltage ripple in the NP for different load current angles (φ).*
Discontinuous lines: no compensation.
Continuous lines: with feedforward compensation.

As the information given is for the worst operation conditions (maximum length of the reference vector, m=1), it can be used for purposes of design. Therefore, going through this graphic, the maximum voltage applied to the capacitors and the devices of the bridge can be calculated as follows:

$$V_{Max} = \frac{V_{DC}}{2}\left(1 + \frac{\Delta V_{NP}}{V_{DC}}\right). \tag{5.6}$$

Nevertheless, when the system behaves as a rectifier (the energy flows from the AC side to the DC side), the ripple is not always centered at a value half the level of the DC-link voltage; and in addition, the system may become instable. This happens at some points nearby unity PF ($\varphi = 180^o$) operation. Some instabilities of the system were also reported [A33] for the SPWM feedforward method.

5.3.3. Instability in the Rectifier Mode

The bizarre behavior of the converter in the rectifier mode can be explained as follows. When the modulation algorithm assumes a balanced SV diagram, the average value of the NP current produced by the medium vectors and calculated over a line period is zero. In contrast, this does not happen with the feedforward modulation. However, their effect can usually be compensated for by proper utilization of the short vectors. The problem appears for very large modulation indices, when the duty cycles of the short vectors are very small. It seems that when the converter is operating as a rectifier, there are some current phase conditions that render the NP current contribution of the short vectors insufficient to compensate the imbalance generated by the medium vectors. Thus, the NP voltage exhibits an offset, which can be positive or negative. However, this new stable point might not be achieved depending on the transition process and the initial conditions of the NP voltage. As a result, the system might collapse in such a way that the full DC-link voltage is applied to only one capacitor. Although the feedforward modulation can still generate a balanced set of AC output voltages in such conditions, the devices of the bridge and one of the capacitors would support too much voltage to maintain system operation.

Fig. 5.8 shows operating conditions in which the converter is unstable in the rectifier mode. The boundary lines have been obtained for some values of the parameter β defined in (5.5). In the areas above the lines the system cannot recover from extreme initial voltage conditions in the capacitors. These initial conditions involve either, zero volts or full DC-link voltage (V_{DC}).

It seems that the instability problem in the rectifier mode can be avoided if the modulation index is limited to or below m=0.95, so that the duty cycles of the short vectors are sufficiently large.

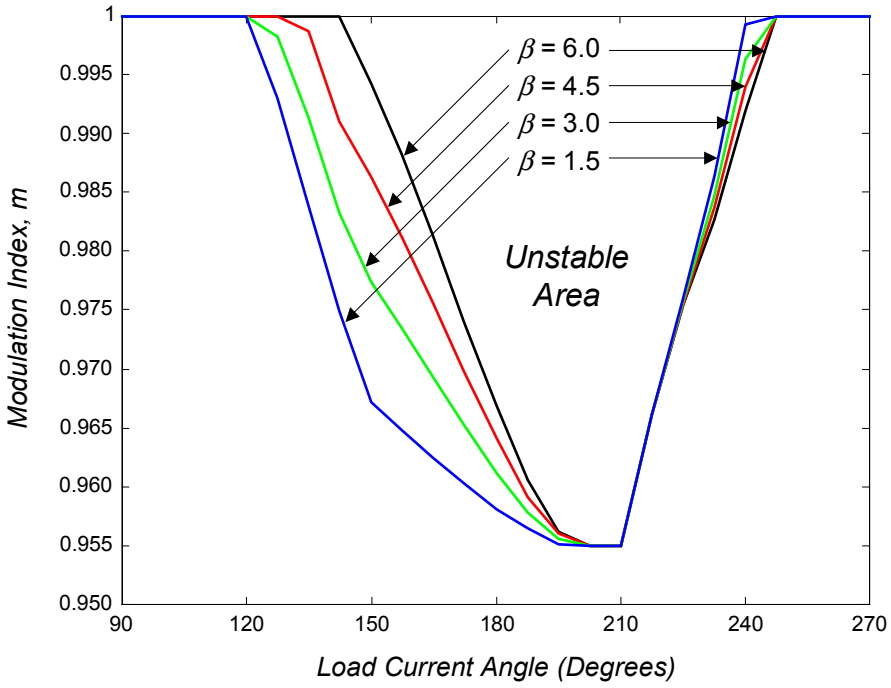


Fig. 5.8. *Stability limits of feedforward modulation in the rectifier operation mode.*

5.3.4. Experimental Results

The feedforward modulation algorithm has been programmed in the 32-bit floating-point DSP (Sharc ADSP 21062) with 25-ns instruction processing time of the SMES system. The algorithm requires less than 6 μs to be processed, only 50% more than the processing time required for noncompensated NTV modulation exposed in Chapter 3.

Fig. 5.9 shows the connection of the converter used for the experimental results. An asynchronous motor is used as a load, and the voltages of the DC-link capacitors are forced to have a permanent voltage imbalance by means of two DC power supplies. The upper one is adjusted to 60 V and the lower one to 10 V. Fig. 5.10 shows the voltages of the two DC-link capacitors, a low-pass-filtered line-to-line output voltage and an output phase current. When the NP connection is released, the modulation itself controls the voltage balance. As the selection of the dual vectors is properly made, the balance is achieved. The line-to-line output voltage and the output current are not affected during this dynamic process, thanks to the feedforward modulation.

In Figs. 5.11 and 5.12, the total DC-link voltage is 60 V, the modulation index m=0.95, and the fundamental output frequency is 10 Hz. This low frequency is

defined in order to achieve significant NP voltage oscillation (v_{C1}). The RMS output phase current in these conditions is I_{RMS}=10 A, with angle φ=-35°. The line-to-line output voltages shown in these figures are also refined by a first-order low-pass filter. These voltages have low-frequency distortion when the feedforward modulation is not used (Fig. 5.11), whereas the waveforms are practically sinusoidal when it is applied (Fig. 5.12). These experimental results are also verified by simulations.

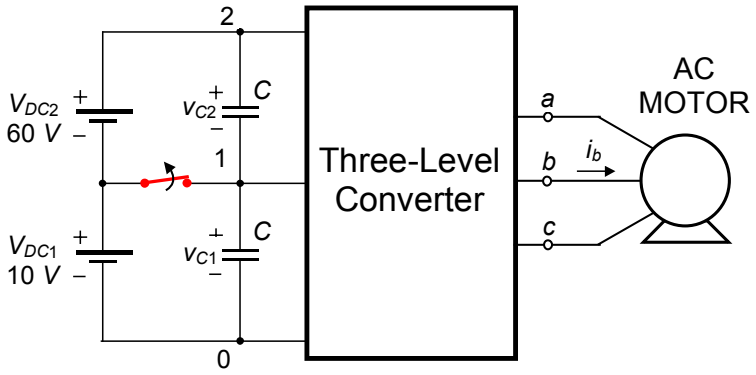
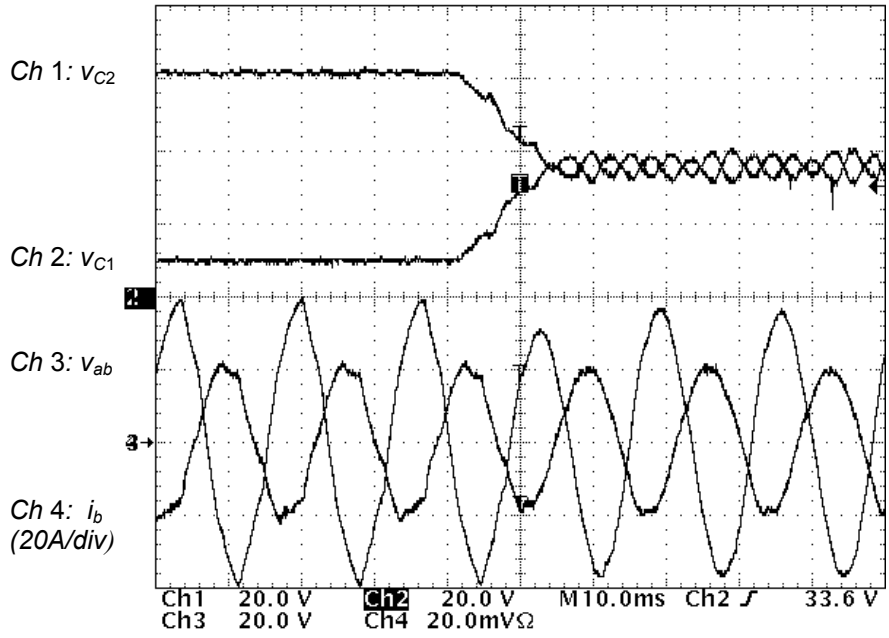
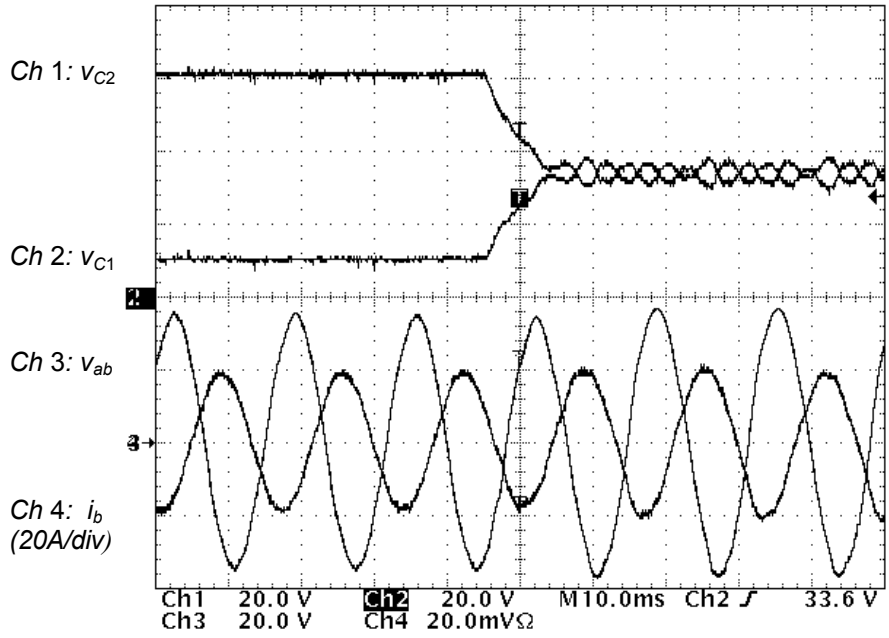


Fig. 5.9. *Connection used for the experimental results.*



(a)



(b)

Fig. 5.10. *DC-link voltages (v_{C1} and v_{C2}), filtered line-to-line voltage (v_{ab}) and output phase current (i_b): (a) no compensation, and (b) with feedforward modulation.*

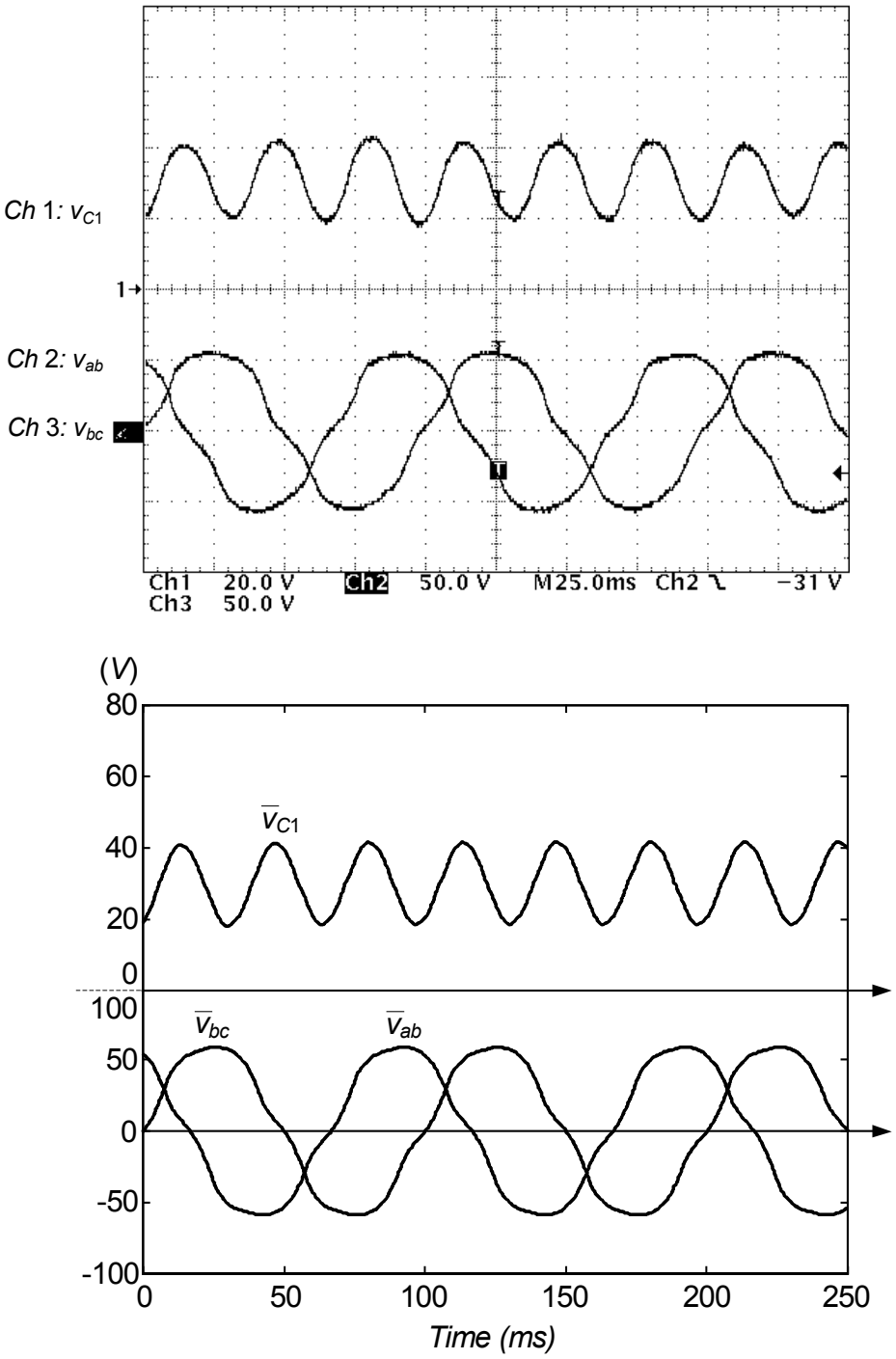


Fig. 5.11. *Experimental and simulated results with significant NP voltage ripple for the noncompensated modulation.*

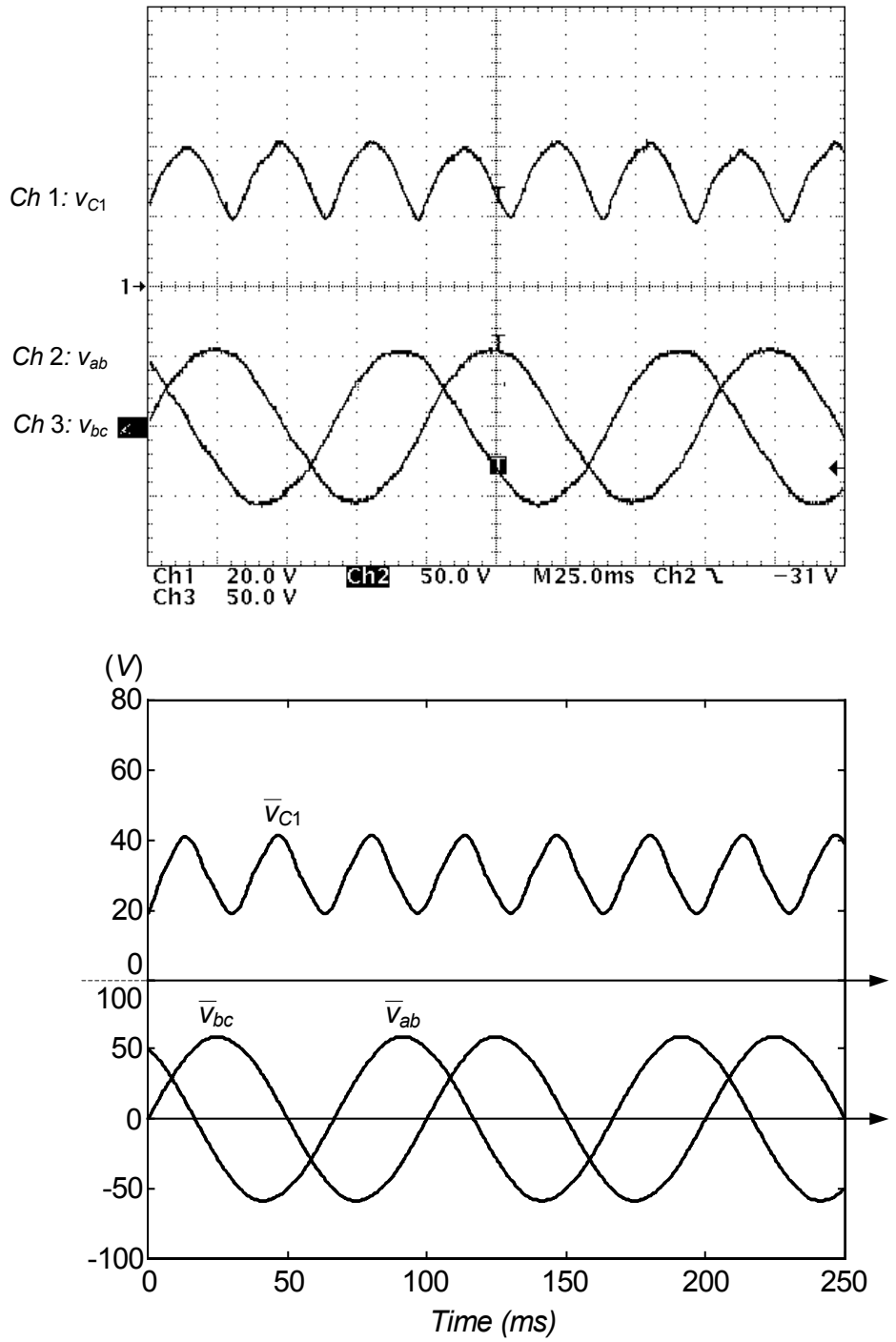


Fig. 5.12. *Experimental and simulated results with significant NP voltage ripple for the feedforward modulation.*

5.4. Conclusions of the Chapter

Using the feedforward SV-PWM method proposed in this chapter, the operating area for the NPC three-level converter can be extended to deep modulation indices and low-power-factor loads while avoiding any low-frequency distortion at the output voltages. Thus, the third-harmonic oscillation in the NP voltage, which appears in those conditions, no longer affects the output voltages and currents. Additionally, no other reason for imbalance in the NP voltage will affect the output voltages when the feedforward modulation is applied. Furthermore, the whole modulation process can be implemented in a DSP operating in real time because it is mainly based on comparison operations and products. As this modulation algorithm requires short processing time, it has been successfully applied in the SMES converter operating at 20-kHz switching frequency.

Since the imbalance in the NP does not affect the output variables, the value of the DC-link capacitors can be greatly reduced. However, as the amplitude of that oscillation increases, there is a corresponding increase in the maximum voltage that the devices and the capacitors themselves must support, and so there is a tradeoff in the selection of the values of the capacitors.

When the system operates as a rectifier with feedforward modulation, some NP voltage offset appears, which can degenerate into instability. The origin of this problem is justified and a solution is proposed, based on limiting the maximum modulation index for those operating conditions.