Universitat Autònoma de Barcelona

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September 2018

Doctoral Thesis

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CERTIFY

that **Mengdi Qian** carried out under their direction the research work entitled "Resistive switching in nanometric $BaTiO_3$ ferroelectric junctions". This work has been developed within a PhD program in Materials Science at the Universitat Autònoma de Barcelona at the department of physics.
For that record they sign the certificate.

Bellaterra, September 2018

Prof. Josep Fontcuberta Griñó	Dr. Ignasi Fina Martínez	Prof. Javier Rodríguez Viejo

Acknowledgements

So many people have provided me with assistance, guidance and support during my PhD. First, I am greatly indebted to Prof. Josep Fontcuberta and Dr. Ignasi Fina for supervising this thesis, for their support during the last four years and for our fruitful discussions. Thanks to Prof. Josep Fontcuberta, for introducing me to the field of oxides and your motivating. Your broad interest, ranging from fundamental physics and even industry-ready applications, encouraged myself to look for inspiration in very different directions. Thanks to Dr. Ignasi Fina, for all the assistance of details in experimental methodology, data interpretation, preparation of scientific presentations and publications.

I am really grateful to everybody who took part in the fabrication of my samples. Without the work of Dr. Florencio Sánchez and Raul Solanas, no ferroelectrics would have formed on the substrates and the samples would not go into their final devices.

I express my sincere gratitude to Dr. Diego Gutiérrez, Dr. Fanmao Liu and Dr. Mateusz Ścigaj for guiding me at the first months with the experimental setups step by step.

I wish to express my special appreciation to all the valuable comments in group meeting during last four years organized by Dr. Gervasi Herranz. I also want to give my acknowledgements to Prof. Vladimir Laukhin, Prof. Vassil Skumryev, Dr. Ferran Macià, Dr. Jaume Gázquez, Dr. Blai Casals, for valuable discussion in my group meeting presentation.

I want to extend my gratitude to Rafael Cichelero, Mathieu Mirjolet, Yu Chen, Jike Lyu, Saúl Estandía and Milena Sulzbach for all assistances during these years and making me feel like home in the group.

I would also like to thank all colleagues at ICMAB, especial to Dr. Carlos Frontera and Dr. Elena Marchante for all the help of my life in Barcelona.

Great thanks go to China Scholarship Council (CSC) for financial support during my doctoral study.

On a personal note, I would like to express my deepest gratitude to my family who would be always at my side and support me to enrich my knowledge abroad.

Abstract

Ferroelectric capacitors consist of two metallic electrodes separated by a ferroelectric layer have great potential for memory and logic devices. Here, the ferroelectric character of the barrier should allow to build multilevel of memory with a response (resistance R) that can be dictated by its previous history (cycling voltage V). Previous applied voltage allow writing on the capacitor different resistance states. Naturally, the success of this approach base on the ability to build ferroelectric capacitor with large RS response at room temperature.

The ultimate goal of the present thesis is the study of the RS behavior of ferroelectric thin and ultrathin films. In particular, the different RS response depending on parameters such as ferroelectric layer thickness, writing time, amplitude and polarity, device temperature, and contact configuration. For that purpose, epitaxial $BaTiO_3$-based ferroelectric capacitors has been used and a complete set-up has been developed and it is documented in the present thesis.

In ultrathin $BaTiO_3$-based ferroelectric capacitors, electrons can tunnel across the ferroelectric barrier. In this case RS results from the different barrier height depending on ferroelectric polarization state. Although, it is assumed that the UP to DOWN switching process it is similar to the DOWN to UP, in tunneling barriers these different processes result in very different dynamics. The different dynamics consists on fast response for one sign of polarization reversal and slow for the other, which has been ascribed to the presence of imprint electric fields caused by the intrinsic device asymmetry.

Characterization of $BaTiO_3$-based ferroelectric capacitors, focusing on its dependence on ferroelectric barrier thickness (t = 3-110nm) has revealed that RS can change its magnitude and sign depending on the barrier thickness and writing protocol. Additional temperature-dependent measurements have been instrumental to obtain evidence of the presence of field-assisted ionic motion contributing to RS. It is argued that the relative balance between purely electronic and ionic diffusion processes, modulate the height of the interfacial Schottky barriers and consequently, are responsible of the observed variations of the magnitude and sign of electroresistance. In ultrathin films these processes are found to be negligible and modulation of the tunneling barrier (purely electronic) takes place.

Taking benefit of the understanding acquired during the elaboration of the presence work, tunneling ferroelectric capacitors have been used to implement a Complementary Resistive Switch (CRS) device. CRS has been developed to overcome the sneak current path problem of passive memory arrays, which reveal's opportunities for higher density nanocrossbar arrays. By using a simple arrangement of ferroelectric tunnel junctions, we implemented the CRS functionality that allows effectively writing and reading binary states of identically large resistance state in the unbiased state. Moreover, it is experimentally demonstrated that this arrangement has significant advantages in power saving, and it is discussed on the basis of the obtained results that the possible bottlenecks that this functionality might show.

Resumen

Los condensadores ferroeléctricos están formados por dos electrodos metálicos separados por una capa ferroeléctrica, y tienen un gran potencial para dispositivos lógicos y memorias. El carácter ferroeléctrico de la barrera permite la aparición de memoria multinivel con una respuesta (resistencia R) que puede venir determinada por su historia (). El voltaje aplicado previamente permite escribir sobre el condensador distintos estados resistivos. Naturalmente, el éxito de este enfoque depende de la habilidad para fabricar condensadores ferroeléctricos con una gran respuesta RS a temperatura ambiente.

El objetivo principal de esta tesis es el estudio del comportamiento RS de capas ferroeléctricas delgadas y ultradelgadas. En particular la distinta respuesta RS que tiene lugar dependiendo del espesor de las capas ferroeléctricas, el tiempo de escritura, amplitud y signo, temperatura y configuración de los contactos. Para ello se han utilizado condensadores ferroeléctricos basados en $BaTiO_3$ epitaxial y se ha desarrollado una configuración completa, presentado en este documento.

En condensadores ferroeléctricos basados en $BaTiO_3$ ultrafino los electrones pueden atravesar la barrera mediante efecto túnel. En este caso el efecto de RS se origina como consecuencia de la dependencia de altura de la barrera con el estado de polarización ferroeléctrico. A pesar de que el proceso de "switching" "UP to DOWN" es similar al proceso inverso ("DOWN to UP"), en barreras con efecto túnel estos procesos diferentes generan dinámicas muy distintas. Las diferentes dinámicas consisten en una respuesta rápida para la inversión de la polarización de un signo, y una respuesta lenta para la inversión de polarización de signo contrario. Esto ha sido asociado a la presencia de campos eléctricos ("imprint") causados por la asimetría intrínseca del dispositivo.

La caracterización de los condensadores ferroeléctricos de $BaTiO_3$, atendiendo al espesor de la barrera ferroeléctrica (t=3-110nm), muestra que el RS puede variar de magnitud y signo en función del espesor de la barrera y del protocolo de escritura.

Medidas adicionales de temperatura han sido necesarias para evidenciar la existencia de una contribución al RS proveniente de un desplazamiento iónico asistido por campo eléctrico. Se

discute cómo el balance relativo entre los procesos de difusión puramente electrónica e iónica modula la altura de la barrera Schottky y consecuentemente cómo son responsables de las variaciones observadas en la magnitud y signo de la electrorresistencia. En capas ultradelgadas se encuentra que estos procesos son despreciables y una modulación de la barrera de efecto túnel (puramente electrónica) tiene lugar.

Aprovechando el conocimiento adquirido a lo largo de la elaboración del presente trabajo, se han utilizado condensadores ferroeléctricos de efecto túnel para implementar un dispositivo CRS ("Complementary Resistive Switching"). El CRS ha sido desarrollado para resolver el problema de corriente de "sneak" de arrays de memoria pasivos, lo cual abre oportunidades para conseguir arrays nanocrossbar de mayor densidad. Mediante el uso de una configuración simple de uniones túnel ferroeléctricas hemos implementado la funcionalidad del CRS que permite la lectura y escritura de estados binarios de idéntico estado de alta resistencia en el estado sin "bias". Además, se demuestra experimentalmente que esta configuración aporta ventajas notables en cuanto al ahorro energético, y se discute sobre los resultados obtenidos los posibles obstáculos que esta funcionalidad podría enfrentar.

Objectives and structure of the thesis

Deep understanding of RS behavior and physical mechanism underneath in ferroelectric capacitors is necessary to face their integration in novel functional devices, such as, the building blocks for the envisaged neuromorphic computers.

Chapter 1

This thesis starts by summarizing the basic properties of ferroelectrics, the ideas and the physic features of the ferroelectric capacitors. We address its fundamental, properties and try to understand the electrical transport through the ferroelectric barrier. The mechanisms of RS are reviewed.

Chapter 2

This chapter contains a brief description of the experimental methods used in the context of the present thesis. Contains sections devoted to sample fabrication, electrical measurement configurations, dielectric, ferroelectric, and RS characterization as well as a detailed description of a new experimental set-up.

Chapter 3

This chapter describes the results in the characterization of RS dynamics in BaTiO3 tunnel junctions (FTJs). We will use I (V) loops to analyze in detail the ferroelectric switching dynamics and to determine the ferroelectric ER of tunnel barrier. Finally, we will describe the mechanisms of the physics behand.

Chapter 4

In chapter 4 we explore the possible occurrence of electronic and ionic contribution to ER in non-tunnel ferroelectric capacitor. We show the time dependence of ER and the retention behavior. We explore the temperature dependence and the mechanisms of ER in thick ferroelectric capacitor.

Chapter 5

We investigate RS of a particular arrangement of FTJs in which two FTJs are connected in series. It will be shown that this device may have some advantages for data storage.

List of publications

[1] M. Qian, I. Fina, F. Sánchez, and J. Fontcuberta, "Synergetic Electronic and Ionic Contributions to Electroresistance in Ferroelectric Capacitors," *Adv. Electron. Mater.*, Submitted, 2018.

[2] M. Qian, I. Fina, F. Sánchez, and J. Fontcuberta, "Asymmetric Resistive Switching Dynamics in BaTiO3 Tunnel Junctions," *Adv. Electron. Mater.*, Submitted, 2018.

[3] G. Radaelli, D. Gutiérrez, M. Qian, I. Fina, F. Sánchez, L. Baldrati, J. Heidler, C. Piamonteze, R. Bertacco, and J. Fontcuberta, "Strain-Controlled Responsiveness of Slave Half-Doped Manganite $La_{0.5}Sr_{0.5}MnO_3$ Layers Inserted in $BaTiO_3$ Ferroelectric Tunnel Junctions," *Adv. Electron. Mater.*, vol. 2, p. 1600368, 2016.

List of communications

4-6. June 2018
ALBA Synchrotron
QUANTY, CRISPY and CTM4XAS Workshop

14-17, March 2018
Sant Feliu de Guíxols, Barcelona
Summer school
Technologies for Oxide Electronics Training School

12-14, March 2018
Sant Feliu de Guíxols, Barcelona
Cost Towards Oxide-Based Electronics Closing Meeting (TO-BE final meeting)
Poster presentation: "Electroresistance in ferroelectric capacitors: Ions come to play"

7-8, November 2017
Instituto de Ciencia de Material de Barcelona (ICMAB-CSIC), Barcelona
3rd scientific meeting of BNC-b PhD Students in Nanoscience
Poster contribution: "Different Contributions in Electroresistance of $BaTiO_3$ Films"

10-12, July 2017
Sant Feliu de Guíxols, Barcelona
Advanced materials and nanotechnology for innovative electrical, electronic and magnetoelectronic devices (nanoselect 2017)
Oral presentation: "Different contributions in electroresistance of BaTiO3 films"

3-5, April 2017
Luxembourg Institute of Science and Technology,Luxembourg

Cost Towards Oxide-Based Electronics spring meeting (TO-BE spring meeting)
Oral presentation: “Reversing ON/OFF resistance states in BaTiO3 ferroelectric tunnel junctions: thickness and writing time dependencies”

28-30, September 2016
Ljubljana Slovenia
Cost Towards Oxide-Based Electronics fall meeting (TO-BE fall meeting)
Oral presentation: “Disentangling tunneling and non-tunneling contributions on electroresistance in $BaTiO_3$-based ferroelectric tunnel junctions”

8-10, June 2016
Sant Feliu de Guíxols, Barcelona
Research conference
Advanced materials and nanotechnology for innovative electrical, electronic and magnetoelectronic devices (nanoselect 2016)
Oral presentation: “Temperature dependence of electroresistance in ferroelectric tunnel junctions”

29-30, June. 2016
University of Autonoma of Barcelona, Barcelona
2rd scientific meeting of BNC-b PhD Students

12-24, Oct. 2015
Cargèse, France
Summer school
International School of Oxide Electronics (ISOE2015)

20-21, May. 2015
University of Autonoma of Barcelona, Barcelona
1st scientific meeting of BNC-b PhD Students

Poster contribution: “Tunnel junctions with adjustable ferroelectric barriers for large electroresistive response”

19, January 2015
Instituto de Ciencia de Material de Barcelona (ICMAB-CSIC), Barcelona
Workshop “AFM beyond imaging. Nanoscale characterization of functional materials” (AFM 2015)

Contents

Chapter 1 Introduction

The aim of this work is to investigate the electron transport through metal–ferroelectric–metal (MFM) junctions with thin or thick barriers in order to determine its dependence on the polarization state of the barrier. Following this aim, I will describe the basic properties of the ferroelectrics and the mechanisms of charge transport through the barriers. The origin of the observed resistive switching effect is also discussed.

1.1 Ferroelectrics

The ferroelectrics are materials that have a spontaneous electric polarization that can be switched by applying an external electric field.[1,2] They are one of the broad class of dielectrics-insulating solids that exhibit an electric polarization under application of an external electric field, breaking the space symmetry of the material. All dielectrics with a non-centrosymmetric structure display piezoelectricity: mechanical stress that leads to the separation of opposite charges at the material surface. This interconvertible behavior was first discovered by Pierre and Jacques Curie in 1880 in crystals of Rochelle salt.[3,4] The other way around, through the inverse piezoelectric effect, an externally applied electric field induces a deformation of these materials.

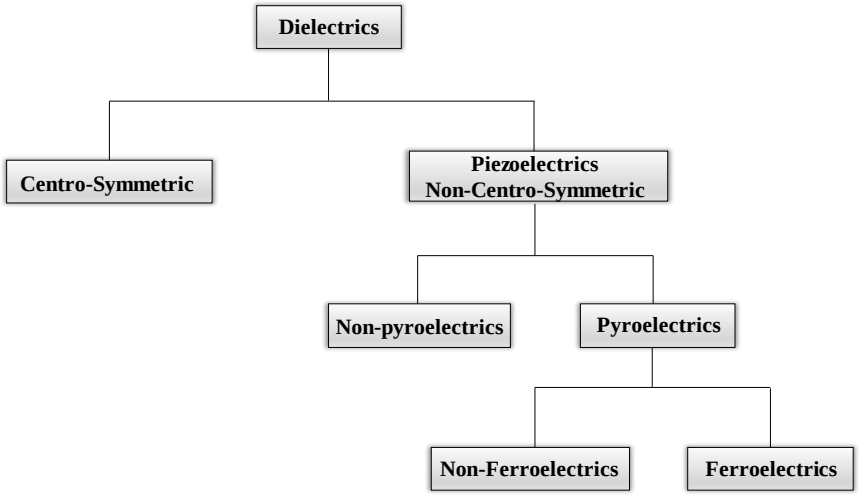


Figure 1.1 *The hierarchy of the different dielectric classes.*

A subset of piezoelectric materials possesses a unique axis of symmetry which makes its members polar and leads to a spontaneous electric polarization. The change in temperature modifies the positions of the atoms slightly within the crystal structure, such that the polarization of the material changes and so these materials are called pyroelectrics. Finally, the spontaneous polarization of certain pyroelectrics can be switched under application of an external electric field and remains non-zero on removal of the field. These materials are called ferroelectrics. First experiment evidence of ferroelectricity was discovered in 1920 by Joseph Valasek during experiments on Rochelle salts.[5] As a summary, the hierarchy of the different dielectric classes is depicted in Figure 1.1.

The distinguishing feature of ferroelectric materials is that the spontaneous polarization can be reversed by a suitably strong applied electric field in the opposite direction; the polarization is therefore dependent not only on the current electric field but also on its history, yielding a hysteresis loop. The hysteresis of the polarization P as a function of the electric field E is shown in Figure 1.2 for polydomain samples. Starting from the origin 0, the material is poled under application of an electric field E so that the polarization P increase. At high fields, its value goes into saturation. Once the electric field is reduced to zero, a ferroelectric material shows a finite remnant polarization P_r. It is identical to the spontaneous polarization for single domain samples. To reverse the polarization, an electric field of opposite polarity is needed. At some value $E=-E_C$ (coercive field) the polarization reduces to zero and subsequent increase

of the opposite field brings the sample to saturation in the opposite direction. Typically, materials demonstrate ferroelectricity only below a certain phase transition temperature, called the Curie temperature (T_C) and are paraelectric above this temperature.

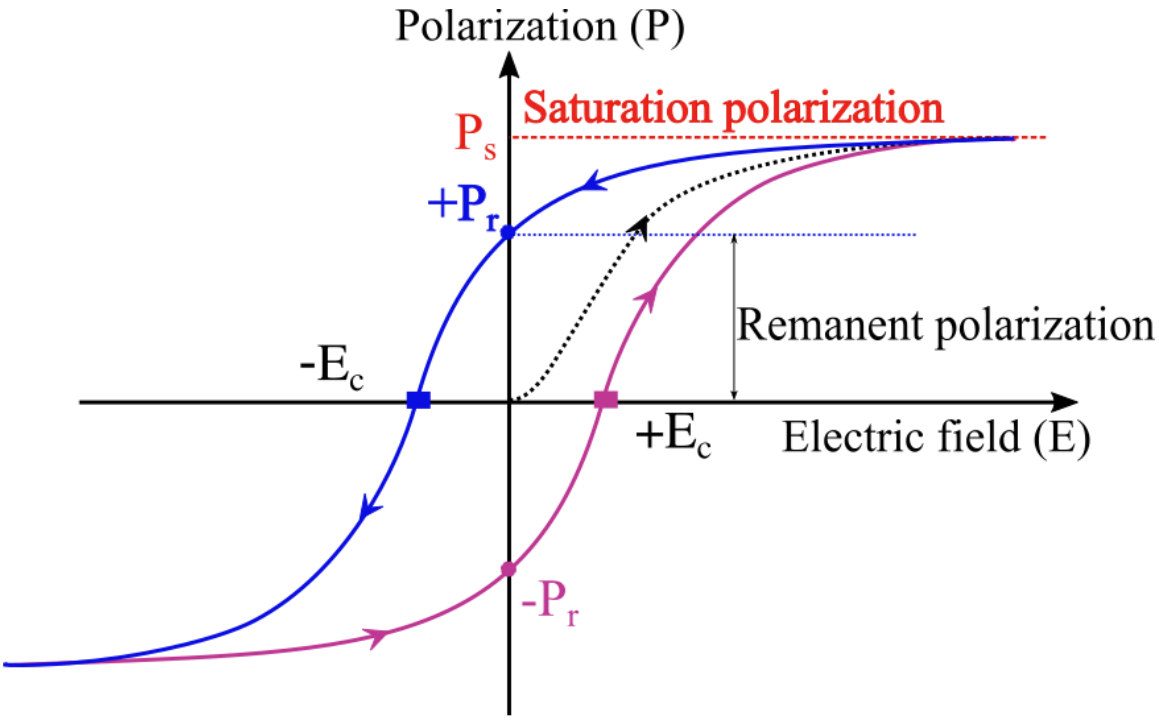


Figure 1.2 *Macroscopic ferroelectric hysteresis loop: evolution of the overall polarization under an electric field.*

1.2 $BaTiO_3$ basic properties

The ferroelectric material used in this thesis is BTO which is a perovskite oxide material (ABO_3). BTO is one of the most studied ferroelectric compounds due to its good ferroelectric properties. At room temperature bulk BTO is tetragonal and presents an out-of-plane $c_0 = 4.038$ *Å* and in plane lattice parameter $a_0 = 3.994$ *Å* (see Figure 1.3). The polarization can be switched in two different orientations along the c axis with a remanent polarization of 26 $\mu C/cm^2$. Strain is imposed when BTO is grown epitaxially on a substrate (i.e. STO). The coupling between strain and polarization in perovskite oxides is known to be very strong, for instance, an enhancement of remnant polarization has been observed in BTO grown on $GaScO_3$ and $DyScO_3$.[6] Bulk BTO shows three phase transitions depending on the temperature. It is cubic at

the temperatures above 120 °*C*, this is a paraelectric phase (i.e. without a spontaneous dipole moment). Below this temperature the arrangement of atoms changes into a lower symmetry (the mentioned tetragonal phase) and the material becomes ferroelectric with a given direction of the polar axis (tetragonal axis). At ≈ 0 °*C* the structure changes to orthorhombic (*P* || [011]) and at ≈ -90 °C it changes again to rhombohedral (P || [111]).

In thin film form BTO is an excellent material to study due to the fact that it can be grown epitaxially on top of a suitable substrate.[7]

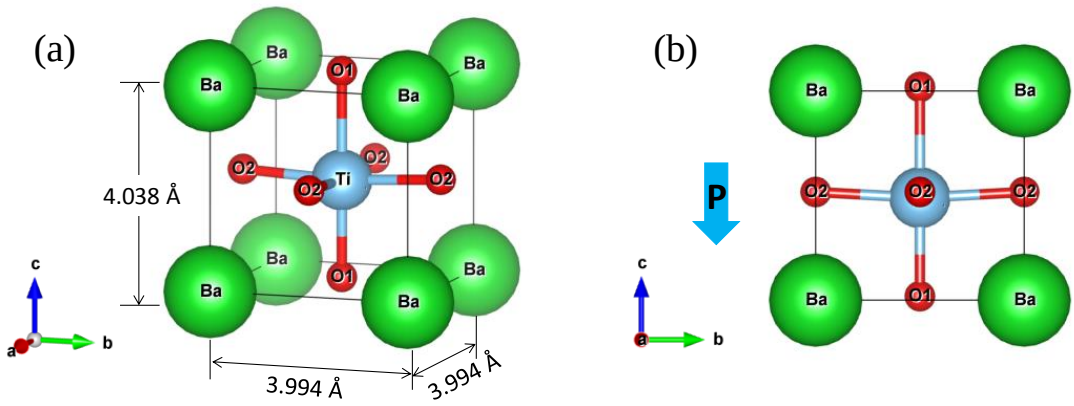


Figure 1.3 *(a) The perovskite structure of a single unit cell of Barium Titanate (BTO). (b) BTO sketch of Ti ion displacement along c axis.*

1.3 Ferroelectric capacitor

A ferroelectric capacitor has a simple three-layer structure: Metal/Ferroelectric/Metal (M/FE/M), as shown in Figure 1.4. The polarization of the ferroelectric thin film points to either one or the other electrode and can be switched by an electric field under application of a voltage across the barrier.[8] The thickness of the ferroelectric layer is a key factor to classify the capacitor in two groups: a) ferroelectric tunnel junctions (FTJs), an ultrathin ferroelectric layer that is sandwiched between two electrodes that allow direct tunneling transport and b) non-tunneling ferroelectric capacitor incorporating thicker ferroelectric films where the transport mechanisms can be grouped in two major categories: interface-controlled mechanisms based on Schottky emission and bulk-controlled mechanisms such as, space-

charge-limited currents, Pool-Frenkel emission, ionic conduction, or a combination of them. The electric transport mechanisms will be explained in the following.

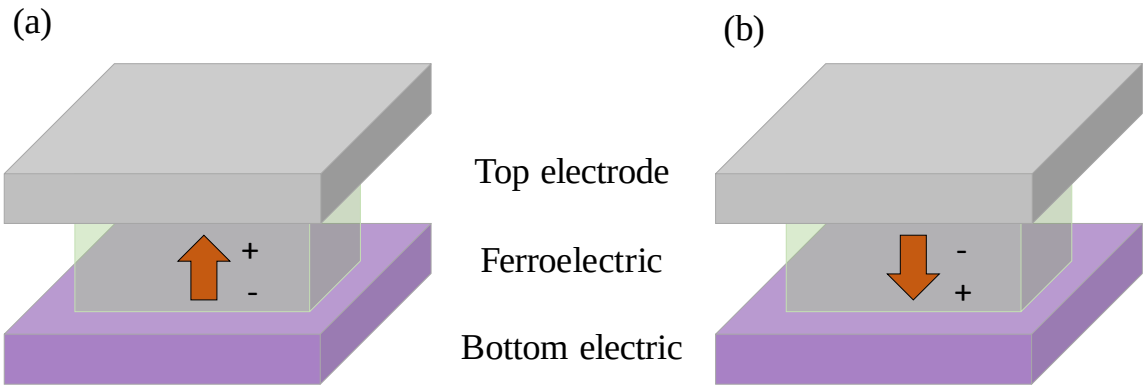


Figure 1.4 *Basic schematic structure of a ferroelectric capacitor. The polarization points either towards the top ↑ (a) or towards the bottom ↓ electrode (b).*

Regarding ultrathin ferroelectric capacitors, recent progress allows the deposition of epitaxial ferroelectric films as thin as a few monolayers. This fact permitted the development of ferroelectric tunnel junctions (FTJs) with high quality ultrathin ferroelectric barriers, allowing electron tunneling. Thus, electric-field controlled polarization reversal makes this system a potential candidate for its use in memory applications, combining fast switching,[9] large contrast,[10,11] good retention, and low fatigue.[12] Moreover, partial polarization switching allowed in ferroelectrics by the formation of different domains can allow intermediate resistance states emulating a memristive device.[10,13] These properties make FTJs a promising candidate to be used as a memory element and/or artificial synapses in neuromorphic architectures.[14] Next, I am going to talk about the transport property in FTJ.

1.3.1 Electrical transport mechanisms through ultrathin insulators

While ferroelectrics are insulating by definition, for very thin ferroelectric films with thickness of some nanometer, direct tunneling has been observed.[15,16] Current can flow between the two electrodes by the tunneling effect. In the simplest approximation tunneling resistance exponentially increases with barrier height and width.

Based on the model of W. F. Brinkman et al.[17] and using the Wentzel-Kramers-Brillouin (WKB) approximation, the current density j_{DT} is given by Gruverman et al. for a trapezoidal potential barrier (Figure 1.5) under an applied voltage V shown in the following:[18]

$$j_{DT} \cong C \frac{\exp\left\{\alpha(V)\left[\left(\Phi_2 - \frac{eV}{2}\right)^{3/2} - \left(\Phi_1 + \frac{eV}{2}\right)^{3/2}\right]\right\}}{\alpha^2(V)\left[\left(\Phi_2 - \frac{eV}{2}\right)^{1/2} - \left(\Phi_1 + \frac{eV}{2}\right)^{1/2}\right]^2} \times \sinh\left\{\frac{3}{2}\alpha(V)\left[\left(\Phi_2 - \frac{eV}{2}\right)^{1/2} - \left(\Phi_1 + \frac{eV}{2}\right)^{1/2}\right]\frac{eV}{2}\right\} \qquad (1.1)$$

Where $C = -(4em^*m_e)/(9\pi^2\hbar^3)$ and $\alpha(V) \equiv [4d(2m^*m_e)^{1/2}]/[3\hbar(\Phi_1 + eV - \Phi_2)]$, m^* is the relative effective mass of the tunneling charge carriers. The constants used are the electron charge e, the electron mass m_e, and the reduced Planck constant $\hbar$.[17,18]

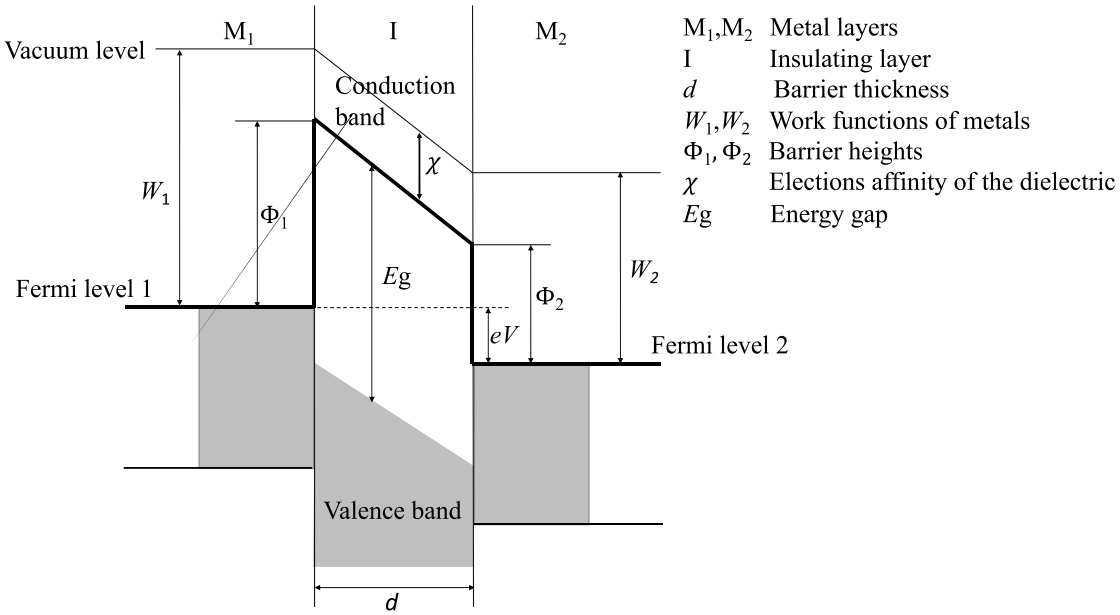


Figure 1.5 *Energy model for a biased metal-insulator-metal tunnel junction.*[19]

Flowler-Nordheim tunneling (FNT) is basically the same phenomena as direct tunneling but dominates at higher voltage and mitght occur in thicker films. When the voltage is applied at M2 and exceeds the barrier height at the interface of the electrode 2, as shown in the Figure

V> Φ_2/e, the effective tunneling barrier width is smaller (Figure 1.6). Therefore, tunneling probability increases.

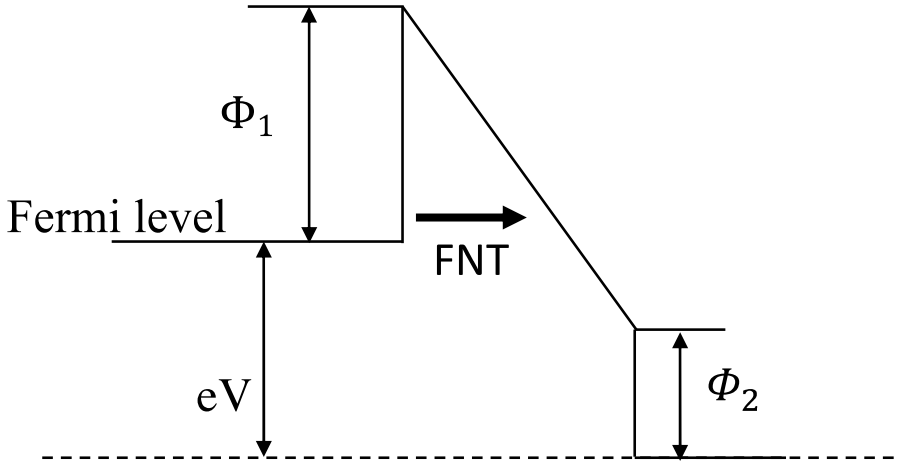


Figure 1.6 *Sketch of energy potential of Fowler-Nordheim tunneling (FNT) under an applied voltage V> Φ_2/e.*

1.3.2 Electrical transport mechanisms through non-tunneling ferroelectric capacitor

1.3.2.1 Schottky emission

Traditionally, ferroelectrics have been regarded as insulators, but this view fails when defects introduce internal charges and it would be more appropriate to treat them as semiconductors with a fairly large band gap.[20] When metal makes contact with a ferroelectric, a Schottky barrier is formed at the metal-semiconductor interface. This barrier is responsible for controlling the current conduction. For a metal with a high work function (W) and n-type semiconductor, when they are put together, the Fermi energy of both materials is aligned, and the formation of the barrier is established. The energy of the barrier Φ_B is roughly given by

$$\Phi_B = W - \chi \quad (1.4)$$

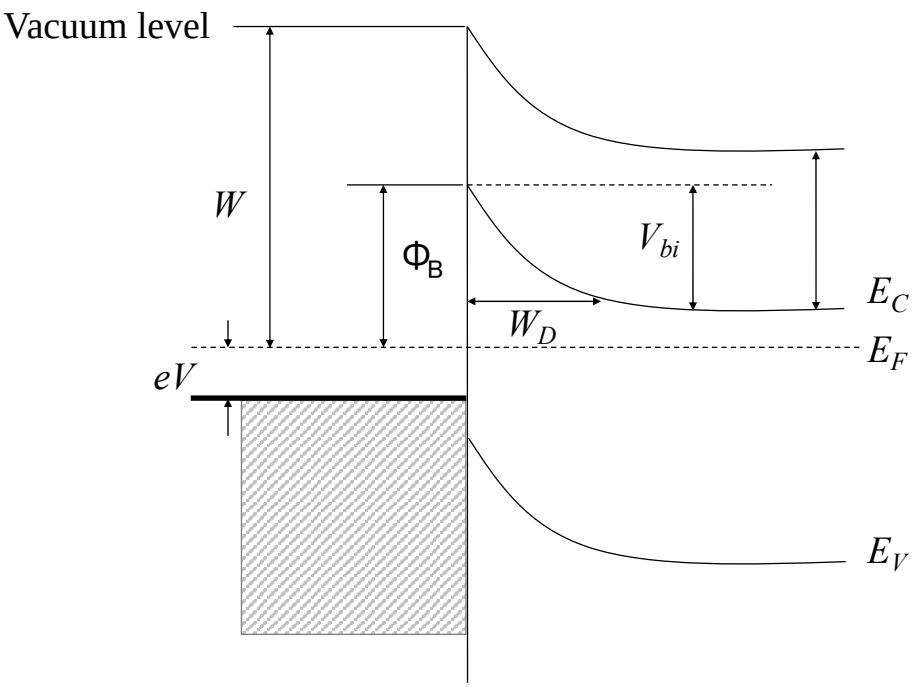


Figure 1.7 *Band diagram for Schottky barrier between metal-semiconductor.*

where χ is the electron affinity of the semiconductor. The alignment of the Fermi energy levels is accompanied by the formation of a depletion layer (W_D) in the semiconductor close to the interface

$$W_D = \sqrt{\frac{2\varepsilon}{qN_D}(V_{bi} - V - k_B T/e)} \tag{1.5}$$

Where ε is the dielectric constant of the semiconductor, qN_D is density charge in the depletion region, V_{bi} is the built voltage (see the Figure 1.7) and $k_B T$ is the thermal energy. The depletion layer produces a capacitance C_D at the interface and it´s given by

$$C_D = \sqrt{\frac{e\varepsilon N_D}{2(V_{bi} - V - k_B T/e)}} \tag{1.6}$$

When a positive bias is applied to the metal, then the equilibrium between the electron in the metal and electrons in the semiconductor is broken. The equation for the current density J is given by

$$J = J_0 \left[\exp\left(\frac{eV}{\eta k_B T}\right) - 1\right] \tag{1.7}$$

For the ideal case of a perfect contact between the metal and the semiconductor η = 1. When the metal and the semiconductor are separated by a thin interfacial insulating layer (intentional or nonintentional) introduced before metal deposition, η increases due to the thickness of the oxide layer and interface.[21]

1.3.2.2 Space-charge-limited emission

Space-Charge-Limited (SCL) emission is a well-known transport mechanism that is often used to explain conduction of an insulator or a semiconductor. Under an applied bias, the free carrier concentration is increased due to the injected carriers in the region of a junction formed by different materials. When the injected carrier concentration is larger than its thermal equilibrium value, the space-charge effect is said to occur. The injected carriers thus control the space charge and the electric-field profile. This results in a feedback mechanism where the field drives the current.[21]

1.4 Resistive Switching mechanisms in ferroelectric capacitor

Ferroelectric memristive devices are based on a very simple capacitor-like structure.[22] Biasing electrically the electrodes to polarize the ferroelectric layer can produce a change in the total device resistance between (at least) two states. These resistance changes are denoted as electroresistance (ER)[16,23] that is defined as the relative change between the two resistance states for both polarization orientations (here defined as pointing downwards or the upwards).

$$ER = \frac{(R_{P\downarrow} - R_{P\uparrow})}{R_{P\uparrow}} \times 100\% \quad (1.8)$$

If $R_{P\downarrow}$ corresponds to the high-resistance state (HRS, OFF-state) and $R_{P\uparrow}$ corresponds to the low-resistance state (LRS, on-state), the ER > 0. As the large resistance changes occurring in FTJs result in very high values (>10^4%)[8] when given in percent, the ratio between the high resistance state (HRS or R_{off}) and low resistance state (LRS or R_{on}) is often used in some work as well.

1.4.1 Resistive switching mechanisms in ferroelectric tunneling junctions

In the following, I present several possible mechanisms that contribute to RS. The first mechanism is the modification of the electrostatic potential across the junction, the second is the interface bonding strength and the third mechanism is the strain associated to the piezoelectric response.

1.4.1.1 Electrostatic effects

Electronic reconstruction occurs in the electronic band diagram of a ferroelectric junction if polarization is reversed. In particular, height and width of the effective insulating barrier can change. In the case, due to tunneling resistance exponentially depends on the height and width of the barrier, the polarization switching results in large changes on resistance state.[16,23] This has been sketched in Figure 1.8, where the band diagrams for a M1/ferroelectric/M2 structure for two opposite polarization states is sketched.

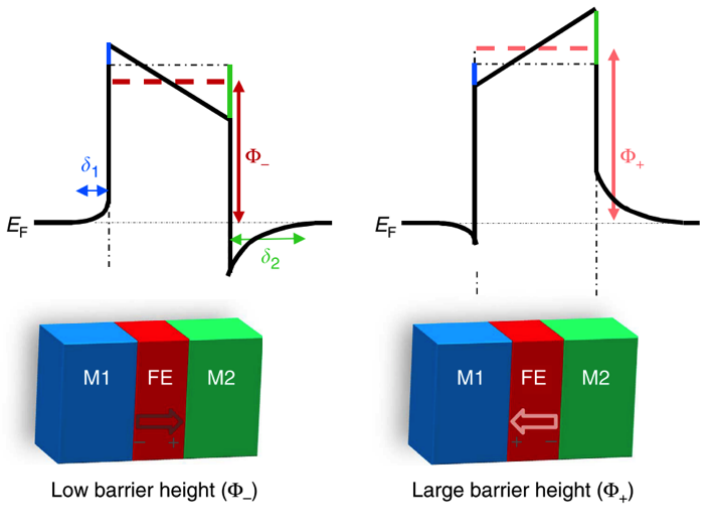


Figure 1.8 *Energy barrier profiles: the different screening lengths cause different changes in the interfacial energy barriers across the metal 1 (M1)/ferroelectric/metal 2 (M2) heterostructure for two orientations (right and left) of the ferroelectric polarization (P). As a consequence, the average barrier height changes (between Φ_- and Φ_+), leading to a change in the tunneling resistance. [Adapted from ref.* [8]*]*

As mentioned, owing to electrostatic effects, the average barrier height is small (Φ_-) or large (Φ_+), when P points to the right or to the left, respectively. Therefore, in eq. (1.1), which models a trapezoidal tunneling barrier, Φ_1 and Φ_2 values will be different for $P\downarrow$ and $P\uparrow$.

Conceded the three different transport mechanisms presented in section 1.3.1, in ref.[24], D. Pantel & M. Alexe have calculated and presented the respective contributions to the total current density in an BTO based FTJ for the two reversal polarization directions as shown in Figure 1.10.[24]

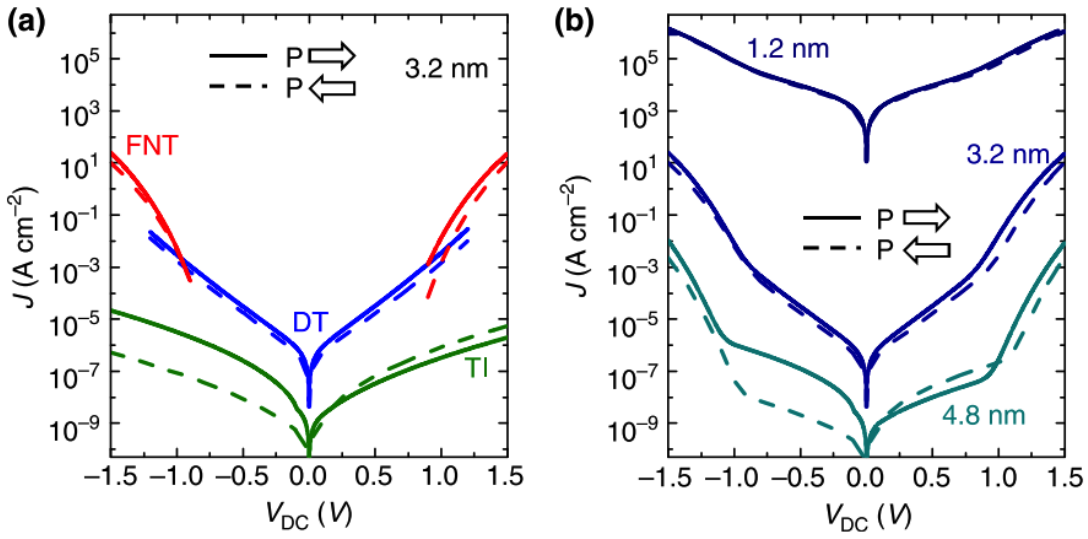


Figure 1.9 *Theoretical tunneling current densities through an FTJ with contributions from direct tunneling (DT), Fowler–Nordheim tunneling (FNT), and thermionic injection (TI) for both polarization directions of the ferroelectric barrier. (a) Current density (J) versus voltage (V) contributions from the three conduction mechanisms through a 3.2 nm ferroelectric. (b) Thickness dependence of the total current density. [Adapted from ref.* [8]*]*

Figure 1.9 (a) clearly shows that direct tunneling dominates at small voltage region then FNT becomes more predominate at higher voltage biased. While by increasing the barrier thickness, TI rules for conduction shown in the green line in Figure 1.9 (b).

1.4.1.2 Atomistic interface effects

Precedent works have shown by combination of first principle calculations and experimental results that the ferroelectric barrier can change as a result of the change of the electronic state of the ferroelectric/metal interface. The ionic displacements induced in the ferroelectric materials upon switching account for the mentioned change due to the alteration of bonding distances.[25,26]

1.4.1.3 Piezoelectric strain effects

As all ferroelectric materials are also piezoelectric, they will exhibit the inverse piezoelectric effect under the application of an external electric field. This can result in a change in the thickness of the ferroelectric layer and therefore in a change in the tunneling barrier width[16]. In principle, this effect cancels out if opposite states of polarization are compared, since strain is an even function of the applied electric field in piezoelectric. However, in presence of extrinsic effects, depending on the direction of the ferroelectric polarization, a given electric field can lead to either compressive or tensile strain, i.e. to an increase or a decrease of the ferroelectric film thickness.

1.4.2 Resistive switching mechanisms in non-tunneling ferroelectric capacitors

Ferroelectric thicker capacitors showed ER with R_{off}/R_{on} ratios of up to 10^2.[27,28] The high resistances owing to the thick highly resistive ferroelectric layers limit their benefit for practical applications as the very low current densities are detrimental for the information read-out. In the following, we present several possible mechanisms contributing to the RS in thicker ferroelectric capacitor.

1.4.2.1 Ionic motion

In ferroelectric films, tunneling through the film is strongly suppressed when thickness increases. Other mechanisms based on defects (ionic or electronic) may contribute to the observed ER and they depend on the amplitude and direction of the applied electric field. These mechanism can be either the formation/rupture of conductive filaments (CF), closely related

to the density and migration behaviors of oxygen vacancies (V_o) or other defects[29,30], or modification of the Schottky barrier.

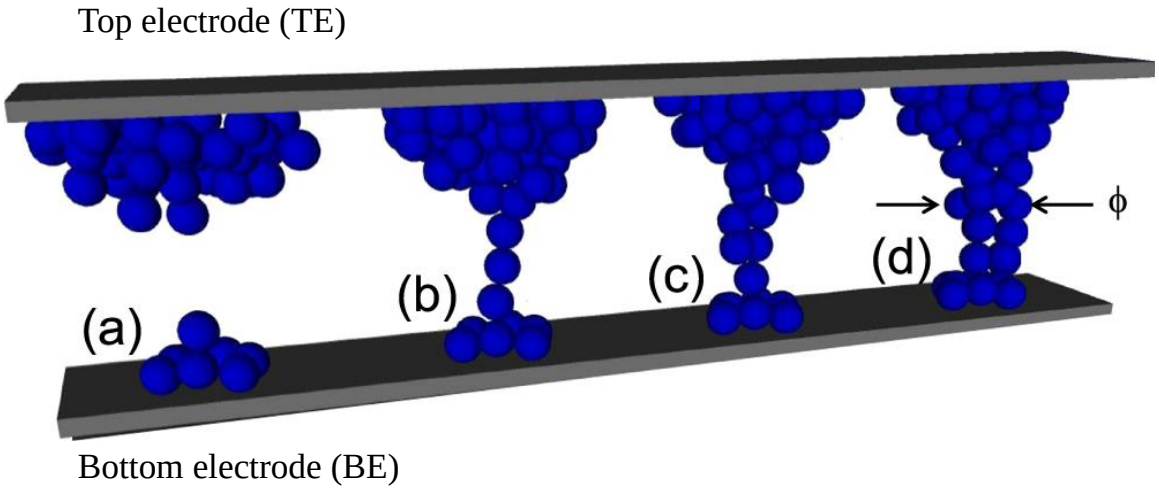


Figure 1.10 *A filament growth model for RS. The application of a positive voltage to the TE results in the migration of positively ionized defects from the reservoir on the (top electrode) TE side (a) toward the (bottom electrode) BE, thus resulting in the nucleation of the CF (b) and its growth at an increasing time (c), (d). The increase of the diameter of the CF ϕ thus results in the decreasing resistance observed during the set transition. [Adapted from ref.* [31]*]*

As a relevant example, Figure 1.10 shows the switching model for a conductive filaments (CF) device. Starting from a situation were filament is not formed (Figure 1.10 (a)), high resistance state is set (assuming that the matrix is less conductive than the filament). The application of a bias induces the migration of charged ions from the top/bottom electrode, which acts as a ions reservoir, along the CF direction. The current density and consequently the temperature increases at the CF. Ion migrations results in a CF increase (Figures 1.10 (b)–(d)) until filament connects both metals resulting in a LRS.

1.4.2.2 Modification of Schottky interface

RS can result from the modification of the Schlocky barrier formed at the ferroelectric/electrode interface if one of them shows semiconducting properties (Figure 1.11 (a)). [32–35] W_D stands for the width of the depleted region in the case of zero voltage applied on

the diode, and Φ for its height. In presence of polarization (pointing towards the Schlocky barrier, Figure 1.11 (b)), sheet of charge $+Q_P$ is located near the interface, in the depleted region. The positive surface charge is compensated by electrons that are attracted. This produces a decrease of the barrier width and height compared with the case where no polarization is present. If polarization points away from the barrier (Figure 1.11 (c)) the opposite situation holds. Different Schlocky barrier shapes will produce different conductivity, thus the presence of RS.

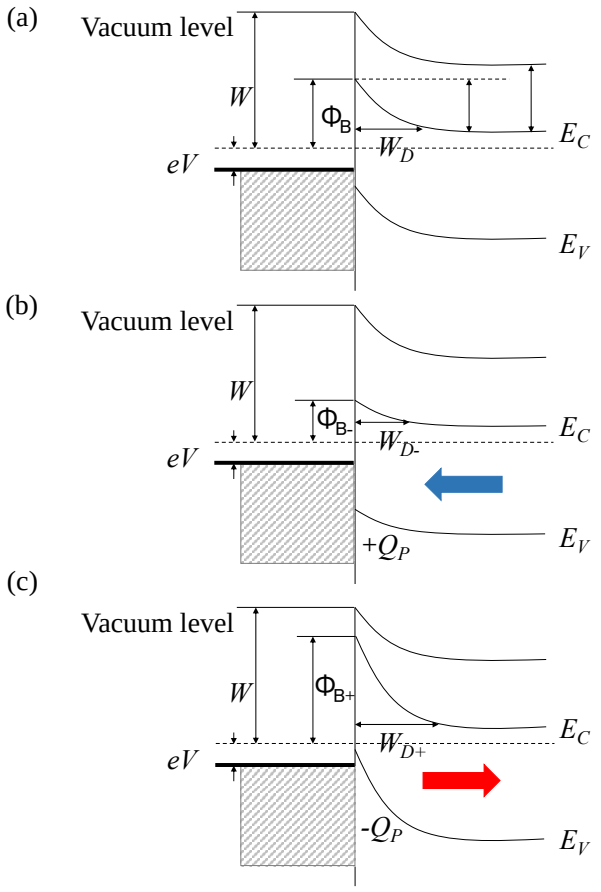


Figure 1.11 *Schematic band diagrams for: (a) Schottky barrier with no ferroelectric polarization; (b) Schottky barrier with polarization pointing to the left; and (c) Schottky barrier with polarization point to the right*

1.4.3 Introduction remarks

Overall, several different mechanisms may contribute to the RS of ferroelectric capacitors, and different mechanisms could be dominant in different materials systems.[36] This uncertainty is exacerbated by the great difficulty in characterizing the physical changes responsible for the electrical switching, because the active regions of the devices are extremely small and buried under a metal contact. Electric field and Joule heating generally coexist in all memristive switching, although their relative importance varies depending on the device stack, materials, electrical operation history and more.

The goal of this thesis is to contribute to the understanding of RS in BTO-based ferroelectric capacitors and its dependence of barrier thickness and writing and reading protocol.

Chapter 2 Experimental

2.1 Sample fabrication and structure

Plano-parallel capacitor is the most suitable geometry for the electrical measurement of polarization and the characterization of RS in bulk ceramics or thin films. The measured ferroelectric material of thickness t is embedded in between two electrodes with a defined area A, as depicted in Figure 2.1.

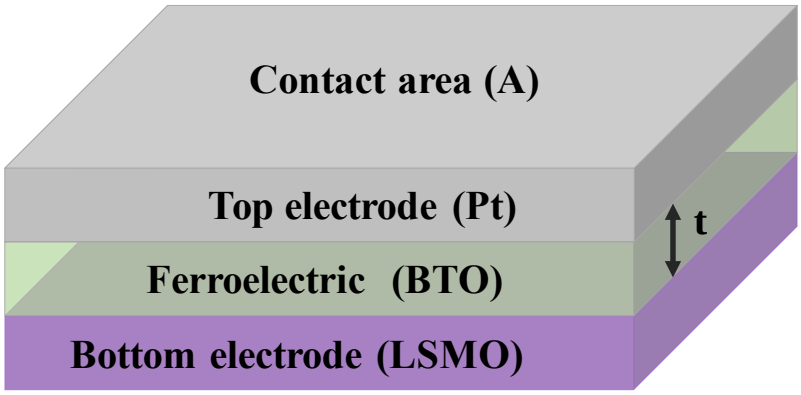


Figure 2.1 *Sketch of a plano-parallel ferroelectric capacitor.*

Epitaxial layers BTO and LSMO have been grown by pulsed laser deposition (PLD) on (001) oriented STO single crystal substrates which impose strain. PLD is a physical vapor deposition (PVD) technique. An illustration sketch of PLD setup and a photo taken during deposition at Institut de Ciència de Materials de Barcelona (ICMAB) is shown in Figure 2.2. In this technique, a high-power excimer laser beam with the wavelength λ=248 nm, passing through a mask and transparent window, is focused on the ceramic target inside the vacuum chamber. The target is ablated due to the high photon energy and high energy density of the laser, that creates a plasma composed by the target species. The created plasma expands perpendicular to the surface of the target. The plasma plume bombards the substrate placed at a certain distance.

Atoms are rearranged and nucleated on the surface of the substrate. Inert or reactive gas is usually introduced during the deposition process.

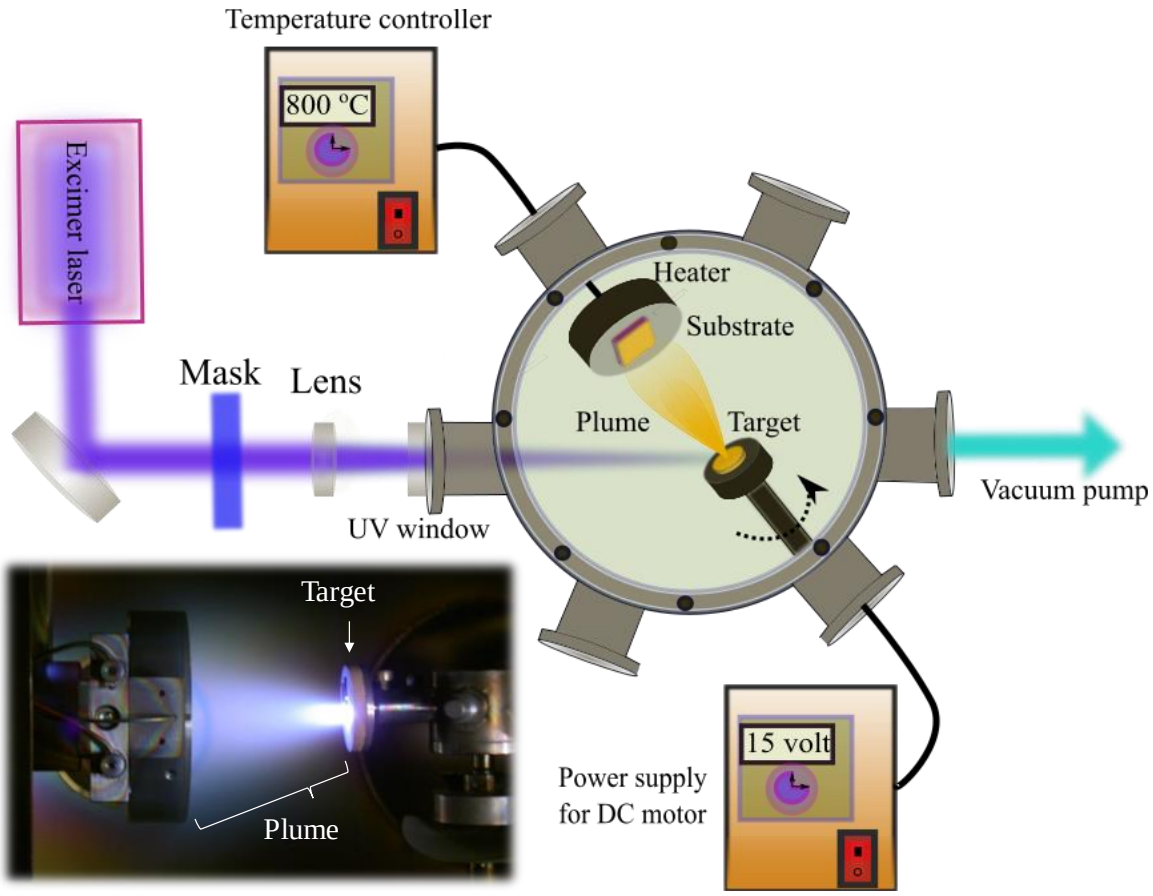


Figure 2.2 *Sketch of PLD system located at ICMAB. Left bottom: deposition is in process.*

BTO thin films in the thesis are grown by PLD service of ICMAB by Dr. Florencio Sánchez following the growth conditions recipe developed earlier. The key growth parameters are the substrate temperature, gas pressure and laser frequency. The kinetic energy of the species at the surface is strongly influenced by the temperature, which allows the atoms to have enough mobility to reach a position energetically propitious, to favor the crystallization. During the deposition, oxygen gas is flowing in the chamber in able to obtain the correct stoichiometry. The growth of LSMO film was performed at 725 °C under an oxygen pressure of 0.2 mbar and a laser frequency of 2 Hz. While BTO was performed at 700 °C and with an oxygen pressure of 0.02 mbar and a laser frequency of 2 Hz. The film thickness is calculated by growth rate times the number of pulses, e.g., the calibrated growth rate of BTO is 0.365 Å.

2.2 Contact fabrication

In this thesis, Platinum electrodes were ex-situ deposited by radio frequency (RF) sputtering on the surface of BTO as top electrodes. The sketch of sputtering chamber is shown in Figure 2.3. Two different sizes Pt top electrodes (with areas of 250 um^2 and 3500 μm^2 and a thickness of ≈ 20 nm) were deposited ex-situ by rf sputtering, through a shadow mask. Pt was chosen because its noble metal nature, very stable in a wide temperature range, easy to grow without impurities and appropriate for ferroelectricity characterization.[37] In sputtering, the target (the Pt here) is set as a cathode and the sample (the BTO thin film here) is set as anode in a vacuum chamber previously evacuated up to high vacuum (~10^{-6} Torr). With Argon gas flowing in the chamber, gas atoms are ionized due to the potential applied and form a plasma bombarding the target, then ions of the target are emitted and deposited on the sample.

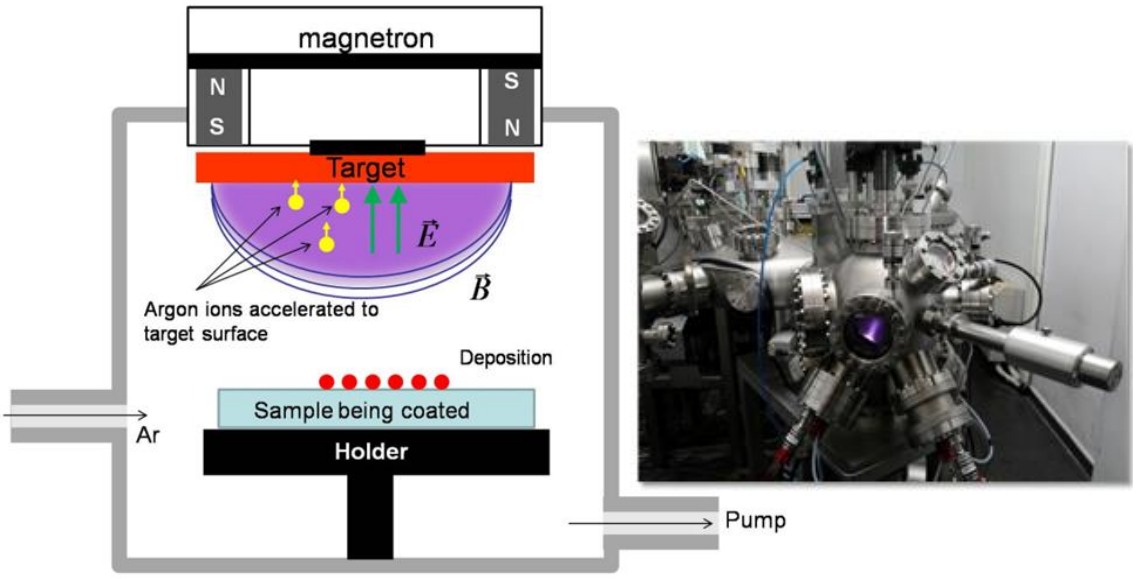


Figure 2.3 *Sketch of the sputtering system and deposition is in process shown in the photo on the right.*

In this thesis, two different sizes of TEM grids were used as mask allowing to deposit about 400 electrodes: 1) circular of diameter 18 μm, 10 μm distance apart and 2) square with 60 μm length, 15 μm distance apart simultaneously. The sputtering was performed at room temperature (RT) with base pressure of 10^{-6} Torr, sputtering power is typically 20 Watts, the flux of Argon is 10 sccm, and distance from target to sample is 5 cm. 3 min sputtering was

performed and ~20 nm Pt was deposited. Figure 2.4 (a, b) shows the deposited Pt electrodes imaged by optical microscope and (c) shows the transparency of the 20 nm Pt.

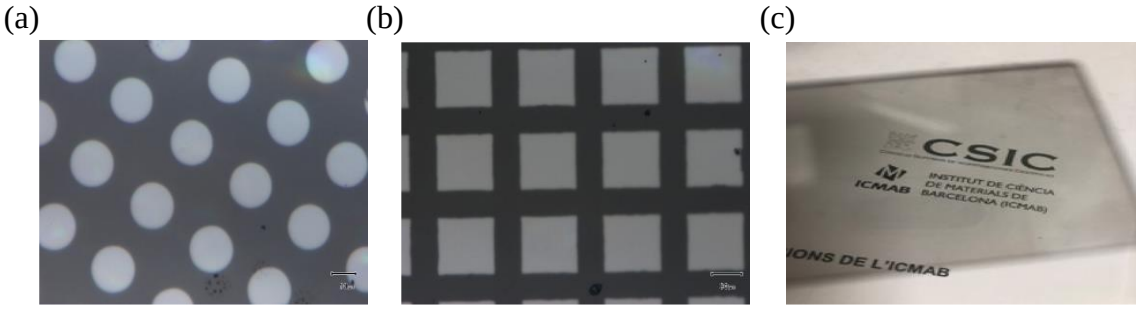


Figure 2.4 *Two different size of Pt electrodes images by optic microscope. (a) circle of diameter 18 μm. (b) 60× 60 μm^2. (c) Transparency manifest of a piece of glass with ~20 nm thick Pt deposited. Darker region is the view of ICMAB label through the glass.*

2.3 Measurement configuration

We call "measurement configuration" the manner in which the thin film is electrically contacted. In this thesis, we have used two measurement configurations: the bottom-top and the top-top, as described in the following. In the bottom-top configuration (Figure 2.5 (a)) the bottom and top electrodes are contacted. Bottom-top is to apply electric field on the top electrode and ground the bottom electrodes (LSMO layer typically). This is an asymmetric configuration, because bottom electrode - insulator and insulator - top electrode interfaces can be different, owing to the fact that top and bottom electrode materials are different. An asymmetric contact configuration (scheme in fig. 2.5 (a)) can lead to very asymmetric P-E or I-V loops or polarity dependent impedance. Exceptionally, in chapter 3 we have used this technique, because of the interest of the asymmetry itself. In the top-top configuration (Figure 2.5 (b)), two top electrodes are contacted. Due to the large difference of resistivity of BTO and LSMO, most electric field will apply on the out-of-plane direction in BTO as the dashed line in Figure 2.4 (b). Therefore, the measured capacitance should correspond to a series connection of two identical capacitors contacted through the bottom electrode (scheme in Figure 2.5 (b)). This is equivalent to the measurement of a single thin film capacitor with double thickness. With this configuration, the asymmetries due to the different metal-insulator interfaces cancel out.

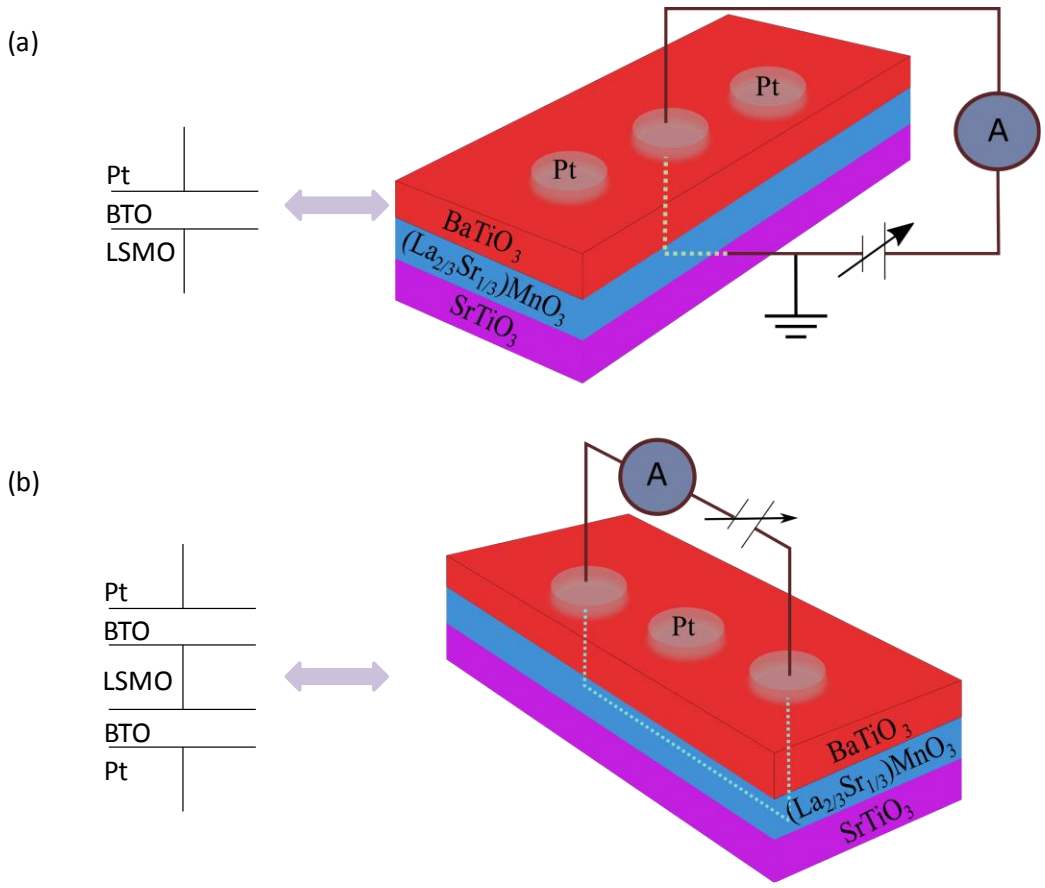


Figure 2.5 *Electrode configurations and equivalent circuits: (a) bottom-top, (b) top-top.*

2.4 Resistive switching

For switching measurements, one can use various input bias sources such as voltage/current sweeps and constant voltage/current pulses. Voltage/current sweeps are frequently used for a simple and quick identification of switching behavior, whereas the application of voltage/current pulses is useful for quantitative investigation on switching kinetics. For successful switching measurements, one should use caution in choosing an input bias source, whether a current or a voltage, and a compliance current to avoid sample breakdown if a voltage source is used. In this thesis, I always set the compliance current at 1 mA.

2.4.1 I-V characteristics

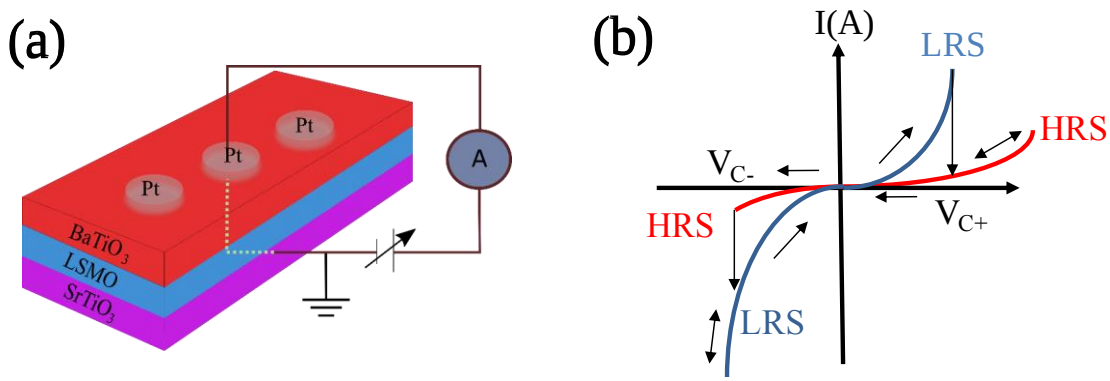


Figure 2.6 *(a) Sketch of the Pt/BTO/LSMO junction and electrical measurement configuration. (b) Sketch illustrative I-V characteristics of a ferroelectric tunnel junction.*

The I(V) characterization of RS was performed using an aixACCT TFAnalizer2000 system with coaxial cable connected to a *Lakeshore* EMPX-HF probe station having 3 μm radius tips (code ZN50R). Current-voltage I-V curves are obtained by applying triangular V(τ_w) pulses of different amplitude V and duration time τ_w, using the contact configuration sketched in Figure 2.6 (a). In all cases the bottom electrode is grounded and the V(τ) signal is applied to the top electrode (Pt). Most of the measurements have been done at room temperature, although in some cases the temperature has been varied between 200K to 450K. Prior to the measurement, a negative electric voltage was applied. The applied voltage is then increased from 0 to the maximum value and decreased back to 0, V (τ) signal as shown in Figure 2.7 (a) and current following the voltage scan (Figure 2.7 (b)). An illustrative I(V) loop is shown in Figure 2.6 (b), in which a transition from low resistive state (LRS) to high resistive state (HRS) and vice versa can be appreciated.

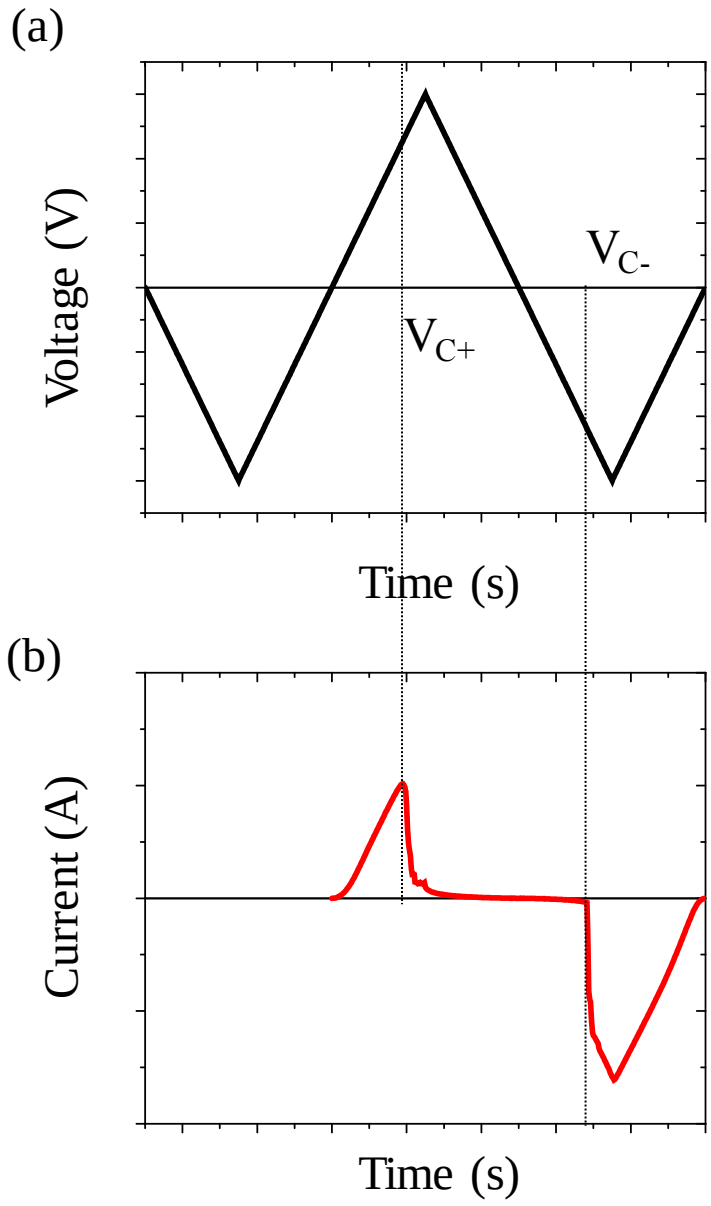


Figure 2.7 *I(V) characterization of RS measurement: applied triangular V(τ_w) pulse signal (a) and result current (b).*

2.4.2 Electroresistance measurements

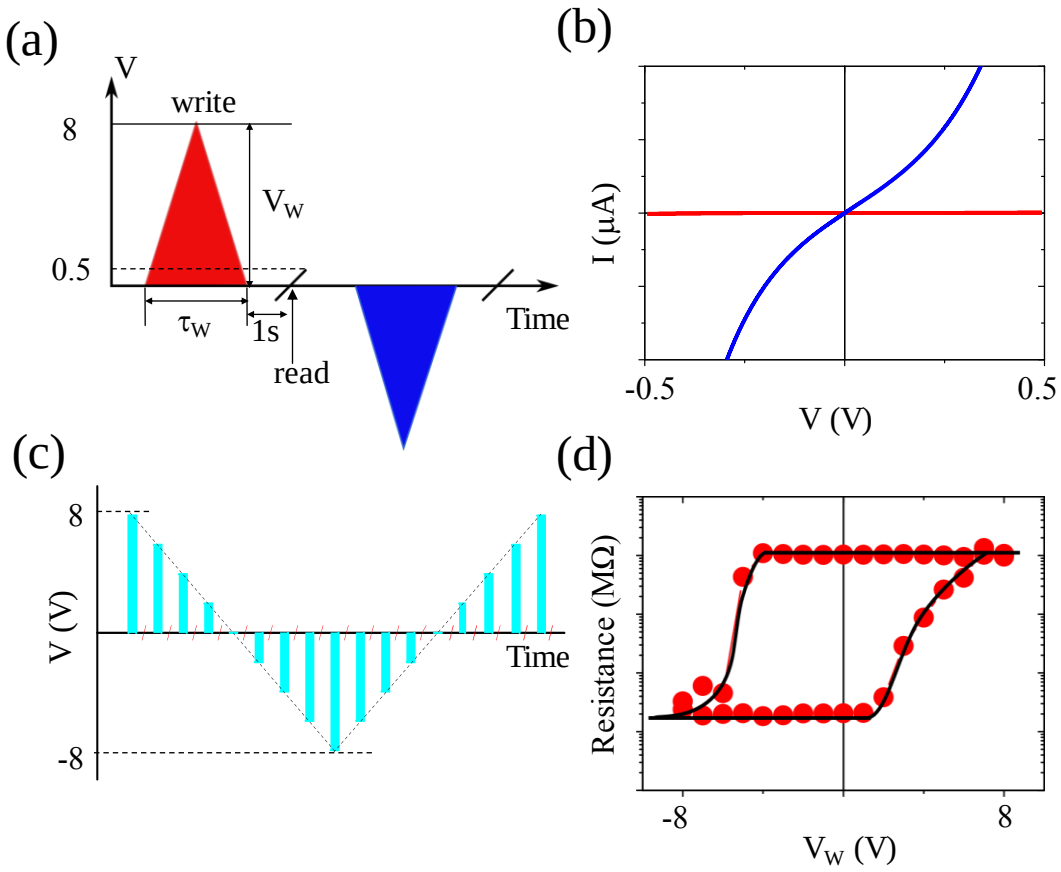


Figure 2.8 *(a) Sketch of the I-V characteristics of a ferroelectric junction measurements. (c) I-V reading pulses recorded after prepolarizating the junction with positive or negative writing voltage of a given writing time τ_w with a delay time τ_D of τ_D = 1s in red and blue line. (c) Sketch of the ER measurement sequence following the +8 V to -8 V to +8V path. (d) A representative ER loop of a ferroelectric tunneling junction.*

The ER measurements of the junctions were performed in two probe geometry as in the case in Figure 2.5 (b). The top electrode is biased. The ferroelectric polarization of BTO barrier was switched applying poling voltages V_w of duration τ_w, subsequently the pulse is removed, and I−V characteristics were performed in the low voltage range (-0.5 V ~ 0.5 V), as shown in the Figure 2.8 (a, b). To obtain the ER loop, a pulse sequence composes of V_W pulses (given duration τ_w), as shown in Figure 2.8 (c), following a triangular profile is applied to the junctions. After each writing pulse, a I(V) curve (represented by the red line) was recorded to read the corresponding resistance R of the junctions. Typically we observed that positive pulses set the

high/low-resistance (OFF/ON) by driving the polarization to point towards the LSMO bottom electrode, whereas negative pulses switch the device to low/high-resistance state (ON/OFF) by polarization reversal.

In this thesis, the ER loops were performed following the +8V to -8V to +8V path, and a representative loop is given in Figure 2.8 (d).

2.5 Top-Top resistive switching

For top-top measurement the electrical connection configuration is shown in Figure 2.5 (b). It corresponds to two ferroelectric capacitors connected in opposition as illustrated in Figure 2.9 (a) and an illustrative I(V) loop is shown in Figure 2.9 (b). It turns out that depending on the applied voltage one of them can be in the HRS whereas the other can be LRS or HRS. Therefore, in principle in this simple device four different states can be obtained: HRS (A) – HRS (B), HRS (A) – LRS (B), LRS (A) – HRS (B), LRS (A) – LRS (B). It will be shown that this combination opens a new opportunity for data storage.

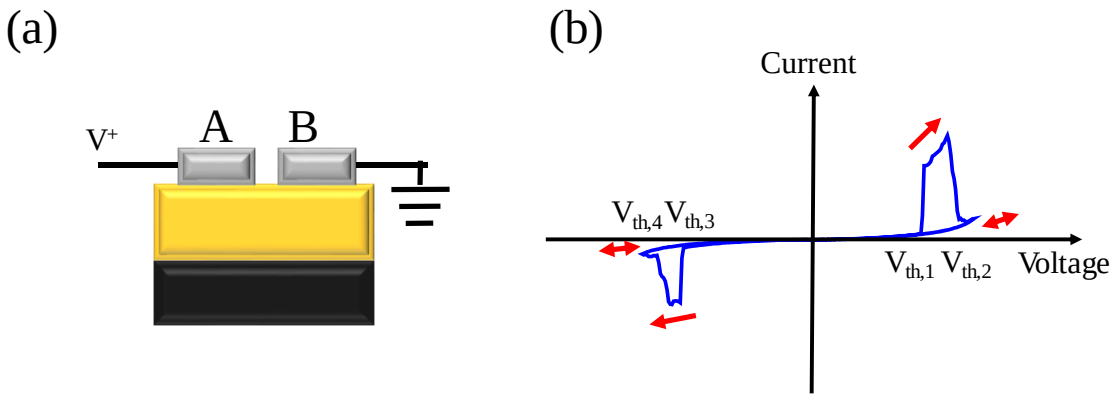


Figure 2.9 *A complementary resistive switching: (a) Sketch of the two Pt/BTO/LSMO junctions in series and electrical measurement configuration. and (b) illustrative hysteretic I–V behavior for combined two elements in series.*

2.6 Ferroelectric and transport characterization technique

2.6.1 Ferroelectric hysteresis loops

Ferroelectricity is a phenomenon that takes place in materials that present the capability to display switchable spontaneous polarization. Therefore, a ferroelectric is more than a dielectric because it can keep a finite polarization in absence of an external applied electric field. The presence of switchable polarization is concomitant to the presence of ferroelectric domains with different polarization directions. The presence of the domains results in a hysteresis of the polarization while cycling the ferroelectric by an external electric field. This hysteresis is depicted in Figure 2.10 (a). First, saturation polarization (*Ps*) is achieved after applying a large electric field. After zeroing the external field, the polarization decreases to the remanence (*Pr*), or remanent polarization. The electric field required to reverse the polarization sign is called the electric coercivity, or electric coercive field (*Ec*). I-V characteristic, as shown in Figure 2.10 (b) is recorded by applying bipolar triangular voltage waveform *V(τ)*, τ is the time, which provide an abrupt current peak where the ferroelectric switching (switching between P^+ and P^- at coercive field) occurs and allows to easily disclose the extrinsic ferroelectric effects. Then the charge *Q* is calculated by integrating *I(τ)* and polarization is the charge per unit surface, so the polarization *P* is the charge *Q* normalized by the area of electrode *A* and the electric field *E* is obtained by dividing the applied voltage (*V*) by the thickness *t*, as indicated by Equation (2.1):

$$P = \frac{\int I(\tau)d(\tau)}{A} \tag{2.1.1}$$

$$E = \frac{V}{t} \tag{2.1.2}$$

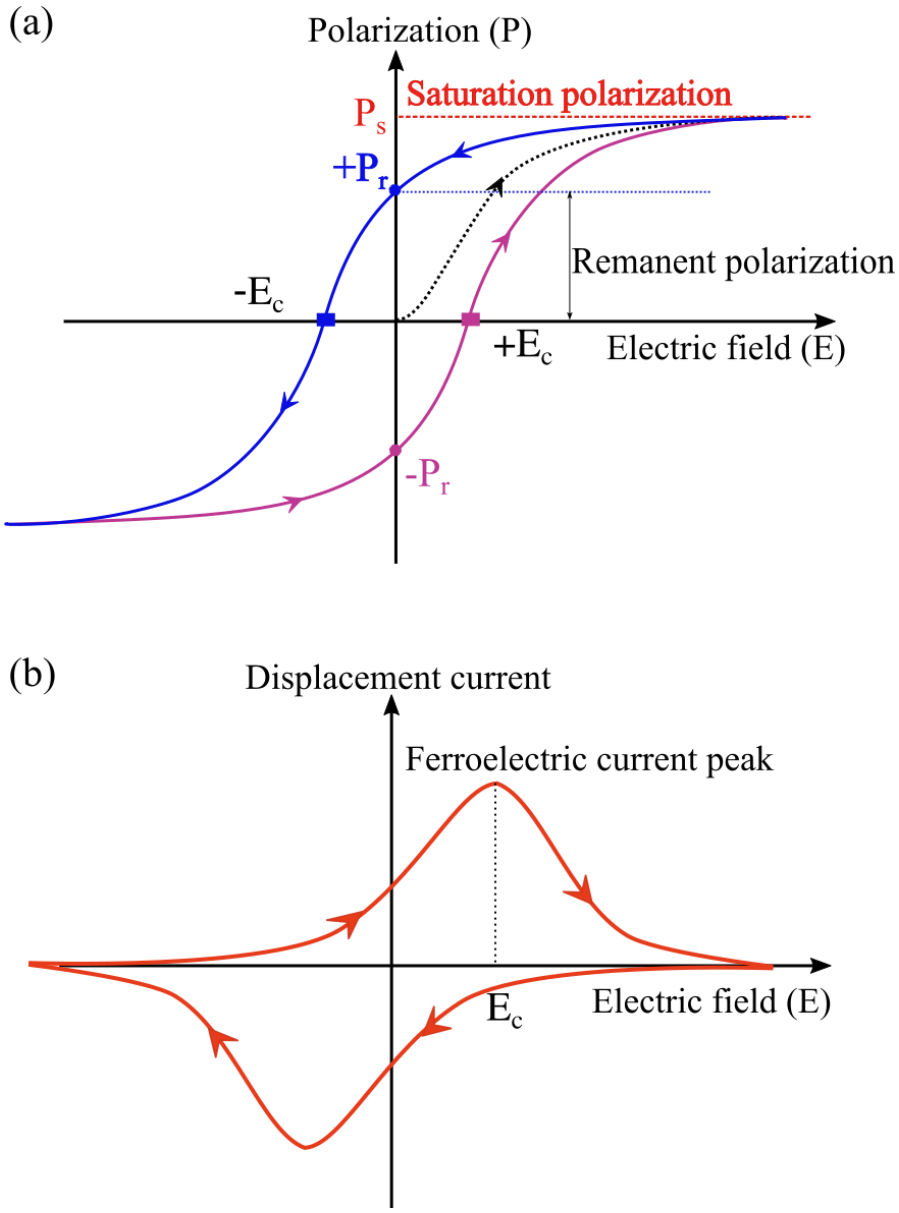


Figure 2.10 *(a) A typical P-E loop integrated from the I-V loop of a standard ferroelectric material. (b) I-V loop of a standard ferroelectric material.*

2.6.2 Dynamic hysteresis measurement (DHM)

I-V loops in the present work have been recorded using the Dynamic Hysteresis Mode (DHM): four bipolar triangular excitation signals of frequency ν_0 are applied with a delay time τ_D between them. The frequency of excitation signal of the *aixACT* setup can vary from 0.01 Hz to 250 kHz. The typical waveform and excitation signal, however, used to measure a hysteresis is shown in Fig. 2.11. The first pre-polarization pulse (black) establishes a defined negative

relaxed polarization state P_{rrel-}. This first pulse is followed by three bipolar pulses with a relaxation time τ_D of 1 sec between the pulses. The current response, corresponding to the second and fourth pulse, is recorded and integrated to obtain the green and blue polarization loops shown in Fig. 2.11 (b). The second pulse (green) starts in P_{rrel-} and cycles a complete hysteresis loop (green loop). The hysteresis loop of this second pulse ends in the negative remnant polarization state P_{r-}. The third pulse (black) establishes a positive relaxed polarization state P_{rrel+}. Subsequently, the fourth pulse (blue) starts in the negative relaxed polarization state P_{rrel+} and ends in the positive polarization state P_{r+}. Finally, the closed hysteresis loop plotted in red in Fig. 2.11 (b) is calculated from the second half of the second pulse and the second half of the fourth pulse. The first and the third pulses are necessary in order to obtain the same measurement conditions while recording the positive and the negative part of the final loop. This method is especially convenient because it does not continuously cycle the sample, avoiding the aging (fatigue).

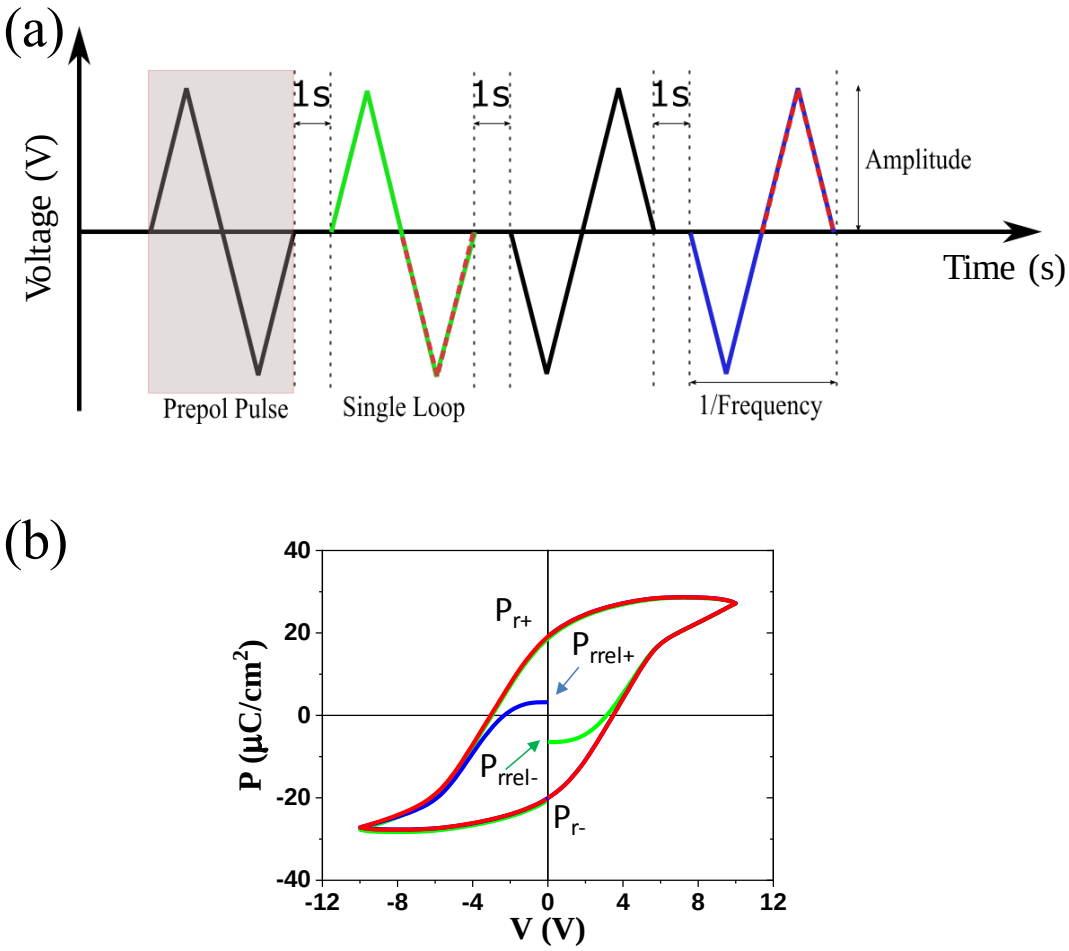


Figure 2.11 *(a) The typical excitation signal of a DHM measurement preformed with the TFA system (b) Typical hysteresis measurement graph indicating the starting point of pulse 2 (green) and pulse 4 (blue).*

The total measured current typically consist of 3 contributions: leakage current ($I_{leakage}$) coming from electrons flowing though the material, dielectric current ($I\varepsilon$) corresponding to charging and discharging current of the capacitor, and the ferroelectric current (I_{FE}) caused by ferroelectric domain switching. The I-V curves obtained by DHM can be corrected for leakage effects using the Dielectric Leakage Current Compensation (DLCC) method that is available at *axiACT*, which can minimize the influence of $I_{leakage}$. By assuming: displacement current ($I\varepsilon + I_{FE}$) varies linearly with the frequency, while $I_{leakage}$, independent of frequency, just varies with the voltage applied. Under these hypotheses, measuring the DHM cycles at two frequencies (ν_0 and $\nu_0/2$) allows subtraction of $I_{leakage}$, and thus only the displacement current remains.

2.7 Resistivity characterization

To determine the resistivity of thin films, studies have been carried out in a 4- contacts configuration. Four probes allow to overcome the problem of voltage drop on contacts and cables. The 4-contacts system permits a precise measurement of the voltage drop across the real sample. Temperature dependence of resistivity measurements can be performed using *Lakeshore* probe station connected to a Keithley 2611, or the contacts are performed through wire bonding, which permits to arrange the sample inside a PPMS (quantum design). Electrical resistivity scheme of the four probes configuration is shown in Figure 2.12. Inject current though I+ and I- and measure the voltage from V+ to V-. Then a resistance R can be calculated. The amplitude of the injected current depends on the materials. For Pt, the current about 1 mA should be a proper scale. While for measuring BTO which is more insulating (large resistance), nA or even smaller injecting current is required to avoid heating.

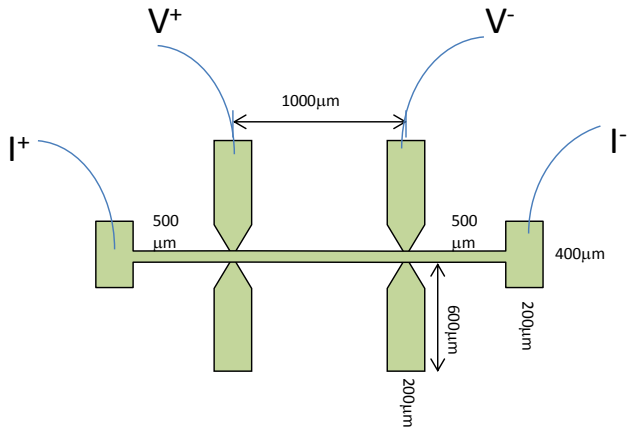


Figure 2.12 *Scheme of the four probes configuration.*

2.8 Dielectric characterization

Dielectric characterization and/or impedance spectroscopy have complex performed using an impedance meter HP4192A LF (Agilent co.), which measure the impedance and the phase of the connected sample. The available measuring frequency ranges go from 5 Hz to 13MHz and the oscillation voltage can be set between 50 mV to 1 V. The sinusoidal voltage (in complex representation) is given by $\tilde{V}(\omega) = V_0 e^{i\omega t}$ which the V_0 is the amplitude of the signal. The current generated by the ac field $\tilde{I}(\omega)$ and the impedance of the capacitor is given by

$$\tilde{V}(\omega) = \tilde{Z}(\omega)\tilde{I}(\omega) \tag{2.3}$$

From this equation the real (Z´) and the imaginary(Z´´) part of the impedance is determined at each frequency. The complex capacitance is determined by

$$\tilde{C} = \frac{1}{i\omega\tilde{Z}} \tag{2.4}$$

2.9 Probe station set-up

2.9.1 Characteristics

The *Lakeshore* EMPX-HF is multifunctional probe station provides vacuum or under specific atmosphere at different temperature. Samples can be measured in vacuum up to 10^{-6} mbar or other atmosphere such as air flow of N_2, Ar, synthetic air, etc., and in a temperature range 5K – 650 K. The sample stages can be either: PS-HTA to be used in the temperature range from 20 K to 675 K or PS-360-EMPX 360° from 5 K to 400 K which can be rotated by 360 º. There is a standard Zoom 70× (7:1 zoom) microscopes available for the probe station. A window on the vacuum chamber lid allows illuminating the sample by coaxial and ring light from the light source and power supply. This allows the vision system to image very highly reflective samples. The ring light surrounds the end of the microscope with light from the source, which illuminates the samples from all directions. The sketch of the system is plotted in Figure 2.13 (a) and the picture shows the measurement performed in the chamber (Figure 2.13 (b)). The *ZN50R–03-W* tip is made of Tungsten with a radius of 3 μm, details are shown in Figure 2.13 (c). The *ZN50R* probe design is optimized for performance from 4 K up to 675 K. This design provides key thermal cooling of the probe tip and blocks unwanted heat to the sample.

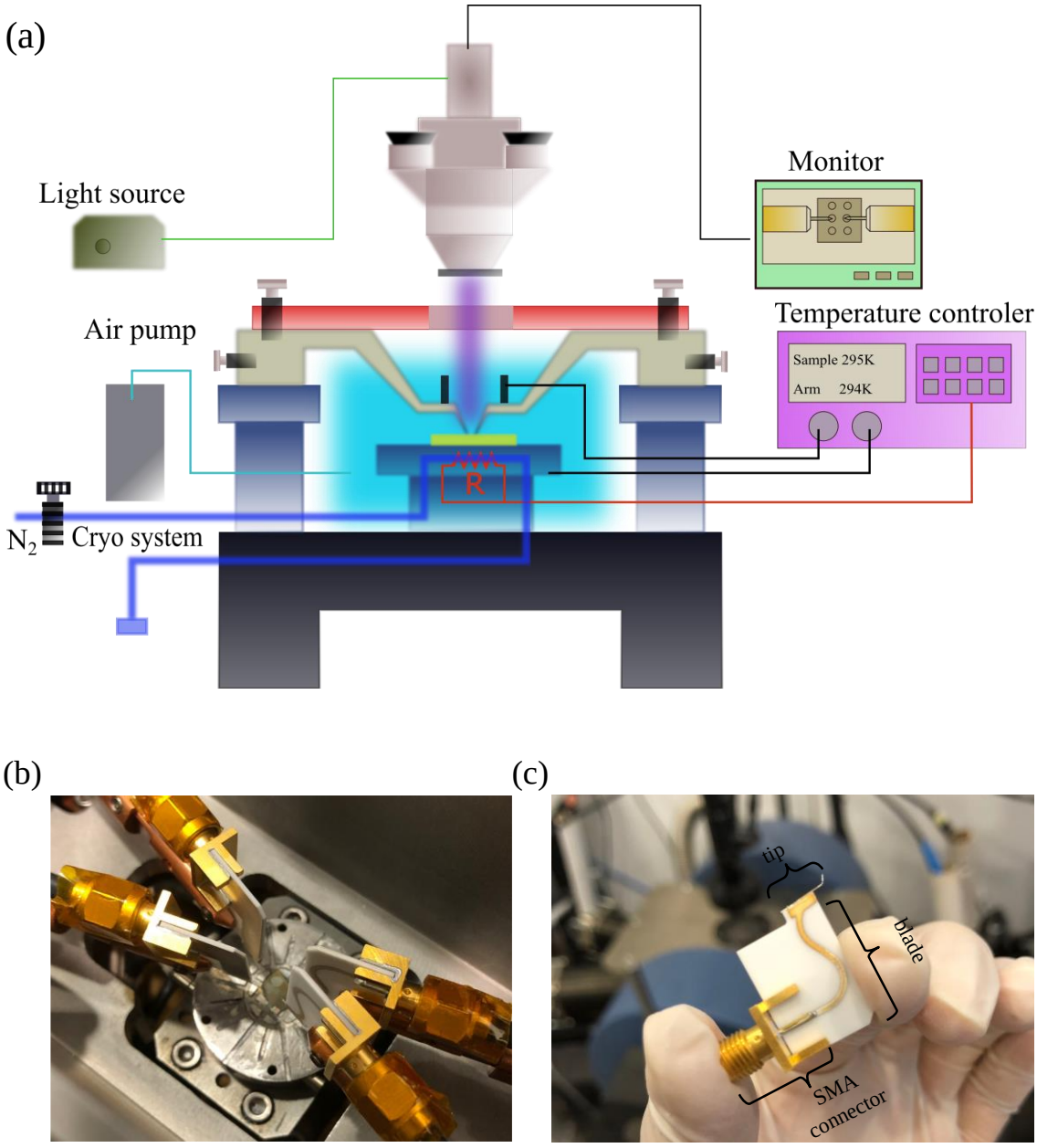


Figure 2.13 *Sketch of Lakeshore EMPX-HF system (a). Picture shows a sample measured in chamber (b) and the detail of ZN50R–03-W tip (c).*

2.9.2 Temperature control and temperature stabilization procedures

Each of the stages in the EMPX-HF (sample, radiation shield, and second shield) have a temperature sensor and heater. Prior to heating or cooling the system it is important to verify that the senor, heater and the temperature controller are all configured properly.

We compare Temperature Coefficient of Resistance (TCR) of Pt measurement by Lakeshore 336 Temperature controller with TCR measured by PPMS to decide the ramping speed.

A temperature coefficient describes the relative change of a physical property that is associated with a given change in temperature. For a property R that changes by dR when the temperature changes by dT, the temperature coefficient α is defined by the following equation:

$$\frac{\Delta R}{R} = \alpha \Delta T \tag{2.2.1}$$

Here α has the dimension of an inverse temperature. If the temperature coefficient α itself does not vary too much with temperature, a linear approximation will be useful in estimating the value R of a property at a temperature T, given its value R_0 at a reference temperature T_0:

$$R\,(T) = R\,(T_0)(1 + \alpha \Delta T) \tag{2.2.2}$$

where ΔT is the difference between T and T_0. For strongly temperature-dependent α, this approximation is only useful for small temperature differences ΔT.

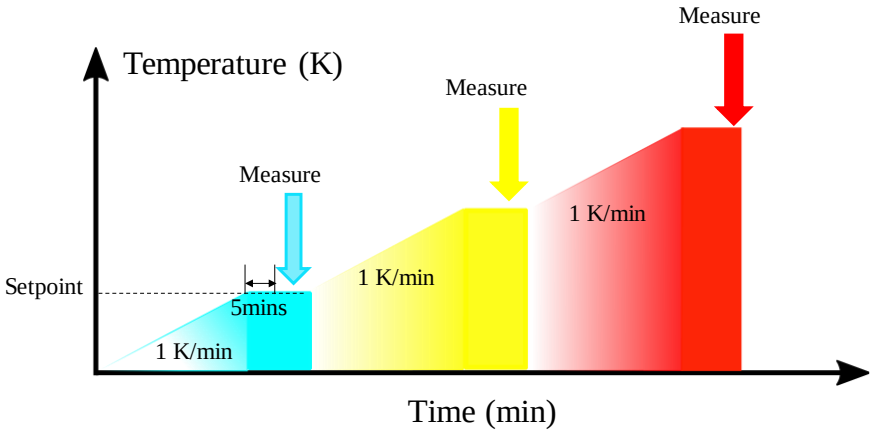


Figure 2.14 *Sketch of ramping speed of temperature dependence measurement.*

We recorded the temperature dependence measurements of resistance of Pt films on different substrates: S160308-01 (Pt/STO), S160308-02 (Pt/MgO) and S160308-03 (Pt/Si). The

measurements have been done using Lakeshore 336 temperature controller with temperature ramping speed 1K/min both increasing up and cooling down. The measurements were performed 5 minutes after the temperature reach the setpoint (Figure 2.14), in case the temperature can stabilize. The I-V cures were measured using multimeter device (Keithley 2611) with four-probe configuration as describe in section 2.7.

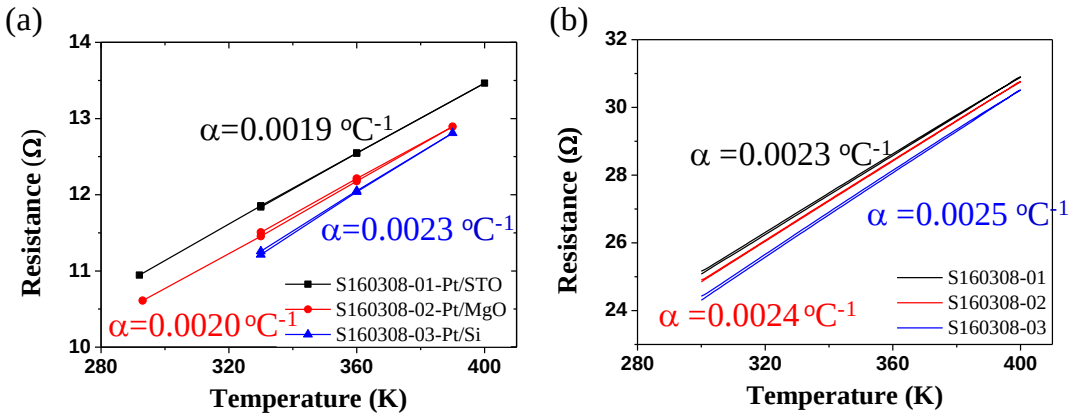


Figure 2.15 *(a)Temperature dependence of resistance of Pt thin films measured in the A Lakeshore EMPX-HF multifunctional probe station. (b) Resistance vs temperature performed in the PPMS service of ICMAB using ramping 1K/min. The calculated temperature coefficient of resistance "alpha" (α) is indicated in the figures.*

In Figure 2.15 (a), we show the Pt resistance linear dependence on the temperature. The difference of the absolute value among the three samples come from the difference of the thermal diffusion coefficient of the substrates. Temperature coefficient of resistance "alpha" (α) of Pt films is around 0.002 $°C^{-1}$ which is reasonable compared with pure platinum has an alpha of 0.0039 $°C^{-1}$ in the 0 to 100 °C range. Figure 2.15 (b) shows α of Pt film is the range of 0.0023 $°C^{-1}$ to 0.0025 $°C^{-1}$ measured by PPMS which is comparable with the number got by lakeshore. While the difference of absolute values between two measurements came from the setup circuit series resistance contributions. While higher ramping is not recommended, as shown in Figure 2.16, there is hysteresis between heating and cooling with ramping 10 K/min, that means the temperature of the sample is not stabilized. In this case, we will use 1 K/min for all the temperature measurements in the following.

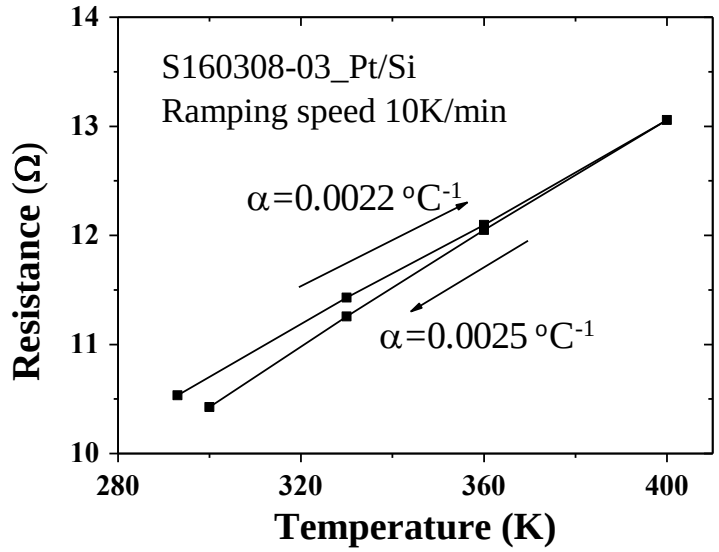


Figure 2.16 *Temperature dependence of resistance of Pt/Si thin films measured in the A Lakeshore EMPX-HF multifunctional probe station with 10 K/min ramping.*

2.9.3 Example

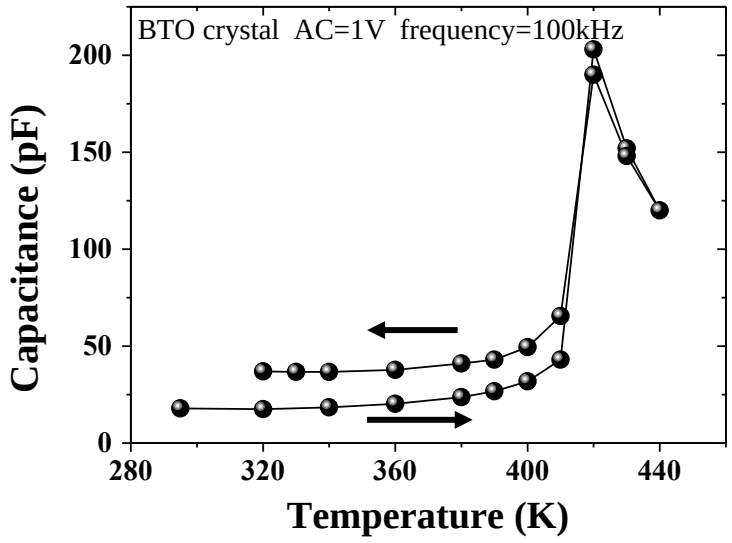


Figure 2.17 *Temperature dependence of capacitance of BTO crystal performed 1K/min heating from room temperature to 440 K and cooling to room temperature. The curie temperature at 420K shown in the peak.*

For calibration purpose, we measure the curie temperature of the BTO crystal to know the absolute difference between the sample and the sample holder as read by the senor.

In Figure 2.17, the capacitance measurement performed with frequency of 100 kHz and Vac = 1V. The measurement was performed heating from room temperature to 440 K and then cooling down with the ramping speed of temperature at 1 K/min. The capacitance was measured at each temperature setpoint stopped as shown in Figure 2.15. We can see clearly the transition peak at 420 K which is coincide in both heating and cooling. That confirms again that with 1 K/min ramping the temperature is well controlled. While the transition temperature we observed is around 20K larger than the reported value of 293 ~ 303 K[38,39] , we consider the temperature shift as a calibration value for the *Lakeshore* sensor and the absolute value of the sample.

2.10 Atmosphere effect on resistive switching measurement

In order to investigate the role of different atmospheres of the *Lakeshore* probe station on electrical measurements, we performed electrical measurement of high-quality Pt / BTO (35 nm and 110 nm) / LSMO junctions grown on (001) oriented STO substrates in different atmospheres. The samples are amounted in a Lake Shore EMPX_HF multifunctional probe station. We measured the current-voltage (I-V) at room temperature using a TFAnalyser 2000 (AixACCT System GmbH. Co.) with current-voltage probes connected to the arms of Lake Shore probe station. Aiming to investigate the atmospheres effect, we have performed the IV measurements in four different conditions within the probe-station: a) open to air, b) under a vacuum of 10^{-5} mbar and c) under N_2 (1 atm) atmosphere, and d) air after measurements b) and c). All measurements have been performed after sample prepoling with +8/-8 V triangular voltage pulses of 10 s.

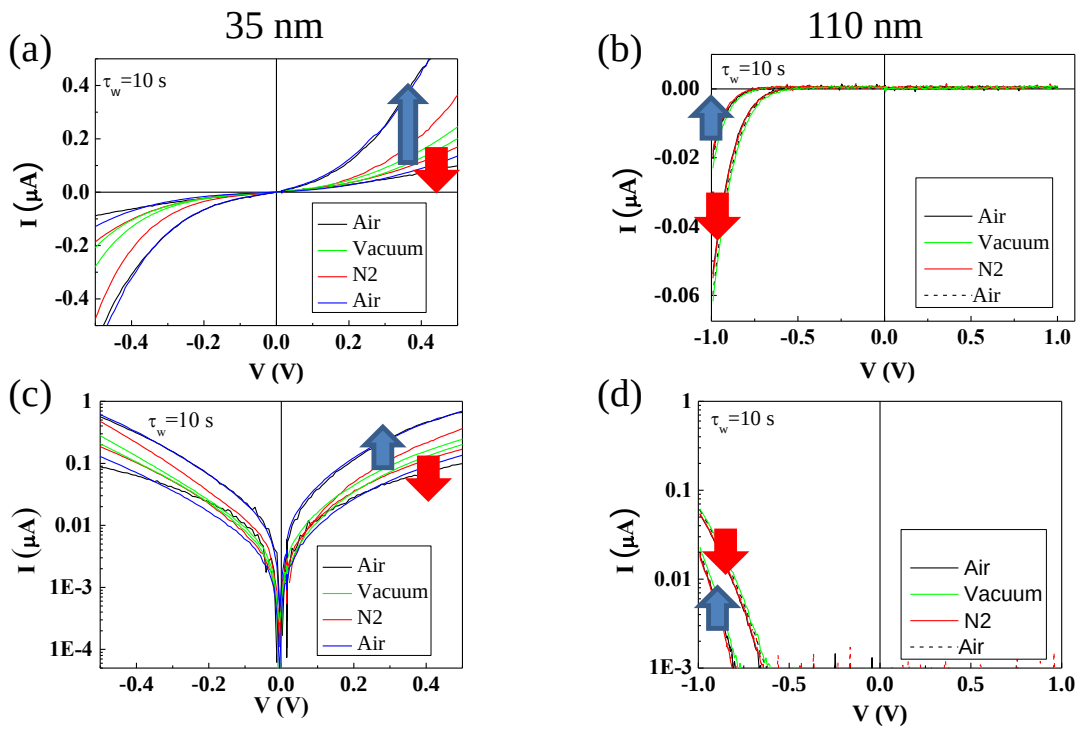


Figure 2.18 *IV characters of ON/OFF states in Pt/BTO/LSMO FTJs under different atmospheres. I-V data after writing 10 s with voltages of +8 V and -8 V in the low-bias region in a Pt/BTO (35 nm)/LSMO FJ in different atmosphere, respectively, open-air (black line), 10-5 mbar vacuum (green line), N2 (red line), air (blue line) presented linearly (a) and in logarithm scale (c). I-V data after writing 10 s with voltages of +8V and -8V in the low-bias region in a Pt/BTO(110 nm)/LSMO FJ in different atmosphere, open-air (black line), 10-5 mbar vacuum (green line), N2 (red line), air (blue line) presented linearly (b) and in logarithm scale (d).*

We performed measurements on samples of two different thickness. Figure 2.18 (a,c) shows representative I-V characteristics in linear and log scale, respectively, for a Pt/BTO(35 nm)/LSMO junction after 10 s poling with +8V/-8V in open air atmospheres (the black line). After poling with -8V (up-arrow) the state is more conductive than after poling with +8V (down arrow). Following the same methods, we performed the measurements in vacuum (10^{-5} mbar, green line) and N_2 (1 atm, the red line) on the same junction. Inspection of the data show that when measurements are performed either in vacuum or under N_2 flow, the I-V characteristics after prepoling with +8V/-8V become closer, that is the resistance contrast between ON/OFF states gets smaller. More precisely, the I-V characteristics after -8V poling (the most conductive state) becomes less conducting (means the resistance is increasing), and the I-V characteristics after +8V poling (the most insulating state) becomes less insulating (means the resistance is decreasing).

Figure 2.18 (b,d) shows representative I-V characteristics for Pt/BTO(110 nm)/LSMO junction after 10 s prepoling with +8V/-8V in open air (the black line). First observation is that the response is diode-like conducting in the reverse direction. This is what is expected on the basis of metal1/ferroelectric/metal2[27,40–46]. After prepoling with -8V the state is less conductive than (up-arrow) than after poling with +8V (down arrow), note that the conductivity of 110 nm thick film after poling with +8V/-8V is opposite to the 35 nm sample.

We performed the same sequence measurements on the 110 nm sample. IV data have been recorded under different atmospheres (air, N_2 and vacuum). It can be observed in Fig 2.18 (b) and (d) that the I-V characteristics show almost no change depending on the atmosphere. Therefore, the sample conductance is not affected by the atmosphere used during measurements.

Figure 2.19 (a) shows the average value of resistance multiplied by area which was read at a bias of 0.1V from the I-V data of 5 measurements in each atmosphere condition (air, vacuum, N_2, and air) in the same Pt/BTO (35 nm)/LSMO junction. The error bars indicate the standard deviation of all the measurements taken on each atmosphere condition. It can be inferred that in vacuum and N_2 is mainly the low resistive state the one that is modified reaching a value similar to the high resistive state. The small difference between the vacuum and N_2 conditions are inside the statistical deviation of different measurements. In the case of the measurement in air conditions after performing the successive vacuum and N_2 atmosphere experiments, the obtained resistance states are very similar to the initial one.

Figure 2.19 (b) we plot the average value of resistance multiplied by area of the 110 nm sample. The resistance was read at a bias of -1 V from the I-V data of 5 measurements in each atmosphere condition. Data for this thicker sample display the same trend than that deduced from the IV curves of Figures 2.18 (c, d). It is observed that the resistance contrast upon poling does not change significantly when measured under different atmosphere condition.

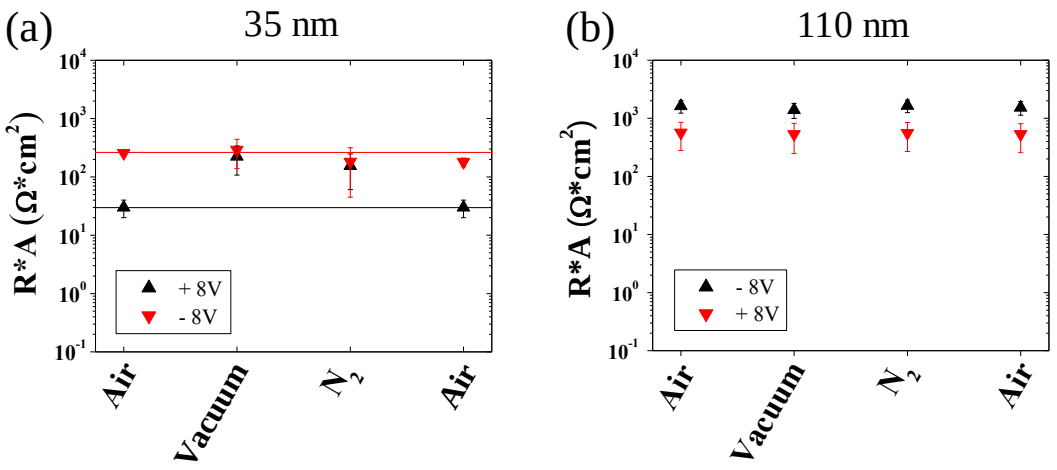
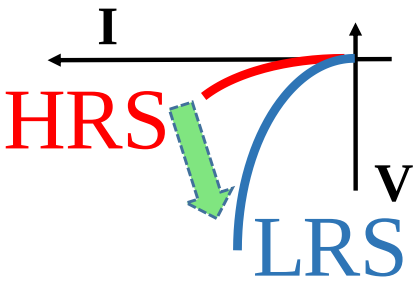


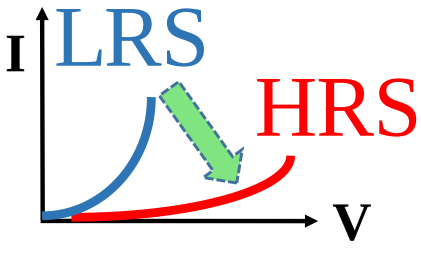
Figure 2.19 *(a,b) Average of resistance multiplied by area and their standard deviation as error bar for 5 consecutive measurements under different atmospheres measured sequentially: air, vacuum, N2, and air for Pt/BTO(35 nm)/LSMO FJ (a) and a Pt/BTO(110 nm)/LSMO FJ, respectively.*

The performed experiments allow to conclude that there is a change of ER for the low thickness sample (positive sign) when measured under vacuum or N_2 conditions. It is observed that the low resistive state does become more resistive under vacuum or N_2 conditions, the change for the high resistive state is less important. No change is observed for thick sample (negative sign) long writing time

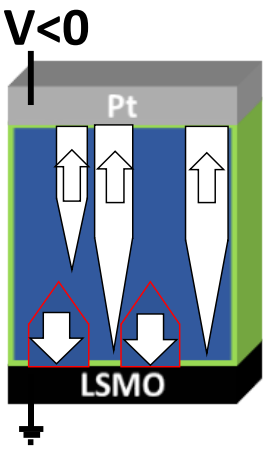
Chapter 3 Asymmetric Resistive Switching Dynamics in BaTiO3 Tunnel Junctions

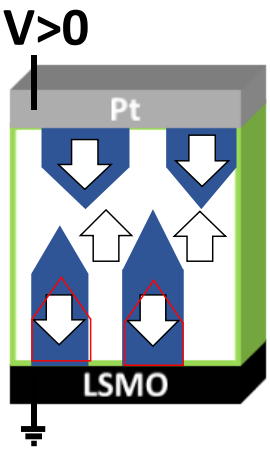


avalanches



expansion





3.1 Abstract

The RS associated to polarization reversal observed in BTO tunnel junctions, is studied in detail with focus on the dynamics of the ferroelectric domain switching. It is observed that the transition between the high-resistive state (HRS) and the low-resistive state (LRS) is largely asymmetric being smooth from LRS-to-HRS but proceed via avalanches in the HRS-to-LRS transitions. We show that this distinct behavior is related to the presence of imprint field in the junction and has important consequences on the junction's performance.

3.2 Introduction

Ferroelectric tunnel junctions in capacitor metal/ferroelectric/metal structures are receiving enormous interest for their potential use as high density (scalability), low energy consumption (small writing/reading voltage) and fast operation non-volatile random access memories (RAM)[8,15,47]. Indeed, switching of the ferroelectric polarization by a suitable writing voltage leads to a changes of the junction resistance with a large resistance contrast between the high resistance state (HRS) and the low resistance state (LRS) than can reach 10^4-10^8%.[4-17] Therefore hysteric I-V characteristics with resistance jumps at the coercive voltages are observed (sketched in Figure 3.1a). These binary easily controllable states are of interest for data storage and digital computing. For that reason ferroelectric RAM (FeRAM) are being intensively investigated.[57] The requirements of growth of single crystalline- like epitaxial oxide layers, with a low defect density to allow charge-tunneling transport channel, are extremely demanding but progress in oxide-based thin film growth technologies have permitted to have tunnel FeRAM at reach.[8]

The extreme thin structure of the dielectric barrier, on the other hand, implies that the ferroelectric domains, whose size decreases with film thickness, must have also a lateral size comparable to the film thickness, that is: few nanometers. Several important consequences emerge from this size scaling. First is that, if ferroelectric domains under the electrode can switch independently under suitable voltage bias, then multiple HRS and LRS can be achieved in a given capacitor and, as polarization switching is known to be dependent on the amplitude

and duration of the polarization voltages,[58–61] memristive response can be achieved.[13] Second, ferroelectric/electrode electrostatic and microstructural effects should play a major role on the time-dependent dynamics of the polarization switching.[62–64] Most commonly, asymmetric electrodes are used in ferroelectric capacitors and as the nature of the corresponding metal/ferroelectric and ferroelectric/metal interfaces are different. Thus, asymmetric polarization switching for positive/negative bias can occur, and it has been experimentally observed.[61,65–69] When refereeing to the RS controlled by ferroelectric polarization, the same arguments given above suggest that the HRS-to-LRS and LRS-to-HRS processes could be also different, implying an asymmetric response when reversing the writing electric fields. Understanding and controlling these effects is pivotal to exploit the potential multistate of the ferroelectric memory. Even more, deep knowledge on asymmetric dynamics is crucial for ferroelectric tunnel junctions implementation in neuromorphic circuits, where time-dependent action potentials trigger the synapse responses.[70]

In the particular case of ferroelectric tunnel barriers, Chanthboula et al.[13] pioneeringly reported the impact of the polarization switching dynamics on the measured change of resistance (so called "ER, or tunnel electroresistance, TER"). These authors observed that under a given voltage bias larger than the coercive field (at a given measuring frequency) the switching from LRS-to HRS was gradual, expanding along a range of voltages. The smooth transition from LRS to HRS was successfully modeled by assuming the contributions of domain nucleation and expansion mechanisms on the domain dynamics. In contrast, the reverse process (HRS-to-LRS) was observed to be more abrupt. This observation, reminiscent of the asymmetric polarization reversal in ferroelectric capacitors [61,65,67–69] may imply a different responsivity of LRS and HRS to external stimuli, thus impacting the memristive response depending on the sign of the biasing electric field.

3.3 Sample

Samples growth and geometry. Nanometric ferroelectric capacitors have been fabricated by pulsed laser deposition by growing thin films of ferroelectric (3.6 nm) BTO on top of an epitaxial metallic LSMO (30 nm) layer deposited on STO(001) substrates. Details of growth conditions and structural characterization of the films have been reported elsewhere.[56,71]

Circular Pt electrodes (20 nm thick, area 250 μm^2) were subsequently deposited ex-situ, by sputtering, on the BTO film surface by using a shadow mask. About 300 electrodes, labelled J_N, where N is the reference number for each electrode, are prepared simultaneously.

3.4 Switching dynamics

3.4.1 I-V characteristics: illustrative loops and reproducibility

Here we focus on the comparison of the resistive transition from LRS-to-HRS and HRS-to LRS in BTO ferroelectric tunnel junctions, triggered by electric fields of different polarity. We show that the dynamics of polarization and the concomitant RS of the BTO junctions are radically different for both polarizations. The resistive transition from LRS-to-HRS is smooth, suggesting it is dominated by random nucleation and growth of polar domains. In contrast, the HRS-to-LRS display avalanche-like features which depend on the amplitude and frequency of the applied electric field. We show that these asymmetric resistive transitions are intimately related to the presence of imprint fields in the device and we argue that its understanding is crucial for applications, such as neuromorphic computing, where the dynamics of the resistive transition is pivotal.

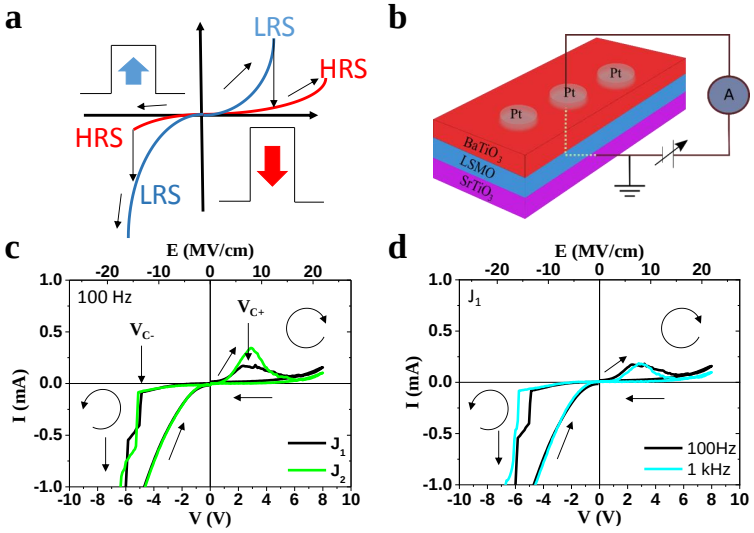


Figure 3.1 *(a) Sketch of the switching process from the low resistance state (LRS) to the high resistance state (HRS) in the I-V characteristics of a ferroelectric tunnel junction, when the barrier height changes from LRS to HRS when reversing polarization (up/down color arrows) as indicated (b) Sketch of the Pt/BTO/LSMO junction and electrical measurement configuration. (c) I-V loops following the -8 V to*

+8 V to -8V path of two different junctions (J_1 (black), J_2 (green)), measured at 100 Hz. (d) I-V loops of the J_1 junction measured at 100 Hz (black) and 1 kHz (cyan).

In Figure 3.1 (c), we show illustrative I-V loops (junctions J_1 and J_2) recorded in the ± 8 V range at 100 Hz. Data indicate that I-V loops have a clockwise and anticlockwise hysterical behavior for V > 0 and V < 0 regions, respectively. In the V > 0 region (positive voltage applied to the top Pt electrode), the clockwise rotation of I-V implies a change from low-resistance state (LRS) to a high-resistance state (HRS) upon increasing V, occurring at a critical voltage (V_{C+}) $V_{C+} \approx 3$ V. The junction remains in the HRS when retreating voltage until a critical voltage (V_{C-}) $V_{C-} \approx -5$V, where the LRS is recovered (anticlockwise rotation). When reducing the amplitude of the V < 0 field, the LRS is preserved. The HRS is only restored again if V_{C+} is overpassed again. It is obvious in Figure 3.1 (c) that the RS signatures are radically different depending on the sense of the switching (HRS-to-LRS and viceversa). It is of limited amplitude and smooth from LRS to HRS, whereas it of large amplitude and displays several steps during the HRS to LRS transition. This different behavior is observed in most of the junctions fabricated on the sample. In Figure 1(d), we show the I-V loops of J_1 recorded at different frequencies (100 Hz and 1 kHz). Data for other junctions are included in Figure 3.2.

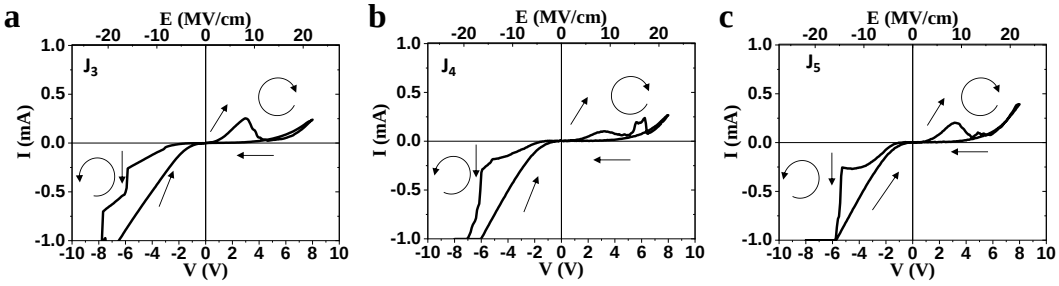


Figure 3.2 *The I-V loops following the -8 V to +8 V to -8V path of three different junctions J_3 (a), J_4 (b) and J_5 (c).*

Inspection of these data reveals two prominent features. First, in the V > 0 region the switching from LRS to HRS appears at higher V and the width and amplitude varies with the measuring frequency. Second, in the V < 0 region, the characteristics steps in I-V curve signaling the transition from HRS to LRS also occur at higher voltages when increasing frequency and the amount and height of the steps in I(V) are also modified. This is a common trend observed in most junctions as seen in Figures 3.3 and 3.4.

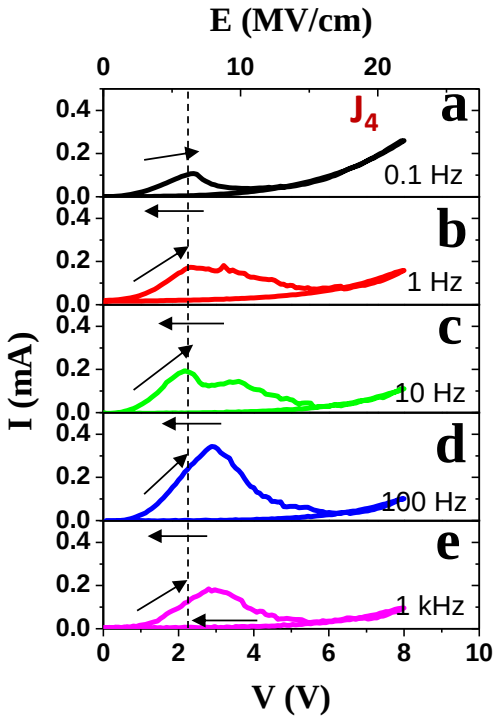


Figure 3.3 *Positive V>0 branch of the I-V loops of junction J_4 recorded using triangular pulses of 0.1 Hz (a), 1 Hz (b), 10 Hz (c),100 Hz (d) and 1 kHz (e). Prior to measurement the junction have been pre-poled with a V = -8 V triangular pulse of τ_W= 1s.*

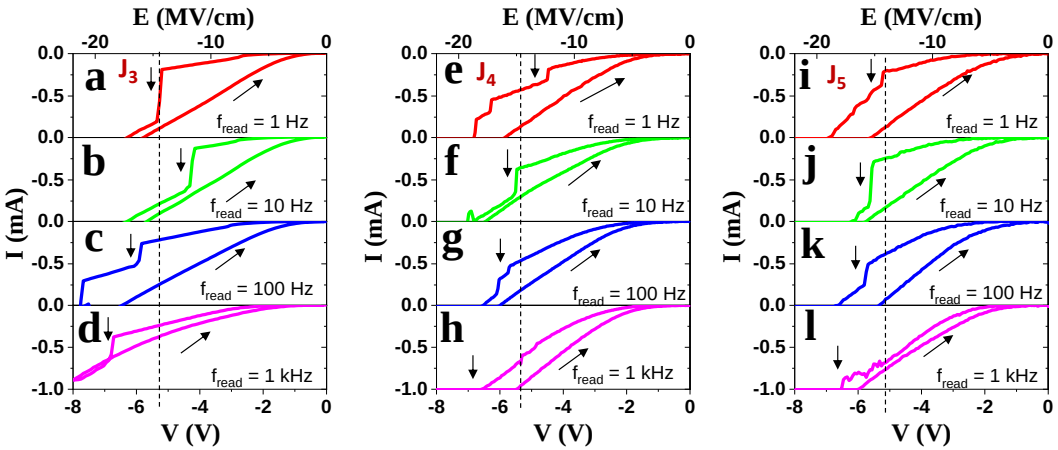


Figure 3.4 *Dependence on the measuring (reading) frequency of the HRS to LRS transitions in the reverse side (V < 0). Prior to measurement the junctions have been pre-poled with a V = +8 V triangular pulse of τ_w= 1s. J_3 (a-d), J_4 (e-h) and J_5 (i-l).*

In the following, we analyze in detail these observations.

3.4.2 I-V characteristics in the V > 0 region the switching from LRS to HRS

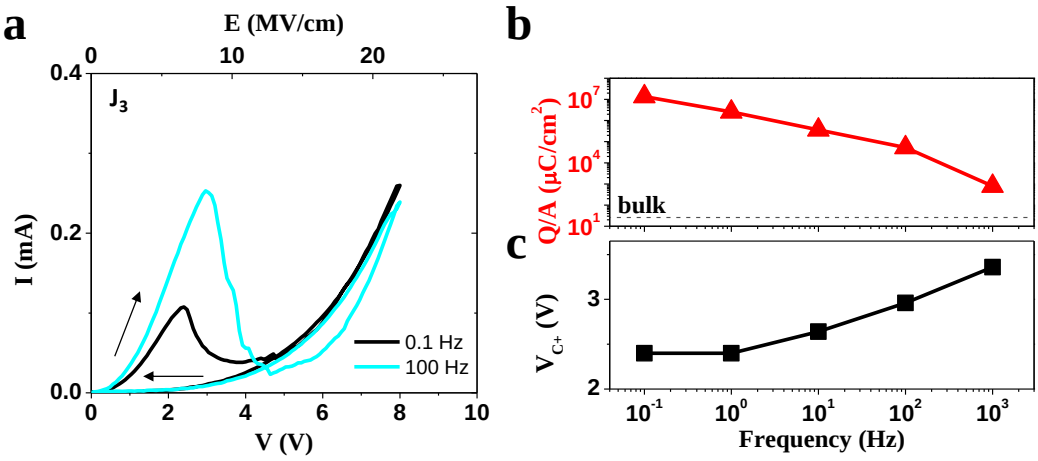


Figure 3.5 *(a) Positive V > 0 branch of the I-V loops of junction J_3 recorded using triangular pulses of frequencies 0.1 Hz and 100 Hz. (b) Integrated area under the I(t) current peak (Q), normalized by the junction area (Q/A), as a function on the measuring frequency. (c) Dependence of the position of the I-V maxima (V_{C+}) on the measuring frequency.*

In Figure 3.5 (a), we show a zoom of the V > 0 region of the I-V loops of junction J_3 recorded using different frequencies (0.1 and 100 Hz). Similar data for other junctions are included in Figure 3.3. In Figure 3.5 (a), the trends already identified in Figure 3.1 (c), namely the shift of the voltage where switching occurs (V_{C+}) and the change of the corresponding peak (increase of amplitude) for increasing measurement frequency can be more clearly appreciated because the selected measurement frequencies shown in Figure 3.5 (a) differ by 3 orders of magnitude. In Figure 3.5 (b), we show the time-integrated area under the switching current peak ($Q = \int I(t)\,dt$) divided by the contact area (A) as a function of frequency. Q/A is a measure of the specific charge that has flowed across the measuring device during the transition from LRS to HRS. It can be observed that Q/A is as large as 10^7 μC/cm^2 at the smallest frequency (0.1 Hz) and decreases rapidly upon increasing frequency. Irrespective of the measurement frequency the Q/A values are orders of magnitude larger than the polarization of bulk BTO (≈ 26 μC/cm^2, dashed line in Figure 3.5 (b) implying that the measured current is dominated by transport current in the device rather than by the displacive current consequence of the ferroelectric polarization switching. Therefore, it can be safely concluded that the observed switching peak at V_{C+} polarization switching displacive current. In Figure 3.5 (c), we summarize the

frequency-dependence of the V_{C+} peak. It is clear that V_{C+} increases with frequency. The roughly linear dependence of V_{C+} on log(ν) (Figure 3.5 (c)) is a common frequency dependence of the coercive fields in ferroelectrics.[72] Therefore, we argue that RS maxima occur at the ferroelectric coercive voltage, and we assume that the switching peak correspond to the switching from LRS to HRS controlled by the polarization reversal of BTO.

In ferroelectric devices backswitching can be a relevant contribution to the polarization dynamics.[69,73] To address this point, we have written a $P^{\uparrow}$ state (where $P^{\uparrow}$ denotes polarization pointing towards Pt) by applying a suitable negative pulse (τ_w = 1 s) equivalent to a measuring frequency of 0.5 Hz, and subsequently we have recorded I-V loops (V > 0) with a delay times (τ_D) between writing and reading voltage pulses as indicated in Figure 3.6 (sketches). We first recorded an I-V curve with τ_D = 0 (green curve in Figure 3.6). Next we have rewritten the same initial state and measured the I-V loop with τ_D = 1 s (red curve in Figure 3.6). We notice in Figure 3.6 that when a delay time τ_D is introduced between writing and reading pulses, the amplitude of the switching peak, as thus the LRS to HRS transition is reduced, but the resistance on the HRS is virtually identical and the retreat curves coincide. This observation indicates that during the delay time τ_D (writing voltage zeroed) some polar domains have spontaneously switched back from $P^{\uparrow}$ to $P^{\downarrow}$. Therefore, an imprint E_{imp} field exists, governing the backswitching of polarization and it is directed from Pt to LSMO as indicated in Figure 3.6.

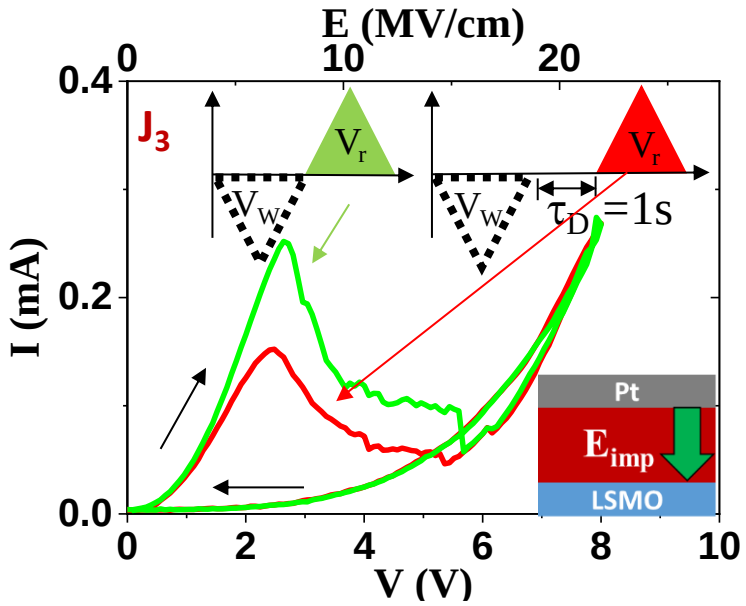


Figure 3.6 *I-V reading pulses recorded after prepolarizating (polarization up, $P^{\uparrow}$) the junction (writing) with a V = -8V pulse of τ_w = 1s, with a delay time τ_D of τ_D = 0 (green curve) and τ_D = 1s (red curve). Top sketches indicate the sequence of prepoling writing (dashed triangle) and reading voltages V(t) pulses (green and read triangles). Bottom sketch indicates the direction (green arrow) of the imprint electric field (E_{imp}) (from Pt to LSMO) responsible for backswitching of P.*

3.4.3 I-V characteristics in the V < 0 region the switching from HRS to LRS

We turn now to the HRS to LRS switching occurring at V < 0. We have collected I-V curves in the V<0 range (after the initial V = +8 V and V= 0 with τ_W = 1s). We have recorded I-V loops when varying the frequency of the V(t) pulse. In Figure 3.7(a-d), we show data of J_4 junction at some illustrative frequencies (1, 10, 100, 1000 Hz). Similar data for other junctions are included in Figure 3.4. Inspection of the I-V curve recorded at 1Hz (Figure 3.7(a)) shows that when increasing the negative bias, well defined steps appear at $V_{C-,1}$ = -4.5 V and $V_{C-,2}$ = -6.2 V, respectively which indicate partial transitions from HRS to LRS. When increasing the measuring frequency, the first step in I-V occurs at somewhat larger (negative) voltage, for instance V_{C-} = -5.5 V at 10 Hz (Figure 3.7 (b)). In Figure 3.7 (e) we show the frequency-dependent of $V_{c-,1}$ values for three different junctions. As indicated above, a gradual shift of $V_{c-,1}$ to larger negative voltage is consistently observed for the different measured junctions.

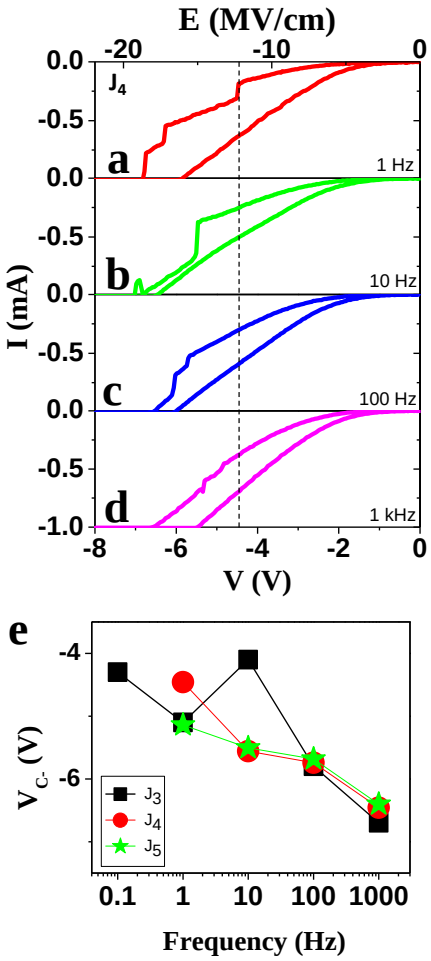


Figure 3.7 *(a-d) Dependence of the HRS to LRS transitions in the reverse side (V < 0) (junction J_4) on the measuring (reading) frequency. Prior to measurement the junctions have been pre-poled with a V = +8 V triangular pulse of τ_W = 1s. Dashed vertical line indicates the position of the 1st current step occurring at $V_{C-,1}$ = -4.5 V (1Hz). (e) First step current onset (V_{C-}) of J_3 (black squares), J_4 (red circles) and J_5 (green stars) junctions versus frequency.*

The I-V trends in Figure 3.7 are reminiscent of domain avalanches promoted by the V(t) excitation in ferroelastic [74,75], ferroelectrics [65,76,77], and other materials [78]. To get additional insight, we recorded I-V curves at V < 0 as above, and compared with the one obtained after returning to V = 0 and, without re-poling the sample (that is without applying any V > 0 pulse), increase again the negative voltage after a delay time τ_D = 0 or 1 s. Measuring cycles are indicated in the sketches in Figures 3.8 (a) and 3.8 (b), where we also show the results obtained for τ_D = 0 (junction J_5) and τ_D = 1 s (junction J_6), respectively. In Figure 3.8 (a), it can be appreciated that the initial I-V loop (green curve), recorded at 10 Hz, in agreement with data

in Figure 3.1 and Figure 3.7, clearly displays conductance steps. Within the proposed framework, the jumps in I-V mean that polar $P^{\uparrow}$ domains have been switched to $P^{\downarrow}$ by the V(t) pulse, bringing the junction from HRS to LRS. In the second V(t) excursion, after zeroing V, the I-V curve (red curve) is radically different. As seen, the sample now reversibly follows the trace of the LRS state, thus indicating that it remains in the LRS and signifying that, in absence of a poling V > 0 field, $P^{\downarrow}$ domains have not switched back to the HRS ($P^{\uparrow}$). This observation implies that the imprint field revealed by data Figure 3.8 does not have a significant role while setting the LRS, because E_{imp} favors LRS. As it could be argued that the backswitching process could be a slow process and thus not perceptible in the time scale of the measurement, we have performed similar measurements but using a longer dwell time $\tau_D = 1$ s at V = 0. The results (Figure 3.8 (b)) display a similar behavior than in Figure 3.8 (a), thus confirming that backswitching from LRS to HRS is not relevant.

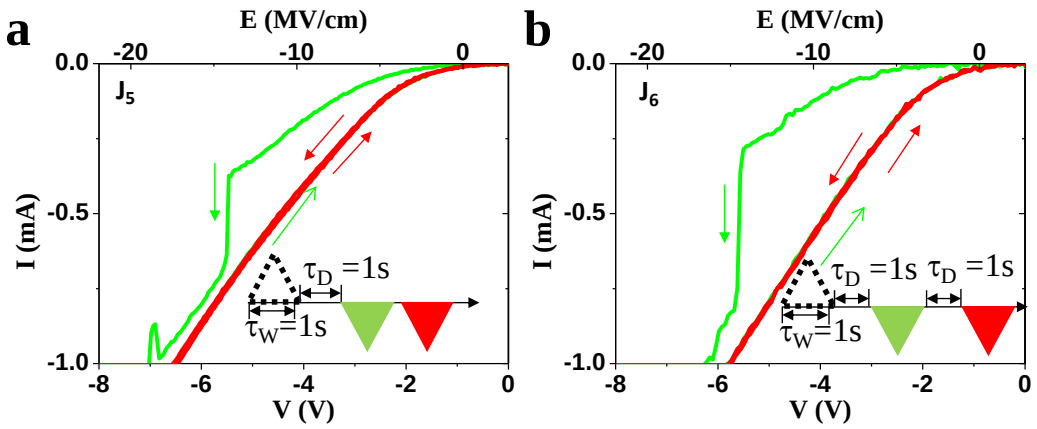


Figure 3.8 *I-V reading pulses after suitable prepoling. Prior to measurements, the junctions have been pre-poled with a V = +8 V triangular pulse of* τ_W *= 1s. Sketches indicate the sequence of prepoling writing (dashed triangle) and reading voltages V(t) pulses (green and read triangles). Reading I-V curves collected at 10 Hz with no delay (*τ_D *= 0 s) between writing and reading (a), and with a delay (*τ_D*= 1 s) between consecutive reading pulses (b).*

3.4.4 Tunneling electroresistance.

We turn now to the tunneling resistance variation upon electric poling of these junctions. Measurements were performed by writing a polar state using a triangular V(t) pulse of varying amplitude up to ± 8 V, of duration τ_w. Afterwards, the junction resistance is measured at 100 mV. In Figure 3.9 (a), we show data written at τ_w = 20 µs. It can be appreciated that after a V >

+8 V pulse (electric field pointing down from Pt to LSMO) a HRS is written. It remains stable until $V_{C-} \approx$ - 7 V where a sudden switch to the LRS is observed. The ER (TER) is quantified by: TER = [R(HRS)-R(LRS)]/R(LRS) where R (HRS, LRS) are the junction resistance in HRS or LRS states, respectively. It can be derived from data in Figure 3.9 (a) that TER ≈ 230%. This is a remarkably large TER value for micrometric sized (250 μm^2) metal/BTO/metal junction at room-temperature.[9,13,55,56] In the reverse side of the loop, switching from LRS to a HRS occurs at a somewhat relatively smaller voltage $V_{C+} \approx$ +2 V. The difference V_{C+} and V_{C-} reveals the presence of an imprint field E_{imp} pointing downwards (from Pt towards LSMO) in agreement with data in Figure 3.6. In Figure 3.9 (c), we plot the I-V curve measured in the ± 8 V range at using a 25 kHz V(t) excursion which correspond to a writing time τ_w of 20 μs, identical to that used (τ_w = 20 μs) in Figure 3.9 (a). There is an obvious coincidence between the switching peaks observed in I-V curves (Figure 3.9 (c)) and the ER changes (Figure 3.9 (a)). When longer writing pulses are used, for instance τ_w = 0.5 s in Figure 3.9 (b), after setting the HRS with a V = + 8 V pulse, the transition to the LRS when reducing writing voltage, starts gradually already at V ≈ 0 and the complete transition is definitely more gradual than that observed using shorter writing pulses (Figure 3.9 (a), τ_w = 20 μs). The corresponding I-V curve is shown in Figure 3.9 (d). It has been recorded at 1 Hz (corresponding *to* τ_w = 0.5 s of Figure 3.9 (b)). The close coincidence between switching peaks and TER changes is also well apparent.

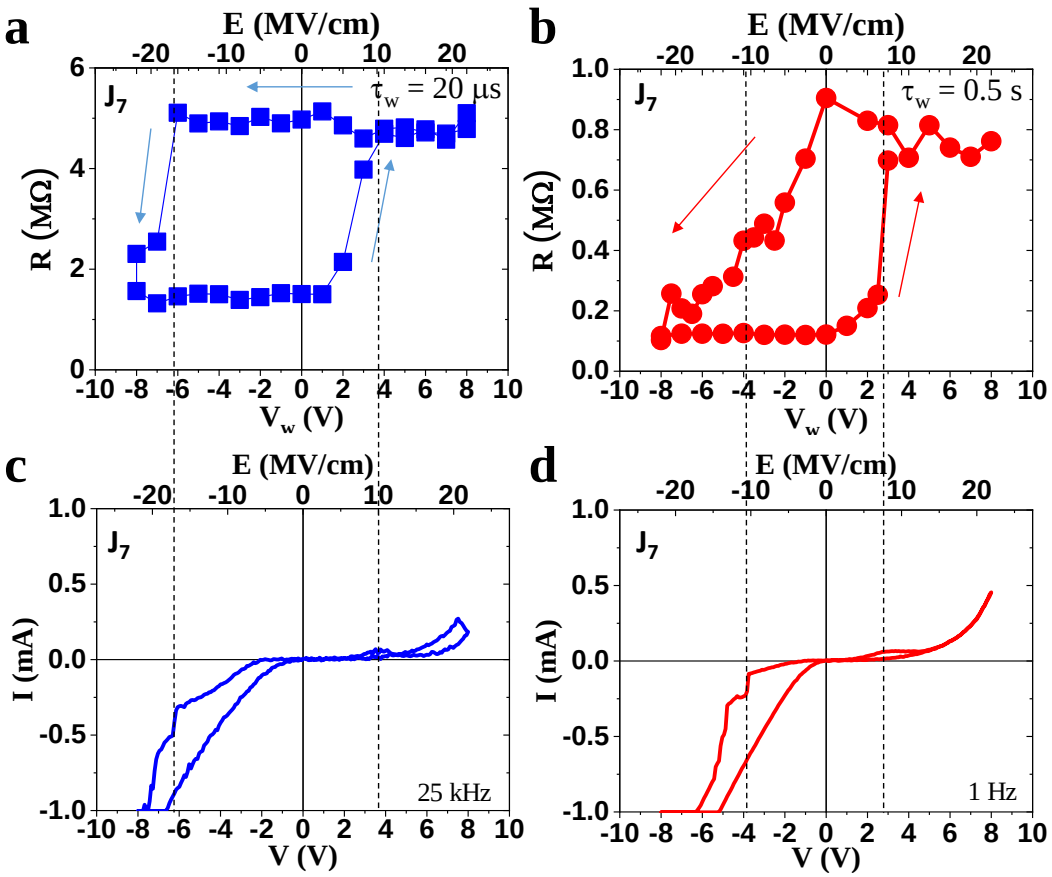


Figure 3.9 *ER recorded in a Pt/BTO/LSMO (J_7) junction after writing pulses (up to ±8V) of duration: (a) τ_w = 20 μs and (b) τ_w = 0.5 s. I-V curves recorded using identical writing times as in (a,b): (c) τ_w = 20 μs and (d) τ_w = 0.5 s.*

3.4.5 Mechanisms.

It can be suspected that differences on polarization switching should be more apparent at low driving fields, namely at subcoercive bias fields ($V < |V_{C+,-}|$). Therefore, we explore the time stability the HRS and LRS states under subcoercive ($V > 0$ and $V < 0$) bias, once written by suitable voltages. We first write a $P^{\uparrow}$ state by applying V = -8 V (τ_w = 1 s) pulse to set the LRS. We subsequently apply a positive reading voltage V_r = +2 V, as sketched in Figure 3.10 (a). Notice that $V < V_{C+}$, thus the set voltage is slightly smaller than the voltage where the switch peak in I(V>0) occurs. The results, displayed in Figure 3.10 (b), indicate that, in spite that $V_r < V_{C+}$, a gradual evolution with time from the LRS to HRS occurs. Next, we write $P^{\downarrow}$ state by applying a V = +8 V (τ_w = 1 s). We subsequently apply a negative reading voltage V_r = -4.5 V.

The measuring sequence is sketched in Figure 3.10 (d), and we record the time evolution of the charge current (proportional to the junction resistance). Results are shown in Figure 3.10 (e). Notice that the V_r has a magnitude smaller than the corresponding coercive voltage (V_{C-}) ($|V_r| < |V_{C-}|$). In spite of this, it is obvious in Figure 10e that the sample displays sudden changes of resistance at some specific instants, that are analogous to the avalanches observed when increasing V (< 0) (as in Figure 3.1 (a), 3.1 (b) and 3.7 (a-d)). These data illustrate the clear differences of the polar domain switching dynamics under V > 0 and V < 0 bias.

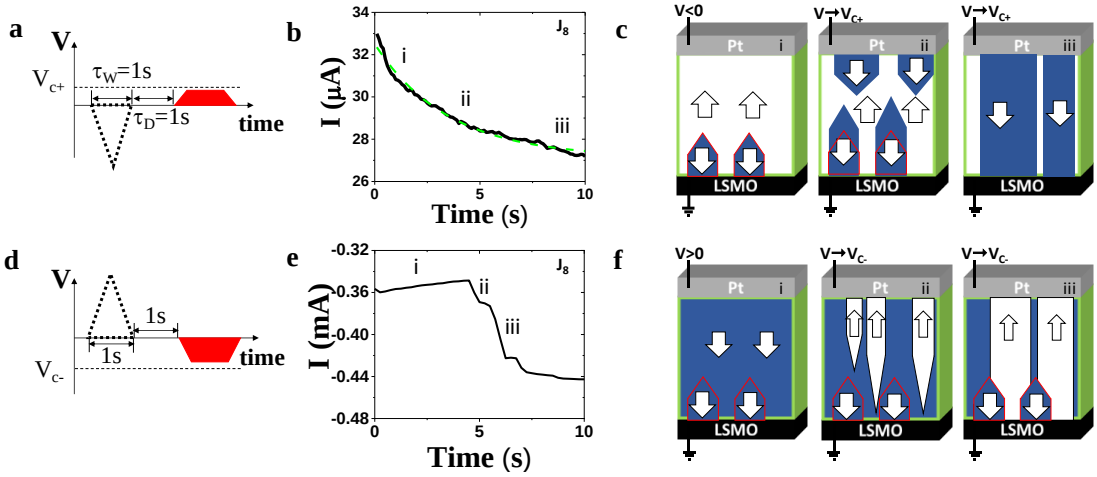


Figure 3.10 *(a) Sketch of measurement sequence for 0 < V < V_{C+}; Notice that the reading V voltage (red trapezoid) is smaller than the coercive field V_{C+} (dashed line). (b) Time-dependent current I(t) collected at constant reading V voltage (0 < V < V_{C+}) (solid line). Dashed line indicates the result of the data fit using a stretched exponential decay (see text). (c) Sketch indicating of gradual growth of unswitchable $P^{\downarrow}$ domains (outlined in red) assisted by the pointing down (towards LSMO) imprint field (i,ii,iii). (d) Sketch of measurement sequence for V_{C-} < V< 0. (e) Time-dependent current I(t) collected at constant reading V (V_{C-}<V<0). (f) Sketch indicating of the abrupt domain switching when the bias field acts against unswitchable polar domains (outlined in red) and imprint; domains of different sizes or bundles of domains switch forming $P^{\uparrow}$ domain avalanches (i,ii,iii).*

Based on all data above, we devise a simple microstructural model than accounts for the observed differences. In Figures 3.10 (c) and 3.10 (f) we sketch the ferroelectric domain evolution as a function of the external bias as derived from the experimental data, and explicitly considering: the existence of an imprint field (E_{imp}) pointing down (from Pt to LSMO) and the different dynamics of HRS to LRS and LRS to HRS processes. The imprint field in

ferroelectric thin films may have a variety of origins, including the presence of unswitchable domains, asymmetric electrostatic boundary conditions, or the presence of polar defects (oxygen vacancies for instance) just to mention a few. For simplicity in the sketches in Figures 3.10 (c,f), we assume here that imprint is associated to the presence of unswitchable polar domains and as a sake of sketch clarity, we locate them at the LSMO/BTO interface (outlined in red). We describe first the results of Figure 3.10 (b), starting from an initially poled-up ($P^{\uparrow}$) state [(i) in Figure 3.10 (c)] obtained by a suitable $V < 0$ pulse. When a voltage $V > 0$ ($V < V_{C+}$) is applied (as in Figure 3.10 (a,b)), the pre-existing $P^{\downarrow}$ and new $P^{\downarrow}$ domains [(ii) and (iii) in Figure 3.10 (c)]. Thus, along the i-ii-iii path the junction resistance gradually increases (because $P^{\downarrow}$ corresponds to HRS) in agreement with the experimental observation [Figure 3.10 (b)]. This nucleation and expansion of $P^{\downarrow}$ is the process that can be roughly described by a modified KIA process. The I(t) time-dependence of Figure 3.10 (b) can be well describe by an stretched exponential behavior (dashed line) as expected from the Kolmogorov-Avrami-Ishibashi (KAI) model[60,79] suggesting that a random nucleation and lateral expansion until coalescence of $P^{\downarrow}$ domains. Similar conclusion had been reported earlier in BTO thin films,[69] However, numerical analysis of the KAI fit in Figure 3.11 shows that the extracted exponent in the stretched exponential is smaller ($n \approx 0.64$) than the smallest possible value ($n = 1$) (bounded by the dimensionality ($D > 1$) of the domain growth system). This indicate that the simplifying assumptions of the KIA model are not fulfilled. Similar discrepancy has been often encountered in ferroelectric thin films. Jo et al.[61] suggested that a Lorentzian distribution of nucleation times, associated to local field variation originating from defect dipoles or others at domain pinning sites, could account for the observed $n < 1$. In the present case, the unavoidable surface and interface roughness could contribute to the suggested distribution of nucleation times.

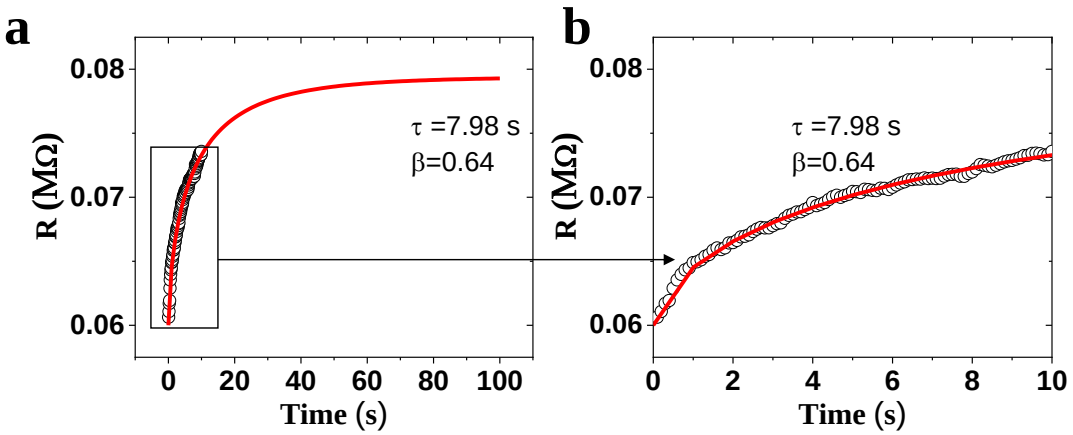


Figure 3.11 *Time-dependente I(t) data collecte in the Pt/BTO/LSMO junction (J_8) after setting the LRS by an appropriate V < 0 wriring pulse (sketch of measuring sequence in Figure 3.10a) Data collected (open symbols) and fitted data (red curves) using* $r(t) = r1 + r2\{1 - exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\}$. *Fitting parameters are indicated.*

We next describe the reverse switching process from $P^{\downarrow}$ to $P^{\uparrow}$ under a subcoercive voltage bias (experimental data Figure 3.10 (e)). We start from a $P^{\downarrow}$ state [(i) in Figure 3.10 (f)] obtained by application of a suitable V > 0 pulse and zeroing it (Figure 3.10 (d)). We subsequently apply a negative V < 0 field, smaller that the corresponding coercive field ($|V| < |V_{C-}|$, Figure 3.10 (d)) and we follow the evolution with time of the junction resistance. Under negative bias, $P^{\uparrow}$ domains should nucleate and expand. We notice however that the presence of pinned $P^{\downarrow}$ domains should locally stabilize the $P^{\downarrow}$ domains due to the energy-favored tail-to-head relative ordering. Moreover, the nucleation process of reverse ($P^{\downarrow}$) domains should be modified by the presence of the imprint field. Indeed, the critical radius of domain nucleation is proportional to ~ $1/(V \pm z \cdot E_{imp})$ where V is the potential applied and ($z \cdot E_{imp}$) is a descriptor of the local voltage associated to the imprint field, and + (-) sign apply when the imprint field adds (opposes) to the applied field.[66,67] Therefore, the critical radius gets larger when the applied field E is antiparallel to E_{imp} thus retarding nucleation, enhancing domain wall pinning and ultimately hampering domain motion. Upon increasing applied voltage, domains walls eventually depin and bundles of domain move a certain distance to a new pining site, in avalanche-like process, as observed in PZT thin films.[63,74] In short, bundles of $P^{\downarrow}$ domains

switch to $P^{\uparrow}$, as depicted in steps [(ii), (iii) in Figure 3.10 (f)] and correspondingly, jumps of the increasing conductance are observed in the I(t) data (Figure 3.10 (e)).

3.5 Conclusion

The experiments above show that asymmetric RS dynamics observed in BTO tunnel devices, can be directly linked to the presence of electric field imprint likely associated, but not necessarily, to the presence of unswitchable polar regions. They induce asymmetric domain grow and switching depending on the polarity of the driving filed with respect to the unswitchable domains. Here, we have observed and analyzed the asymmetry of the switching process on the basis of the ER (I-V) data of nanometric thin tunnel junctions. Recently Balke et al. obtained a direct visualization by piezo force microscopy of an asymmetric switching process in symmetric parallel planar $SrRuO_3/BiFeO_3/SrRuO_3$ capacitors [68]. In agreement with current theories [64,80,81] and earlier experiments[69] of preferential nucleation in one electrode in symmetric capacitors, they also conclude that a build-in electric field at the ferroelectric/electrode breaks the symmetry of the capacitor geometry and ultimately leads to different switching behavior for positive or negative switching voltages.

Asymmetric RS has been observed in other RS devices such as in valence change memories (VCM), and more precisely in filamentary-type VCM. These devices typically display a strong asymmetry in the HRS to LRS switching process. It has been recently demonstrated that this asymmetric switching can be directly related to an asymmetric dissipation than in some cases can also stimulate and control ionic motion, with concurrent impact on device resistance.[82] Our data indicate that avalanches are visible when the system switches from HRS-to-LRS but not in the LRS-to-HRS switching, and thus one may wonder if domain avalanches are assisted by the higher power dissipated at the junctions when in the HRS. The observation (Figures 3.7(a-d)) that when increasing frequency (that is: shorter V(t) and thus less power dissipates at the device when in the HRS) the switching occurs at higher V_{c-} voltage, appears at first sight to be also compatible with a possible occurrence of thermal effects assisting or promoting domain avalanches. The present data at first sight, do not univocally exclude any of the suggested mechanisms. However, the experimental observation that the power consumption of the Pt/BTO/LSMO junctions in the HRS-to-LRS transition at $V < 0$, where avalanches occurs, is

smaller (30%) than the one consumed at the LRS-to-HRS switching peak (V > 0) (see Figure 3.12) indicates that thermal effects are not the driving force for the assymetric switching observed in micrometric (this work, see also in Ref [83] and nanometric [13] BTO tunnel barriers.

In the scenarios above, obtaining symmetric switching dynamics for positive and negatives seems to be intrinsically very challenging. However, the observed asymmetry can be properly handled; for instance, in ferroelectric memories, unipolar reading of the memory state (from LRS to HRS) appears to lead to steady and provide a robust output; negative reading could also be handled if the abrupt conductance jumps are nor detrimental to digital data storage. However, the results presented here may have more important implications for the integration of ferroelectric materials in neuromorphic computing, where knowing time-dependent evolution of the potentials triggering the presynapse responses is crucial and, as argued here, this is much depending on electrostatic and microstructural boundary conditions at the electrode/ferroelectric layer.

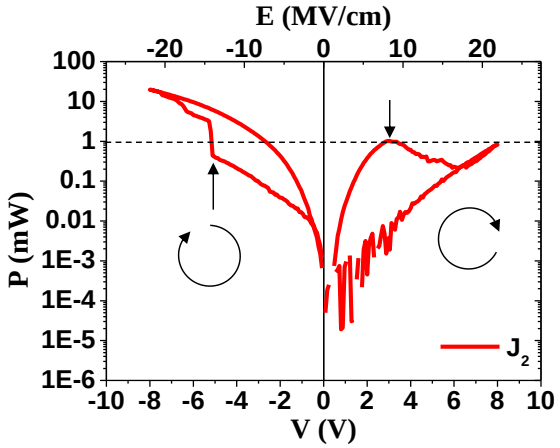
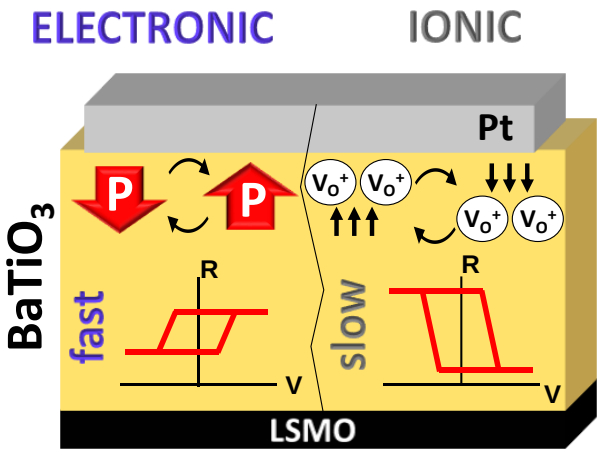


Figure 3.12 *Power consumption P of the Pt/BTO/LSMO junction (J_2). The correspondinh IV curve is shown in Figure 3.1c. It can be appreciated that avalanche switching visible in the V < 0 section of the I-V curve (pointing-up arrow), which correspond to the HRS to LRS transition, occurs at lover power (30%) than the one consumed at the LRS to HRS switching peak observed in the V > 0 region (pointing-down arrow). This observation suggest that thermal dissipation effects are not governing the asymetry of HRs-to-LRS trabsitions and viceversa.*

Chapter 4 Synergetic electronic and ionic contributions to electroresistance in ferroelectric capacitors

Sign and magnitude of ER in BTO ferroelectric thin film capacitors is modulated by modifying the writing electric field pulses duration and by modifying the measurement temperature. The results are explained in the framework of electronic band structure reconfiguration caused by the ferroelectric switching and electric-field-driven ionic movent in the ferroelectric.



4.1 Abstract

Advanced use of ferroelectric capacitors in data storage and computing, relies basically on the change of their electrical resistance (*ER*) produced by the change of the electrostatic potential profile across the capacitor upon electric field-driven polarization switching. Here we report on the observation that BTO-based capacitors, sandwiched between metallic Pt and $La_{12/3}Sr_{1/3}MnO_3$ electrodes, display *ER* whose magnitude (up to 10^4 % at room temperature) and a remarkable sign-change ($ER > 0$, $ER < 0$) depending on the barrier thickness and writing pulse duration and temperature. Temperature-dependent measurements have been instrumental to obtain evidence of the presence of a thermally activated process additional to the pure electronic changes produced by ferroelectric polarization switch both contributing to *ER*. Detailed analysis allows concluding that the thermally activated process can be attributed to field-assisted ionic motion. It is argued that the relative balance between purely electronic and ionic diffusion processes, modulate the height of the interfacial Schottky barriers and consequently, are responsible of the observed variations of the magnitude and sign of ER.

4.2 Introduction

Ferroelectric tunnel capacitors are considered promising candidate for a next generation of low consumption memory devices and to be the building blocks of circuits with endless potentialities in present and future applications, from multilevel data storage to neuromorphic computing.[8,9,13] Essentially these devices consist on a metal/ferroelectric/metal (M/FE/M) structure, where two different states of electric resistance can be obtained by switching the direction of the polarization (*P*) of the ferroelectric barrier. Indeed, it has been shown that huge changes of resistance (*ER*) as large as 10^4 % can be achieved in metal/BTO/metal capacitors or similar structures.[9,10,53,54,56,84,12,13,18,48–52]

In spite of the simplicity of the structure of the device, deep understanding of its response is challenging. Shortly, if only electronic processes are considered, the scenario for a ferroelectric tunnel device (few nanometer thick ferroelectric barrier) is as follows.[16,23,85] The ferroelectric material is embedded within two metal electrodes ($M_{1,2}$) of given work-functions and an energy

barrier (E_0) exists for electrons to cross the ferroelectric. The $M_{1,2}$ electrodes also provide the necessary charges to screen the surface charge of the ferroelectric. If different metallic electrodes are used, the electronic screening length ($\delta_{1,2}$) is not identical at both sides of the junction and thus an electric field (E-field) exists within the ferroelectric that revers its sign when P is reversed. The internal E-field changes the height [$\Delta\phi \approx \pm P\ (\delta_1 - \delta_2)$] of the E_0. Thus, two different barriers $E_0 \pm \Delta\phi$ are obtained when reversing P and consequently the junction resistance differs for both states [$R(P^{\downarrow}) \neq R(P^{\uparrow})$]. The corresponding change of junction resistance named ER [$ER = R(P^{\downarrow}) - R(P^{\uparrow}) / \min (R(P^{\downarrow}), R(P^{\uparrow}))$] is the figure of merit of the junction. The exponential dependence of the tunneling current on the barrier height accounts for the large ER values observed and its sign is fixed and dictated by the screening length of the electrodes. This simple model has been widely used to describe the ER of ferroelectric tunnel junctions, most commonly fabricated by epitaxial growth of the ferroelectric layer (perovskite oxide structure) on lattice-matching $(La_{2/3}Sr_{1/3})MnO_3$ (LSMO) or $SrRuO_3$ metallic perovskite electrodes.[18,23,86,87] In presence of defects, such as oxygen vacancies, the ferroelectric layer can be viewed as a doped semiconductor and thus the polarization-dependent internal E-field can change the width of the depletion layer in Schottky barriers at interfaces,[27,33,56,88] thus changing also the effective barrier width. In this case, P reversal induces a simultaneous change of barrier height and width, both contributing to ER.[56]

Alternatively, metal/ferroelectric/semiconducting (M/FE/SC) structures have also been explored. Interestingly, it has been reported that the polarization-dependent depletion-layer width within the n-doped semiconducting electrode, Nb:STO, results in large ER,[48] which may reach a giant ER ($\approx 10^5$ %) using optimally doped semiconducting electrodes.[34] Therefore, the electronic nature (p or n-type) of the ferroelectric[89,90] and the electrode[91] modulates the magnitude of ER and its sign.

Whereas the models above collect fundamentally electronic reconstruction processes, the potential role of ionic motion, and in particular oxygen vacancies motion under, the E-field was put forward by D. J. Kim et al.[55] or R. Soni et al.[92] by claiming that the E-field could promote redox processes at interfaces. The presence of mobile oxygen vacancies within the ferroelectric layer may largely impact ER.[93] Indeed, M. Li et al.[94] and others[95] showed that largely different ER were observed depending on the growth conditions (oxygen pressure) of

the ferroelectric layer (BTO), and argued that a key ingredient was the oxygen-vacancy screening of *P* and the resulting modifications of the interfacial Schottky energy barriers. The picture was expanded further by Q. H. Qin et al.[96] by claiming that the observed *ER* basically comes from an electronic reconstruction at the used LSMO electrode: an E-field controlled oxygen motion within the LSMO layer produces a hole-depletion, which results in a metal to insulator transition with the concomitant increase of the tunneling width. Consequently, it was argued that the observed *ER* is not primarily related to the ferroelectric polarization, but it results from purely ionic motion within the electrode.

This brief summary illustrates the existing debate between purely electronic and ionic processes, and how challenging is to discriminate them on the *ER* response of ferroelectric capacitors. Understanding the mechanisms contributing to *ER* is crucial for a proper engineering of ferroelectric switching devices as those considered in advanced applications such as crossbar RS devices[83] or as a building blocks for neuromorphic computing.[97]

Here we contribute at solving this puzzle by reporting on the ER measured on Pt/BTO/LSMO capacitors. The bottom line of our strategy is that polarization-controlled electronic reconstructions and ion motion can both contribute to the ER under the influence of the applied E-field. Ions or other charged-defects, most likely oxygen vacancies (V_O), may drift under the effect of E-field[98,99] and modify the electrostatic boundaries conditions including polarization screening and Schottky barrier at interfaces.[88] As ionic drift is temperature and time dependent, instrumental for the proposed research is to explore the role of the duration of the writing voltage (so called *writing time,* τ_w) and the temperature dependence of the ER. Therefore, we report on the *ER* of Pt/BTO/LSMO capacitors where the BTO thickness has been varied gradually (≈ 30 - 110 nm) and compared with *ER* of ultrathin thin (few nanometers) BTO barriers. It turns out that for the (relatively) thinner films (≈ 35 nm), *ER* is observed to be positive ($ER > 0$) as in ultrathin tunnel barriers (≈ 4 nm). However, the reverse sign ($ER < 0$) can be observed in thicker barriers (≈ 110 nm). In fact, for films of intermediate thickness at room temperature (≈ 70 nm), it turns out that a change of sign of *ER* (from $ER > 0$ to $ER < 0$) depends on the writing time τ_w. A key discovery is that the critical time where the *ER* sign reversal occurs (τ_{CRIT}) depends on the measuring temperature and on film thickness. These

findings allow disentangling purely electronic from ionic effects in a device and to achieve a more complete understanding of the *ER* phenomenon in ferroelectric capacitors.

4.3 Samples

Ferroelectric capacitors have been fabricated by pulsed laser deposition by growing thin films of ferroelectric BTO of thicknesses $t_1 \approx 35$ nm, $t_2 = 70$ and $t_3 = 110$ nm on top of an epitaxial metallic $La_{0.67}Sr_{0.33}MnO_3$ (LSMO) (30 nm) layer deposited on $SrTiO_3$(001) substrates. Two series of samples (I & II) have been grown under nominally identical conditions and having similar thickness. A nanometric tunnel BTO ($t_0 \approx 4$ nm) has also be grown for comparative purposes. Films thickness is determined from the growth rate calibration and the used laser pulses. Details of growth conditions and structural characterization of the films have been reported elsewhere.[7,100–102] Square Pt electrodes (20 nm thick, area 3600 μm^2 for t_1, t_2 and t_3 samples and 250 μm^2 for t_0) were subsequently deposited ex-situ, by sputtering, on the BTO film surface by using a shadow mask. About 300 electrodes, labelled J_N, where N is the reference number for each electrode, are prepared simultaneously. Data in this chapter refer to samples of series I. Consistent results have been obtained using samples of series II, as shown in Supporting Information.

4.4 Electroresistance

4.4.1 Time dependence of I-V characteristics

We will first describe the results obtained on a Pt/BTO/LSMO capacitor of BTO intermediate thickness (t_2 = 70 nm). The sample has been connected to the voltage source and measuring set-up via a top Pt electrode; the bottom electrode LSMO was grounded (Figure 4.1a). We first focus on the change of conductivity (evaluated from the *I-V* characteristics) as a function of the amplitude (V) and duration (τ_w) of the writing voltage pulse V_w (sketch in Figure 4.1b). In Figure 4.1c, we show the reading *I-V* curves collected on junction J_1 (J_N is the junction code in the sample) after prepoling the device with +8 V (red) and -8 V (black) pulses of duration τ_w = 20 μs (solid lines) and τ_w = 20 s (dotted lines). Notice that the current scale for τ_w = 20 s (dotted lines) has been multiplied by 1/100 to allow data comparison. Some obvious

observations emerge: a) there is a significant change of conductance of the device depending on the sign of prepoling voltage, b) after a short writing pulse (τ_w = 20 μs) the resistance is smaller for V_w = -8 V than for V_w = +8 V. That is, the OFF state is observed for $V_w > 0$. This is in agreement with our own early findings in ultrathin tunnel barriers[56,71,103] as well as with results from literature,[9,13,55] and c) after a long writing pulse (τ_w = 20 s) the resistance of the junction is radically reduced (roughly ≈ 1/100) and the resistance is smaller for V_w = + 8 V than for V_w = - 8 V. That is, the OFF state is observed for $V_w < 0$. We define the ER as $ER = (R^+-R^-)/\min(R^+,R^-)$ where (R^+, R^-) indicate the resistance measured for V^+ (V > 0), V^- (V < 0) and $\min(R^+,R^-)$ their minimal value. Accordingly, $ER > 0$ is positive for τ_w = 20 μs and ER sign is reversed ($ER < 0$) for τ_w = 20 s. Therefore, data indicates that, contrary to the common wisdom, the sign of ER is not simply dictated by the nature of the electrodes.

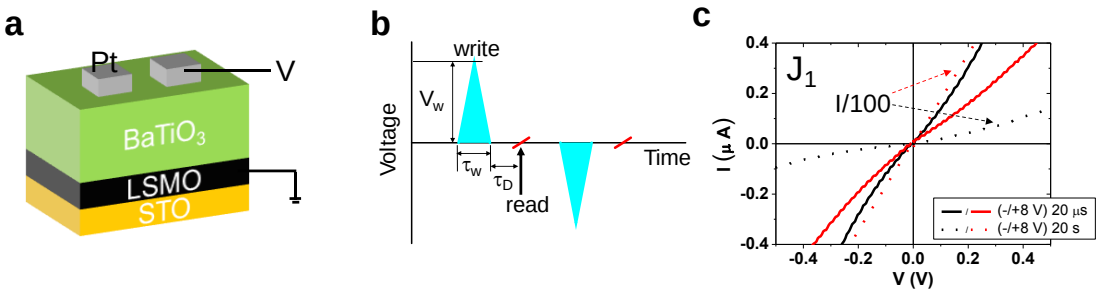


Figure 4.1 *(a) Sketch of the Pt/BTO/LSMO junctions and electrical measurement configuration. (b) Sketch of the* I-V *measuring protocol, for writing and reading junction resistance. The delay time (τ_D) is fixed to 1 s. Pulse of* τ_w *= 20 μs (black and red solid lines), and* τ_w *= 20 s (black and red dotted lines, note the current has been divided by 100). The measurements correspond to the 70 nm – BTO sample.*

4.4.2 Time dependence of electroresistance

To gain insight into this intriguing change of sign of ER, we first explored the ER as a function of poling voltage ER (V_w) using suitable voltage-pulses train (see section 2.4). In order to put in context the results and main message of the present manuscript, we first show in Figure 4.2 **(**a,b) the ER (V_w) loops of the 4 nm BTO barriers, written with V_w pulses of duration τ_w = 20 μs and τ_w = 20 s, respectively. We note that the junctions display a remarkably large ER (≈ 8 10^4 %) irrespective of the τ_w that is among then largest values reported for similar junctions

at room-temperature.[56,71,103] It can also be appreciated that the loops are anticlockwise for any writing time and have a remarkable squareness indicating the stability of the ON/OFF states and reflecting the quality of the films.

We now describe the corresponding results obtained on a Pt/BTO/LSMO capacitor of BTO intermediate thickness (t_2 = 70 nm). The results for τ_w = 20 μs and τ_w = 20 s are shown Figures 4.2c,d. The *ER* (V_w) loops in Figures 4.2c and 4.2d clearly bear some similitudes with those observed in tunnel devices. However, consistently with data in Figure 4.1c, two main differences emerge: a) the ER of the shortly-written junction (Figure 4.2c) is only of about 200 %, which is about 10^2 smaller than that of tunnel barriers (Figures 4.2a,b) and the loop is substantially pinched, and b) the loops are anticlockwise for τ_w = 20 μs, as in tunnel barriers, but clockwise for τ_w = 20 s (Figure 4.2d), reflecting the change of sign of the *ER*, already noticed in Figure 4.1c. As mentioned, when using τ_w = 20 s the OFF state is written after V_w < 0, the *ER* radically increases up to about 4.6 10^3 %, the squareness of the *ER*(V_w) loop is definitely improved and the ON/OFF states robustly persists until $V_w \approx \pm$ 6V (Figure 4.2d). Comparing the values of the resistance in Figures 4.2c and 4.2d it is obvious that when using longer writing pulses, the device resistance is reduced as already observed in Figure 4.1c.

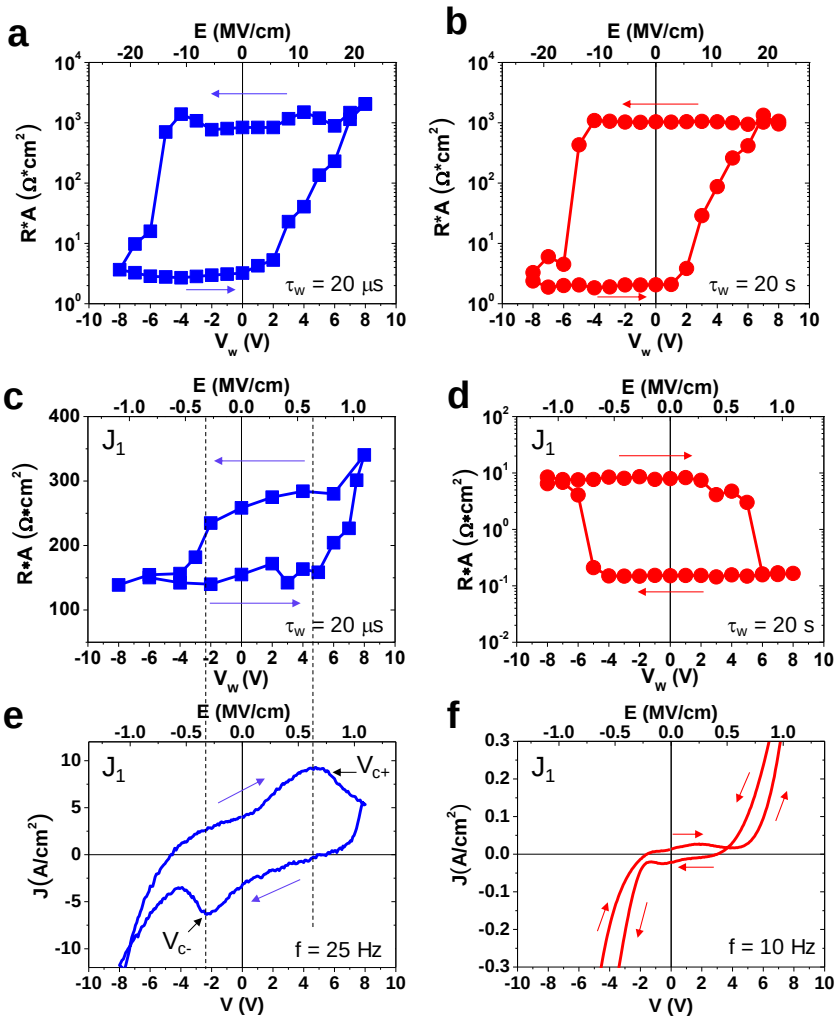


Figure 4.2 *(a,b) ER loops collected with* τ_w *= 20* μ*s and* τ_w *= 20 s, respectively for the t ≈ 4 nm BTO sample. (c,d) ER loops collected with* τ_w *= 20* μ*s and* τ_w *= 20 s, respectively for the* t_2 *= 70 nm sample. (e,f) J-V loops following the -8 V to +8 V to -8 V path measured at 25 kHz and 10 Hz.*

To disclose the mechanism behind the distinct responsiveness of the junctions depending on τ_w shown in Figures 4.2c and 4.2d, we recorded the *J-V* loops up to 8 V at different frequencies (*f*). The results collected using *f* = 25 kHz and 10 Hz are shown in Figure 4.2e and 4.2f. The selected frequencies were chosen finding a compromise between being similar to the writing time τ_w used in Figures 4.2c and 4.2d, and large enough to make displacive current contribution sizeable. In the *J-V* curve recorded at 25 kHz (Figure 4.2e) one can appreciate the polarization switching peaks. It can be noticed that the voltage positions at which the switching peaks occur (dashed lines around +4 V and -3.5 V), fingerprints of the coercive fields (V_{C+} and V_{C-}) of the

ferroelectric film, are closely coincident with the voltages where the corresponding $ER(V_w)$ loop (Figure 4.2c) display the most remarkable changes of resistance. Further analysis allows to conclude that the current peaks of Figure 4.2e correspond to ferroelectric switching (see Figure 4.3).

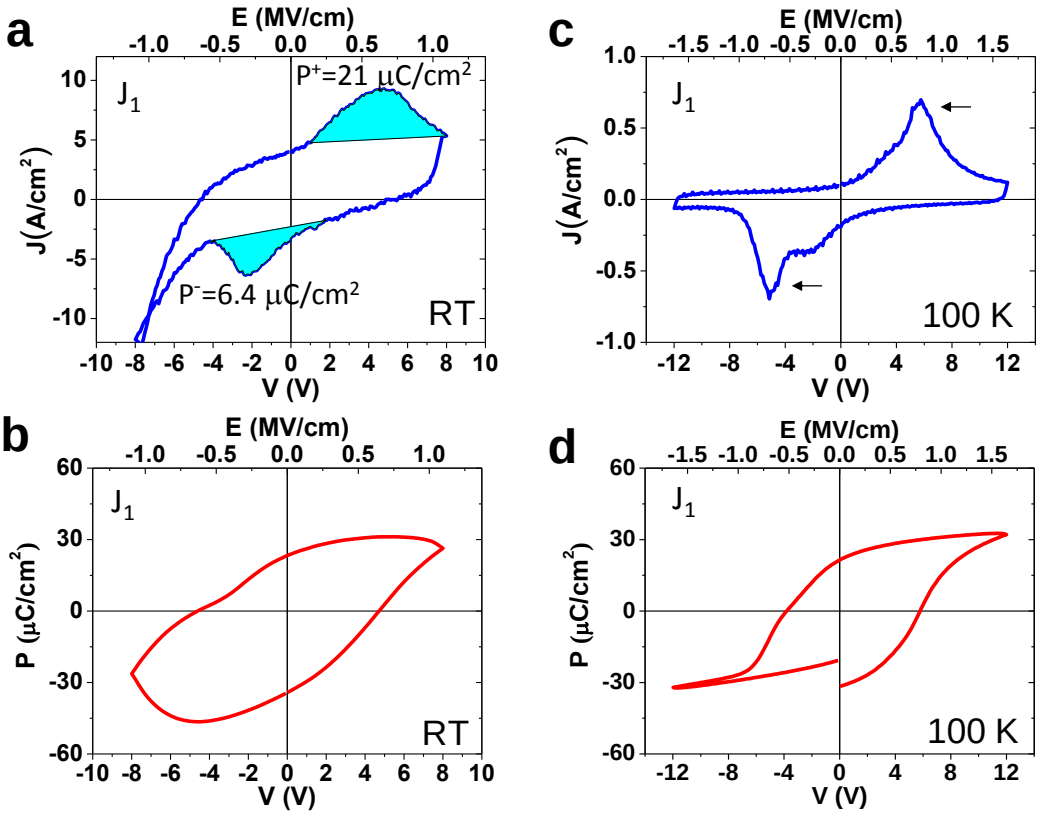


Figure 4.3 *(a)* J-V *loops of J_1 junction of the* t_2 *=70 nm BTO capacitor measured at room temperature, at 25 kHz. Polarization values for positive and negative switching, evaluated from the area underneath the switching peak (≈2·*P_r*, where* P_r *is the remanent polarization) are 21 μC/cm² and 6.4 μC/cm², respectively. The lateral shift of the* J-E *loops signals the imprint field. The asymmetry of the polarization values signals the presence asymmetric leakage current contribution, which might have hidden the presence of switching current [see panel b)]. This polarization value is smaller than that obtained for bulk BTO (2·*P_r *= 52 μC/cm²). (b)* P-V *loop recorded at room temperature. The presence of leakage is very important not allowing to extract reliable polarization value as indicated in panel (a). (c)* J-V *loops measured at 100 K at 1 kHz. Here the switching ferroelectric current peaks are well-visible, because the reduced leakage current compared with the measurements at room temperature. (d)* P-V *loop recorded at 100 K at 1 kHz. Extraction of polarization is more obvious from data collected*

at low temperature. Values near 30 μC/cm² (2·Pr = 60 μC/cm²) are obtained. Thus, it is confirmed that the switching peaks observed at room temperature [panel (a)], correspond to the ferroelectric switching of the film, somewhat obscured by the presence of the leakage current.

4.4.3 Retention of R(ON) and R(OFF)

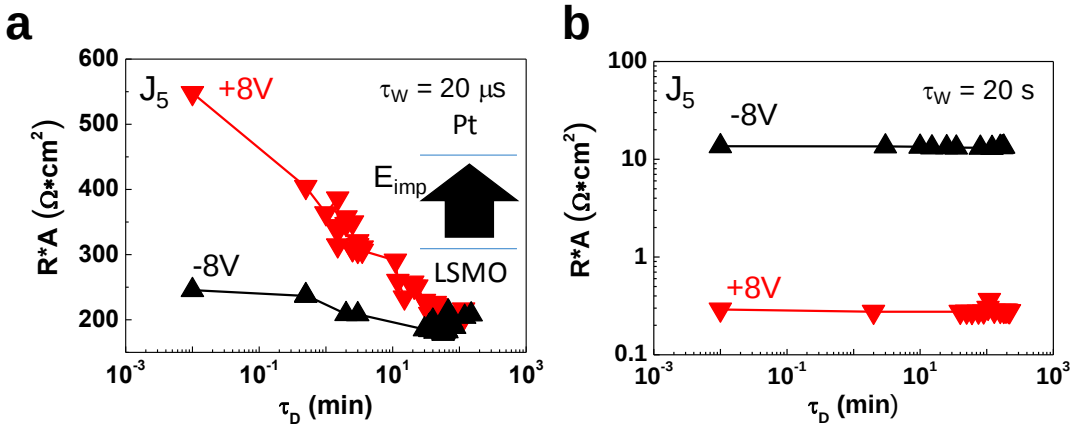


Figure 4.4 *Retention measurements for +8 V (red) and -8 V (black) prepoled resistive states after applying a triangular pulse of 20 μs (a) and 20 s (b), respectively. The retention experiment is performed following the procedure described by Figure 4.1b varying* τ_D.

The shift of J-V along the positive voltage indicates the presence of an internal E-field favoring upwards polarization state as shown in Figure 4.4. Retention experiments for the 70 nm BTO thin film capacitor after prepolarizing it with short (τ_w = 20 μs) and long (τ_w = 20 s) writing times. The important effect of internal E-field, revealed already in Figure 4.2d, can be well appreciated in the retention experiment and manifested as faster depoling of the polarization up (V^+) state. Indeed, in Figure 4.4a, it is shown that the resistance value for the OFF state decreases until converging with the ON state. This is an indication that the ferroelectric state corresponding to polarization pointing towards Pt is favored by the mentioned internal electric field. Instead, in Figure 4.4b, it is shown that both resistance values for OFF and ON state remain constant for the explored τ_D values, illustrating the different origin of the ON/OFF states and the negligible role of the imprint field when the junction response is mainly dictated by ionic motion as argued in this chapter.

Therefore, we conclude that the *ER* recorded at high frequency (25 kHz) (short writing time) is intimately connected with the ferroelectric polarization switching. Interestingly, this conclusion is at odds with what is observed in the *J-V* curves recorded at lower frequency (*f* = 10 Hz) of Figure 4.2f. Indeed, the switching peaks appear at roughly about +2 V and -1 V. The fact that the ferroelectric switching peak occurs at lower voltage when reducing measuring frequencies is in agreement with the well-known dependence of V_C of frequency observed in ferroelectrics.[72] More interesting is the observation that the abrupt change of conductance in the *J-V* curves of the junctions occur at significantly larger voltages that the corresponding V_{C+} and V_{C-} (see Figure 4.2d). This suggest that when junctions are driven by long voltage pulses, the observed changes of resistance are not primarily ruled by the polarization switching. Data in Figures 4.2c,d,e,f correspond to junction J_1. Similar *ER* data have been collected in other junctions on the same sample (see Supporting Information S1).

4.4.4 Temperature Dependence of ER(ON) and ER(OFF)

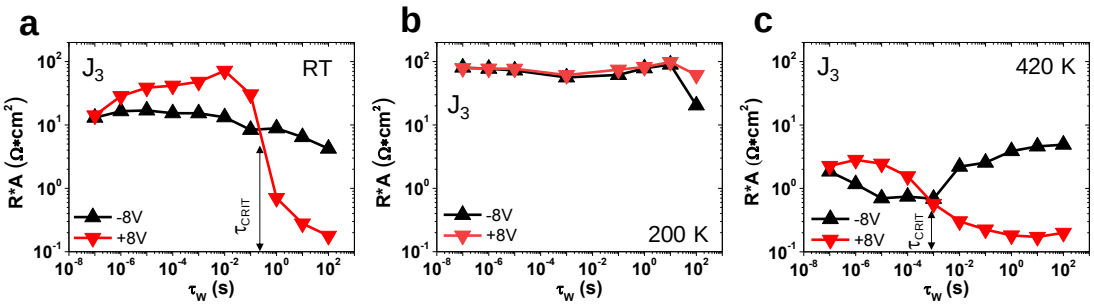


Figure 4.5 *Resistance times area after prepolarizing the junction (writing) with V_w = -8V/+8V pulses of different duration τ_w at different temperatures: (a) RT, (b) 200 K and (c) 420 K (junction J_3). The arrows indicate the critical writing time (τ_{CRIT}) where ER changes of sign.*

To get a further insight, we recorded the change of resistance and ER of a junction as a function of τ_w and temperature. In Figure 4.5a, we show data recorded at room temperature (RT), using writing times τ_w spanning more than 9 orders of magnitude (from 80 ns to 100 s). It can be appreciated that τ_w longer than ≈ 100 ns are required to produce visible changes of the junction resistance. Indeed, $ER \approx 0$ for τ_w = 100 ns and ER gradually increases up to 10 ms. In this τ_w range, *ER* is positive and the corresponding $ER(V_w)$ loops are similar to that of Figure 4.2c.

Data in Figure 4.5a also indicate that *ER* reduces in magnitude when τ_w is further increased above 10 μs until zeroing at some critical writing time τ_{CRIT}(RT) ≈ 200 ms and eventually increases again for τ_w > 200 ms but now having a negative *ER*, that is: $R^+ < R^-$. This behavior is in agreement with data in Figure 4.2d, where the $ER(V_w)$ loop collected τ_w > 10 s was depicted. Data collected at T > RT follow the same trend, that is *ER* changes its sign when increasing τ_w, as illustrated in Figure 4.5c where data collected at 420 K are shown. When comparing to data collected at room temperature, the most perceptible variation is that the critical writing time for the change of sign of *ER* is definitely shorter, in fact it is reduced by about 3 orders of magnitude: τ_{CRIT}(420 K) ≈ 1 ms (see in Supporting Information S2 similar data and behavior in other junctions). In contrast, data recorded at lower temperature (200 K, Figure 4.5b) indicates that there is no change of sign of ER but only signs of junction failure at the longest writing time. Overall, these data suggest that different competing mechanism may contribute to the ER of the junctions, whose relative weight could be temperature-dependent.

Note that this lower time limit is below the time constant of the measuring circuit in Figure 4.6. Determination of the time constant of the circuit. We applied a triangular voltage waveform to determine the circuit time constant for the t_1 = 35 nm sample. We selected this sample because it is the thinner one; thus, the maximum capacitance and the longest circuit time constant (τ = RC, where τ is the time constant) is expected. Therefore, it is the time constant of our circuit the one limiting the observation of switching.

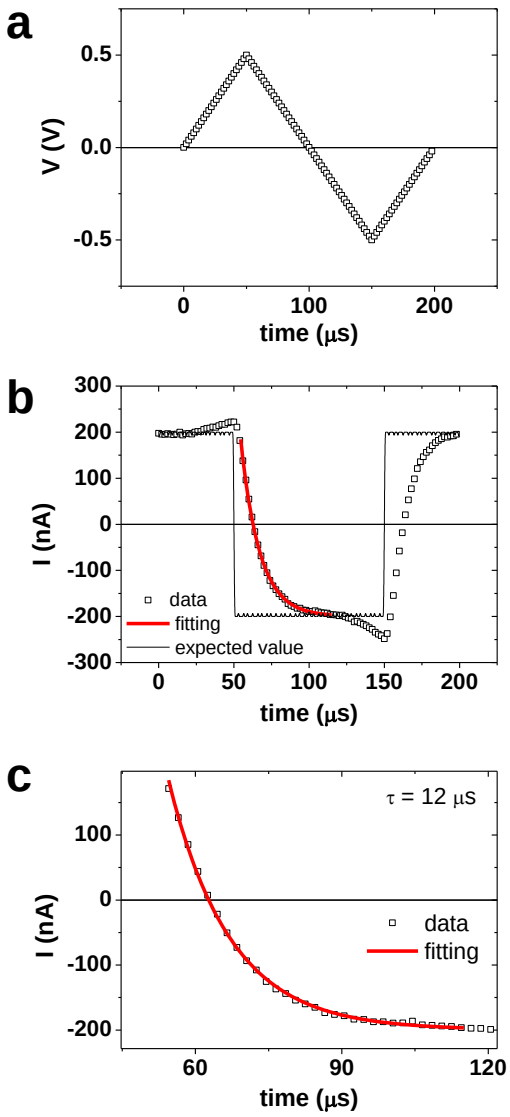


Figure 4.6 *Applied voltage dependence on time. It corresponds to a triangular bipolar signal of 0.5 V of amplitude with a frequency of 1 kHz. (b) Measured current (empty symbols) in the* t_1 *= 35 nm film capacitor. The black thin line is the expected pure displacive current without series resistance and leakage currents contributions. It can be observed that the measured current exponentially approached the expected one. This time-delayed response is due to the circuit time constant. The red thick line corresponds to the fitting of an exponential curve (*$I=I_0e^{t/\tau}$*, I_0 is the amplitude and τ the circuit time constant). We obtained* $\tau \approx 12$ *μs. (c) Zoom of (b) to better visualize the data fit.*

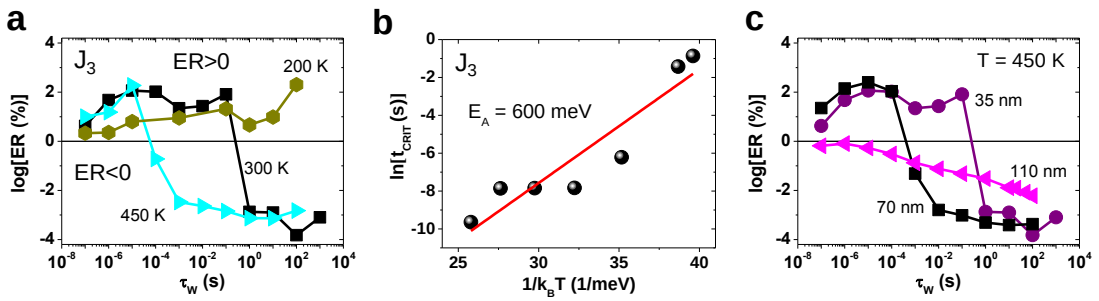


Figure 4.7 *Dependence of the ER [ER = $(R^+-R^-)/min(R^+,R^-)$] on writing time τ_w at some selected temperatures, of J_3 junction of the t_2 = 70 nm sample. Note that the negative sign of log(ER) corresponds to negative ER sign. (b) Temperature dependence (inverse) of τ_{CRIT}. Solid line is the data-fit using an Arrhenius model; the corresponding activation energy is ≈ 600 meV. (c) Dependence of ER dependence on the writing time τ_w of samples having different BTO thicknesses (t_1 = 35 nm (purple), t_2 = 73 nm (black) and t_3 = 110 nm (pink)), measured at a fixed temperature (450 K).*

To derive the temperature dependence of τ_{CRIT}, we have explored the temperature dependence of *ER* in the 200 - 450 K range. In Figure 4.7a we show $ER(\tau_w)$ data collected at 200, 300 and 450 K. Data for other temperatures are included in Supporting Information S3. Data in Figure 4.7a clearly indicate that the sign change of *ER* occurs at progressively shorter (longer) writing times when the sample is warmed (cooled). In fact, as depicted in Figure 4.7a, at the lowest temperature, *ER* remains positive for all explored τ_w. Notice that, as mentioned, using writing times longer than 10 s, typically results on an irreversible damage of the junction). These observations suggest that a thermally activated mechanism could be at play. In Figure 4.7b, we plot the temperature (inverse) dependence of τ_{CRIT} recorded on the same junction. The corresponding raw $ER(\tau_w,T)$ data are in Supporting Information S3. The τ_{CRIT} *vs* $1/k_BT$ Arrhenius-like data in Figure 4.7b indeed suggest an activated behavior. From the fit we extract an activation energy of about E_A = 600 meV.

If the observed variation of the *ER* with τ_w and temperature reflect the dynamics of the electronic and/or ionic species within the BTO barrier eventually modifying the electronic properties of the metal/ferroelectric interfaces, one could suspect that at some fixed temperature, τ_{CRIT} should depend the BTO thickness. Therefore, we have performed similar measurements on capacitors having different BTO barrier thicknesses (t_1 = 35 nm and t_3 =

110 nm). In Figure 4.7c, we show the dependence of *ER* on τ_w for t_1, t_2 and t_3 samples at 450 K (raw data in Supporting Information S4). This particular temperature has been selected because at this temperature, the t_1 and t_2 barriers display the change of sign of *ER* within the available τ_w range and allows monitoring the thickness dependence of τ_{CRIT}. Data in Figure 4.7c, show that the change of sign occurs at progressively shorter time, which is: τ_{CRIT} get shorter, when increasing BTO thickness. In fact, for the thickest sample (t_3 = 110 nm) only the *ER* < 0 state can be seen at the selected temperature. In short, the room temperature *ER*(τ_w) data display a fully consistent behavior with the 450 K data shown in Figure 4.8. Dependence of the ER of t_1, t_2 and t_3 samples on τ_w collected at room temperature. Raw data is also included in panels b,c,d.

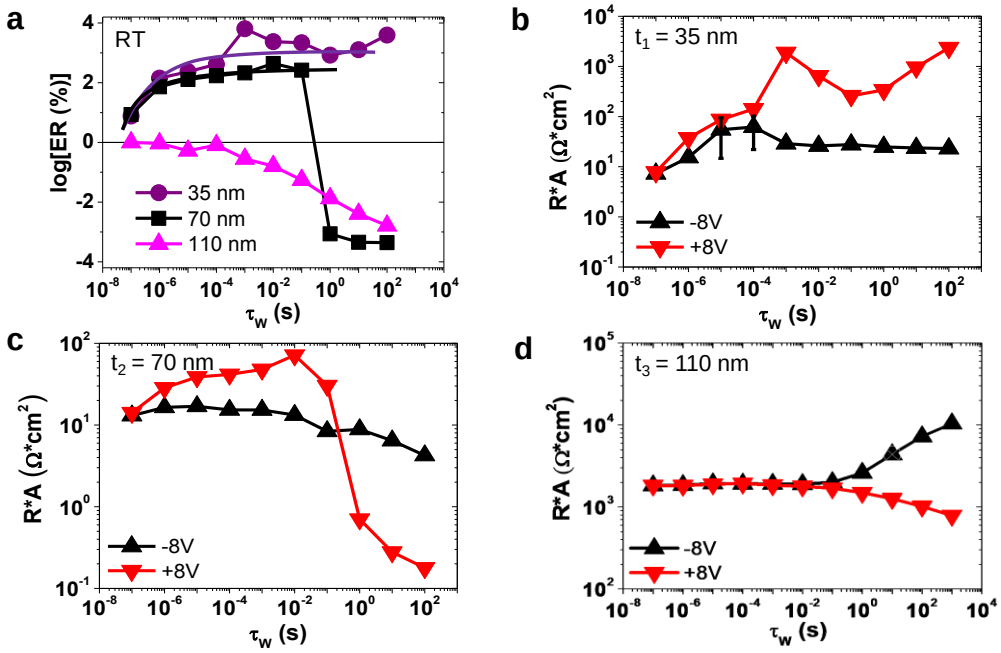


Figure 4.8 *Dependence of the ER on τ_w of t_1, t_2 and t_3 BTO capacitors at room temperature. (b,c,d) Resistance times area after prepoling the junction (writing) with V_w = -8 V/+8 V pulses of τ_w, for t_1, t_2 and t_3 BTO capacitors, respectively, measured at room temperature. The resistance of the t_3 = 109 nm sample was measured at -1 V, as indicated, due to its lower conductivity.*

4.5 Discussion

Overall the experimental results strongly suggest that the ER of BTO capacitors of thicknesses within the 30 – 100 nm range, appears to be ruled by two different mechanisms that dictate either $ER < 0$ or $ER > 0$ and whose strength depends on the duration of the writing pulse and measuring temperature. To rationalize these observations, we start by analyzing first the temperature dependence of τ_{CRIT}, which fixes the lower bound for the time scale where the slowest process, giving rise to $ER < 0$, governs the RS mechanism of the junction.

The exponential increase of τ_{CRIT} with temperature (Figure 4.7b) allowed to extract an activation energy $E_A = 600$ meV. It is interesting to notice that this value is comparable to the activation energy for oxygen vacancy diffusion reported for BTO and related perovskites, being oxygen vacancies the most common point defects in perovskite thin films and the ones with the highest mobility.[104–106] For instance, S. Zafar et al.[107] measured the time-dependent transient conductivity of (Ba,Sr)TiO_3 films and reported a $E_A \approx 1000$ meV, which was in reasonable agreement with values extracted from oxygen-diffusion experiments in titanate thin films.[108] Similarly, Y. B. Nian et al.[109] reported $E_A \approx 400$ meV in (Pr,Ca)MnO_3. Therefore, we can assume that oxygen migration determines τ_{CRIT}. An alternative view can be derived by noticing that if one assumes that τ_{CRIT} corresponds to the diffusion time of oxygen vacancies across the whole BTO film thickness to reach the interface, then $\tau_{CRIT} \approx 100$ μs (as observed for the t_2 films at 450 K) corresponds to a mobility $\mu \approx 5\ 10^{-8}$ cm^2/Vs, at $V_w = 5$ V, which is orders of magnitude smaller than typical electronic mobilities in these oxides (≈ 1 cm^2/Vs).

Therefore, we should build up band diagrams for the LSMO/BTO/Pt structures where electronic reconstructions are governing the response at short writing pulses and where ionic motion plays a role at long writing pulses. We first notice that the measured device structure can be viewed as a back-to-back Schottky diodes arrangement formed at the corresponding LSMO/BTO and BTO/Pt interfaces. Therefore, irrespectively of measuring bias configuration, one of the interface diodes is in reverse and thus this interface limits the current-flow across the device.[110,111] If BTO is assumed to be an n-type semiconductor,[112] when junction resistance measurements are performed with a V^+ on Pt, the LSMO interface is in reverse and thus the

corresponding Schottky barrier shall determine the *ER* of the LSMO/BTO/Pt capacitor. Accordingly, we focus our attention on the LSMO/BTO interface.

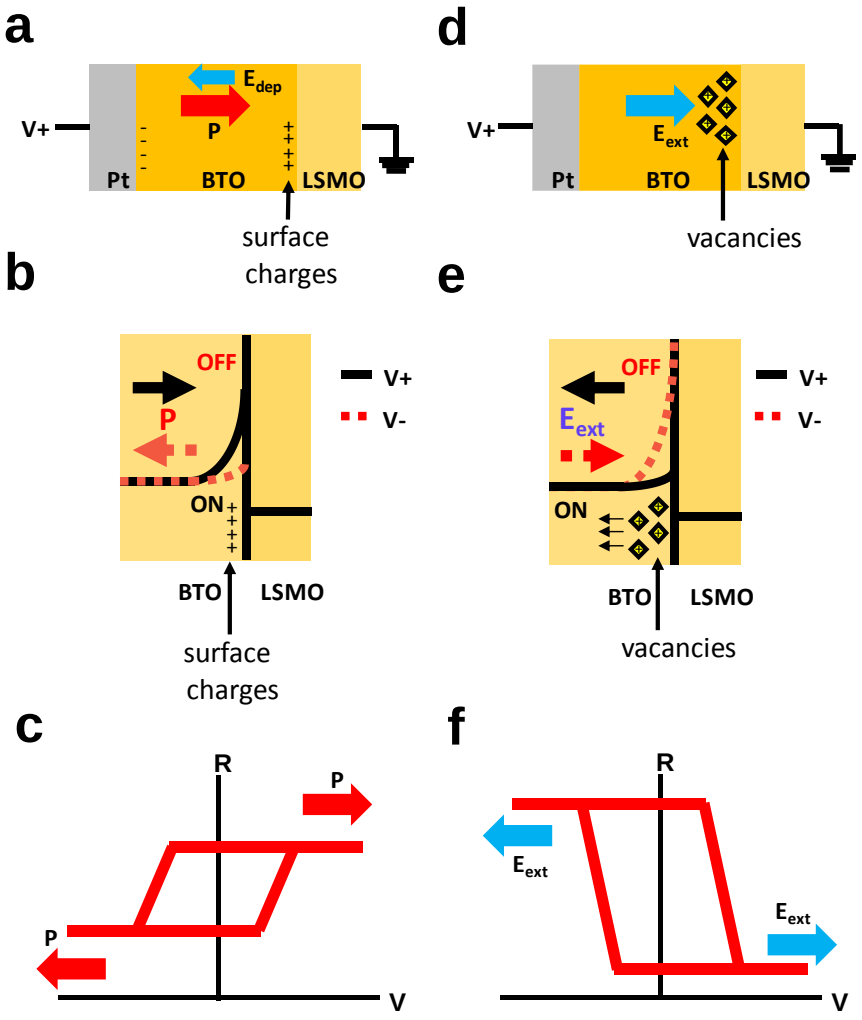


Figure 4.9 *(a) Sketch of polarization and depoling electric E-field directions for V^+ applied to Pt. (b) Sketch of the energy band diagram near the BTO/LSMO interface for V^+ and V^- when polarization is relevant (c) Sketch of amplitude and sign of ER loop resulting from the proposed scenario for short writing times when ferroelectric polarization and residual depoling field are relevant; ER is small and positive (d) Sketch of external applied electric field and oxygen vacancies (rhombi) accumulation for V^+ applied to Pt. (e) Sketch of the energy band diagram near the BTO/LSMO interface for V^+ and V^- when oxygen vacancies are most relevant. (f) Sketch of amplitude and sign of ER loop resulting from the proposed scenario for long writing times when oxygen vacancies are relevant; ER is large and negative.*

In Figure 4.9a, we sketch the LSMO/BTO/Pt capacitor. After prepoling the BTO film with V^+, the polarization points towards LSMO (P^+, red arrow). In Figure 4.9b, we sketch a Schottky barrier of height (Φ_{SB}) at the LSMO/BTO when P^+ points towards LSMO (solid line). Positive surface charges at the BTO/LSMO interface (signaled by positive symbols) had reduced Φ_{SB} compared with the non-polar case and increased the junction conductance (resistance ON). However, in presence of an imperfect and asymmetric polarization screening, a residual depoling field (E_{dep}) exists across the junction (blue arrow in Figure 4.9a).[113] If P^+ points towards LSMO (for V^+), the residual E_{dep} will produce a rise of the Φ_{SB} for V^+ as depicted in Figure 4.9b (solid line). Well documented in ultrathin BTO barriers, imperfect screening leads to an change of the barrier height depending on polarization direction; in LSMO/BTO/Pt the OFF state is commonly observed for P^+.[18,56,71,103,114] We have observed the same response in an ultrathin barrier, as shown by Supporting Information S5. Reversing P should result in a reduction of Φ_{SB} (Figure 4.9b, dashed line). Accordingly, OFF and ON states should be observed for V^+ and V^-, respectively, as depicted in Figure 4.9c, which is agreement with our observation (Figure 4.2c). In this scenario, the time response of the device is mainly dictated by the polarization switching process, which is known to be substantially fast.[115,116] It thus follows that the observed ER >0 [OFF(ON) for $V^+(V^-)$] at short writing times, reflects the ferroelectric polarization reversal and the concomitant modulation of the Schottky barriers (≈ 0.12 eV and 0.7 eV for LSMO and Pt sides).

We turn now to the response of the junctions to long writing pulses. In Figure 4.9d, we sketch the LSMO/BTO/Pt capacitor when an external E-field (E_{ext}) has been applied for a long time. As we have experimentally observed that for long writing time, the RS is not dictated by the polarization reversal, we omit P in the sketch and we only indicate E_{ext}. In Figure 4.9d, we depict $E_{ext}{}^+$ (towards LSMO) for V^+ applied to the Pt electrode (blue arrow). The positively charged oxygen vacancies under the action of $E_{ext}{}^+$, will be accumulated at the BTO/LSMO interface (solid rhombi) thus producing a reduction of Φ_{SB} and therefore the ON state is obtained (Figure 4.9e, solid line). For V^-, the reverse situation holds and thus the device is in the OFF state (Figure 4.9e, dashed line). The resulting, $ER(V_w)$ loop, sketched in Figure 4.9f, is agreement with our observation (Figure 4.2d). It is worth noticing here that local heating

associated to the larger thermal energy involved when using longer pulses could assist and even exacerbate ionic or vacancy motion as it is well documented in some RS devices.[36]

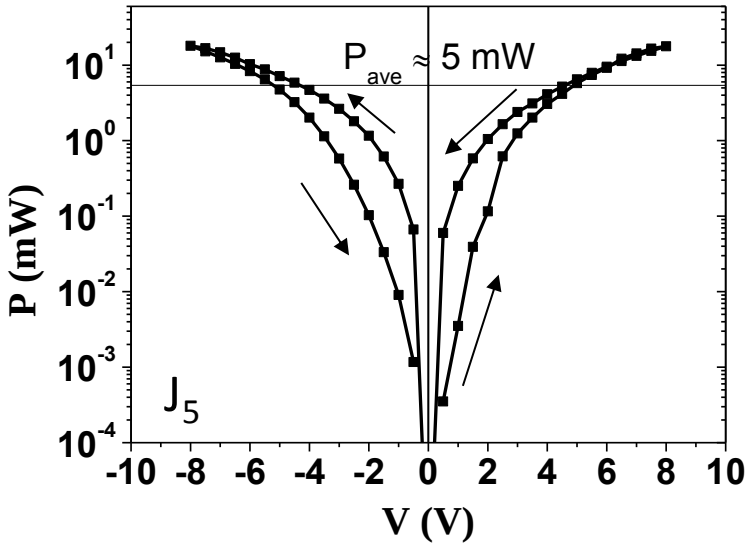


Figure 4.10 *Power as a function of voltage of the Pt/BTO (70 nm)/LSMO junction J_5. Data has been collected in quasi-static mode applying constant voltage for each collected power measurement using an integration time of 1 s.*

The average power dissipated in the loop is $P_{ave} \approx 5$mW. Therefore, we can estimate the energy dissipated to the sample for representative writing voltage pulses of 8V and τ_w = 20 μs and 20 s:

$$E(+8\text{ V}, 20\ \mu\text{s}) = P_{ave}/2 * \tau_w = 63\text{ mW}/2 * 20\ \mu\text{s} = 125\text{ nJ}$$

$$E(+8\text{ V}, 20\text{ s}) = P_{ave}/2 * \tau_w = 63\text{ mW}/2 * 20\text{ s} = 125\text{ mJ}.$$

In this estimate we used half of the power ($P_{ave}/2$), because for unipolar (instead of the bipolar cycle Figure 4.10) are typically used in the experiments reported in this chapter. The obtained values indicate that for the long writing times pulses, significant amount of energy, is dissipated. This might result in an increase of device temperature as reported in oxides-based systems, which might help ionic processes to occur.[36,117]

The model described above accounts for the reversing of ON/OFF states as a function of τ_W, as observed in the $t_2 = 73$ nm junction, and strongly suggest that polarization reversal and ionic motion processes coexist and contribute to the *ER*. It thus follows that, if the BTO films are thinner (35 nm, as reported here), the prevalence of ionic motion will become perceptible for large τ_w, as its ER for shorter writing times (polarization dominated) is larger. The relatively larger ER of the $t_1 \approx 35$ nm) sample is more visible in the room temperature data (Figure 4.8a). Therefore, the corresponding τ_{CRIT} is also larger, as observed. Naturally, the reverse situation should occur for thicker BTO barriers (110 nm in the present case) and consistently, shorter τ_w is required to write distinct resistance states and the ionic contribution (ER < 0) prevails at any practical τ_w. The same picture accounts for the observed dependence of τ_w on temperature. Indeed, when cooling (warming) the junctions, the activated ionic motion is hampered (reinforced) and thus the electronic response (ER > 0) (ionic response ER < 0) prevails up the longest (shorter) writing time, as observed in Figure 4a.

4.6 Conclusions

Overall, the experimental results reported here indicate that the sign and magnitude of the ER on BTO capacitors of intermediate thickness (> 35 nm), clearly contain contributions reflecting different physical processes. Instrumental to this discovery has been the availability of experimental ER data at different temperatures (up to 450 K) which have provided clear indications of a thermally activated process contributing to govern the ER. We have observed that whereas at short writing times, a modest ($\approx 10^2$ %) positive ER is observed, its sign is reversed for longer writing times and its magnitude increases, reaching large *ER* values ($\approx 4.6\ 10^3$ %) which are comparable to those observed in tunnel BTO barriers. The presence of two time scales for the ER could be of relevance for the design and exploitation of ferroelectric-based RS devices. For instance, the observed ER(τ_W) response is reminiscence of second-order memristors[118] such those used to implement biorealistic synapses.[119] The results presented here, show that temperature-controlled ER provide, achievable exploiting self-heating mechanisms, offer a new toggle to tune the RS and the functionality of ferroelectric capacitors.[36]

4.7 Supporting Information

Supporting Information S4-1. Electroresistance of the same t_2 =70 nm BTO film as reported in the manuscript main body, but collected for another junction (J_2) showing a similar result change of sign of *ER* when increasing the writing time.

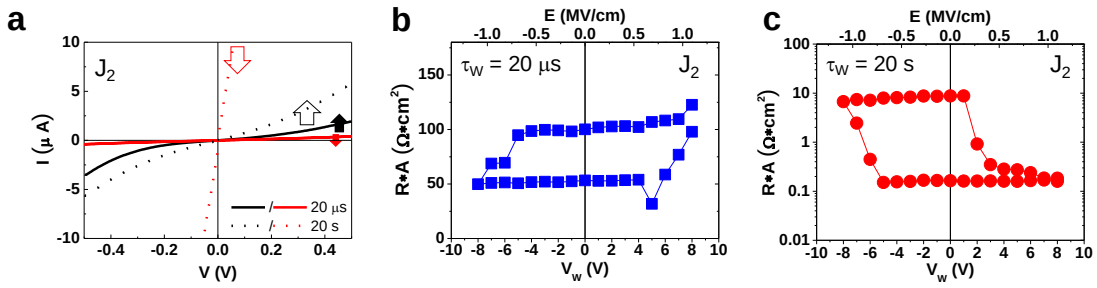


Figure S4-1. (a) *I-V* reading pulses recorded of J_2 junction of the t_2 = 70 nm BTO capacitor, after prepoling the junction (writing) with a V_w = -8 V/+8 V pulse of τ_w = 20 μs (black and red solid line), and τ_w = 20 s (black and red dot line). (b,c) *ER* loops collected using τ_w =20 μs and 20 s, respectively. All the data correspond to J_2 of the t_2 =70 nm BTO capacitor.

Supporting Information S4-2. Dependence of the resistances of the ON and OFF states of t_2 = 70 nm sample **(**equivalent to Figures 4.3a,b in chapter 4 main body), but measured in a different junction of the same sample and at different temperatures, showing similar results.

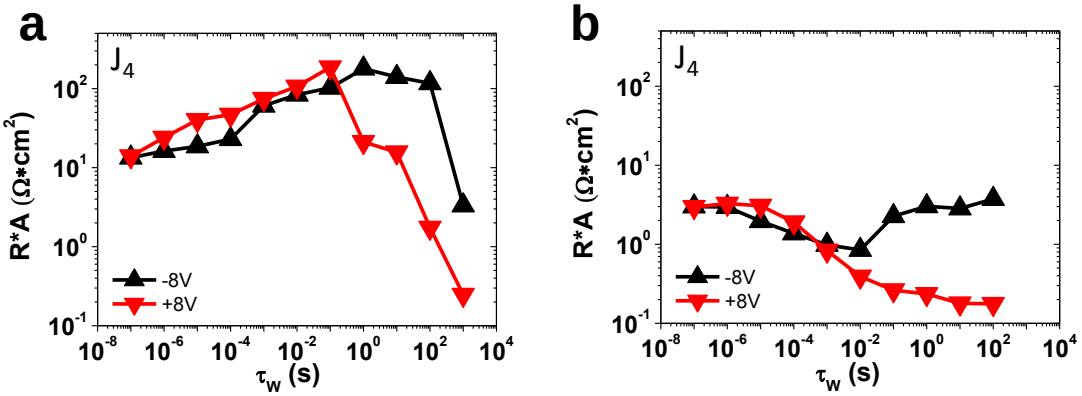


Figure S4-2. Resistance times area of the J_4 junction of the t_2 =70 nm BTO capacitor, after prepoling the junction (writing) with V_w = -8 V/+8 V pulse of τ_w for different length of the writing pulses, of junction J_4: (a) room temperature and (b) 400 K.

Supporting Information S4-3. Dependence of the *ER* on writing time τ_w for all the measured temperatures of J_3 junction of the t_2 = 70 nm sample.

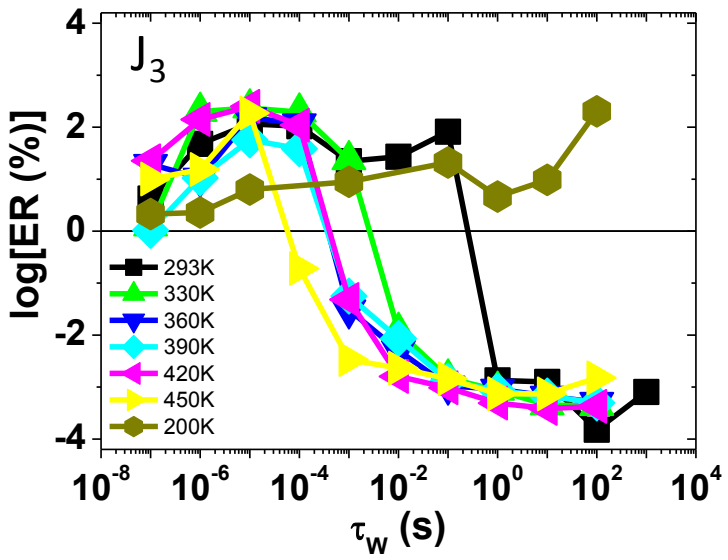


Figure S4-3. Dependence of the electroresistance of junction J_3 of the t_2 =70 nm BTO capacitor on the writing time at several temperatures, as indicated.

Supporting Information S4-4. Raw data of the ER dependence on τ_w for the samples of different thicknesses shown in Figure 4.7c.

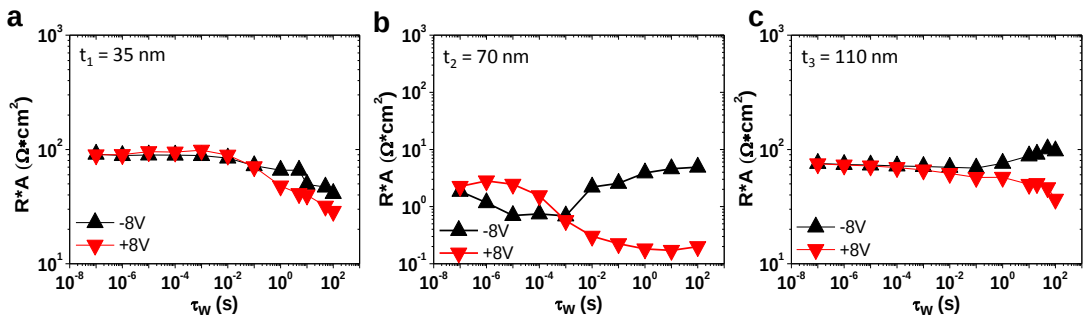


Figure S4-4. Resistance times area after prepoling the junction (writing) with V_w = -8 V/+8 V pulse of τ_w of BTO capacitors with different thicknesses: (a) t_1, (b) t_2 and (c) t_3 measured at 450 K. The resistance of the t_3 = 110 nm sample was measured at -1 V due to its lower conductivity.

Supporting Information S4-5. Extraction of tunnel barrier parameters from *I-V* characteristics of 4 nm BTO thin film capacitor for opposite prepoling voltage.

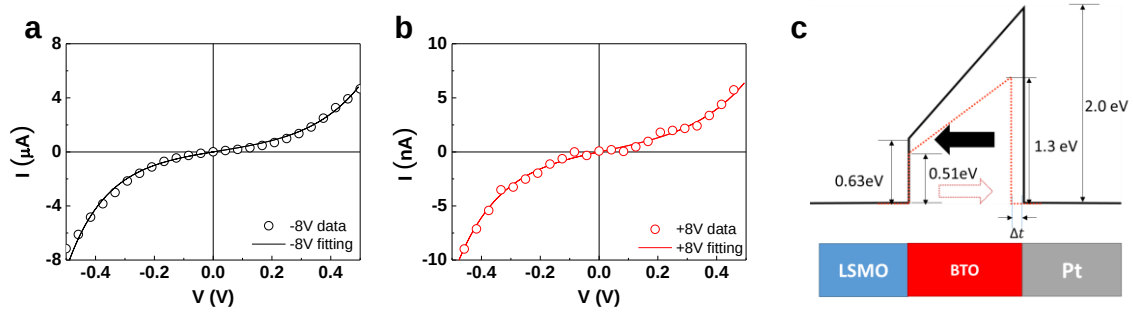


Figure S4-5: *I-V* characteristics measured at room-temperature on BTO junction of 4 nm, and electrode area of 250 μm^2 for: (a) ON and (b) OFF states, respectively. Solid lines across the experimental data are the results of the fits according to the Brinkman model for tunnel transport across trapezoidal potential barriers in the Wentzel–Kramers–Brillouin (WKB) approximation.[17,18] (c) Sketch of the resulting shape of the barrier in the BTO tunnel junction with the fitting results indicated in the sketch. Black line corresponds to +8 V prepoling, and red line to -8 V.

The fitting parameters are:

ON state: φ_1(ON) = 0.51 eV, φ_2(ON) = 1.30 eV and d(ON) = 2.1 nm,

OFF state: φ_1(OFF) = 0.63 eV, φ_2(OFF) = 2.0 eV and d(OFF) = 2.3 nm

The results indicate a substantial rising of the average barrier height and its asymmetry and barrier thickness in the OFF state. Note that both barrier heights φ_1 and φ_2 corresponding to LSMO/BTO and BTO/Pt interfaces, respectively, increase after +8 V, which corresponds to polarization pointing towards LSMO.

Supporting Information S4-6. Electroresistance characterization for samples of series II. In panels (a,b,c), we plot the *I-V* characteristics in the voltage range ±0.5 V after prepolarizing the sample with ±8 V using different writing times (short τ_w = 20 μs and long τ_w =20 s) for the t_1 = 35 nm, t_2 = 70 nm and t_3 = 110 nm BTO samples. The experiment is equivalent to that shown in Figure 4.1c. For the the t_1 = 35 nm sample shown in (a) ON (OFF) states are obtained for negative (positive) prepoling, and their difference increases with τ_w. For t_2 = 70 nm sample shown in (b), ON (OFF) states are obtained for negative (positive) prepoling for short writing time, but the opposite for long writing time. For t_3 = 110 nm sample shown in (c), OFF (ON) states are obtained for negative (positive) prepoling for short and long writing time, although for short writing time the difference is negligible. In panels (d,e,f), the *ER* measurement following the sequence of Figure 4.2a using different writing times (short τ_w = 20 μs and long τ_w = 20 s) is shown for the t_1 = 35 nm, t_2 = 70 nm and t_3 = 110 nm BTO samples. Here, it can be more clearly observed the different sign and magnitude depending on writing time and thickness for ER. For the t_1 = 35 nm sample shown in (d), positive ER is observed irrespective of the writing time, but increasing with it. For the t_2 = 70 nm sample shown in (e), positive ER is observed for short writing times, and negative (much larger) for long writing times. For the t_3 = 110 nm sample shown in (f), negative ER is observed for short and long writing times, and its absolute value increases with thickness. Overall, it can be observed that similar trends to those reported in the manuscript are observed for representative junctions in samples of serie II.

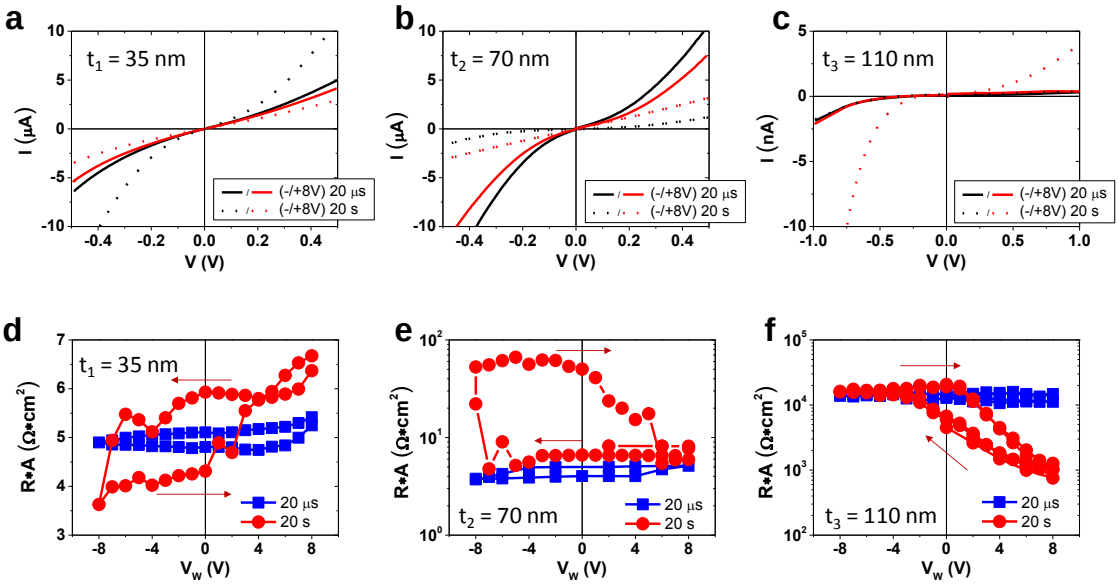


Figure S4-6. ER data of samples of series II. (a-c) *I-V* reading pulses recorded of t_1 = 35 nm, t_2 = 70 nm, t_3 = 110 nm after prepolarizing the junction (writing) with a V_w = -8 V/+8 V pulse of τ_w = 20 μs (black and red solid line), and τ_w = 20 s (black and red dot lines). Resistance times the area for different prepoling voltages of duration 20 μs and 20 s , measurement sequence following the +8 V to -8 V to +8 V path, for (d) t_1 = 35 nm, (e) t_2 = 70 nm and (f) t_3 = 110 nm.

Chapter 5 Complementary resistive switching using ferroelectric tunnel junctions

5.1 Abstract

Complementary resistive switching (CRS) devices are driving attention as a potential way to solve the current snake problem typical of memory arrays based on resistive switching elements. Here we show that a simple arrangement of ferroelectric tunnel junctions, based on $BaTiO_3$, with symmetric top metallic electrodes, allows effectively writing and reading binary states of identically large resistance state in the unbiased state. Moreover, we experimentally demonstrate that this arrangement has significant lower power consumption that single ferroelectric tunnel junctions to perform writing/reading functions.

5.2 Introduction

Dramatic changes of electric resistance are observed in some thin-film devices when stressed by electric signals, for instance electric current or voltage. This resulting resistive switching (RS) has been observed in large variety of materials and heterostructures and different mechanism are shown to be at play depending on the precise nature of materials and measuring conditions. The structure of the device is rather simple trilayer structure composed by a suitable thin film sandwiched in between two metallic electrodes. What is relevant here is that two non-volatile resistance states, low-resistance state (LRS) and high resistance state (HRS) can be obtained by suitable electric stimulus applied to the electrodes. These two states, can be view as ON and OFF states and used to store logic information ("0" and "1"). The non-volatile nature of the resistive switching processes and the fact that the information is stored in the resistance, implies that in principle, resistive switching devices can be scaled down as required by the most aggressive scaling in electronic industry. This is an important advantage compared

with electronic memory devices based on electric charge switching. In fact, the resistive random access memory (RRAM) elements are intensively investigated on the path towards higher memory density and enhanced computing performance as required by present and future information technologies. The so-called passive crossbar array of resistive switching devices (sometime also lousy named, memristive devices), constitutes the backbone of random access memories (RAMs) and of reconfigurable logics and holds promises to become central in the quest for fusion of logic and memory functions.

The crossbar array consists on an array of parallel bottom metallic electrodes and a perpendicular array of top metallic electrodes (word and bit lines) that sandwich at each crossing point, the resistive switching element. Applying suitable voltage at the specified word and bit lines the state of a RS element can be set to LRS (ON) or HRS (OFF). Inherent to this array configuration is that the bottom electrode connects all elements in a raw and the top electrode connects all elements in a column. It thus follows that: i) if several elements are in LRS state, when current is used to probe the state of a particular element, charge will leak across all LRS elements (*sneak current*) thus compromising the lecture and ii) the presence of LRS states implies a permanent current leakage and a concomitant Joule dissipation. These intrinsic bottlenecks of crossbar arrays are well recognized and several approaches, such as integration of strongly rectifying elements, have been proposed to overcome this drawback.[120] In 2010, Linn et al[121] proposed a simple solution to solve the sneak problem: connect two RS devices antiserial in such a way that if one is in LRS state the other is in the HRS state (so-called complementary resistive switching, CRS). In these circumstances, information is stored not in the state of a single RS element but in the state of the distinguishable coupled pair: LRS+HRS and HRS+LRS, representing logic states "0" and "1". Of relevance is that the resulting coupled state is always in a high resistance state at remanence and thus the sneak current and leakage could be reduced.

This novel approach to data storage has been successfully demonstrated using a variety of materials and resistive switching mechanisms. For instance, filamentary conductivity in Pt/SiO2/GeSe/Cu,[121] and all-oxides RRAMs,[122–128] where logic functions were also implemented. In general, in this approach the data reading is achieved by applying a voltage pulse large enough to switch one of the RS elements from HRS to LRS and reading the

subsequent current. This readout mechanism is destructive as it switches one of the memory elements and thus a rewriting pulse step is required to restore the information.

Ferroelectric tunnel junctions are receiving some attention to be used for RS. In ferroelectric tunnel junctions, electric field biasing allows switching the polarization state of the ferroelectric material thus giving rise to two distinguishable resistance states.[10–26] It has been reported that this mechanism (purely electronic) can coexist with ionic contributions.[48,55,92–95,129] . If ferroelectric memory elements are used in crossbar geometry the current sneak problem remains. To overcome this limitation, recently Xi et al.[83] have taken advantage of the strongly rectifying nature of the Schotkky barrier between a ferroelectric ($BaTiO_3$) and a semiconducting electrode (Nb:$SrTiO_3$) and its polarization dependence, to create a CRS. Using this approach, the authors successfully demonstrated a significant suppression of the sneak current and a non-destructive readout.

However, from a practical point of view, the observed gradual switching and the use of a semiconducting electrode such as Nb:STO is hardly integrable in technological processes and thus other approaches are required to create CRS. In addition, CRS devices based on ferroelectric tunnel junctions with Schottky barrier controlled responses show gradual HRS/LRS and LRS/HRS transitions. [83] Here we show that using simply two metallic electrodes: Pt and $LaSrMnO_3$, sandwiching a ferroelectric $BaTiO_3$ epitaxial layer to create a tunnel junction, a CRS device can be obtained. I-V characteristics of the here reported CRS device show sharp switching between LRS/HRS similar to Pt/SiO2/GeSe/Cu.[121]

5.3 Experimental

Ferroelectric $BaTiO_3$ (BTO) thin films (4 nm thick) where epitaxial grown on (001) (LaAlO3)0.3(Sr2TaAlO6)0.7(001) (LSAT) substrates buffered by a thin $La_{2/3}Sr_{1/3}MnO_3$ (LSMO) (20 nm) layer acting as metallic electrode. Films were grown by pulsed laser deposition (PLD) using the conditions discussed elsewhere.[7,100–102] Structural characterization is shown in Supp. Inform. Figure S5-1. Circular platinum (Pt) electrodes were deposited ex-situ by sputtering using suitable metallic masks to produce top contacts of lateral dimensions 20 μm and a thickness of about 20 nm.

Current-voltage (I-V) electric measurements were done in two configurations. In the first configuration a ferroelectric junction, named A, was tested by applying a bias voltage ($V^{+/-}$) on a top Pt electrode while grounding the bottom electrode (LSMO), as sketched in Figure 5.1(a) inset. In this configuration, so-called "top-bottom" (T-B), I-V curves were collected using a triangular V(t) signal following the path $-V_{max} \rightarrow +V_{max} \rightarrow -V_{max}$, where V_{max} is the absolute value of the maximum applied voltage]. In the second configuration, two top Pt electrodes where connected, one connected to $V^{+/-}$ and the other grounded, as sketched in Figure 5.1(b) inset. In this configuration, so-called "top-top" (T-T), I-V curves were collected using the same protocol than in the T-B configuration. In this configuration two junctions are connected in anti-series, via the common LSMO electrode, thus mimicking the proposed CRS arrangement. For the used writing/reading schemes, the writing and reading pulses are trapezoidal signals of $3 \cdot \tau$ duration, where τ is the duration of the rise, plateau, and decay of the trapezoidal signal. Trapezoidal voltage pulses are used to minimize the associated displacive current peaks. In the following experiments performed using different writing ($\tau_W = \tau$), reading times ($\tau_R = \tau$) will be reported. The time interval between writing and reading is denoted as the delay time (τ_D).

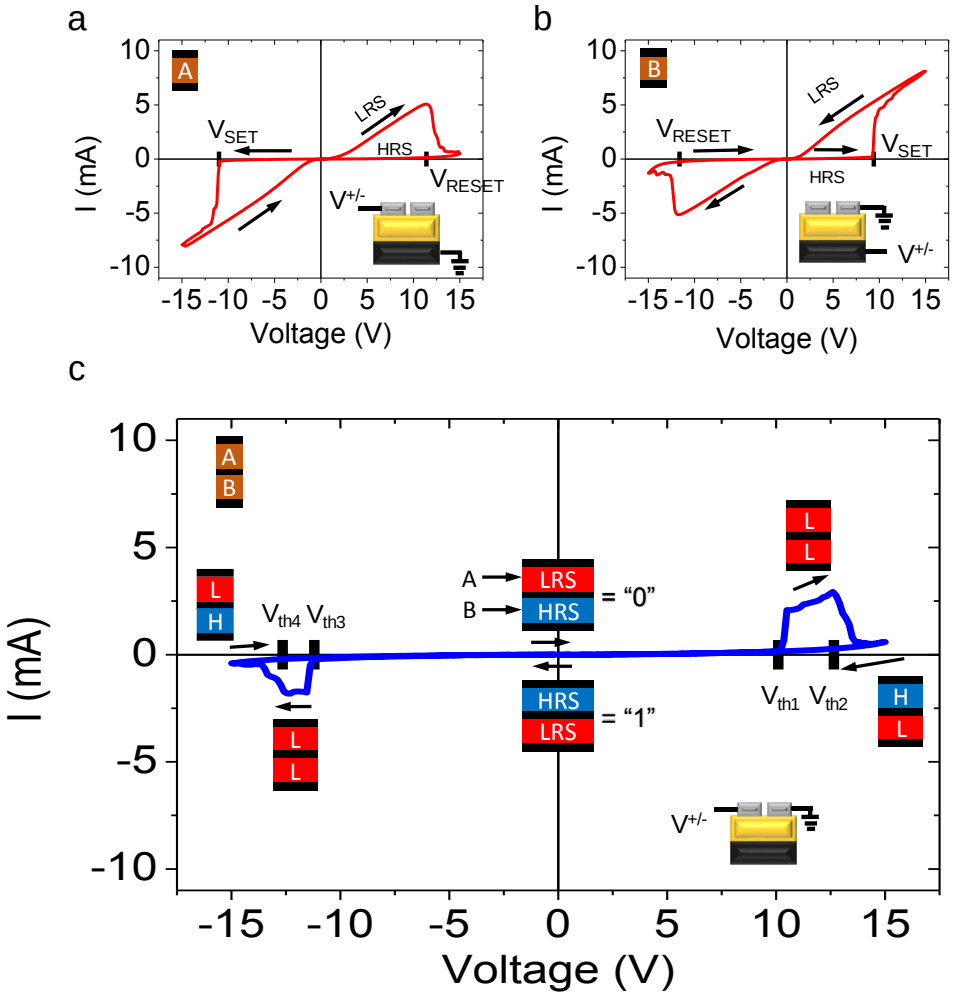


Figure 5.1*. (a) I-V curve of junction A recorded in top-bottom (T-B) contact configuration. (b) I-V of junction B recorded in reversed T-B configuration. (c) I-V curve of device AB recorded in top-top (T-T) contact configuration.*

5.4 Results

5.4.1 I-V characteristic of complementary resistive switching

In Figure 5.1(a), we show the I-V curve recorded for V_{max} = 15 V of junction A. It can be appreciated in Figure 5.1(a) that the I-V curve is clockwise in the V > 0 range and anticlockwise in the V < 0 range. In the V > 0 region, a switch from the low-resistance state (LRS) to the high resistance state (HRS) occurs at a threshold voltage, known as reset voltage (V_{RESET}). This switching process has been associated to the reversing the ferroelectric polarization P of the barrier from $P^{\uparrow}$ to $P^{\downarrow}$, where ↑ and ↓ indicate the pointing direction of the polarization (towards

Pt and LSMO respectively)[56,103,129]. In the V < 0 region, a switch from the HRS to the LRS occurs at V_{SET}, where $P^{\downarrow}$ switches to $P^{\uparrow}$. Due to the fact that in the T-T device to be described in the following, A and B junctions are connected anti-series, the V-bias polarization is of opposite sign in them. Consequently, in Figure 5.1(b) we show the I-V characteristics of a reversely biased B junction. Notice that due to the fact that this B junction is reversely V-biased, the V > 0 region is anticlockwise and the V < 0 region is clockwise. Consequently, in B junction, the HRS to LRS switch occurs at $V_{SET} > 0$ and the LRS to HRS occurs at $V_{RESET} < 0$.

To measure the electroresistance of a CRS device, the I-V curve across the AB device is measured using the T-T contact configuration. In Figure 5.1(c), we show the I-V curve measured biasing the top electrode of the A junction and grounding the top electrode of the B junction. One can appreciate the dramatically different shape of the I-V curves with two fundamental features, namely: (i) at remanence, that is at V = 0, the device is always in a high resistance state (HRS_{CRS}) and (ii) two well defined voltage are observed at V > 0, where the switch to a low resistance state (LRS_{CRS}) of the AB device is observed (V_{th1}) and the recovery of a HRS_{CRS} is obtained (V_{th2}). Similarly, at V < 0, a transition from the HRS_{CRS} to LRS_{CRS} states occurs at V_{th3} while the HRS_{CRS} is recovered at V_{th4}. Overall, the shape of the I-V curve shown in Figure 5.1(c) is identical to that observed the CRS devices exploiting either valence change or electrochemical metallization induced resistive switching responses[121,128,130,131]. Detailed data inspection (see Supp. Inform. Figure S5-2 where the I-V characteristics of the AB device is shown in logarithmic scale) shows that there is a small difference between the current measured while increasing and decreasing voltage near the 0 V regions. This current difference can potentially be used to perform read operation, although, it can not be considered as a genuine result of a CRS. We recorded similar I-V curves in other junction pairs (see Supp. Inform. Figure S5-3).

5.4.2 Writing protocol of the resistance states

To understand the features of the I-V curves in Figures 5.1(c), we argue as follows. Assume that in accordance with the I-V curves of A and B shown in Figures 5.1(a) and 1(b), after the V = -16 V poling, junction A at V = 0 is in a LRS and consequently B is in HRS (see Table 1).

Increasing V (> 0) in agreement with I-V curves of Figure 5.1(a) and 5.1(b), all voltage basically drops at B which is the HRS; at some voltage (V_{th1}) the B junction will switch to the LRS whereas A remains at LRS, thus the current flowing in the system will abruptly increase (this is marked in red in the table). Note that the HRS to LRS switch occurs only if $|V_{SET}|$ is smaller than $|V_{RESET}|$. When reaching the V_{th2} threshold, A will switch to the HRS and the current will drop as seen in Figure 5.1(c). This state: A (HRS) and B (LRS) [HRS_A-LRS_B] is denoted "**1**" in Table 1. When V is reduced back to V=0, the HRS_A-LRS_B state is preserved. Indeed, even reversing the voltage polarity, as far as $V > V_{th3}$, the state of the device will be preserved. At $V = V_{th3}$, according to Figure 5.1(a), A will switch to LRS and the current across the device will increase abruptly as A and B will be both at LRS (this is marked in red in the table). At $V < V_{th4}$, B will be switched to the HRS and thus the flowing current will be reduced again. This state: A(LRS) and B(HRS) [LRS_A-HRS_B] is denoted "**0**" in Table 1. When V is reduced back to V=0, the LRS_A-HRS_B state is preserved. The key point of our work is that at remanence (V = 0), two different states (LRS_A-HRS_B and HRS_A-LRS_B) can be written having a similarly HRS_{CRS} but being physically different, as emphasized in Table 1.

Table 1. Voltage dependence of the resistance state of the junctions A and B, and their connection in anti-series (indicated as A-B). HRS, LRS refer to the resistance states of each single element (A,B). HRS_{CRS} and LRS_{CRS} refer to the resistance state of the A-B combination and ("0" or "1") to their logic state.

V	0	$V<V_{th1}$	$V_{th1}>V>V_{th2}$	$V>V_{th2}$	0	$V>V_{th3}$	$V_{th3}<V<V_{th4}$	$V>V_{th4}$	0
A B	LRS HRS	LRS HRS	LRS **LRS**	**HRS** LRS	HRS LRS	HRS LRS	**LRS** LRS	LRS **HRS**	LRS HRS
A-B	HRS_{CRS}	HRS_{CRS}	LRS_{CRS}	HRS_{CRS}	HRS_{CRS}	HRS_{CRS}	**L**RS_{CRS}	HRS_{CRS}	HRS_{CRS}
State	**0**				**1**				**0**

5.4.3 Reading protocol of the resistance states

Having stablished that different states can be written, we turn now to the reading protocols applied after the LRS_A-HRS_B state is settled. In the following the width of the writing and

reading pulses is $\tau_W = \tau_R = 1$ ms and the time delay between writing and reading pulses is of $\tau_D = 1$ s.

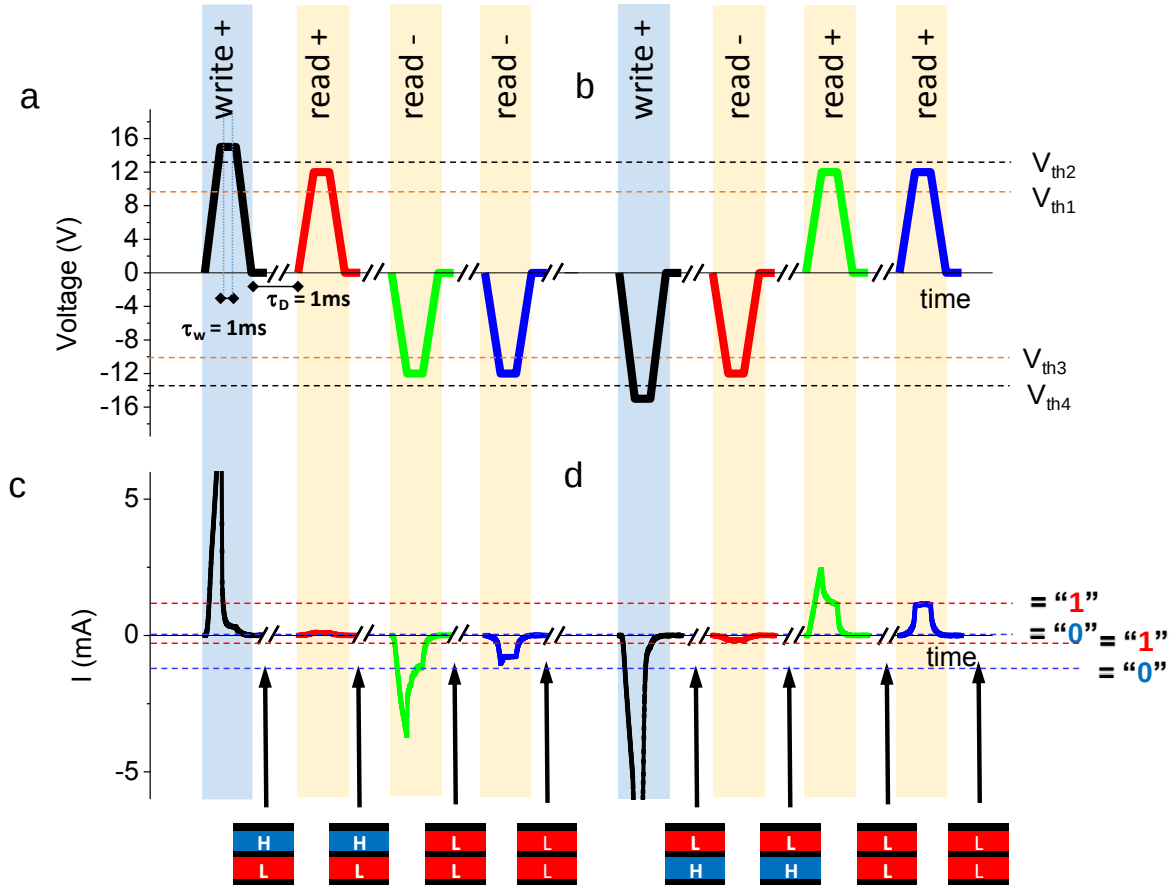


Figure 5.2 *(a) Voltage pulse train used to write and read HRS_A-LRS_B (which corresponds to "0"). (b) Voltage pulse train used to write and read LRS_A-HRS_B (which corresponds to "1"). (c,d) Measured current during application of voltage pulse train shown in (a,b). Background colors indicate if a writing (blue) or reading (yellow) pulse is applied. Top labels also indicate if the write and reading pulses are positive (+) or negative (-). Bottom sketches indicate the resistance states (H ≡ HRS, L ≡ LRS) of the two anti-series connected capacitors.*

a "0" and "1" states. **(c)** the corresponding current pulses. We used $\tau_W = 1$ s and $\tau_R = 1$ s and the time delay $\tau_D = 1$ s as indicated.

In Figure 5.2(a,b), we shown the voltage pulses used to write the LRS_A-HRS_B and HRS_A-LRS_B states (black). In Figure 5.2(c), we show the corresponding measured current pulses. According to Figure 5.1(c) and Table 1, to write HRS_A-LRS_B (which corresponds to "0") a $V > V_{th2}$ is

required. We used V_w = +16 V [Figure 5.2(a)]. In Figure 5.2(b), one can appreciate (black pulse) that a large current spike (> 5 mA) occurs reflecting that during the 0 to 16 V voltage writing excursion a transitory LRS_A-LRS_B state has been settled before reaching HRS_A-LRS_B . To read the state, a V_R = 12 V ($V_{th1} < V_R < V_{th2}$) pulse (red) is applied. As shown in Figure 5.2(b), a small current pulse (≈ 100 μA) (red) is measured indicating HRS_{CRS}. To discriminate between LRS_A-HRS_B and HRS_A-LRS_B we simply compare the output signals (red and green current pulses in Figure 5.2c) obtained using $V_R >$ (red pulse) and $V_R < 0$ (green pulse) (Figure 5.2b). It is obvious that the measured current is much larger (≈ 2 mA) when using $V_R < 0$ than for $V_R < 0$ thus indicating that memory state has been changed to a LRS_{CRS}. As in $V_R < V_{th3} < 0$ a LRS_A-LRS_B is stablished, this implies that the initial state was HRS_A-LRS_B. Therefore, the reading is completed.

Writing and reading the LRS_A-HRS_B (which corresponds to "1") is done similarly. According to Figure 5.1(c) and Table 1, to write LRS_A-HRS_B a $V < V_{th4}$ is required. We used V_w = -16 V (Figure 5.2(b) (black pulse)). In Figure 5.2(d), where the measured current is plotted, one can appreciate (black pulse) that a large negative current spike (< -5 mA) occurs during the writing process reflecting that during the 0 to -16 V voltage writing excursion a transitory LRS_A-LRS_B state has been settled before reaching LRS_A-HRS_B . To read the state, a V_R = -12 V ($V_{th4} < V_R < V_{th3}$) pulse (red) is applied. As shown in Figure 5.2c, a small current pulse (≈ 100 μA) (red) is measured indicating HRS_{CRS}. To discriminate between LRS_A-HRS_B and HRS_A-LRS_B we simply compare the output signals [red and green current pulses in Figure 5.2(d)] obtained using $V_R < 0$ (red pulse) and $V_R > 0$ (green pulse) [Figure 5.2(b)]. It is obvious that the measured current is much larger when using $V_R > 0$ than for $V_R < 0$ thus indicating that memory state has been changed to a LRS_{CRS} for $V_R > 0$. As in $V_{th1} > V_R > V_{th2}$ a LRS_A-LRS_B is stablished, this implies that the initial state was LRS_A-HRS_B. Therefore, the reading is completed. In Supp. Inform. Figure S5-4, we show the I-V characteristics for a whole set (HRS_A-HRS_B, LRS_A-HRS_B, HRS_A-LRS_B, and LRS_A-LRS_B) of states, which helps to visualize how the reading process is achieved.

In Figures 5.2(a,b,c,d), we also include the results of a repeated reading process, after a positive V_W writing step, with $V_R < 0$ (color). Naturally the output current data (blue) is very similar to the first reading process (green) with the only exception that a current spike was observed in

the first but not in the second [Figures 5.2(c,d)]. The absence of the spike, also confirm that during the first reading process a reversal of the state of one of the junctions had occurred but it does not occur any longer during subsequent reading steps. Application of subsequent $+V_w$ pulses does not change the written HRS_A-LRS_B state and thus no spike occurs, opposite to the result observed if $-V_w$ pulses are applied (see Supp. Inform. Figure S5-5).

5.4.4 Stability of CRS states

We turn now to the stability different states and duration of the writing pulse required to set a precise state, respectively. With this purpose we explore the role of τ_D and τ_w on the corresponding output signals. We proceed as follows. First, we set a well-defined initial state preparing the device in a the HRS_A-LRS_B state obtained applying a large ($V = +16\ V > V_{th2}$) and long (100 ms) prepoling positive pulse. Positive or negative voltages ($V_W = \pm 16V$) has been used to set the different HRS_A-LRS_B and LRS_A-HRS_B states, respectively. Two reading V_R pulses of 12 V have been applied (see the pulse voltage train in Supp. Inform. Figure S5-6). The current measured during the second V_R is plotted in Figures 5.3. We used the second V_R to avoid the presence of current spikes allowing better comparison. The current measured during the first V_R is in Supp. Inform. Figure S5-7). In Figure 5.3(a), we show the measured current after delay times of τ_D = 1 s, 1 min and 1 h between the V_W and V_R keeping constant the τ_W = 1ms. It can be observed that irrespective of the value of τ_D, the two states (blue and red for HRS_A-LRS_B and LRS_A-HRS_B respectively) are well defined and the measured current does not significantly vary with τ_D. Thus, we can conclude that within the explored time scale, both states are non-volatile. In Figures 5.3(b), we show the current measured during the reading pulse, after writing pulses (blue for positive and red for negative) of duration τ_w = 0.1, 1, 5 and 100 ms keeping constant the τ_D = 1 s. As in Figure 5.3(a), to avoid spikes, we include only the data collected after a repeated reading pulse. See in Suppl. Inform. Figure S5-8, data on first reading pulse. It can be appreciated that conductance contrast between the two different states starts to increase at ≈1 ms and keep increasing up to about 10 ms, where the contrasts gradually saturates (Supp. Inform. Figure S5-8). Therefore, it follows that relatively slow pulses (about 1 ms) are needed to write the information. This time scale is several orders of magnitude longer than the switching time of a ferroelectric film thus suggesting that other effects are limiting the observed time-response. A hint into the physical origin can be obtained

by considering the time constant ($\tau = RC$) our measuring circuit. Using $HRS_{CRS} \approx 1M\Omega$ (measured at 12 V) and a measured capacitance of ≈ 3pF (100 kHz), it turns out that $\tau \approx 1$ ms, which is in good agreement with the experimental observation.

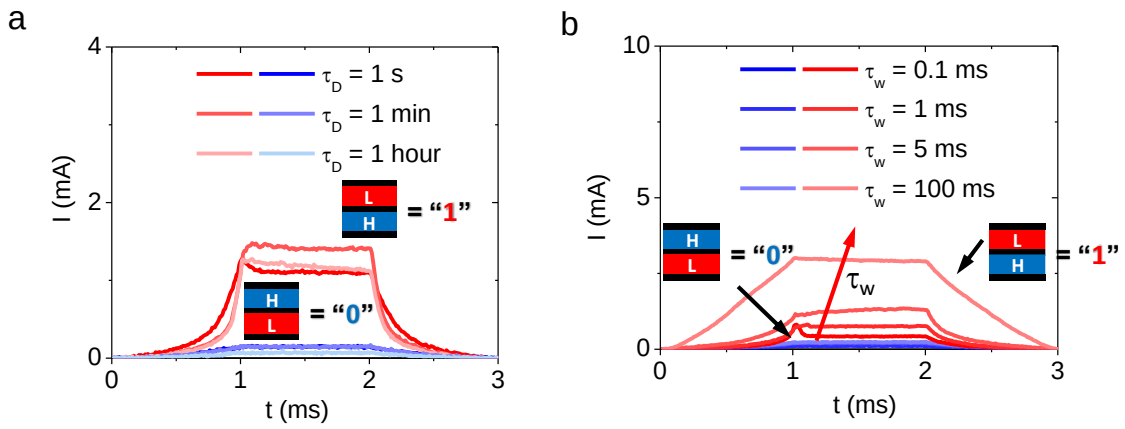


Figure 5.3 *(a) Current during the second reading pulse measured using different delay times (τ_D = 1 s, 1 min and 1 h) after the writing pulse of +16 V (blue) or -16 V (red) of τ_W = 1 ms of duration. (b) Current during the second reading pulse measured after the writing pulse of +16 V (blue) or -16 V (red) of τ_W = 0.1, 1 , 5 and 100 ms of duration fixing the t delay times to τ_D = 1 s*

5.4.5 Writing/reading power consumption using the T-T and T-B configurations

Finally, we analyze the power dissipated in the T-T, equivalent to a CRS device, using the writing/reading scheme described. With this aim, we have applied a long write/read pulse of amplitude $V_W = \pm 16$ and $V_R = 12$ V, as indicated in Figure 4 (see in Supp. Inform Figure S9 the writing and reading pulses). In Figure 4(a), we show the write/read power ($P=I \cdot V$) consumption for the defined pulse train. It is evident that the maximum power is dissipated during the writing pulses. If the power is time-integrated for the defined pulse train it turns out that the dissipated energy is ≈ 120 μJ. The significance of this energy consumption can better appreciated if compared to the energy dissipated to perform a similar writing/reading process, when using the T-B configuration. In T-B configuration, which is in fact the measurement of a single ferroelectric junction, we used $V_W = \pm 15$ and $V_R = 0.1$ V. In Figure 5.4(b) we show the corresponding power for the defined pulse train. In this T-B configuration, the power dissipated during the writing is also much larger than during reading. It can also be noticed that for positive writing pulses the dissipated power is much larger than for negative due to the intrinsic junction asymmetry. While comparing the power used in writing/reading operations

in T-T and T-B (Figure 5.4(a) and Figure 5.4(b), it can be observed that the power consumed in T-B configuration is about one order of magnitude larger than in T-T and the corresponding energy (power integrated though the writing and reading pulses) is about near ≈800 μJ in T-B, which is about 7 times larger than the dissipated energy for the T-T configuration, showing the larger efficiency of the latter.

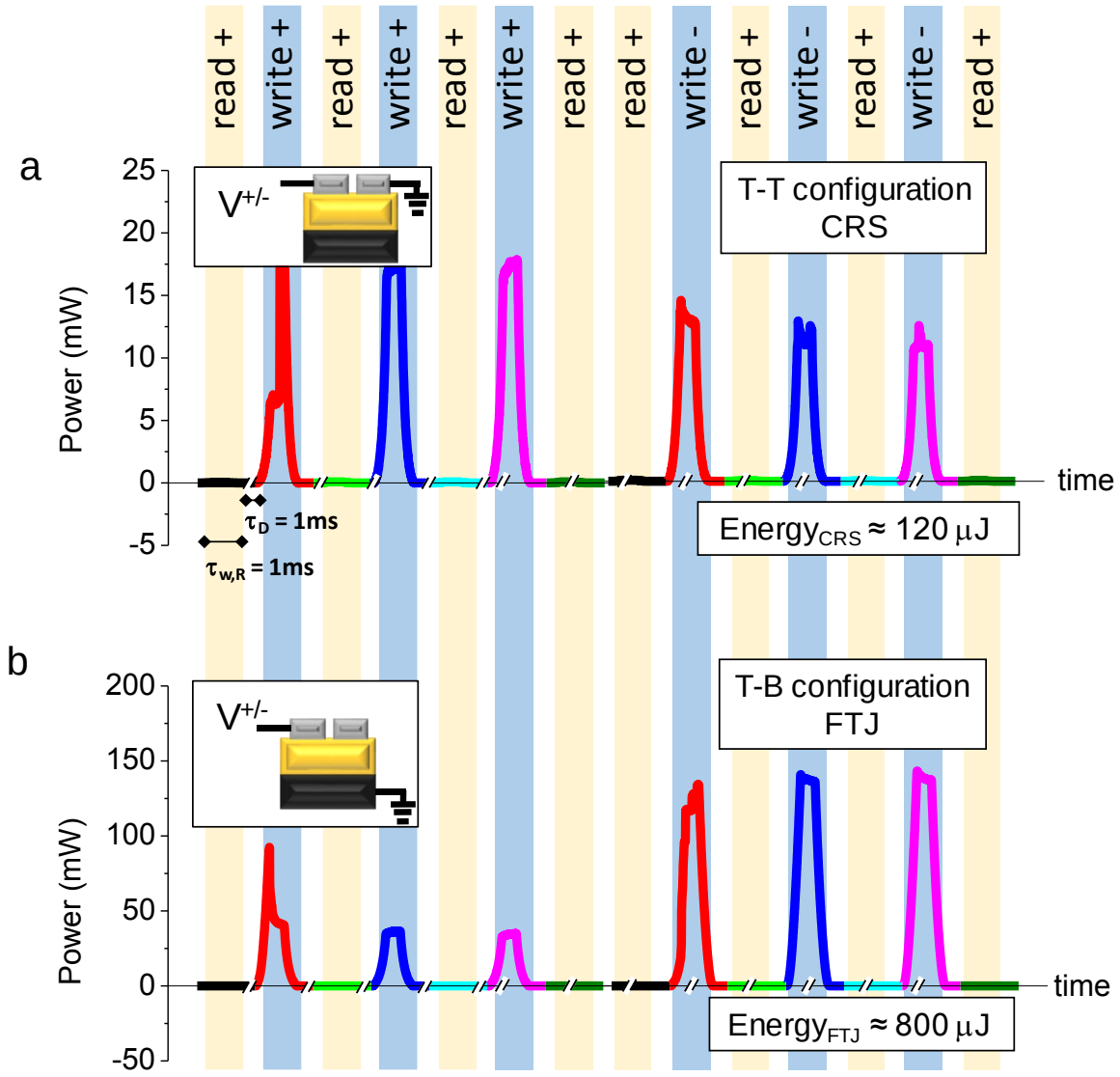


Figure 5.4*. (a) Writing/reading power consumption using the T-T configuration (sketched in the inset). Writing voltage is ± 16 V and reading voltage is +12 V. Background colors indicate if a writing (blue) or reading (yellow) pulse is applied. Top labels also indicated if the write/reading pulses are positive*

(+) or negative (-).(b) Writing/reading power consumption using the T-B configuration (sketched in the inset). Writing voltage is ±15 V and reading voltage is +0.1 V.

5.5 Conclusions

The results presented show that using $BaTiO_3$ ferroelectric barriers and metallic electrodes, the two different resistive states, HRS and LRS can be used as building blocks for a complementary resistive switch (CRS). In the reported approach the CRS is fabricated by simply using two top metallic contacts on a ferroelectric layer grown on a suitable metallic electrode (bottom), which is a definitely simpler structure than the complex metal-oxide/metal layers required in some earlier designs of CRS.[121] Here we have used antiserial connection of two $BaTiO_3$ tunnel barriers allows to obtain I-V characteristics analogous to those reported using Pt/SiO2/GeSe/Cu-/GeSe/SiO2/Pt.[121] We have shown that according to the expected properties of a CRS device, two logic sates "1" and "0", corresponding to the HRS-LRS and LRS-HRS of the used elements, can be written. The information is stored in a high resistance state, thus avoiding current sneak related problem. We have also shown that the writing/reading energy consumption is significant lower (about a factor 1/7) that that required to perform the same tasks in a single ferroelectric tunnel barrier. A drawback is that in the configuration used here the writing pulses are substantially long (>1 ms). However, as it appears that this limit is imposed by the time constant of the measuring circuit rather than by the intrinsic switching speed of the ferroelectric barrier, appropriate device engineering may allow overcome this limit. Therefore, our simple Pt/BTO/LSMO-BTO/Pt structure appears to be of potential use in resistive crossbar memory arrays.

5.6 Supporting Information

Figure S5-1. θ-2θ scans around BTO(002) reflection. Small bumps around the BTO peak are ascribed to Laue oscillations. Data simulation for a perfect BTO layer using c = 4.268 Å and thickness of 12.5 unit cells (corresponding to 5.3nm near its nominal value) is also shown. The simulation is in agreement with the bumps observed surrounding the BTO peak.

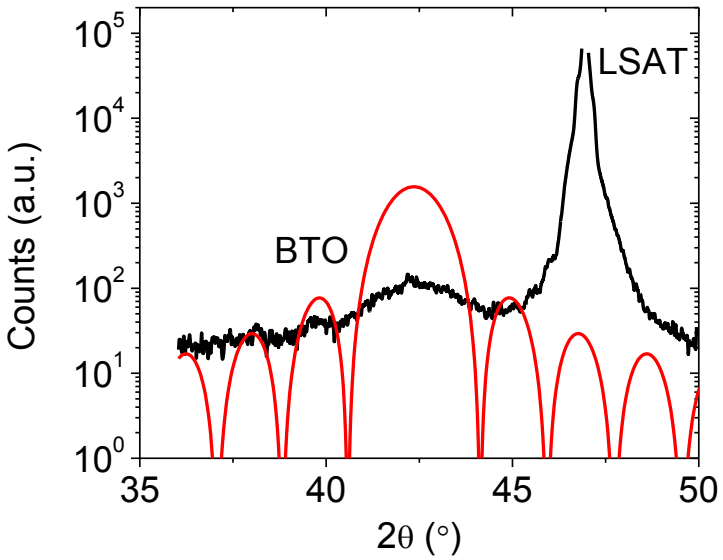


Figure S5-2 I-V curve in logarithmic scale of the devices measured in T-T contact configuration of the AB device shown in Figure 5.1(c).

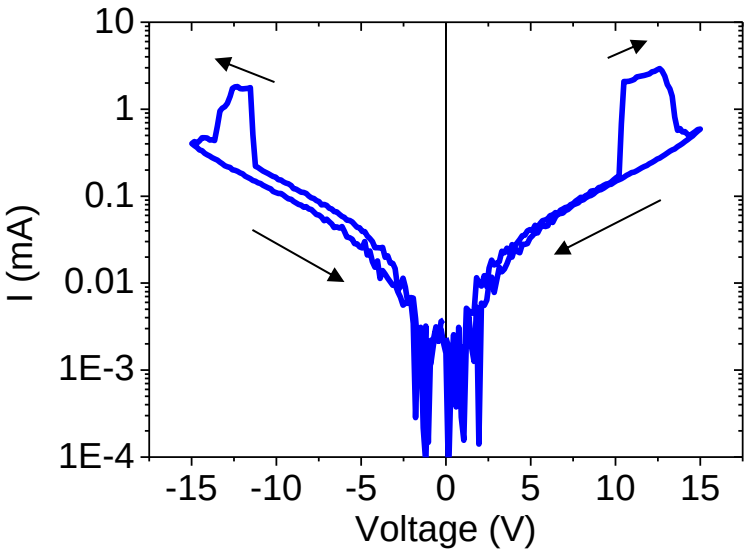


Figure S5-3. I-V curve of several devices measured in T-T contact configuration across the sample.

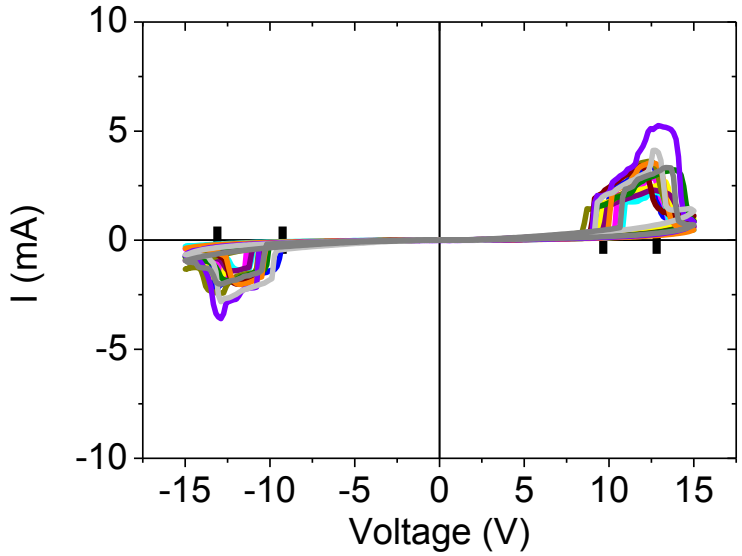


Figure S5-4. I-V curve measured in T-T contact configuration after preparing the indicated different initial states. In these experiments the different states has been prepared separately in junction A and B (according to the figure 5.1 notation) using writing pulses of ±15 V. The

voltage excursion used starts at 0 and after voltage is increased or decreased as indicated by the arrow. It can be observed that depending on the different initial state the recorded I-V is different.

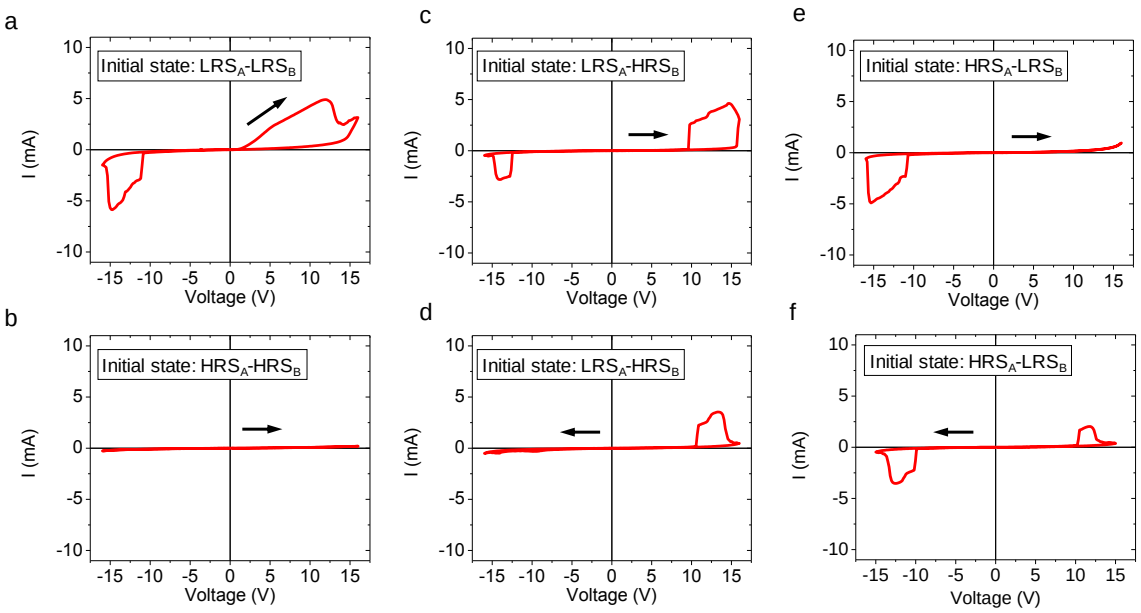


Figure S5-5. (a) Repetitive write/read voltage pulse train using writing voltages of +16 V and reading voltages of +12 V. (b) Repetitive write/read voltage pulse train using writing voltages of -16 V and reading voltages of +12 V. (c,d) Measured current during the application of voltage pulse train shown in (a) and (b), respectively. It can be observed that repetitive writing produces similar measured current during the reading.

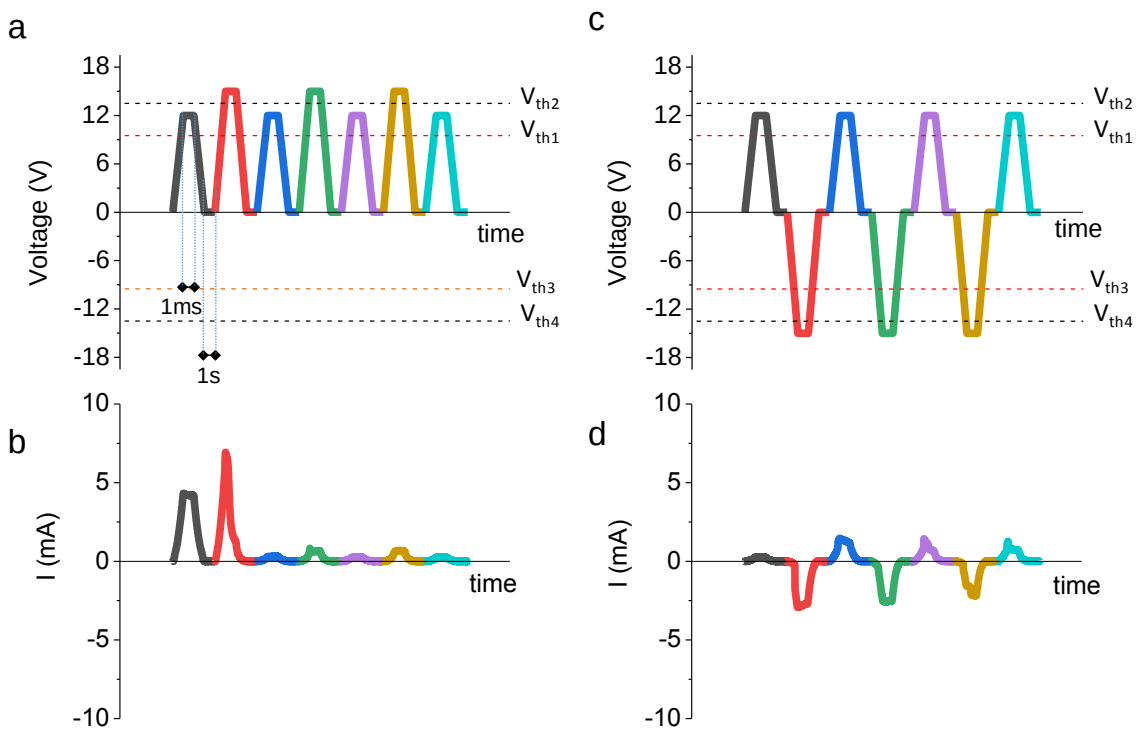


Figure S5-6. Used write/read voltage pulse train for the experiment shown in Figure 5.3.

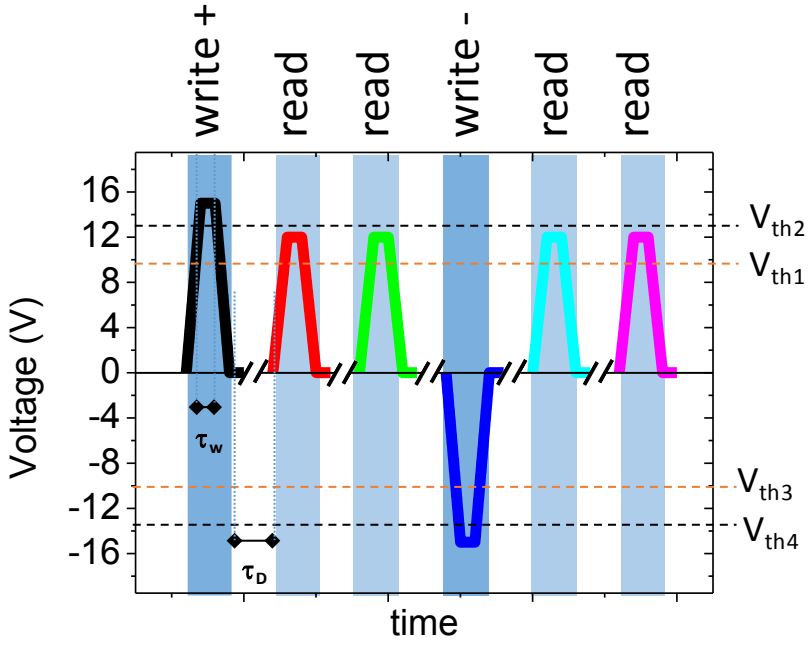


Figure S5-7. Measured current during the first (solid lines) and the second (dashed lines) reading pulses measured using different delay times (τ_D = (a)1 s, (b)1 min and (c)1 h) after the writing pulse of +16 V (blue) or -16 V (red) of τ_W = 1 ms of duration. The voltage pulse train used is that shown in Supp. Inform. Figure 5.6. It can be observed that during first reading pulse a current spike (not apparent in the second appears).

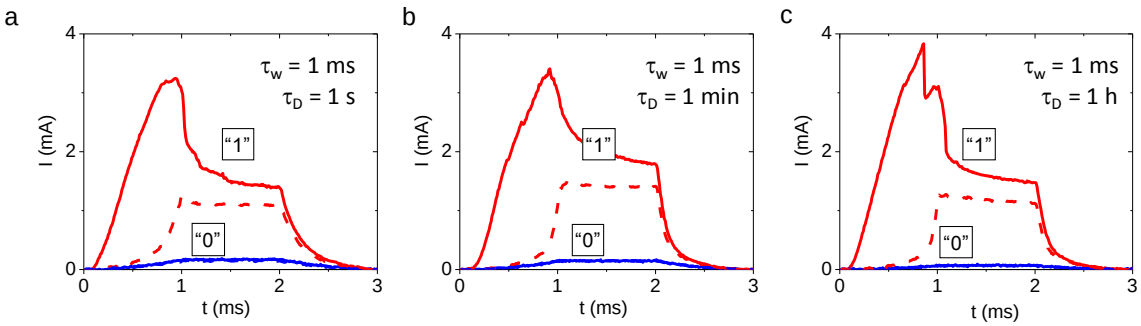


Figure S5-8. Current measured during the first (solid lines) and second (dashed lines) reading pulses measured after the writing pulse of +16 V (blue) or -16 V (red) of τ_W = (a)0.1, (b)0.5, (c)1, (d)10 and (e)100 ms of duration fixing the t delay times to τ_D = 1 s. It can be observed that measured current during the second pulse for τ_w of 10 and 100 ms is very similar indicating that the contrast between the two states is saturated. It can be observed that during first reading pulse a current spike (not apparent in the second appears).

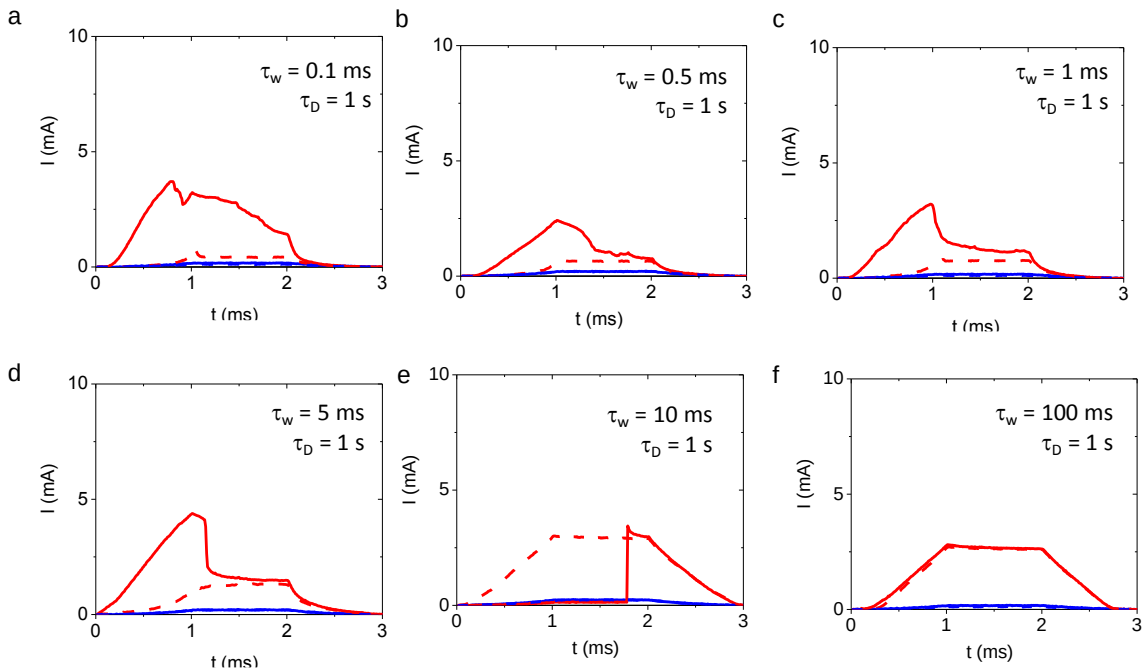
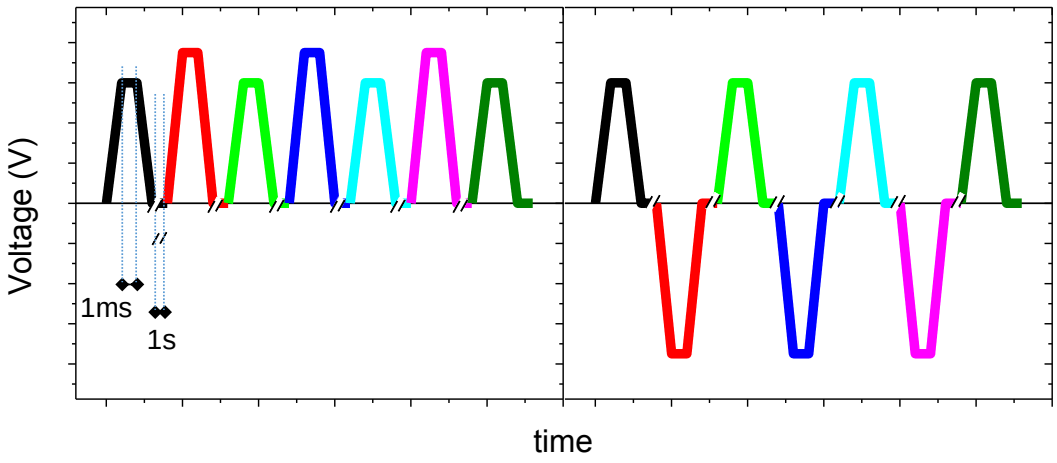


Figure S5-9. Used write/read voltage pulse train for the experiment shown in Figure 5.4.



Chapter 6 Conclusions

In this work, it is reported the investigations on the change electrical resistance under electric field of ferroelectric capacitors based on $BaTiO_3$, in view of their possible use as memristive device in non-volatile memory and logic applications.

Ferroelectric nanometric junctions of epitaxial $BaTiO_3$ thin films grown on suitable crystalline substrates and using appropriate bottom metallic electrodes ($La_{2/3}Sr_{1/3}MnO_3$) and top electrodes (Platinum) were characterized. We have observed and analyzed the polarization switching process and its impact on the electroresistance (ER), on the basis of the I-V data of nanometric (< 5nm) tunnel junctions. First, I-V curves were analyzed showing that, at low bias, they can be used to extract the parameters of the tunnel barrier and its variation upon polarization reversal. These devices display ER values (calculated as the relative increase of the resistance) as large as 10^4% at room temperature. When increasing the voltage excursion, a field-induced switching between a high-resistive state (HRS) and a low-resistive state (LRS) (and vice versa) is observed in the I-V characteristics. It is found that the switching process is largely asymmetric being smooth from LRS-to-HRS but proceed via avalanches in the HRS-to-LRS transitions. Combining measurements of the ferroelectric polarization switching process with investigations of the transport properties, a link between the ferroelectric domain and the conduction mechanism has been found. We argue that the asymmetric resistive switching dynamics observed in BTO tunnel devices finds it origin in the presence of an electric imprint field that controls the polarization reversal.

Next, we analyzed the ER of ferroelectric capacitors, in which the ferroelectric barrier is thick enough to cancel any direct tunneling (> 10 nm). We report on the observation that BTO-based capacitors can also display a large ER at room temperature: we discovered a remarkable sign-change of the ER (> 0, or < 0) depending on the barrier thickness and writing pulse duration and temperature. By using pioneering measurement of ER as a function of temperature, we have obtained evidence of the presence of a thermally activated process contribution to the ER,

additional to the pure electronic changes associated to ferroelectric polarization switching. Detailed analysis allows infer that the thermally activated process can be attributed to field-assisted ionic motion. We concluded that the relative balance between purely electronic and ionic diffusion processes, modulate the height of the interfacial Schottky barriers and consequently, are responsible of the observed variations of the magnitude and sign of ER.

Finally, we demonstrated that a simple arrangement of two top-top contacts (Pt) on a BTO film shunted by a common metallic electrode ($La_{2/3}Sr_{1/3}MnO_3$) allows a practical realization of a complementary resistive switching (CRS) device. In this realization, two ferroelectric tunnel junctions are connected antiserial and allow building a device which is able to store, in a high resistance state at remanence, logic information ("1", "0") in distinguishable HLR-LRS and LRS-HRS states. This device can solve the sneak problem in crossbar arrays of resistive switching data storage units. We have shown that writing/reading processes using our CRS have also significant advantages in terms power consumption if compared to single FTJs memory elements although, at this stage, suffering slow time response.

Chapter 7 Outlook

Although the basic principles of the resistive switching mechanism and the ferroelectric domain dynamics in ferroelectric tunnel junctions are understood, systems with ultrathin ferroelectric layers still provide a playground for research, just as in view of potential applications. In the case of ferroelectric tunnel junctions with different electrodes further investigations might be necessary to elucidate the mechanisms behind the interface defect formation to achieve for instance, symmetric switching behavior. Ferroelectric materials for tunnel barriers, having larger electroresistance ratios and lower leakage and allowing larger endurance and capable of sustaining intermediate resistance (logic) values should be developed for some particular applications.

In this direction, the fabrication of tunnel junctions with a $BaTiO_3/SrTiO_3$ composite barrier structure, allowing a more precise control of device asymmetry, may be interesting. Indeed, the preliminary tests have performed on junctions containing an additional $SrTiO_3$ barrier provides suggest that this could be an interesting approach.

A future and probably unavoidable step is to develop fully patterned arrays of ferroelectric tunnel junctions using suitable lithographic techniques (optical or electron beam).

In connection with the complementary resistive switching device, described in the last chapter of this PhD, it would be great to explore the response of arrays (even if limited in size) of complementary resistive switching patterned devices, with emphasis put in two directions: i) reduce amplitude of the writing voltages and ii) explore non-destructive readout schemes.

Last but not least, the experience accumulated in this PhD on the resistive switching of ferroelectric capacitors can be instrumental to the study of other ferroelectric materials. More precisely, the recent discovery of ferroelectric response in HfO_2, including epitaxial films as developed at ICMAB by Dr. F. Sánchez, could be an objective in the short term.

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List of figures

Abbreviations

BTO	$BaTiO_3$
STO	$SrTiO_3$
LSMO	$La_{2/3}Sr_{1/3}MnO_3$
LSAT	$(LaAlO_3)_{0.3}(SrAl_{0.5}Ta_{0.5}O_3)_{0.7}$
FTJ	Ferroelectric tunneling junction
RS	Resistive switching
CRS	Complementary resistive switching