ANALYTICAL MODELING OF ULTRASHORT-CHANNEL MOS TRANSISTORS

Kerim Yilmaz

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Analytical Modeling of Ultrashort-Channel MOS Transistors

KERIM YILMAZ

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DOCTORAL THESIS

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Kerim Yılmaz, M. Sc.

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to my lovely mother,

Gülşen Yılmaz

&

to the loving memory

of my dear father,

Ali Yılmaz

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List of Symbols

Latin Alphabet

Symbol	Description	Unit
A	channel cross-sectional area	[nm^2]
C_{ox}	gate oxide capacitor	[F]
C'_{ox}	cylindrical gate oxide capacitor per gate length	[F nm^{-1}]
C_{s}	capacitor represents coupling of source terminal to the top of the energy barrier E_{m}	[F]
C_{d}	capacitor represents coupling of drain terminal to the top of the energy barrier E_{m}	[F]
D_{ch}	channel electric displacement field	[As/cm^2]
D_{ox}	oxide electric displacement field	[As/cm^2]
E	electric field	[V cm^{-1}]
E_{avg}	average electron energy contributing to tunneling	[eV]
E_{bg}	bandgap energy	[eV]
E_{CB}	conduction band energy	[eV]
E_{eq}	equivalent energy barrier height	[eV]
$E_{\mathrm{f,d}}$	Fermi energy in the drain region	[eV]
$E_{\mathrm{f,s}}$	Fermi energy in the source region	[eV]
E_{m}	energy barrier height	[eV]
E_{x}	electron energy in x-direction	[eV]
$E_{\mathrm{x,max}}$	electron energy in x-direction with maximum contribution to tunneling	[eV]
E_{ρ}	transverse electron energy	[eV]
f_{d}	Fermi-Dirac distribution at the drain/channel interface	[−]

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f_s	Fermi-Dirac distribution at the source/channel interface	[−]
g_ds	channel conductance	[A V^{-1}]
g_m	transconductance	[A V^{-1}]
$\hbar$	reduced Planck constant	[eV s]
h	Planck constant	[eV s]
high-κ	material with high relative permittivity	[−]
H_NW	height of Ω-gate NW FET	[nm]
I_dd	drift-diffusion current	[A]
I_ds	total drain-to-source current	[A]
I_OFF	current in OFF-state	[A]
I_ON	current in ON-state	[A]
I_t	tunneling current	[A]
I_te	thermionic emission current	[A]
J_C	tunneling current per unit area along the channel center	[A/cm^2]
J_N	normalized tunneling current per unit area	[−]
J_S	tunneling current per unit area along the channel surface	[A/cm^2]
J_t	tunneling current per unit area	[A/cm^2]
J_te	thermionic emission current per unit area	[A/cm^2]
J_ds	total drain-to-source current per unit area	[A/cm^2]
k_fit	fitting parameter to adjust the equivalent wavenumber	[−]
k	wavenumber	[nm^{-1}]
K	square of the wavenumber	[nm^{-2}]
k_eq	eqivalent wavenumber	[nm^{-1}]
K_eq	square of the equivalent wavenumber	[nm^{-2}]
k_B	Boltzmann's constant	[eV K^{-1}]
L_ch	channel length	[nm]
L_DG	channel length of DG FET	[nm]
L_g	gate length	[nm]
L_GAA	channel length of GAA NW FET	[nm]
L_sd	equal source and drain length	[nm]
L_t	tunneling length	[nm]
m_e	electron rest mass	[kg]
m_eff	effective electron mass	[kg]
n_eq	equivalent radial electron density	[cm^{-3}]
N	supply function	[eV]

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n_{i}	intrinsic electron concentration	[cm^{-3}]
$n_{\mathrm{i,eff}}$	effective intrinsic electron concentration	[cm^{-3}]
n_{C}	mobile electron concentration in the channel center	[cm^{-3}]
$N_{\mathrm{s/d/ch}}$	source/drain/channel doping concentration	[cm^{-3}]
P_{t}	tunneling probability	[−]
PN	product of tunneling probability and supply function	[eV]
q	electron charge	[A s]
$Q_{\mathrm{i,0}}$	inversion charge per unit area in short-channel DG FET calculated at any V_{gs} in the subthreshold region	[As/cm^2]
$Q_{\mathrm{i,2D}}$	total inversion charge per unit length in long-channel GAA NW FET assuming volume inversion at potential Φ_{S}	[A s cm^{-1}]
$Q_{\mathrm{i,d}}$	inversion charge per unit length at the drain end of short-channel GAA NW FET	[A s cm^{-1}]
$Q_{\mathrm{i,DG}}$	total inversion charge per unit area in long-channel DG FET derived from 2-D Laplace equation	[As/cm^2]
$Q_{\mathrm{i,fb}}$	inversion charge per unit length in short-channel GAA NW FET calculated at $V_{\mathrm{gs}} = V_{\mathrm{fb}}$	[A s cm^{-1}]
$Q_{\mathrm{i,GAA}}$	total inversion charge per unit length in long-channel GAA NW FET derived from 2-D Laplace equation	[A s cm^{-1}]
$Q_{\mathrm{i,s}}$	inversion charge per unit length at the source end of short-channel GAA NW FET	[A s cm^{-1}]
r	radial coordinate	[nm]
R	channel radius of GAA NW FET	[nm]
S_{sth}	subthreshold swing	[mV/dec]
T	ambient temperature	[K]
T_0	room temperature	[K]
T_{c}	critical temperature	[K]
T_{ch}	channel thickness	[nm]
$T_{\mathrm{ch}}^{\mathrm{DG}}$	channel thickness of DG FET	[nm]
$T_{\mathrm{ch}}^{\mathrm{GAA}}$	channel thickness of GAA NW FET	[nm]
$T_{\mathrm{ch}}^{\mathrm{QG}}$	channel thickness of GAA QG FET	[nm]
T_{ox}	gate oxide thickness	[nm]
V	potential energy	[eV]
$V_{\mathrm{bi}}^{\mathrm{s/d}}$	source/drain built-in potential	[V]
$V_{\mathrm{bi,eff}}^{\mathrm{s/d}}$	source/drain effective built-in potential	[V]

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$V_{\mathrm{s/d}}$	source/drain voltage	[V]
V_{ds}	drain-to-source voltage	[V]
V_{dsat}	drain saturation voltage	[V]
$\tilde{V}_{\mathrm{dss}}$	V_{ds} smoothly limited to V_{dsat}	[V]
V_{fb}	flatband voltage	[V]
V_{g}	gate voltage	[V]
V_{gs}	gate-to-source voltage	[V]
V_{gx}	V_{gs} smoothly limited to V_{T}	[V]
V_{th}	thermal voltage	[V]
V_{T}	threshold voltage	[V]
W_0	principal branch of the Lambert W function	[−]
W_{ch}	channel width	[nm]
W_{top}	top width of Ω-gate NW FET	[nm]
r	radial coordinate	[nm]
x	Cartesian coordinate	[nm]
x_{L}	x-position of the classical turning point on the left side of the barrier in a DG FET	[nm]
x_{m}	x-position of the potential barrier in a DG FET	[nm]
x_{R}	x-position of the classical turning point on the right side of the barrier in a DG FET	[nm]
$x_{\mathrm{s/d}}$	distance of the potential drop inside of the source/drain region in a DG FET	[nm]
y	Cartesian coordinate	[nm]
z	Cartesian coordinate	[nm]
z_{m}	z-position of the potential barrier in a GAA NW FET	[nm]

Greek Alphabet

Symbol	**Description**	**Unit**
α	wavelet coefficient	[−]
β	wavelet coefficient	[−]
γ	connection coefficient	[1/m^2]
$\Delta E_{\mathrm{bg/2}}$	energy discontinuity of the conduction band edge at the source/channel or drain/channel interface	[eV]

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ΔE^{QC}	energetic distance of the first subband from the conduction band edge	[eV]
$\Delta E^{\mathrm{QC}}_{\mathrm{DG}}$	energetic distance of the first subband from the conduction band edge of a DG FET	[eV]
$\Delta E^{\mathrm{QC}}_{\mathrm{GAA}}$	energetic distance of the first subband from the conduction band edge of a GAA NW FET	[eV]
$\Delta E^{\mathrm{QC}}_{\mathrm{QG}}$	energetic distance of the first subband from the conduction band edge of a QG FET	[eV]
$\Delta V^{\mathrm{QC}}_{\mathrm{T}}$	threshold voltage shift due to quantum confinement	[V]
$\varepsilon_{\mathrm{ch}}$	channel permittivity	[$\mathrm{A\,s\,V^{-1}\,cm^{-1}}$]
$\varepsilon_{\mathrm{ox}}$	oxide permittivity	[$\mathrm{A\,s\,V^{-1}\,cm^{-1}}$]
ε_{r}	relative permittivity	[−]
$\varepsilon_{\mathrm{s/d}}$	source/drain permittivity	[$\mathrm{A\,s\,V^{-1}\,cm^{-1}}$]
η	mother wavelet	[$1/\sqrt{\mathrm{m}}$]
θ	Heaviside step function	[−]
κ	channel permittivity devided by oxide permittivity	[−]
λ	connection coefficient	[$1/\mathrm{m}^2$]
λ	natural length	[nm]
λ_{DB}	de-Broglie wavelength	[nm]
φ	father wavelet or scaling function	[$1/\sqrt{\mathrm{m}}$]
ϕ	polar angle	[rad]
Φ_{C}	center electrostatic potential	[V]
Φ_{gs}	gate-source voltage reduced by the flatband voltage	[V]
Φ_{i}	inversion potential	[V]
Φ_{m}	potential barrier height	[V]
Φ_{S}	surface electrostatic potential	[V]
Ψ	1-D wave function	[$1/\sqrt{\mathrm{m}}$]
$\Psi^{\star}$	2-D electrostatic potential	[V]

Other

Symbol	Description	Unit
∂	partial differential operator	[−]

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List of Acronyms

Acronym	Description
1-D	one-dimensional
2-D	two-dimensional
3-D	three-dimensional
BJT	bipolar junction transistor
Ch	channel
CMOS	complementary metal-oxide-semiconductor
cm	compact modeling
D	drain
DC	direct current
DD	drift-diffusion
DD-model	drift-diffusion compact model
DD-sim	drift-diffusion simulation
DG	double-gate
DSDT	direct source-to-drain tunneling
DIBL	drain-induced barrier lowering
DIBT	drain-induced barrier thinning
EOT	equivalent oxide thickness
FEM	finite element method
FET	field-effect transistor
FinFET	fin field-effect transistor
G	gate
Ge	germanium
GAA	gate-all-around
HfO_2	hafnium dioxide

HfSiON	hafnium silicon oxynitride
IC	integrated circuit
ITRS	international technology roadmap for semiconductors
LETI	Laboratoire d'électronique des technologies de l'information
MBCFET	multi-bridge channel field-effect transistor
MIM	metal-insulator-metal
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MG	multiple-gate
NEGF	nonequilibrium Green's function
NEGF-sim	NEGF simulation
NS	nanosheet
NW	nanowire
PPM	parapolic potential model
QC	quantum confinement
QCM	quasi-compact model
QME	quantum mechanical effect
QG	quadruple-gate
S	source
SCE	short-channel effect
SG	single-gate
Si	silicon
SiNS	silicon nanosheet
SiO_2	silicon dioxide
SOI	silicon on insulator
sSi	strained silicon
TCAD	technology computer-aided design
TCE	thin-channel effect
TE	thermionic emission
TiN	titanium nitride
WKB	Wentzel-Kramers-Brillouin

CHAPTER 1

Introduction

Every year, large corporations literally flood the market with new generations of smartphones, tablets, TVs, computers, wearables and much more. Faster, better, cheaper is often the motto. Most of these devices have practically become a part of our lives and it is almost impossible to imagine life without them. It is amazing to see how many changes have taken place only over the last two decades. Considering this, we should be excited about the upcoming innovations of future decades. It would not be wrong to claim that we owe this fact primarily to the development of transistors. These electronic semiconductor devices are indispensable when it comes to electrical switching ON and OFF in analog and digital integrated circuits (ICs). A connection to an electrical circuit is realized with at least three terminals, where the third one controls the current flow between the other two terminals. The development of transistors is a milestone, which has immensely accelerated technological progress and whose inventors were deservedly honored with the Nobel Prize.

The improvement of transistor device parameters is the main activity of many scientists around the world. The aim is to achieve at lowest cost the highest possible performance with minimum energy consumption in the smallest possible space. Consequently, computer chips, which today consist of billions of transistors, are becoming more compact, more powerful and denser every year as the transistors become scaled down. The continuous reduction of the device structure is referred to as scaling. Unfortunately, as device parameters decrease, undesirable parasitic effects also occur, so an end to miniaturization is expected for reliable high-power transistors. Thanks to extensive research, the predicted scaling limit is being pushed back, but results in the need for increasingly complex device geometries which have to be in a continuous

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optimization process. The most commonly used and important transistor type in the semiconductor electronics industry is the so-called metal-oxide-semiconductor field-effect transistor (MOSFET).

In the following Section 1.1, the historical development of transistors and ICs is briefly discussed. Subsequently, Section 1.2 explains the reasons for a scaling limit of MOSFET and presents various possibilities to reduce parasitic effects. Section 1.3 discusses briefly the importance of device simulations as well as the relevance of compact modeling. In the last Section 1.4 of this chapter, an overview of the whole thesis is given with reference to the subsequent chapters. Finally, the last chapter gives an overall conclusion.

1.1 Historical Development of Transistors and Integrated Circuits

The history of transistors and ICs has several very important milestones. The first one was set almost one century ago when the physicist and electrical engineer Julius Edgar Lilienfeld patented the theory behind field-effect transistors (FETs) in 1925 entitled "Method and apparatus for controlling electric currents" [1]. The first working transistor, called the bipolar point-contact transistor was invented by John Bardeen and Walter Brattain under the leadership of William Shockley at Bell Labs 22 years later in December 1947 [2]. In particular, this was made possible by the reduction of surface states that led to the shielding of the semiconductor and prevented a working field-effect device. Only six month later, William Shockley developed on his own the grown-junction transistor, which was the first type of bipolar junction transistor (BJT). The difference to a point-contact transistor is that a BJT has instead of a point-contact a surface-contact for the three semiconductor zones emitter, base, and collector. In addition, the three-dimensional (3-D) manufacturing problem of a point-contact transistor is reduced to the less complicated two-dimensional (2-D) device structure of a BJT. Both inventions were patented one after another and published in 1950 and 1951 [3, 4]. The first non-germanium, but silicon-based transistor was developed by Morris Tanenbaum at Bell Labs in 1954 [5]. In the same year, commercial production of the silicon-based BJT was launched by Gordon Teal at Texas Instruments [6].

A few years passed before the material silicon (Si) was able to prevail over germanium (Ge). Undesirable surface states on Si impeded the penetration of electric fields into the semiconductor material. These could only be overcome by surface passivation of Si by means of thermal oxidation. The Egyptian engineer Mohamed Atalla explained this effect and, together with his Korean colleague Dawon Kahng, he developed the

first metal-oxide-semiconductor field-effect transistor (MOSFET) from it at Bell Labs in 1959 and patented it in 1960 [7–9]. This invention of an insulated gate (G) FET was another milestone, as it was the first well-scalable transistor in mass production [10]. Fig. 1.1 shows the MOSFET design from Dawon Kahng's patent [8].

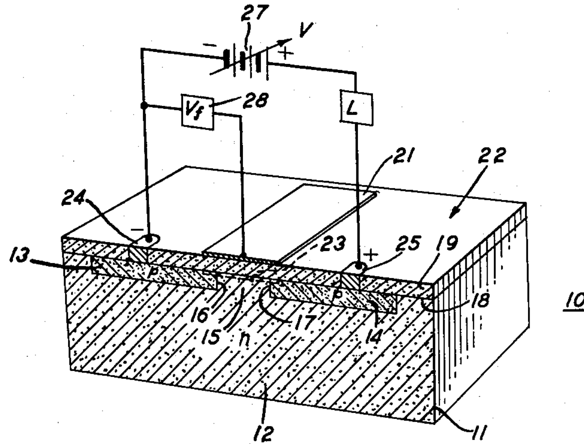

Figure 1.1: Geometric structure from Dawon Kahng's MOSFET patent [8].

In 1958, one year before the invention of MOSFET, the first IC was invented, patented and commercialized by Jack Kilby, an employee of Texas Instruments [11]. His invention, which represented the first milestone related to ICs, was honored with the Nobel Prize in physics 42 years later, in 2000. However, a decisive disadvantage of his invention was that it was a hybrid IC. The new technology required external wire connections, thus mass production was not easy. Fig. 1.2 shows Kilby's first IC with the wire bond connections between the devices.

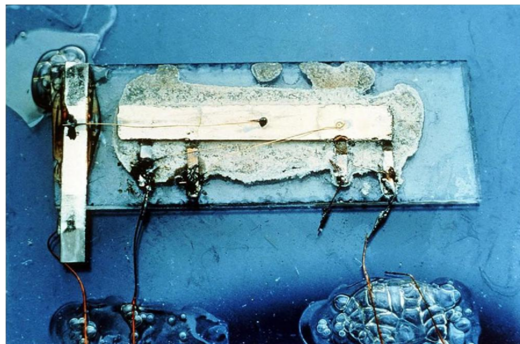

Figure 1.2: Kilby's Invention: The first hybrid IC made from germanium [12].

In 1959, in parallel with the invention of MOSFETs, the monolithic IC was invented at Fairchild Semiconductor by Robert Noyce, later co-founder of Intel Corporation. This was another milestone in circuit history. All components of the patented IC were connected planar via aluminum metal lines on a single chip (see Fig. 1.3) [13]. Together with the invention of MOSFETs high-density monolithic ICs became possible. Since then, transistors have been scaled down so that over the years several hundred million transistors can fit on a tiny little chip.

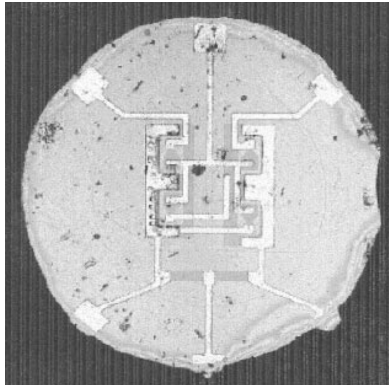

Figure 1.3: One of the first planar monolithic Si IC chip made at Fairchild [14].

Scientists widely agree that Kilby and Noyce would have shared the Nobel Prize if he had been alive during the award ceremony in 2000. Unfortunately, the regulations for awarding the Nobel Prize do not provide for honoring scientists who have already died, even if their contribution to science would be honorable.

1.2 Scaling Limit and Multigate MOSFET Architecture

It was Gordon E. Moore, another co-founder of Intel, who predicted already in 1965 that the transistor density of an IC would approximately double every two years due to the miniaturization of MOSFETs [15]. His observation has since become known as Moore's Law, and for about half a century it remained valid. Another very important statement about transistor density was made by him 40 years later. In an interview in 2005, he stated that the exponential increase in transistor density is slowing down and may come to an end by 2025 [16]. Reaching atomic sizes (diameter: 1-2 Å) is seen as a fundamental obstacle to the further miniaturization of transistors. Moore's Law was considered as the guide for long-term planning for the semiconductor industry. The evolution of the technology node is shown in Table 1.1 [17].

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Table 1.1: MOSFET scaling

No.	Technology Node	Year
1	10 μm	1971
2	6 μm	1974
3	3 μm	1977
4	1.5 μm	1981
5	1 μm	1984
6	800 nm	1987
7	600 nm	1990
8	350 nm	1993
9	250 nm	1996
10	180 nm	1999
11	130 nm	2001
12	90 nm	2003
13	65 nm	2005
14	45 nm	2007
15	32 nm	2009
16	22 nm	2012
17	14 nm	2014
18	10 nm	2016
19	7 nm	2018
20	5 nm	2020
	Future	
21	3 nm	2022
22	2 nm	2024

For a long time the node number was equivalent to the actual gate length of a metal-oxide-semiconductor (MOS) transistor on a chip. Since 1996, however, the designation node no longer represents any physical length of the transistor geometry and is primarily used for marketing purposes. Since then, a smaller node number stands only for a higher transistor density on the chip, shorter switching times and lower power consumption compared to its predecessor.

The downscaling of transistor geometries is not an easy challenge to overcome and pushes scientists more and more to its technological and fundamental limits. In addition to the lithographical manufacturing issues that must be overcome and the risk of overheating due to the extremely high transistor density on a chip [18], there are challenges associated with the functionality of a single nanoscale MOSFET. One of the major problems is the reduced electrostatic control of the channel (Ch) region

by the gate electrode as the channel length (L_{ch}) decreases and reaches the size of the depletion layer width of the source (S) and drain (D) junctions. As a consequence, the control of the current flow from the source to the drain region through the channel region is shared with the S/D electrodes. This type of parasitic effect belongs to the short-channel effects (SCEs) and negatively affects the performance of transistors.

Figure 1.4 shows a scheme of a typical planar single-gate (SG) n-MOS short-channel transistor in enhancement mode, and the related conduction band edge (E_{CB}) at gate biases far below the threshold voltage (V_{T}). The attenuation of the electrostatic gate control of the channel is demonstrated by increasing the drain-to-source bias (V_{ds}). The so-called drain-induced barrier lowering (DIBL) and in case of ultrashort-channel devices the additional drain-induced barrier thinning (DIBT) effects are two typical SCEs. The DIBL primarily affects V_{T}, which in simplified form decreases by the value of the DIBL. This is known as V_{T} roll-off and is not liked by IC designers who prefer V_{T} values independent of device geometry and bias conditions, which is the case for long-channel transistors. Furthermore, ultrathin Si layers influence V_{T} due to quantization of the energy subbands by quantum confinement (QC). Unlike the effect of DIBL on V_{T}, QC increases V_{T} due to an increase in barrier height through effective bandgap widening [19, 24]. The DIBT, on the contrary, reduces the effective channel length, which plays a fundamental role with respect to the quantum mechanical direct source-to-drain tunneling (DSDT), when the device dimensions in MOS devices reach single-digit nanometer ranges.

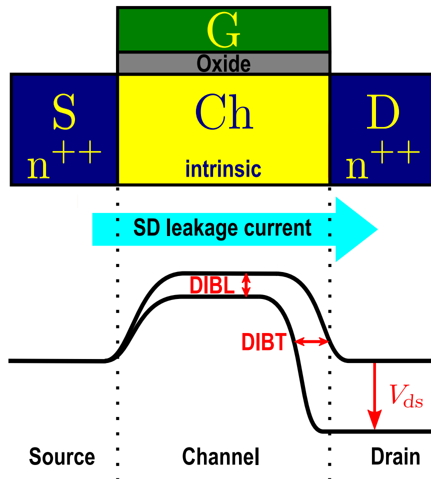

Figure 1.4: Sketch of a short-channel SG n-MOS and the corresponding E_{CB}. Demonstration of the DIBL and DIBT effect by increasing V_{ds}.

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With scaling, the subthreshold leakage current increases, which is defined as the current flow from source to drain in the OFF-state of the device, where an inversion channel has not yet been formed for current transport. The increase in leakage current leads to higher energy consumption in ICs and worse switching behavior of the MOSFET. A progressive degradation of the subthreshold swing (S_{sth}) takes place. The S_{sth} indicates the value by which the voltage (V_{gs}) between the gate and source electrode must be increased so that the current (I_{ds}) between drain and source increases by a factor of 10 ($S_{\mathrm{sth}} = \ln(10)\ \partial V_{\mathrm{gs}}/\partial \ln(I_{\mathrm{ds}})$). The smaller S_{sth} is, the shorter is the switching time of a transistor. In ideal MOSFETs without SCEs, this value is linearly temperature (T) dependent ($S_{\mathrm{sth}} = \ln(10)\,(k_{\mathrm{B}}T/q)$ where k_{B} is the Boltzmann's constant and q the elementary charge) and borders on 60 mV/dec at T= 300 K [25].

Another limitation in scaling concerns the gate oxide thickness (T_{ox}). To improve device performance, the loss of barrier height control by the gate can be counteracted by reducing the thickness of the insulating oxide layer with dielectric constant $\varepsilon_{\mathrm{ox}}$ between the channel and the gate electrode. This results in an increase in capacitance per gate area ($C'_{\mathrm{ox}} = \varepsilon_{\mathrm{ox}}/T_{\mathrm{ox}}$), which in turn reduces the potential drop within the insulating layer and, thus improves gate control. However, as a side effect, this leads to undesirable quantum mechanical electron tunneling through the thin dielectric [26, 27]. This additional leakage current from the source to the gate must be avoided as it leads to unnecessary power dissipation and potential heat source in ICs.

To suppress these scaling problems, material optimization became necessary. Better switching behavior was obtained in the 90 nm technology node by increasing the charge carrier mobility using strained silicon (sSi) in 2003 [28], and better gate control of the channel could be achieved in the 45 nm technology node in 2007 by replacing the gate insulator material from conventional silicon dioxide (SiO_2) to high-κ gate dielectric materials with much better insulating properties [29]. Replacing the dielectric material was an important step in improving the electrical performance without further T_{ox} scaling. The quality of the material improvement is often evaluated by the so-called equivalent oxide thickness (EOT), which compares the new high-κ dielectric with the standard SiO_2, and is obtained by equating both capacitors ($\mathrm{EOT} = T_{\mathrm{ox}}^{\text{high-}\kappa} \cdot \varepsilon_{\mathrm{ox}}^{\mathrm{SiO_2}}/\varepsilon_{\mathrm{ox}}^{\text{high-}\kappa}$).

In addition to material optimization, scientists are also working on alternative transistor structures to suppress the SCEs. The logical consequence to achieve much better gate control is to increase the number of gates surrounding the channel. Cylindrical gate-all-around (GAA) FETs are considered as the ultimate transistor structure among multiple-gate (MG) devices. The most important MG MOSFET structures are shown in Figure 1.5.

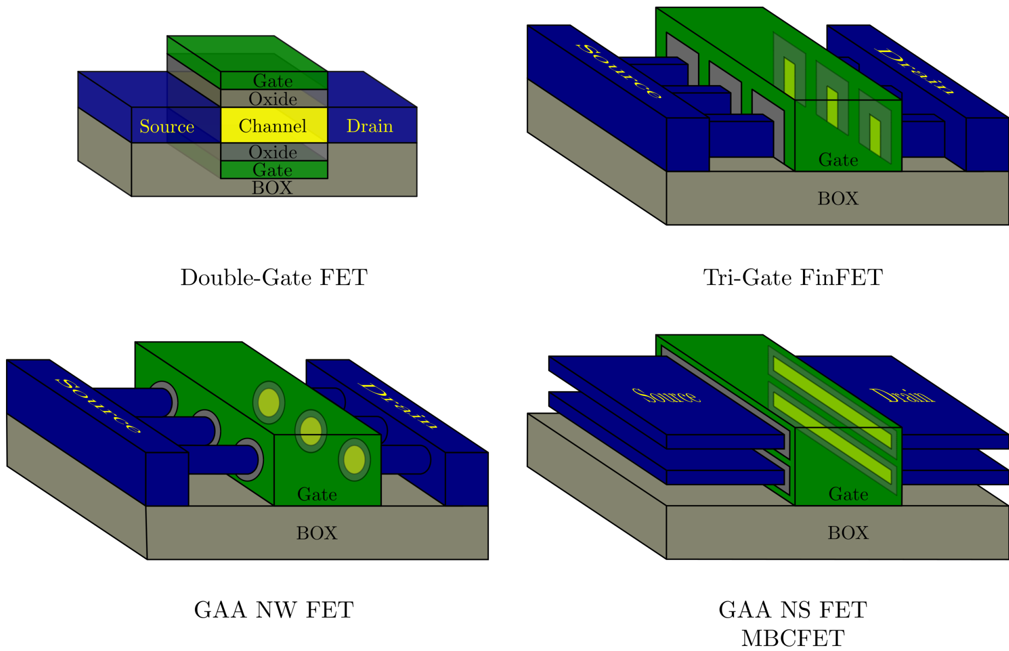

Figure 1.5: The four most important MG MOSFET structures.

A breakthrough advance was introduced by Intel in 2011 with the development of the first commercially available three-dimensional (3-D) tri-gate fin field-effect transistor (FinFET) structure in the 22 nm technology node with more than 2.9 billion transistors on the microprocessor (Ivy Bridge) [30]. The change from planar 2-D to 3-D technology was an important innovation to continue Moore's Law and to enable further voltage scaling and less power consumption. This revolutionary step was also predicted by the international technology roadmap for semiconductors (ITRS) [31].

The company Apple currently (2021) produces the commercially available microprocessor with the most transistors (see Fig. 1.6). The chip, called M1 Max, contains 57 billion MOSFETs and is manufactured using the 5 nm process technology of the Taiwanese company TSMC.

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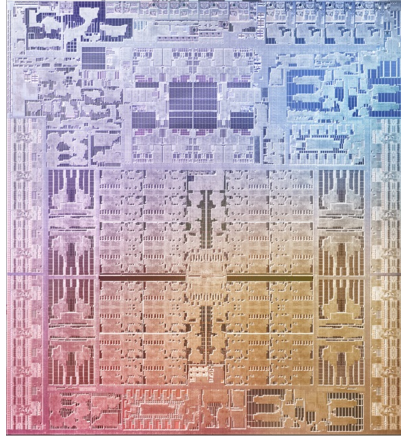

Figure 1.6: Apple's M1 MAX chip with 57 billion FinFETs [32].

The next shift in the transistor design is planned by Samsung in 2022. While other manufacturers e.g. Intel and TSMC will still rely on FinFETs technology in the 3 nm process node, Samsung plans to replace this transistor architecture entirely by GAA nanosheet (NS) FETs. Although cylindrical GAA FETs are considered as the ultimate transistor structure for ideal electrostatics, they are still difficult to fabricate, and the complexity of integration outweighs the benefits concerning SCEs. Furthermore, a larger channel area, as in NS transistors, is beneficial to achieve sufficient current flow through the device. Samsung has trademarked its own variant of the GAA NS FET under the name multi-bridge channel field-effect transistor (MBCFET). A key advantage of MBCFETs over FinFETs, besides less SCEs, is that it consists of vertically stacked nanosheets, which sets it apart from the FinFET technology. This type of manufacturing process is reminiscent of skyscrapers. This revolutionary design makes better use of the third dimension, so that a significant increase in transistor and power density can again be expected in the future, while the surface area remains the same.

1.3 Importance of Device Simulation and Relevance of Compact Modeling

The development of high-performance transistors and microprocessors is not an easy task. With each passing year, the requirements for individual transistors and ICs with high packaging density become ever greater and more complex. Since the invention of monolithic ICs, downscaling of device parameters plays by far the most important role in

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technological progress. New device structures are also an integral part of this evolution in technology. The transition from planar 2-D to 3-D technology increases the complexity, but in return we benefit from the physical advantages such as the suppression of SCEs. However, depending on the field of application, changes in material composition, device geometry and manufacturing techniques are not uncommon. It is always a risky and very costly step to change one or more of these parameters or to switch to totally novel structures. Therefore, it is even more important to know in advance before production how parameter changes affect the functionality of transistors individually and in circuits, and at which geometries and material compositions the necessary requirements can be met.

For this reason, companies such as Synopsys [33], Global TCAD Solutions [34], SILVACO [35] and others are developing technology computer-aided design (TCAD) simulation software to understand and predict the impact of device geometries, materials with different physical properties, different doping concentrations and profiles, ambient temperature and much more on, in particular, the I-V or C-V characteristics of transistors. In addition, TCAD simulations offer a deeper insight into the physical properties of the components, which can be determined purely by measurement either only with extremely high effort or not at all. These include among others the visualization of band structures, electric fields, current densities or charge carrier mobilities of both classical and, in single-digit nanoscale ranges, quantum mechanical nature.

These simulators numerically solve a system of elaborate and complex physical differential equations using the finite element method (FEM). As the name implies, this method divides the object under study into zones with sufficiently fine “finite elements” and solves the partial differential equations approximately. Subsequent iterations of the intermediate results are necessary to meet predefined convergence criteria in order to achieve a desired accuracy of the final simulation result. Depending on the mesh size and the physical models to be considered in the calculation, the simulation time can vary greatly, ranging from a few minutes to several days.

Considering that today’s microchips consist of tens of billions of transistors, a circuit simulation in a similar way would not be conceivable at all. It would simply be too time consuming. Therefore, circuit simulators such as SPICE [36] use very fast physics-based compact models of electronic components, which are simple mathematical or physical equations validated by FEM simulations or measurement results on test wafers. The more complex the device structure is, the more difficult it becomes to develop scalable compact models with high accuracy. It is often very helpful to make use of geometric symmetries to reduce 3-D problems to 2-D or even one-dimensional (1-D) problems by

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reasonable approximations. Thereby, it is not unusual to use physics-based, but bias independent fitting parameters.

In the literature, various solutions for cylindrical nanowire (NW) FETs can be found [20–23], but there are also attempts by researchers to develop unified models that are applicable to a variety of MOSFET geometries through small parameter changes [37, 38]. However, these solutions only work with restrictions. While they can be used for long-channel devices, they are not accurate enough when SCEs must be included. Thus, one challenge of this thesis is to describe 3-D ultrashort-channel cylindrical GAA NW FETs with a set of equivalent 2-D double-gate (DG) dimensions in order to implement them in the analytical potential model of a 2-D DG FET already developed by our research group [39].

Furthermore, nanodevices require the consideration of quantum mechanical effects (QMEs) in current transport. In particular, these include QC transverse to the channel direction and the DSDT effect. Depending on the simulation tool used, one or both of these effects can be taken into account by activating corresponding physical models. Among them, the numerical nonequilibrium Green's function (NEGF) formalism is considered as the most sophisticated one with high accuracy, but very time consuming. Thus, it is all the more important to develop compact models that, on the one hand, are very close to the NEGF results and, on the other hand, are significantly less complex and very fast to calculate. Therefore, this thesis also deals with the new wavelet-based DSDT calculation as a suitable replacement for the NEGF formalism or the widely used Wentzel-Kramers-Brillouin (WKB) method.

1.4 Outline of the Thesis

This doctoral thesis is a collection of conference and journal articles and focuses mainly on modeling of SCEs including QMEs in the two most interesting transistor structures of future technology nodes. In general, the chapters 2 and 3 refer to cylindrical NW FET and the chapters 4, 5 and 6 refer to silicon nanosheet (SiNS) FET. The final Chapter 7 gives overall conclusions and marks all the important results of the whole dissertation. In the following, a brief overview of the next five chapters is provided.

Chapter 2 presents an analytical method that enables for intrinsic or lightly doped channels in the subthreshold region the transfer of the 2-D DG analytical solution of Laplace's or Poisson's equation to a cylindrical NW geometry. With the equivalent potential model, the formulation of current equations for short-channel NW FETs follows, which are also based on DG FETs. Furthermore, the developed model is verified

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with FEM simulation and measurement data.

Chapter 3 focuses on the analysis, simulation, and model implementation of QC. Further, the equivalent potential model presented in Chapter 2 is confirmed by an equivalent capacitor model. The extended current model is verified by own measurements on a test wafer provided on loan by ASCENT member CEA-Leti.

Chapter 4 deals with the accurate determination of the DSDT tunneling probabilities ($P_{\mathrm{t}}\,(E_{\mathrm{x}})$) of electrons with different energies (E_{x}) and tunneling lengths (L_{t}) in ultrashort-channel DG FETs. P_{t} is numerically calculated using a new approach, the wavelet method. The influence of the tunneling current on short-channel characteristics (S_{sth} and DIBL) are compared with the numerically very sophisticated but reliable NEGF simulations and also with TCAD simulations using the WKB approach.

Chapter 5 describes an analytical calculation method for P_{t} and the tunneling current (I_{t}) for the purpose of compact modeling. Various approximations of E_{CB}, L_{t} and the tunneling current density (J_{t}) allow the formulation of a quasi-compact model (QCM). For comparison, all those approximations are implemented besides the wavelet method also in the WKB method. Again, both approaches are compared to NEGF simulation results of SiNS FETs.

Chapter 6 uses the analytical model from Chapter 5 as well as NEGF simulations for a further in-depth analysis of the subthreshold current in dependence of cryogenic temperature and S/D doping concentrations. In particular, the different saturation behavior of the subthreshold current, DIBL and swing in dependence of temperature at different S/D doping levels is investigated and physically explained. It turns out that the position of the Fermi level in the semiconductor material, which depends mainly on the chosen doping concentration, has a significant impact on the previously mentioned saturation behavior at low temperatures.

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CHAPTER 2

Equivalent Length Concept for Compact Modeling of Short-Channel GAA and DG MOSFETs

We present a way to analytically describe short-channel effects (SCEs) in cylindrical gate-all-around (GAA) MOSFETs with intrinsic or lightly-doped channels. For a given device dimension, the center and surface potentials (Φ_C and Φ_S) are correctly determined by using the conformal mapping technique for two-dimensional (2-D) double-gate (DG) FETs. An equivalent channel length is used in a compact drain current model of a DG device, which thereby is modified to get results for a cylindrical GAA MOSFET. To verify the introduced equivalent correlation for different channel lengths and thicknesses we compare both potentials Φ_C and Φ_S, the subthreshold swing (S_sth) and the drain-induced barrier lowering (DIBL) of our new compact model with 3-D GAA MOSFET TCAD simulation data. In addition, we compare for one chosen device dimension the direct current (DC) characteristics of our model with TCAD and measurement data.

2.1 Introduction

For an ideal subthreshold swing and to reduce the drain-induced barrier lowering (DIBL) effect in short-channel devices, it is necessary to surround the complete channel with gate material. As a consequence the electrostatic control of the gate electrode in GAA MOSFETs is much better than in DG MOSFETs.

For compact modeling it is a challenge to analytically describe GAA MOSFETs in 3-D with already existing DG compact models in 2-D. By cutting a cylindrical GAA MOSFET of radius R lengthwise through the center we get a 2-D DG MOSFET of

thickness $T_{\mathrm{ch}} = 2\ R$ (see Figure 2.1). This means, if we know the electrostatic behavior of the 2-D structure, we can trace back to the 3-D structure due to the rotational symmetry. By considering the subthreshold region the most important parameters, which are needed to capture the electrostatic of GAA MOSFETs are position and value of Φ_{C} and Φ_{S}.

Earlier evanescent-mode analysis [1] predict that DG MOSFETs have to be scaled to a 53 % larger channel length than GAA MOSFETs in order to provide the same immunity to short-channel effects. TCAD simulations show that a fixed conversion factor of 1.53 is not usable for all device dimensions, especially for short-channel devices. In addition, Φ_{C} and Φ_{S} need different conversion factors. Therefore, we derive an analytical expression which shows a dependence on the channel thickness $T_{\mathrm{ch}} = 2\ R$ and oxide thickness T_{ox}.

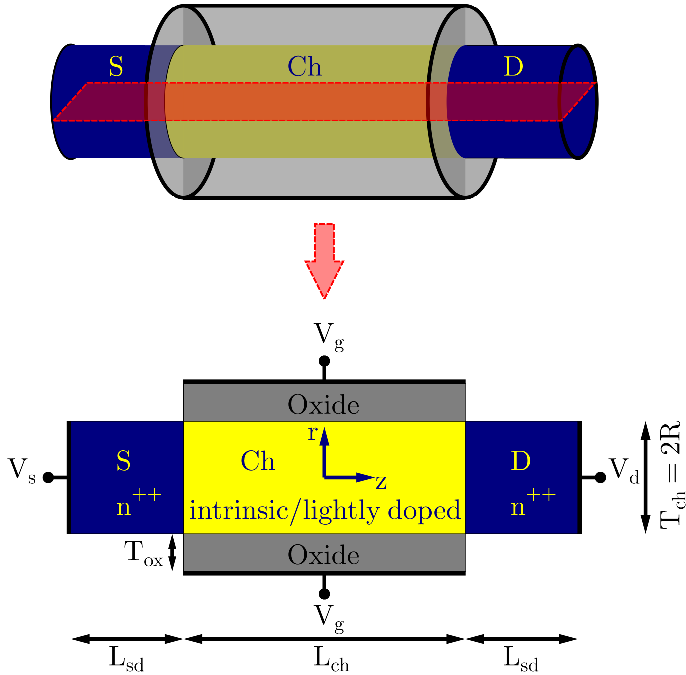

Figure 2.1: Sketch of a cylindrical GAA MOSFET and its DG cross section under study. Source/Drain (S/D) regions are highly n-doped ($N_{\mathrm{s/d}} = 10^{20}/\mathrm{cm}^3$) and $L_{\mathrm{sd}} = 10$ nm long. The channel (Ch) is intrinsic or lightly p-doped ($N_{\mathrm{ch}} \leq 10^{16}$). The gate oxide material is made of the high-κ material hafnium dioxide (HfO_2).

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2.2 Conversion Factor for the Channel Length

Similar to Young [2], we consider a parabolic potential $\Phi\,(r,z)$ through the channel thickness and derive an equation for the so-called natural length λ by solving the 2-D Poisson equation along the channel/oxide interface in cylindrical coordinates. The Poisson equation is as follows:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\Phi\,(r,z)\right)+\frac{\partial^2}{\partial z^2}\Phi\,(r,z)=\frac{qN_{\mathrm{ch}}}{\varepsilon_{\mathrm{ch}}} \tag{2.1}$$

with

$$\Phi\,(r,z)=c_0(z)+c_1(z)\cdot r+c_2(z)\cdot r^2. \tag{2.2}$$

N_{ch} is the channel doping concentration and $\varepsilon_{\mathrm{ch}}$ the dielectric constant of the silicon channel.

The following three boundary conditions are necessary to determine the three unknown values c_i (i = 0, 1, 2):

1. At the channel/oxide interface the potential is $\Phi_{\mathrm{S}}\,(z)$.

$$\Phi\,(R,z)=c_0(z)+c_1(z)\cdot R+c_2(z)\cdot R^2=\Phi_{\mathrm{S}}\,(z) \tag{2.3}$$

2. The electric field in the channel center is zero.

$$\left.\frac{\partial}{\partial r}\Phi\,(r,z)\right|_{r=0}=0=c_1(z) \tag{2.4}$$

3. The electric displacement fields D_{ch} and D_{ox} at the channel/oxide interface are equal.

$$D_{\mathrm{ch}}=\varepsilon_{\mathrm{ch}}\left.\frac{\partial}{\partial r}\Phi\,(r,z)\right|_{r=R}\stackrel{!}{=}\varepsilon_{\mathrm{ox}}\,E\,(R)=D_{\mathrm{ox}} \tag{2.5}$$

where $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of the gate oxide HfO_2. The 3-D surface electric field $E\,(R)$ of the oxide is given by:

$$E\,(R)=\frac{Q}{2\,\pi\,R\,L_{\mathrm{GAA}}+\varepsilon_{\mathrm{ox}}}=\frac{C_{\mathrm{ox}}\,(\Phi_{\mathrm{gs}}-\Phi_{\mathrm{S}}\,(z))}{2\,\pi\,R\,L_{\mathrm{GAA}}\,\varepsilon_{\mathrm{ox}}}=\frac{\Phi_{\mathrm{gs}}-\Phi_{\mathrm{S}}\,(z)}{R\ln\left(1+\frac{T_{\mathrm{ox}}}{R}\right)} \tag{2.6}$$

where C_{ox} is the cylindrical capacitor of a GAA-FET with the oxide thickness T_{ox} and the channel length $L_{\mathrm{ch}} = L_{\mathrm{GAA}}$.

The potential $\Phi(r,z)$ results from the boundary conditions as:

$$\Phi(r,z) = \Phi_{\mathrm{S}}(z) - \frac{\Phi_{\mathrm{gs}} - \Phi_{\mathrm{S}}(z)}{2\,\kappa\,\ln\left(1+\frac{T_{\mathrm{ox}}}{R}\right)} + \frac{\Phi_{\mathrm{gs}} - \Phi_{\mathrm{S}}(z)}{2\,\kappa\,\ln\left(1+\frac{T_{\mathrm{ox}}}{R}\right)}\frac{r^2}{R^2} \tag{2.7}$$

where $\kappa = \varepsilon_{\mathrm{ch}}/\varepsilon_{\mathrm{ox}}$.

Using (2.7) in (2.1) the Poisson equation along the channel surface becomes:

$$\frac{\partial^2 \Phi_{\mathrm{S}}(z)}{\partial z^2} - \frac{\Phi_{\mathrm{S}}(z) - \Phi_{\mathrm{gs}}}{(\lambda_{\mathrm{GAA}}^{\mathrm{S}})^2} = \frac{q\,N_{\mathrm{ch}}}{\varepsilon_{\mathrm{ch}}} \tag{2.8}$$

with

$$\lambda_{\mathrm{GAA}}^{\mathrm{S}} = \sqrt{\frac{1}{2}\,\kappa\,T_{\mathrm{ox}} R\left(\frac{R}{T_{\mathrm{ox}}}\ln\left(1+\frac{T_{\mathrm{ox}}}{R}\right)\right)} \tag{2.9}$$

Yan et al. [3] solves the natural length λ in Cartesian coordinates (2.10). Suzuki et al. [4] and Auth et al. [5] derive λ along the channel center, in Cartesian (2.11) and in cylindrical coordinates (2.12), respectively.

$$\lambda_{\mathrm{DG}}^{\mathrm{S}} = \sqrt{\kappa\,T_{\mathrm{ox}}\,R} \tag{2.10}$$

$$\lambda_{\mathrm{DG}}^{\mathrm{C}} = \sqrt{\kappa\,T_{\mathrm{ox}}\,R\left(1+\frac{R}{2\,\kappa\,T_{\mathrm{ox}}}\right)} \tag{2.11}$$

$$\lambda_{\mathrm{GAA}}^{\mathrm{C}} = \sqrt{\frac{1}{2}\,\kappa\,T_{\mathrm{ox}}\,R\left(\frac{R}{T_{\mathrm{ox}}}\ln\left(1+\frac{T_{\mathrm{ox}}}{R}\right)+\frac{R}{2\,\kappa\,T_{\mathrm{ox}}}\right)} \tag{2.12}$$

In all four cases the potential drops exponentially along the channel as $\Phi(r,z) \propto \exp(\pm\, z/\lambda)$. To obtain in a DG and GAA device along the surface and center of the channel the same potential profile we compare the corresponding exponents. Thus, we get the conversion factor for coordinate z, and hence the equivalent channel length:

$$z_{\mathrm{DG}}^{\mathrm{S}} = \sqrt{2}\cdot\sqrt{\frac{T_{\mathrm{ox}}/R}{\ln\left(1+\frac{T_{\mathrm{ox}}}{R}\right)}}\cdot z_{\mathrm{GAA}}^{\mathrm{S}} \tag{2.13}$$

$$z_{\mathrm{DG}}^{\mathrm{C}} = \sqrt{2}\cdot\sqrt{\frac{1+\frac{R}{2\,\kappa\,T_{\mathrm{ox}}}}{\frac{R}{T_{\mathrm{ox}}}\ln\left(1+\frac{T_{\mathrm{ox}}}{R}\right)+\frac{R}{2\,\kappa\,T_{\mathrm{ox}}}}}\cdot z_{\mathrm{GAA}}^{\mathrm{C}} \tag{2.14}$$

In equation (2.14), the second term in the numerator and denominator are dominant over the first term for $R >> T_{\text{ox}}$. This results in $z_{\text{DG}}^{\text{C}} \approx \sqrt{2}\, z_{\text{GAA}}^{\text{C}}$.

Furthermore, Oh et al. [1] hold the view that a parabolic approximation of Φ differs widely from that of the sinusoidal solution and derive a potential $\Psi^{\star}$ for DG and GAA MOSFETs, which satisfies the Laplace equation. We simplify these equations due to the fact that source and drain are equally doped and consider them without any bias:

$$\Psi_{\text{DG}}^{\star} \approx \Phi_{\text{C}} \cos\left(\frac{x}{\lambda'_{\text{DG}}}\right) \cosh\left(\frac{z_{\text{DG}}}{\lambda'_{\text{DG}}}\right) \tag{2.15}$$

$$\Psi_{\text{GAA}}^{\star} \approx \Phi_{\text{C}}\, J_0\left(\frac{r}{\lambda'_{\text{GAA}}}\right) \cosh\left(\frac{z_{\text{GAA}}}{\lambda'_{\text{GAA}}}\right) \tag{2.16}$$

J_0 is the Bessel function of order zero. By assuming $R >> T_{\text{ox}}$ and fulfilling the boundary condition for both DG and GAA device at the channel/oxide interface ($x = r = R + \kappa\, T_{\text{ox}}$) considering the effective electrical oxide thickness it follows $z_{\text{DG}}^{\text{S}} \approx \left(\lambda_{\text{DG}}'^{S}/\lambda_{\text{GAA}}'^{S}\right) z_{\text{GAA}}^{\text{S}} \approx 1.53\, z_{\text{GAA}}^{\text{S}}$, with $\lambda_{\text{DG}}'^{S} = 2\ (R + \kappa\, T_{\text{ox}})/\pi$ and $\lambda_{\text{GAA}}'^{S} = 2\ (R + \kappa\, T_{\text{ox}})/4.810$ [1]. In addition we compare both equations (2.15), (2.16) along the center of a device by a first order Taylor polynomial without any regard to the boundary conditions at the channel/oxide interface:

$$\cos\left(\frac{x}{\lambda_{\text{DG}}'^{C}}\right) \approx 1 - \frac{x^2/2}{\left(\lambda_{\text{DG}}'^{C}\right)^2} \overset{!}{\approx} 1 - \frac{r^2/4}{(\lambda_{\text{GAA}}'^{C})^2} \approx J_0\left(\frac{r}{\lambda_{\text{GAA}}'^{C}}\right) \tag{2.17}$$

This results in $\lambda_{\text{DG}}'^{C} = \sqrt{2}\ \lambda_{\text{GAA}}'^{C}$. Accordingly, we get two different conversion factors for surface and center: $z_{\text{DG}}^{\text{S}} \approx 1.53\, z_{\text{GAA}}^{\text{S}}$ and $z_{\text{DG}}^{\text{C}} \approx \sqrt{2}\, z_{\text{GAA}}^{\text{C}}$.

In the first place we realize by comparing DG and GAA simulation data that the sinusoidal solution of the potential gives better results at the channel/oxide interface than the parabolic ansatz. On the other hand we need a device dimensions dependent conversion factor, which is achieved with the parabolic solution. As a conclusion, combining both leads to the best solution. Thus, we obtain two different conversion factors for the surface and center potential:

$$z_{\text{DG}}^{\text{S}} = 1.53 \cdot \sqrt{\frac{T_{\text{ox}}/R}{\ln\left(1 + \frac{T_{\text{ox}}}{R}\right)}}\, z_{\text{GAA}}^{\text{S}} \tag{2.18}$$

$$z_{\text{DG}}^{\text{C}} = \sqrt{2} \cdot \sqrt{\frac{T_{\text{ox}}/R}{\ln\left(1 + \frac{T_{\text{ox}}}{R}\right)}}\, z_{\text{GAA}}^{\text{C}} \tag{2.19}$$

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2.3 Inversion Charge and Current Equation

The DG compact model from Kloes et al. [6] uses the total inversion charge $Q_{\mathrm{i,0}}$ for any gate-source bias $V_{\mathrm{gs}} = V_0$ in the subthreshold region. This charge at the potential barrier at position z_{m} is used to calculate the total drain current I_{ds}. We determine $Q_{\mathrm{i,0}} \to Q_{\mathrm{i,fb}}$ for a gate-source bias at the flatband voltage $V_0 = V_{\mathrm{fb}}$ by integration over the density of free electrons $n\,(r) = n_{\mathrm{i}}\,\exp\left(\Phi(r,z_{\mathrm{m}})/V_{\mathrm{th}}\right)$ within the channel cross section $A = \pi R^2$ at the virtual cathode. As a modification we take advantage of the rotational symmetry and integrate in cylindrical coordinates with $dA = r\,dr\,d\phi$:

$$Q_{\mathrm{i,fb}} = q \int_A n_{\mathrm{i}}\, e^{\frac{\Phi(r,z_{\mathrm{m}})}{V_{\mathrm{th}}}}\, dA \tag{2.20}$$

where n_{i} is the intrinsic carrier density and $V_{\mathrm{th}} = k_{\mathrm{B}}T/q$ the thermal voltage.

Considering a parabolic potential $\Phi\,(r) = \Phi_{\mathrm{C}}$ - $\frac{r^2}{R^2}\,(\Phi_{\mathrm{C}} - \Phi_{\mathrm{S}})$ through the channel thickness with Φ_{C} and Φ_{S} at position z_{m} leads to:

$$Q_{\mathrm{i,fb}} = q \int_0^{2\pi}\int_0^{R} n_{\mathrm{i}}\, e^{\frac{\Phi_{\mathrm{C}} - \frac{r^2}{R^2}(\Phi_{\mathrm{C}} - \Phi_{\mathrm{S}})}{V_{\mathrm{th}}}}\, r\,dr\,d\phi = \frac{q\,\pi\,V_{\mathrm{th}}\,n_{\mathrm{i}}\,R^2}{\Phi_{\mathrm{C}} - \Phi_{\mathrm{S}}}\left(e^{\frac{\Phi_{\mathrm{C}}}{V_{\mathrm{th}}}} - e^{\frac{\Phi_{\mathrm{S}}}{V_{\mathrm{th}}}}\right) \tag{2.21}$$

The transition to above threshold region is enabled by assuming volume inversion in the channel at potential Φ_{S} without considering short channel effects. The integral inversion charge in the channel cross section is:

$$Q_{\mathrm{i,2D}} = q\,\pi\,n_{\mathrm{i}}\,R^2\,e^{\frac{\Phi_{\mathrm{S}}}{V_{\mathrm{th}}}} \tag{2.22}$$

The charge potential relationship is given by:

$$C'_{\mathrm{ox}}(V_{\mathrm{gs}} - V_{\mathrm{fb}} - \Phi_{\mathrm{S}}) = Q_{\mathrm{i,2D}} \tag{2.23}$$

For the capacitance we insert the cylindrical capacitor per gate length instead of the parallel-plate capacitor of a DG-FET:

$$C'_{\mathrm{ox}} = \frac{2\,\pi\,\varepsilon_{\mathrm{ox}}}{\ln\left(1 + T_{\mathrm{ox}}/R\right)} \tag{2.24}$$

Analogous to (6)-(14) in [6], we obtain following expression from (2.22) and (2.23)

for the mobile charge density $Q_{\mathrm{i,s}}$ at the source end in a GAA device:

$$Q_{\mathrm{i,s}} = \alpha\, C'_{\mathrm{ox}}\, V_{\mathrm{th}} \times W_0 \left\{ \frac{Q_{\mathrm{i,fb}}}{\alpha\, C'_{\mathrm{ox}}\, V_{\mathrm{th}}} \exp\left(\frac{C'_{\mathrm{ox}}(V_{\mathrm{gs}} - V_{\mathrm{fb}}) + Q_{\mathrm{i,fb}}}{\alpha C'_{\mathrm{ox}} V_{\mathrm{th}}} \right) \right\}, \tag{2.25}$$

where α is the ratio between the degraded S_{sth} and the ideal swing (60 mV per decade at $T = 300$ K). W_0 stands for the principal branch of the Lambert W function.

The mobile charge density $Q_{\mathrm{i,d}}$ at the drain end is calculated as follows:

$$Q_{\mathrm{i,d}} = Q_{\mathrm{i,s}} - C'_{\mathrm{ox}} \tilde{V}_{\mathrm{dss}}, \tag{2.26}$$

where $\tilde{V}_{\mathrm{dss}}$ is the voltage V_{ds} smoothly limited by the saturation voltage and allows the smoothly transition between subthreshold and above threshold region.

In [7] a charge-based model for drain current I_{ds} of symmetric DG MOSFETs has been presented. This model can simply be transferred to a cylindrical GAA MOSFET. The channel width in the current equation for DG has to be removed, since this dimension is already considered by integration in (2.21). Finally, the total drain current is:

$$I_{\mathrm{ds}} = \frac{\mu}{L_{\mathrm{GAA}}} \left[V_{\mathrm{th}}(Q_{\mathrm{i,s}} - Q_{\mathrm{i,d}}) + \frac{(Q_{\mathrm{i,s}}^2 - Q_{\mathrm{i,d}}^2)}{2\, C'_{\mathrm{ox}}} \right]. \tag{2.27}$$

The subthreshold swing S_{sth} including short-channel effect can be calculated from the current equation I_{ds}. For small gate biases the current is approximately proportional to the charge $Q_{\mathrm{i,fb}}$. Hence we get S_{sth} from the potential $\Phi_{\mathrm{C}}\,(\Phi_{\mathrm{g}})$ and $\Phi_{\mathrm{S}}\,(\Phi_{\mathrm{g}})$ for a given gate potential Φ_{g} as follows:

$$\begin{aligned} S_{\mathrm{sth}} &= \ln(10)\, \frac{\partial V_{\mathrm{gs}}}{\partial \ln(Q_{\mathrm{i,fb}})} \approx \ln(10)\, \frac{\Delta V_{\mathrm{gs}}}{\Delta \ln(Q_{\mathrm{i,fb}})} \\ &= \frac{\ln(10)\, \Delta V_{\mathrm{gs}}}{\ln\left(\frac{e^{\Phi_{\mathrm{C},2}/V_{\mathrm{th}}} - e^{\Phi_{\mathrm{S},2}/V_{\mathrm{th}}}}{e^{\Phi_{\mathrm{C},1}/V_{\mathrm{th}}} - e^{\Phi_{\mathrm{S},1}/V_{\mathrm{th}}}} \right) - \ln\left(\frac{\Phi_{\mathrm{C},2} - \Phi_{\mathrm{S},2}}{\Phi_{\mathrm{C},1} - \Phi_{\mathrm{S},1}} \right)}, \end{aligned} \tag{2.28}$$

where $\Delta V_{\mathrm{gs}} = 0.1$ V, $\Phi_{\mathrm{C},2} = \Phi_{\mathrm{C}}(\Delta V_{\mathrm{gs}})$, $\Phi_{\mathrm{C},1} = \Phi_{\mathrm{C}}(0)$, $\Phi_{\mathrm{S},2} = \Phi_{\mathrm{S}}(\Delta V_{\mathrm{gs}})$ and $\Phi_{\mathrm{S},1} = \Phi_{\mathrm{S}}(0)$.

We determine the drain-induced barrier lowering from S_{sth} and two OFF currents at different drain-source biases $V_{\mathrm{ds},2}$ and $V_{\mathrm{ds},1}$ as follows:

$$DIBL = S_{\mathrm{sth}}\, \frac{\ln\left(Q_{\mathrm{i,fb}}(V_{\mathrm{ds},2})/Q_{\mathrm{i,fb}}(V_{\mathrm{ds},1})\right)}{\ln(10)\,(V_{\mathrm{ds},2} - V_{\mathrm{ds},1})} \tag{2.29}$$

2.4 Model Verification

Applying the conversion factors from (2.18) and (2.19) to the channel length in the analytical potential model [8] of a DG transistor we obtained the results for GAA devices shown in Figure 2.2. We see an excellent agreement of Φ_{C}, Φ_{S}, DIBL and S_{sth} for different channel lengths and radius's between TCAD simulation data and our new developed compact model.

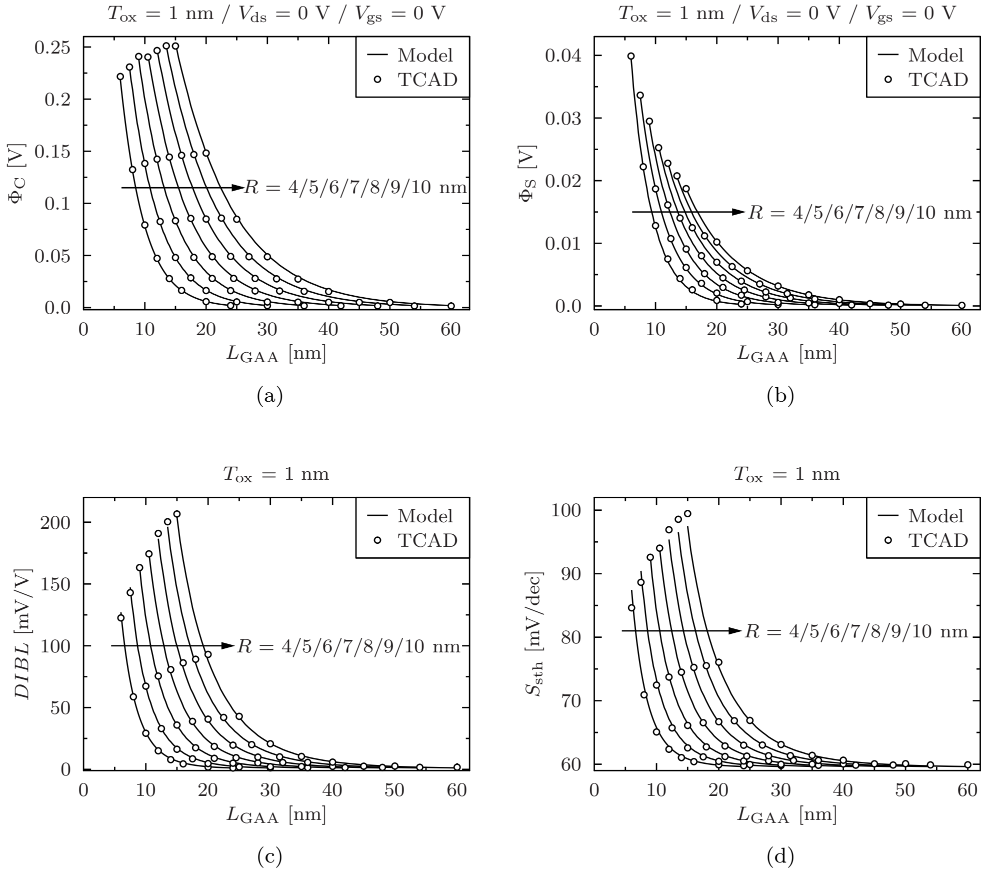

Figure 2.2: Comparison of compact model (lines) with TCAD simulations (symbols) of (a) center, (b) surface potential, (c) DIBL and (d) subthreshold swing as a function of L_{GAA} with various channel radius.

In Figure 2.3 for a chosen GAA device showing short-channel effect we compare the transfer and output characteristics with TCAD. We implemented the conversion factors

(2.18), (2.19) and the total inversion charge (2.21), capacitance (2.24) and subthreshold swing (2.28) of a cylindrical GAA-FET into the DG compact model from [6] to obtain a model for a GAA device. Once again we see that it is possible to obtain a very good match between TCAD Sentaurus data and results from the compact model (S_{sth} = 71 mV/dec, DIBL = 59 mV/V).

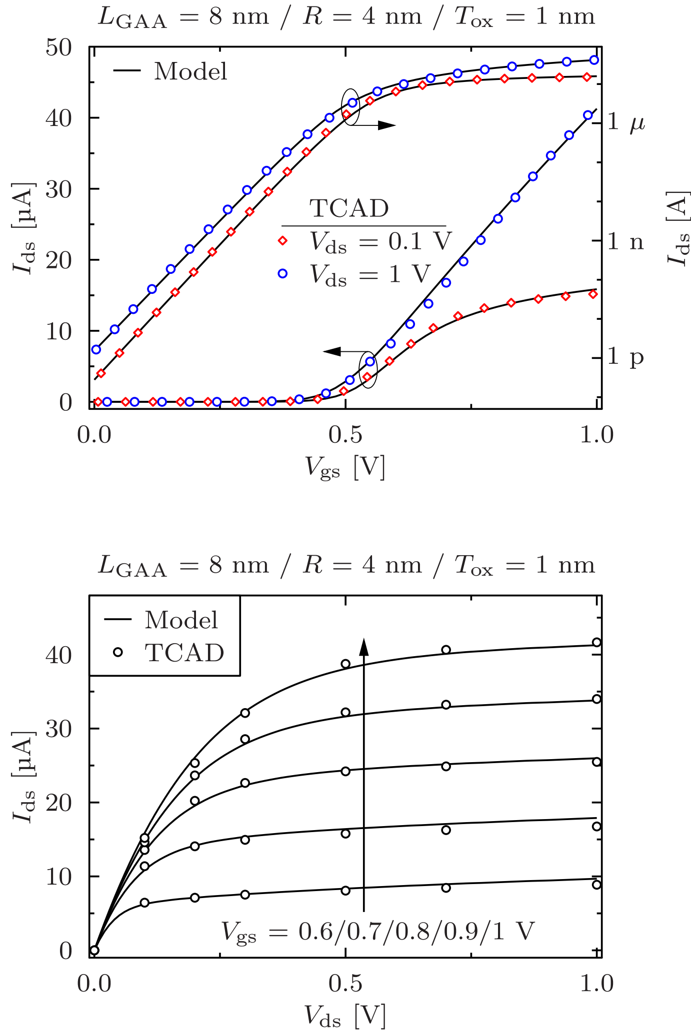

Figure 2.3: Comparison of compact model (lines) with TCAD simulations (symbols) of transfer and output characteristics of a short-channel GAA MOSFET.

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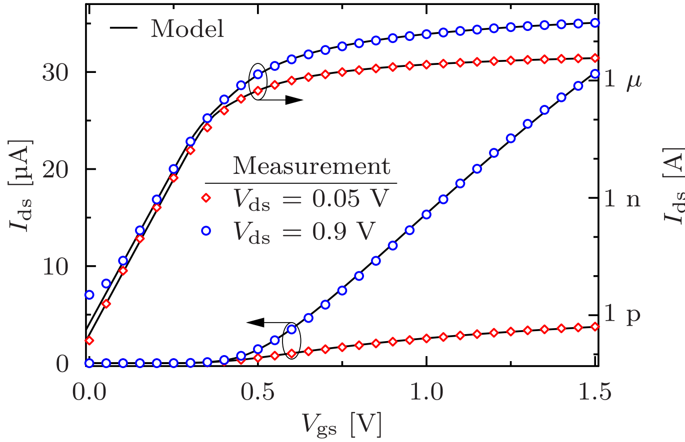
In Figure 2.4 our model is compared with measurement data of two devices with 24 nm and 28 nm gate length [9]. We don't know how far the dopants penetrate from source and drain into the channel. Therefore, the effective channel length is a fitting parameter in our model. It has to be 12.5 nm and 16.5 nm in order to get the right swing and DIBL. This means that the dopants penetrate from both sides in average about 5-6 nm, which is reasonable.



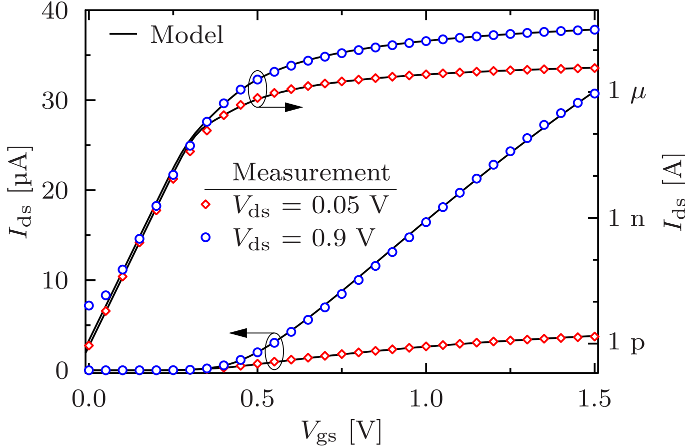


Figure 2.4: Experimental data (symbols) [9] and compact model (lines) of a GAA n-MOSFET. The effective channel length L_{eff} is almost half of the indicated gate length L_g.

However, additional experimental data including output characteristics are under preparation to further verify the new compact model for even shorter channel lengths with more pronounced short-channel effects.

2.5 Conclusion

We developed an analytical concept to convert the electrostatics of a GAA to an equivalent DG MOSFET. Different scaling factors for surface and center potential relate GAA to DG concepts regarding their short-channel immunity. Thus a DG current model can be used to predict the DC behavior of ultimately scaled GAA MOSFETs.

Acknowledgment

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CHAPTER 3

Equivalent DG Dimensions Concept for Compact Modeling of Short-Channel and Thin Body GAA MOSFETs Including Quantum Confinement

In this work, short-channel effects (SCEs) in cylindrical gate-all-around (GAA) MOSFETs with intrinsic or lightly doped channels are analytically described by using the conformal mapping technique for two-dimensional (2-D) double-gate (DG) FETs. An equivalent capacitor model leads to an equivalent channel length concept, which allows to correctly determine the SCEs relevant center and surface potentials (Φ_C and Φ_S) at the potential barrier. Furthermore, we make use of the rotational symmetry of GAA FETs and modify a compact drain current model of a DG device to use it for GAA transistors. Also, a mathematical correlation regarding quantum confinement for thin body transistors is derived, which shows that the mostly unwanted quantum effects occur in GAA structures already for thicker channels compared to DG transistors. Both transistor types experience a comparable influence with regard to quantization if the channel thickness of GAA FETs is 53% more than that of DG FETs. The dc behavior of our adapted model is verified with 3-D TCAD simulation data and applied to experimental data of ultrascaled silicon on insulator (SOI) omega-gate nanowire N-MOSFETs.

3.1 Introduction

Excellent electrostatic gate control in MOSFETs is very important for ideal subthreshold transfer characteristics. This control decreases and gains more and more importance the closer the device dimensions reaches into single-digit nanometer ranges [1], [2]. The gate

control becomes difficult due to increasing influence of the source and drain regions on the channel electrostatics. This influence can be reduced by enclosing the whole channel from all sides with gate material. As a result, cylindrical gate-all-around (GAA) FETs offer significantly better resistance to higher subthreshold swing (S_{sth}) and drain-induced barrier lowering (DIBL) than double-gate (DG) FETs. Therefore, GAA FETs are of great interest and belong to the most promising devices due to their superior gate control over the channel that suppresses short-channel effects (SCEs) and leakage currents [3–6]. Nevertheless, SCEs do occur, which have to be considered in circuit design by the use of accurate compact models.

Several authors have published different modeling approaches for downscaled multiple-gate (MG) MOSFETs that use either numerical solutions or analytical expressions and consider SCEs [7–9]. In previous publications, the possibility to model MG FETs with the help of equivalent DG FETs has been investigated too. In [10], a concept of equivalent thickness and width is presented and in [11] a unified analytic drain-current model for different MG FETs is published, which uses the proportionality of the inversion charge to the silicon cross-sectional area in the subthreshold and to the gate perimeter of the silicon body in the above threshold region. A further concept to link planar and even cylindrical junctionless FETs is described in [12]. Unfortunately, all three models are only valid for long channel transistors and do not consider SCEs.

In [13] we presented an analytical concept to capture the electrostatics of a GAA FET with an equivalent 2-D DG FET. The used potential model is based on the conformal mapping technique and solves the 2-D Poisson's equation approximately in the subthreshold region in an analytical closed-form [14]. The model neglects mobile carriers in the channel, but includes the influence of source-drain doping on the subthreshold characteristics. It is applicable because the lengthwise cut through the center of a cylindrical GAA FET has the shape of a DG FET (see Figure 3.1). The model requires different equivalent channel length for surface and center potentials (Φ_{S} and Φ_{C}) to relate GAA to DG concepts regarding their short-channel immunity. This equivalent length concept was derived from Laplace's and Poisson's equation and shall now be derived from a comparison of capacitor models.

In Section 3.2, we will initially derive a concept to describe the electrostatics in a GAA FET by a DG FET with equivalent key parameters as DIBL and slope. Then in Section 3.3 we will transfer a charge-based long-channel DG current model to a long-channel cylindrical GAA current model. Section 3.4 modifies charge expressions of a potential-based (short-channel) DG model to be applicable to the GAA FET and to use them in the previously derived GAA current model. In Section 3.5, quantum

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confinement (QC) effects are discussed and a way to include them in the model is proposed. The compact model is verified by comparison to TCAD and measurements in Section 3.6. Finally, Section 3.7 gives a conclusion.

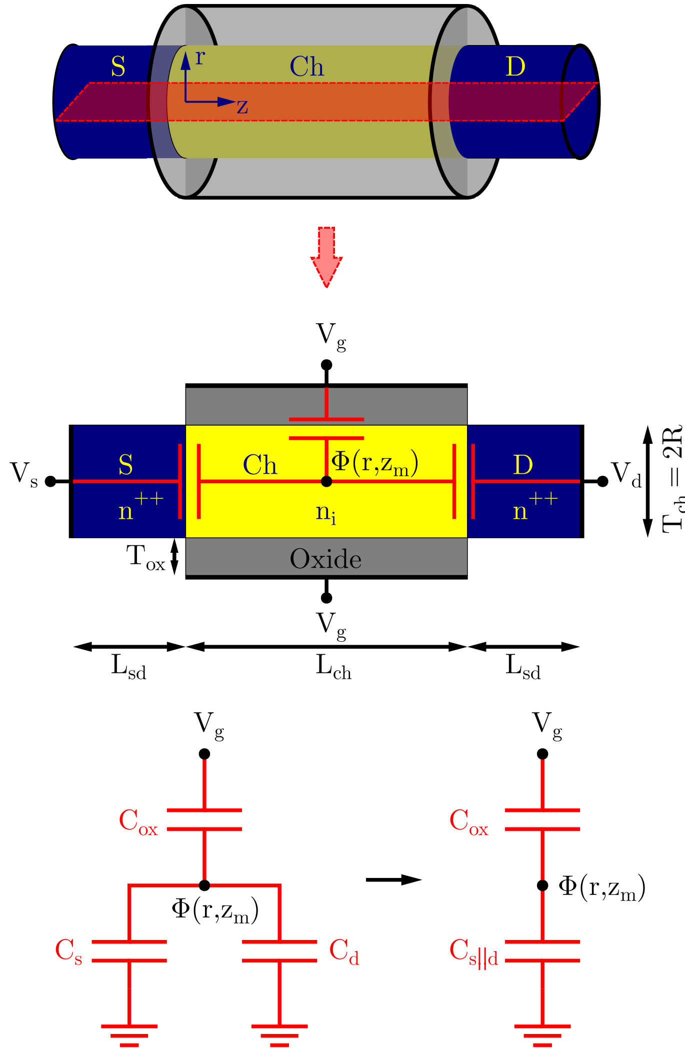

Figure 3.1: Sketch of a cylindrical GAA MOSFET, its DG cross section and the corresponding simplified capacitor circuit under study. Source-drain (S/D) regions are highly n-doped. The channel (Ch) is intrinsic or lightly p-doped ($N_{ch} \leq 10^{16}$ cm^{-3}) and the gate oxide is a high-κ material. In the capacitor circuit, exemplary the S/D terminals are grounded, while a voltage is applied to the gate terminal.

3.2 Capacitor Based Derivation of the Equivalent DG Dimensions

We focus on the subthreshold region and assume that cylindrical GAA and DG FETs only provide comparable DIBL and S_{sth} if the shape of the potential barrier through the channel thickness is almost identical for the same bias conditions. For this, we keep the channel and oxide thicknesses equal and determine an equivalent channel length that is responsible for SCEs.

Lundstrom describes a capacitor model in [15], where each capacitor stands for the electrostatic coupling of a terminal to the potential barrier $\Phi\,(r{,}z_{\mathrm{m}})$ at position z_{m}, which is the virtual source for the device. We apply his model to our DG and GAA FETs and analyze the simple circuit in Figure 3.1.

A distinction between Φ_{C} and Φ_{S} will be introduced later. We assume that only the gate or drain terminal is biased. The respective other one is grounded together with the source terminal and connected in parallel. The simplified circuit thus represents a capacitive voltage divider. Assuming subthreshold operation and hence, negligible charge at the potential barrier, the potential at the virtual source is given by superposition as

$$\Phi = \left(\frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + C_{\mathrm{s}||\mathrm{d}}}\right) V_{\mathrm{g}} + \left(\frac{C_{\mathrm{d}}}{C_{\mathrm{ox}} + C_{\mathrm{s}||\mathrm{d}}}\right) V_{\mathrm{d}} \tag{3.1}$$

where $C_{\mathrm{s}||\mathrm{d}} = C_{\mathrm{s}} + C_{\mathrm{d}}$. Since the source to drain current I_{ds} is exponentially related to the height of the potential barrier as

$$I_{\mathrm{ds}} \propto \exp\left(\Phi\,(r{,}z_{\mathrm{m}})\,/V_{\mathrm{th}}\right) \tag{3.2}$$

the subthreshold swing at a constant drain voltage can be determined from the definition

$$S_{\mathrm{sth}} = \ln(10)\,\frac{\partial V_{\mathrm{gs}}}{\partial \ln\left(I_{\mathrm{ds}}\right)} = \eta\,\ln\left(10\right)\,V_{\mathrm{th}} \tag{3.3}$$

with

$$\eta = 1 + \frac{C_{\mathrm{s}||\mathrm{d}}}{C_{\mathrm{ox}}} \tag{3.4}$$

where $V_{\mathrm{th}} = k_{\mathrm{B}}\,T/q$ is the thermal voltage, k_{B} the Boltzmann's constant, T the temperature and q is the elementary charge.

Furthermore, S_{sth} increases with the drain voltage, since the capacitors also vary with bias. By applying a drain bias, the potential shape along the channel gets significantly

influenced. The position of the potential barrier moves toward the source and reduces the classical plate distance of the source capacitor and correspondingly increases the plate distance of the drain capacitor. In total, $C_{\mathrm{s||d}}$ is slightly increasing because C_{s} is dominant over C_{d}. Keeping this in mind, we equate S_{sth} for GAA and DG FETs and establish the following correlation between capacitors:

$$S_{\mathrm{sth}}^{\mathrm{GAA}} = S_{\mathrm{sth}}^{\mathrm{DG}} \Leftrightarrow \left(\frac{C_{\mathrm{s||d}}}{C_{\mathrm{ox}}}\right)^{\mathrm{GAA}} = \left(\frac{C_{\mathrm{s||d}}}{C_{\mathrm{ox}}}\right)^{\mathrm{DG}}. \tag{3.5}$$

At this point, we assume for simplicity that the relative deviation of the bias dependent changes in the S/D capacitors are the same between GAA and DG FETs, so that they cancel each other out in (3.5).

Table 3.1 lists the formulas for GAA and DG FETs related capacitors, where $\varepsilon_{\mathrm{ch}}$ and $\varepsilon_{\mathrm{ox}}$ are the dielectric constant of the silicon channel and the gate oxide, L_{GAA} and L_{DG} the channel length, W_{ch} and $T_{\mathrm{ch}} = 2\,R$ the channel width and thickness, R the channel radius and T_{ox} is the oxide thickness.

Table 3.1: GAA and DG Capacitors

Capacitor	**GAA**	**DG**
$C_{\mathrm{s\|\|d}}$	$2\,\frac{\varepsilon_{\mathrm{ch}}\,\pi\,R^2}{L_{\mathrm{GAA}}/2}$	$2\,\frac{\varepsilon_{\mathrm{ch}}\,W_{\mathrm{ch}}\,T_{\mathrm{ch}}}{L_{\mathrm{DG}}/2}$
C_{ox}	$\frac{2\,\pi\,\varepsilon_{\mathrm{ox}}}{\ln\left(1+\frac{T_{\mathrm{ox}}}{R}\right)}\,L_{\mathrm{GAA}}$	$\frac{2\,\varepsilon_{\mathrm{ox}}\,W_{\mathrm{ch}}}{T_{\mathrm{ox}}}\,L_{\mathrm{DG}}$

Using these equations in (3.5) results in

$$L_{\mathrm{DG}} = \sqrt{2}\sqrt{\frac{T_{\mathrm{ox}}/R}{\ln\left(1+T_{\mathrm{ox}}/R\right)}}\,L_{\mathrm{GAA}}. \tag{3.6}$$

Applying the conversion factor from (3.6) to the channel length in TCAD simulations of a DG transistor we realize that, with exception of Φ_{C}, the remaining variables (Φ_{S}, S_{sth}, DIBL) do not reflect the values of a GAA transistor as we wish. This is not quite strange, as the charges are distributed in the channel and thus the introduced parallel plate capacitors are only a simple assumption. Nevertheless, the charges are in equilibrium mainly located along the channel center, so that the conversion factor from (3.6) is applicable for Φ_{C}.

As already mentioned the capacitor model does not distinguish between center and surface potentials. This limitation can be circumvented by solving the Laplace equation. With the assumption of [16] that the electrostatic potential along the channel thickens is sinusoidal in Cartesian and Bessel function in cylindrical coordinates, we obtain for the channel/oxide interface the constant conversion factor 1.53 (and for the channel center $\sqrt{2}$) [13]. In combination with (3.6) the conversion factor for the surface results in

$$L_{\mathrm{DG}}^{\mathrm{S}} = 1.53 \sqrt{\frac{T_{\mathrm{ox}}/R}{\ln\left(1 + T_{\mathrm{ox}}/R\right)}}\, L_{\mathrm{GAA}}^{\mathrm{S}}. \tag{3.7}$$

Since this equivalent length concept is only interested in equalizing the barrier height, the shape of the electrostatic potential along the channel does not have to be exactly the same. Therefore, the conversion factors from (3.6) and (3.7) to the channel length should be used with caution and apply mainly at the potential barrier in the subthreshold region for intrinsic or lightly doped channels. Having this in mind, determining the subthreshold swing and DIBL is possible.

3.3 Transferring the Long-Channel DG Current Model to Long-Channel GAA FETs

In this section, we derive a charge-based current model for long-channel GAA FETs based on the method from [17] for long-channel symmetric DG FETs. The SCEs will be included in the next Section 3.4 by calculating the charges from a 2-D DG potential model modified for GAA FETs.

First, we use the one-dimensional (1-D) DG potential distribution through the channel thickness as the GAA solution, since we want to determine a DG FET with a channel length which results for this device in approximately the same potentials Φ_{C} and Φ_{S} as in the GAA device

$$[17] \rightarrow \text{DG:}\;\; \Phi\left(x\right) = \Phi_{\mathrm{C}} - 2\,V_{\mathrm{th}}\,\ln\left(\cos\left(\xi\,x\right)\right) \tag{3.8}$$

$$(\mathrm{x}\rightarrow\mathrm{r})\;\text{GAA:}\;\; \Phi\left(r\right) \approx \Phi_{\mathrm{C}} - 2\,V_{\mathrm{th}}\,\ln\left(\cos\left(\xi\,r\right)\right) \tag{3.9}$$

with

$$\xi = \sqrt{\frac{q\,n_{\mathrm{C}}}{2\,\varepsilon_{\mathrm{ch}}\,V_{\mathrm{th}}}} \tag{3.10}$$

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and

$$n_{\mathrm{C}} = n_{\mathrm{i}} \, \exp\left(\Phi_{\mathrm{C}}/V_{\mathrm{th}}\right). \tag{3.11}$$

In order to use (3.9) in the cylindrical 1-D Poisson equation, we have to consider that this is only possible if the channel length is modified. In the end of the last section, we already mentioned that we obtained for the channel center the constant conversion factor $z_{\mathrm{DG}} \approx \sqrt{2}\, z_{\mathrm{GAA}}$ in the direction of the channel length. Starting from the 2-D Laplace equation for DG and GAA FETs

$$\text{DG:} \quad \frac{\partial^2 \Phi}{\partial x^2} + \frac{\partial^2 \Phi}{\partial z_{\mathrm{DG}}^2} = 0 \tag{3.12}$$

$$\text{GAA:} \quad \frac{1}{r}\frac{\partial}{\partial r}\left(r\,\frac{\partial \Phi}{\partial r}\right) + \frac{\partial^2 \Phi}{\partial z_{\mathrm{GAA}}^2} = 0 \tag{3.13}$$

we get following expression by substituting the differential ∂z_{DG} with $\sqrt{2}\,\partial z_{\mathrm{GAA}}$:

$$\frac{\partial^2 \Phi}{\partial x^2} = -\frac{\partial^2 \Phi}{\partial z_{\mathrm{DG}}^2} \approx -\frac{1}{2}\,\frac{\partial^2 \Phi}{\partial z_{\mathrm{GAA}}^2} = \frac{1}{2}\,\frac{1}{r}\,\frac{\partial}{\partial r}\left(r\,\frac{\partial \Phi}{\partial r}\right). \tag{3.14}$$

Using the relations from (3.14) for the 1-D Poisson equation we obtain an equivalent radial electron density $n_{\mathrm{eq}}(r)$.

$$\frac{q}{\varepsilon_{\mathrm{ch}}}\, n(x) = \frac{\partial^2 \Phi}{\partial x^2} \approx \frac{1}{2}\,\frac{1}{r}\,\frac{\partial}{\partial r}\left(r\,\frac{\partial \Phi}{\partial r}\right) = \frac{q}{\varepsilon_{\mathrm{ch}}}\, n_{\mathrm{eq}}(r). \tag{3.15}$$

Applying (3.9) in (3.15) gives the equivalent electron density for GAA FETs as follows:

$$\frac{1}{2}\,\frac{1}{r}\,\frac{\partial}{\partial r}\left(r\,\frac{\partial \Phi(r)}{\partial r}\right) = \frac{q}{\varepsilon_{\mathrm{ch}}}\,\underbrace{\frac{1}{2}\left(\frac{n_{\mathrm{C}} \tan(\xi \cdot r)}{\xi\, r} + \frac{n_{\mathrm{C}}}{\cos^2(\xi\, r)}\right)}_{n_{\mathrm{eq}}(r)}. \tag{3.16}$$

The 2-D cylindrical total inversion charge can be expressed as

$$Q_{\mathrm{i,GAA}} = 2\,\pi\, q \int_0^R n_{\mathrm{eq}}(r)\; r\, dr = \pi\, R\, \underbrace{q\, n_{\mathrm{C}}\, \frac{\tan(\xi\, R)}{\xi}}_{\frac{Q_{\mathrm{i,DG}}}{2}} \tag{3.17}$$

which is $\pi\, R$ times half of the 1-D total inversion charge of a DG FET ($Q_{\mathrm{i,DG}}$) from [17]. Considering this and the fact that GAA and DG capacitors per gate length differ

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in size, the rest of the derivation is identical to the one in [17]. In combination with the Pao-Sah model [18] we obtain the following equation (3.18) for the drain current:

$$I_{\mathrm{ds}} = \frac{\mu}{L_{\mathrm{GAA}}} \left[V_{\mathrm{th}} \left(Q_{\mathrm{i,s}} - Q_{\mathrm{i,d}} \right) + \frac{\left(Q_{\mathrm{i,s}}^2 - Q_{\mathrm{i,d}}^2 \right)}{2\, C'_{\mathrm{ox}}} \right] \tag{3.18}$$

where μ is the electron mobility and C'_{ox} is the cylindrical capacitor per gate length. $Q_{\mathrm{i,s}}$ represents the 2-D cylindrical total inversion charge at the source end and is equal to $Q_{\mathrm{i,GAA}}$ for long-channel devices. $Q_{\mathrm{i,d}}$ is the mobile charge density at the drain end.

3.4 GAA Inversion Charge and Adaptation to the Current Model.

To include SCEs into the derived current equation in (3.18), the inversion charge is determined by using the converted electrostatics from any analytic DG potential model, e.g., [19]. For our DG compact model from [20] the validity of the potential model in the subthreshold regime is sufficient. To adapt the model to GAA devices, the inversion charge ($Q_{\mathrm{i,fb}}$) is calculated for a gate-source bias at the flatband voltage (V_{fb}). $Q_{\mathrm{i,fb}}$ is determined by integrating over the density of free electrons within the channel cross section at the virtual cathode at position z_{m}. Assuming a parabolic potential

$$\Phi\left(r,z_{\mathrm{m}}\right) = \Phi_{\mathrm{C}}\left(z_{\mathrm{m}}\right) - \frac{r^2}{R^2}\left(\Phi_{\mathrm{C}}\left(z_{\mathrm{m}}\right) - \Phi_{\mathrm{S}}\left(z_{\mathrm{m}}\right)\right) \tag{3.19}$$

we integrate in polar coordinates with $dA = r\, dr\, d\phi$

$$\begin{aligned} Q_{\mathrm{i,fb}} &= q \int_A n_{\mathrm{i}}\, e^{\frac{\Phi(r,z_{\mathrm{m}})}{V_{\mathrm{th}}}}\, dA \\ &= q \int_0^{2\pi} \int_0^R n_{\mathrm{i}}\, e^{\frac{\Phi_{\mathrm{C}} - \frac{r^2}{R^2}(\Phi_{\mathrm{C}} - \Phi_{\mathrm{S}})}{V_{\mathrm{th}}}}\, r\, dr\, d\phi \\ &= \frac{q\, \pi\, V_{\mathrm{th}}\, n_{\mathrm{i}}\, R^2}{\Phi_{\mathrm{C}}\left(z_{\mathrm{m}}\right) - \Phi_{\mathrm{S}}\left(z_{\mathrm{m}}\right)} \left(e^{\frac{\Phi_{\mathrm{C}}(z_{\mathrm{m}})}{V_{\mathrm{th}}}} - e^{\frac{\Phi_{\mathrm{S}}(z_{\mathrm{m}})}{V_{\mathrm{th}}}} \right). \end{aligned} \tag{3.20}$$

The inversion charge for higher gate biases and the transition to above threshold region is described in [13]. With following expression, we obtain the mobile charge density $Q_{\mathrm{i,s}}$ at the source end for any V_{gs}:

$$Q_{\mathrm{i,s}}\left(V_{\mathrm{gs}}\right) = \alpha\, C'_{\mathrm{ox}}\, V_{\mathrm{th}} \times W_0 \left\{ \frac{Q_{\mathrm{i,fb}}}{\alpha\, C'_{\mathrm{ox}}\, V_{\mathrm{th}}} \exp\left(\frac{C'_{\mathrm{ox}}\left(V_{\mathrm{gs}} - V_{\mathrm{fb}}\right) + Q_{\mathrm{i,fb}}}{\alpha\, C'_{\mathrm{ox}}\, V_{\mathrm{th}}} \right) \right\}, \tag{3.21}$$

where W_0 is the principal branch of the Lambert W function and α is the ratio between the degraded S_{sth} and the ideal swing (e.g. 59.5 mV per decade at T = 300 K). For $V_{\mathrm{gs}} = V_{\mathrm{fb}}$ the charge density becomes $Q_{\mathrm{i,s}} = Q_{\mathrm{i,fb}}$. In [14] a universal expression of the charge density $Q_{\mathrm{i,d}}$ is given for all operation regimes as

$$Q_{\mathrm{i,d}} = Q_{\mathrm{i,s}} - C'_{\mathrm{ox}}\,\tilde{V}_{\mathrm{dss}} \tag{3.22}$$

where the drain voltage $\tilde{V}_{\mathrm{dss}}\,(V_{\mathrm{ds}},V_{\mathrm{dsat}})$ is smoothly limited by the saturation voltage $V_{\mathrm{dsat}}\,(V_{\mathrm{T}})$. The use of smoothing functions provides a smooth transition from weak to strong inversion at the threshold voltage V_{T}, where the device is in saturation mode. The smoothness is also ensured for the transconductance g_{m} and the channel conductance g_{ds}. Both charge densities $Q_{\mathrm{i,s}}$ and $Q_{\mathrm{i,d}}$ are used in equation (3.18).

3.5 Quantum Confinement

MG transistors are thought to be the most promising among various MOS devices due to their better gate control and hence, larger immunity to SCEs. By migrating into the nanometer regime device designers have to consider not only SCEs but also thin-channel effects (TCEs) such as the widely discussed impact of QC. The critical channel thickness T_{ch} and channel width W_{ch} below which QC effects appear are declared to be 10 nm for DG FETs [21–24] and assumed to be the same in GAA FETs [25, 26]. The influence of channel width and thickness has been extensively discussed and successfully modeled in recent scientific work on nanosheet FETs [27]. The nonideal conditions for the subband energies based on an ideal 1-D particle-in-a-box model with infinite boundaries are circumvented by introducing empirically determined fitting parameters. The model works for a certain range of aspect ratio of nanosheet FETs, but cannot simply be extended to a comparison of different MG configurations.

In this section, we investigate the role and compare the influence of QC in the direction normal to the silicon/oxide interface on the current in MOSFETs with different MG configurations and relate them to each other. In detail, we focus on the energetic distance ΔE^{QC} of the first subband from the conduction band edge. We consider the quantum effects in DG, quadratic quadruple-gate (QG) and GAA transistors by assuming a 2-D infinite potential well in confinement direction. In [28] the 2-D, time-independent, free-particle Schrödinger equation, in the relevant Cartesian or cylindrical

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coordinates has been solved, so that the following smallest energy levels appear:

$$\text{DG:}\ \Delta E_{\text{DG}}^{\text{QC}} = \frac{\hbar^2}{2\, m_{\text{eff}}\, T_{\text{ch}}^2}\, \pi^2 \tag{3.23}$$

$$\text{QG:}\ \Delta E_{\text{QG}}^{\text{QC}} = \frac{\hbar^2}{2\, m_{\text{eff}}\, T_{\text{ch}}^2}\, 2\,\pi^2 \tag{3.24}$$

$$\text{GAA:}\ \Delta E_{\text{GAA}}^{\text{QC}} = \frac{\hbar^2}{2\, m_{\text{eff}}\, T_{\text{ch}}^2}\, 4 \cdot 2.4048^2 \tag{3.25}$$

where $\hbar$ is the reduced Planck constant and m_{eff} is the effective electron mass. To achieve the same quantum mechanical influence, the parameters ΔE^{QC} are set equal and resolved according to their radii as follows:

$$\Delta E_{\text{DG}}^{\text{QC}} = \Delta E_{\text{GAA}}^{\text{QC}} \leftrightarrow T_{\text{ch}}^{\text{GAA}} = 1.53\, T_{\text{ch}}^{\text{DG}} \tag{3.26}$$

$$\Delta E_{\text{DG}}^{\text{QC}} = \Delta E_{\text{QG}}^{\text{QC}} \leftrightarrow T_{\text{ch}}^{\text{QG}} = \sqrt{2}\, T_{\text{ch}}^{\text{DG}}. \tag{3.27}$$

Both (3.26) and (3.27) predict that the influence of QC increases significantly with the increasing number of gates around the channel and with their shrinking distance from channel center. Hence, the largest QC effect occurs in cylindrical GAA transistors. So, it has to be weighed up, what is preferred more, increase the device performance by more gates and thus less SCEs or weaken it simultaneously because of stronger quantization. Furthermore, it can be concluded that the critical channel thickness for GAA transistors, below which QC effects cannot be neglected, is 15 nm instead of 10 nm.

QC is implemented at two places in our modified DG compact model. A quasi classical implementation is done by reducing the intrinsic charge carrier concentration n_{i} in (3.20) due to the widening of the bandgap E_{bg}. For simplicity, the same ΔE^{QC} has been assumed for conduction and valence band. Since n_{i} is exponentially related to the bandgap as

$$n_{\text{i}} \propto \exp\left(-\frac{E_{\text{bg}}}{2\, k_{\text{B}}\, T}\right) \tag{3.28}$$

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the effective intrinsic charge carrier concentration $n_{\mathrm{i,eff}}$ for GAA FETs is given as

$$\begin{aligned} n_{\mathrm{i,eff}} &\propto \exp\left(-\frac{E_{\mathrm{bg}} + 2\,\Delta E_{\mathrm{GAA}}^{\mathrm{QC}}}{2\,k_{\mathrm{B}}\,T}\right) \\ &\propto \exp\left(-\frac{E_{\mathrm{bg}}}{2\,k_{\mathrm{B}}\,T}\right)\,\exp\left(-\frac{\Delta E_{\mathrm{GAA}}^{\mathrm{QC}}}{k_{\mathrm{B}}\,T}\right) \\ n_{\mathrm{i,eff}} &= n_{\mathrm{i}}\,\exp\left(-\frac{\Delta E_{\mathrm{GAA}}^{\mathrm{QC}}}{k_{\mathrm{B}}\,T}\right). \end{aligned} \tag{3.29}$$

Secondly, we know from various publications that QC increases the threshold voltage [23, 24]. This can be explained by the fact that with a larger bandgap the potential barrier becomes larger. Thus, the inversion potential Φ_{i} increases by $\Delta E^{\mathrm{QC}}/q$. The impact of QC on V_{T} can be given by the relationship that a change in gate potential with respect to changes in surface potential is equal to the change in threshold voltage with respect to the changes in bandgap due to QC. Thus, the following applies in general to the threshold voltage shift:

$$\Delta V_{\mathrm{T}}^{\mathrm{QC}} = \frac{dV_{\mathrm{gs}}}{d\Phi_{\mathrm{S}}}\Delta E^{\mathrm{QC}}/q. \tag{3.30}$$

The differential $dV_{\mathrm{gs}}/d\Phi_{\mathrm{S}}$ is given by (3.4) with parameter η. In analogy to [20], we obtained V_{T} by linear extrapolating Φ_{S} in the subthreshold region to an inversion potential Φ_{i}, which is used as a fitting parameter.

It should be noted that the impact of QC on the mobility has been neglected in this work. For simplicity, the mobility model we used in (3.18) corresponds to the one in [14] and includes the perpendicular gate electric field and velocity saturation effects. Nevertheless, a more sophisticated model as proposed in [29] could easily be implemented in (3.18).

3.6 Results and Discussion

To determine the impact of the confined electron carrier density on the quasi-Fermi level, we need to consider several valleys in the band structure instead of the single-valley representation. Quantization effects are implemented in Synopsys TCAD Sentaurus simulations with the connection to an external parabolic 2-D Schrödinger solver, which is the physically most sophisticated model. Assuming parabolic dispersion, the 4 L-valleys

and the Γ-valley are modeled using the ConstantEllipsoid valley Model. For a more detailed treatment of band dispersion including nonparabolicity and warping the 3 X-valleys in the direction of the three main axes are modeled based on the 2kpEllipsoid valley model. The quantum-mechanical carrier density correction is performed on several 2-D slices perpendicular to the channel direction and interpolated to the volume enclosed by the slices.

For model verification, we converted the channel length in the analytical potential model [14] of a DG transistor for center and surface with the conversion factors from (3.6) and (3.7) and obtained equivalent GAA center and surface potentials Φ_C and Φ_S. The analytic expressions for DIBL and S_sth are given in [13]. They are extracted from the inversion charge, described in Section 3.4, and from simulation data in the subthreshold regime close to V_fb at two different drain or, respectively gate biases.

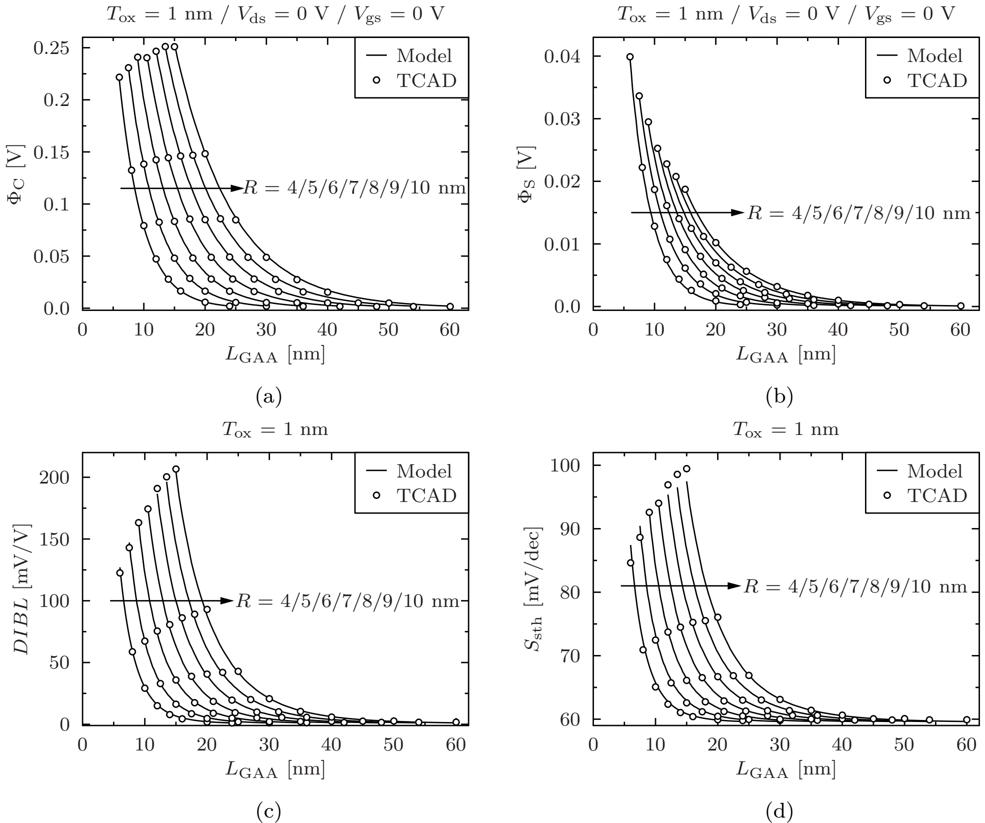

Figure 3.2: Comparison of compact model (lines) with TCAD simulations (symbols) of (a) center, (b) surface potential, (c) DIBL, and (d) subthreshold swing as a function of L_GAA with various channel radius [13].

In Figure 3.2, Φ_{C}, Φ_{S}, DIBL and S_{sth} with different channel length and radii (intrinsic channel and HfO_2 as gate oxide material) are compared with TCAD simulation data of a cylindrical nanowire (NW) FET. We see an excellent agreement of the GAA electrostatics to our equivalent DG compact model. A further validation of the model was already carried out in [13] by comparing the corresponding transfer and output characteristics of one chosen device with TCAD data showing SCEs.

In Figure 3.3, we see the change in effective intrinsic density and electron current density within the channel from classical physics to that with activated QC of an ultrathin GAA FET. Both show that the charge and current distribution is changing dramatically due to the wave characteristic of electrons in a quantum-mechanical approach. The boundary condition for the wave function at the channel/oxide interface is near to zero. Thus, the probability to locate there an electron goes towards zero as well. As a consequence, the QC forces the charge to the center of the channel. Even in the ON-state, where the potential barrier at the channel surface is smaller than at the center, the inversion channel is formed along the channel center. This is due to the relatively higher density of states in this area.

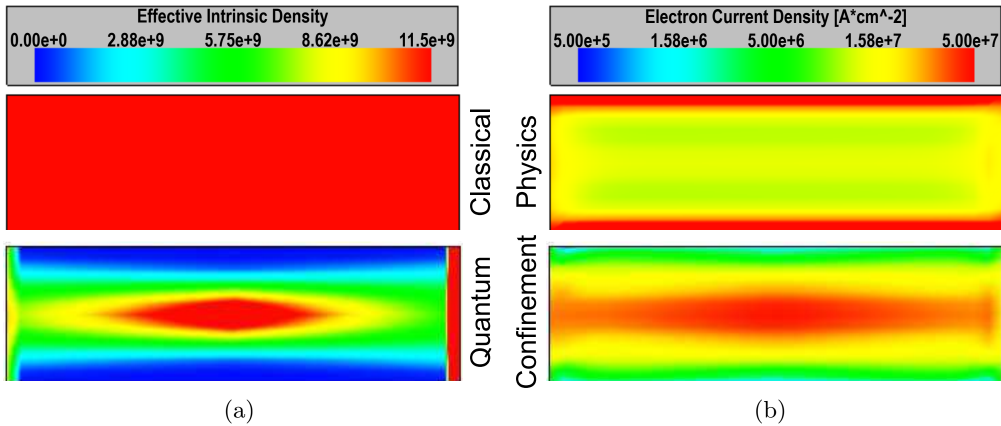

Figure 3.3: (a) Comparison of the effective intrinsic density of free electrons and (b) electron current density inside of the channel between classical physics and activated QC for $R = 3$ nm, $L_{\mathrm{GAA}} = 20$ nm, $T_{\mathrm{ox}} = 1$ nm, $V_{\mathrm{gs}} = 1$ V and $V_{\mathrm{ds}} = 0.1$ V.

In Figure 3.4, we compare the impact of QC on the transfer characteristics between GAA and DG simulations. First of all, the chosen channel length is long enough to avoid SCE and to focus only on the quantum-mechanical impact on the current. With this plot, we verify the accuracy of the conversion factor in (3.26) for the channel thickness between GAA and DG FETs and proof simultaneously that current reduction by QC

occurs already for larger channel thickness in MG transistors. If the channel thickness is equal to 6 nm, then the extent of current reduction and threshold voltage increase for GAA transistors is significantly greater. The classical current is divided by 12.8 (GAA) compared to 2.8 (DG). If the channel thickness of the same transistor is larger by a factor of 1.53, then the effect is comparable to that of DG FETs without increasing the channel thickness. Now the classical subthreshold current is divided by 2.9 (GAA), which is very close to 2.8 (DG).

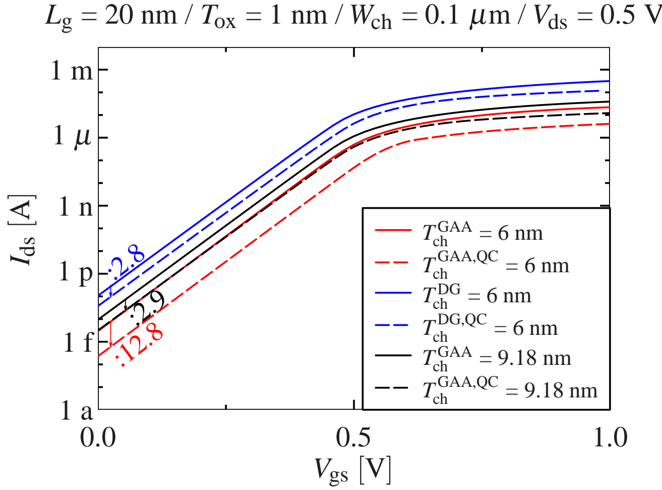

Figure 3.4: Comparison of the transfer characteristics between GAA and DG simulations with classical (solid lines) or with activated QC (dashed lines).

Fig 3.5 shows a cross-sectional view of a typical Ω-gate NW N-MOSFET [30]. We performed statistical I_{ds}-V_{gs} and I_{ds}-V_{ds} measurements to extract in first place short-channel parameters as S_{sth} and DIBL and to compare with our model. The measured devices have a NW height of H_{NW} = 10 nm and a (mask) top width of W_{top} = 10 nm. The (mask) gate length varies from long L_g = 200 nm down to very short L_g = 10 nm. The devices have a high-κ/metal gate stack (HfSiON/TiN) with an equivalent oxide thickness (EOT) of T_{ox} = 1.2 nm. The actual width and length of the gate is usually longer than the mask dimensions. The average values corresponding to 14 optical measurements on different dies of the wafer are W_{top} = 16.5 nm and L_g = 14.1 nm for the shortest gate length among the devices. For modeling purposes of transistors with other gate length, we assume an average gate length that is 4.1 nm longer than the mask length.

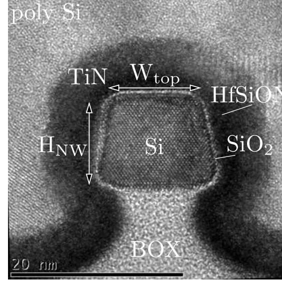

Figure 3.5: TEM cross section of a silicon on insulator (SOI) Ω-gate NW N-MOSFET.

To illustrate the dispersion between mask and actual dimensions, Figure 3.6 shows the strong variation of the transfer characteristics between different dies but same short (mask) gate length L_g = 15 nm. These variations are mainly due to the steps of resist trimming used to shorter gate and active patterns in this process.

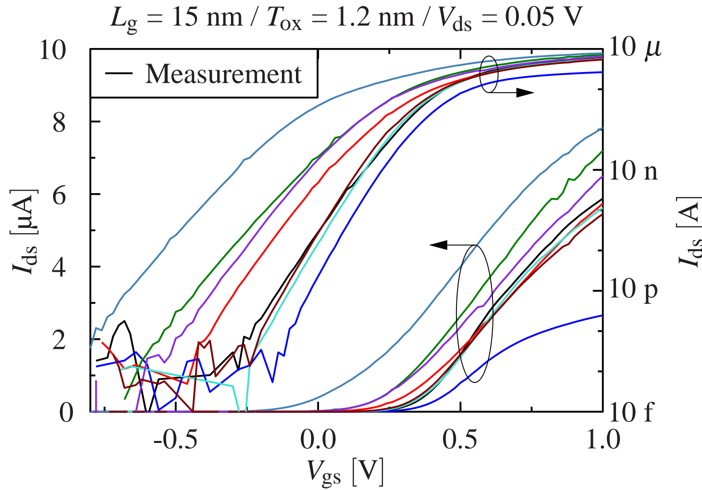

Figure 3.6: Variation of the transfer characteristics between different dies but same transistor geometry.

In Figure 3.7, our model is compared in log scale with the extracted mean value of DIBL and subthreshold swing versus the mean gate length ($L_{GAA} = L_g + 4.1$ nm) within three standard deviations represented by the error bars. Assuming an additional bottom gate, the corresponding mean channel thickness of a cylindrical NW having the same circumference ($T_{ch}\,\pi = 2\,(H_{NW} + W_{top})$) would be approximately T_{ch} = 2 (10 nm + 16.5 nm)/$\pi \approx$ 17 nm. A worse gate control due to the missing bottom gate allows us

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to choose a slightly larger value for T_{ch} without determining new equivalent conversion rules for the channel length of an Ω-gate transistor. Apart from the shortest (mask) gate length, $T_{\mathrm{ch}} = 20$ nm have proved to be suitable.

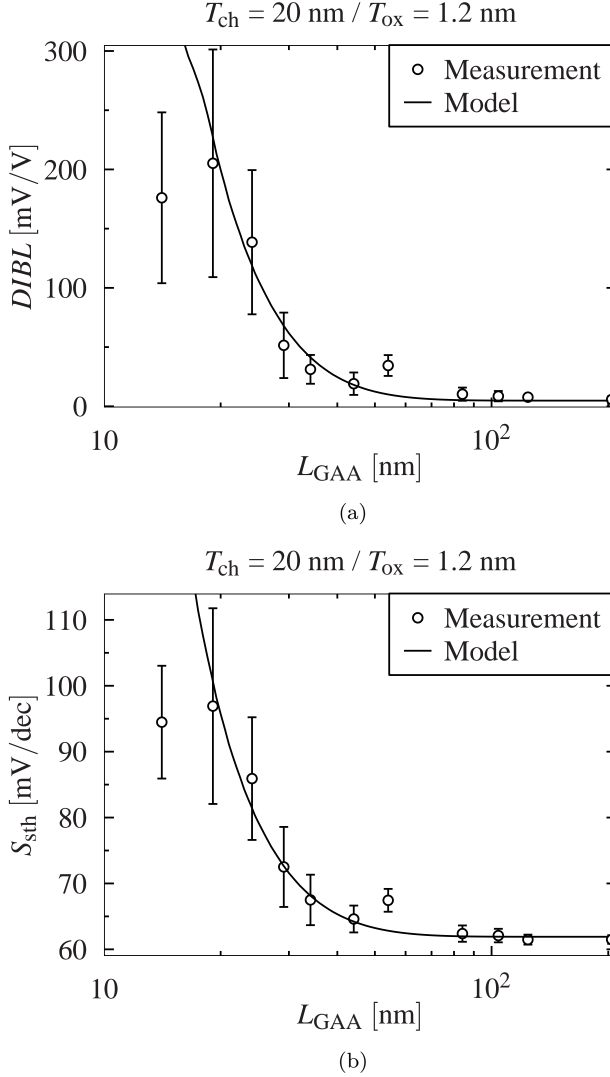
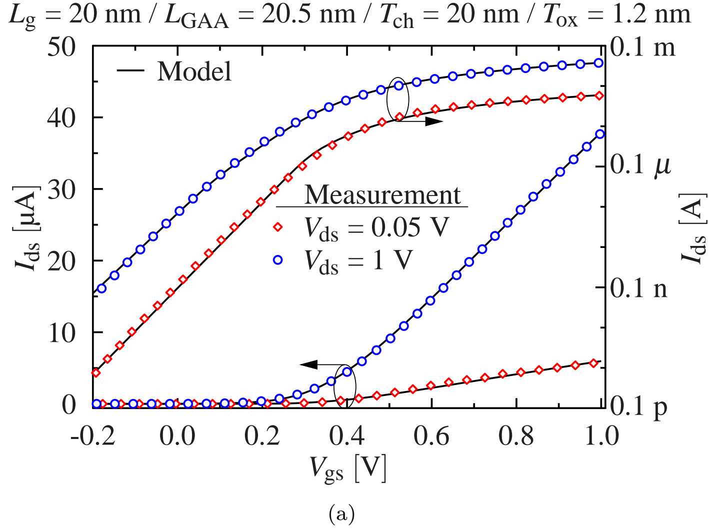


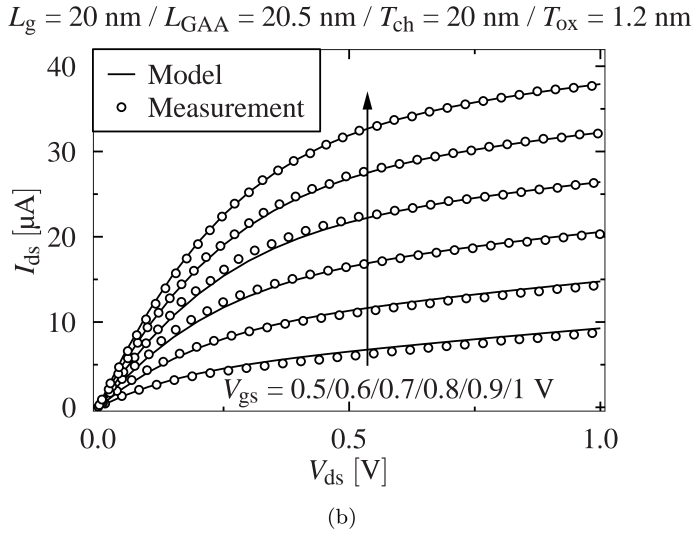
Figure 3.7: (a) Comparison of DIBL and (b) S_{sth} between measurement data (symbols) and compact model (lines).

In Figure 3.8, for a chosen device showing pronounced SCE ($S_{\mathrm{sth}} = 89$ mV/dec, DIBL = 176 mV/V) we compare the transfer and output characteristics and in Figure

3.9 the transconductance and the channel conductance with our compact model. By using $T_{ch} = 20$ nm as the mean diameter of the NWs, we can determine an effective channel length for each transistor and consider at the same time the random dopant penetration from source and drain side to the channel. In case of our chosen device this length is 20.5 nm and hence, just 0.5 nm longer then the mask length.

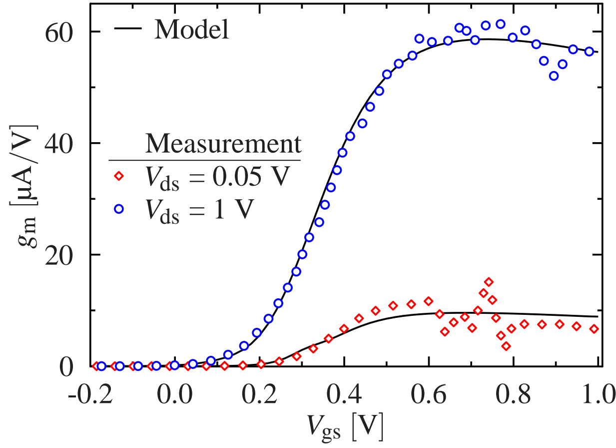


(a)

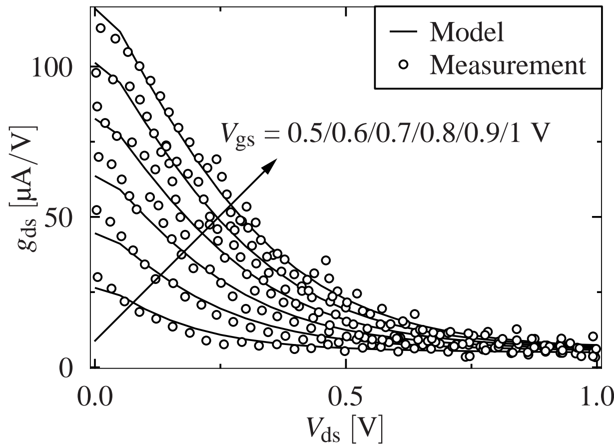


(b)

Figure 3.8: (a) Comparison of compact model (lines) and measurement data (symbols) of transfer characteristics, and (b) output characteristics of a short-channel Ω-gate NW N-MOSFET.



(a)



(b)

Figure 3.9: (a) Comparison of compact model (lines) and measurement data (symbols) of transconductance, and (b) channel conductance of a short-channel Ω-gate NW N-MOSFET.

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3.7 Conclusion

We confirmed the transferability of electrostatics including SCEs from GAA to DG FETs with the equivalent channel length concept and demonstrated its applicability to omega-gate NW N-MOSFETs, since cylindrical NW FETs with SCE are rarely fabricated so far. We extended our modified DG model by the effect of circular QC and clearly showed by simulation that a full surrounding of the channel with gate material results in a higher critical channel thickness and hence, an earlier onset of the undesired quantum effects. Furthermore, it was shown that in the ON-state due to QC, the inversion channel does not form at the surface as usual, but along the center of the channel. In addition, the current strength decreases significantly due to lower density of states and effectively higher bandgap. We also verified our model by very good reflection of the SCE parameters from statistical measurements down to a (mask) gate length of 15 nm and showed perfect modeling results of I-V characteristics on one selected device.

Acknowledgment

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CHAPTER 4

Direct Source-to-Drain Tunneling Current in Ultrashort-Channel DG MOSFETs by Wavelet Transform

In this work, a new approach to determine the effect of direct source-to-drain tunneling (DSDT) on two-dimensional (2-D) double-gate (DG) MOSFETs is presented. The tunneling probability of electrons with different energy levels and tunneling distances through the potential barrier is calculated using harmonic wavelets and the results are compared to those calculated with the Wentzel-Kramers-Brillouin (WKB) method. Next, by having the tunneling probability the DSDT current is calculated and compared to TCAD simulations data, which are based on WKB model, and also to NanoMOS, a nonequilibrium Green's function (NEGF) 2-D simulator for DG devices. The difference between these methods and their impacts on the resulted DSDT as well as the subthreshold behavior are investigated. Furthermore, a first step towards compact modeling is made by approximating the tunneling current density.

4.1 Introduction

Due to decreasing device dimensions more and more short-channel effect (SCE) are superposing each other. Some of them only influence the subthreshold region, others the above threshold and again others both regions. The degradation of the subthreshold slope S_{sth} and the drain-induced barrier lowering (DIBL) are one of the most frequently discussed aspects of SCEs. Once the device dimensions reach the single-digit nanometer region, the quantum mechanical effects can usually no longer be ignored. Two different views are expressed regarding scalability due to quantum effects. On the one hand,

DSDT is considered as a limiting factor for channel length scaling, since it dominates the OFF-current when the channel length is 3 nm long, which means the ON/OFF ratio of the device is too low for meaningful applications [1, 2]. On the other hand, authors argue that quantum confinement will suppress DSDT, because one-dimensional (1-D) treatments are inadequate and overestimating tunneling [3]. This work focuses on DSDT and its influence on the aforementioned SCEs and neglects quantum confinement from gate to gate.

Figure 4.1 shows the geometry of the studied n-MOS DG transistor.

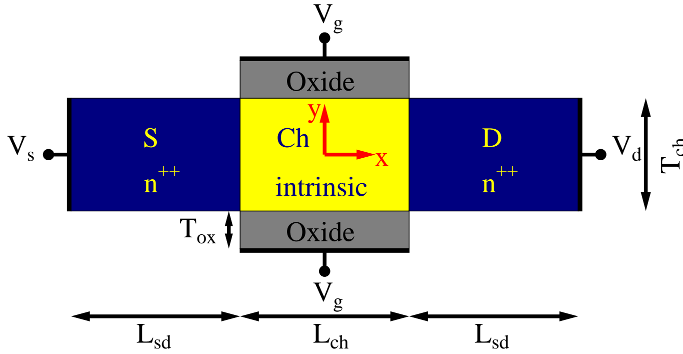

Figure 4.1: Sketch of the DG MOSFET under study. Source/Drain (S/D) regions are highly n-doped. The channel (Ch) is intrinsic and the gate oxide is a high-κ material.

In order to determine the tunneling coefficient of a wave function, it is necessary to solve the time-independent Schrödinger equation. There is no exact solution for potential forms as in the channel of a DG transistor (see Figure 4.2). The WKB and the wavelet methods are techniques to obtain approximated solutions for the time-independent Schrödinger equation in 1-D. The WKB approximation is one of the most frequently used methods, but its accuracy is doubtful, as it can only be applied if the potential varies “slowly”. In other words, the location dependent variation of the de-Broglie wavelength λ_{DB} of electrons must be significantly less than 1, which is not fulfilled at the classical turning points, at which the electron energy E_{x} and the potential energy $V(x)$ are equal and hence λ_{DB} becomes infinite as following [4]

$$\left|\frac{\lambda_{\mathrm{DB}}}{dx}\right| << 1 \qquad \text{with} \qquad \lambda_{\mathrm{DB}} = \frac{h}{2\,m_{\mathrm{e}}\left(V(x) - E_{\mathrm{x}}\right)}, \tag{4.1}$$

where h is the Planck constant and m_{e} the electron mass. The wavelet method is not as fast and easy to implement as the WKB method, but it does not have the mentioned

weak points and can therefore be used for various potential forms. It was successfully used, among others, to determine the tunneling coefficient for triangular barriers in metal-insulator-metal (MIM) stack [5] or to compare it with the exact solution of the Schrödinger equation for rectangular barriers [6].

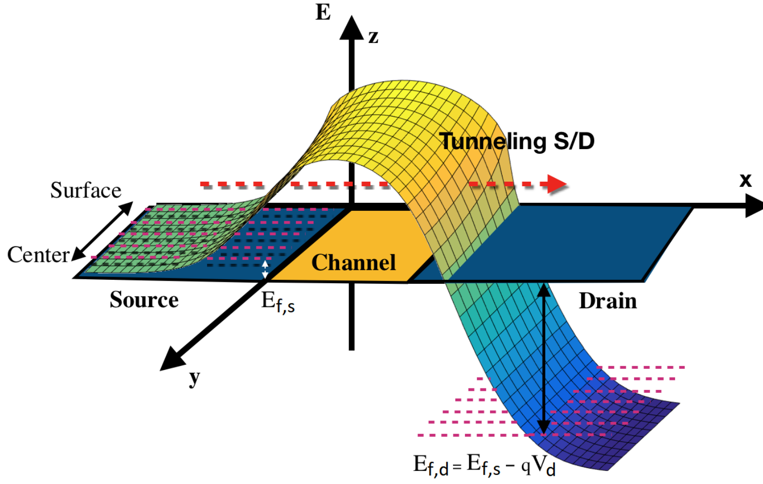

Figure 4.2: Illustration of DSDT: Half DG structure superposed with the conduction band edge E_{CB}.

4.2 Modeling Approach

The first step in determining the tunneling current is to determine the tunneling probabilities for each electron energy and each parallel slice in y-direction of the channel. The necessary formulas are introduced in the following subsection. For further details please refer to the references.

4.2.1 WKB-Based Model

According to the WKB method and its approximated solution to the 1-D Schrödinger equation, the tunneling probability in x-direction is given as [4]:

$$P_{\mathrm{t}} = \exp\left[-2\int_{x_{\mathrm{L}}}^{x_{\mathrm{R}}} k(x)\, dx\right] \tag{4.2}$$

with

$$k(x) = \sqrt{\frac{2\, m_{\text{eff}}\, \left(E_{\text{CB}}\,(x) - E_{\text{x}}\right)}{\hbar^2}}. \tag{4.3}$$

x_{L}, x_{R} are the classical turning points and their distance is the longest considered tunneling length for tunneling electrons with energy E_{x}. The wavenumber $k(x)$ is determined by the effective mass m_{eff} in tunneling direction and the reduced Planck constant $\hbar = h/2\pi$. The energy barrier $V\,(x)$ is equal to the conduction band edge $E_{\text{CB}}\,(x)$.

4.2.2 Wavelet-Based Model

To calculate the transmission coefficient it is necessary to know the wave function Ψ of the electron. Therefore, the Schrödinger equation must be solved here as well. In wavelet method, it is considered that the solution of the time independent Schrödinger equation is the Shannon wavelet.

$$\frac{d^2\Psi}{dx^2} - K(x)\,\Psi = 0 \qquad \text{with} \qquad K(x) = (k(x))^2 \tag{4.4}$$

The central point of this method is that by using Shannon wavelets the Schrödinger equation is solved approximately as rectangular potential for each electron energy separately, which is the time consuming part. For this purpose, the initially position-dependent wavenumber $k\,(x)$ is transformed into an equivalent but constant value k_{eq} [6].

$$K_{\text{eq}} = \frac{1}{2\,\pi} \int\limits_{-2\,\pi}^{2\,\pi} \hat{K}(\omega) d\omega \tag{4.5}$$

$$k_{\text{eq}} = \sqrt{K_{\text{eq}}} \tag{4.6}$$

$\hat{K}(\omega)$ is the Fourier transformation of $K(x)$ and the equivalent wavenumber k_{eq} is obtained by integrating this value over the period of -2π and 2π. The transmission coefficient is part of the calculated wave function outside the barrier and is used for further current calculation. Please refer to Chapter 5.3.2 for more details.

4.2.3 Tunneling Current Density

The net electron tunneling current density (J_{t}) along the x-axis is calculated with the TSU-ESAKI tunneling formula by integration in the energy domain with reference level $E_{\mathrm{CB}} = 0$ eV at the source end [7]

$$J_{\mathrm{t}}(y) = \frac{q\, m_{\mathrm{eff}}}{2\,\pi^2\,\hbar^3} \int_0^{E_{\mathrm{m}}} P_{\mathrm{t}}(E_{\mathrm{x}})\; N(E_{\mathrm{x}})\; dE_{\mathrm{x}}, \tag{4.7}$$

with q the elementary charge and $N(E_{\mathrm{x}})$ the supply function defined by [8], which is a description of the supply of charge carriers for tunneling:

$$N(E_{\mathrm{x}}) = \int_0^{\infty} \left(f_{\mathrm{s}}(E) - f_{\mathrm{d}}(E)\right) dE_{\rho} \tag{4.8}$$

Both, f_{s} and f_{d} describe the Fermi-Dirac distribution at the source/channel and channel/drain interface, respectively. The total energy is separated into transverse (E_{ρ}) and longitudinal parts (E_{x}). By integrating from the conduction band edge E_{CB} to infinity in transversal direction we obtain:

$$N(E_{\mathrm{x}}) = q\,V_{\mathrm{th}}\,\ln\left(\frac{1+\exp\left(-\frac{E_{\mathrm{x}}-E_{\mathrm{f,s}}}{q\,V_{\mathrm{th}}}\right)}{1+\exp\left(-\frac{E_{\mathrm{x}}-E_{\mathrm{f,d}}}{q\,V_{\mathrm{th}}}\right)}\right), \tag{4.9}$$

where V_{th} is the thermal voltage constant and $E_{\mathrm{f,s}}$ and $E_{\mathrm{f,d}}$ are the Fermi energies.

4.2.4 Tunneling Current

The calculation of $J_{\mathrm{t}}(y)$ must be done for each slice along the y-axis within the channel thickness (T_{ch}). An integration over the mesh size in y-direction and a final multiplication with the channel width (W_{ch}) gives the total tunneling current through the potential barrier.

$$I_{\mathrm{t}} = W_{\mathrm{ch}} \int_{-\frac{T_{\mathrm{ch}}}{2}}^{\frac{T_{\mathrm{ch}}}{2}} J_{\mathrm{t}}(y)\; dy \tag{4.10}$$

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4.2.5 Compacted Tunneling Current

A first step to make the model compact is performed by approximating the change of $J_{\mathrm{t}}(y)$ versus y from center (J_{C}) to surface (J_{S}) with a linear curve. The required area beneath this new curve is determined by a triangle and rectangle as it is shown in Figure 4.6. Multiplying this area with W_{ch} gives the compacted tunneling current as following:

$$I_{\mathrm{t}} \approx W_{\mathrm{ch}} \left[T_{\mathrm{ch}} \left(\frac{J_{\mathrm{C}} - J_{\mathrm{S}}}{2} \right) + T_{\mathrm{ch}}\, J_{\mathrm{S}} \right]. \tag{4.11}$$

4.3 Model Verification

$E_{\mathrm{CB}}(x{,}y)$ was extracted from TCAD Sentaurus simulation data [9] in order to verify the approach simultaneously with the WKB-based model for the tunneling probability. In order to claim that the wavelet method is better than the WKB approximation the results are not only compared to TCAD Sentaurus but also to NanoMOS [10], a nonequilibrium Green's function (NEGF) 2-D simulator for DG MOSFET devices with quantum transport model. The NEGF formalism is expected to give more accurate results compared to the WKB method. Thus, we assume that the new method will match the NEGF one. Both simulations are performed with the parameters listed in Table 4.1.

Table 4.1: TCAD Sentaurus and NanoMos simulation parameter set

Parameter	Value	Parameter	Value
L_{ch}	3-8 nm	N_{ch}	intrinsic
T_{ch}	2 nm	Device Material	Silicon
T_{ox}	1 nm	Oxide Material	$\mathrm{HfO_2}$
L_{sd}	10 nm	$N_{\mathrm{s/d}}$	10^{20} cm^{-3}
W_{ch}	1 μm	m_{eff}	0.26 m_{e}

In Figure 4.3 several information about the differences between WKB and wavelet method are given. For two different drain voltages ($V_{\mathrm{ds}} = 0.1/1$ V) and channel length ($L_{\mathrm{ch}} = 4/8$ nm), it shows the tunneling probability as a function of the electron energy in logarithmic and linear scale. It is obvious that for each electron energy the tunneling probability determined by the wavelet method is always smaller. Thus it can be expected that not only the tunneling current but also the subthreshold swing will be significantly smaller. The question arises as to what influence we expect on the classical DIBL, which

we can read from this graph at 100% tunneling probability. The graph in logarithmic scale shows that each electron energy has its own value for the DIBL. The reason for this quasi DIBL is that applying a drain voltage to short-channel transistors not only reduces the height of the potential barrier, but also makes the barrier thinner. This shortens the tunnel length and thus effectively increases the tunneling probability for each electron energy compared to smaller drain voltages. It should also be mentioned that the smaller the channel thickness T_{ch}, the smaller is the drain-induced barrier thinning (DIBT) effect [1]. In order to make a statement about where the quasi DIBL visible in the I-V characteristics can be read, its weighting in the energy scale must be taken into account.

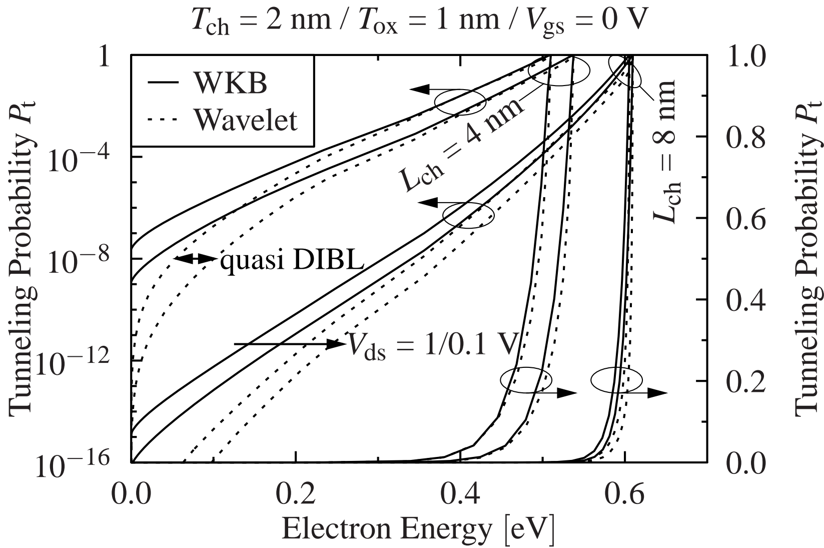

Figure 4.3: Tunneling probability vs. electron energy in linear and log scale for a short and relatively long-channel device.

The weighting is determined by multiplying the tunneling probability with the supply function according to equation (4.9). This is proportional to the first derivation of the tunneling current density, which we plot against the tunneling probability in Figure 4.4 for 4 nm channel length. As expected the values determined with the wavelet method are smaller than with the WKB method. The interesting aspect of this graph is that the electrons with a tunneling probability of about 10^{-5} respectively 10^{-6} make the largest contribution to the tunneling current because of the Fermi-Dirac distribution. Thus those are definitely not to be neglected. This graph together with Figure 4.3 shows that the quasi DIBL is only an average value and cannot be read exactly from the Figure 4.3.

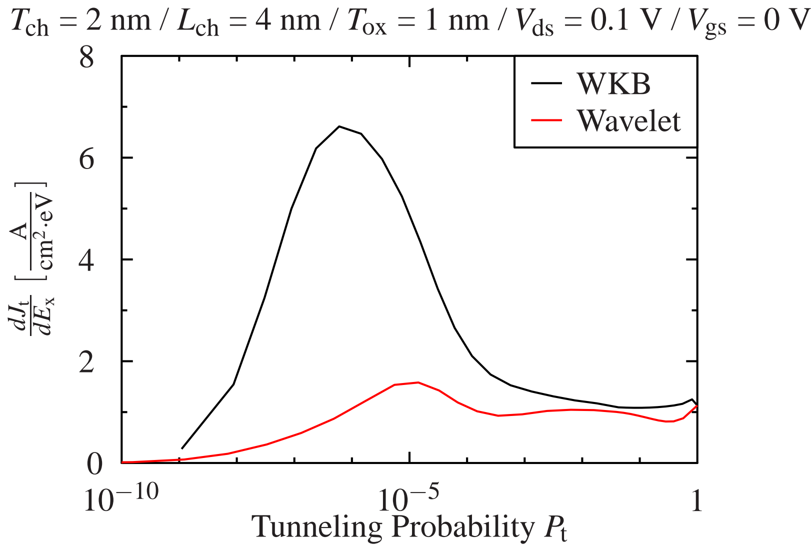

Figure 4.4: First derivation of the tunneling current density after electron energy vs. tunneling probability.

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Figure 4.5 shows the normalized first derivation of the tunneling current density vs. the tunneling probability for different channel lengths. As the channel length increases, the peak shifts to higher tunneling probabilities and thus to higher electron energies. An exception is the channel length with 4 nm. This represents the transition between both regions. A plot in the energy space would show an ascending order. A decisive factor for longer channels is the effective tunneling length, which is short enough only for electrons with higher energy due to the shape of the potential barrier. The current disappears as soon as the area under the curve disappears, which happens for channel lengths longer than 8 nm.

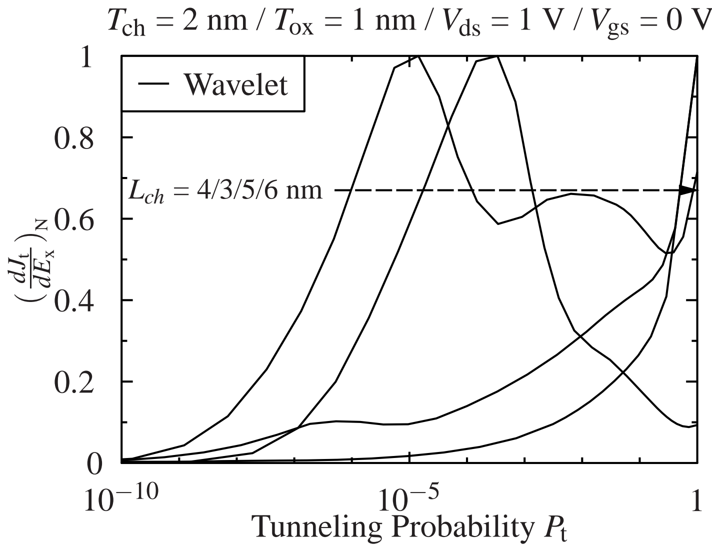

Figure 4.5: Normalized first derivation of the tunneling current density after electron energy vs. tunneling probability for different channel length.

Figure 4.6 compares the channel cross section of the normalized current density for two different bias conditions. It can be seen that the main part of the tunneling current flows through the center of the channel. The surface current is not negligible because it increases with the gate voltage. Similar to the linear approximation mentioned in 4.2.5, the current is determined by calculating the area beneath the curve of the current density J_{t}. With the linear approximation from center to surface we reduce the calculation time, hence only the surface and center current density is needed. This approach is a first step towards compact modeling (cm).

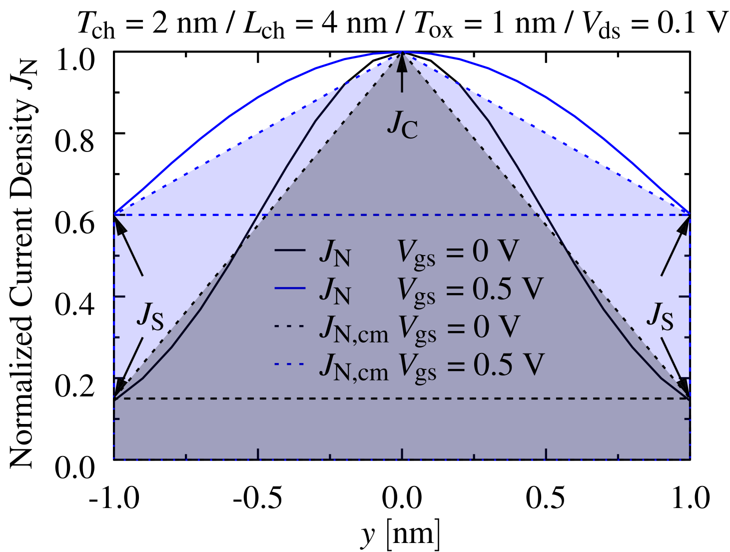

Figure 4.6: Channel cross section of the normalized current density for two different bias conditions and their approximation by a triangle and rectangle.

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Figure 4.7 compares the subthreshold transfer characteristics between wavelet- and WKB-based model with their compacted model for two different drain biases (V_{ds} = 0.1/1 V). As expected the WKB method overestimates for small gate biases the current compared to the wavelet method. A very good approximation of the current is achieved with the compacted model. This is shown as an example for a short-channel transistor with a length of 4 nm.

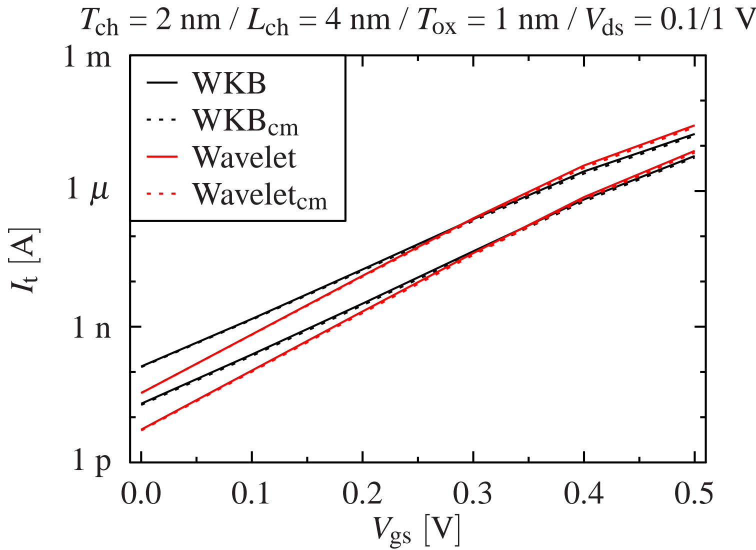
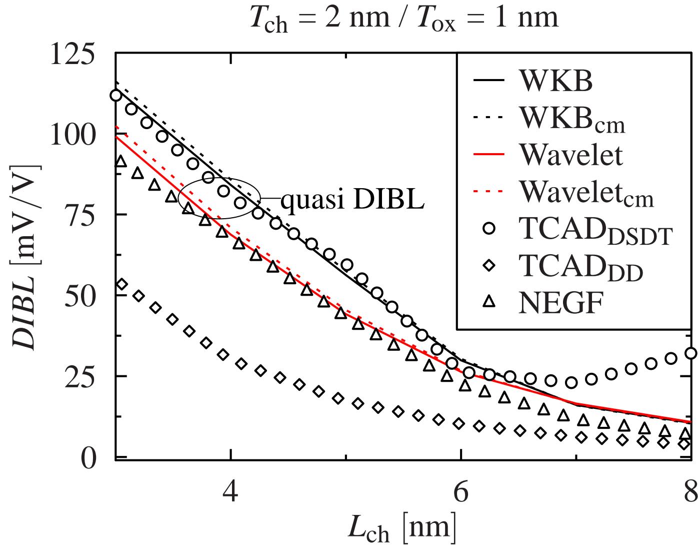
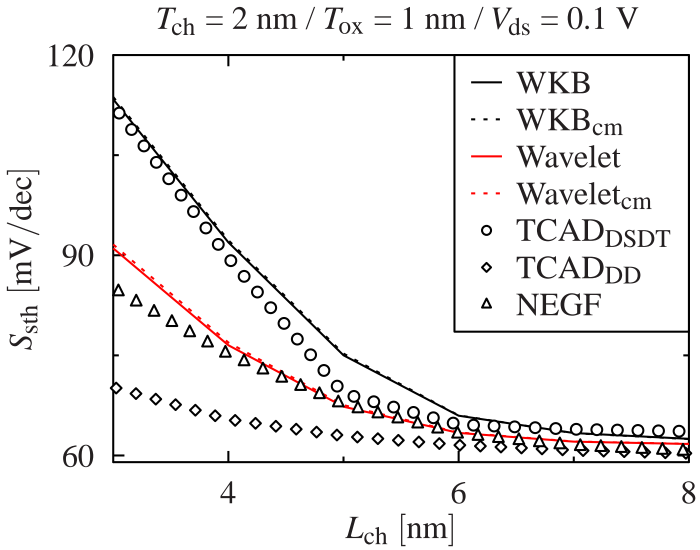


Figure 4.7: Comparison of the transfer characteristics between wavelet- and WKB-based model with their compacted model for two different V_{ds}.

In Figure 4.8(a) and 4.8(b) we see a very good agreement of DIBL and S_{sth} for different channel lengths between our wavelet method and NanoMOS simulation data (NEGF-based method). Both are between the results of TCAD simulation data with only drift-diffusion (DD) current and only DSDT current. At the same time we have verified that the used WKB method combined with the Tsu-Esaki formula gives similar results as that of TCAD Sentaurus, which uses a WKB-based model. Furthermore, the compacted models for different channel lengths also agree with the not approximated results.



(a)



(b)

Figure 4.8: Comparison of DIBL (a) and S_{sth} (b) between wavelet and WKB method, their compacted models, TCAD simulations with only DSDT or DD current and NEGF 2-D simulator with NanoMOS.

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4.4 Conclusion

In this work the wavelet/WKB method and the Tsu-Esaki formula were used to calculate the DSDT current in a ultrashort-channel DG MOSFET. The analysis has shown that the WKB method is overestimating the tunneling probability and thus also the current, DIBL and S_{sth}. It was clearly confirmed that the solutions with the wavelet method are much closer to the results of the NEGF method and therefore more accurate. It was also shown that it is sufficient to know the electrostatic behavior in the center and at the surface of the channel for an approximation of the DSDT. For full device modeling, an analytical potential solution as in [11] must be used.

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CHAPTER 5

Quasi-Compact Model of Direct Source-to-Drain Tunneling Current in Ultrashort-Channel Nanosheet MOSFETs by Wavelet Transform

We present an analytical approach for the calculation of direct source-to-drain tunneling (DSDT) probability of electrons in gate-all-around (GAA) silicon nanosheet (SiNS) MOSFETs. The used method is based on the wavelet transform and leads to a quasi-compact model (QCM) for the DSDT current of ultrashort-channel devices. Among them, we introduce a four-piece parabolic approximation method for the conduction band edge and present analytical expressions for the tunneling distances of electrons with different energy levels. The development of a QCM is achieved by limiting the number of interpolation points for the tunneling current density to seven specific electron energies, distributed around the energy level that makes the largest contribution to the tunneling current. A further simplification is achieved by the Gaussian approximation of the tunneling current density in transverse direction so that only the center and surface potentials (Φ_C and Φ_S) at the barrier are of interest for the modeling. For comparison, all those approximations are also implemented in the Wentzel-Kramers-Brillouin (WKB) approximation. Furthermore, the approach is verified by nonequilibrium Green's function (NEGF) simulation.

5.1 Introduction

The aggressive downscaling of device dimensions into the single-digit nanometer range makes it inevitable to consider quantum mechanical effects and their influences on

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the entire current characteristics [1–3]. Besides, quantum confinement (QC) in the transverse direction of thin body transistors and quantum mechanical tunneling effects in the direction of current transport play a significant role. In classical MOSFETs, direct source-to-drain tunneling (DSDT) rather has negative influences and should be avoided if possible. Mainly, it leads to a worse ON-OFF current ratio, a further slope degradation and a higher drain-induced barrier lowering (DIBL). These aspects must be considered as accurately as possible in compact modeling of devices with a channel length of less than 7 nm. Since an exact solution of the time-independent Schrödinger equation for the tunneling coefficient of a wave function is not given unless the potential barrier has a rectangular shape, approximate values are mostly determined with the widely used Wentzel-Kramers-Brillouin (WKB) method. The accuracy of this method is doubtful because for applicability of the WKB approximation the electrostatic potential has to vary "slowly" [4].

A recently published scientific work presents a compact model, in which the incorporation of DSDT with ballistic transport is mentioned for all operating regimes [5]. The analytic model based on the WKB approximation is tested against nonequilibrium Green's function (NEGF) simulation using SILVACO. Unfortunately, the modeling results presented do not agree well enough with the simulation results. The main reason is that the entire energy spectrum is covered with only one fixed parabolic approximation of the conduction band and there is no adjustment of the parabolic function for different electron energies. In addition, the channel lengths shown with 5 and 7 nm for only one drain bias of 0.6 V are not sufficient, considering that DSDT starts just below 7 nm. The main areas of influence such as slope degradation and DIBL are not discussed sufficiently.

In [6] we compare for double-gate (DG) FETs the results of DSDT current determined with the WKB method with those obtained with harmonic wavelets and with the simulation tool NanoMOS, a NEGF simulator for DG devices [7]. The good agreement between wavelet and the numerically complex but highly accurate NEGF-based method concludes that the WKB method is overestimating the tunneling probability and thus current, DIBL and subthreshold swing (S_{sth}). In this previous work we extracted the electrostatic potential from TCAD simulations and the whole approach was not ready in terms of development of a fully analytic calculation.

The approach in this work can be applied to any analytical potential model that reflects the center and surface electrostatics at the barrier of a silicon nanosheet (SiNS) FET.

The basis for calculating the tunneling current (I_{t}) in classical MOSFETs is to

determine the correct tunneling probability (P_{t}) of electrons with different energies through the potential barrier. For this we need a simple but accurate expression for the electrostatic potential through the device. In Section 5.2, we will first give a mathematical expression for the position of the barrier height in the channel, derived from an analytical potential solution. Then, we simplify this potential together with the source and drain extensions and present a four-piece parabolic and, hence, asymmetric approximation of the conduction band edge. On this basis, we give an energy-dependent analytical expression for the tunneling length (L_{t}).

As a next step in Section 5.3, we derive a term for the transmission coefficient: one for the WKB-based model and one for the wavelet-based model, which we have claimed as a better alternative. This is done by a single parabolic and hence symmetric approximation of the energy barrier between the classical turning points of each electron with kinetic energy smaller than the barrier height. This procedure is similar to the one in [8] for DSDT in III-V transistors. The main difference is that in this publication the potential is treated as a rectangular barrier, which is inaccurate for silicon-based ultrashort-channel devices with significantly higher effective mass.

Next, in Section 5.4, we will go through several approximation methods for the individual tunneling parameters and make the tunneling current density (J_{t}), which is given by a nonanalytically solvable integral, to a quasi-compact model (QCM). Furthermore, a Gaussian approximation of J_{t} in the transversal y-direction is introduced, and from this, an expression for the tunneling current (I_{t}) is derived. For simplicity and in the sense of compact modeling, we determine I_{t} and the corresponding S_{sth} only at the flatband voltage (V_{fb}). These initial values are used in a suitable exponential function to describe the increase of the tunneling current in the transfer characteristic. Furthermore, the rise of the tunneling current around the threshold voltage (V_{T}) is continuously braked and stopped and finally forced into a slightly decreasing trend with a proper fitting parameter.

In Section 5.5, we verify our QCM by comparison with nonapproximated solutions as well as with NEGF simulation data and give a conclusion in Section 5.6.

5.2 Electrostatic Potential And Tunneling Length

5.2.1 Analytical Solution

Figure 5.1 shows the SiNS FET geometry under investigation.

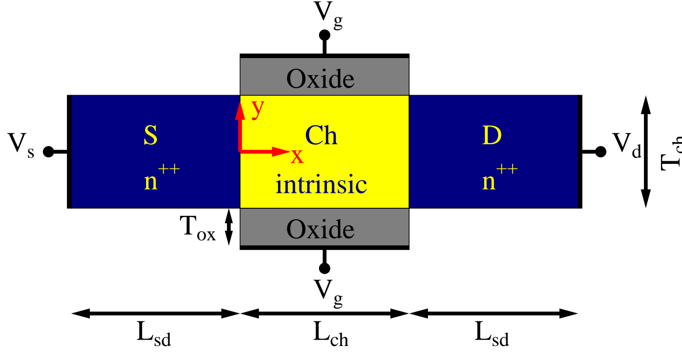

Figure 5.1: Sketch of the studied SiNS FET. Source/Drain (S/D) regions are highly n-doped and the channel (Ch) is intrinsic with a high-κ gate oxide material.

In [9], the following expression fulfilling all boundary conditions describes the corresponding two-dimensional (2-D) potential distribution $\Phi\,(x,y)$:

$$\begin{aligned}\Phi\,(x,y) = {} & \left(V^{\mathrm{s}}_{\mathrm{bi,eff}}\,(y) - \alpha(y)\right) \frac{\sinh((L_{\mathrm{ch}} - x)\,/\lambda\,(y))}{\sinh\,(L_{\mathrm{ch}}/\lambda\,(y))} \\ & + \left(V^{\mathrm{d}}_{\mathrm{bi,eff}}\,(y) - \alpha\,(y)\right) \frac{\sinh\,(x/\lambda\,(y))}{\sinh(L_{\mathrm{ch}}/\lambda\,(y))} + \alpha\,(y) \end{aligned} \tag{5.1}$$

with the effective built-in potential $V^{\mathrm{s/d}}_{\mathrm{bi,eff}}\,(y) = V^{\mathrm{s/d}}_{\mathrm{bi}} + V_{\mathrm{s/d}} - \Delta V^{\mathrm{s/d}}_{\mathrm{bi}}\,(y)$, the potential drop $\Delta V^{\mathrm{s/d}}_{\mathrm{bi}}\,(y)$ according to [9] and the built-in potenial $V^{\mathrm{s/d}}_{\mathrm{bi}} = V_{\mathrm{th}} \ln\left(N_{\mathrm{s/d}} N_{\mathrm{ch}}/n_{\mathrm{i}}^2\right)$ across the source/channel or drain/channel junction, $\alpha\,(y) = \Phi_{\mathrm{gs}} - \frac{qN_{\mathrm{ch}}}{\varepsilon_{\mathrm{ch}}}\lambda\,(y)^2$ the long channel (surface-to-surface) potential, $\lambda\,(y)$ the DG natural length along the vertical (y) dimension according to [10], L_{ch} the channel length, $V_{\mathrm{s/d}}$ the source or drain voltage, V_{th} the thermal voltage, $\Phi_{\mathrm{gs}} = V_{\mathrm{gs}} - V_{\mathrm{fb}}$ the gate to source voltage reduced by the flatband voltage, $\varepsilon_{\mathrm{ch}}$ the dielectric constant of the channel, $N_{\mathrm{s/d/ch}}$ the source, drain or channel doping concentration and n_{i} the intrinsic carrier concentration of the semiconductor. The primary use of (5.1) is to obtain the exact position $x = x_{\mathrm{m}}$ of the potential barrier $\Phi\,(x_{\mathrm{m}},y) = \Phi_{\mathrm{m}}$ by setting the electric field along the channel direction to zero. A simple analytic solution for x_{m} was derived in [11]:

$$x_{\mathrm{m}} = \frac{L_{\mathrm{ch}}}{2} - \frac{\lambda}{2} \ln\left(\frac{\gamma - e^{L_{\mathrm{ch}}/\lambda}}{1 - \gamma\, e^{L_{\mathrm{ch}}/\lambda}}\right) \tag{5.2}$$

with

$$\gamma = \frac{V_{\mathrm{bi,eff}}^{\mathrm{s}} - \alpha}{V_{\mathrm{bi,eff}}^{\mathrm{d}} - \alpha}. \tag{5.3}$$

5.2.2 Four-Piece Parabolic Approximation

Since our goal is to derive a simple analytic expression for L_{t}, we will not use (5.1). Together with the source and drain depletion regions, we reproduce the electrostatic potential Φ and the conduction band edge E_{CB} piecewise from four parts ($x \in i/ii/iii/iv$ shown in Figure 5.2).

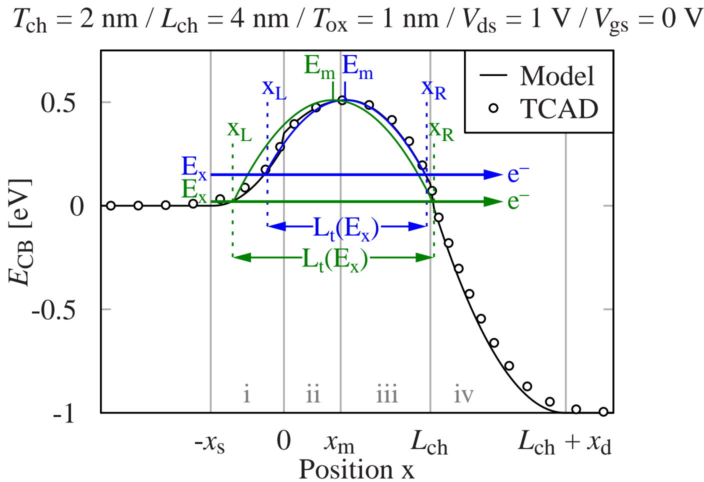

Figure 5.2: Modeled conduction band edge E_{CB} (black line according to (5.6)) of TCAD simulations (symbols) and demonstratively examining the accuracy of two possible parabolic approximations (blue or green line according to (5.22)) at two different energies E_{x} with their conventions. The parabolic approximation is used in Section 5.3.3 and 5.3.4 to formulate the analytical tunneling formula (5.25) or wavenumber (5.26).

The potential drops inside of the source (i) and drain (iv) region are given by the solution of the one-dimensional (1-D) Poisson equation, which are parabolic equations, and the channel electrostatic potential is given by two parabolic approximations, one between the source/channel interface and the potential barrier (ii) and the other between

the potential barrier and the drain/channel interface (*iii*):

$$\Phi = \begin{cases} V_{\mathrm{bi}}^{\mathrm{s}} + V_{\mathrm{s}} - \frac{qN_{\mathrm{s}}}{2\varepsilon_{\mathrm{s}}}\left(x + x_{\mathrm{s}}\right)^2 & \text{if } x \in i \\ \Phi_{\mathrm{m}} + \left(V_{\mathrm{bi,eff}}^{\mathrm{s}} - \Phi_{\mathrm{m}}\right)\frac{(x-x_{\mathrm{m}})^2}{x_{\mathrm{m}}^2} & \text{if } x \in ii \\ \Phi_{\mathrm{m}} + \left(V_{\mathrm{bi,eff}}^{\mathrm{d}} - \Phi_{\mathrm{m}}\right)\frac{(x-x_{\mathrm{m}})^2}{(L_{\mathrm{ch}}-x_{\mathrm{m}})^2} & \text{if } x \in iii \\ V_{\mathrm{bi}}^{\mathrm{d}} + V_{\mathrm{d}} - \frac{qN_{\mathrm{d}}}{2\varepsilon_{\mathrm{d}}}\left(x - (x_{\mathrm{d}} + L_{\mathrm{ch}})\right)^2 & \text{if } x \in iv \end{cases} \tag{5.4}$$

where x_{s} and x_{d} are the distances over which the potential drops occur and are given by

$$x_{\mathrm{s/d}} = \sqrt{\frac{2\varepsilon_{\mathrm{s/d}}\Delta V_{\mathrm{bi}}^{\mathrm{s/d}}}{qN_{\mathrm{s/d}}}}. \tag{5.5}$$

As (5.5) results from a 1-D solution, it should be used with caution. This is important because these values should be determined as accurately as possible, especially for those electron energies with high tunneling contribution. Next, we transform (5.4) into E_{CB} by considering the effect of different bandgaps in the channel region as an additional energy discontinuity $\Delta E_{\mathrm{bg/2}} = (E_{\mathrm{bg}}^{\mathrm{ch}}/2) - (E_{\mathrm{bg}}^{\mathrm{s/d}}/2)$. This is necessary due to different doping concentrations between the channel and source or drain region and the resulting narrowing of the bandgap outside the channel. Furthermore, this energy discontinuity remains in the ON-state of the device as a small energy barrier and is thus also the reason for the persistence of a slightly decreasing residual tunneling current. With reference level $E_{\mathrm{CB}} = 0$ eV at the source end, E_{CB} can finally be expressed as

$$E_{\mathrm{CB}} = \begin{cases} \frac{q^2N_{\mathrm{s}}}{2\varepsilon_{\mathrm{s}}}\left(x + x_{\mathrm{s}}\right)^2 & \text{if } x \in i \\ \Delta E_{\mathrm{bg/2}} + q\left(V_{\mathrm{bi}}^{\mathrm{s}} + V_{\mathrm{s}} - \Phi_{\mathrm{m}}\right) & \\ -q\left(V_{\mathrm{bi,eff}}^{\mathrm{s}} - \Phi_{\mathrm{m}}\right)\frac{(x-x_{\mathrm{m}})^2}{x_{\mathrm{m}}^2} & \text{if } x \in ii \\ \Delta E_{\mathrm{bg/2}} + q\left(V_{\mathrm{bi}}^{\mathrm{s}} + V_{\mathrm{s}} - \Phi_{\mathrm{m}}\right) & \\ -q\left(V_{\mathrm{bi,eff}}^{\mathrm{d}} - \Phi_{\mathrm{m}}\right)\frac{(x-x_{\mathrm{m}})^2}{(L_{\mathrm{ch}}-x_{\mathrm{m}})^2} & \text{if } x \in iii \\ q\left(V_{\mathrm{bi}}^{\mathrm{s}} + V_{\mathrm{s}} - V_{\mathrm{bi}}^{\mathrm{d}} - V_{\mathrm{d}}\right) & \\ +\frac{q^2N_{\mathrm{d}}}{2\varepsilon_{\mathrm{d}}}\left(x - (x_{\mathrm{d}} + L_{\mathrm{ch}})\right)^2 & \text{if } x \in iv. \end{cases} \tag{5.6}$$

This composition in (5.6) shall be referred to as the four-piece parapolic potential model (PPM).

5.2.3 Tunneling Length L_t

In order to determine the tunneling length (L_t), we need to calculate the position of the two classical turning points x_L and x_R for a specific kinetic energy E_x of tunneling electrons. These values are energy-dependent and therefore have to be determined piecewise from (5.6) by rearranging it to the coordinate x. Due to the piecewise definition (5.7) and (5.8) are formulated by using several Heaviside step functions θ with energy values E_x as arguments.

$$
\begin{aligned}
x_\mathrm{L}(E_\mathrm{x}) = & \left(-x_\mathrm{s} + \sqrt{E_\mathrm{x}\frac{2\,\varepsilon_\mathrm{s}}{q^2\,N_\mathrm{s}}}\right)\theta\left(q\,\Delta V_\mathrm{bi}^\mathrm{s} - E_\mathrm{x}\right) \\
& + \left(x_\mathrm{m} - x_\mathrm{m}\sqrt{\frac{\Delta E_{\mathrm{bg}/2} + q\left(V_\mathrm{bi}^\mathrm{s} + V_\mathrm{s} - \Phi_\mathrm{m}\right) - E_\mathrm{x}}{q\left(V_\mathrm{bi,eff}^\mathrm{s} - \Phi_\mathrm{m}\right)}}\right) \\
& \cdot \left[\theta\left(\Delta E_{\mathrm{bg}/2} + q\left(V_\mathrm{bi}^\mathrm{s} + V_\mathrm{s} - \Phi_\mathrm{m}\right) - E_\mathrm{x}\right) - \theta\left(\Delta E_{\mathrm{bg}/2} + q\,\Delta V_\mathrm{bi}^\mathrm{s} - E_\mathrm{x}\right)\right]
\end{aligned}
\tag{5.7}
$$

$$
\begin{aligned}
x_\mathrm{R}(E_\mathrm{x}) = & \left(x_\mathrm{m} + (L_\mathrm{ch} - x_\mathrm{m})\sqrt{\frac{\Delta E_{\mathrm{bg}/2} + q\left(V_\mathrm{bi}^\mathrm{s} + V_\mathrm{s} - \Phi_\mathrm{m}\right) - E_\mathrm{x}}{q\left(V_\mathrm{bi,eff}^\mathrm{d} - \Phi_\mathrm{m}\right)}}\right) \\
& \cdot \left[\theta\left(\Delta E_{\mathrm{bg}/2} + q\left(V_\mathrm{bi}^\mathrm{s} + V_\mathrm{s} - \Phi_\mathrm{m}\right) - E_\mathrm{x}\right)\right. \\
& \left. -\theta\left(\Delta E_{\mathrm{bg}/2} + q\left(V_\mathrm{bi}^\mathrm{s} + V_\mathrm{s} - V_\mathrm{bi,eff}^\mathrm{d}\right) - E_\mathrm{x}\right)\right] \\
& + L_\mathrm{ch} \cdot \left[\theta\left(\Delta E_{\mathrm{bg}/2} + q\left(V_\mathrm{bi}^\mathrm{s} + V_\mathrm{s} - V_\mathrm{bi,eff}^\mathrm{d}\right) - E_\mathrm{x}\right)\right. \\
& \left. -\theta\left(q\left(V_\mathrm{bi}^\mathrm{s} + V_\mathrm{s} - V_\mathrm{bi,eff}^\mathrm{d}\right) - E_\mathrm{x}\right)\right] \\
& + \left((x_\mathrm{d} + L_\mathrm{ch}) - \sqrt{\left(E_\mathrm{x} - q\left(V_\mathrm{bi}^\mathrm{s} - V_\mathrm{s} + V_\mathrm{bi}^\mathrm{d} + V_\mathrm{d}\right)\right)\frac{2\,\varepsilon_\mathrm{d}}{q^2\,N_\mathrm{d}}}\right) \\
& \cdot \theta\left(q\left(V_\mathrm{bi}^\mathrm{s} + V_\mathrm{s} - V_\mathrm{bi,eff}^\mathrm{d}\right) - E_\mathrm{x}\right)
\end{aligned}
\tag{5.8}
$$

Later in Section 5.4.1, we will introduce the tunneling formula and find out that noticeable tunneling currents larger than the leakage current flow only in ultrashort-channel transistors. Due to the Fermi-Dirac statistics, those electrons tunneling directly from the source into the drain region, i.e., from outside the channel, provide the largest contribution to the current. For illustration purposes in Figure 5.3(a), the change in current density J_t as a function of E_x is plotted against the tunneling length for various channel lengths L_ch. As can be seen, a significant increase in current density begins when the tunneling length is equal to or greater than the studied channel length. Hence, the tunneling length $L_\mathrm{t} = x_\mathrm{R} - x_\mathrm{L}$ can be simplified as follows and is compared to the

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original one in Figure 5.3(b):

$$L_{\mathrm{t}} \approx x_{\mathrm{s}} + x_{\mathrm{d}} + L_{\mathrm{ch}} - \sqrt{\frac{2\,\varepsilon_{\mathrm{s/d}}}{q^2\,N_{\mathrm{s/d}}}} \left(\sqrt{E_{\mathrm{x}} + q\,V_{\mathrm{ds}}} + \sqrt{E_{\mathrm{x}}}\right). \tag{5.9}$$

Obviously, this simplification is applicable to a wide range of energy. Although the tunneling length is not correctly determined for large energies near the barrier height, it is reasonable to use (5.9) for this range as well. Especially because both the WKB and the wavelet approximation consider only the potential shape above the electron energy under study and always treat the potential shape below E_{x} as flat, which leads to enhanced tunneling probabilities (see Figure 5.4(a)) for energies close to the maximum barrier height and this is incorrect. The influence of an approximated tunneling length on different parameter can be seen as dotted lines in most of the presented figures.

Next, the tunneling probabilities will be formulated in the following section.

5.3 Modeling of tunneling probability

5.3.1 WKB-Based Approach

The 1-D tunneling probability of electrons is approximated as follows [4]:

$$P_{\mathrm{t}}\left(y,E_{\mathrm{x}}\right) = \exp\left[-2\int_{x_{\mathrm{L}}}^{x_{\mathrm{R}}} k\left(x,y,E_{\mathrm{x}}\right)dx\right] \tag{5.10}$$

with

$$k\left(x,y,E_{\mathrm{x}}\right) = \sqrt{\frac{2\,m_{\mathrm{eff}}\left(E_{\mathrm{CB}}\left(x,y\right) - E_{\mathrm{x}}\right)}{\hbar^2}}. \tag{5.11}$$

The wavenumber $k\left(x,y,E_{\mathrm{x}}\right)$ is determined by the transverse effective electron mass $m_{\mathrm{eff}} = 0.19\ m_{\mathrm{e}}$ in tunnel direction x and the reduced Planck constant $\hbar$ [12].

One major problem of (5.10) is that the tunneling probability for energies close to 0 eV is small but not zero. Therefore, the accuracy of this equation is doubtful, at least for small energies.

5.3.2 Wavelet-Based Approach

Since an exact solution of the time-independent Schrödinger equation ($\Psi'' (x)$ - $K (x) \Psi (x) = 0$, with $K (x) = k^2 (x)$) is not given for nonrectangular potentials, the wavelet-based model approximates the solution by decomposing the wave function Ψ into harmonic wavelets. Suitable functions are the so-called Shannon wavelets, the father wavelet (or scaling function) φ and mother wavelet η with their complex conjugates $\bar{\varphi}$ & $\bar{\eta}$, which have the advantage that they are orthogonal and localized and their Fourier transforms are a square window function. Moreover, the exponential decay of the wave within the barrier is exploited for energies below the barrier height. Ψ is reconstructed as follows [13]:

$$\Psi (x) = \sum_{j=-\infty}^{\infty} \left(\alpha_j^0 \, \varphi_j^0 (x) + \tilde{\alpha}_j^0 \, \bar{\varphi}_j^0 (x) + \sum_{i=0}^{\infty} \beta_j^i \, \eta_j^i (x) + \tilde{\beta}_j^i \, \bar{\eta}_j^i (x) \right) , \qquad (5.12)$$

where α,$\tilde{\alpha}$ and $\beta, \tilde{\beta}$ are the wavelet coefficients. The derivatives of wavelets are related to the basis itself in the following manner:

$$\frac{d^2 \varphi_j^0 (x)}{dx^2} = \sum_{p=-\infty}^{\infty} \lambda_{pj}^{(2)} \, \varphi_p^0 (x) \quad \Bigg| \quad \frac{d^2 \eta_j^i (x)}{dx^2} = \sum_{q=0}^{\infty} \sum_{p=-\infty}^{\infty} \gamma_{pj}^{qi(2)} \, \eta_p^q (x) \, , \qquad (5.13)$$

where λ, γ and in analogy their conjugates $\bar{\lambda}$, $\bar{\gamma}$ are the following corresponding connection coefficients in Dirac notation:

$$\lambda_{pj}^{(2)} = \langle \varphi_p^0 (x) \mid \varphi_j^{0\,\prime\prime} (x) \rangle \quad \Bigg| \quad \gamma_{pj}^{qi(2)} = \langle \eta_p^q (x) \mid \eta_j^{i\,\prime\prime} (x) \rangle \, . \qquad (5.14)$$

Usually, around five terms are sufficient to reflect the important characteristics of functions within a short interval [14]. The Schrödinger equation becomes as follows when only the lowest scale approximation for $\Psi (x)$ and $\Psi'' (x)$ is considered as:

$$\begin{aligned} &\alpha_0^0 \, \lambda_{00}^{(2)} \, \varphi_0^0 (x) + \tilde{\alpha}_0^0 \, \bar{\lambda}_{00}^{(2)} \, \bar{\varphi}_0^0 (x) + \beta_0^0 \, \gamma_{00}^{00(2)} \, \eta_0^0 (x) + \tilde{\beta}_0^0 \, \bar{\gamma}_{00}^{00(2)} \, \bar{\eta}_0^0 (x) \\ &\qquad -K (x) \left[\alpha_0^0 \, \varphi_0^0 (x) + \tilde{\alpha}_0^0 \, \bar{\varphi}_0^0 (x) + \beta_0^0 \, \eta_0^0 (x) + \tilde{\beta}_0^0 \, \bar{\eta}_0^0 (x) \right] = 0. \end{aligned} \qquad (5.15)$$

By projection of the Schrödinger equation into the wavelet space, as described in

[15], we obtain the following equation system:

$$\begin{cases} \alpha_0^0\, \lambda_{00}^{(2)} - \alpha_0^0\, \underbrace{\langle \varphi_0^0\,(x)\mid K\,(x)\rangle}_{=b_0^0} = 0 \\ \tilde{\alpha}_0^0\, \bar{\lambda}_{00}^{(2)} - \tilde{\alpha}_0^0\, \underbrace{\langle \bar{\varphi}_0^0\,(x)\mid K\,(x)\rangle}_{=d_0^0} = 0 \\ \beta_0^0\, \gamma_{00}^{00(2)} - \beta_0^0\, \underbrace{\langle \eta_0^0\,(x)\mid K\,(x)\rangle}_{=c_0^0} = 0 \\ \tilde{\beta}_0^0\, \bar{\gamma}_{00}^{00(2)} - \tilde{\beta}_0^0\, \underbrace{\langle \bar{\eta}_0^0\,(x)\mid K\,(x)\rangle}_{=e_0^0} = 0. \end{cases} \tag{5.16}$$

Normally, the connection coefficients are determined by (5.14), but we note that due to the lowest scale approximation of Ψ, they now depend on $K\,(x)$. After previous division by the wavelet coefficients and multiplication with corresponding wavelet, the superposition of the equations in (5.16) gives:

$$\begin{aligned} \lambda_{00}^{(2)}\, \varphi_0^0(x) + \bar{\lambda}_{00}^{(2)}\, \bar{\varphi}_0^0\,(x) + \gamma_{00}^{00(2)}\, \eta_0^0\,(x) + \bar{\gamma}_{00}^{00(2)}\, \bar{\eta}_0^0\,(x) \\ = b_0^0\, \varphi_0^0\,(x) + d_0^0\, \bar{\varphi}_0^0\,(x) + c_0^0\, \eta_0^0\,(x) + e_0^0\, \bar{\eta}_0^0\,(x)\,. \end{aligned} \tag{5.17}$$

The left-hand side of (5.17) is identical to the one of an equivalent rectangular barrier with $K\,(x) = K_{\mathrm{eq}}$. The right-hand side is $K\,(x)$ decomposed into wavelets. Equating the Euclidean norm in Hilbert space L^2 of $K\,(x)$ and K_{eq} gives for each electron energy E_{x} the height of the equivalent rectangular barrier

$$\begin{aligned} ||K_{\mathrm{eq}}||^2 &= ||K\,(x)\,||^2 \\ \langle K_{\mathrm{eq}} \mid K_{\mathrm{eq}}\rangle &= \langle K\,(x)\mid K\,(x)\rangle \\ K_{\mathrm{eq}}^2 L_{\mathrm{t}} &\approx |b_0^0|^2 + |d_0^0|^2 + |c_0^0|^2 + |e_0^0|^2 \\ K_{\mathrm{eq}} &\approx \frac{1}{L_{\mathrm{t}}} \sqrt{|b_0^0|^2 + |d_0^0|^2 + |c_0^0|^2 + |e_0^0|^2} \end{aligned} \tag{5.18}$$

Instead of calculating all b, d, c, and e, a measurable function such as $K\,(x)$ is also Lebesgue integrable. It follows:

$$K_{\mathrm{eq}} = k_{\mathrm{eq}}^2 \approx \sqrt{\frac{1}{L_{\mathrm{t}}} \int_0^{L_{\mathrm{t}}} K\,(x)^2\, dx} \tag{5.19}$$

This result is used in the analytic expression for the tunneling probability of a rectangular energy barrier, which is given as follows:

$$P_{\mathrm{t}}\left(y,E_{\mathrm{x}}\right)=\left(1+\frac{\sinh^{2}\left(k_{\mathrm{eq}}\left(y,E_{\mathrm{x}}\right)\,L_{\mathrm{t}}\right)}{4\,\frac{E_{\mathrm{x}}}{E_{\mathrm{eq}}}\left(1-\frac{E_{\mathrm{x}}}{E_{\mathrm{eq}}}\right)}\right)^{-1} \tag{5.20}$$

with

$$E_{\mathrm{eq}}\left(E_{\mathrm{x}}\right)=\frac{\hbar^{2}}{2\,m_{\mathrm{eff}}}\,k_{\mathrm{eq}}^{2}+E_{\mathrm{x}} \tag{5.21}$$

as the equivalent potential barrier height.

5.3.3 WKB-Based Analytical Solution

For compact modeling purposes, we need to further simplify the analytic expression of E_{CB} in (5.6). We assume that each electron with energy E_{x} tunnels through a single parabolic energy barrier (see Figure 5.2) with its tunneling distance determined in Section 5.2.3. We use the following formula:

$$E_{\mathrm{CB}}\approx E_{\mathrm{m}}-\left(E_{\mathrm{m}}-E_{\mathrm{x}}\right)\frac{\left(x-x_{\mathrm{m}}\right)^{2}}{\left(L_{\mathrm{t}}/2\right)^{2}} \tag{5.22}$$

with E_{m} as the electron barrier height given by

$$E_{\mathrm{m}}=\mathit{\Delta}E_{\mathrm{bg}/2}+q\left(V_{\mathrm{bi}}^{\mathrm{s}}+V_{\mathrm{s}}-\mathit{\Phi}_{\mathrm{m}}\right). \tag{5.23}$$

For simplicity, we relocate the vertex of the parabola from x_{m} to $L_{\mathrm{t}}/2$. Consequently, the approximated equation for K is given by

$$K(x')=k\left(x'\right)^{2}\approx\frac{2\,m_{\mathrm{eff}}}{\hbar^{2}}\left(E_{\mathrm{m}}-\left(E_{\mathrm{m}}-E_{\mathrm{x}}\right)\frac{\left(x'-L_{\mathrm{t}}/2\right)^{2}}{\left(L_{\mathrm{t}}/2\right)^{2}}-E_{\mathrm{x}}\right). \tag{5.24}$$

By substituting (5.24) into (5.10) we obtain the following analytical equation for the

WKB-based tunneling probability:

$$P_\mathrm{t} = \exp\left[-\sqrt{\frac{8\,m_\mathrm{eff}}{\hbar^2}}\int_0^{L_\mathrm{t}}\sqrt{E_\mathrm{m} - (E_\mathrm{m} - E_\mathrm{x})\,\frac{(x' - L_\mathrm{t})^2}{(L_\mathrm{t}/2)^2} - E_\mathrm{x}dx'}\right]$$
$$= \exp\left(-\frac{\pi}{2}L_\mathrm{t}\sqrt{\frac{2\,m_\mathrm{eff}}{\hbar^2}\,(E_\mathrm{m} - E_\mathrm{x})}\right). \tag{5.25}$$

The behavior of (5.25) versus E_x is shown in green in Figure 5.4(a) for both approximated (dotted line) and non-approximated (solid line) tunneling length L_t.

5.3.4 Wavelet-Based Analytical Solution

The presented parabolic approximation of the energy barrier in (5.22) can also be used for the wavelet-based method in (5.19). It follows:

$$k_\mathrm{eq} \approx k_\mathrm{fit}\,(8/15)^{\frac{1}{4}}\sqrt{\frac{2\,m_\mathrm{eff}}{\hbar^2}\,(E_\mathrm{m} - E_\mathrm{x})}, \tag{5.26}$$

where k_fit is an additional fitting parameter which is necessary due to the previously applied approximations in the derivation of the wavelet-based approach from Section 5.3.2. An appropriate value for k_fit is 1.09. This result in (5.26) can be interpreted in such a way that each electron with energy E_x tunnels through an equivalent rectangular barrier with reduced total barrier height. By substituting (5.26) into (5.21) the equivalent potential barrier height is calculated as

$$E_\mathrm{eq} = k_\mathrm{fit}^2\,\sqrt{8/15}\,E_\mathrm{m} + \left(1 - k_\mathrm{fit}^2\,\sqrt{8/15}\right)E_\mathrm{x}. \tag{5.27}$$

Both (5.26) and (5.27) are implemented in (5.20), which is shown in blue in Figure 5.4(a) as in the WKB part from the previous section.

5.4 Calculation of Tunneling Current

5.4.1 TSU-ESAKI Tunneling Formula

Using the tunneling probability, we determine the tunneling current density $J_\mathrm{t}(y)$ by weighting P_t with the amount of electrons available at a given tunneling energy E_x, the so-called supply function $N\,(E_\mathrm{x})$ introduced by Gehring [16]. The net electron tunneling

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current density is described by the TSU-ESAKI formula by integration in the energy domain [17]

$$J_{\mathrm{t}}(y) = \frac{q\, m_{\mathrm{eff}}}{2\,\pi^2\,\hbar^3} \int_0^{E_{\mathrm{m}}} \underbrace{P_{\mathrm{t}}(y, E_{\mathrm{x}})\, N(E_{\mathrm{x}})}_{=:PN(E_{\mathrm{x}})}\, dE_{\mathrm{x}}. \tag{5.28}$$

The supply function considers the tunneling in both directions by using the Fermi-Dirac distributions f_{s} and f_{d} at the source/channel and channel/drain interfaces. $N(E_{\mathrm{x}})$ can be expressed as

$$N(E_{\mathrm{x}}) = \int_0^{\infty} (f_{\mathrm{s}}(E) - f_{\mathrm{d}}(E))\, dE_\rho = q\,V_{\mathrm{th}}\, \ln\left(\frac{1+\exp\left(-\frac{E_{\mathrm{x}}-E_{\mathrm{f,s}}}{q\,V_{\mathrm{th}}}\right)}{1+\exp\left(-\frac{E_{\mathrm{x}}-E_{\mathrm{f,d}}}{q\,V_{\mathrm{th}}}\right)}\right) \tag{5.29}$$

and contains only the integration in transverse (E_ρ)-direction. The longitudinal part E_{x} of the total energy E is considered after weighting with the tunneling probability in (6.1). $E_{\mathrm{f,s}}$ and $E_{\mathrm{f,d}}$ are the Fermi energies.

5.4.2 Quasi-Compact Modeling Of Current Density J_{t}

The integration in (6.1) is not analytically solvable for either the WKB-based or the wavelet-based solution of P_{t}. To keep the number of function values necessary to calculate the integral as small as possible, we first determine the electron energy $E_{\mathrm{x,max}}$ with maximum contribution to the tunneling current. This requires a classical zero calculation of the derivative of the integrand $PN(E_{\mathrm{x}})$ from (6.1) with respect to the energy. A rearrangement of the result to E_{x} is analytically not possible, and hence, Newton's iterative method is used to localize the position $E_{\mathrm{x,max}}$. Although, in view of Figure 5.4(b), $E_{\mathrm{m}}/3$ would be suitable as the initial estimation point, it was found that even smaller values would be needed for, e.g., large V_{ds} in the WKB approach. Therefore, without any restrictions on small V_{ds}, $E_{\mathrm{m}}/6$ is used here as the initial estimation point. Furthermore, a total of two iterations are sufficient. Since the derivative cannot be determined so easily, $PN(E_{\mathrm{x}})$ is first approximated for the sought energy range. An approximation of the supply function in (5.29) with the Boltzmann statistics is helpful here

$$N(E_{\mathrm{x}}) \approx qV_{\mathrm{th}} \left(1 - e^{-\frac{V_{\mathrm{ds}}}{V_{\mathrm{th}}}}\right) e^{-\frac{E_{\mathrm{x}}-E_{\mathrm{f,s}}}{qV_{\mathrm{th}}}}. \tag{5.30}$$

In addition, in case of the wavelet-based approach, (5.20) can be significantly simplified for probabilities smaller than 1‰. This is only given if the hyperbolic function is large. It follows:

$$P_{\mathrm{t}}\left(y,E_{\mathrm{x}}\right) \approx 16\,\frac{E_{\mathrm{x}}}{E_{\mathrm{eq}}}\left(1-\frac{E_{\mathrm{x}}}{E_{\mathrm{eq}}}\right)e^{-2\,k_{\mathrm{eq}}(y,E_{\mathrm{x}})\cdot L_{\mathrm{t}}} \tag{5.31}$$

with

$$E_{\mathrm{eq}}\left(E_{\mathrm{x}}=\frac{E_{\mathrm{m}}}{6}\right) \approx k_{\mathrm{fit}}^2\,\sqrt{8/15}\,E_{\mathrm{m}}+\left(1-k_{\mathrm{fit}}^2\,\sqrt{8/15}\right)\frac{E_{\mathrm{m}}}{6} \approx 0.89\,E_{\mathrm{m}}. \tag{5.32}$$

Furthermore, we use the simplified equation in (5.9) for the tunneling length L_{t}.

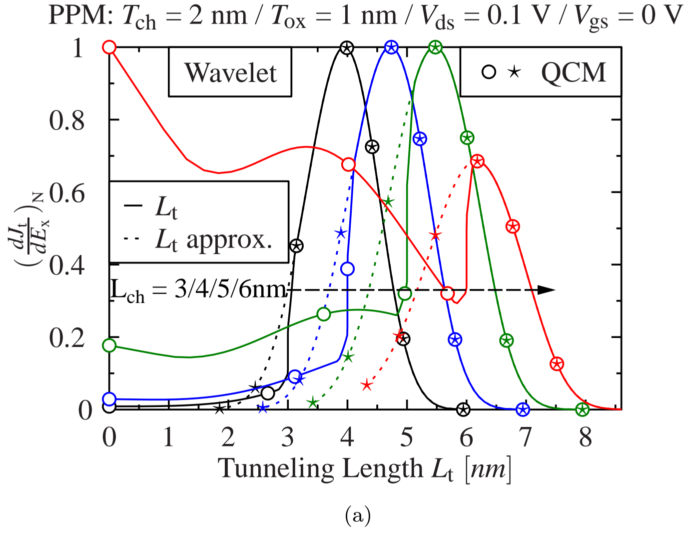
$$J_{\mathrm{t}} \approx \frac{q\,m_{\mathrm{eff}}}{2\,\pi^2\,\hbar^3}\sum_{i=0}^{N-1}\frac{E_{\mathrm{x,max}}}{N}\cdot\frac{PN\left(E_{\mathrm{x,max}}\frac{i+1}{N}\right)+PN\left(E_{\mathrm{x,max}}\frac{i}{N}\right)}{2}+\frac{E_{\mathrm{m}}-E_{\mathrm{x,max}}}{N}\cdot \frac{PN\left(E_{\mathrm{x,max}}+\left(E_{\mathrm{m}}-E_{\mathrm{x,max}}\right)\frac{i}{N}\right)+PN\left(E_{\mathrm{x,max}}+\left(E_{\mathrm{m}}-E_{\mathrm{x,max}}\right)\frac{i+1}{N}\right)}{2} \tag{5.33}$$

With (5.33) for three more equidistant positions (N = 3) before and after the determined maximum $E_{\mathrm{x,max}}$, the exact function values of $PN\left(E_{\mathrm{x}}\right)$ are calculated, linearly interpolated, and the area underneath is determined (see Figure 5.4(b)).

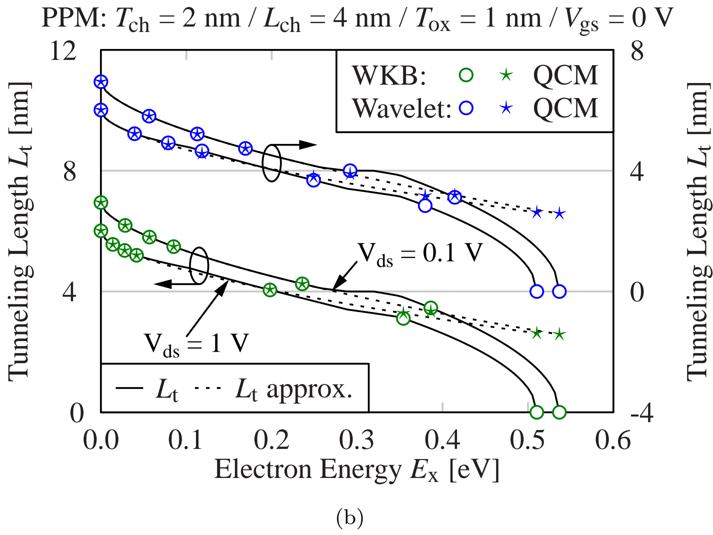
In Figures 5.3, 5.4 and 5.6, the interpolation points are shown as symbols for the WKB and wavelet approaches. In particular, it can be seen from the interpolation points in 5.4(b) that the localization of $E_{\mathrm{x,max}}$ proves to be somewhat inaccurate in the case of WKB. The reason for this is the approximation of the Fermi-Dirac statistics by the Boltzmann statistics. The Boltzmann statistics gives sufficiently accurate results only for electron energies about three times the thermal energy above the source-related Fermi level ($E_{\mathrm{x}} > 3\,q\,V_{\mathrm{th}} + E_{\mathrm{f,s}}$). In our case, this corresponds to an energy of about 0.14 eV. As can be easily seen, $E_{\mathrm{x,max}}$ is below this value in the case of WKB and above it in the case of wavelet.

5.4.3 Tunneling Current I_{t}

In [6] we have found for DG FETs that the current density J_{t} shows a linear course in the transverse direction from center (J_{C}) to surface (J_{S}). This is a very good approximation for small gate biases and ultrashort-channel devices. Further studies have shown that an even more precise approximation is possible with the following Gaussian function, which is more accurate, especially for gate biases close to the threshold voltage (see

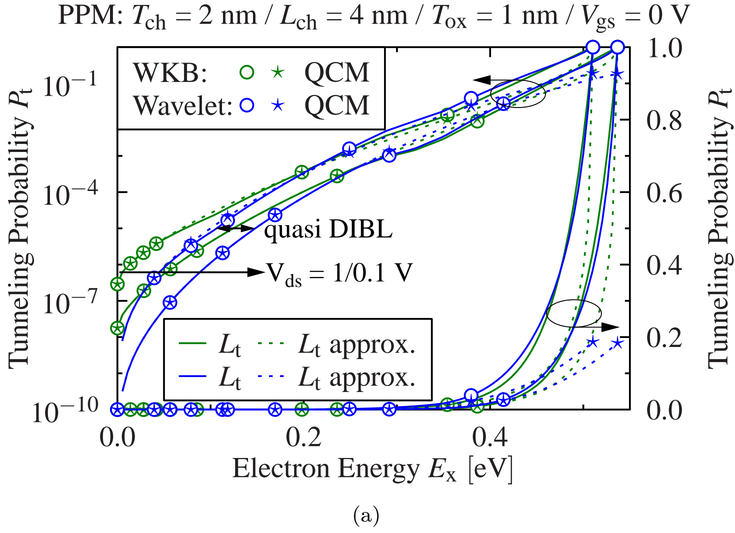


(a)

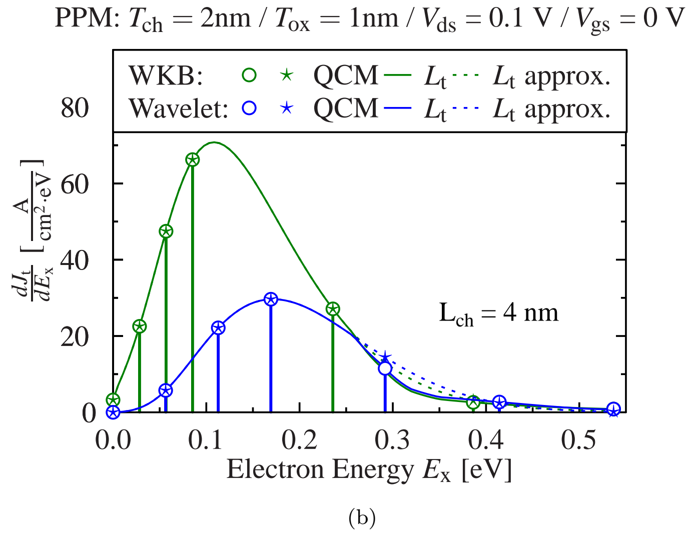


(b)

Figure 5.3: Normalized first derivation of J_t with respect to E_x against (a) L_t. (b) Tunneling length against the electron energy E_x. (b) WKB and Wavelet are compared with each other. (a)-(b) Symbols represent the QCM applied to models with approximated (5.9) (dotted line) and nonapproximated (5.7)+(5.8) (solid line) tunneling lengths.



(a)



(b)

Figure 5.4: Normalized first derivation of J_t with respect to E_x against (b) E_x. (a) First derivation of J_t with respect to E_x against E_x. (a)-(b) WKB and Wavelet are compared with each other. (a)-(b) Symbols represent the QCM applied to models with approximated (5.9) (dotted line) and nonapproximated (5.7)+(5.8) (solid line) tunneling lengths.

Figure 5.5) and also for longer channels:

$$J_{\mathrm{t}}(y) \approx J_{\mathrm{C}}\, e^{-\frac{y^2}{(T_{\mathrm{ch}}/2)^2}\, \ln\left(\frac{J_{\mathrm{C}}}{J_{\mathrm{S}}}\right)}. \tag{5.34}$$

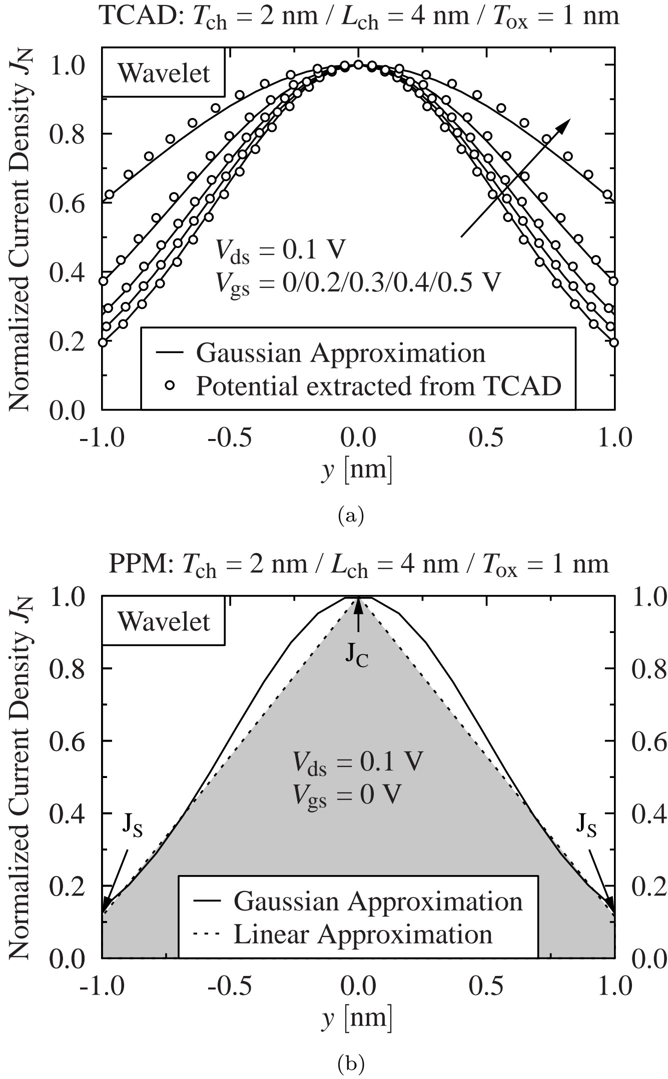


Figure 5.5: Channel cross section of the normalized current density J_{N} for (a) different gate biases and their Gaussian approximation and (b) compared to a linear approximation.

A negative side effect is the existence of the Gauss error function, which cannot be evaluated in closed form in terms of elementary functions and must be determined numerically. The obtained formula for SiNS FET is

$$I_{\mathrm{t}} = W_{\mathrm{ch}} \int_{-\frac{T_{\mathrm{ch}}}{2}}^{\frac{T_{\mathrm{ch}}}{2}} J_{\mathrm{t}}(y)\, dy \approx \frac{\sqrt{\pi}}{2} J_{\mathrm{C}} T_{\mathrm{ch}} W_{\mathrm{ch}} \frac{Erf\left(\sqrt{\ln\left(\frac{J_{\mathrm{C}}}{J_{\mathrm{S}}}\right)}\right)}{\sqrt{\ln\left(\frac{J_{\mathrm{C}}}{J_{\mathrm{S}}}\right)}}. \tag{5.35}$$

5.4.4 Total Current I_{ds}

The total current I_{ds} is the sum of the tunneling current I_{t} and the drift-diffusion current I_{dd}:

$$I_{\mathrm{ds}} = I_{\mathrm{t}} + I_{\mathrm{dd}}. \tag{5.36}$$

I_{dd} is determined with our compact model published in [18] and [19]. As already mentioned in Section 5.1, we determine I_{t} from (5.35) and the corresponding subthreshold swing (S_{sth}) from two gate biases $V_{\mathrm{gs},1} = V_{\mathrm{fb}}$ and $V_{\mathrm{gs},2} = V_{\mathrm{fb}} + 0.1$ V as

$$S_{\mathrm{sth}}(V_{\mathrm{ds}}) = \frac{\ln(10)\,(V_{\mathrm{gs},2} - V_{\mathrm{gs},1})}{\ln(I_{\mathrm{t}}(V_{\mathrm{gs},2}, V_{\mathrm{ds}})) - \ln(I_{\mathrm{t}}(V_{\mathrm{gs},1}, V_{\mathrm{ds}}))} \tag{5.37}$$

In subthreshold regime we rewrite $I_{\mathrm{t}} \to I_{\mathrm{T}}$ as follows:

$$I_{\mathrm{T}}(V_{\mathrm{gs}}, V_{\mathrm{ds}}) = I_{\mathrm{t}}(V_{\mathrm{gs}} = V_{\mathrm{fb}}, V_{\mathrm{ds}}) \cdot e^{(V_{\mathrm{gx}} - V_{\mathrm{fb}})\frac{\ln(10)}{S_{\mathrm{sth}}}} \tag{5.38}$$

and use it instead of I_{t} in (5.36). The parameter V_{gx} is the gate-to-source voltage V_{gs} smoothly limited by the threshold voltage V_{T}

$$V_{\mathrm{gx}} = V_{\mathrm{gs}} - \frac{\ln\left(1 + e^{C(V_{\mathrm{gs}} - (V_{\mathrm{T}} - \Delta V_{\mathrm{T}}))}\right)}{\ln(1 + A\, e^{C})} \tag{5.39}$$

with $C = \ln(10) / (2\, S_{\mathrm{sth}})$ and empirical fitting parameters $A \approx 0.5$ and $\Delta V_{\mathrm{T}} \approx -0.06$ V. I_{t} will not completely vanish above V_{T} because a minimum barrier always remains due to the additional energy discontinuity $\Delta E_{\mathrm{bg/2}}$. However, this current plays a minor role in the ON-state anyway, since I_{dd} overwhelms it by several orders of magnitude. The control is done by the parameter A.

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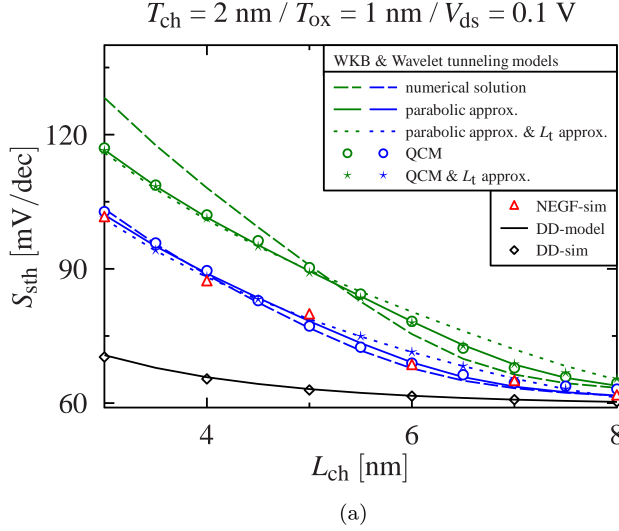
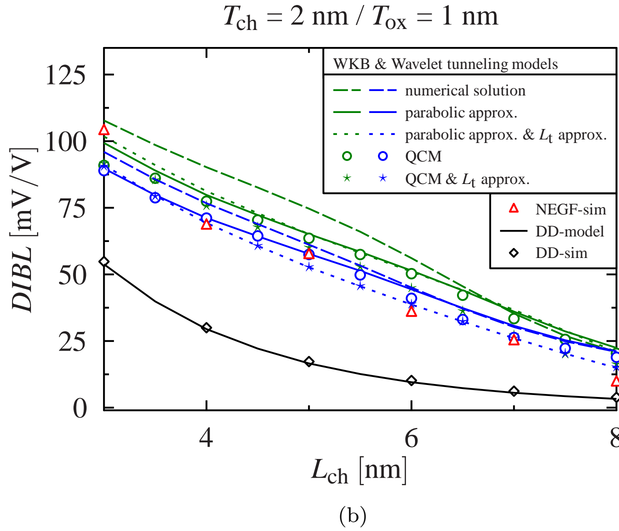
5.5 Model Verification

In this section, the influences of the tunneling current on the short channel characteristics and the total current are presented. The channel thickness considered is $T_{\mathrm{ch}} = 2$ nm with a gate oxide layer thickness of $T_{\mathrm{ox}} = 1$ nm using $\mathrm{HfO_2}$ as the gate material with a relative permittivity $\varepsilon_{\mathrm{r}} = 22$. The channel length L_{ch} is varied between 3 and 8 nm, where $L_{\mathrm{ch}} = 3$ nm is borderline because the ratio I_{ON} to I_{OFF} becomes smaller than 10^5. The channel is undoped, while the source and drain regions are heavily n-doped with $N = 10^{20}$ cm^{-3}. It is worth noting that lower doping also leads to smaller tunneling currents since the potential drop according to (5.5) in the source and drain regions occurs over a longer distance in the current direction, thus increasing the tunneling length. The potential barrier Φ_{m} is determined by using our potential model from [18, 20], which is based on the conformal mapping technique. QC has a negligible influence on the subthreshold swing and DIBL behavior of the tunneling current I_{t} but reduces both I_{t} and I_{dd} due to bandgap widening. The effective increase in Φ_{m} is considered in the aforementioned potential model and the consequent increase in threshold voltage V_{T} is already implemented in our compact model published in [18] and [19].

In Figure 5.6(a) and 5.6(b), the subthreshold swing S_{sth} as well as the DIBL are plotted as a function of channel length. The results shown for WKB and wavelet are obtained from the current equation (5.35) and from transmission characteristics of the NEGF simulator (NEGF-sim) NanoMOS [7]. The comparison between WKB, wavelet, and NEGF shows that the wavelet model has a much better agreement with the numerically more sophisticated but more accurate NEGF simulator. In addition, the wavelet model is more resistant to the performed approximations than the WKB method. Already, the parabolic approximation from Section 5.3.3 to find an analytical equation for the tunneling probability is a big hurdle for the WKB method. This is because, as can be seen very well from Figure 5.2, the blue parabola describes the potential curve at smaller energies better than the green parabola. Concomitantly, it is already known from Figure 5.4(b) that in case of WKB, tunneling occurs closer to the conduction band edge E_{CB} compared to the wavelet method.



(a)



(b)

Figure 5.6: (a) Subthreshold swing S_{sth} and DIBL (b) against the channel length. The symbols (circle and star) represent the QCM applied to the parabolic models (green: WKB (5.25) and blue: wavelet (5.26)) with approximated (dotted line) and nonapproximated (solid line) tunneling lengths. The red symbols (triangular) represent the NEGF simulation (NEGF-sim) and the black line or symbol the drift-diffusion compact model (DD-model) or Sentaurus TCAD simulation DD-sim. The dashed lines stand for the numerical calculation of P_t (WKB approach according to (5.10)) or K_{eq} (wavelet approach according to (5.19)).

Furthermore, in Figure 5.6(a) and 5.6(b), a slight deviation from the numerical (dashed lines) and parabolic approximation (solid lines) results for larger channel length due to the approximation of L_t (dotted lines) according to (5.9) at higher energies. Again, this deviation due to a larger effective tunneling length has a rather positive effect for higher energies since the potential curve below E_x, as already mentioned, is neglected in the calculation of the tunneling probability and therefore theoretically leads in parabolically shaped potential to increased current, subthreshold swing, and DIBL. A larger effective tunneling length at higher energies suppresses and partially compensates for this inaccuracy in the approaches. Also, it is clearly visible that the symbols (circle and star) representing the QCM follow the solid or dotted lines and are therefore quite useful. Furthermore, drift-diffusion simulations (DD-sims) with Sentaurus TCAD, as well as the corresponding drift-diffusion compact model (DD-model) according to [18] and [19] are included in the comparison without consideration of the tunneling current.

Figure 5.7 shows for a chosen device with channel length $L_{ch} = 4$ nm the separation of the total device current I_{ds} into the drift-diffusion current I_{dd} and DSDT current I_T with our QCM using the wavelet method. In the transfer characteristics, the drift-diffusion current I_{dd} describes the device behavior in the ON-state, whereas the DSDT current I_T according to (5.38) dominates the subthreshold region. Again, the model is compared to NEGF simulations and shows good agreement.

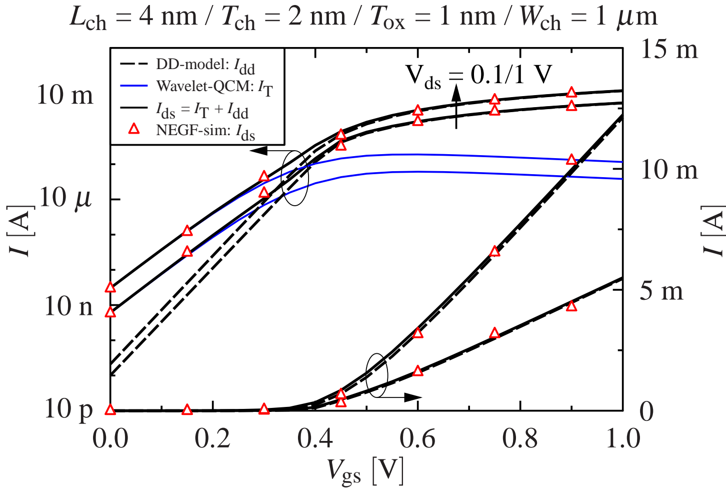


Figure 5.7: Separation of the total model current I_{dd} into the drift-diffusion (dd) current I_{dd} and tunneling current I_T. The transfer characteristics is given by both, the model and simulation data at $V_{ds} = 0.1$ and 1 V.

5.6 Conclusion

In this work, we have presented a QCM for calculating the DSDT current in ultrashort-channel SiNS FETs. The analysis highlights the importance of tunneling from outside the channel directly from source into the drain region and the need for accurate determination of the tunneling length in this region. Due to the inaccuracy of the WKB method close to the conduction band edge, we conclude that this approach is not optimal for determining tunneling current. Instead, an equivalent rectangular barrier using the wavelet method represents much better the property of a rapidly decreasing tunneling probability near the conduction band edge and is dominated in this region by a more accurate tunneling length than by the size of the enclosed area above E_{x}. Therefore, in comparison, the parabolic approximation is significantly less problematic. With this approach and the performed approximations, an analytically compact description of the tunneling current is possible, and thus, in combination with a classical drift-diffusion model, a complete QCM for all operation regimes down to ultrashort channels is realized. Because the analytical approach requires a Newton iteration and linear interpolation for solving the integral (6.1), we call the model “quasi compact”.

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CHAPTER 6

Cryogenic Temperature and Doping Analysis of Source-to-Drain Tunneling Current in Ultrashort-Channel Nanosheet MOSFETs

This work analyzes the impact of doping concentration on the temperature dependent subthreshold current and swing saturation due to direct source-to-drain tunneling (DSDT) in short-channel silicon nanosheet (SiNS) metal-oxide-semiconductor field-effect transistors (MOSFETs). Further, their influence on the drain-induced barrier lowering (DIBL) effect is investigated. Special attention is paid to the importance of the Fermi level and the average tunneling energy, whose energetic positions and distance from each other in the band diagram has a significant role in the temperature-dependent saturation behavior of the subthreshold current and swing, as well as the value of DIBL. Furthermore, we model and present with device simulation the existence of two merging subthreshold swings (S_{sth}) and DIBL effects with increasing gate bias at cryogenic temperatures. The merging is achieved by the superposition of the DSDT and thermionic emission (TE) current, which originate from their own dominated and visibly separated gate-bias regions.

6.1 Introduction

Low temperature applications gain more and more importance. Either the given ambient temperature like in space makes it necessary to develop functioning devices such as sensors and detectors or the demand for higher performance due to their limits at room temperature or the existence of completely new technologies only at deep cryogenic temperatures. As an example, the latter includes quantum computing and is performed

by quantum computers using quantum bit systems (qubits) that correspond to the classical bits in conventional computers. These systems are surrounded and wired by electronics including complementary metal-oxide-semiconductor (CMOS) devices, which also provides scalability of quantum processors [1, 2]. This makes reliable modeling of low-temperature devices of MOSFETs inevitable. Unfortunately, existing I-V models are not always inherently valid for cryogenic conditions [3], so that measurements, simulation analysis and model development of different transistor types are the focus of research [4–8].

Several parameters of semiconductor materials such as the intrinsic carrier concentration, the density-of-states, the bandgap including Fermi energy, the charge carrier mobility and the effective carrier masses are influenced by the temperature (T) and are well described in [4]. We observe its direct impact on the subthreshold domain of the transfer characteristics.

In general, it is known that the lower the temperature (T), the better the device performance. According to the linear temperature dependence of the Boltzmann limit of the subthreshold swing ($S_{\mathrm{sth}} = \ln(10)\,(k_{\mathrm{B}}T/q)$ where k_{B} is the Boltzmann's constant and q the elementary charge) in classical MOSFETs, an ideal, infinitely steep, quasi step-like switching behavior of the current is expected at deep-cryogenic temperatures. Unfortunately, this is not what is observed experimentally. Thus, the validity of the Boltzmann limit is also not given at low temperatures even for larger ratios of channel lengths to channel thicknesses (4:1) in the nanometer scale range, where no subthreshold swing degradation or drain-induced barrier lowering (DIBL) due to short-channel effect appears.

A temperature-dependent limit for the subthreshold swing of MOSFETs with μm-range gate length was reported in [9–11]. Below the critical temperature $T_{\mathrm{c}} = 46$ K a device technology dependent saturation limit of about $S_{\mathrm{sth}} \approx 10$ mV/dec was measured and explained by the presence of an exponential band tail or the rise of trap density near the band edge. Recently, another type of temperature dependent swing saturation for nanometer-scale devices has been reported. In [12], it was mentioned that nonequilibrium Green's function (NEGF) simulations have shown that for a given channel length L_{ch} the current and the S_{sth} become insensitive to temperature reduction after reaching a critical value T_{c}. This value increases as L_{ch} decreases. The insensitivity was explained by the low temperature dependence of the quantum mechanical direct source-to-drain tunneling (DSDT) current [13], which superimposes the steep swing of the thermionic emission (TE) current determined by the aforementioned Boltzmann limit. Increasing the effective tunneling mass m_{eff} by suitable semiconductor selection, as well as the

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use of gate-source and gate-drain underlappings or thin tunnel barriers at the source junction are mentioned as possible adjusting screws to reduce the tunneling current [12].

In this work, the impact of doping concentration and operating temperature on the subthreshold current, swing and DIBL is examined. In the following Section 6.2, we describe the used simulation setup and the modeling approach. Next, in Section 6.3, we give several results and discuss them with the help of the Fermi-Dirac distribution function, which is part of the Tsu-Esaki formula for the tunneling process. Last but not least, we give a conclusion in Section 6.4.

6.2 Simulation and Modeling Approach

NEGF simulations of double-gate (DG) devices are performed using the NanoMOS tool [14]. Quantum-mechanical effects such as quantum confinement (QC) in thin transistors transverse to the current direction and the DSDT current along the channel are captured for the electron subbands by solving the Schrödinger equation self-consistently with the Poisson equation. Prior analyzes have shown that QC does not have a direct impact on the subthreshold characteristics in terms of swing or DIBL degradation [15]. It is mainly reducing the intrinsic carrier concentration and hence the current and increases the threshold voltage of the device due to bandgap widening [16, 17].

Besides DSDT and TE current, no further influences such as electron-phonon scattering or traps are taken into account. Both assumptions are valid, since the focus is on the subthreshold region and the investigated devices are short-channel transistors whereas scattering appears when the channel length is long compared to the mean free path for electron-phonon interactions [18]. In all simulations, the crystal orientation $< 100 >$ of silicon is chosen along the channel direction, and the channel surface orientation is chosen as (001). The gate workfunction is set to 4.45 eV. Furthermore, abrupt junctions are used for simplicity, and due to convergence issues in the simulation, we have analyzed the temperature dependence down to 25 K, but not below. In addition, due to degenerate doping in the source and drain region, dopant freeze-out is negligible [19–21]. The device parameters are chosen for analysis and modeling purposes, and are not related to any scaling roadmap.

Our analytical model is based on the wavelet approach, which solves the tunneling probability for each energy level E_{x} by assuming a rectangular energy subband with an equivalent barrier height E_{eq}. This approach has been extensively discussed in [22, 23] and is preferred over the Wentzel-Kramers-Brillouin (WKB) method, because especially for very small E_{x} the tunneling probability $P_{\mathrm{t}}\,(y,E_{\mathrm{x}})$ is determined more accurately.

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The tunneling current density $J_{\mathrm{t}}(y)$ in channel (x-)direction at position y transverse to the channel is calculated by the TSU-ESAKI formula and is given by:

$$J_{\mathrm{t}}(y) = \frac{q m_{\mathrm{eff}}}{2\pi^2\hbar^3} \int_0^{E_{\mathrm{m}}} \underbrace{P_{\mathrm{t}}(y,E_{\mathrm{x}})\, N(E_{\mathrm{x}})}_{=:PN(E_{\mathrm{x}})} dE_{\mathrm{x}}, \tag{6.1}$$

with $\hbar$ the reduced Planck constant, E_{m} the barrier height, $N(E_{\mathrm{x}})$ the supply function and $m_{\mathrm{eff}} = 0.19\ m_{\mathrm{e}}$ the transverse effective electron mass in tunneling direction x with the electron rest mass m_{e} [24]. The Tsu-Esaki formula uses the three-dimensional (3-D) density of states in momentum space and thus does not consider QC, while the NEGF simulations use the two-dimensional (2-D) density of states including QC. A closed expression for a 2-D Tsu-Esaki formula that takes QC into account is not given. But since our analysis in [15] has shown that QC has no impact on the subthreshold swing and DIBL degradation, for a simple analytical approach, the 3-D Tsu-Esaki formula is applicable. $N(E_{\mathrm{x}})$ contains the Fermi-Dirac statistics with Fermi energies $E_{\mathrm{f,s}}$ and $E_{\mathrm{f,d}}$ at the source and drain regions, respectively, and gives the amount of electrons available for tunneling at a given energy E_{x}. The formula for $N(E_{\mathrm{x}})$ is:

$$N(E_{\mathrm{x}}) = qV_{\mathrm{th}} \ln\left(\frac{1+\exp\left(-\frac{E_{\mathrm{x}}-E_{\mathrm{f,s}}}{qV_{\mathrm{th}}}\right)}{1+\exp\left(-\frac{E_{\mathrm{x}}-E_{\mathrm{f,d}}}{qV_{\mathrm{th}}}\right)}\right) \tag{6.2}$$

with V_{th} as the thermal voltage.

The neglect of QC and the use of 3-D density of states requires an adjustment of the absolute value of the current. This adjustment is found to be different for the DSDT and TE currents and is done through m_{eff}, which is the only adjustable proportionality factor used in the Tsu-Esaki formula. The thermionic emission current density $J_{\mathrm{te}}(y)$ is calculated using the same formula as in (6.1) but with three differences. The integration is performed between E_{m} and infinity for electrons with an adjustment of m_{eff} equal to m_{e} an absolute value of the TE current in agreement with NEGF simulations and 100 % tunneling probability:

$$J_{\mathrm{te}}(y) = \frac{q m_{\mathrm{e}}}{2\pi^2\hbar^3} \int_{E_{\mathrm{m}}}^{\infty} N(E_{\mathrm{x}})\, dE_{\mathrm{x}}. \tag{6.3}$$

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The overall current density $J_{\mathrm{ds}}(y)$ from source to drain is obtained by summing the two densities in (6.1) and (6.3):

$$J_{\mathrm{ds}}(y) = J_{\mathrm{t}}(y) + J_{\mathrm{te}}(y). \tag{6.4}$$

The current for a device with channel width W_{ch} and thickness T_{ch} is determined from the following equation:

$$I_{\mathrm{ds}} = I_{\mathrm{t}} + I_{\mathrm{te}} = W_{\mathrm{ch}} \int_{-\frac{T_{\mathrm{ch}}}{2}}^{\frac{T_{\mathrm{ch}}}{2}} J_{\mathrm{t}}(y) + J_{\mathrm{te}}(y)\, dy. \tag{6.5}$$

To avoid a possible misfit to analytical potential models with decreasing temperature, the conduction band edge used to calculate P_{t} and the corresponding Fermi levels to determine $N(E_{\mathrm{x}})$ are extracted directly from the NEGF simulations.

Figure 6.1(a) illustrates the studied silicon nanosheet (SiNS) FET geometry and Figure 6.1(b) shows the first subband energy of a short-channel device together with a color plot illustrating exemplary the electron energy dependent normalized tunneling and thermionic emission current densities.

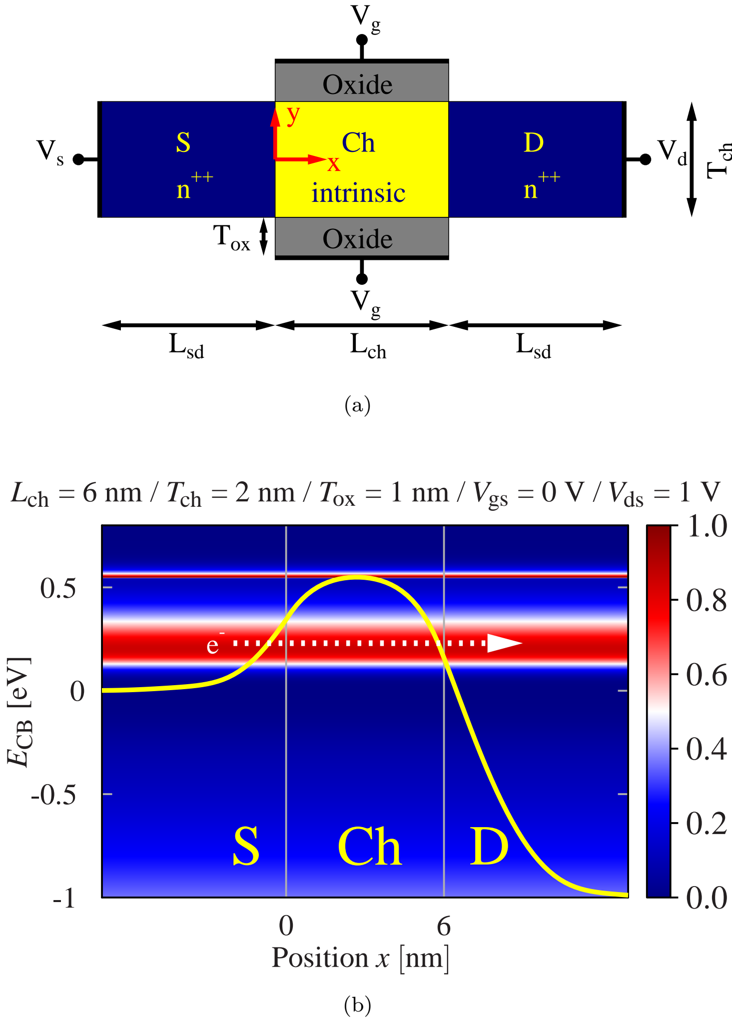

Figure 6.1: (a) Sketch of the SiNS FET under investigation. Source/Drain (S/D) are highly n-doped and the channel (Ch) is undoped with a high-κ gate oxide material of $\varepsilon_r = 22$. (b) First subband energy of the conduction band together with a color plot showing the electron energy dependent normalized tunneling and thermionic emission current densities at an operating temperature $T = 300$ K with S/D doping of $N_{s/d} = 10^{20}$ cm^{-3}.

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6.3 Results and Discussion

First, we would like to understand what causes both the current and the subthreshold swing S_{sth} to saturate with decreasing temperature T as mentioned in [12, 25]. We are using the supply function $N(E_{\mathrm{x}})$ in (6.2) to explain the subthreshold current and swing saturation S_{sth} at low temperatures and the influence on DIBL. Specifically, we focus on the ratio of the supply function at a given temperature T to the same supply function at room temperature $T_0 = 300$ K, and vary the tunneling electron energy E_{x} relative to the Fermi energy $E_{\mathrm{f,s}}$. This is shown in Figure 6.2.

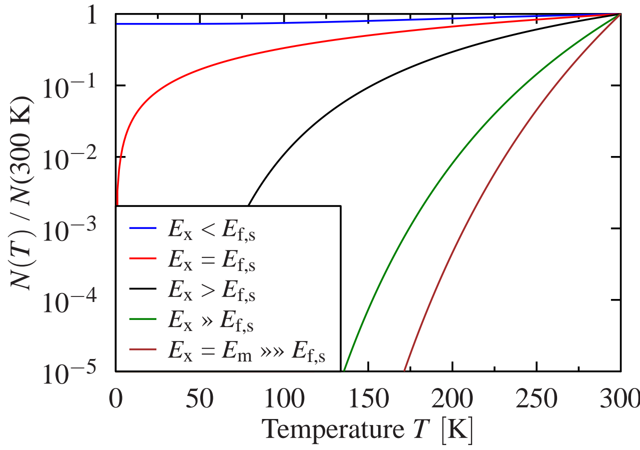
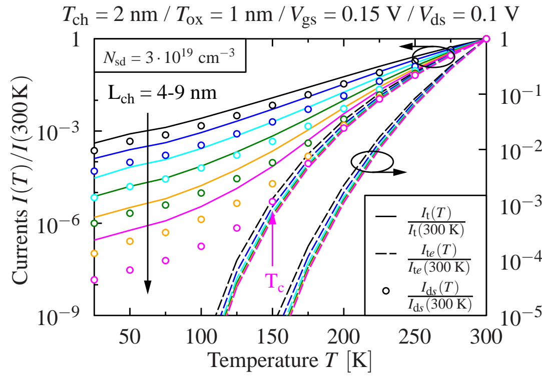
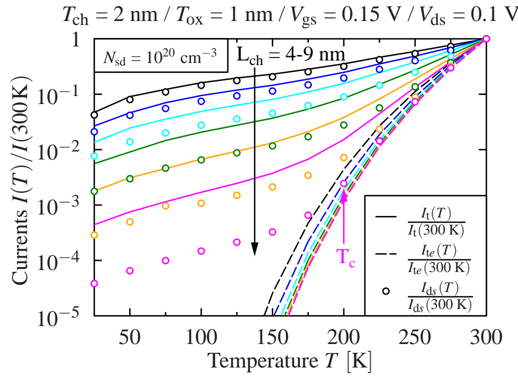


Figure 6.2: Ratio of the supply function at temperature T to the supply function at $T_0 = 300$ K versus the T for different electron energies E_{x}. The following values for E_{x} are used from top to bottom for demonstration purposes: $E_{\mathrm{x}} = 0.114$ eV, $E_{\mathrm{x}} = 0.135$ eV $= E_{\mathrm{f,s}}$, $E_{\mathrm{x}} = 0.179$ eV, $E_{\mathrm{x}} = 0.356$ eV, $E_{\mathrm{x}} = 0.5$ eV $= E_{\mathrm{m}}$.

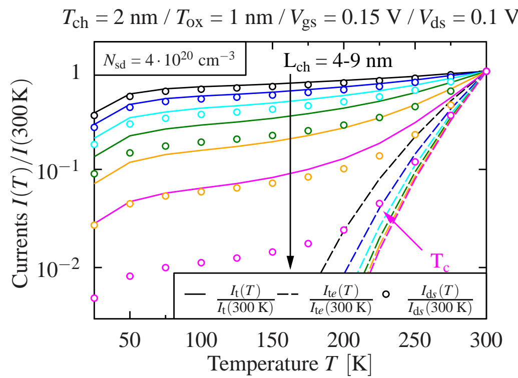
We find that as the temperature drops, the amount of electrons that have the opportunity to cross the channel, whether by tunneling or thermal emission, is relatively stable for energies less than $E_{\mathrm{f,s}}$ and becomes sharply decreasing for energies above $E_{\mathrm{f,s}}$. This means that the immunity to temperature changes depends on whether a large fraction of the electrons crossing the channel $(PN(E_{\mathrm{x}}))$ are distributed well above or around $E_{\mathrm{f,s}}$.



(a)



(b)



(c)

Figure 6.3: Ratio of the modeled OFF currents I_t, I_{te}, I_{ds} at a given operating temperature T to the reference temperature $T_0 = 300$ K plotted against T. For channel lengths L_{ch} between 4 and 9 nm, plots (a), (b) and (c) show the different strength of current saturation due to differences in ions. Here, we also see that the saturation current is more important at higher $N_{s/d}$ doping. The position of T_c is shown just empirically. It indicates when the TE current is overwhelmed by the DSDT current.

In analogy to Figure 6.2, in Figure 6.3 we plot against T at $V_{\rm gs} = 0.15$ V and $V_{\rm ds} = 0.1$ V for the channel lengths from $L_{\rm ch} = 4$ to 9 nm the ratio of the modeled subthreshold currents $I_{\rm t}$, $I_{\rm te}$ and $I_{\rm ds}$ at T to the one at T_0. We see the impact of doping concentration $N_{\rm s/d}$ in these figures. First, we note that the critical temperature $T_{\rm c}$ below which saturation appears shrinks with decreasing $N_{\rm s/d}$. This was to be expected since the range of the potential drops in the source and drain regions, and thus the tunneling length $L_{\rm t}$, increases as $N_{\rm s/d}$ decreases. The rise in $L_{\rm t}$ has a comparable effect on $T_{\rm c}$ as the rise in $L_{\rm ch}$. Significant differences are apparent when looking at the orders of magnitude by which the current decreases. In particular below $T_{\rm c}$, where tunneling becomes dominant over thermal emission, there is strong current saturation for high dopant concentrations, while at lower concentrations the current still decreases by 2 to 3 orders of magnitude. As an example, the temperature dependence of the saturation current for three different doping concentrations $N_{\rm s/d}$ is demonstrated again for the channel length $L_{\rm ch} = 4$ nm in Figure 6.4. We note that current saturation is much less pronounced at smaller doping concentrations. Therefore, at lower doping levels, it is more appropriate to consider the $T_{\rm c}$ value caused by DSDT less as an indicator of current saturation and more as a critical value above which the TE current is overwhelmed by the DSDT current.

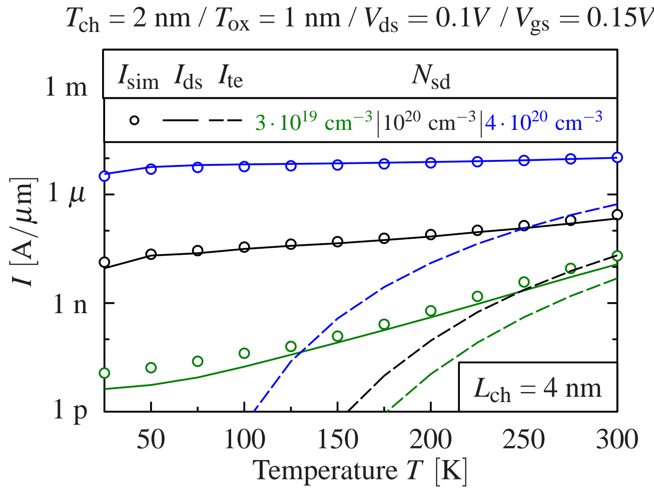


Figure 6.4: OFF current at $V_{\rm gs} = 0.15$ V and $V_{\rm ds} = 0.1$ V versus operating temperature T for three different source/drain doping concentrations $N_{\rm s/d}$. The (dashed) lines represent the modeling results using wavelet approach, while the symbols represent numerical NEGF simulation data. For the chosen channel length $L_{\rm ch} = 4$ nm $I_{\rm t}$ dominates over $I_{\rm te}$.

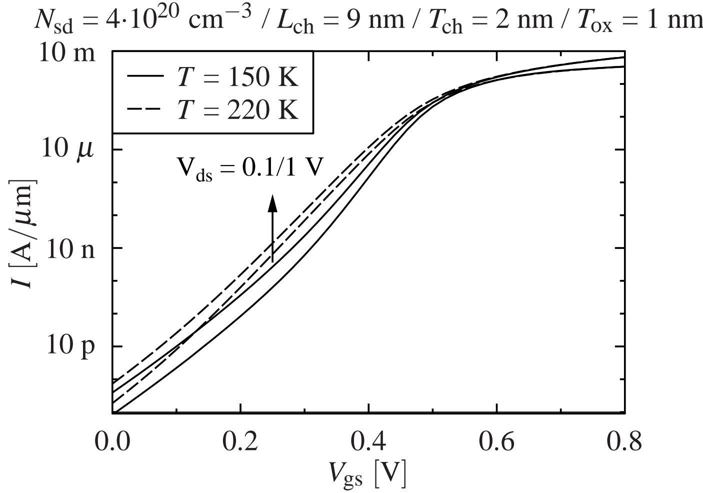
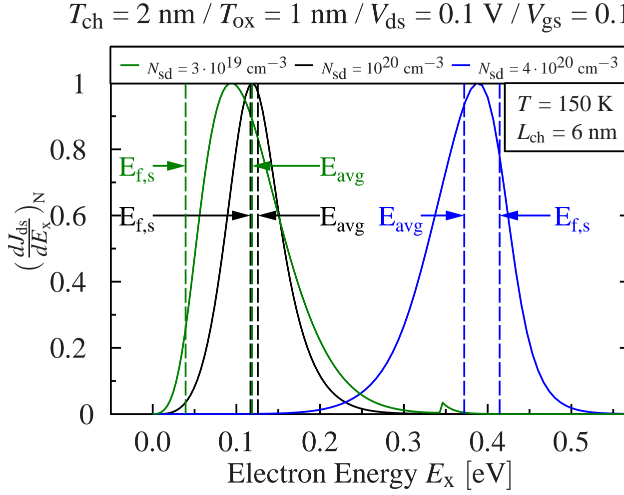


Figure 6.5: Comparison ot the transfer characteristics between the operating temperatures T = 220 K with marginal and T = 150 K with pronounced tunneling current.

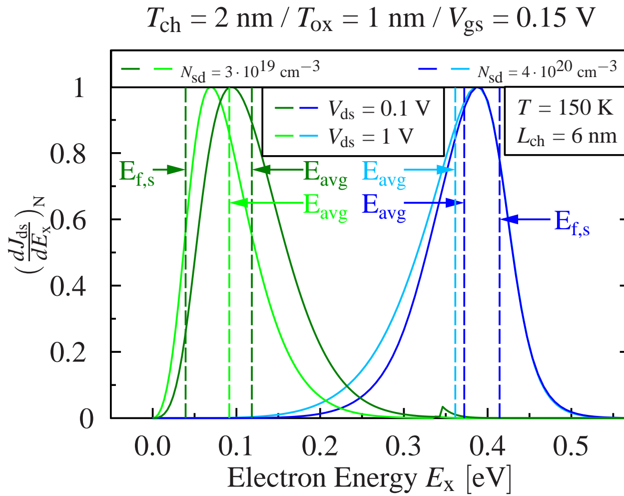
Another point worth mentioning regarding T_c is that the evaluation of when T_c is reached also depends on the gate-source voltage V_{gs} at which the investigation is performed. At room temperature T_0 the thermal emission current I_{te} completely dominates over the tunneling current I_t for channel lengths L_{ch} larger than 9 nm,[23]. Since the subthreshold swing of I_t is always at least as bad or worse than the subthreshold swing of I_{te}, I_t becomes with decreasing temperature noticeable first at low V_{gs} as soon as we are within the measurable current range of about 0.1 pA. Now, let us have a look at the simulation results in Figure 6.5. At very high doping levels ($N_{s/d} = 4 \cdot 10^{20}$ cm^{-3}), for two different temperatures (220 K and 150 K), the transfer characteristics are demonstrated. If T_c is captured at $V_{gs} = 0$ V, the current and swing is already nearly saturated with respect to the temperature. If T_c is captured at $V_{gs} = 0.2$ V the only current and swing in saturation with respect to the temperature is the one at T = 150 K, while at T = 220 K I_{te} is still dominating over I_t.

In the literature, electron tunneling is assumed to be mainly energetically localized in the form of a peak around the Fermi level $E_{f,s}$ [13]. However, this assumption is not correct, at least for doping concentrations with resulting source related Fermi levels $E_{f,s}$ close to or beneath the conduction band edge. The reason is, that the peak position is given by the product of $P_t(E_x) \cdot N(E_x)$ and as already mentioned in [23], the tunneling probability P_t for a rectangular barrier decreases extremely fast near the band edge.

In other words, if the source related Fermi level $E_{f,s}$ is near the conduction band edge those electrons have much less contribution for tunneling compared to electron energies slightly above $E_{f,s}$. This phenomenon is shown in Figure 6.6(a).



(a)



(b)

Figure 6.6: Normalized first derivation of J_{ds} with respect to E_x against E_x. (a) For three different doping levels $N_{s/d}$, the Fermi positions $E_{f,s}$ and the average energy E_{avg} of the electrons contributing to tunneling are highlighted. (b) For the highest and lowest $N_{s/d}$ considered, both E_{avg} at two different Vds are compared respectively.

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For three different doping concentrations the normalized tunneling current density per electron energy is plotted against E_{x} at a gate-source bias V_{gs} where in all three cases the tunneling is dominant over thermionic emission and is measurable.

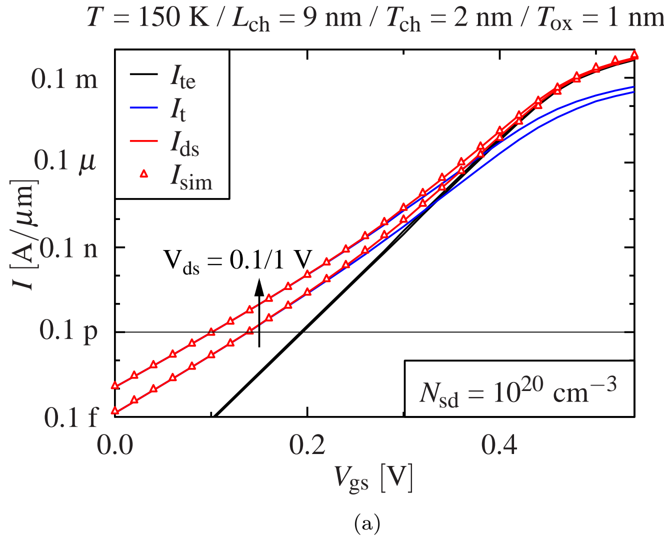
Besides $E_{\mathrm{f,s}}$, the related average energy E_{avg} weighted with its contribution for tunneling is also indicated. This value is supposed to be representative for the entire tunneling process and is given as:

$$E_{\mathrm{avg}} = \frac{m_{\mathrm{eff}} \int_0^{E_{\mathrm{m}}} E_{\mathrm{x}}\, PN(E_{\mathrm{x}})\; dE_{\mathrm{x}} + m_{\mathrm{e}} \int_{E_{\mathrm{m}}}^{\infty} E_{\mathrm{x}}\, N(E_{\mathrm{x}})\; dE_{\mathrm{x}}}{J_{\mathrm{ds}}\, 2\,\pi^2\,\hbar^3/q}. \tag{6.6}$$

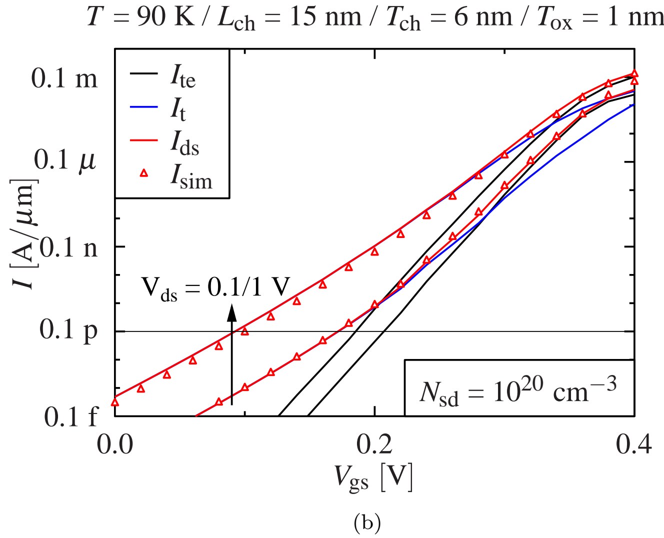
As one can see clearly, for the lowest doping concentration ($N_{\mathrm{s/d}} = 3 \cdot 10^{19}$ cm^{-3}) the amount of electrons tunneling through the barrier with energy $E_{\mathrm{f,s}}$ is quasi not existent. The peak position is obviously higher. In addition, the difference between E_{avg} and $E_{\mathrm{f,s}}$ is much larger compared to the device with the second highest doping level ($N_{\mathrm{s/d}} = 10^{20}$ cm^{-3}). This circumstance together with Figure 6.2 explains furthermore why the current is not saturating at lower doping levels. The blue curve stands for the highest doping concentration with $N_{\mathrm{s/d}} = 4 \cdot 10^{20}$ cm^{-3}. Of course the $E_{\mathrm{f,s}}$ is the highest here but in contrary to the other two cases, E_{avg} is smaller than $E_{\mathrm{f,s}}$. This explains the strong current saturation. In Figure 6.6(b), we investigate the influence of higher V_{ds} on the peak positions and the possible shift of E_{avg}. At very high doping levels, the peak position and E_{avg} show resistance to changes in V_{ds}. Thus, no changes in current and swing saturation behavior can be expected. However, at lower doping levels, the peak position moves towards the Fermi level, so that the distance between $E_{\mathrm{f,s}}$ and E_{avg} decreases noticeably. Thus, at high V_{ds} the current will saturate comparatively more than at small V_{ds}. This has a significant impact on DIBL, which we will examine in more detail at the end of this section.

As already mentioned, I_{t} starts to appear at low V_{gs} and propagates to higher V_{gs} with decreasing temperature. Depending on the device dimensions and the ambient temperature, it is possible to have two different DIBL and S_{sth} values simultaneously in the subthreshold transfer characteristics. This is shown in the Figures 6.7(a) and 6.7(b). The transition between the two regions is clearly evident and also shows that the applied wavelet model provides a superior fit to the simulation results. In addition, Figure 6.7(b) shows that for sufficiently thick channels ($T_{\mathrm{ch}} = 5$ nm) with less QC, even a 15 nm long-channel can provide enough tunneling current in the measurable range and therefore should not be ignored at all. The smooth transition from I_{t} to I_{te} leads to a continuous alignment of both swings and DIBLs with the gate bias. This can be

followed very well on the level of the current densities (see Figure 6.8).



(a)



(b)

Figure 6.7: Double subthreshold swing S_{sth} and DIBL effect: (a-b) Separation of the total modeled subthreshold current I_{ds} (red line) using wavelet approach into the tunneling part I_{t} (blue line) and the thermionic emission part I_{te} (black line) together with the NEGF simulation data (red symbols). The horizontal line represents the beginning of the minimum measurable current level. (a) With and (b) without classical thermionic emission short-channel S_{sth} and DIBL degradation.

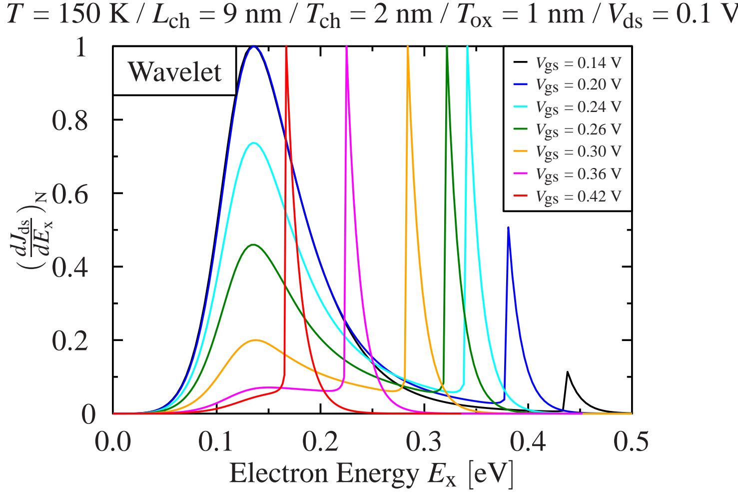


Figure 6.8: Corresponding transition of normalized first derivation of J_{ds} with respect to E_{x} versus E_{x} from tunneling dominance to dominance of thermionic emission with increasing gate bias V_{gs} for the transfer characteristic in Figure 6.7(a).

Lastly, we use the knowledge gained about the control of tunneling by the Fermi energy to interpret the channel length dependent swing and DIBL for different doping levels in respectively three plots (Figures 6.9(a) - 6.9(c) and Figures 6.9(d) - 6.9(f)) with different ambient temperatures, as well as the temperature dependent swing and DIBL for once again in respectively three plots (Figures 6.10(a) - 6.10(c) and Figures 6.10(d) - 6.10(e)) for different channel lengths.

The swing does not only increase due to the reduction of the tunneling length because of the higher doping. The transition from thermionic emission to tunneling current is much steeper at higher doping levels and more pronounced at lower temperatures (Figures 6.9(a) to 6.9(c)). The tunneling induced DIBL also increases with increasing doping concentration, analogous to thermionic emission induced DIBL (Figure 6.9(d)). As the temperature is lowered, a steep transition from thermionic emission to tunneling is present (see Figure 6.9(e)). Thereafter, the slope is more or less constant until the DIBL of thermionic emission would occur. From here on, the DIBL of tunneling adapts to the steepness of thermionic emission and becomes significantly larger with smaller channel length. Further, it can be seen from Figure 6.9(f) that with decreasing temperature the DIBL increases for smaller doping concentrations, so that even the positions swap at T = 75 K. Explanations to this are given later.

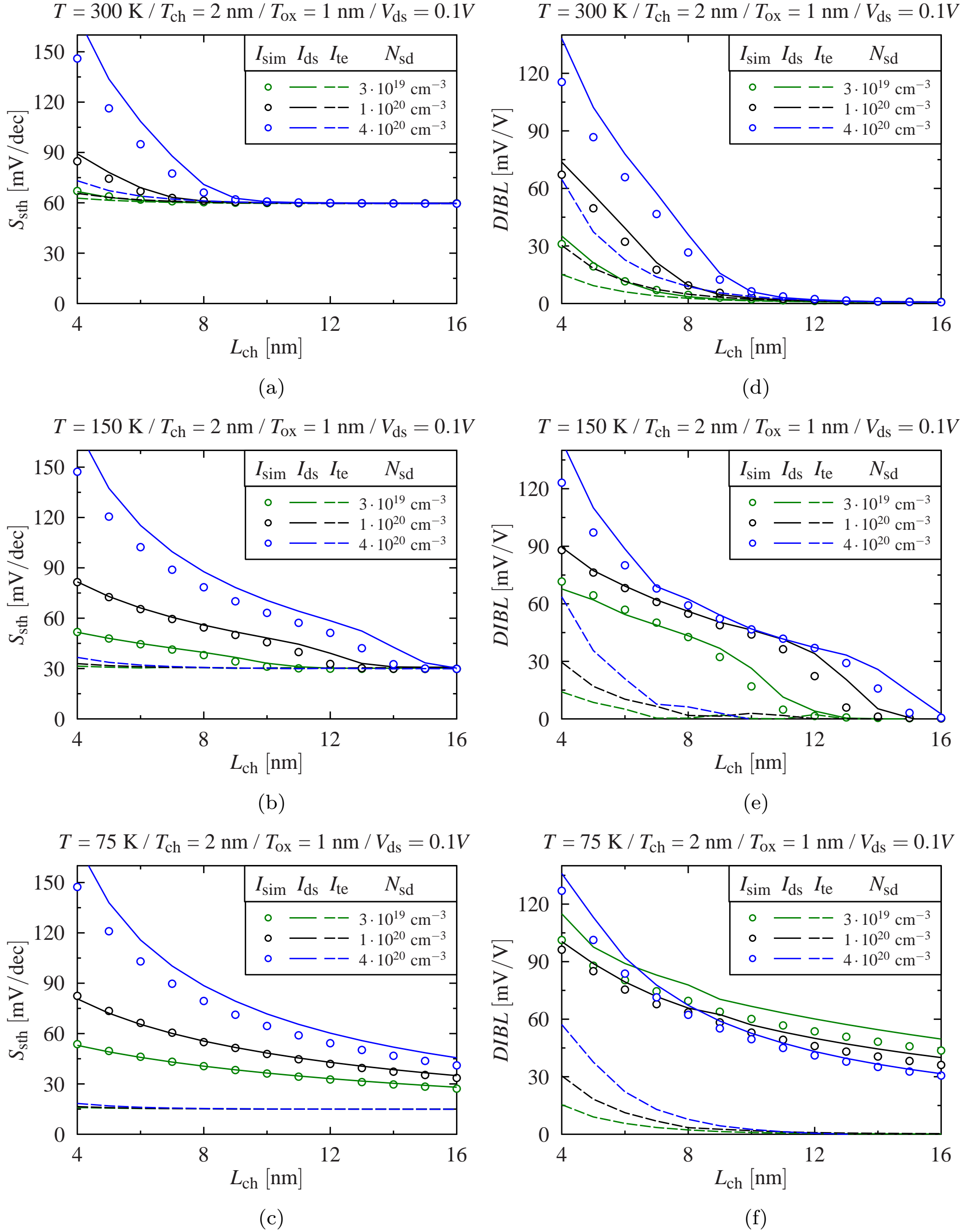


Figure 6.9: Comparison of modeled (lines) and simulated (symbols) S_{sth} (a-c) and DIBL (d-f) using the analytical wavelet and the numerical NEGF approach, respectively, against the channel length L_{ch} between three different doping levels at three different operating temperatures T.

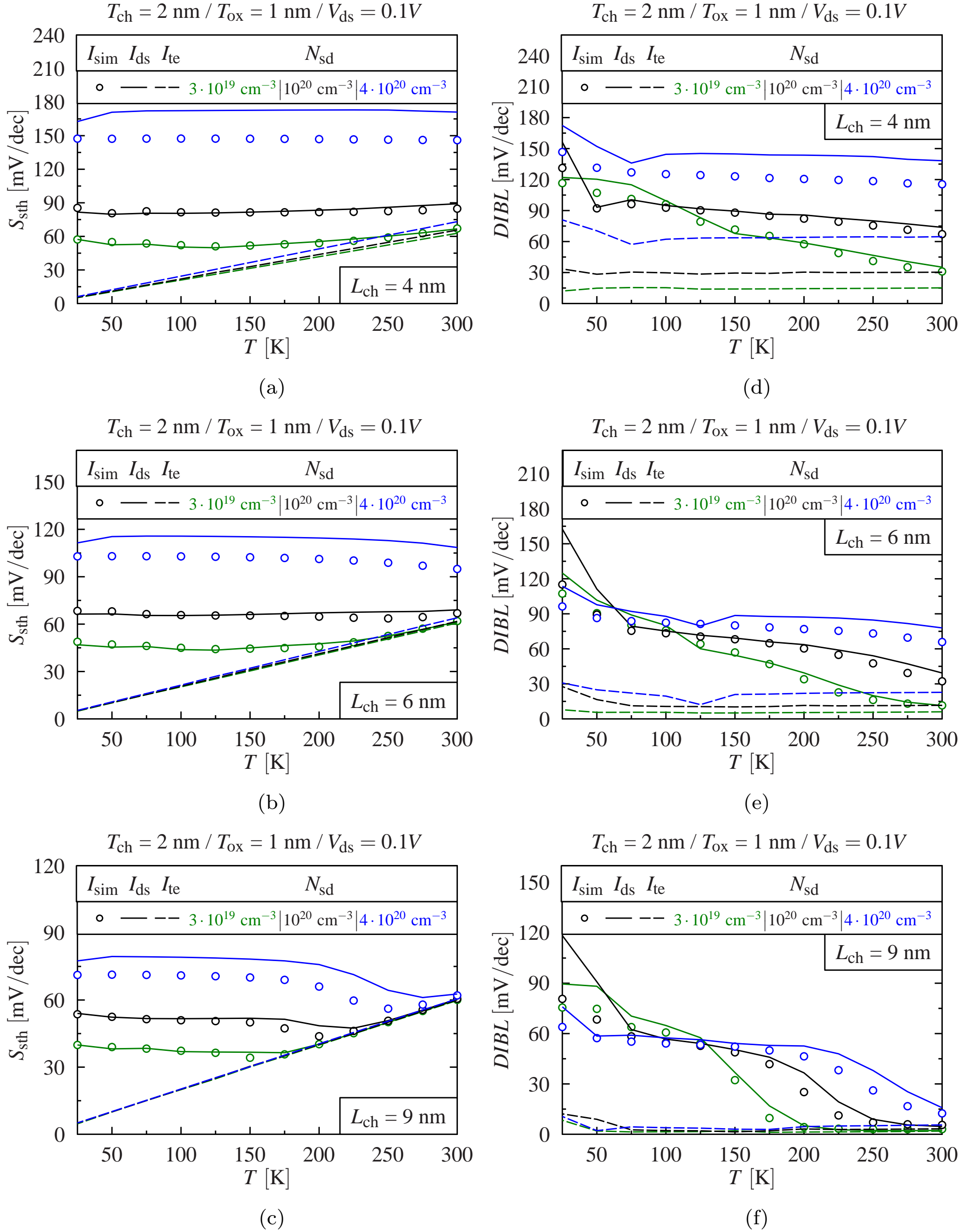


Figure 6.10: Comparison of modeled (lines) and simulated (symbols) S_{sth} (a-c) and DIBL (d-f) using the analytical wavelet and the numerical NEGF approach, respectively, against the operating temperature T between three different doping levels for three different channel length L_{ch}.

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Previously, it was mentioned and explained that at lower doping concentrations, subthreshold current saturation at lower temperature does not occur. The progressive tunneling decrease is not yet comparable to the sharp reduction of the thermionic emission current. The swing is not fully saturating at the critical temperature, but is relatively stable below this (Figures 6.10(a) - 6.10(c)). We expect at extremely low cryogenic temperatures ($T < 25$ K) a forced current and swing saturation since the distance between $E_{\mathrm{f,s}}$ and E_{avg} also has to shrink. Furthermore, it is visible in Figure 6.10(c) that during the transition from thermal emission to tunneling, the swing initially increases again, especially at higher dopant concentrations, before saturation occurs. This is an indication for a larger angle between both current types in the transfer characteristics and a sharper kink.

Returning to the swapping of the DIBL positions with reduction of the temperature, we see in Figures 6.9(d) to 6.9(f) that the DIBL goes into saturation at high doping concentrations. This is not surprising at all because if both the subthreshold current and swing goes into saturation the DIBL has to follow.

The situation is different at lower doping concentrations. The swing is quite stable, but the ongoing current reduction with temperature decrease is smaller at higher drain-source biases V_{ds} than at lower V_{ds}. The reason for the different rate of current reduction with temperature is that a higher V_{ds} brings the peak position together with E_{avg} slightly closer to $E_{\mathrm{f,s}}$ compared to low V_{ds} (see Figure 6.6(b)), thus increasing the insensitivity of the supply function $N(E_{\mathrm{x}})$ to temperature changes.

6.4 Conclusion

In this work, we have analyzed and modeled with the wavelet approach the impact of different doping levels on the subthreshold behavior of ultrashort-channel MOSFETs at cryogenic temperatures down to 25 K. We highlighted the role of the source related Fermi energy $E_{\mathrm{f,s}}$ in the supply function and its energetic distance to the average electron energy E_{avg}, weighted with its contribution for tunneling. The controllability with doping in achieving or not achieving saturation for the current, swing and DIBL are demonstrated. We also clarified that it is more appropriate to use T_{c} to describe a critical temperature below which the TE current is overwhelmed by the DSDT current than to define it as a value below which subthreshold current and swing saturation take place. Further, we showed a swapping in DIBL with decreasing temperature and we also described and explained the existence of two merging DIBL and S_{sth} regions in the I-V characteristics. We conclude that DSDT plays a significant role at cryogenic

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temperatures and might be the most important drawback to achieve extreme steep subthreshold swings. We recommend to keep the doping concentration at least in the source region as low as possible, so that in the best case even $E_{\mathrm{f,s}}$ is below the conduction band edge, resulting in extremely low or vanishing DSDT.

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CHAPTER 7

Overall Conclusions

This doctoral thesis deals with the simulation, modeling and in-depth analysis of the two most promising GAA MOSFET structures of future technology nodes. These are cylindrical NW and SiNS FETs, which are expected to replace the currently market dominating FinFET technology due to the better control of the channel electrostatic potential by the gate electrode surrounding from all sides and the resulting stronger SCE suppression. This change in transistor design is associated with manufacturing difficulties, but it makes further device scaling possible. Therefore, with ongoing scaling and thus the strong presence of SCEs, accurate modeling of NW and SiNS FETs including QMEs becomes ever more important.

In the following, we summarize point by point the key finding of this thesis:

- In the subthreshold regime of ultrascaled NW FETs with intrinsic or lightly doped channels, the height of the electrostatic potential (Φ_{m}) along the channel at any distance from the gate can be mimicked by DG potential models by using an appropriate scalable equivalent channel length. Since the shape of the potential barrier through the channel thickness can be parabolically approximated, the accurate determination of the surface and center potential barrier heights (Φ_{S} & Φ_{C}) using two equivalent DG channel lengths ($L_{\mathrm{DG}}^{\mathrm{S}}$ & $L_{\mathrm{DG}}^{\mathrm{C}}$) is sufficient for further charge and current calculations. The scalability of $L_{\mathrm{DG}}^{\mathrm{S}}$ and $L_{\mathrm{DG}}^{\mathrm{C}}$ is verified by TCAD Sentaurus simulations.

- The inversion charge in NW FETs is calculated by integration over the density of free electrons within the channel cross section in polar coordinates using Φ_{S} and Φ_{C} obtained with the equivalent DG potential model. This charge, which

includes the SCEs, is inserted into a charge-based current model for long-channel NW FETs derived from a current model for long-channel DG FETs.

- The adapted 2-D DG analytical potential and current model enables the prediction of the subthreshold swing and DIBL behavior of cylindrical short-channel NW FETs.

- QMEs are not negligible when device dimensions are in the single-digit nanometer range. TCAD simulations have shown that the influence of QC on the current and threshold voltage in a cylindrical NW FET is equivalent to that in a DG FET when the channel thickness of the NW FET is larger by a factor of 1.53. This means that in NW FETs the unwanted QC has a stronger influence and therefore already occurs at thicker channel thicknesses. The modified DG model is extended by the impact of QC by considering the additional bandgap widening in the calculation of an effective intrinsic charge carrier concentration and also in the calculation of the threshold voltage (V_{T}) by increasing the inversion potential (Φ_{i}).

- DSDT current is simulated and modeled for DG FETs due to the lack of suitable simulation tools that use the NEGF approach for NW FETs. Unlike QC, DSDT provides an increase in subthreshold leakage current and a degradation of swing and DIBL, but a negligible current increase in the ON-state of the device.

- There are essentially two major challenges in modeling the tunneling current. The first is the correct determination of the electron energy dependent tunneling probability ($P_{\mathrm{t}}\left(E_{\mathrm{x}}\right)$) and the second is the analytical calculation of the tunneling current density (J).

- The modeling results, where P_{t} is determined using the new wavelet approach, are in very good agreement with the NEGF-based NanoMOS simulation data and differ from the Synopsys TCAD Sentaurus simulation data, which are based on the widely used WKB approximation. In the wavelet approach, an equivalent rectangular barrier height is calculated for each electron energy and treated as such, so that the exact analytical formula for the 1-D tunneling probability through a rectangular barrier can be used. The exact tunneling formula for rectangular barriers describes the decrease in P_{t} near E_{CB} clearly with more accuracy than the WKB-based P_{t}.

- DSDT analysis has shown that due to the Fermi-Dirac distribution, the main current contribution is provided by electrons tunneling from outside the channel

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directly from the source into the drain region, although P_t is very small due to larger tunneling length and barrier height. Hence, a four-piece parabolic approximation of E_{CB} became necessary to derive a simplified closed form formula for the energy dependent tunneling length ($L_t(E_x)$), which is used in the calculation of P_t.

- Since the integrand $PN(E_x)$ in the Tsu-Esaki tunneling formula is not integrable in closed form, an analytical approach named QCM is derived. This approach greatly reduces the computational effort, but requires a Newton iteration in the calculation of the energy with maximum contribution to the tunneling current. In addition, $PN(E_x)$ is calculated at 3 equidistant nodes, which helps to approximate the integral by linear interpolation. This improves the numerical efficiency required for compact models. Furthermore, the obtained numerical stability fulfills the requirement to use the compact model for circuit simulations.

- For compact modeling, it is sufficient to determine the tunneling current along the center and surface of the channel. The intermediate region can be accurately approximated with a Gaussian function. This also reduces the computational effort enormously.

- Further detailed analysis based upon the model has shown that the statement below which channel length (L_{ch}) the TE current is overwhelmed by the DSDT current depends, besides L_{ch} itself, in particular on three parameters. These are the ambient temperature (T), the doping concentrations ($N_{s/d}$), and the gate-to-source bias (V_{gs}).

- The critical temperature (T_c) is redefined as the temperature below which tunneling dominates the TE current below a given V_{gs}. Above this specific V_{gs} and below V_T the TE current continues to dominate. This explains the possible coexistence of two smoothly merging subthreshold swings and DIBLs at temperatures around T_c. Further reduction of T leads to complete dominance of the DSDT current in the subthreshold region.

- The DSDT current is much more resistant to temperature changes compared to TE current, so that at cryogenic temperatures below T_c, the expected extremely steep subthreshold swing according to the Boltzmann limit of the TE current is hindered by the swing of the DSDT current.

- The strength of the subthreshold current, swing, and DIBL saturation due to DSDT with decreasing T is found to depend strongly on the source related doping

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concentration (N_{s}). At high N_{s}, where the related Fermi level ($E_{\mathrm{f,s}}$) is significantly far from E_{CB} and close to or above the average electron energy (E_{avg}), the current, swing, and DIBL saturation is strong. Whereas at lower N_{s}, where $E_{\mathrm{f,s}}$ is closer to E_{CB} and well below E_{avg}, the DIBL and current saturation is not present and the swing shows an extremely slight increase below T_{c}.

- Furthermore, lower doping ultimately leads to a comparatively smaller value for T_{c} also because of the increase in tunneling length and the resulting decrease in tunneling current compared to the TE current.
- Ultrashort-channel MOSFETs with sub-10-nm gate length showing DSDT are rarely fabricated yet. Therefore, the findings from temperature and doping analysis are based on the comparison of model results with NEGF simulation data and have not yet been verified with measurement data.
- In addition, the wavelet approach does not consider the electron interference effects on reflection of electron waves from the potential barrier. Such interference phenomena occur at electron energies greater than the barrier height. This additional QME can be included in the compact model in future works.

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