CHARGE-BASED COMPACT MODELING OF CAPACITANCES AND LOW-FREQUENCY NOISE IN ORGANIC THIN-FILM TRANSISTORS

Jakob Simon Leise

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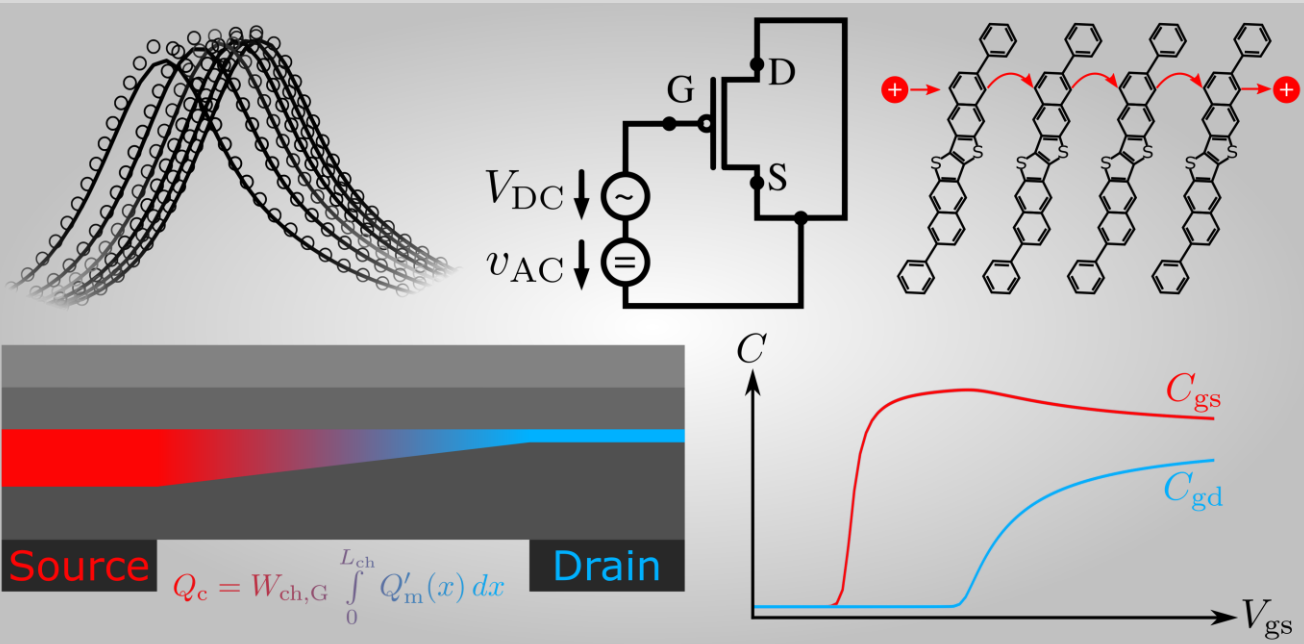
Charge-Based Compact Modeling of Capacitances and Low-Frequency Noise in Organic Thin-Film Transistors

JAKOB SIMON LEISE



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Jakob Simon Leise

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DOCTORAL THESIS

Supervised by Prof. Dr. Benjamín Iñíguez
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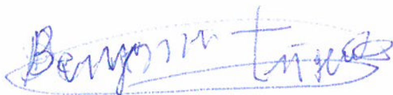

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Jakob Simon Leise

Abstract

Organic thin-film transistors are promising candidates for novel electronics applications due to the possibility of fabricating organic electronic devices at low temperatures on flexible substrates like plastic or paper. This doctoral thesis deals with the development of a charge-based compact model for the description of the capacitive behavior and the low-frequency noise in organic thin-film transistors. Based on an existing DC model, expressions for the total charges under quasistatic operation conditions are derived. Non-quasistatic effects are captured by different methods such as the channel-segmentation approach or frequency-dependent scaling functions of the areas in the transistor where charges are calculated. The model for the total charges is verified by capacitance measurements of a staggered organic TFT and by numerical simulations of organic TFTs in the staggered and coplanar architectures using the device simulator Sentaurus TCAD. The non-quasistatic models are verified by frequency-dependent admittance measurements of a staggered transistor and by scattering-parameter measurements of coplanar and staggered transistors. The compact model is implemented in the hardware description language Verilog-A and the simulation of a differential amplifier is compared to measurements which shows a good agreement. The noise model is verified by measurements of staggered organic thin-film transistors and by TCAD simulations. The compact model shows an overall good agreement and flexibility with respect to the device architecture (e.g. staggered or coplanar) and the used materials.

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Für Katja

"Viel zu lernen du noch hast."
Meister Yoda

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Conferences

- Jakob Leise, Jakob Prüfer, Aristeidis Nikolaou, Ghader Darbandy, Hagen Klauk, Benjamín Iñíguez and Alexander Kloes "Macromodel for AC and Transient Simulations of Organic Thin-Film Transistor Circuits Including Nonquasistatic Effects," in *ESSDERC/ESSCIRC, France (Virtual)*, 2021, Conference Proceedings published in *IEEE Transactions on Electron Devices*, vol. 67, issue 11, pp. 4672–4676, Nov. 2020.

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List of Symbols

Latin Alphabet

Symbol	Description	Unit
$A^{\star}$	Effective Richardson constant	$[\mathrm{A\,m^{-2}\,K^{-2}}]$
A_{AC}	Amplification of the differential amplifier	[dB]
A_{v}	Fitting parameter of the model for the temperature-dependent threshold-voltage shift	[V]
$a_{\mathrm{f}}...f_{\mathrm{f}}$	Coefficients for the polynomial smoothing function for the case distinction of the total charges around $V_{\mathrm{ds}} = 0\,\mathrm{V}$	[−]
B_{v}	Fitting parameter of the model for the temperature-dependent threshold-voltage shift	[V]
C	Capacitance	[F]
C'_{diel}	Gate dielectric capacitance per gate area	$[\mathrm{F\,cm^{-2}}]$
C_1	Auxiliary constant during the derivation of the decoupling of the sub-threshold swing from the mobility	[A]
C'_{ch}	Channel charge capacitance	$[\mathrm{F\,cm^{-2}}]$
$C_{\mathrm{diel,d}}$	Capacitance of the gate dielectric in the gate-to-drain overlap region of a staggered OTFT	[F]
$C_{\mathrm{diel,s}}$	Capacitance of the gate dielectric in the gate-to-source overlap region of a staggered OTFT	[F]
C_{dd}	Drain-drain capacitance	[F]
C_{dg}	Drain-gate capacitance	[F]
C_{ds}	Drain-source capacitance	[F]
C_{gd}	Gate-drain capacitance	[F]
C_{gg}	Gate-gate capacitance	[F]

C_{gs}	Gate-source capacitance	[F]
C_{load}	Load capacitance at the output of the differential amplifier	[F]
$C_{\mathrm{osc,d}}$	Capacitance of the depleted organic semiconductor in the gate-to-drain overlap region of a staggered OTFT	[F]
$C_{\mathrm{osc,s}}$	Capacitance of the depleted organic semiconductor in the gate-to-source overlap region of a staggered OTFT	[F]
C_{scale}	Fitting function for the scaling of the charges in fringe regions	[−]
C_{scale2}	Fitting function for the scaling of the charges in the channel and the overlap regions	[−]
$C_{\mathrm{scale,high}}$	Value that C_{scale} assumes at very high frequencies	[−]
$C_{\mathrm{scale2,high}}$	Value that C_{scale2} assumes at very high frequencies	[−]
$C_{\mathrm{scale,low}}$	Value that C_{scale} assumes at very low frequencies	[−]
$C_{\mathrm{scale2,low}}$	Value that C_{scale2} assumes at very low frequencies	[−]
C_{sd}	Source-drain capacitance	[F]
C_{sg}	Source-gate capacitance	[F]
C_{ss}	Source-source capacitance	[F]
c_1	Constant in the LCAO theory	[−]
c_2	Constant in the LCAO theory	[−]
c_{min}	Auxiliary capacitance that Cadence Virtuoso connects between each node and ground	[F]
d_{B}	Distance from the gate dielectric to the position where the representative barrier height is extracted	[m]
d_{fing}	Distance between two fingers in a multi-finger OTFT	[m]
d_{m}	Thickness of the accumulation channel of the OTFT	[m]
dV	Voltage drop along the channel of the transistor	[V]
dV_{g}	Change of the gate voltage with respect to a point in the channel	[V]
E	Energy	[eV]
$E_{0,\mathrm{DOS}}$	Center position of the Gaussian DOS	[eV]
E_{a}	Activation energy	[eV]
E_{C}	Conduction band energy	[eV]
E_{F}	Fermi energy	[eV]
E_{g}	Band gap energy	[eV]
E_{HOMO}	Energy of the HOMO level	[eV]

E_{LUMO}	Energy of the LUMO level	[eV]
E_{sb}	Electric field at the Schottky barrier	[V m^{-1}]
E_{V}	Valence band energy	[eV]
E_{μ}	Energy at which the states are regarded as mobile states	[eV]
F	Electric field in the TCAD simulations	[V m^{-1}]
$f(E)$	Fermi distribution function	[−]
$f_{\mathrm{poly}}(V_{\mathrm{ds}})$	Polynomial function for the switching of the total charges around $V_{\mathrm{ds}} = 0\,\mathrm{V}$	[−]
f	Frequency	[Hz]
f_{T}	Transit frequency	[Hz]
G	Conductance	[S]
$G_{\mathrm{ch}}(x)$	Local channel conductance in a transistor	[S]
G_{dg}	Drain-gate conductance	[S]
G_{gd}	Gate-drain conductance	[S]
G_{gg}	Gate-gate conductance	[S]
G_{gs}	Gate-source conductance	[S]
G_{d}	Conductance of the partial transistor closer to the drain terminal	[S]
G_{md}	Local transconductance of the transistor at the drain end of the channel	[S]
G_{ms}	Local transconductance of the transistor at the source end of the channel	[S]
G_{s}	Conductance of the partial transistor closer to the source terminal	[S]
$g_{\mathrm{decision}}(V_{\mathrm{ds}})$	Decision function for the case distinction of the total charges around $V_{\mathrm{ds}} = 0\,\mathrm{V}$	[−]
g_{min}	Auxiliary conductance that Cadence Virtuoso connects between each node and ground	[S]
g_{m}	Transconductance of the transistor	[S]
H	Hamilton operator	[J]
h	Planck constant	[J s]
$\hbar$	Reduced Planck constant	[J s]
h_{21}	Small-signal current gain of a transistor	[−]
I_{c}	Current flowing through a capacitor	[A]

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$I_{\mathrm{D,d}}$	Current through the Schottky barrier at the drain-to-semiconductor junction	[A]
I_{d}	DC current flowing at the drain terminal of the transistor	[A]
$I_{\mathrm{d,DC}}$	Same as I_d	[A]
I_{g}	DC current flowing at the gate terminal of the transistor	[A]
I_{s}	DC current flowing at the source terminal of the transistor	[A]
$I_{\mathrm{s,DC}}$	Same as I_s	[A]
I_{ds}	Drain-source current	[A]
$I_{\mathrm{ds,off}}$	Drain-source current under sub-threshold operation conditions	[A]
$I_{\mathrm{s,d}}$	Reverse-bias saturation current of the drain-to-semiconductor Schottky barrier	[A]
$I_{\mathrm{s,s}}$	Reverse-bias saturation current of the source-to-semiconductor Schottky barrier	[A]
I_{sp}	Specific current	[A]
i_{d}	Small-signal current flowing at the drain terminal of the transistor	[A]
i_{ds}	Normalized drain-source current of the transistor	[−]
i_{g}	Small-signal current flowing at the gate terminal of the transistor	[A]
i_{j}	Small-signal current flowing at a terminal with the index j	[A]
i_{s}	Small-signal current flowing at the source terminal of the transistor	[A]
K_1	Auxiliary parameter in the derivation of the carrier-number-fluctuation noise model	[$\mathrm{A^2\,Hz^{-1}\,m^{-1}}$]
K_2	Auxiliary parameter in the derivation of the carrier-number-fluctuation noise model	[$\mathrm{A^2\,Hz^{-1}}$]
K_3	Auxiliary parameter in the derivation of the bulk-mobility-fluctuation noise model	[$\mathrm{A^2\,Hz^{-1}}$]
K_{fit}	Fitting parameter for the short-channel capacitance model	[−]
K_{r}	Fitting parameter for the short-channel capacitance model	[−]
k_{B}	Boltzmann constant	[$\mathrm{J\,K^{-1}}$]
L_{ch}	Channel length	[m]
L_{inj}	Injection Length	[m]
$L_{\mathrm{ov,GD}}$	Gate-to-drain overlap length	[m]

$L_{\mathrm{ov,GS}}$	Gate-to-source overlap length	[m]
L_{T}	Transfer length	[m]
l	Secondary quantum number of an atom	[−]
m	Magnetic quantum number of an atom	[−]
m_{particle}	Mass of a particle	[kg]
N	Number of transistor connected in the channel-segmentation model	[−]
$N_{0,\mathrm{trap}}$	Total number of Gaussian-distributed deep traps in the bandgap of the OSC	[$\mathrm{cm^{-3}\,eV^{-1}}$]
$N'(x)$	Number of charge carriers per gate area at position x in the channel	[$\mathrm{cm^{-2}}$]
N_{fing}	Number of source/drain electron pairs in a multi-finger OTFT	[−]
N_{st}	Equivalent density of shallow traps	[$\mathrm{cm^{-3}}$]
N'_{t}	Density of traps per energy and volume in the gate dielectric used for the noise calculation	[$\mathrm{eV^{-1}\,cm^{-3}}$]
N'_{tc}	Number of trapped charge carriers per gate area	[$\mathrm{cm^{-2}}$]
$N_{\mathrm{t,DOS}}$	Maximum number of states in a Gaussian distribution	[$\mathrm{cm^{-3}}$]
$N'_{\mathrm{t,max}}$	Maximum number of filled deep bulk and interface traps per gate area in the DC model	[$\mathrm{cm^{-2}}$]
N_{v}	Effective density of states in a standard square-root distribution	[$\mathrm{cm^{-3}}$]
n	Main quantum number of an atom	[−]
n_{h}	Number of accumulated holes per volume in the organic semiconductor	[$\mathrm{cm^{-3}}$]
p_{scale}	Exponent of the denominator of the function C_{scale}	[−]
p_{scale2}	Exponent of the denominator of the function C_{scale2}	[−]
Q_{b}	Total charges associated with the bulk region of a transistor (irrelevent for TFTs)	[A s]
Q_{c}	Total charges in the channel of the transistor	[A s]
$Q_{\mathrm{c,final}}$	Total charges in the channel of the transistor with a smooth transition around $V_{\mathrm{ds}} = 0\,\mathrm{V}$	[A s]
$Q_{\mathrm{c,nonzero}}$	Total charges in the channel of the transistor if $V_{\mathrm{ds}} \neq 0\,\mathrm{V}$	[A s]
$Q_{\mathrm{c,zero}}$	Total charges in the channel of the transistor if $V_{\mathrm{ds}} = 0\,\mathrm{V}$	[A s]
$Q'_{\mathrm{c}}(x)$	Charge density per gate area in the channel of the transistor	[$\mathrm{A\,s\,cm^{-2}}$]

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Q_{d}	Total charges associated with the drain terminal of the transistor	[A s]
$Q_{\mathrm{d,final}}$	Total charges associated with the drain terminal of the transistor with a smooth transition around $V_{\mathrm{ds}} = 0\,\mathrm{V}$	[A s]
$Q_{\mathrm{d,nonzero}}$	Total charges associated with the drain terminal of the transistor if $V_{\mathrm{ds}} \neq 0\,\mathrm{V}$	[A s]
$Q_{\mathrm{d,zero}}$	Total charges associated with the drain terminal of the transistor if $V_{\mathrm{ds}} = 0\,\mathrm{V}$	[A s]
$Q_{\mathrm{ex,D,copl}}$	Total extrinsic charges associated with the drain terminal of a coplanar transistor	[A s]
$Q_{\mathrm{ex,S,copl}}$	Total extrinsic charges associated with the source terminal of a coplanar transistor	[A s]
$Q_{\mathrm{ex,D,stag}}$	Total extrinsic charges associated with the drain terminal of a staggered transistor	[A s]
$Q_{\mathrm{ex,D,stag,new}}$	Same as $Q_{\mathrm{ex,D,stag}}$ but including the influence of the new charge partitioning	[A s]
$Q_{\mathrm{ex,S,stag}}$	Total extrinsic charges associated with the source terminal of a staggered transistor	[A s]
$Q_{\mathrm{ex,S,stag,new}}$	Same as $Q_{\mathrm{ex,S,stag}}$ but including the influence of the new charge partitioning	[A s]
Q_{g}	Total charges opposing the channel charge at the gate	[A s]
$Q'_{\mathrm{i}}(x)$	Density of inversion charges per gate area in the channel of a conventional MOSFET	[A s cm^{-2}]
Q_{i}	Total charges associated with the terminal with index i	[A s]
Q_{j}	Total charges associated with the terminal with index j	[A s]
Q'_{m}	Charge density per gate area	[A s cm^{-2}]
$Q'_{\mathrm{m}}(x)$	Charge density per gate area at a position x in the channel	[A s cm^{-2}]
Q'_{ms}	Charge density per gate area at the source end of the channel	[A s cm^{-2}]
$Q'_{\mathrm{ms,off}}$	Charge density per gate area at the source end of the channel under sub-threshold operation conditions	[A s cm^{-2}]
Q'_{md}	Charge density per gate area at the drain end of the channel	[A s cm^{-2}]
$Q'_{\mathrm{md,off}}$	Charge density per gate area at the drain end of the channel under sub-threshold operation conditions	[A s cm^{-2}]
$Q'_{\mathrm{md,barr}}$	Charge density per gate area at the drain end of the channel taking into account the contact voltage drop	[A s cm^{-2}]

Q_{s}	Total charges associated with the source terminal of the transistor	[A s]
$Q_{\mathrm{s,final}}$	Total charges associated with the source terminal of the transistor with a smooth transition around $V_{\mathrm{ds}} = 0\,\mathrm{V}$	[A s]
$Q_{\mathrm{s,nonzero}}$	Total charges associated with the source terminal of the transistor if $V_{\mathrm{ds}} \neq 0\,\mathrm{V}$	[A s]
$Q_{\mathrm{s,zero}}$	Total charges associated with the source terminal of the transistor if $V_{\mathrm{ds}} = 0\,\mathrm{V}$	[A s]
Q_{sp}	Specific charge density	[$\mathrm{A\,s\,cm^{-2}}$]
Q'_{t}	Density of trapped charge carriers per gate area	[$\mathrm{A\,s\,cm^{-2}}$]
q	Elementary charge	[A s]
q_{c}	Normalized charge density per gate area in the channel region of the transistor	[−]
q_{d}	Normalized charge density per gate area at the drain end of the channel	[−]
q_{m}	This is the same as q_c	[−]
q_{s}	Normalized charge density per gate area at the source end of the channel	[−]
$R \cdot W$	Width-normalized total resistance between drain and source of a transistor	[Ω cm]
$R_{\mathrm{n,l,m}}(r)$	Radial component of the wave function	[$\mathrm{m^{-3/2}}$]
R_{c}	Contact resistance in the TCAD simulation	[Ω]
R_{contact}	Ohmic component of the contact resistance in the model	[Ω]
R_{C}	Contact resistance as determined by the TLM analysis	[Ω]
R_{CS}	Resistance for self-stabilization in a differential amplifier	[Ω]
$R_{\mathrm{C}} \cdot W$	Width-normalized total contact resistance of a transistor	[Ω cm]
R_{D}	Series resistance of each of the transistors in the differential pair	[Ω]
R_{noise}	Auxiliary factor during the derivation of the noise model	[−]
$R_{\mathrm{sb,s}}$	Contact resistance due to the Schottky barrier at the source	[Ω]
R_{sheet}	Sheet resistance of the semiconductor	[Ω]
r	Radius	[m]
S_{300}	Observable subthreshold swing at $\mathrm{T} = 300\,\mathrm{K}$	[mV/dec]

$S_{\Delta I_{nD}^2}$	Total power spectral density of the drain current noise as the integral over $S_{\delta I_{nD}^2}$. It is in principle the same as $S_{I_d^2}$.	$[A^2\,Hz^{-1}]$
$S_{\delta I_n^2}$	Power spectral density of the local noise current source in the transistor channel	$[A^2\,Hz^{-1}]$
$S_{\delta I_{nD}^2}$	Power spectral density of the contribution of the local noise source to the total drain current noise	$[A^2\,Hz^{-1}]$
$S_{\delta Q_t^2}$	Power spectral density of the fluctuation of the charge carriers	$[A^2s^2/m^4/Hz]$
$S_{I_d^2}$	Power spectral density of the total drain current noise	$[A^2\,Hz^{-1}]$
S_{meas}	Measured sub-threshold swing extracted from transfer curves	[mV/dec]
S_{new}	New subthreshold swing calculated for a specific temperature	[mV/dec]
S_{obs}	Observable sub-threshold swing which the model really exhibits	[mV/dec]
S_{sth}	Sub-threshold swing of the model (non-compensated)	[mV/dec]
$S_{V_{fb}}$	Power spectral density of the fluctuation of the flatband voltage	$[V^2\,Hz^{-1}]$
s	Spin quantum number of an atom	[–]
T	Temperature	[K]
T_{new}	New temperature at which the new subthreshold swing is calculated	[K]
t	Time	[s]
t_{diel}	Thickness of the gate dielectric	[m]
t_{osc}	Thickness of the organic-semiconductor layer	[m]
V	Potential energy of a system	[eV]
V_c	Voltage drop across a capacitor	[V]
V_{ch}	Channel voltage	[V]
V_d	Potential at the drain electrode	[V]
$V_{d,contact}$	Explicitly calculated voltage drop across all contact elements at the drain	[V]
V_{dd}	Supply voltage for the differential amplifier	[V]
V_{ds}	Drain-source voltage	[V]
$V_{ds,V_{sbd,sat}}$	Maximum voltage drop over the drain-to-semiconductor Schottky barrier	[V]
V_{dsx}	Auxiliary voltage for the inclusion of the output-conductance effect	[V]
V_{fb}	Flat-band voltage	[V]

V_{g}	Potential at the gate electrode	[V]
V_{gd}	Gate-drain voltage	[V]
$V_{\mathrm{gd'}}$	Gate-drain voltage of the inner transistor comprising contact resistances	[V]
V'_{gd}	Auxiliary voltage for the limitation of the voltage drop across the series connection of capacitances at the gate-to-drain overlap region of a staggered OTFT	[V]
V_{gs}	Gate-source voltage	[V]
$V_{\mathrm{gs'}}$	Gate-source voltage of the inner transistor comprising contact resistances	[V]
V'_{gs}	Auxiliary voltage for the limitation of the voltage drop across the series connection of capacitances at the gate-to-source overlap region of a staggered TFT	[V]
V_{iCM}	Common-mode input voltage for both transistors of the differential pair	[V]
$V_{\mathrm{i+}}$	Input voltage at one of the transistors in the differential pair	[V]
$V_{\mathrm{i-}}$	Input voltage at the other transistor in the differential pair	[V]
V_{j}	Potential at the transistor terminal with index j	[V]
V_{odr}	Gate-overdrive voltage	[V]
$V_{\mathrm{0+}}$	Output voltage at one of the transistors in the differential pair	[V]
$V_{\mathrm{0-}}$	Output voltage at the other transistor in the differential pair	[V]
V_{p}	Pinch-off voltage	[V]
V_{s}	Potential at the source electrode	[V]
$V_{\mathrm{sb,d}}$	Voltage drop across the drain-to-semiconductor Schottky barrier	[V]
$V_{\mathrm{sb,s}}$	Estimated voltage drop across the source-to-semiconductor Schottky barrier	[V]
$V_{\mathrm{s,contact}}$	Explicitly calculated voltage drop across all contact elements at the source	[V]
V_{th}	Thermal voltage	[V]
V_{T0}	Threshold voltage	[V]
V_{x}	Channel voltage at position x	[V]
v_{AC}	Superimposed small-signal voltage at the differential amplifier	[V]
v_{ds}	Small-signal component of the drain-source voltage	[V]

v_{gs}	Small-signal component of the gate-source voltage	[V]
v_{particle}	Velocity of a particle	[m s^{-1}]
W_{ch}	Channel width of the simple model	[m]
$W_{\mathrm{ch,eff}}$	Effective channel width including the effect of fringe currents	[m]
$W_{\mathrm{ch,G}}$	Total gate width of the transistor including all electrodes and fringe regions	[m]
$W_{\mathrm{ch,SD}}$	Sum of the geometric finger widths of a multi-finger OTFT	[m]
W_{contact}	Width of one single source/drain contact	[m]
$w_{\mathrm{d}}(x)$	Weighting function for the charges associated with the drain	[–]
w_{ovl}	Symmetrical fringe width beyond the first and the last finger of an OTFT	[m]
$w_{\mathrm{s}}(x)$	Weighting function for the charges associated with the source	[–]
w_{sat}	Fitting parameter controlling the saturation of the drain-to-semiconductor Schottky barrier	[–]
x	Position in the direction of the channel length	[m]
Y_{11}	Admittance parameter	[S]
$\mathrm{Y}_{\mathrm{l,m}}(\theta, \phi)$	Angular component of the wave function	[–]
$\underline{Y}$	Complex admittance	[S]

Greek Alphabet

Symbol	**Description**	**Unit**
α	Slope degradation factor	[–]
$\tilde{\alpha}$	Slope degradation factor that is used in the total charge equations	[–]
$\alpha^{\star}$	Parameter related to the Coulomb scattering coefficient in the noise model	[V s cm^{-2}]
α_{c}	Coulomb scattering coefficient	[V s C^{-1}]
α_{corr}	Correlation parameter linking a carrier-number fluctuation to an induced mobility fluctuation in Ghibaudo's model	[–]
α_{H}	Hooge constant for the mobility fluctuations	[–]
$\alpha_{\mathrm{H,TCAD}}$	Hooge parameter which is set in TCAD	[–]
β	Exponent of the power-law mobility	[–]

β_{c}	Factor in the derivation of the noise model based on the normalized DC model	$[\mathrm{A\,V^{-2}}]$
β_{PF}	Fitting parameter in the Poole-Frenkel mobility in TCAD	$[K\sqrt{(m/V)}]$
$\Gamma(E)$	Gaussian distribution function for the DOS	$[\mathrm{cm^{-3}\,eV^{-1}}]$
γ_{PF}	Fitting parameter in the Poole-Frenkel mobility in TCAD	$[\sqrt{(m/V)}]$
ΔR	Resistance of a small noisy element in the channel of a transistor	$[\Omega]$
Δt	Time span in which the gate-voltage is swept during the transient analysis	[s]
$\Delta\Phi_{\mathrm{B}}$	Amount by which the Schottky barrier is lowered due to image charges	[eV]
ΔV	Change of the channel voltage	[V]
ΔV_{cap}	Voltage change that is used for the numerical calculation of the capacitances	[V]
ΔV_{T0}	Shift of the threshold voltage in order to compensate the influence of the mobility	[V]
$\delta I_{\mathrm{D}}/I_{\mathrm{D}}$	Relative fluctuation of the current in a small segment of the transistor channel	[−]
δI_{n}	Local noise current of the noisy element in the transistor channel	[A]
δI_{nD}	Contribution of the local noise current to the total fluctuation in the drain current	[A]
δ_{fit}	Fitting parameter for the fringe current model	[−]
ε_0	Vacuum permittivity	$[\mathrm{A\,s\,V^{-1}\,m^{-1}}]$
$\varepsilon_{\mathrm{r,diel}}$	Relative dielectric permittivity of the gate dielectric material	[−]
$\varepsilon_{\mathrm{r,osc}}$	Relative dielectric permittivity of the depleted organic semiconductor	[−]
η	Fitting parameter for the reverse-bias saturation current of the Schottky barriers at the metal-to-semiconductor junctions	[−]
Θ	Polar angle of a spherical coordinate system	$[^\circ]$
θ	Non-ideality factor of the Schottky barriers at the metal-to-semiconductor junctions	[−]
κ	Low-field mobility in the power-law mobility model	$[\mathrm{cm^2V^{-\beta-1}s^{-1}}]$
λ	Channel-length modulation factor	$[\mathrm{V^{-1}}]$
λ_{Tun}	Tunneling attenuation distance	[m]

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$\lambda_{\mathrm{particle}}$	De Broglie wave length of a particle	[m]
μ	Power-law charge-carrier mobility	[cm^2 V^{-1} s^{-1}]
μ_0	Constant mobility in case that the power-law mobility is not used in the model	[cm^2 V^{-1} s^{-1}]
μ_{Arrh}	Mobility at very high temperatures in case that the Arrhenius power-law is used	[cm^2 V^{-1} s^{-1}]
μ_{off}	Power-law charge-carrier mobility in a deep sub-threshold operation point	[cm^2 V^{-1} s^{-1}]
μ_{eff}	Effective mobility in the compact model including contact resistances	[cm^2 V^{-1} s^{-1}]
μ_{low}	Low-field mobility appearing during the derivation of the noise model	[cm^2 V^{-1} s^{-1}]
μ_{n}	Constant mobility for electrons as set in the TCAD simulation	[cm^2 V^{-1} s^{-1}]
μ_{PF}	Poole-Frenkel mobility in the TCAD simulation	[cm^2 V^{-1} s^{-1}]
μ_{p}	Constant mobility for holes as set in the TCAD simulation	[cm^2 V^{-1} s^{-1}]
ν	Fitting parameter for the charge-partitioning scheme	[–]
σ	Exponent of the frequency in the noise models	[–]
σ_{DOS}	Standard deviation of the Gaussian DOS	[eV]
σ_{trap}	Standard deviation of the Gaussian-distributed deep traps in the bandgap of the OSC	[eV]
τ_0	Time constant in the TCAD noise simulations	[s]
τ_1	Time constant in the TCAD noise simulations	[s]
τ_{scale}	Time constant of the function C_{scale}	[s]
τ_{scale2}	Time constant of the function C_{scale2}	[s]
Φ	Azimuthal angle of a spherical coordinate system	[°]
ϕ_{AC}	Phase shift of the differential amplifier	[°]
Φ_{B0}	Initial barrier height of a Schottky barrier	[eV]
$\Phi_{\mathrm{m,g}}$	Work function of the gate material	[eV]
$\Phi_{\mathrm{m,sd}}$	Work function of the source/drain electrodes	[eV]
χ_{osc}	Electron affinity of the organic semiconductor	[eV]
$\Psi(x,y,z)$	Wave function of an electron	[m$^{-3/2}$]
Ψ_{AO}	Atomic orbital of a single atom	[m$^{-3/2}$]
Ψ_{MO}	Molecular orbital	[m$^{-3/2}$]

$\Psi_{\mathrm{n,l,m}}$	Wave function of an electron depending on the quantum numbers	[$\mathrm{m}^{-3/2}$]
Ψ_{s}	Surface potential in a transistor	[V]
ω	Angular frequency	[s^{-1}]

Other

Symbol	Description	Unit
∇	Nabla operator	[−]
∂	Partial differential operator	[−]
$\mathcal{L}$	First branch of the Lambert W function	[−]

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List of Acronyms

Symbol	Description
2D	Two-dimensional
3D	Three-dimensional
AC	Alternating current
BC	Bottom-contact
CEA	Commissariat à l'Énergie Atomique et aux Énergies Alternatives
CMOS	Complementary metal oxide semiconductor
CPU	Central processing unit
DC	Direct current
DIBL	Dain-induced barrier lowering
DNTT	Dinaphto[2,3-b:2',3'-f]thieno[3,2-b]thiophene
DPh-DNTT	2,9-diphenyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene
DOS	Density of states
EDA	Electronic design automation
HOMO	Highest occupied molecular orbital
LCAO	Linear combination of atomic orbitals
LCR	Formula symbols for the inductance (L), the capacitance (C), and the resistance (R)
LITEN	Laboratoire d'Innovation pour les Technologies des Energies Nouvelles et les Nanomatériaux
LUMO	Lowest unoccupied molecular orbital
MIM	Metal-insulator-metal
MISM	Metal-insulator-semiconductor-metal
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field-effect transistor
MPI	Max Planck Institute
OSC	Organic semiconductor

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OTFT	Organic thin-film transistor
PEN	Polyethylenenaphtalate
PFBT	Pentafluorobenzenethiol
PhD	Philosophiae Doctor
PSD	Power spectral density
SAM	Self-assembling monolayer
SEM	Scanning electron microscopy
SPICE	Simulation Program with Integrated Circuit Emphasis
TC	Top-contact
TCAD	Technology Computer Aided Design
TLM	Transmission-line method
TH	Technische Hochschule
TFT	Thin-film transistor
UMEM	Unified model and parameter extraction method
VRH	Variable-range hopping

CHAPTER 1

Introduction

1.1 General Introduction

Daily life is nearly unimaginable without electronic devices such as computers or smartphones. The fundamental building block of nearly every complex electric circuit is the transistor which has been extensively studied and developed over the last few decades. Already in 1926, Julius Edgar Lilienfeld was granted a patent for a device controlling the current between two terminals by the application of a potential at a third terminal [1]. However, it was impossible to fabricate such a device at that time. In the following decades, transistors were subject to intense research. To mention some milestones, in 1951, Schockley proposed a p-n junction bipolar transistor [2]. In 1958, the first integrated circuit was demonstrated by Kilby [3]. Nowadays, most of the integrated circuits are based on the metal oxide semiconductor field-effect transistor (MOSFET) which was invented in 1959 [4]. By means of doping, transistors with different majority carriers (p or n) can be fabricated. In comparison to n-type transistors, p-type transistors conduct negative currents and need negative voltages [5]. Combining n-type and p-type transistors leads to the so-called complementary MOS (CMOS) process which has been introduced in 1963 [6]. In 1971, the first microprocessor was developed by Intel [7].

Nowadays, the research of semiconductor devices focuses on the improvement of the device switching behavior in order to reduce the power consumption of electric circuits. For this purpose, for example, tunnel field-effect transistors are investigated [8] which allow for a steeper and faster switching from the off-state to the on-state.

In contrast to the bulk MOSFETs, another technology evolved over time: the thin-film transistor (TFT). In 1979, a thin-film transistor based on hydrogenated amorphous silicon was presented [9]. In contrast to the bulk MOSFET, a thin-film transistor only contains a thin film of the semiconductor and does not have a bulk region. Even if the first TFTs were regarded as useless, they evolved over time to be the most important transistors used in active-matrix

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displays [9]. With increasing interest in TFTs, the materials used as the active region were studied. In the 1980s, organic semiconductors were looked at more intensively [9]. As the name implies, organic semiconductors (OSCs) are based on molecules containing carbon [10]. The interest in organic semiconductors is increasing since organic electronics can be fabricated at room temperature on flexible substrates, such as plastic foils or paper [11–14] which makes them interesting for the fabrication of novel electronics like flexible displays. Furthermore, in contrast to the silicon-based semiconductors the organic semiconductors can be solution-processed which simplifies the production of electronic devices [9]. From the 1980s until today, many organic semiconductors have been investigated and employed as the active region in OTFTs. There exists a variety of organic semiconductors with different molecule sizes ranging from long-chain polymers to small-molecule semiconductors [9]. In contrast to their silicon counterparts, the carrier mobilities of organic semiconductors are still low and only range up to $20\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for holes [9]. Furthermore, contact resistances play a key role in the limitation of overall OTFT performance [9, 15–18]. However, due to the development of new materials [19, 20] and novel fabrication approaches [21], the overall TFT performance has been improved.

1.2 Organization

In the following, the organization of this thesis is explained. To start with, in this first chapter, an overview over the field of organic chemistry is given which is necessary in order to understand the functional principles of organic transistors. Furthermore, the aim of this work is defined. In this context, the term "compact model" is introduced and the basic concepts behind such models are highlighted.

In Chap. 2, a charge-based DC compact model serving as the basis for this work is reviewed. The concept of the compact model is explained and minor model extensions and improvements are presented.

In Chap. 3, a general introduction into the concept of intrinsic and extrinsic charges in transistors is presented. Based on the standard theory for MOSFETs, the charges and their importance for a proper device model are outlined.

In Chap. 4, the development of a charge-based compact model for the total charges is presented. Analytical equations for the total charges associated with the source, drain, and gate terminals of the transistor are derived including both the intrinsic channel components and the extrinsic components arising from fringe regions and gate-to-contact overlap regions. Thereby, the two device geometries "staggered" and "coplanar" are investigated in detail.

In Chap. 5, a compact modeling scheme for the calculation of low-frequency noise in organic thin-film transistors is presented. This modeling scheme can include different types of noise such as mobility fluctuations or charge-carrier number fluctuations. Closed-form equations for both types of noise are developed.

In Chap. 6, the compact models for the total charges and the low-frequency noise are verified. Measurements of transistors and a simple circuit representing a differential amplifier are compared to the compact model. Furthermore, finite-element simulations are used in order to simulate the quasistatic and non-quasistatic behavior of organic thin-film transistors. The noise model is verified by measurement data and finite-element simulations.

The compact model has some limitations with regard to the non-quasistatic behavior and short-channel effects. Therefore, in Chap. 7, model extensions are presented. First, the channel-segmentation model is explained which allows for a non-quasistatic modeling of long-channel transistors. This model is verified by measurements and simulations. Next, based on finite-element simulations, a semi-empirical description for the total charges in short-channel transistors is developed. In the next section, a comprehensive model for the description of the small-signal gain in short-channel transistors operated under high-frequency conditions is presented. The last section deals with a small investigation on the influence of temperature effects on the transistor behavior.

In Chap. 8, a summary of literature covering the capacitive behavior and the low-frequency noise in organic transistors is presented.

Finally, in Chap. 9, the work is summed up and conclusions are drawn.

1.3 Organic Chemistry

1.3.1 Atomic orbitals

In this section, the most important concepts of the organic chemistry are summarized based on ref. [10]. The term "organic" refers to molecules containing the element carbon which is the sixth element in the periodic table of elements and is located in the fourth main group. According to Bohr's atomic model, the chemical elements are characterized by positively charged cores with electrons moving around them. However, in the concept of quantum physics, small particles may behave in parallel like a classical particle obeying the conventional laws of movement according to Newton and also like a wave [22]. If electrons are accelerated and sent towards a small double-slit with a screen behind, then a behavior can be observed which from the classical point of view is only known for waves: the electrons create an interference pattern meaning that the density of electrons behind the double-slit has several minima and maxima.

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Furthermore, the electrons appear on the screen at positions where they could not go according to the classical description of particles [22]. Because of this, De Broglie defined that small particles obey a wave-particle dualism and that every particle can be assigned a wavelength which is denoted as the De Broglie wavelength [22]:

$$\lambda_{\text{particle}} = \frac{h}{m_{\text{particle}} \cdot v_{\text{particle}}} \tag{1.1}$$

where h is the Planck constant, m_{particle} is the mass of the particle, and v_{particle} is the velocity of the particle. Extending Bohr's atomic model with the concept of the particle-wave dualism, the atom is now regarded as a positively charged core where electrons form standing waves around the core. The wave function of an electron is denoted as $\Psi(x,y,z)$ which is dependent on the three coordinates of the three-dimensional (3D) space. This function $\Psi(x,y,z)$ does not have a descriptive meaning. However, the value $\Psi^2(x,y,z) \cdot dx \cdot dy \cdot dz$ can be interpreted as the probability to find the electron in the volume $dx \cdot dy \cdot dz$ [10]. In the literature, it is debated whether a probability of residence is a figurative way of interpreting the function $\Psi^2(x,y,z)$ or whether it makes more sense to interpret electrons only by their wave functions without calling the square of Ψ a probability [22]. In 1926, Erwin Schrödinger developed the well-known differential equation linking the wave function of a system like the electron to the energy [10]:

$$H\Psi = E\Psi \tag{1.2}$$

where H is the so-called Hamilton operator and E is the energy. The Hamilton operator is defined as [22]:

$$H = -\left(\frac{\hbar^2}{2m_{\text{particle}}}\right)\nabla^2 + V \tag{1.3}$$

where $\hbar$ is the Planck constant divided by 2π, $\nabla^2 = \partial^2/\partial x^2 + \partial^2/\partial y^2 + \partial^2/\partial z^2$ is the Nabla operator squared (which is also denoted as the Laplace operator), and V is the potential energy. Functions fulfilling the Schrödinger equation are denoted as eigenfunctions and the energies corresponding to these eigenfunctions are denoted as eigenvalues.

The theory according to the Schrödinger equation can be transferred to the atomic model. The basic concept of quantum physics is that the electrons in atoms can only assume discrete energy levels which are described by four quantum numbers. The first quantum number is n and it is denoted as the main quantum number. The second quantum number is l and it is denoted as the secondary quantum number. The third quantum number, m, is denoted as the magnetic quantum number and the fourth quantum number, s, is called the electron spin. Some of the quantum numbers are dependent on each other and only certain integer values are allowed. The range for the quantum numbers is defined as follows [10, 22]:

- $n = 1, 2, 3, ..., \infty$. The value indicates the shells which are also denoted as K, L, M, ...
- $l = 0, 1, 2, ..., n-1$: This quantum number defines the atomic orbitals. The values of this quantum number are denoted as (in ascending order) s, p, d, f, ...
- $m = +l, +(l-1), ...0, ... -(l-1), -l$
- $s = +1/2$ or $-1/2$.

As can be seen, the quantum number s only has two values which are allowed. The quantum numbers and their interdependence leads to the periodic table of elements. As explained above, the energy of an electron in an atom may only assume discrete values in dependence on the quantum numbers. As a consequence, there only exist discrete wave functions with certain sets of quantum numbers for which the Schrödinger equation can be solved.

In general, the wave function of an electron can be expressed as a product of two functions in spherical coordinates which depend on the quantum numbers n, l, and m [10]:

$$\Psi_{\mathrm{n,l,m}} = R_{\mathrm{n,l}}(r) \cdot Y_{\mathrm{l,m}}(\Theta, \Phi) \tag{1.4}$$

where $R_{\mathrm{n,l}}(r)$ is denoted as the radial component and $Y_{\mathrm{l,m}}(\Theta, \Phi)$ is denoted as the angular component. As can be seen, the radial component is only dependent on the radius r and the angular component is dependent only on the angles Θ and Φ. The two components of Ψ are usually regarded separately. On the one hand, the absolute value of the angular function $Y_{\mathrm{l,m}}(\Theta, \Phi)$ is plotted in a 3D coordinate system. The endpoints of the vectors form a 3D surface enclosing the spatial region in which the electrons can reside. On the other hand, the value of Ψ^2 can be plotted in dependence on the radius r in order to depict the probability of residence in a certain distance from the atomic core.

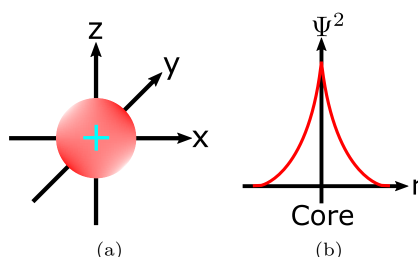

Figure 1.1.: (a) Visualization of the angular function $Y_{\mathrm{l,m}}(\Theta, \Phi)$ for $l = 0$. This is denoted as the s orbital. (b) Visualization of the squared wave function Ψ^2 for $l = 0$ showing the probability of residence of an electron in a certain distance r from the core of the atom. These pictures are inspired by ref. [10].

If $l = 0$, the quantum number m can only assume one value which is zero. Therefore, there exists only one orbital. This s orbital is a sphere which is depicted in Fig. 1.1(a). The probability function Ψ^2 is visualized in Fig. 1.1(b). If, by contrast, $l = 1$, there are three values which

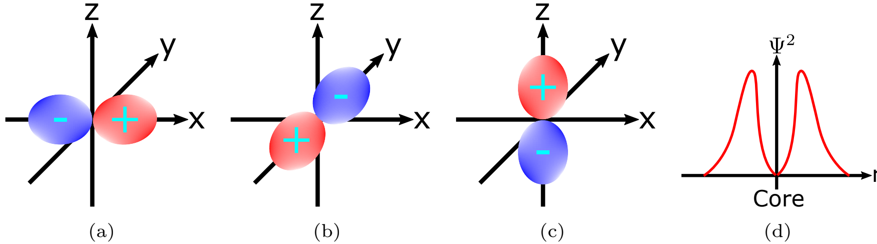

Figure 1.2.: Visualization of the angular function $Y_{\mathrm{l,m}}(\Theta, \Phi)$ for $l = 0$ and (a) $m = +1$, (b) $m = -1$, and (c) $m = 0$. The orbitals are denoted as p_{x}, p_{y}, and p_{z} orbitals, depending on the axis that they are symmetric to. (d) Visualization of the squared wave function Ψ^2 for $l = 1$ showing the probability of residence of an electron in a certain distance r from the core of the atom. These pictures are inspired by ref. [10].

the quantum number m can take: -1, 0, and +1. Depending on the value of m, the p orbitals have different shapes. In Fig. 1.2(a)-(c), the angular function $Y_{\mathrm{l,m}}(\Theta, \Phi)$ is shown for the three different values of m where the plus and minus signs are a consequence of the mathematical description of the wave function [10]. In Fig. 1.2(d), the probability function is shown in dependence on the radius.

As soon as a system contains more than one electron, the Schrödinger equation cannot be solved analytically any longer [10] because of the interaction of electrons [22]. However, the orbitals of a multi-electron atom can be approximated by expressing them as modified hydrogen orbitals. According to Pauli's principle, one orbital can be occupied by a maximum number of two electrons which then have different electron spins. Based on this theoretical framework, for each single atom of the periodic table the orbitals can be determined.

1.3.2 Chemical bonds

When two or more atoms get into connection and form a chemical bonding, a molecule results. Since the atoms are in connection their single atomic orbitals are no longer present. There exist different theories for the approximation of the Schrödinger equation: the theory of molecular orbitals and the valence bond theory. Both are in principle equivalent but are based on different model views [10].

According to the theory of molecular orbitals, due to the bonding of the single atoms their single atomic orbitals are no longer present and they merge into orbitals belonging to the whole molecule. These molecular orbitals can be described by a mathematical superposition of

single atomic orbitals. A common method for this is the linear combination of atomic orbitals (LCAO) which is also employed in commercial quantum-chemical simulation software such as QuantumATK [23]. In the LCAO method, the resulting molecular orbital Ψ_{MO} based on two identical single atomic orbitals is expressed as [10]:

$$\Psi_{\mathrm{MO}} = c_1 \cdot \Psi_{\mathrm{AO}} \mp c_2 \cdot \Psi_{\mathrm{AO}} \tag{1.5}$$

where Ψ_{AO} is the atomic orbital of a single atom and c_1 and c_2 are constants the values of which are determined numerically in such a way that the resulting energy has its minimum value corresponding to a stable state [10]. As can be seen, the superposition of the atomic orbitals occurs once by adding and once by subtracting the single atomic orbitals. Figure 1.3 depicts

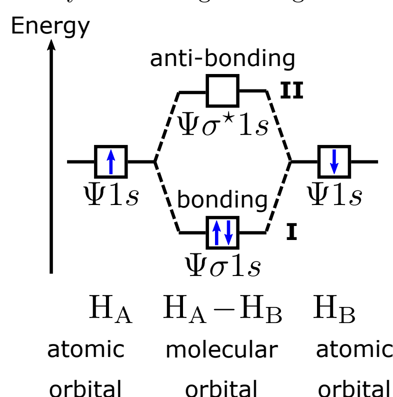

Figure 1.3.: Energy diagram of the molecular orbitals of the H_2 molecule. Each of the single hydrogen atoms has an atomic orbital which are superposed according to the LCAO method. The result is a bonding and an anti-bonding molecular orbital. The blue arrows represent electrons occupying the states where the direction of the arrow shows the electron spin. This picture is inspired by ref. [10].

an energy diagram of an H_2 molecule. Each of the single hydrogen atoms has an atomic orbital which are combined by the LCAO method. As a consequence, the molecule has two molecular orbitals denoted as **I** and **II**. Adding the two atomic orbitals leads to the molecular orbital **I** which has a lower energy than the original atomic orbitals. By contrast, when subtracting the single atomic orbitals the resulting molecular orbital **II** has a higher energy [10]. The electrons of the hydrogen atoms now occupy the molecular orbitals. According to Pauli's principle, the lowest energetic states are occupied first. Thus, the two electrons now occupy the molecular orbital **I** with the lower energy. Since the energy of the molecular orbital **I** is lower than that of the original atomic orbitals the connection of the two hydrogen atoms is stable. Breaking the bond between the two atoms would require energy to lift the electrons in their original states again. Therefore, the molecular orbital **I** is denoted as a bonding orbital. By contrast, since the energy of the molecular orbital **II** is higher than that of the original atomic orbitals it is denoted as anti-bonding, which is often marked by an asterisk ($\star$). An electron occupying an anti-bonding orbital is not part of the atomic bond and it can be regarded as a free electron [10].

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Directly linked to the theory of the molecular orbitals, the valence bond theory has a slightly different view on atomic bonds. According to the valence bond theory, the atomic orbitals which are characterized as charge clouds are overlapping. This effectively means that the electrons of the single atoms are now part of the connection between the atoms [10]. Most often, two electrons (one from each atom) are part of the connection. There may be electrons or pairs of electrons that are not part of the chemical bond which are then denoted as free electrons. These thoughts lead to the well known valence structure that is used to note down chemical bonds. For example, the H_2 molecule is written down as [10]:

$$\mathrm{H} - \mathrm{H} \tag{1.6}$$

where the dash (−) represents a pair of electrons.

1.3.3 Carbon

Carbon is the sixth element in the periodic table of elements. In its basic state, two electrons occupy the s orbital of the first shell, two electrons occupy the s orbital of the second shell, and two electrons occupy the p orbital of the second shell. Written in abbreviated form, this electron configuration is: $1s^2 2s^2 2p^2$. The electron configuration of the carbon atom in its basic state is depicted in Fig. 1.4(a). It might be assumed that carbon is only capable of forming two

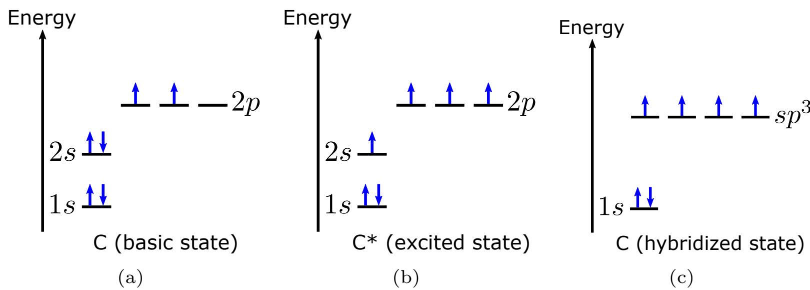


Figure 1.4.: Energy diagram of carbon. (a) Basic state. (b) Excited state where one electron from the $2s$ orbital is lifted in the $2p$ orbital. (c) Hybridized state where the $2s$ orbital and the three $2p$ orbitals form four identical sp^3 hybrid orbitals which are occupied by the electrons. This picture is inspired by ref. [10].

equal bonds with other atoms since only two $2p$ orbitals are occupied by a solitary electron. In order to form four bonds, one electron occupying the $2s$ orbital would have to be lifted in the third $2p$ orbital which is visualized in Fig. 1.4(b). As a consequence, the carbon atom would form unequal bonds with other atoms since three of the electrons are in the same energetic state while one is in a lower energetic state. However, it was discovered that the methane molecule (CH_4) has the shape of a tetrahedron where the four hydrogen atoms have equal distances to the carbon atom. Based only on the theory of atomic and molecular orbitals, these four equal connections of carbon to the hydrogen atoms could not be explained [10].

As a consequence, an extension of the orbital theory has been developed: the hybridization. The concept of hybridization is a mathematical mixing of atomic orbitals [10].Mixing one s orbital and three p orbitals, four sp^3 hybrid orbitals with equal energy can be created. This is shown in Fig. 1.4(c). With the hybridization model, the properties of the methane molecule can be explained. Chemical bonds where in both atoms either two s orbitals or an s and a p orbital or two p orbitals are combined are denoted as σ bonds [10]. Such bonds are tight and the electrons are bound in these states. If a molecule forms the maximum possible number of σ bonds, it is called a saturated molecule [10]. In case that atoms in a molecule do not form the maximum possible number of σ bonds (and consequently not all atomic orbitals of the second shell are hybridized), the molecule is denoted as unsaturated. The atomic p orbitals which are not hybridized remain as they are and may also overlap with the other non-hybridized orbitals of the other atoms. Bonds of these non-hybridized p orbitals are denoted as π bonds, which are weaker than the σ bonds [10]. In Fig. 1.5, an ethene molecule is shown. On the left, the valence structure is shown. In the middle, the double bond between the two carbon atoms is shown as a σ bond and the two remaining non-hybridized p_z orbitals are visualized. On the right, the connection of the two p_z orbitals is shown which leads to a π bond. The ethene molecule contains σ and π bonds.

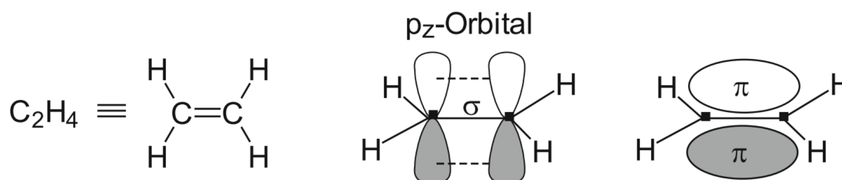


Figure 1.5.: Valence structure and visualization of the orbitals of an ethene molecule. The p_z orbitals which are not hybridized can form a π bond as shown in the sub-picture to the right. This picture is taken from ref. [10].

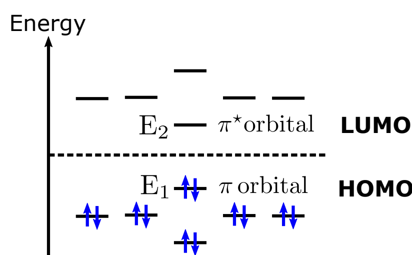


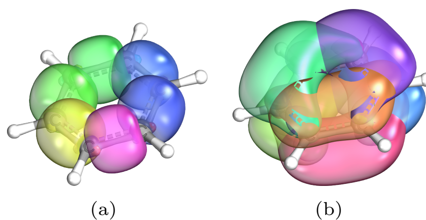
Figure 1.6.: Energy diagram of the ethene molecule in the basic state. This picture is inspired by ref. [10].

In Fig. 1.6, the energy diagram of the ethene molecule in the basic energetic state is depicted. According to the theory of molecular orbitals, there are several bonding and several anti-bonding molecular orbitals. The bonding molecular orbitals are drawn below the dashed horizontal line and the anti-bonding molecular orbitals are shown above. According to Pauli's principle,

energetic states are filled in ascending order [10]. The highest bonding orbital with energy E_1 is a π orbital and since it is the highest orbital which is occupied in the basic energetic state, it is denoted as the highest occupied molecular orbital (HOMO). By contrast, the first energetic state E_2 which is anti-bonding and which is not occupied in the basic state is denoted as lowest unoccupied molecular orbital (LUMO). Electrons occupying states above the LUMO are not tightly bound and can be characterized as mobile charges [10].

1.3.4 Organic semiconductors

For organic electronics, molecules with alternating double and single bonds between the adjacent carbon atoms are of interest. Such molecules are denoted as π-conjugated molecules [10]. A special property of such π-conjugated systems is that the carbon atoms are located in one plane. As a consequence, the non-hybridized p orbitals are located normal to the molecule plane and they can overlap. In π-conjugated systems, the electrons in the p orbitals are delocalized which means that they can be imaged as an electron cloud which is distributed around the molecule [10]. If an electron is located in a π bond, it can either behave like a bound electron or like a freely movable electron depending on whether it is located in a bonding or an anti-bonding molecular orbital. In Fig. 1.7, the σ and the π orbitals of such a π-conjugated system are shown:



(a) (b)

Figure 1.7.: Visualization of the molecular orbitals of the molecule benzene. (a) σ orbitals that are part of the connection between the atoms. (b) π orbitals. The graphics are created using the software IBOview as described in ref. [24].

the benzene molecule. In this molecule, the phenomenon of mesomery becomes important. Mesomery describes the fact that the alternating single and double bonds can occur in several positions in the molecule so that the exact structure of the molecule cannot be determined. Expressed in other words: mesomeric structures can assume several forms. In such a system, the electrons in π orbitals are completely delocalized which means that they can move around the molecule in a kind of cloud. If electrons have enough energy so that they can be excited from the HOMO to the LUMO, they can thus be regarded as chemically unbound and completely mobile charge carriers which are able to leave the molecule. In principle, the molecule is ionized then since the electron has left its original position in the atomic bond. Thus, one can say that an electron-hole pair has been created since the electron can easily leave the molecule now and another electron entering the molecule could occupy the original state [10].

If several molecules are located close to each other, there is the possibility for an electron to move to an adjacent molecule. There are some parallels to conventional crystalline semiconductors since also in these materials, a charge carrier is able to leave its original position in the crystal if it has a sufficiently high energy [25]. Thus, a bunch of π-conjugated organic molecules shows a behavior similar to a semiconductor. However, in contrast to crystalline semiconductors, organic molecules can hardly be arranged so that they form perfect crystals but they rather have a certain degree of spatial (and thus also energetic) disorder [26–29]. This has an influence on the density of states (DOS) of the material. Due to the non-crystallinity the single organic molecules are disordered and their energy diagrams are slightly shifted with respect to adjacent molecules. Therefore, in contrast to a crystalline semiconductor like silicon [25], there is no band-like energetic structure. The density of states for quasi-mobile charges in organic semiconductors is debated in the literature [30]. Often for disordered systems, a Gaussian-distributed density of states (DOS) is assumed [26, 30–33]. In Fig. 1.8(a), the

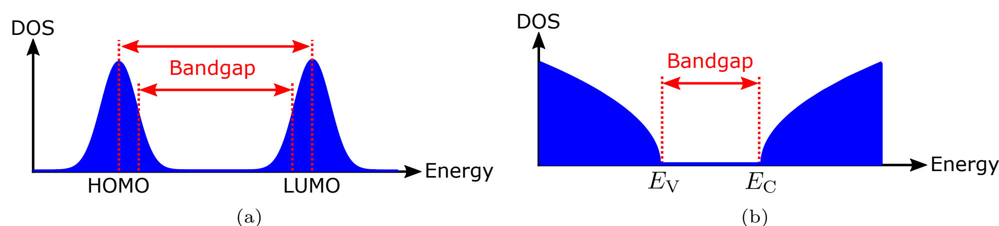


Figure 1.8.: (a) Visualization of a Gaussian DOS which occurs in disordered semiconductors. (b) Visualization of a square-root DOS which is typical in crystalline semiconductors.

DOS of an organic semiconductor is visualized as a Gaussian distribution. Since there is an energetic distance between the HOMO and the LUMO, the organic semiconductor has the typical property that is one of the prerequisites in order to denote a material as semiconducting: an energetic gap between conducting and bounding states with a distance not too high [25] and a forbidden zone in between. In Fig. 1.8(b), for the purpose of comparison, the DOS in a crystalline semiconductor such as silicon is depicted. The DOS can be described as a square-root function of the energy [25]. In the bandgap, there are no energetic states. Thus, an electron can either be in a state below the valence band edge E_V, where it behaves like a bound electron, or it can be in an energetic state above the conduction band edge E_C, where it can be treated as a mobile charge carrier that can move through the whole crystal. As indicated by Fig. 1.8(a), in organic semiconductors, there is the difficulty of defining the bandgap properly. For a single molecule, the energy distance between HOMO and LUMO is defined by the molecular orbitals. However, due to the non-crystallinity of the organic material, the LUMO and HOMO levels of the organic semiconductor are not aligned, as mentioned above. Thus, the effective bandgap of the semiconductor is smaller than that of a single molecule. Consequently, there exist different interpretations of the bandgap in such disordered materials such that either the distance between the peaks of the Gaussian distributions are taken or a

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value smaller than that [33]. In the following course of the dissertation, the band diagram of the organic thin-film transistors (OTFTs) will be treated like the band diagram of a conventional semiconductor. The HOMO energy level is regarded equivalently as the valence band edge E_V and the LUMO energy level is regarded equivalently as the conduction band edge E_C.

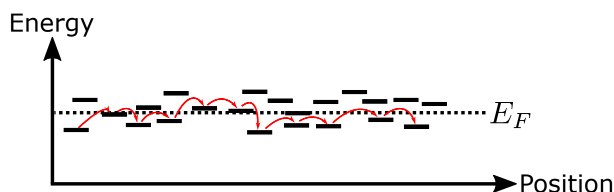

Figure 1.9.: Illustration of the variable-range-hopping transport in organic semiconductors. This picture is inspired by ref. [34].

There are various models describing the charge transport in organic materials [35] such as the mobility-edge model, the multiple-trap-and-release model, the variable-range-hopping (VRH) model, or the percolation model [29]. The applicability of these models to an organic semiconductor depends on the degree of disorder. In Fig. 1.9, the charge transport according to the VRH is depicted. The dashes represent energetic states above the LUMO in which the charge carriers behave like quasi-mobile charges. In the VRH model, it is assumed that the charge transport occurs mainly by the hopping of charge carriers from molecule to molecule. This is in principle a tunneling process from one molecule to an adjacent one. Although the charge transport in organic materials is quite different from that in crystalline semiconductors, it is possible to describe the current assuming a band-like transport with a very low mobility [36]. A model accounting for the hopping transport can then be adapted in terms of an effective mobility [37], as will be explained later.

1.4 Organic Transistors

1.4.1 Architectures and Fabrication

The above-described properties of π-conjugated materials allow them to be employed as the active layer in field-effect transistors. The transistor is the most important building block in modern electronics and there exists a huge variety of literature in which the operational principles of transistors of various types are described [5, 25, 38, 39]. In this section, a short overview over the fabrication and operation principles of OTFTs are presented. In principle, there are several ways of fabricating organic transistors such as a vacuum deposition using silicon stencil lithography [17, 40] or by printing and spin-coating [41]. In this section, the explanation of the transistor architectures is based on the process as conducted by the Max Planck Institute for Solid State Research [17, 40, 42, 43]. Figure 1.10 shows the layout of an OTFT fabricated in the bottom-gate top-contact architecture. Since the different layers of

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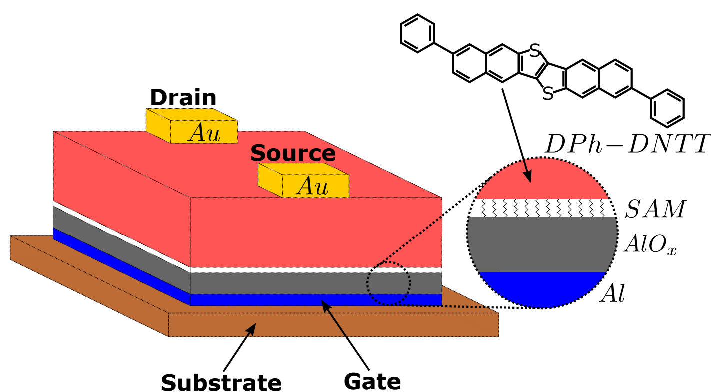

Figure 1.10.: Organic thin-film transistor fabricated in the bottom-gate top-contact architecture which is also denoted as the staggered architecture. The different layers of the transistor are stacked above each other.

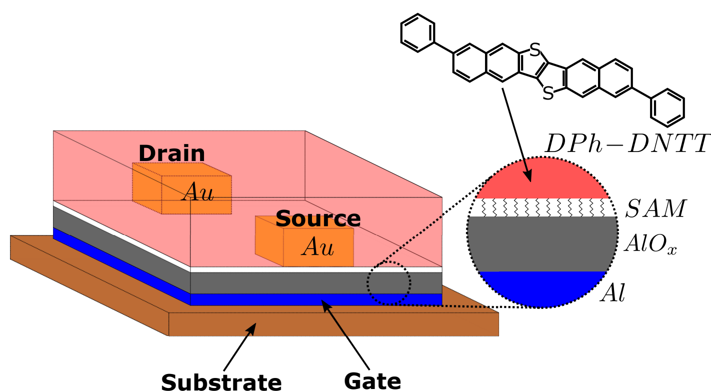

Figure 1.11.: Organic thin-film transistor fabricated in the bottom-gate bottom-contact architecture which is also denoted as the coplanar architecture. The channel region of the organic semiconductor is in the same plane as the source/drain electrodes.

this transistor are stacked above each other this architecture is also denoted as the staggered architecture. By contrast, in Fig. 1.11, a transistor fabricated in the coplanar architecture is depicted. In this architecture, the channel region of the organic semiconductor is located in the same plane as the source/drain electrodes which gives this architecture the name "coplanar". Both architectures can be fabricated in the same process which will briefly be described.

The transistors according to refs. [17, 40, 42, 43] are fabricated on flexible plastic substrates. In a vacuum chamber, interconnects for the gate, source, and drain terminals are patterned by thermal sublimation of gold through a mask that is attached above the substrate. The interconnects are not shown in Figs. 1.10 and 1.11. After this process step, the mask is changed and a gate consisting of aluminum is patterned. Subsequently, the substrate is exposed to an oxygen

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plasma which forms a layer of aluminum oxide on top of the aluminum. This is the first part of the gate insulator. In order to improve the quality of the gate insulator and to reduce leakage current, the substrate is then immersed into a liquid containing e.g. n-tetradecylphosphonic acid. The special property of these molecules is that they form a self-assembling monolayer (SAM) on top of the aluminum oxide, i.e. they form one single layer and all molecules are oriented in the same direction. Such hybrid gate dielectrics consisting of aluminum oxide and a SAM show good dielectric properties and they assist in a formation of an organic-semiconductor film of good quality. As explained above, the quality of an organic semiconductor is dependent on the degree of disorder. Employing a SAM helps in the reduction of this disorder. After the formation of the SAM, the substrate is put in the vacuum chamber again. Until this step, the fabrication of staggered and coplanar transistors is equal but from now on the order of the fabrication steps differs.

Staggered:
An organic semiconductor is evaporated by thermal sublimation. In Fig. 1.10, the material 2,9-diphenyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DPh-DNTT) is shown as the organic semiconductor. After the evaporation of the semiconductor, the substrate is taken out of the vacuum and a mask for the source/drain electrodes is attached. In the last process step, the source/drain electrodes are patterned by thermal evaporation of gold. The reason for choosing gold as the source/drain material will be explained later.

Coplanar:
The source/drain contacts are evaporated by thermal sublimation directly on top of the SAM. In the next step, in principle, the organic semiconductor could be evaporated. However, in order to improve the current injection at the source-to-semiconductor interface, a good connection between the source electrode and the organic semiconductor is needed. Therefore, similar to the SAM that is used on top of the aluminum oxide, a SAM can be formed around the source/drain contacts [44]. This helps for a better attachment of the organic molecules. The SAM is formed by immersing the substrate in a liquid containing the desired molecules such as pentafluorobenzenethiol (PFBT). After this process step, the organic semiconductor is evaporated in the vacuum chamber.

Figure 1.12 shows the four most important architectures that these OTFTs are fabricated in. In principle, the two architectures in Figs. 1.12(a) and (c) are equal. The horizontal flipping of the transistor does not change its electric properties. Similarly, the two structures in Figs. 1.12(b) and (d) are equal. The only factor governing the difference between the architecture is whether the source/drain electrodes are in the same plane as the organic semiconductor or whether they are stacked above each other. However, the order of the deposition of the different layers may change the interface qualities and thus, the inverted structure might exhibit a slightly different behavior than the non-inverted structure.

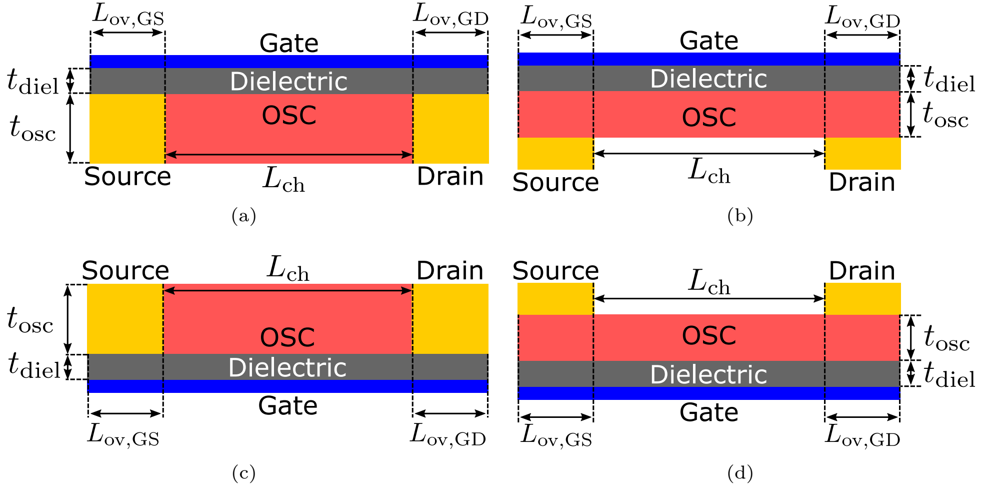

Figure 1.12.: Four different architectures of OTFTs. (a) Top-gate top-contact transistor, also denoted as coplanar. (b) Top-gate bottom-contact transistor, also denoted as staggered. (c) Bottom-gate bottom-contact transistor, also denoted as inverted coplanar. This case is identical to (a) but horizontally flipped. (d) Bottom-gate top-contact transistor, also denoted as inverted staggered. This case is identical to (b) but horizontally flipped.

1.4.2 Electronic Operation Principle

The operation principle of OTFTs has many similarities with the operation of a MOSFET [5, 25, 38]. As shown in Fig. 1.12, the OTFTs comprise metal-to-organic-semiconductor junctions. In this regard, they resemble Schottky-barrier field-effect transistors [45]. As usual for TFTs, the OTFTs have three connection terminals which are the gate, the drain, and the source. The basic idea is that charge carriers can move from the source to the drain terminal but the resistivity of the channel can be modulated by the gate-source voltage. Thus, the OTFT, just as every transistor, is an electronic device that can control the current flow between two terminals by a third terminal. In Fig. 1.13, the band diagram of an OTFT along a cutline normal to

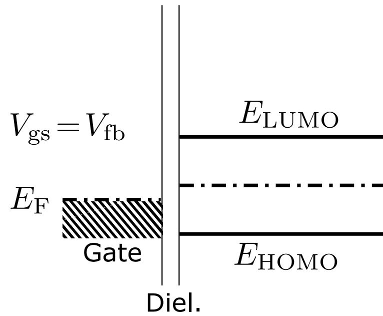

Figure 1.13.: Band structure of an OTFT along a cutline normal to the gate plane. Here the gate-source voltage is set to the flatband voltage.

the gate plane is depicted. The bands are shown at an arbitrary position in the channel. As can be seen, the transistor has a positive flatband voltage in this case since the Fermi level of the gate electrode is shifted down with respect to the Fermi level of the organic semiconductor in order to obtain flat bands. Since the organic semiconductor is not doped the Fermi level without any outer influences is approximately in the mid-bandgap. The reason for a non-zero flatband voltage is a difference in the work functions between the gate material and the organic semiconductor. The work function is defined as the difference between the vacuum energy level and the Fermi level. In Fig. 1.14, the band diagram of the OTFT is shown along a cutline in

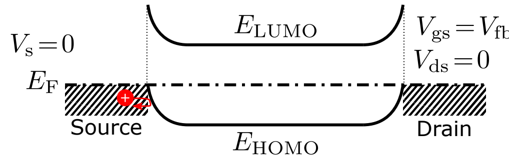

Figure 1.14.: Band structure of an OTFT along a cutline in the direction of the channel. Here the gate-source voltage is set to the flatband voltage and the drain-source voltage is zero. The work function of the source/drain metal is aligned with the HOMO of the organic semiconductor.

the direction of the channel from source to drain. Also here, the flatband voltage is applied as the gate-source voltage. Due to the electrostatic influence of the source/drain electrodes there occurs a band bending [46]. As can be seen in Fig. 1.14, the HOMO level matches the Fermi level at the source-to-semiconductor and drain-to-semiconductor junctions. The reason for this is that the work function of the source/drain material is chosen to match the HOMO level of the organic semiconductor. The consequence is that at the metal-to-semiconductor junctions no Schottky barriers for holes are present. If, by contrast, the work function of the source/drain

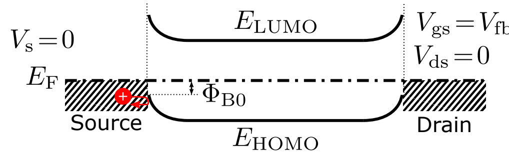

Figure 1.15.: Band structure of an OTFT along a cutline in the direction of the channel. Here the gate-source voltage is set to the flatband voltage and the drain-source voltage is zero. The work function of the source/drain metal is different from the HOMO of the organic semiconductor. Thus, a Schottky barrier of height Φ_{B0} is present.

material is different from the HOMO level of the organic semiconductor, there are Schottky barriers which play an important role for the current injection at the source-to-semiconductor interface and will result in parasitic contact resistances [18, 33, 47]. In Fig. 1.15, the band diagram along the channel cutline is depicted again, but this time, a Schottky barrier of height Φ_{B0} is present.

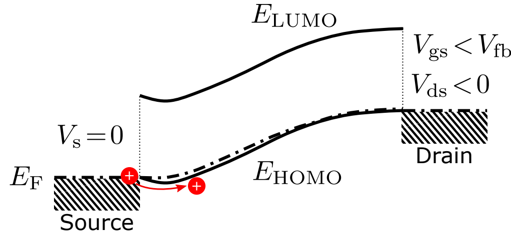

Figure 1.16.: Band structure of an OTFT along a cutline in the direction of the channel. Here, the gate-source voltage is set to a voltage smaller than the flatband voltage and the source-drain voltage is set to a negative value. The work function of the source/drain metal is aligned with the HOMO of the organic semiconductor.

In order to allow a current flow from source to drain, charge carriers need to be injected at the source-to-semiconductor junction so that they can flow to the drain. Under the conditions shown in Fig. 1.14 no significant current can flow because the bands in the channel region form a barrier for the charge carriers. This is indicated by the hole that is repelled at the junction. Therefore, the barrier in the channel needs to be lowered so that charge carriers can surmount it and flow to the drain. Furthermore, a drain-source voltage needs to be applied. In Fig. 1.16, the band diagram of the OTFT is shown for the case that a gate-source voltage smaller than the flatband voltage is applied. Furthermore, a negative drain-source voltage is applied. As a consequence, holes can be injected from the source into the channel and they can flow towards the drain.

As explained above, the organic semiconductor is undoped so that under equilibrium conditions the Fermi level equals the intrinsic Fermi level which is approximately in the middle of the bandgap. From this, there arises an interesting consequence: whether an OTFT is an n-type or a p-type transistor depends on the work function of the source/drain metal in relation to the bands of the organic semiconductor [48]. Typical semiconductors such as pentacene or Dinaphto[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) have HOMO levels of approximately 5 eV [40, 48]. The work function of gold is approximately 5.1 eV [25] and thus, there is only a small Schottky barrier at the gold-to-semiconductor junction. Since organic semiconductors such as DNTT have very large bandgaps in the range of 3 eV [40] it is difficult to find a metal with a sufficiently small work function so that the transistor could be used as an n-type transistor. Typical metals such as gold, aluminum and silver have work functions between 4 eV and 5.1 eV which means that the resulting transistor will show the behavior of a p-type transistor. The organic transistors investigated in this work are all p-type transistors. However, in order to facilitate the understanding of the equations the compact models will be derived for n-type devices which can easily be transferred to p-type devices by negating the polarity of the voltages, currents and charges.

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1.5 Outline

This PhD thesis targets on the development of a charge-based compact model for the capacitive behavior and the low-frequency noise in organic thin-film transistors of both the staggered and the coplanar architectures. In this section, the aim of developing a compact model will be outlined.

When developing an electric circuit, it is of utmost importance that the circuit behaves properly before the mass production can start. For this purpose, in earlier times the electric circuits were theoretically planned and then built on test boards. The behavior of the test circuit was evaluated and in case of unsatisfactory results, the discrete circuit elements such as resistors, capacitors, inductors or transistors were exchanged or the topology of the circuit was altered. This method is denoted as breadboarding [49]. Having adapted the circuit and the circuit elements in such a way that the circuit behaves properly the circuit could then be fabricated. However, when it comes to the design of integrated circuits the method of breadboarding is no longer suitable. The reason is that the circuit components that are fabricated on a substrate show a different behavior than discrete elements used in a macroscopic circuit since in an integrated circuit there are additional effects such as parasitic capacitances with respect to adjacent elements [49]. Furthermore, the lengths of the interconnects of the circuit elements are quite different when comparing a macroscopic circuit to an integrated one. As a consequence, simulation programs with integrated circuit emphasis (SPICE) are nowadays used in order to simulate an integrated circuit rather than constructing it on a test board [49].

In order to use a computer-aided circuit simulation tool, the circuit simulator needs to know how the single components behave. For this purpose, mathematical equations linking the voltages to the steady-state and capacitive charging currents in the devices are necessary and a description of the noise behavior of the devices is needed. The behavior of a single device could in principle be obtained by a numerical device simulation, for example, by employing the finite element method. While these physical device simulators such as Sentaurus Technology Computer Aided Design (TCAD) [50] may show a very accurate reproduction of real devices they impose a high computational load on the central processing unit (CPU) of the computer resulting in long execution times. It may take hours or even days until one single device is simulated in a finite-element simulation. However, integrated circuits may contain hundreds of thousands of transistors or even more [49] so that conducting a physics-based device simulation for every single transistor would be impossible to solve. For this purpose, compact models are needed. A compact model is a set of mathematical equations that describes the properties of a single device in an accurate but computationally efficient manner [49, 51, 52]. Such compact models are the key components of modern electronic design automation (EDA) tools [51]. There exist different types of compact models which will briefly be explained in the following according to ref. [49].

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Physics-based models

A physics-based compact model is derived based on an analytical description of the device physics, preferably in a closed-form description. The great benefit of such models is that the parameters of the equations are entirely motivated by the device physics and allow for a scaling of the device with respect to the dimensions or the materials. Often, it is impossible to find completely closed-form descriptions so that approximations are necessary which in turn diminish the accuracy of the model. The development of such compact models is rather complicated and may take several man-years [49].

Table-lookup models

Instead of deriving physics-based equations for the model description, a very simple method is the creation of a lookup-table. The values for the lookup table can be obtained by measuring fabricated devices or by finite-element simulations. Between the values in the table, an interpolation, for example, by cubic splines is necessary. The advantage of such a table-lookup model is that it is very easy to solve and extremely quick to execute since only an interpolation between adjacent points is necessary. If, however, large numbers of values are stored in the tables the model will have huge memory requirements. Furthermore, the disadvantage is that the model is not scalable, i.e. as soon as a different device geometry is used or other material parameters are used the lookup-table needs to be filled again by finite-element simulations or measurements. Furthermore, the model is only valid for the voltage range stored in the table. The model cannot safely predict any values beyond its scope [49].

Empirical models

Empirical models are somehow comparable to table-lookup models but with the difference that they do not consist of value pairs stored in a table but rather of empirical functions that provide a description of the values. An empirical model can thus be characterized as a mathematics-based modeling where the parameters of the functions are tuned such that the model agrees well with measured curves or with the results of finite-element simulations. The advantage of such models is that they have much smaller storage requirements than table-lookup models but they may be less accurate.

In the reality, physics-based models and empirical models are often mixed. A model can be motivated by the physics but in order to capture certain effects, empirical fitting functions or fitting parameters may be introduced [49]. Nevertheless, if the model is physics-based and includes some empirical fitting or correction methods it is still denoted as a physics-based model.

For a good compact model, the following requirements can be formulated [49, 51, 52]:

- Fast execution time
- High accuracy with respect to measurements or finite-element simulations

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- Close link to the physics and consequently a possibly low number of empirical fitting parameters
- Scalability with respect to the device geometry and the materials
- Deterministic way of parameter extraction
- Numerical stability, i.e. continuity of the equations *and* of the derivatives
- Stable behavior for bias points far away from the normal operation since the simulator may apply voltages beyond the normal scope during the iterations of the non-linear circuit solver

Observing these claims, it can be said that some of them are mutually exclusive. The higher the accuracy of a model is the more side effects need to be taken into account which may result in the necessity of defining more fitting functions or parameters. In turn, a higher number of equations will lead to a larger execution time. Thus, there is no "perfect" compact model in the regard that it fulfills all claims completely. However, it is important to ensure that a numerical stability of the model is given since otherwise the model may be useless in a circuit simulator.

In the device modeling and research group at the TH Mittelhessen, such compact models for different transistors are developed. Among them is also a physics-based compact model for the static direct current (DC) behavior of OTFTs with large channel lengths [36]. This compact model is able to reproduce measured DC characteristics of OTFTs but it does not contain a description of the capacitive behavior and the noise. Thus, this PhD thesis is an advancement of the existing DC compact model. The DC equations are extended by the quasistatic and non-quasistatic charging currents arising from the charging and discharging of intrinsic and extrinsic capacitances. Furthermore, a model for the quantification of the low-frequency noise is developed. The compact model developed in this work is a physics-based model which at some points needs to be extended by empirical fitting functions.

CHAPTER 2

Charge-Based DC Model

For the description of the static DC characteristics of the OTFTs, a compact model has already been developed at the TH Mittelhessen group [36]. The DC model has been extended by Pruefer et al. in order to capture contact effects and short-channel effects, i.e. the non-linear injection of the current at the source-to-semiconductor junction and the voltage drop across the drain-to-semiconductor junction [47], as well as the effects of a drain-induced barrier lowering (DIBL), and a shift of the threshold voltage due to short channels [53].

In addition to that, the DC model in ref. [36] has been extended in order to capture the 3D effect of fringe currents in the transistors [54] and some corrections to the DC model have been performed which were published in ref. [55].

Although this thesis is dedicated to the modeling of the dynamic behavior of OTFTs, it is essential to give an overview over some aspects of the DC compact model since the dynamic model is based on the DC model and thus has a close link to the DC equations. In this chapter, a review of the most important points of the DC model will be presented.

2.1 Simple DC Model

In this section, the original version of the DC model according to ref. [36] will be reviewed. The starting point of the derivation is the density of states which is described as:

$$\Gamma(E) = \frac{N_{\mathrm{t,DOS}}}{\sqrt{2\pi}\sigma_{DOS}} \exp\left(-\frac{(E - E_{0,\mathrm{DOS}})^2}{2\sigma_{\mathrm{DOS}}^2}\right) \tag{2.1}$$

where $N_{\mathrm{t,DOS}}$ is the maximum number of states, σ_{DOS} is the standard deviation, and $E_{0,\mathrm{DOS}}$ is the center of the distribution. It has been discussed in the literature, whether it makes sense to assume the center of the Gaussian DOS exactly at the HOMO or whether it should be shifted in order to more precisely capture the effect that the states are more likely to be found beyond

the HOMO and not in the bandgap [33]. However, for the compact model, this does not play such a critical role since a shift of the Gaussian DOS results in a shift of the resulting transfer curves along the V_{gs}-axis which can be compensated later. Thus, it is now assumed that the center of the Gaussian DOS equals the valence band edge (E_{V}). In Fig. 2.1, a diagram of

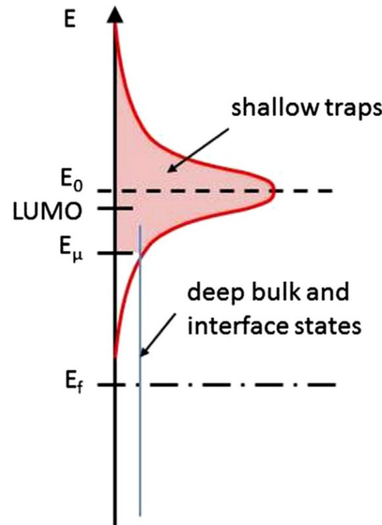

Figure 2.1.: Diagram of the Gaussian DOS which is assumed in the DC model. This picture is taken from ref. [36]. The shallow traps correspond to states in which the quasi-mobile charges are found. The deep bulk and interface states correspond to traps in the bandgap that do not contribute to the DC current but have an influence on the electrostatics.

different energetic states is shown as published in ref. [36]. The shallow traps can be observed which are the energetic states in which the charge carriers behave like quasi-mobile charges. These shallow traps are Gaussian-distributed. Furthermore, the deep bulk and interface traps are shown. Charge carriers can get trapped there but it is unlikely that they jump to adjacent traps and contribute to the DC current. However, charges in these traps influence the device electrostatics and have an influence on the threshold voltage and the sub-threshold behavior.

The density of quasi-mobile charges for an arbitrary energy is then calculated as follows:

$$Q'_{\mathrm{m}} = q d_{\mathrm{m}} \int_{E_{\mu}}^{\infty} \mathit{\Gamma}(E) f(E) dE \tag{2.2}$$

where q is the elementary charge, d_{m} is the thickness of the accumulation channel, E_{μ} is the energy at which the charge carriers are treated as quasi-mobile carriers, and $f(E)$ is the function describing the Fermi statistics. Based on this equation, it is possible to calculate the amount of charge that will be available for transport and thus contribute to the current. However, the difficulty is that the Fermi level has to be known in order to correctly relate the Fermi statistics

to the band diagram. Furthermore, the Fermi statistics are complicated to treat in combination with a Gaussian DOS. Therefore, in ref. [36], the Fermi statistics are approximated by the Boltzmann statistics. Performing several steps, the model yields a differential that links the amount of accumulated charge to the channel voltage. Originally, in ref. [36], the equation is presented for the charges at the source end of the channel but it can be formulated more general for any arbitrary point in the channel:

$$\frac{dQ'_{\mathrm{m}}}{dV_{\mathrm{g}}} = \frac{1}{\frac{\alpha V_{\mathrm{th}}}{Q'_{\mathrm{m}}} + \frac{1}{C'_{\mathrm{diel}}}} \tag{2.3}$$

where V_{g} is the gate potential, α is the slope degradation factor with respect to the ideal slope of $\approx 60\,\mathrm{mV/dec}$ at room temperature, $V_{\mathrm{th}} = k_{\mathrm{B}}T/q$ is the thermal voltage with k_{B} as the Boltzmann constant and T as the temperature, and C'_{diel} is the capacitance of the gate dielectric per gate area. This differential will become important later when the model for the total charges is derived. Based on the differential, the DC model in ref. [36] finally comes to closed-form equations for the charge densities at the source end and the drain end of the channel. The charge density can only be calculated at the endpoints of the channel. Originally, a definition of the charge densities based on the trap densities and the parameters of the Gaussian DOS is derived. However, due to the assumption of the Boltzmann statistics and due to some further fitting parameters, this trap-based formulation of the DC model is unhandy to use. In order to give a closer link to the parameters that are known to circuit designers, an equivalent threshold voltage and the sub-threshold swing are defined. Based on these parameters, the charge density equation reads as follows:

$$Q'_{\mathrm{ms/d}} = \frac{S_{\mathrm{sth}}}{\ln(10)} \cdot C'_{\mathrm{diel}} \cdot \mathcal{L}\left\{\exp\left(\frac{V_{\mathrm{gs/d}} - V_{\mathrm{T0}}}{S_{\mathrm{sth}}/\ln(10)}\right)\right\} \tag{2.4}$$

where $\mathcal{L}$ is the first branch of the Lambert W function, S_{sth} is the sub-threshold swing, V_{T0} is the threshold voltage, and V_{gs} and V_{gd} is the gate-to-source and gate-to-drain voltage, respectively. The DC current is finally based on an integration over the drift-diffusion model which leads to:

$$I_{\mathrm{ds}} = \mu W_{\mathrm{ch}} \cdot \left(\frac{k_{\mathrm{B}}T}{q} \cdot \frac{Q'_{\mathrm{ms}} - Q'_{\mathrm{md}}}{L_{ch}} + \frac{Q'^2_{\mathrm{ms}} - Q'^2_{\mathrm{md}}}{2L_{\mathrm{ch}}C'_{\mathrm{diel}}}\right) \tag{2.5}$$

where W_{ch} and L_{ch} are the channel width and length, respectively, and μ is the charge-carrier mobility. It has to be noted that this equation is only true if the slope degradation factor α is equal to one. Performing the integration over the drift-diffusion model, in principle α has to be included as a factor in the diffusion component of the current in Eq. (2.5). However, since the overall influence of the diffusion current on the total current is comparatively small, the equation presented here will be utilized and not the version incorporating α as a pre-factor in the diffusion current.

The charge-carrier mobility is described as a power-law which is often done for OTFTs [28, 29, 56, 57]. The mobility then reads as:

$$\mu = \kappa \cdot \left(\frac{Q'_{\mathrm{ms}}}{C'_{\mathrm{diel}}} \right)^{\beta} \tag{2.6}$$

where $\kappa\,[\mathrm{cm^2 V^{-\beta-1} s^{-1}}]$ is the so-called low-field mobility and β is the unitless exponent of the power-law. The next step is the inclusion of a channel-length modulation in order to represent the effect that the transistor does not show a perfectly constant current with respect to the drain-source voltage V_{ds} when operated in saturation. An auxiliary voltage controlling the saturation is defined as follows:

$$V_{\mathrm{dsx}} = \frac{1}{C'_{\mathrm{diel}}} \cdot \left(Q'_{\mathrm{ms}} - Q'_{\mathrm{md,barr}} \right) \tag{2.7}$$

where $Q'_{\mathrm{md,barr}}$ is the charge density per gate area at the drain end of the channel after the reduction of the drain-source voltage by the voltage drop over the Schottky barrier at the drain as presented in Eq. (2.17) later. Finally, the model allows the inclusion of a contact resistance. Following the principle in ref. [58], a contact resistance is included in terms of an effective mobility:

$$\mu_{\mathrm{eff}} = \frac{\mu}{1 + \mu \cdot \frac{W_{\mathrm{ch}}}{L_{\mathrm{ch}}} \cdot (R_{\mathrm{contact}} + R_{\mathrm{sb,s}}) \cdot Q'_{\mathrm{ms}}} \tag{2.8}$$

where R_{contact} and $R_{\mathrm{sb,s}}$ are the series resistances to be included. With these definitions, the drain current of the simple model finally reads as follows:

$$I_{\mathrm{ds}} = \mu_{\mathrm{eff}} \cdot W_{\mathrm{ch}} \cdot \left(\frac{k_{\mathrm{B}} \cdot T}{q} \cdot \frac{Q'_{\mathrm{ms}} - Q'_{\mathrm{md,barr}}}{L_{\mathrm{ch}}} + \frac{Q'^2_{\mathrm{ms}} - Q'^2_{\mathrm{md,barr}}}{2 \cdot L_{\mathrm{ch}} \cdot C'_{\mathrm{diel}}} \right) \cdot (1 + \lambda \cdot (V_{\mathrm{ds}} - V_{\mathrm{dsx}})) \tag{2.9}$$

where λ is the channel length modulation factor. The contact resistance consists of two components. One of these is a constant Ohmic contact resistance denoted as R_{contact} which depends on the transistor structure. In coplanar transistors, R_{contact} is simply constant but in staggered transistors, the situation is a little more difficult. Figure 2.2 shows a staggered OTFT in which the current injection in the source overlap region is shown. The current has

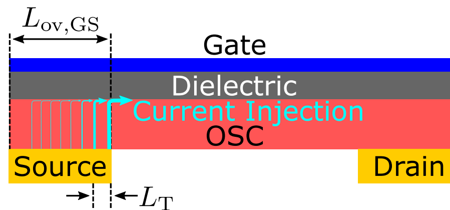

Figure 2.2.: Sketch of a staggered OTFT where the current injection is depicted. This principle is adapted from ref. [59]. The density of the injected current is higher in proximity to the source end of the channel which is emphasized by the different thicknesses of the cyan-colored arrows. The transfer length L_{T} is defined as the length in which 63 % of the current is injected.

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to travel from the electrode normal to the channel direction and is diverted close to the gate dielectric towards the channel direction. The density of the injected current varies along the gate-to-source overlap length and is significantly reduced farther away from the source end of the channel. This principle is taken from ref. [59] where the contact resistance is described based on the sheet resistance (R_{sheet}) of the organic semiconductor layer, the transfer length (L_{T}) in which 63 % of the current is injected, and the gate-to-source overlap length ($L_{\text{ov,GS}}$):

$$R_{\text{contact}} = 2 \cdot \frac{R_{\text{sheet}}}{W_{\text{ch}}} \cdot L_{\text{T}} \cdot \coth\left(\frac{L_{\text{ov,GS}}}{L_{\text{T}}}\right). \tag{2.10}$$

In addition to the constant resistance R_{contact}, the contact resistance also includes the effect of a non-linear current injection at the source-to-semiconductor junction which will be reviewed in the following section.

2.2 Workfunction Mismatch

The metal-to-semiconductor junctions in OTFTs behave like Schottky barriers. In ref. [47], the influence of the Schottky barriers on the static drain current characteristics are investigated in detail. If the transistor is operated in a normal operation point (e.g. the above-threshold regime), the Schottky barrier at the source end of the channel is operated in reverse direction whereas the Schottky barrier at the drain is operated in forward direction. Both of the Schottky barriers are non-linear, parasitic contact resistances and can have a major influence on the current-voltage characteristics of the transistor. Due to the reverse operation of the source Schottky barrier its resistance will be much higher than the resistance of the drain barrier. The model in ref. [47] provides closed-form equations for the non-linear resistance of the source Schottky barrier and the estimated voltage drop over the drain Schottky barrier. The effect of a Schottky barrier lowering due to image charges [46] is taken into account which allows for a description of the S-shape effect in the linear regime of operation of the transistor. A full review of ref. [47] will not be presented here but some of the equations are needed later for the short-channel extension of the dynamic model. Therefore, a short overview over some of the

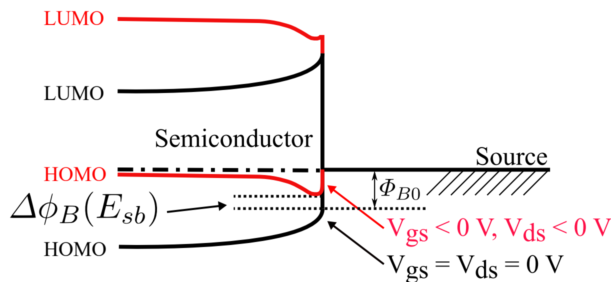

Figure 2.3.: Band diagram of the transistor at the source-to-semiconductor junction of the organic transistor. Due to an electric field E_{sb} the height of the Schottky barrier can be lowered. This figure is taken from ref. [47].

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concepts presented there will be given. Figure 2.3 shows the band diagram of an OTFT at the source-to-semiconductor junction. An electric field can lead to the already mentioned effect of a Schottky barrier lowering. Applying a conformal mapping technique, the electric field in both transistor architectures (staggered and coplanar) is calculated. The model describes the influence of the reversely operated Schottky barrier at the source by means of a contact resistance ($R_{\mathrm{sb,s}}$) which is added to the Ohmic component of the contact resistance in Eq. (2.8).

The resistance of the source Schottky barrier is denoted as $R_{\mathrm{sb,s}}$ which is a function of the applied voltages and the device geometry and materials. The model in ref. [47] estimates the voltage drop over the source Schottky barrier but this voltage drop cannot be calculated precisely. In principle, the current through a series connection of a transistor and a reversely driven Schottky barrier at the source terminal would have to be calculated numerically, e.g. by making use of the Newton algorithm. However, the model in [47] circumvents this by the definition of the barrier resistance $R_{\mathrm{sb,s}}$:

$$R_{\mathrm{sb,s}} = \frac{V_{\mathrm{sb,s}}}{-I_{\mathrm{s,s}} \cdot \left(\exp\left(\frac{-qV_{\mathrm{sb,s}}}{\theta k_{\mathrm{B}} T}\right) - 1\right)} \tag{2.11}$$

where $V_{\mathrm{sb,s}}$ is the estimated voltage drop over the Schottky barrier, $I_{\mathrm{s,s}}$ is the reverse-bias saturation current of the diode, and θ is a fitting parameter describing the non-ideality of the diode. The estimated voltage drop $V_{\mathrm{sb,s}}$ is very similar to the voltage V_{dsx} but here the charge density Q'_{md} is used before the voltage is reduced due to the drain contact:

$$V_{\mathrm{sb,s}} = \frac{Q'_{\mathrm{ms}} - Q'_{\mathrm{md}}}{C'_{\mathrm{diel}}}. \tag{2.12}$$

The reverse-bias saturation current of the diode is defined as follows:

$$I_{\mathrm{s,s}} = W_{\mathrm{ch}} L_{\mathrm{inj}} A^{\star} T^2 \exp\left(\frac{-q\left(\Phi_{\mathrm{B0}} - \Delta\Phi_{\mathrm{B}}\right)}{\eta k_{\mathrm{B}} T}\right) \tag{2.13}$$

where L_{inj} is the injection length in which the main part of the current is injected, $A^{\star}$ is the effective Richardson constant, η is a fitting-parameter, Φ_{B0} is the initial barrier height, and $\Delta\Phi_{\mathrm{B}}$ is the amount by which the Schottky barrier is lowered. This amount is dependent on the electric field across the barrier and varies between the two transistor architectures. A detailed review of ref. [47] will not be presented here. The injection length L_{inj} is also dependent on the transistor architecture. In staggered transistors, L_{inj} is equal to the transfer length L_{T} in which 63 % of the current is injected. By contrast, in coplanar transistors, the injection length is equal to the thickness of the charge-carrier channel.

Since the Schottky barrier at the drain is operated in forward direction it has a lower resistance compared to the Schottky barrier at the source. Furthermore, there is an interesting property: For higher voltages, a forward-driven Schottky diode becomes increasingly conductive. By contrast, a transistor is driven into saturation as the drain-source voltage is increased. Consequently, at very high drain-source voltages, the series connection of an inner transistor and a forward-driven drain Schottky barrier saturates to the same current as a transistor without barrier would do. However, the saturation sets on a little bit later under the presence of a drain Schottky barrier which can be verified by observing Fig. 6 (b) in ref. [47]. It proved to be sufficient to model the voltage drop over the drain Schottky barrier in the linear operation regime of the transistor as a linear function of V_{ds} until at a certain voltage the saturation sets on. Generally, the investigation of the drain barrier starts at a similar point as the investigation of the source barrier. Theoretically, the drain barrier could not analytically be included in a compact model but would require the numerical calculation by a method like the Newton algorithm. However, a closed form description with good accuracy is derived in ref. [47]. The current through the drain barrier can be described as follows:

$$I_{\mathrm{D,d}} = I_{\mathrm{s,d}} \cdot \left(\exp\left(\frac{qV_{\mathrm{sb,d}}}{\theta k_{\mathrm{B}} T} \right) - 1 \right) \tag{2.14}$$

where $I_{\mathrm{s,d}}$ is the reverse-bias saturation current of the diode and $V_{\mathrm{sb,d}}$ is the voltage drop across the drain barrier. $I_{\mathrm{s,d}}$ is very similar to that of the source diode but here the effect of the Schottky barrier lowering does not have to be taken into account:

$$I_{\mathrm{s,d}} = W_{\mathrm{ch}} L_{\mathrm{inj}} A^{\star} T^2 \exp\left(\frac{-q\Phi_{\mathrm{B0}}}{\eta k_{\mathrm{B}} T} \right). \tag{2.15}$$

As explained above, in deep saturation, a transistor with a drain Schottky barrier will conduct the same current as a transistor without such a barrier. Making use of this, the voltage drop $V_{\mathrm{ds,V_{sbd,sat}}}$ over the Schottky barrier can be calculated in the saturation regime of operation. The voltage drop $V_{\mathrm{sb,d}}$ is then calculated as a linear function of Q'_{ms} until it finally saturates to a value defined as

$$V_{\mathrm{ds,V_{sbd,sat}}} = w_{\mathrm{sat}} \frac{Q'_{\mathrm{ms}}}{C'_{\mathrm{diel}}} \tag{2.16}$$

where w_{sat} is a fitting parameter that controls at which point the saturation starts. The final equation for $V_{\mathrm{sb,d}}$ is not presented here. The reader is kindly asked to refer to ref. [47]. In contrast to the source Schottky barrier, the barrier at the drain is included in the compact model by the voltage drop $V_{\mathrm{sb,d}}$. Accordingly, the charge density at the drain end of the channel has to be recalculated taking into account $V_{\mathrm{sb,d}}$:

$$Q'_{\mathrm{md,barr}} = \frac{S_{\mathrm{sth}}}{\ln(10)} C'_{\mathrm{diel}} \mathcal{L} \left\{ \exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}} - V_{\mathrm{ds}} + V_{\mathrm{sb,d}}}{S_{\mathrm{sth}}/\ln(10)} \right) \right\}. \tag{2.17}$$

In the final current equation, instead of Q'_{md}, the new charge density $Q'_{\mathrm{md,barr}}$ is used.

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2.3 Fringe Effects

The equations presented so far are based on a quite simple two-dimensional view on the transistors. However, there are three-dimensional effects to be taken into account. Due to the fabrication process, the organic semiconductor layer extends beyond the intrinsic transistor and constitutes so-called fringe regions. Furthermore, in order to provide stability to the silicon stencil masks used for patterning, the openings in the mask are often chosen to be comparatively small [42]. This would limit the channel width that could be fabricated. Even if the performance of OTFTs is continuously increasing, the mobility of organic semiconductors is still small in comparison to that of common crystalline semiconductors [9]. Therefore, in order to achieve a sufficiently high current in an OTFT, the channel width has to be increased. Since in the silicon stencil lithography the width of one electrode is limited the transistors can be fabricated in a multi-finger structure. This is in principle a parallel connection of several identical transistors. Special emphasis has been put on such multi-finger structures as presented in [54, 55]. The modeling thoughts will be reviewed here.

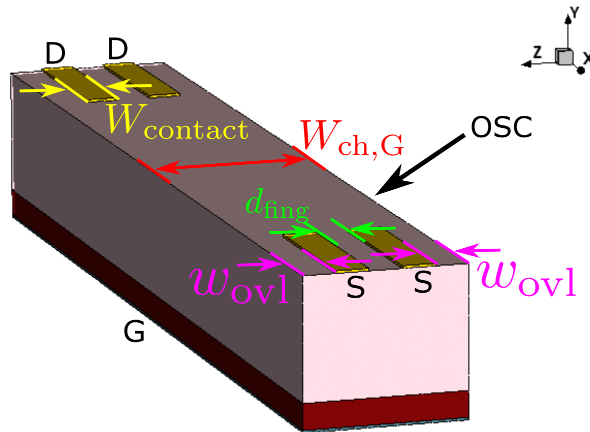

Figure 2.4.: Three-dimensional sketch of a staggered OTFT as simulated in Sentaurus TCAD [50]. This picture was published in ref. [54] and was extended by some labels. Due to the fabrication process there are regions between and beyond the source/drain electrodes and the intrinsic channel regions. These are denoted as fringe regions.

Figure 2.4 shows a three-dimensional sketch of a staggered OTFT as simulated in Sentaurus TCAD [50]. Here, a transistor comprising two source and two drain electrodes is shown. The little pictogram in the top right corner shows the orientation of the coordinate system. The width of a single finger is denoted as W_{contact}. Between two fingers, there is an unpatterned region of width d_{fing}. Beyond the first and the last finger, the organic semiconductor layer is also marginally extended. The width of this region is denoted as w_{ovl}. For the modeling, this width is assumed to be symmetrically present at both ends of the transistor. The complete width of the transistor is denoted as the gate width $W_{\mathrm{ch,G}}$. This width will be important for

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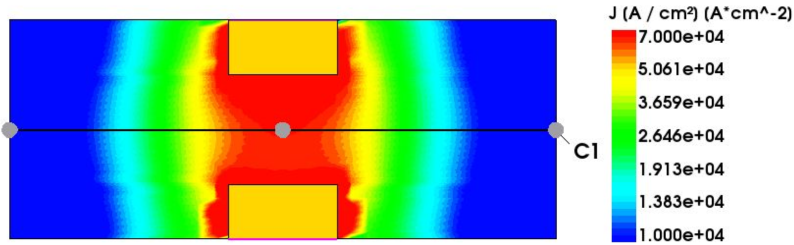
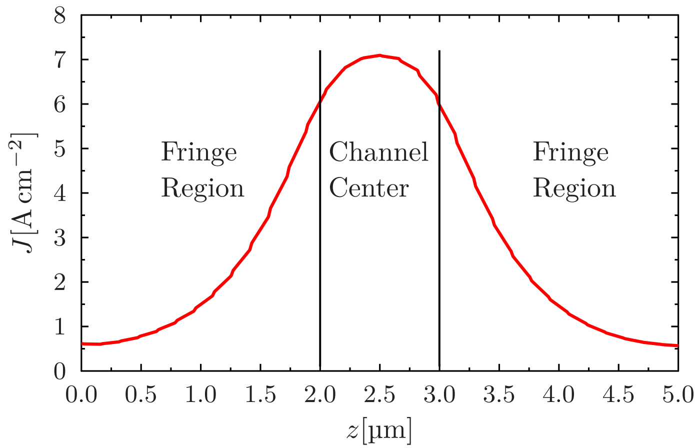
the calculation of the total charges since charges are accumulated at every position where the gate stack consisting of the gate electrode and the gate dielectric is in contact with the organic semiconductor.



(a)



(b)

Figure 2.5.: 3D Sentaurus TCAD simulation of a coplanar OTFT. (a) The current density in a cutplane close to the gate dielectric is shown. (b) Current density along the cutline C1. The current density decreases beyond the channel center.

The presence of fringe regions opens further current paths. Figure 2.5 shows the results of a 3D Sentaurus TCAD simulation of a coplanar OTFT. It can be seen that a current flows beyond the channel center but the current density is reduced farther away from the channel. The effect of the current spreading is schematically depicted in Fig. 2.6 where two cutplanes of coplanar single-finger transistor geometries with an identical finger width W_{contact} but different fringe widths w_{ovl} are shown. The dark-blue arrows indicate the part of the current that flows in the center of the intrinsic transistor. The cyan-colored arrows indicate the fringe currents that flow beyond the channel center. It is obvious that the amount of fringe currents is dependent on the fringe width w_{ovl}. The same principles apply to both kinds of geometries (staggered and coplanar). The difficulty is that from a static DC measurement the contributions from

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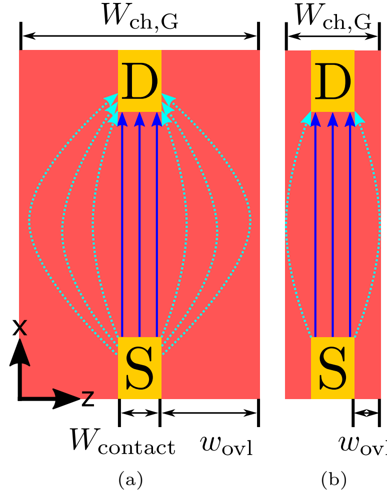

Figure 2.6.: Current paths in a cutplane in a coplanar transistor comprising fringe regions. A transistor with one finger is shown. (a) The fringe width w_{ovl} is large and a huge amount of current can flow beyond the channel center. However, the amount of fringe current is limited because the current paths farther away from the intrinsic channel center are longer and have higher resistances. (b) The fringe width w_{ovl} is rather small and only a little amount of current flows beyond the center of the intrinsic transistor.

the intrinsic transistor current and the fringe currents cannot be separated from each other. If compact models are fitted to such measurements it often leads to a mobility overestimation [60]. In the literature, the fringe part is sometimes accounted for by defining it as a certain percentage of the intrinsic DC current [40, 61]. Other researchers also considered these fringe currents [41] and proposed analytical methods for its calculation by a conformal mapping technique [62]. A quite simple and empirical model has been developed which despite its simplicity creates the necessary basis for the calculation of the total charges later. The model concept that was presented in refs. [54, 55] will be reviewed here.

Looking at the fringe currents from a practical point of view, a pre-factor before the current equation is needed that increases the current. As stated before, the mobility could be overestimated in order to fit the current [60] but it was decided to incorporate the fringe currents in the model by defining an effective channel width. First, some geometric dimensions are defined. The total gate width $W_{ch,G}$ is the width of the whole transistor consisting of all regions:

$$W_{ch,G} = N_{fing} \cdot W_{contact} + 2 \cdot w_{ovl} + (N_{fing} - 1) \cdot d_{fing} \tag{2.18}$$

where N_{fing} is the number of fingers. The sum of the geometric finger widths is defined as

$$W_{ch,SD} = N_{fing} \cdot W_{contact}. \tag{2.19}$$

Without any fringe model, this width $W_{\mathrm{ch,SD}}$ would be used as the channel width in the compact model. For the inclusion of the fringe effects, an effective channel width is defined:

$$W_{\mathrm{ch,eff}} = \delta_{\mathrm{fit}} \cdot (W_{\mathrm{ch,G}} - W_{\mathrm{ch,SD}}) + W_{\mathrm{ch,SD}} \tag{2.20}$$

where $\delta_{\mathrm{fit}} \in [0,1]$ is an empirical fitting parameter. Figuratively speaking, if δ_{fit} is set to zero, the effective channel width equals the sum of the electrode widths. If δ_{fit} is set to one, the whole width of the transistor is used as the channel width. It is worth noting that this method is not capable of predicting the fringe part of the current of an arbitrary transistor geometry. Based on a TCAD simulation, it is possible to determine meaningful values of δ_{fit}. However, as will be seen later in the derivation of the charge model, the value assigned to δ_{fit} does not have any influence on the total charges and capacitances. It is, however, necessary to define the gate width $W_{\mathrm{ch,G}}$ and the sum of the electrode widths $W_{\mathrm{ch,SD}}$ separately.

The formulation of the effective channel width used in this work implies that each of the single fingers of the transistor can be regarded as independent single-finger transistors where the total current results from their superposition. Thus, in the region between two fingers, the currents of both adjacent fingers flows which when superposed yields the total current flowing in this region. With the definition of the effective channel width, the DC compact model is reformulated:

$$I_{\mathrm{ds}} = \mu_{\mathrm{eff}} \cdot W_{\mathrm{ch,eff}} \cdot \left(\frac{k_{\mathrm{B}} \cdot T}{q} \cdot \frac{Q'_{\mathrm{ms}} - Q'_{\mathrm{md,barr}}}{L_{\mathrm{ch}}} + \frac{Q'^{2}_{\mathrm{ms}} - Q'^{2}_{\mathrm{md,barr}}}{2 \cdot L_{\mathrm{ch}} \cdot C'_{\mathrm{diel}}} \right) \cdot (1 + \lambda \cdot (V_{\mathrm{ds}} - V_{\mathrm{dsx}})) \,. \tag{2.21}$$

Furthermore, the effective channel width is also used in the mobility which leads to

$$\mu_{\mathrm{eff}} = \frac{\mu}{1 + \mu \cdot \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \cdot (R_{\mathrm{contact}} + R_{\mathrm{sb,s}}) \cdot Q'_{\mathrm{ms}}} \,. \tag{2.22}$$

As a last point, it has to be mentioned that the Ohmic part of the contact resistance in staggered OTFTs has to be reformulated as well:

$$R_{\mathrm{contact}} = 2 \cdot \frac{R_{\mathrm{sheet}}}{W_{\mathrm{ch,SD}}} \cdot L_{\mathrm{T}} \cdot \coth\left(\frac{L_{\mathrm{ov,GS}}}{L_{\mathrm{T}}}\right) . \tag{2.23}$$

Since the injection of the current occurs only in those regions where the source electrode is in direct contact with the organic semiconductor the geometric channel width $W_{\mathrm{ch,SD}}$, which is the sum of all of the finger widths, is used in this equation.

2.4 Compensation of the Threshold-Voltage Shift and a Slope Change

2.4.1 Introduction

The charge-based DC model incorporates a power-law mobility model according to Eq. (2.6). In the literature, such power-law mobility models are also reported [57, 63]. Theoretically, this power-law mobility should have an influence only on the above-threshold regime of operation. However, an investigation of the compact DC model [36] has shown that there is an undesired and non-negligible influence of the power-law mobility on the sub-threshold regime of operation. The

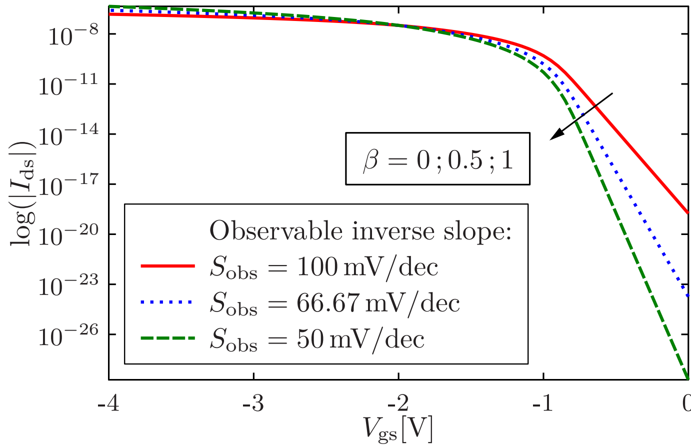

Figure 2.7.: Transfer curves of a staggered OTFT as calculated by the compact model for three different values of the power-law exponent β at $V_{ds} = -1\,V$. The sub-threshold swing is set to $S_{sth} = 100\,mV/dec$ but it is clearly visible that with a change in β the model exhibits different sub-threshold swings. The legend shows the sub-threshold swing that the curves really exhibit. The remaining compact model parameters are equal for every curve. Since the problem is not dependent on the other fitting parameters, they are not listed here. This figure was published in ref. [55] and slightly modified.

problem can be visualized by plotting the transfer curves of the compact model in a logarithmic scale at the current axis for different values of β and then observing the sub-threshold behavior, see Fig. 2.7. Even if the sub-threshold swing is set to a value of $S_{sth} = 100\,mV/dec$, it can be seen that only for $\beta = 0$ the model really exhibits a swing of $100\,mV/dec$. As β is increased, the sub-threshold swing that the model really exhibits is significantly reduced which is of course an undesired behavior. Furthermore, which will become visible in the course of this section, the threshold voltage is also affected by the power-law mobility. In the next paragraphs, equations that compensate the influence of the power-law mobility on the sub-threshold swing and the threshold voltage will be derived. These equations were published in ref. [55].

2.4.2 De-Coupling of the Sub-Threshold Swing from the Power-Law Mobility

The first step is to derive an equation for the de-coupling of the sub-threshold swing from the power-law mobility. The starting point of this derivation is the mobility. As explained above, the mobility incorporates contact effects which leads to the formulation of an effective mobility according to Eq. (2.22). Since for this investigation a sub-threshold operation point is assumed the mobility can be simplified: In the sub-threshold regime of operation, the charge density Q'_{ms} is very low. Consequently, the second summand in the denominator of Eq. (2.22) becomes notably smaller than the first summand and the mobility reduces to the power-law mobility according to Eq. (2.6). This makes sense from a practical point of view: When operated in the sub-threshold regime of operation, the depleted transistor channel has a high Ohmic resistance. The channel resistance can become orders of magnitude larger than the contact resistance and hence, the contact resistance does not have a notable influence on the total current. The mobility in the off-state reads as:

$$\mu_{\mathrm{off}} = \kappa \cdot \left(\frac{Q'_{\mathrm{ms,off}}}{C'_{\mathrm{diel}}} \right)^{\beta} \tag{2.24}$$

where $Q'_{\mathrm{ms,off}}$ is the charge density per gate area at the source end of the channel in the off-state of the transistor, i.e. in a sub-threshold operation point. Next, it is desired to find a simplified expression for the off-state charge densities. The charge density at the source/drain end of the channel is given by Eq. (2.4) which is presented here again in order to improve the reading flow:

$$Q'_{\mathrm{ms/d}} = \frac{S_{\mathrm{sth}}}{\ln(10)} \cdot C'_{\mathrm{diel}} \cdot \mathcal{L} \left\{ \exp\left(\frac{V_{\mathrm{gs/d}} - V_{\mathrm{T0}}}{S_{\mathrm{sth}} / \ln(10)} \right) \right\}.$$

The Lambert W function is the inverse function of the problem

$$y = x \cdot \exp(x). \tag{2.25}$$

This equation cannot analytically be rearranged for x but by means of the Lambert W function, which can be solved by e.g. a Taylor series, it can anyhow be rearranged for x:

$$x = \mathcal{L}(y). \tag{2.26}$$

Suppose that the value of x is close to zero. Then, in Eq. (2.25), the exponential function is nearly one and the equation simplifies to

$$y \approx x. \tag{2.27}$$

Substituting this simple result in Eq. (2.26) leads to

$$\mathcal{L}(x) \approx x. \tag{2.28}$$

In other words: For very small arguments, the Lambert W function nearly behaves as a linear function. This fact is useful with regard to Eq. (2.4): When operated in the sub-threshold regime, the numerator of the exponential function within the Lambert W function becomes negative. The value of the exponential function is thus close to zero and as a consequence, the Lambert W function almost returns the value of its argument. Thus, the charge densities can be written in this greatly simplified form:

$$Q'_{\mathrm{ms/d,off}} = \frac{S_{\mathrm{sth}}}{\ln(10)} \cdot C'_{\mathrm{diel}} \cdot \exp\left(\frac{V_{\mathrm{gs/d}} - V_{\mathrm{T0}}}{S_{\mathrm{sth}}/\ln(10)}\right). \tag{2.29}$$

Having performed these simplifications, the off-state charge density $Q'_{\mathrm{ms,off}}$ can be incorporated into the off-state mobility (Eq. (2.24)) which leads to:

$$\begin{aligned}\mu_{\mathrm{off}} &= \kappa \cdot \left(\frac{S_{\mathrm{sth}}}{\ln(10)} \cdot \exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}}}{S_{\mathrm{sth}}/\ln(10)}\right)\right)^{\beta} \\ &= \kappa \cdot \left(\frac{S_{\mathrm{sth}}}{\ln(10)}\right)^{\beta} \cdot \exp\left(\beta \cdot \frac{V_{\mathrm{gs}} - V_{\mathrm{T0}}}{S_{\mathrm{sth}}/\ln(10)}\right).\end{aligned} \tag{2.30}$$

The next step is to observe the current equation. For convenience, the current equation (Eq. (2.21)) is shown again:

$$I_{\mathrm{ds}} = \mu_{\mathrm{eff}} \cdot W_{\mathrm{ch,eff}} \cdot \left(\frac{k_{\mathrm{B}} \cdot T}{q} \cdot \frac{Q'_{\mathrm{ms}} - Q'_{\mathrm{md,barr}}}{L_{\mathrm{ch}}} + \frac{Q'^{2}_{\mathrm{ms}} - Q'^{2}_{\mathrm{md,barr}}}{2 \cdot L_{\mathrm{ch}} \cdot C'_{\mathrm{diel}}}\right) \cdot (1 + \lambda \cdot (V_{\mathrm{ds}} - V_{\mathrm{dsx}})).$$

In order to simplify the further derivation, this equation is also simplified. First, one can say that since the transistor is operated in the sub-threshold regime of operation, the contact resistances will have a minor influence. Therefore, the charge density at the drain end of the channel can be calculated without considering the voltage drop across the drain Schottky barrier: $Q'_{\mathrm{md,barr}} \approx Q'_{\mathrm{md}}$. The validity of this assumption can be verified by simulating two transistors of which one has a barrier at the drain-to-semiconductor junction and one has no barrier, and showing that the currents in the sub-threshold regime are equal [47]. Furthermore, in the sub-threshold regime of operation, the channel-length modulation is not of interest and it is neglected here. A third simplification concerns the different components that the current consists of: The summands where Q'_{ms} and Q'_{md} are contained to the power of one represent a diffusion current whereas the summands containing Q'_{ms} and Q'_{md} to the power of two represent a drift current. Since Q'_{ms} and Q'_{md} are small in the sub-threshold regime of operation their quadrature yields even smaller values. Consequently, in accordance with the theory [39], the diffusion current dominates the overall current in the sub-threshold regime of operation and the drift current can be neglected. These three assumptions lead to the following expression for the off-state drain current:

$$I_{\mathrm{ds,off}} = \mu_{\mathrm{off}} \cdot \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \cdot \frac{k_{\mathrm{B}} T}{q} \left(Q'_{\mathrm{ms,off}} - Q'_{\mathrm{md,off}}\right). \tag{2.31}$$

Subsequently, the off-state mobility (Eq. (2.30)) and the off-state charge densities (Eq. (2.29)) are inserted in this equation which leads to

$$\begin{aligned} I_{\mathrm{ds,off}} =& \kappa \cdot \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \cdot \frac{k_{\mathrm{B}}T}{q} \cdot \left(\frac{S_{\mathrm{sth}}}{\ln(10)}\right)^{\beta} \cdot \exp\left(\beta \cdot \frac{V_{\mathrm{gs}} - V_{\mathrm{T0}}}{S_{\mathrm{sth}}/\ln(10)}\right) \\ & \times \left(\frac{S_{\mathrm{sth}}}{\ln(10)} \cdot C'_{diel} \cdot \exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}}}{S_{\mathrm{sth}}/\ln(10)}\right) - \frac{S_{\mathrm{sth}}}{\ln(10)} \cdot C'_{diel} \cdot \exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{ds}} - V_{\mathrm{T0}}}{S_{\mathrm{sth}}/\ln(10)}\right)\right). \end{aligned} \tag{2.32}$$

This equation can be rearranged and the exponential laws can be applied which leads to the following expression:

$$\begin{aligned} I_{\mathrm{ds,off}} =& \kappa \cdot \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \cdot \frac{k_{\mathrm{B}}T}{q} \cdot \left(\frac{S_{\mathrm{sth}}}{\ln(10)}\right)^{\beta+1} \cdot C'_{\mathrm{diel}} \\ & \times \exp\left((\beta+1)\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}}}{S_{\mathrm{sth}}/\ln(10)}\right) \cdot \left(1 - \exp\left(\frac{-V_{\mathrm{ds}}}{S_{\mathrm{sth}}/\ln(10)}\right)\right). \end{aligned} \tag{2.33}$$

Please recall that this equation represents the off-state current of the DC model. All the simplifications and assumptions do not diminish the validity of the equations so long as the model is operated in the deep sub-threshold regime. Observing Eq. (2.33), an interesting effect becomes visible: The off-state current has a dependence on the drain-source voltage V_{ds}. This can lead to a behavior in the transfer curves of the transistor which resembles the DIBL effect as reported in ref. [36]. It can be seen that this effect is exponentially depending on $-V_{\mathrm{ds}}$ which means that with higher values of V_{ds} (in the context of an n-type transistor) the influence becomes smaller until finally, at very high V_{ds}, the effect is no longer visible. Furthermore, in the exponential function, $-V_{\mathrm{ds}}$ is divided by the sub-threshold swing S_{sth}. The consequence of this is that a transistor with a large sub-threshold swing needs a larger V_{ds} in order to achieve a sufficiently large negative argument for the exponential function. Hence, the quasi-DIBL effect is more pronounced in transistors with large sub-threshold swings. This is in accordance with the findings in ref. [36]. The effect mentioned here must not be mistaken with the *real* DIBL effect which is the lowering of the barrier between source and drain due to the drain-source voltage [53].

Now, the derivation of the compensation equation for the influence of the power-law exponent on the sub-threshold swing will be resumed. In order to simplify the readability, a constant C_1 is defined containing all those factors of Eq. (2.33) that are independent of the gate-source voltage:

$$C_1 = \kappa \cdot \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \cdot \frac{k_{\mathrm{B}}T}{q} \cdot \left(\frac{S_{\mathrm{sth}}}{\ln(10)}\right)^{\beta+1} \cdot C'_{\mathrm{diel}} \cdot \left(1 - \exp\left(\frac{-V_{\mathrm{ds}}}{S_{\mathrm{sth}}/\ln(10)}\right)\right). \tag{2.34}$$

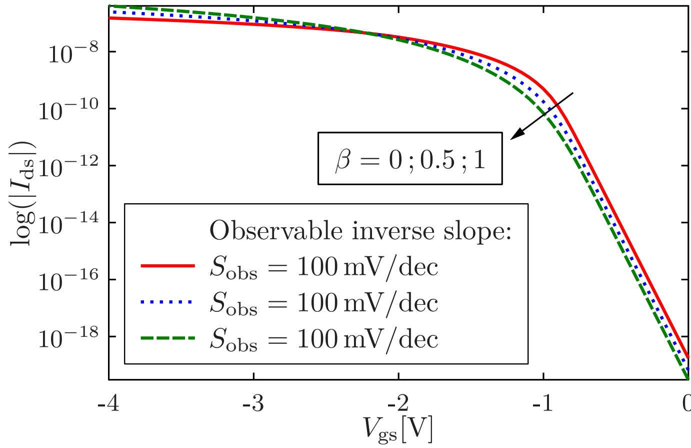

Figure 2.8.: Transfer curves of a staggered OTFT as calculated by the compact model for three different values of the power-law exponent β at $V_{ds} = -1\,\mathrm{V}$. The sub-threshold swing is set to $S_{obs} = 100\,\mathrm{mV/dec}$ and the de-coupling equation Eq. (2.39) is used. The model now exhibits a constant sub-threshold swing for all different values of β. However, the curves are shifted along the V_{gs} axis. This figure was published in ref. [55] and slightly modified.

With this definition, Eq. (2.33) can be written as

$$I_{ds,off} = C_1 \cdot \exp\left((\beta+1)\,\frac{V_{gs} - V_{T0}}{S_{sth}/\ln(10)}\right). \tag{2.35}$$

The goal of the derivations so far is to calculate the observable sub-threshold swing S_{obs} that the model *really* exhibits. From Fig. 2.7 it is known that the model obviously exhibits a different measurable sub-threshold swing S_{obs} than the value S_{sth} which is set as a model parameter. In order to provide a de-coupling equation, S_{obs} needs to be known in dependence of S_{sth} and β. For this purpose, the logarithm to base 10 of Eq. (2.35) is calculated leading to

$$\begin{aligned}\log_{10}(I_{ds,off}) &= \log_{10}(C_1) + \log_{10}\left(\exp\left((\beta+1)\,\frac{V_{gs} - V_{T0}}{S_{sth}/\ln(10)}\right)\right)\\ &= \log_{10}(C_1) + \left((\beta+1)\,\frac{V_{gs} - V_{T0}}{S_{sth}/\ln(10)}\right)\cdot \log_{10}(e)\end{aligned} \tag{2.36}$$

where it can be made use of the fact that $\log_{10}(e) = 1/\ln(10)$ which leads to

$$\log_{10}(I_{ds,off}) = \log_{10}(C_1) + (\beta+1)\,\frac{V_{gs} - V_{T0}}{S_{sth}}. \tag{2.37}$$

Now, the sub-threshold swing S_{obs} that the model exhibits can be calculated by deriving the current in logarithmic scale with respect to the voltage and taking the inverse value of that:

$$S_{obs} = \frac{dV_{gs}}{d\log_{10}(I_{ds,off})} = \frac{S_{sth}}{(\beta+1)}. \tag{2.38}$$

The essence of this equation is that only for the case that $\beta = 0$, the compact model exhibits the sub-threshold swing that is entered in the model parameters. If, for example, $\beta = 1$, the model will show a swing that is only half of the swing entered in the model parameters. This is exactly the behavior that can be observed in Fig. 2.7. Now, a de-coupling equation for the sub-threshold swing from the power-law exponent has been derived. The user enters the sub-threshold swing S_{obs} that the model should exhibit but internally the value is multiplied by $(\beta + 1)$:

$$S_{\text{sth}} = S_{\text{obs}} \cdot (\beta + 1)\,. \tag{2.39}$$

The charge densities at the source/drain end of the channel are now expressed as follows:

$$Q'_{\text{ms/d}} = \frac{(\beta + 1) \cdot S_{\text{obs}}}{\ln(10)} \cdot C'_{\text{diel}} \cdot \mathcal{L}\left\{\exp\left(\frac{V_{\text{gs/d}} - V_{\text{T0}}}{(\beta + 1) \cdot S_{\text{obs}}/\ln(10)}\right)\right\}. \tag{2.40}$$

Figure 2.8 shows the results of the compact model where this de-coupling equation is used. It can be seen that the model now shows a constant sub-threshold swing independent of β. However, a new problem appears: The three curves are shifted along the V_{gs} axis in the deep sub-threshold regime. From the circuit designer's perspective, this behavior is undesired because a tuning of β should only lead to a change in the shape of the above-threshold current but not in the threshold voltage. Therefore, in the next section, a de-coupling function of the threshold voltage from the power-law exponent will be developed.

2.4.3 De-Coupling of the Threshold Voltage from the Power-Law Mobility

As explained in the section before, the threshold voltage should be independent of the exponent of the power-law mobility. The goal is to define a shift of the threshold voltage depending on the power-law exponent:

$$\mathit{\Delta} V_{\text{T0}} = f(\beta) \tag{2.41}$$

which can then be incorporated into the charge densities at the source/drain end of the channel. The charge densities at the source/drain end of the channel are then expressed as follows:

$$Q'_{\text{ms/d}} = \frac{(\beta + 1) \cdot S_{\text{obs}}}{\ln(10)} \cdot C'_{\text{diel}} \cdot \mathcal{L}\left\{\exp\left(\frac{V_{\text{gs/d}} - V_{\text{T0}} - \mathit{\Delta} V_{\text{T0}}}{(\beta + 1) \cdot S_{\text{obs}}/\ln(10)}\right)\right\}. \tag{2.42}$$

Making again use of the fact that in the sub-threshold regime of operation the Lambert W function approximately returns its argument, this equation can be simplified:

$$Q'_{\text{ms/d,off}} = \frac{(\beta + 1) \cdot S_{\text{obs}}}{\ln(10)} \cdot C'_{\text{diel}} \cdot \exp\left(\frac{V_{\text{gs/d}} - V_{\text{T0}} - \mathit{\Delta} V_{\text{T0}}}{(\beta + 1) \cdot S_{\text{obs}}/\ln(10)}\right). \tag{2.43}$$

The starting point of the derivations is the following claim: The compact model should always lead to the same off-state current, independent of whether $\beta = 0$ or $\beta \neq 0$. If $\beta = 0$, $\mathit{\Delta} V_{\text{T0}}$ is defined to be zero. By contrast, if $\beta \neq 0$, V_{T0} shall be used in order to fulfill the claim.

Formulated in terms of an equation, the claim reads as:

$$I_{\mathrm{ds,off}}\Big|_{\beta=0,\varDelta V_{\mathrm{T0}}=0} = I_{\mathrm{ds,off}}\Big|_{\beta\neq 0,\varDelta V_{\mathrm{T0}}\neq 0} . \tag{2.44}$$

First, the new expression for the charge densities (Eq. (2.43)) needs to be inserted into the off-state power-law mobility (Eq. (2.24)) which leads to:

$$\mu_{\mathrm{off}} = \kappa \cdot \left(\frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)}\right)^{\beta} \cdot \exp\left(\beta \cdot \frac{V_{\mathrm{gs}} - V_{\mathrm{T0}} - \varDelta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right). \tag{2.45}$$

Next, Eqs. (2.43) and (2.45) can be inserted into the claim in Eq. (2.44). In order to increase the readability of the next steps, the left-hand side and right-hand side of this equation will be regarded separately. For the current, Eq. (2.31) is used. After the insertion of the off-state mobility and the modified off-state charge densities, the right-hand side of Eq. (2.44) reads as follows:

$$\begin{aligned} I_{\mathrm{ds,off}}\Big|_{\beta\neq 0,\varDelta V_{\mathrm{T0}}\neq 0} &= \kappa \cdot \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \cdot \frac{k_{\mathrm{B}}T}{q} \cdot \left(\frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)}\right)^{\beta} \cdot \exp\left(\beta \cdot \frac{V_{\mathrm{gs}} - V_{\mathrm{T0}} - \varDelta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right) \\ &\times \left(\frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)} \cdot C'_{\mathrm{diel}} \cdot \exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}} - \varDelta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right. \\ &\quad \left. - \frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)} \cdot C'_{\mathrm{diel}} \cdot \exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{ds}} - V_{\mathrm{T0}} - \varDelta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right) \end{aligned} \tag{2.46}$$

which can be rearranged by factoring out some terms and making use of the exponential laws:

$$\begin{aligned} I_{\mathrm{ds,off}}\Big|_{\beta\neq 0,\varDelta V_{\mathrm{T0}}\neq 0} &= \kappa \cdot \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \cdot \frac{k_{\mathrm{B}}T}{q} \cdot \left(\frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)}\right)^{\beta+1} \cdot C'_{\mathrm{diel}} \\ &\times \left(\exp\left((\beta+1)\,\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}} - \varDelta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right. \\ &\quad \left. - \exp\left((\beta+1)\,\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}} - \varDelta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)} - \frac{V_{\mathrm{ds}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right) \end{aligned} \tag{2.47}$$

which can be further simplified to

$$\begin{aligned} I_{\mathrm{ds,off}}\Big|_{\beta\neq 0,\varDelta V_{\mathrm{T0}}\neq 0} &= \kappa \cdot \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \cdot \frac{k_{\mathrm{B}}T}{q} \cdot \left(\frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)}\right)^{\beta+1} \cdot C'_{\mathrm{diel}} \\ &\times \exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}} - \varDelta V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right) \cdot \left(1 - \exp\left(\frac{-V_{\mathrm{ds}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right). \end{aligned} \tag{2.48}$$

This is the final version of the right-hand side of Eq. (2.44). Before continuing with the left-hand side of the claim, one interesting fact about this equation will be discussed. It can be seen that, similar to Eq. (2.33), this equation contains a term depending on V_{ds}. Please recall that Eq. (2.48) is in principle the off-state current of a transistor where the correction function for the sub-threshold swing has already been performed. What is striking is that now, in the denominator of the term containing V_{ds}, the pre-factor $(\beta+1)$ appears before S_{obs} whereas this pre-factor does not appear in Eq. (2.33). As was already discussed in the context of Eq. (2.33), the V_{ds} term causes the model to exhibit a shift of the sub-threshold current that resembles the DIBL effect. As in the V_{ds} term, the new pre-factor before S_{obs} is contained, the consequence is that the transistor incorporating the compensation function exhibits a different quasi-DIBL behavior than a transistor without the compensation function. In principle, this change is undesired but it is inevitable.

Next, the left-hand side where $\beta = 0$ and $\Delta V_{\mathrm{T0}} = 0$ will be dealt with. This case is much easier to treat since the power-law mobility reduces simply to the constant κ and since no shift of the threshold voltage needs to be looked at. The left-hand side reads as follows:

$$\begin{aligned} I_{\mathrm{ds,off}}\Big|_{\beta=0,\Delta V_{\mathrm{T0}}=0} =& \kappa\cdot\frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}}\cdot\frac{k_{\mathrm{B}}T}{q}\cdot\frac{S_{\mathrm{obs}}}{\ln(10)}\cdot C'_{\mathrm{diel}} \\ &\times\left(\exp\left(\frac{V_{\mathrm{gs}}-V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right)-\exp\left(\frac{V_{\mathrm{gs}}-V_{\mathrm{ds}}-V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right)\right), \end{aligned} \tag{2.49}$$

which is simplified by factoring out the exponential function:

$$\begin{aligned} I_{\mathrm{ds,off}}\Big|_{\beta=0,\Delta V_{\mathrm{T0}}=0} =& \kappa\cdot\frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}}\cdot\frac{k_{\mathrm{B}}T}{q}\cdot\frac{S_{\mathrm{obs}}}{\ln(10)}\cdot C'_{\mathrm{diel}}\cdot\exp\left(\frac{V_{\mathrm{gs}}-V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right) \\ &\times\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{S_{\mathrm{obs}}/\ln(10)}\right)\right). \end{aligned} \tag{2.50}$$

After these preparations, Eq. (2.48) and Eq. (2.50) can be equated leading to the following rather unhandy expression:

$$\begin{aligned} &\kappa\cdot\frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}}\cdot\frac{k_{\mathrm{B}}T}{q}\cdot\left(\frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)}\right)^{\beta+1}\cdot C'_{\mathrm{diel}} \\ &\times\exp\left(\frac{V_{\mathrm{gs}}-V_{\mathrm{T0}}-\Delta V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right)\cdot\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right) \\ &=\kappa\cdot\frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}}\cdot\frac{k_{\mathrm{B}}T}{q}\cdot\frac{S_{\mathrm{obs}}}{\ln(10)}\cdot C'_{\mathrm{diel}}\cdot\exp\left(\frac{V_{\mathrm{gs}}-V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right)\cdot\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{S_{\mathrm{obs}}/\ln(10)}\right)\right). \end{aligned} \tag{2.51}$$

This expression can be drastically simplified by dividing both sides by

$$\kappa\cdot\frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}}\cdot\frac{k_{\mathrm{B}}T}{q}\cdot C'_{\mathrm{diel}}\cdot\exp\left(\frac{V_{\mathrm{gs}}-V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right)$$

which is allowed from the mathematical perspective since none of the factors of this equation can become zero. This division leads to:

$$\begin{aligned}&\left(\frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)}\right)^{\beta+1}\cdot\exp\left(\frac{-\mathit{\Delta} V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right)\cdot\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right)\\&=\frac{S_{\mathrm{obs}}}{\ln(10)}\cdot\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{S_{\mathrm{obs}}/\ln(10)}\right)\right).\end{aligned}\tag{2.52}$$

This equation will be rearranged for $\mathit{\Delta} V_{\mathrm{T0}}$ in the next steps:

$$\exp\left(\frac{-\mathit{\Delta} V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right)=\frac{\frac{S_{\mathrm{obs}}}{\ln(10)}\cdot\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{S_{\mathrm{obs}}/\ln(10)}\right)\right)}{\left(\frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)}\right)^{\beta+1}\cdot\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right)}.\tag{2.53}$$

Making use of the exponential laws, this can be further rearranged to

$$\exp\left(\frac{-\mathit{\Delta} V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right)=\frac{\frac{S_{\mathrm{obs}}}{\ln(10)}\cdot\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{S_{\mathrm{obs}}/\ln(10)}\right)\right)}{(\beta+1)^{(\beta+1)}\cdot\left(\frac{S_{\mathrm{obs}}}{\ln(10)}\right)^{\beta+1}\cdot\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right)}\tag{2.54}$$

where one term cancels out leading to

$$\exp\left(\frac{-\mathit{\Delta} V_{\mathrm{T0}}}{S_{\mathrm{obs}}/\ln(10)}\right)=\frac{\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{S_{\mathrm{obs}}/\ln(10)}\right)\right)}{(\beta+1)^{(\beta+1)}\cdot\left(\frac{S_{\mathrm{obs}}}{\ln(10)}\right)^{\beta}\cdot\left(1-\exp\left(\frac{-V_{\mathrm{ds}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right)}.\tag{2.55}$$

Observing this equation, there can be deduced some interesting consequences for the compact model. On the one hand, it can be seen that the necessary shift $\mathit{\Delta} V_{\mathrm{T0}}$ is dependent on the the power-law exponent β. On the other hand, $\mathit{\Delta} V_{\mathrm{T0}}$ is also dependent on the drain-source voltage V_{ds}. As can be seen, in the numerator and the denominator of the fraction almost the same expression containing V_{ds} is present but the denominator contains $(\beta+1)$ as a pre-factor before S_{obs} whereas the term in the numerator does not contain a pre-factor before S_{obs}. So, unfortunately, the two terms do not cancel out. As discussed in the context of Eq. (2.48), the consequence of this is that a transistor incorporating the compensation method for the sub-threshold swing reacts differently to a change in V_{ds} than a transistor without the compensation would do. Theoretically, the influences of β and V_{ds} in Eq. (2.55) could be separated from each other by defining separate compensations. However, as already explained before, the quasi-DIBL effect is only important for transistors with very bad sub-threshold swings. Furthermore, it is desired that the model only contains bias-independent model parameters. If the shift V_{T0} was defined to be dependent on V_{ds}, this would, for example, result in changes in the output curves of the transistor. In order to come to a solution, it is mandatory to define a simplification. It is assumed that the drain-source voltage is sufficiently high so that the exponential functions tend to zero. It is not intended to compensate for the different influences of V_{ds} on the curves.

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CHARGE-BASED COMPACT MODELING OF CAPACITANCES AND LOW-FREQUENCY NOISE IN ORGANIC THIN-FILM TRANSISTORS
Jakob Simon Leise

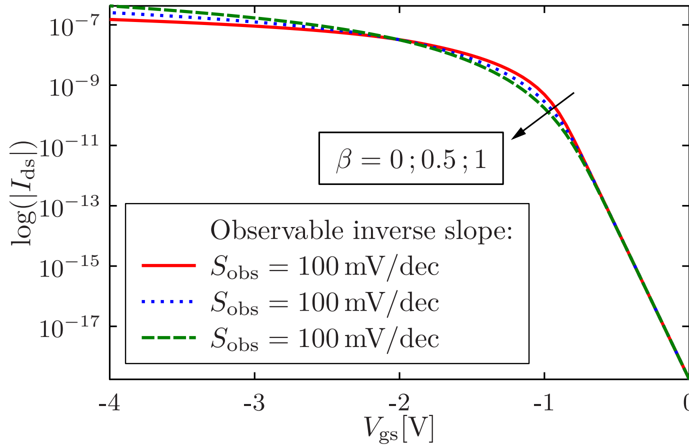

Figure 2.9.: Transfer curves of a staggered OTFT as calculated by the compact model for three different values of the power-law exponent β at $V_{ds} = -1\,\mathrm{V}$. The sub-threshold swing is set to $S_{obs} = 100\,\mathrm{mV/dec}$ and the complete de-coupling equation is used in order to eliminate the influence of the power-law exponent on the sub-threshold swing and the threshold voltage. The three curves are equal in the sub-threshold regime now. This figure was published in ref. [55] and slightly modified.

This leads to the following simplified form of the equation:

$$\exp\left(\frac{-\Delta V_{T0}}{S_{obs}/\ln(10)}\right) = \frac{1}{(\beta+1)^{(\beta+1)}\cdot\left(\frac{S_{obs}}{\ln(10)}\right)^{\beta}} \tag{2.56}$$

which can be rearranged for ΔV_{T0}:

$$\Delta V_{T0} = \frac{S_{obs}}{\ln(10)}\cdot\ln\left((\beta+1)^{(\beta+1)}\cdot\left(\frac{S_{obs}}{\ln(10)}\right)^{\beta}\right). \tag{2.57}$$

This is the final equation. Now, there is a comprehensive model for the correction of the sub-threshold swing and the threshold voltage which in the earlier version of the model were subject to a change due to the power-law exponent β. The final equation for the charge density at the source end of the channel reads as follows:

$$Q'_{ms} = \frac{(\beta+1)\cdot S_{obs}}{\ln(10)}\cdot C'_{diel}\cdot\mathcal{L}\left\{\exp\left(\frac{V_{gs}-V_{T0}-\Delta V_{T0}}{(\beta+1)\cdot S_{obs}/\ln(10)}\right)\right\}. \tag{2.58}$$

The final equation for the charge density at the drain end of the channel reads as follows:

$$Q'_{md,barr} = \frac{(\beta+1)\cdot S_{obs}}{\ln(10)}\cdot C'_{diel}\cdot\mathcal{L}\left\{\exp\left(\frac{V_{gs}-V_{T0}-V_{ds}+V_{sb,d}-\Delta V_{T0}}{(\beta+1)\cdot S_{obs}/\ln(10)}\right)\right\}. \tag{2.59}$$

Figure 2.9 proves that the de-coupling works well when implemented into the model.

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CHAPTER 3

Charges and Capacitances

In this chapter, an overview over the topic of charges in transistors will be given. As explained in the former sections, every transistor contains intrinsic and extrinsic charges. Depending on the applied terminal voltages the amount of charges in the transistor varies. However, charges cannot be created or disappear, they have to leave or enter the device through the source, drain or gate terminals [38].

3.1 Comparison to a Water System

In order to give a more figurative explanation of the importance of charges in transistors, the transistor is compared to a controllable valve in a water circuit. As can be seen in Fig. 3.1, the

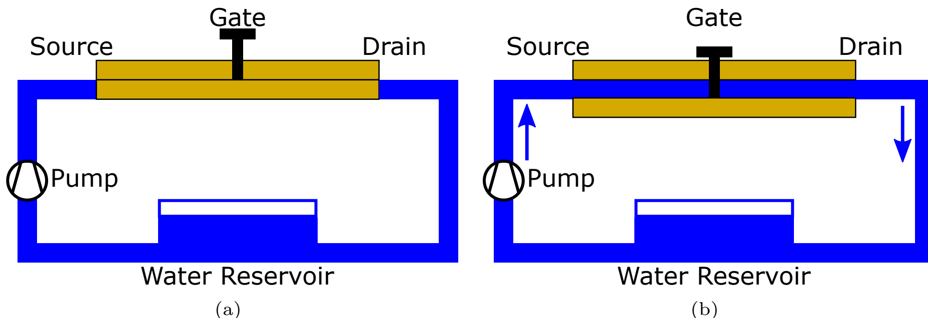

Figure 3.1.: (a) Model of a transistor as a controllable valve in a water circuit. Here the valve is closed and hence no water is contained in the valve. (b) Here the valve is opened allowing for a flow of water. In addition to the flow, there is an amount of water within the valve that had to enter the valve during the opening process.

transistor could be imagined as two plates that can be moved by a button. In Fig. 3.1(a), the valve is closed. Consequently, no water can flow even if the pump creates pressure. When the plates are moved away from each other they provide a conductive path for the water which can be seen in Fig. 3.1(b). Furthermore, it can be seen that in the region between the plates there

is a certain amount of water. This water has to enter the construction through the connections which in analogy to a transistor are denoted as source and drain. After the opening of the valve it will obviously take some time until it is filled with water and a steady-state water flow is established. This imagination can be compared to a transistor where the water plays the role of charges. It has to be noted that the water model is just a very figurative way of describing something which in reality is more complicated. In Fig. 3.2, the opening process of the valve

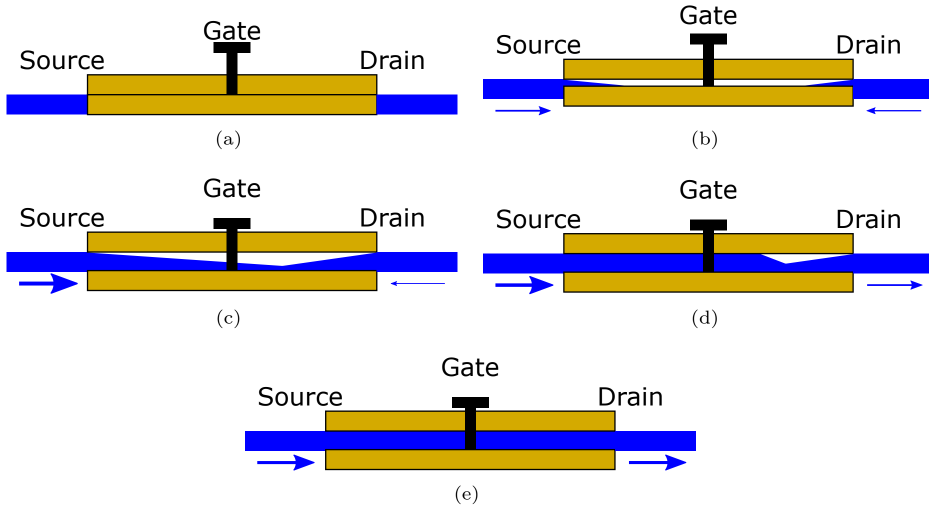

Figure 3.2.: Model of the transistor as a valve in a water circuit. An overview over the opening process of the valve is shown. The line thickness of the blue arrows indicates the amount of the water flow. Subfigures (a) to (e) show the system in subsequent time points.

is illustrated. The thickness of the blue arrows indicates the water flow in the corresponding terminal. As shown in Fig. 3.2(a), the valve is still closed and no water flow is visible. In (b), the valve has already been opened to a certain degree. It can be seen that a little vacuum is created and the water starts entering the device. Since the pressure at the source side is higher (due to the water pump) the water flow is a little bit higher here than at the drain. It can be observed at the drain terminal that there is also some water flowing in the direction of the device because there is water everywhere in the pipe system allowing the vacuum in the device to be filled to a certain degree by water molecules in the drain pipe. In (c), the valve is shown opened completely. However, still not the whole amount of water as under steady-state conditions is in the valve. Since the pressure at the source side is higher than at the drain the current will later flow from source to drain. It can be seen in (c) that already much more water is flowing in the source terminal than in the drain terminal. As can be seen in (d) the direction of the water flow at the drain terminal has reversed. There is only a little vacuum left in the valve that needs to be charged and there is already some of the water coming from the source that leaves the drain terminal. More physically speaking: The capacitive water charging current of the drain terminal is lower than the steady-state DC current at this time. Subfigure

(e) finally shows the steady-state operation. Since no vacuum is left in the valve the same water flow that enters the device through the source terminal leaves it through the drain. It shall be emphasized again that the water system described above is just a very simplified picture which can, however, be useful to understand the transient behavior of the transistor which will be elaborated on in Chap. 7.

3.2 Intrinsic Charges in Transistors

3.2.1 Introductory Information

Similarly as in the water system, a transistor contains varying amounts of charges depending on the terminal voltages. In Fig. 3.3, the sketch of a coplanar transistor which contains accumulation charges in the channel is shown. The transistor shown here is operated in a linear operation point since the charges are equally distributed along the channel. In this section, a

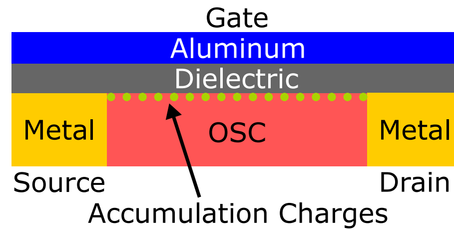

Figure 3.3.: Sketch of a coplanar transistor containing accumulation charges in the channel.

more theoretical background on the charges in transistors is given. The principles which will be described in the following are a review of ref. [38]. First, the intrinsic charges are dealt with and subsequently, a more complete picture will be drawn including different extrinsic contributions to the capacitive behavior.

The current flowing through a transistor is a composition of the steady-state current and the charging currents flowing in order to charge or discharge the intrinsic and extrinsic capacitances of the transistor. The charges in the transistor are distributed along the channel and they are attributed to be under control of the source and drain terminals to a certain degree. The total amount of charges in the channel is denoted as Q_c whereas the total amount of charges belonging to the drain and the source side of the channel are defined as Q_s and Q_d, respectively. In a four-terminal transistor, there also exists a bulk charge Q_b but in this work, only thin-film transistors comprising three terminals (gate, source and drain) are dealt with. The amount of total charges at every terminal is dependent on all of the terminal voltages V_g, V_s and V_d. The steady-state currents flowing through the transistor terminals are described in capital letters: I_g, I_s, I_d where the subscript corresponds to the gate, source and drain terminals. In addition, the time-dependent transient currents flowing through these terminals are written in small letters: i_g, i_s, i_d. In the following, a quasistatic operation is assumed which means that the

intrinsic capacitances of the transistor can be charged arbitrarily fast so that the amount of total charge in every alternating current (AC) operation point is the same as it would be under DC conditions. With this assumption the transient currents at the three transistor terminals can be defined as follows [38]:

$$i_{\mathrm{s}}(t) = -I_{\mathrm{s}}(V_{\mathrm{g}}(t), V_{\mathrm{d}}(t), V_{\mathrm{s}}(t)) + \frac{dQ_{\mathrm{s}}}{dt} \tag{3.1}$$

$$i_{\mathrm{d}}(t) = I_{\mathrm{d}}(V_{\mathrm{g}}(t), V_{\mathrm{d}}(t), V_{\mathrm{s}}(t)) + \frac{dQ_{\mathrm{d}}}{dt} \tag{3.2}$$

$$i_{\mathrm{g}}(t) = \frac{dQ_{\mathrm{g}}}{dt} = -\frac{dQ_{\mathrm{c}}}{dt}. \tag{3.3}$$

The minus sign before the DC current in Eq. (3.1) originates from the fact that the capitalized currents are defined as the currents entering the transistor terminals. However, the DC currents at the source and the drain are flowing in opposite directions. Thus, by defining the drain current to be positive, the source current needs to be negative. Due to the charge conservation principle, in transistors, equal amounts of charges are opposing in the gate electrode and the channel. Consequently, it can be concluded that the total gate charge Q_{g} is the same as the total channel charge Q_{c} but with an opposite sign. Furthermore, the sum of the charges associated with the source and the drain terminal is equal to the total channel charge. This leads to the expression for the charge conservation:

$$Q_{\mathrm{g}} + Q_{\mathrm{s}} + Q_{\mathrm{d}} = 0. \tag{3.4}$$

In order to solve the time-dependent current equations presented here, the total charges associated with drain and source would be required. However, they are not known explicitly. By contrast, it is possible to calculate the total amount of charges in the channel (and accordingly in the gate). Therefore, it is at least possible to define the sum of the source and drain transient currents:

$$i_{\mathrm{s}} + i_{\mathrm{d}} = I_{\mathrm{ds}}(V_{\mathrm{g}}(t), V_{\mathrm{d}}(t), V_{\mathrm{s}}(t)) + \frac{dQ_{\mathrm{c}}}{dt} \tag{3.5}$$

where I_{ds} is the steady-state drain-source current. Generally speaking, the total amount of charges in the channel (Q_{c}) can be obtained by an integration over the charge density per gate area along the channel:

$$Q_{\mathrm{c}} = W_{\mathrm{ch}} \int_0^{L_{\mathrm{ch}}} Q'_{\mathrm{c}}(x)\, dx \tag{3.6}$$

where x points in the direction of the channel length, W_{ch} is the channel width, and L_{ch} is the channel length. For standard MOSFETs, the total charge Q_{c} can be calculated based on the transistor and material parameters and the applied voltages. In the next section, a short overview over the well-known Meyer model is presented which is an easy but imprecise way of calculating the transistor capacitances.

3.2.2 The Meyer Model

As can be seen in Fig. 3.3, the charges in the transistor are distributed along the channel. However, such a distributed capacitance is hard to treat and to calculate since for that, the channel would have to be treated as a distributed transmission line consisting of small portions of the intrinsic channel resistance and the intrinsic channel capacitance [64]. In order to come to an easy solution that is sufficient for circuit simulation, the simplified approach according to the Meyer model can be used as presented in ref. [38].

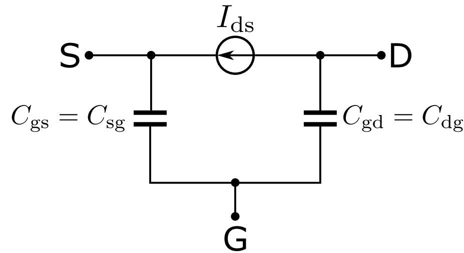

Figure 3.4.: Equivalent circuit of a MOSFET showing the capacitances as lumped elements.

In the Meyer model, the transistor capacitances are assumed to be lumped elements that can be found between the gate and the other terminals. The transistor is imagined as an equivalent circuit as shown in Fig. 3.4. The Meyer model defines the capacitances as the change of the total gate charges with respect to a change in the voltages:

$$C_{gs} = \frac{\partial Q_g}{\partial V_{gs}} \tag{3.7}$$

$$C_{gd} = \frac{\partial Q_g}{\partial V_{gd}}. \tag{3.8}$$

This definition of the capacitances circumvents the necessity of calculating the charges Q_s and Q_d separately. Furthermore, the capacitances are assumed to be reciprocal, i.e. a change in the charge stored in C_{gs} can be induced either by a change in the gate potential or by the same change in the source potential. Although it is simple, the Meyer model has drawbacks that diminish its usefulness. On the one hand, the Meyer model often leads to charge-non-conversation. This is because during the integration in two subsequent time steps t_1 and t_2 in a SPICE simulator the capacitances C_{gs} and C_{gd} are only known at the discrete time points t_1 and t_2. In the time between t_1 and t_2, the capacitances can, for example, be averaged between those two values. However, this implementation may lead to a non-conversation of the charges, i.e. that after some time in a transient simulation, the sum of the charges that entered and left the transistor can be imbalanced. If the time step in a SPICE simulator is chosen very small, then the charge-non-conversation will not be noticeable [38].

A further and quite critical aspect is that the Meyer model assumes the transistor capacitances to be reciprocal. However, in a real transistor the capacitances are non-reciprocal. One might ask the question why this is the case. In a normal plate capacitor, it is not of importance at which plate the potential is changed. The capacitor will respond equally to a potential change on each of the two plates. A figurative way of understanding the non-reciprocity of the

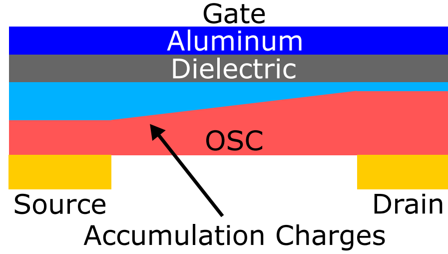

Figure 3.5.: Sketch of a staggered transistor containing accumulation charges in the channel. The charge density varies along the channel.

capacitances can be done by again having a look at a sketch of the transistor. In Fig. 3.5, a staggered transistor is depicted. This transistor structure is essentially the same as the coplanar structure shown in Fig. 3.3 but here the OSC separates the electrodes and the gate insulator from each other. It is now assumed that the transistor in Fig. 3.5 is operated in a certain DC operation point which leads to a charge density varying along the channel as depicted by the blue wedge-shaped area. From this DC operation point the potential of the gate electrode is slightly changed and the resulting changes of the charges are observed. The result is that both the gate-source voltage V_{gs} and the gate-drain voltage V_{gd} are altered a little bit whereas V_{ds} is kept constant. By contrast, if the gate and drain potentials remain constant and a little change on the source potential is imposed it effectively means that V_{gs} and V_{ds} are altered whereas V_{gd} is kept constant. It is obvious that the change in the total charge in the transistor is different in both cases. It will now be expressed in a more mathematics-based way that the reciprocity of the capacitances is actually not true. For this purpose, Eq. (3.4) is derived once with respect to V_{gs} and once with respect to V_{gd}:

$$\frac{\partial Q_{\mathrm{g}}}{\partial V_{\mathrm{gs}}} + \frac{\partial Q_{\mathrm{s}}}{\partial V_{\mathrm{gs}}} + \frac{\partial Q_{\mathrm{d}}}{\partial V_{\mathrm{gs}}} = 0 \tag{3.9}$$

$$\frac{\partial Q_{\mathrm{g}}}{\partial V_{\mathrm{gd}}} + \frac{\partial Q_{\mathrm{s}}}{\partial V_{\mathrm{gd}}} + \frac{\partial Q_{\mathrm{d}}}{\partial V_{\mathrm{gd}}} = 0. \tag{3.10}$$

Assuming reciprocity of the capacitances ($C_{\mathrm{ij}} = C_{\mathrm{ji}}$, where i, j represent the terminals g, s, or d) it can be said that

$$C_{\mathrm{gs}} = \frac{\partial Q_{\mathrm{g}}}{\partial V_{\mathrm{gs}}} \equiv C_{\mathrm{sg}} = \frac{\partial Q_{\mathrm{s}}}{\partial V_{\mathrm{sg}}} = -\frac{\partial Q_{\mathrm{s}}}{\partial V_{\mathrm{gs}}} \tag{3.11}$$

$$C_{\mathrm{gd}} = \frac{\partial Q_{\mathrm{g}}}{\partial V_{\mathrm{gd}}} \equiv C_{\mathrm{dg}} = \frac{\partial Q_{\mathrm{d}}}{\partial V_{\mathrm{dg}}} = -\frac{\partial Q_{\mathrm{d}}}{\partial V_{\mathrm{gd}}}. \tag{3.12}$$

Now, Eq. (3.11) is inserted into Eq. (3.9) and Eq. (3.12) into Eq. (3.10) which results in:

$$\frac{\partial Q_{\mathrm{d}}}{\partial V_{\mathrm{gs}}} = 0 \tag{3.13}$$

$$\frac{\partial Q_{\mathrm{s}}}{\partial V_{\mathrm{gd}}} = 0. \tag{3.14}$$

The consequence from this is that the drain charge would not change if the gate-source voltage was altered. Furthermore, the source charge would not change if the gate-drain voltage was altered. However, this is not true. Observing Fig. 3.5, it can be see that the charge is distributed along the channel and does not consist of two distinct portions that can be attributed ultimately to each of the terminals. Assuming, for example, that the gate-source voltage is increased by a certain amount, the charge density per gate area at the source end of the channel would increase. The charge density per gate area at the drain end of the channel would stay the same. The thickness of the blue wedge-shaped area in Fig. 3.5 represents the charge density. It is obvious that with the charge density at the source end being increased the whole blue area would be changed. Also in direct proximity to the drain terminal, an increase in V_{gs} would lead to a small increase in the charge density. As will be discussed in the next section, charges in the channel are under control of both the source and the drain terminals to a certain degree. Even those charge carriers that are closer to the drain terminal are influenced by the source terminal to a small extent. Thus, an increase in V_{gs} alters the amount of charges that is attributed to the drain terminal. The same consideration holds true for the charges associated with the source which is also under control of the drain terminal to a small extent. Thus, the reciprocity of the capacitances is a wrong assumption. Due to these drawbacks of the Meyer model new kinds of models were developed: the so-called charge-based models. The final equations of the Meyer model will not be presented here.

3.2.3 Charge-Based Capacitance Models

As explained in the previous section, the small-signal current at each terminal of the transistor is a function of the terminal voltages and of the capacitances of the transistor. In general, each terminal has a capacitive coupling to the remaining terminals. Hence, the small-signal part of the current at an arbitrary terminal with index j reads as [38]:

$$i_{\mathrm{j}} = \frac{dQ_{\mathrm{j}}}{dt} = \frac{\partial Q_{\mathrm{j}}}{\partial V_{\mathrm{g}}}\frac{\partial V_{\mathrm{g}}}{\partial t} + \frac{\partial Q_{\mathrm{j}}}{\partial V_{\mathrm{s}}}\frac{\partial V_{\mathrm{s}}}{\partial t} + \frac{\partial Q_{\mathrm{j}}}{\partial V_{\mathrm{d}}}\frac{\partial V_{\mathrm{d}}}{\partial t}. \tag{3.15}$$

In this equation, it becomes evident that the charges at each terminal j are derived with respect to the voltages at all three terminals. These derivatives are now defined as the capacitances of the transistor. A capacitance C_{ij} is generally defined as:

$$C_{\mathrm{ij}} = \begin{cases} -\frac{\partial Q_{\mathrm{i}}}{\partial V_{\mathrm{j}}} & i \neq j \quad i,j = g,s,d \\ \frac{\partial Q_{\mathrm{i}}}{\partial V_{\mathrm{j}}}, & i = j \end{cases} . \tag{3.16}$$

The capacitances where the two indices are different from each other are called the internodal capacitances or trans-capacitances or intrinsic capacitances. By contrast, the capacitances with equal indices are denoted as self capacitances. As shown in the equation the internodal capacitances have a minus sign. This minus sign is a convention and its purpose is that the capacitances behave "normal" which means that the amount of charge increases if the voltage at that terminal is increased and that it decreases if any of the voltages at any other terminal is increased. As an example, the capacitance

$$C_{\mathrm{gs}} = -\frac{\partial Q_{\mathrm{g}}}{\partial V_{\mathrm{s}}} \tag{3.17}$$

will be observed. This equation is rewritten as

$$\partial Q_{\mathrm{g}} = -C_{\mathrm{gs}} \cdot \partial V_{\mathrm{s}}. \tag{3.18}$$

It can now be imagined that the potential V_{s} at the source terminal is slightly increased. Consequently, the potential difference V_{gs} between gate and source becomes smaller. A "well-behaved" device now shows the behavior that the total amount of gate charge will decrease marginally. Without the minus sign the gate charge would, however, increase.

A transistor with three terminals will have nine capacitances which can be compiled in a capacitance matrix [38]:

$$C_{\mathrm{ij}} = \begin{bmatrix} C_{\mathrm{gg}} & -C_{\mathrm{gd}} & -C_{\mathrm{gs}} \\ -C_{\mathrm{dg}} & C_{\mathrm{dd}} & -C_{\mathrm{ds}} \\ -C_{\mathrm{sg}} & -C_{\mathrm{sd}} & C_{\mathrm{ss}} \end{bmatrix}. \tag{3.19}$$

This very general view on the transistor's capacitances has the advantage that the capacitances are not treated as reciprocal. The capacitance matrix has some properties which make the use of the capacitances easier. Each row and each column of the matrix has to sum up to zero in order to ensure reference-independence and charge-conversation. This rather theoretical aspect gains more figurativeness if two examples are regarded. At first, the first row of the matrix is observed. The claim is that the row sums up to zero, i.e.

$$C_{\mathrm{gg}} = C_{\mathrm{gd}} + C_{\mathrm{gs}}. \tag{3.20}$$

This makes sense from the practical point of view: C_{gg} is the amount of charges that change at the gate electrode when the gate potential is slightly changed (and consequently V_{gs} and V_{gd} are changed by the same amount). Accordingly, C_{gd} is the amount of gate charges that change when only the drain terminal is modulated around its steady-sate value, and C_{gs} is the amount of gate charges that change when only the source terminal is modulated a little bit. Assuming that both the drain and the source terminal are modulated by the same amount, it obviously has the same effect as if the gate potential was altered by the same amount.

Secondly, the first column of the matrix is taken and the claim that it has to sum up to zero is formulated:

$$C_{\mathrm{gg}} = C_{\mathrm{dg}} + C_{\mathrm{sg}}. \tag{3.21}$$

The validity of this equation is even clearer than the validity of the first claim. The three capacitances in Eq. (3.21) all have in common that their second index is the gate potential, i.e. they all reflect changes of charges when the gate potential is altered. The principle of charge conversation says that the total gate charges Q_{g} consist of the sum of Q_{s} and Q_{d}:

$$Q_{\mathrm{g}} + Q_{\mathrm{s}} + Q_{\mathrm{d}} = 0. \tag{3.22}$$

Deriving the three summands in this equation with respect to V_{g} and making use of the fact that $Q_{\mathrm{g}} = -Q_{\mathrm{c}}$ directly leads to the condition that the first column of the matrix sums up to zero.

The advantage of such a charge-based approach is that a completely consistent and well-behaving model can be derived. The question which remains is how to attribute the charges in the channel either to the source side or the drain side. Ward and Dutton proposed a partitioning scheme for the charges [65] which has been widely accepted in the modeling community and has been used for different transistor technologies, and as well for OTFTs [30, 32, 38, 66]. The partitioning scheme according to Ward and Dutton [65] introduces simple weighting functions that attribute the charges to belong to a certain degree to both the drain and the source terminals depending on their position in the channel. In general, one can say that charges are more under control of the terminal to which they are closer to. This is visualized in Fig. 3.6

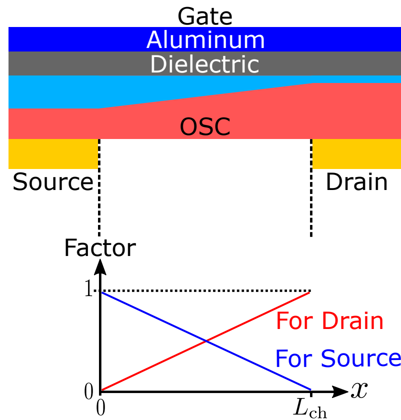

Figure 3.6.: Weighting functions of the partitioning scheme according to Ward and Dutton [65]. The total channel charges are multiplied by the functions that are plotted below the sketch of the transistor.

where the trends of the linear weighting functions are shown depending on the position in the channel. If, for example, the total charges associated with the source terminal are calculated the charge density in the channel is multiplied at every point by the blue function which gives

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a weight to it. The advantage of this partitioning scheme is that there is no sharp border at which the charges are attributed to either the source or the drain terminal. Rather, as it would happen in reality, the charges are always under control of both terminals.

3.3 Extrinsic Charges

The charges and capacitances that were described in the former subsections are all intrinsic charges. This means that they are located in the active region of the transistor, i.e. the channel region. However, a real transistor always has additional capacitances which are located in the peripheral regions. These capacitances are referred to as extrinsic capacitances. In Fig. 3.7,

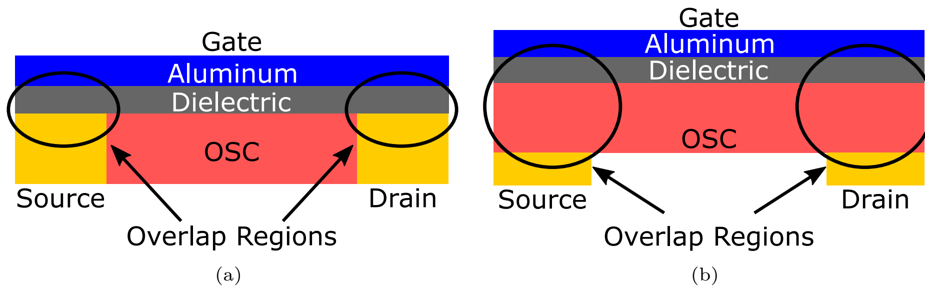


Figure 3.7.: Schematic sketches of OTFTs where the gate-to-contact overlap regions are highlighted. (a) A coplanar transistor is shown. (b) A staggered transistor is shown.

two transistors in the coplanar and staggered architecture are shown. Due to the fabrication process, it is inevitable that there is a certain overlap between the gate electrode and the source/drain electrodes. In case of coplanar transistors, the overlap capacitances show a very easily predictable behavior because they behave to a first approximation as parallel-plate capacitors. By contrast, a more sophisticated approach has to be used to characterize the overlap capacitances in staggered transistors. Here, in the overlap regions, a stack of the organic semiconductor and the gate dielectric is present. As long as the channel length of the transistor is much longer than the gate-to-contact overlap lengths the extrinsic capacitances only make a small contribution to the overall capacitances. However, if short-channel transistors are fabricated, the gate-to-contact overlap lengths may be even longer than the intrinsic channel lengths [55]. In this case, the extrinsic capacitances are even larger than the intrinsic capacitances. This emphasizes that the treatment of the extrinsic charges will be important for a well-working compact model.

CHAPTER 4

Modeling of the Total Charges

This chapter is dedicated to the compact modeling of total charges. A compact model for the description of the total charges that are stored in the OTFT is derived. Depending on the transistor architecture (staggered or coplanar), the compact model is extended to properly describe the charges in overlap regions. In addition, the charges in fringing regions will be treated in more detail.

4.1 Intrinsic Charges

In this section, equations for the intrinsic channel charges in OTFTs are derived. Based on the charge-based compact DC model [36], a comparatively simple model can be obtained. This model was published in refs. [54, 55, 67] and will be presented in detail here. The derivation is based on an n-type transistor and can easily be transferred to p-type transistors by exchanging the sign of the charges. In Fig. 4.1, schematic sketches of a coplanar and a

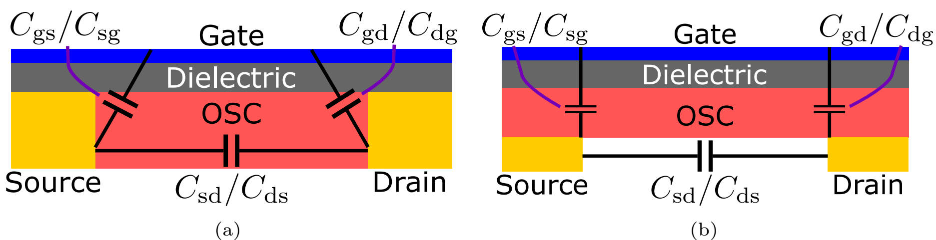
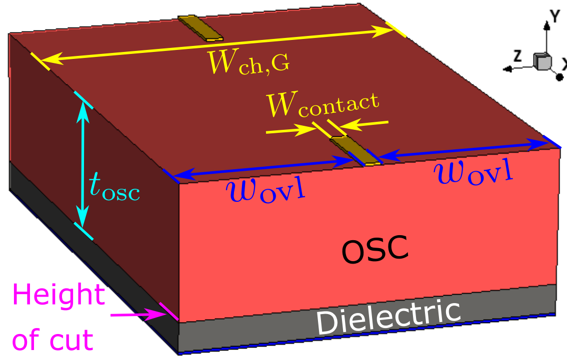


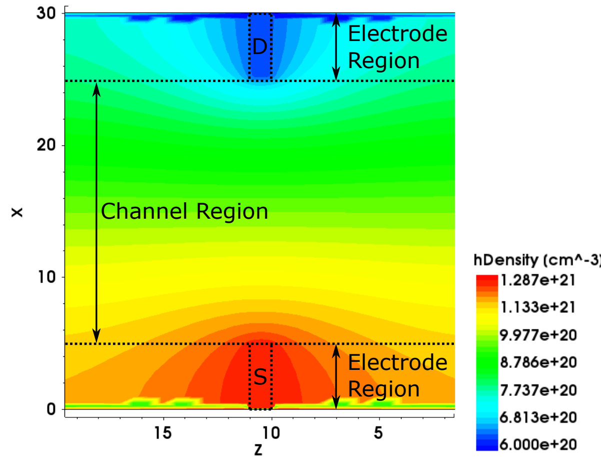
Figure 4.1.: (a) Sketch of a coplanar transistor where the intrinsic capacitances are shown as lumped elements. In reality, the capacitances are neither lumped elements nor reciprocal but this figure shall help to imagine the capacitances. (b) Sketch of a staggered transistor where the intrinsic capacitances are as well shown as lumped elements.

staggered OTFT are shown where the intrinsic capacitances are shown as lumped elements. It has to be emphasized that the capacitances in reality are distributed capacitances which are non-reciprocal as explained in Chap. 3. The intrinsic charges are derived following the well-

known principles which have been used for other transistor technologies or OTFTs [38, 68, 69] by combining the drift-diffusion model with charge-based expressions for the charge densities at the source and drain end of the channel. These principles will be used in the following sections in order to derive the model. Before presenting the derivation, special attention has to be paid to three-dimensional effects in the OTFTs. In ref. [54], charge equations including the charges in fringe regions were presented. Figure 4.2 shows the results of a 3D Sentaurus TCAD simulation where a staggered OTFT comprising fringe regions was simulated.



(a)



(b)

Figure 4.2.: Three-dimensional Sentaurus TCAD simulation of a staggered OTFT. The pictures were published in ref. [54] and were slightly modified. The voltages are $V_{gs} = -4\,\mathrm{V}$, $V_{ds} = -1\,\mathrm{V}$. (a) shows the structure of the transistor. The OSC layer has a thickness of $t_{osc} = 25\,\mathrm{nm}$. Please note that the y axis is scaled tremendously larger than the other axes. (b) shows the density of quasi-mobile accumulated holes in a cutplane in the organic semiconductor close to the gate dielectric at the height indicated in (a). As a guide for the eye, the projections of the source and drain electrodes onto the cutplane are shown.

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In Fig. 4.2(a), the simulated structure can be observed while in Fig. 4.2(b), the density of quasi-mobile accumulated holes in a cutplane close to the gate dielectric is shown. In the channel region, the charge density is nearly equal for every z position. Furthermore, in the electrode regions, the charge density varies only marginally with the z direction. From these observations, some important information can be deduced for the charge model:

- Charges are accumulated everywhere where the gate stack is in contact with the organic semiconductor.
- The density of quasi-mobile accumulation charges is nearly independent of the z position of the transistor. It is thus not of importance whether a point in the geometric channel center is observed or a point in the fringe regions.
- The density of accumulated charges is obviously independent of the current density. As previously shown in Fig. 2.5, the current density differs between points in the channel center and the fringe regions.

Very generally speaking, the total charges in the channel can be calculated by performing an integration over the charge density per gate area along the channel. The charges associated with the source and drain terminals are calculated by applying weighting functions according to Ward and Dutton [65]. As shown in Fig. 4.2(b), the density of quasi-mobile charges is

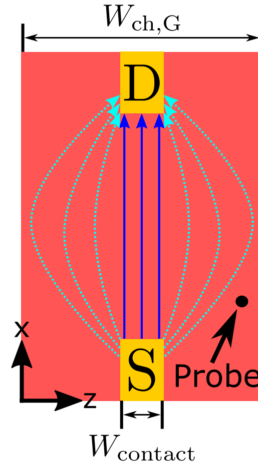

Figure 4.3.: Schematic of a cutplane in a coplanar transistor where the effect of current spreading is shown. The probe point is located far from the channel center. Therefore, the current density is low there. However, the density of accumulated quasi-mobile charges is nearly the same as in the channel center at the same x coordinate. This picture was published in ref. [54] and was slightly modified.

nearly the same for every position in the direction of the channel width even if points beyond the geometric channel center are regarded. This shall be emphasized by looking at Fig. 4.3 where again a cutplane in a coplanar transistor comprising fringe regions is shown. The probe

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point is located beyond the channel center. Therefore, the current density in this point will be low. However, as explained before, the density of accumulated quasi-mobile charges is the same as in the channel center for that x position. Therefore, the total gate width $W_{\mathrm{ch,G}}$ of the transistor has to be used for the total charge calculation. The following three integrals serve as the starting point for the derivation:

$$Q_{\mathrm{c}} = W_{\mathrm{ch,G}} \int_{0}^{L_{\mathrm{ch}}} Q'_{\mathrm{m}}(x)\, dx, \tag{4.1}$$

$$Q_{\mathrm{d}} = W_{\mathrm{ch,G}} \int_{0}^{L_{\mathrm{ch}}} \frac{x}{L_{\mathrm{ch}}} Q'_{\mathrm{m}}(x)\, dx, \tag{4.2}$$

$$Q_{\mathrm{s}} = W_{\mathrm{ch,G}} \int_{0}^{L_{\mathrm{ch}}} \left(1 - \frac{x}{L_{\mathrm{ch}}}\right) Q'_{\mathrm{m}}(x)\, dx \tag{4.3}$$

where $W_{\mathrm{ch,G}}$ is the geometric width of the transistor including all fringe regions, L_{ch} is the channel length, and $Q'_{\mathrm{m}}(x)$ is the charge density per gate area at position x in the channel. The difficulty about these equations is that the charge density Q'_{m} is not known for every arbitrary position in the channel. Only at the source end of the channel ($x = 0$) and at the drain end of the channel ($x = L_{\mathrm{ch}}$), the charge densities are known from the compact DC model. Therefore, in order to find a solution, some substitutions have to be performed. According to the drift diffusion model, the drain current can be calculated in every point of the channel by the charge density and the electric field at that position [39]:

$$I_{\mathrm{ds}} = \mu_{\mathrm{eff}} W_{\mathrm{ch,eff}} Q'_{\mathrm{m}}(x) \frac{dV}{dx} \tag{4.4}$$

where in comparison to ref. [39], the effective mobility and channel width are used. dx is a small segment of the channel in the direction of the channel length and dV is the voltage drop in the direction of the channel. It shall be emphasized here that dV is a change in the quasi-Fermi potential and not in the electrostatic potential [39]. Here, no minus sign is added, because the drain-source current is defined to be positive if a positive V_{ds} is applied. In the next step, Eq. (4.4) is rearranged for dx:

$$dx = \left(\frac{W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{I_{\mathrm{ds}}} \cdot Q'_{\mathrm{m}}(x)\right) dV. \tag{4.5}$$

The goal is to reformulate the charge integrals in such a way that the integration variable changes from x to Q'_{m}. Equation 4.5 already allows for a substitution of the integration variable x by V. The next step is to link the drift-diffusion differential to the differential according to Eq. (2.3). The latter links a change in the gate potential to a change in the density of accumulated quasi-mobile charges. Some additional thoughts are necessary in order to combine the two differentials. Figure 4.4 shows a sketch of a coplanar OTFT where two points A and B

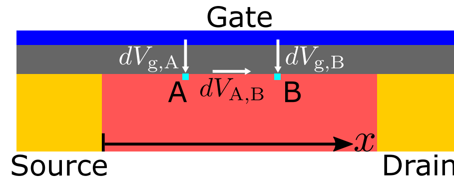

Figure 4.4.: Sketch of a coplanar OTFT. When moving from point A to point B the quasi-Fermi potential changes by an amount $dV_{\mathrm{A,B}}$. The voltage drops $dV_{\mathrm{g,A}}$ and $dV_{\mathrm{g,B}}$ are the potential differences between the gate electrode and points A and B, respectively.

in the intrinsic charge-carrier channel are shown. An application of a gate-source voltage and a gate-drain voltage leads to the propagation of a channel voltage varying monotonically along the channel so that the quasi-Fermi potentials at the source/drain ends of the channel are aligned with the Fermi-levels at the electrodes [39]. Assuming that when moving from point A to point B in Fig. 4.4, the channel voltage increases, the change of the voltage drops from the gate to the corresponding points change, as well. Since the gate potential is the same for every x-position in the channel, $dV_{\mathrm{g,B}}$ will be lower than $dV_{\mathrm{g,A}}$ by an amount of $dV_{\mathrm{A,B}}$. Switching to figurative speech: When walking up some stairs, the distance to the ceiling is decreasing by the same amount. Here, each stair step represents an increase in the channel voltage and the distance to the ceiling represents the voltage drop from the gate electrode to the channel. For the density of accumulated quasi-mobile charges, it is not of importance whether a change in the electrostatics is due to a change in the channel potential or due to a change in the gate potential. It has to be emphasized that the potential applied to the gate electrode is in fact constant but a change in the channel potential by an amount of dV has the same effect on the density of accumulated charges as an equivalent change $-dV_{\mathrm{g}}$ in the gate potential would have. These theoretical thoughts allow for a linking of the two voltage changes:

$$dV = -dV_{\mathrm{g}}. \tag{4.6}$$

Considering this, the two differentials in Eqs. (4.5) and (2.3) can be linked which leads to

$$dx = -\left(\frac{W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{I_{\mathrm{ds}}} \cdot Q'_{\mathrm{m}}(x)\right) \cdot \left(\frac{\tilde{\alpha} \cdot V_{\mathrm{th}}}{Q'_{\mathrm{m}}(x)} + \frac{1}{C'_{\mathrm{diel}}}\right) \cdot dQ'_{\mathrm{m}} \tag{4.7}$$

where $V_{\mathrm{th}} = k_{\mathrm{B}}T/q$ is the thermal voltage. Please note that originally the differential in Eq. (2.3) contains the slope degradation factor α whereas here $\tilde{\alpha}$ is used. The reason for this is that the model shows a slightly unstable behavior for transistors exhibiting a sub-threshold swing notably larger than $\approx 60\,\mathrm{mV/dec}$ at room temperature. It proved out that setting $\tilde{\alpha} = 1$ leads to good and stable results. The differential in Eq. (4.7) is now substituted in the three charge integrals in Eqs. (4.1), (4.2), and (4.3). Since the integration variable changes from x to Q'_{m}, the integration limits need to be exchanged. The former integration limit 0 representing the source end of the channel is replaced by the charge density at the source end which is Q'_{ms}.

Accordingly, the former integration limit L_{ch} is replaced by Q'_{md}. Hence, the charge integral for the total channel charge according to Eq. (4.1) can already be calculated analytically. However, for the total charges associated with the source and the drain (Q_{s} and Q_{d}), the variable x appears because of the Ward-Dutton partitioning scheme [65]. In order so solve Eqs. (4.2) and (4.3), the variable x needs to be expressed as a function of the new integration variable Q'_{m}. For this purpose, a simple integration is performed. In general, x can be expressed as

$$x = \int_{0}^{x} dx \tag{4.8}$$

where again the substitution according to Eq. (4.7) is performed which leads to

$$x = -\int_{Q'_{\mathrm{ms}}}^{Q'_{\mathrm{m}}(x)} \left(\frac{W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{I_{\mathrm{ds}}} \cdot Q'_{\mathrm{m}}(x)\right) \cdot \left(\frac{\tilde{\alpha} \cdot V_{\mathrm{th}}}{Q'_{\mathrm{m}}(x)} + \frac{1}{C'_{\mathrm{diel}}}\right) \cdot dQ'_{\mathrm{m}}. \tag{4.9}$$

Rearranging this equation yields

$$x = -\frac{W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{I_{\mathrm{ds}}} \int_{Q'_{\mathrm{ms}}}^{Q'_{\mathrm{m}}(x)} \left(\tilde{\alpha} \cdot V_{\mathrm{th}} + \frac{Q'_{\mathrm{m}}(x)}{C'_{\mathrm{diel}}}\right) \cdot dQ'_{\mathrm{m}}. \tag{4.10}$$

This simple integration can be carried out which results in

$$x = -\frac{W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{I_{\mathrm{ds}}} \left[\tilde{\alpha} \cdot V_{\mathrm{th}} \cdot Q'_{\mathrm{m}}(x) + \frac{Q'^{2}_{\mathrm{m}}(x)}{2C'_{\mathrm{diel}}}\right]_{Q'_{\mathrm{ms}}}^{Q'_{\mathrm{m}}(x)} \tag{4.11}$$

which can finally be written as

$$x = \frac{W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{I_{\mathrm{ds}}} \left(\tilde{\alpha} \cdot V_{\mathrm{th}} \cdot Q'_{\mathrm{ms}} + \frac{Q'^{2}_{\mathrm{ms}}}{2C'_{\mathrm{diel}}} - \tilde{\alpha} \cdot V_{\mathrm{th}} \cdot Q'_{\mathrm{m}}(x) - \frac{Q'^{2}_{\mathrm{m}}(x)}{2C'_{\mathrm{diel}}}\right). \tag{4.12}$$

Based on this, the charges associated with the channel, the source, and the drain can be calculated analytically. The solution of the three integrals in Eqs. (4.1), (4.2), and (4.3) is presented in Appendix A. Observing these final equations, an interesting fact becomes visible: The effective channel width $W_{\mathrm{ch,eff}}$ and the drain current I_{ds} both appear in the charge equations to the same power but on opposite sides of the fraction. Please recall that the current is linearly dependent on the effective channel width (see Eq. (2.21)) and has the following form:

$$I_{\mathrm{ds}} = W_{\mathrm{ch,eff}} \cdot f\left(Q'_{\mathrm{ms}}, ...\right). \tag{4.13}$$

Consequently, in the fraction $W_{\mathrm{ch,eff}}/I_{\mathrm{ds}}$, the effective channel width is canceled. Thus, the choice of δ_{fit} does not have any influence on the final charge equations, and a distinction between intrinsic channel currents and fringe currents is not necessary for a well-working model.

If the drain source voltage (V_{ds}) is close to zero, the drain current becomes zero and the charge densities at the source end and the drain end of the channel become equal. In this case, the charge equations are no longer valid since a division by the drain current is performed. If V_{ds} is exactly zero the total channel charge is perfectly evenly distributed so that $Q_{\mathrm{s}} = Q_{\mathrm{d}} = 0.5Q_{\mathrm{c}}$. The charge equations would result in expressions where zero is divided by zero. In order to circumvent this problem, the following thoughts lead to a much simpler solution: If the charges are totally evenly distributed, it means that $Q'_{\mathrm{ms}} = Q'_{\mathrm{md}}$. There is no gradient of the charges in the direction of the channel and hence, the charge density Q'_{ms} is present everywhere in the entire plane of the transistor. Thus, the charge integral for the total channel charge (Eq. (4.1)) greatly reduces to:

$$\begin{aligned} Q_{\mathrm{c,zero}} &= W_{\mathrm{ch,G}} \cdot Q'_{\mathrm{ms}} \int_0^{L_{\mathrm{ch}}} dx \\ &= W_{\mathrm{ch,G}} \cdot L_{\mathrm{ch}} \cdot Q'_{\mathrm{ms}}. \end{aligned} \tag{4.14}$$

The charges at the source and the drain are expressed as:

$$Q_{\mathrm{d,zero}} = \frac{1}{2} Q_{\mathrm{c}} = \frac{1}{2} \cdot W_{\mathrm{ch,G}} \cdot L_{\mathrm{ch}} \cdot Q'_{\mathrm{ms}}, \tag{4.15}$$

$$Q_{\mathrm{s,zero}} = \frac{1}{2} Q_{\mathrm{c}} = \frac{1}{2} \cdot W_{\mathrm{ch,G}} \cdot L_{\mathrm{ch}} \cdot Q'_{\mathrm{ms}}. \tag{4.16}$$

When implementing the model in a programming language, in principle, a simple case distinction could be performed. If V_{ds} equals zero, the asymptotic case according to Eqs. (4.14), (4.15) and (4.16) is used. Otherwise, the derived equations as presented in Appendix A are used. Even if the equations in Appendix A converge to the asymptotic case presented here, the procedure using a case distinction may produce numerical instabilities if the model is implemented in a hardware description language such as Verilog-A. A compact model should ideally not have any discontinuities in its functions or in the derivatives [49]. If the asymptotic switching is used, however, this results in a little discontinuity. In order to overcome this problem, a transition function $g_{\mathrm{decision}}(V_{\mathrm{ds}})$ is defined which smoothly switches between the zero-case and the non-zero-case:

$$Q_{\mathrm{c,final}} = Q_{\mathrm{c,nonzero}} \cdot g_{\mathrm{decision}}(V_{\mathrm{ds}}) + Q_{\mathrm{c,zero}} \cdot \left(1 - g_{\mathrm{decision}}(V_{\mathrm{ds}})\right), \tag{4.17}$$

$$Q_{\mathrm{d,final}} = Q_{\mathrm{d,nonzero}} \cdot g_{\mathrm{decision}}(V_{\mathrm{ds}}) + Q_{\mathrm{d,zero}} \cdot \left(1 - g_{\mathrm{decision}}(V_{\mathrm{ds}})\right), \tag{4.18}$$

$$Q_{\mathrm{s,final}} = Q_{\mathrm{s,nonzero}} \cdot g_{\mathrm{decision}}(V_{\mathrm{ds}}) + Q_{\mathrm{s,zero}} \cdot \left(1 - g_{\mathrm{decision}}(V_{\mathrm{ds}})\right). \tag{4.19}$$

It shall be emphasized that the $Q_{\mathrm{c,nonzero}}$, $Q_{\mathrm{d,nonzero}}$ and $Q_{\mathrm{s,nonzero}}$ are the equations for the total charges as defined in Eqs. (4.1), (4.2) and (4.3). However, in order to improve the reading flow, the charges are not denoted as non-zero-case charges before.

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Based on experiments with the simulator Spectre by Cadence Virtuoso [70], the following requirements are formulated for the switching process:

- In a region between $-1\,\mu\text{V} < V_\text{ds} < 1\,\mu\text{V}$, constantly the zero-case charges shall be used and the change of the charge distribution with respect to V_ds shall be ignored.
- In the ranges $-2\,\mu\text{V} < V_\text{ds} \leq -1\,\mu\text{V}$ and $1\,\mu\text{V} \leq V_\text{ds} < 2\,\mu\text{V}$, the total charges shall transit from the zero-case charges to the non-zero-case charges.
- If the absolute value of V_ds is greater than or equal to $2\,\mu\text{V}$, the non-zero-case charges shall be used.
- The transition function has to provide a smooth transition so that there are no discontinuities.

As implied above, in the decision function g_decision still a case distinction is used in order to determine whether V_ds is

(i) in the range of $\mp 1\,\mu\text{V}$ around zero or

(ii) in the range between absolute values of $1\,\mu\text{V}$ and $2\,\mu\text{V}$ or

(iii) in the range of absolute values greater than or equal to $2\,\mu\text{V}$.

The requirement is now that the transition function which is active during condition (ii) continuously connects the two regimes in points (i) and (iii) so that there are no discontinuities in the points where the case decision is performed. The following requirements need to be fulfilled by the function g_decision:

(a) The function value at $V_\text{ds} = 1\,\mu\text{V}$ is zero.

(b) The first and the second derivatives of the function at $V_\text{ds} = 1\,\mu\text{V}$ have to be zero.

(c) The function value at $V_\text{ds} = 2\,\mu\text{V}$ is equal to one.

(d) The first and the second derivatives of the function at $V_\text{ds} = 2\,\mu\text{V}$ have to be zero. In principle, it could also be required that more than just the first two derivatives are set to zero but experiments with Cadence Virtuoso have shown that it is sufficient to set the first two derivatives to zero.

As can be seen, there are six requirements which the function has to fulfill. It is decided to use a polynomial function f_poly and since six requirements need to be incorporated, a polynomial of degree five is used which has six constants to be determined:

$$f_\text{poly}(V_\text{ds}) = a_\text{f} \cdot \frac{|V_\text{ds}|^5}{1\,\text{V}^5} + b_\text{f} \cdot \frac{|V_\text{ds}|^4}{1\,\text{V}^4} + c_\text{f} \cdot \frac{|V_\text{ds}|^3}{1\,\text{V}^3} + d_\text{f} \cdot \frac{|V_\text{ds}|^2}{1\,\text{V}^2} + e_\text{f} \cdot \frac{|V_\text{ds}|}{1\,\text{V}} + f_\text{f} \tag{4.20}$$

where $|V_\text{ds}|$ is divided by a value of 1 with the unit of volt to the respective power in order to make the function unitless. Here, the absolute value of V_ds is used so that the function

is symmetric for negative and positive values of V_{ds}. The determination of the coefficients a_{f} to f_{f} is straightforward by formulating the six above-mentioned conditions in terms of equations which leads to a system of six linear equations which can be solved using the software Matlab [71]. The results for the coefficients are:

$$\begin{aligned} a_{\mathrm{f}} &= 6\cdot 10^{30} & b_{\mathrm{f}} &= -4.5\cdot 10^{25} & c_{\mathrm{f}} &= 1.3\cdot 10^{20} \\ d_{\mathrm{f}} &= -1.8\cdot 10^{14} & e_{\mathrm{f}} &= 1.2\cdot 10^{8} & f_{\mathrm{f}} &= -31. \end{aligned} \tag{4.21}$$

Since the function f_{poly} smoothly connects the two cases there is no discontinuity at the switching points up to the second derivative. The final decision function $g_{\mathrm{decision}}(V_{\mathrm{ds}})$ is defined as:

$$g_{\mathrm{decision}} = \begin{cases} 1 & \text{for} \quad V_{\mathrm{ds}} \leq -2\,\mu\mathrm{V} \\ f_{\mathrm{poly}}(V_{\mathrm{ds}}) & \text{for} \quad -2\,\mu\mathrm{V} < V_{\mathrm{ds}} \leq -1\,\mu\mathrm{V} \\ 0 & \text{for} \quad -1\,\mu\mathrm{V} < V_{\mathrm{ds}} < 1\,\mu\mathrm{V} \\ f_{\mathrm{poly}}(V_{\mathrm{ds}}) & \text{for} \quad 1\,\mu\mathrm{V} \leq V_{\mathrm{ds}} < 2\,\mu\mathrm{V} \\ 1 & \text{for} \quad V_{\mathrm{ds}} \geq 2\,\mu\mathrm{V}. \end{cases} \tag{4.22}$$

The function g_{decision} is plotted in Fig. 4.5 over a small range of V_{ds} values around zero.

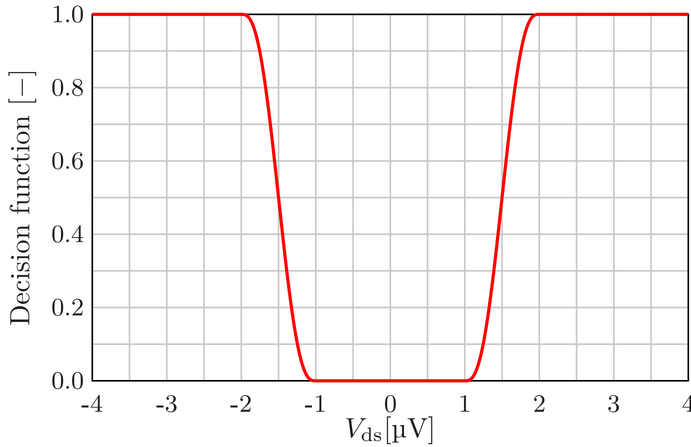

Figure 4.5.: Decision function $g_{\mathrm{decision}}(V_{\mathrm{ds}})$ shown over V_{ds} in a small range.

4.2 Extrinsic Charges

In addition to the intrinsic charges presented in the section before, a transistor will usually have additional charges that are stored in the periphery, for instance in the gate-to-contact overlap regions. These charges are referred to as extrinsic charges. In organic thin-film transistors, the overlap regions can be large in comparison to the intrinsic channel length [55]. Consequently, the charges in overlap regions will have a major influence on the overall capacitive behavior of the transistor. In this section, analytical equations for the charges in the gate-to-contact overlap regions will be derived for the two transistor architectures.

4.2.1 Coplanar Transistors

The gate-to-contact overlap capacitances are comparatively easy to treat. Figure 4.6 depicts a coplanar structure where special emphasis is put on the overlap regions. Since the gate electrode is separated from the source/drain electrodes by the gate dielectric, the overlap regions behave to a first approximation as simple parallel-plate capacitors. The lengths of the overlap regions ($L_{\mathrm{ov,GS}}$, $L_{\mathrm{ov,GD}}$) of fabricated OTFTs are usually some orders of magnitude larger than the thickness of the gate dielectric [40, 43, 59]. Therefore, the additional field lines beyond the parallel plates will not have a major influence on the capacitance.

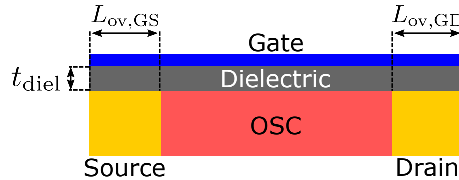

Figure 4.6.: Structure of a coplanar OTFT, similar as in ref. [55]. The gate-to-contact overlap regions behave to a first approximation like simple plate capacitors.

In addition to the overlap charges, attention has to be paid to the charges in fringe regions. In Fig. 4.7, a cutplane in an OTFT comprising two source/drain electrodes is shown where fringe regions are present. For simplicity, the compact model assumes that the charge density at the source end of the channel is present everywhere in the fringe regions next to the source electrode which is emphasized by the cyan/red-hashed area. Similar thoughts hold true for the drain side where the charge density Q'_{md} is assumed to be present in the entire yellow/red-hashed region. The extrinsic charges in coplanar transistors can be described by a sum of the following two components:

1. Charges stored in the parallel-plate capacitors originating from the gate-to-contact overlap lengths.

2. Charges that are accumulated in the fringe regions between the fingers and beyond the first and the last finger.

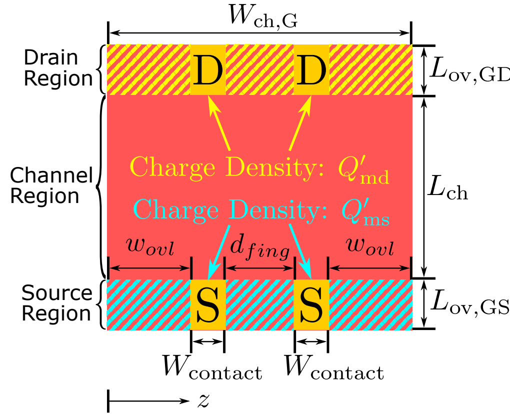

Figure 4.7.: Cutplane in a two-finger coplanar OTFT. In the electrode regions which are the fringe regions next to the source/drain electrodes charges are accumulated. It is assumed that the charge density at the source end of the channel is present everywhere in the electrode region at the source. Similar considerations hold true at the drain side. This picture was published in ref. [55].

The extrinsic charges in coplanar transistors can be calculated as follows:

$$Q_{\text{ex,S,copl}} = V_{\text{gs}} C'_{\text{diel}} L_{\text{ov,GS}} N_{\text{fing}} W_{\text{contact}} + \left(2w_{\text{ovl}} + \left(N_{\text{fing}} - 1\right) d_{\text{fing}}\right) L_{\text{ov,GS}} Q'_{\text{ms}} \tag{4.23}$$

$$Q_{\text{ex,D,copl}} = V_{\text{gd}} C'_{\text{diel}} L_{\text{ov,GD}} N_{\text{fing}} W_{\text{contact}} + \left(2w_{\text{ovl}} + \left(N_{\text{fing}} - 1\right) d_{\text{fing}}\right) L_{\text{ov,GD}} Q'_{\text{md}}. \tag{4.24}$$

4.2.2 Staggered Transistors

In staggered transistors, the gate electrode is separated from the source/drain electrodes by a stack consisting of the gate dielectric and the organic semiconductor as shown in Fig. 4.8. Depending on the applied voltages such a structure shows different behaviors. If the organic

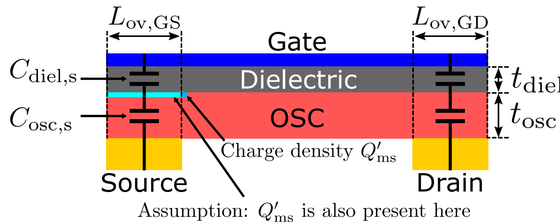

Figure 4.8.: Structure of a staggered OTFT similar as published in ref. [55]. The gate-to-contact overlap regions behave like series connections of two capacitors when the organic semiconductor is operated in depletion. In accumulation, the charge density Q'_{ms} is present in the whole overlap region at the source. Similar considerations hold true for the drain side.

semiconductor is depleted, it has the properties of an insulator with a dielectric constant $\varepsilon_{\text{r,osc}}$. Then, the overlap regions can be treated to a first approximation as a series connection of two parallel-plate capacitors. However, as the organic semiconductor is driven into accumulation

its overall behavior changes towards a conductor. The accumulated charges greatly influence the electrostatics and the imagination of a series connection of two capacitors is no longer valid. This is visualized in Fig. 4.9 where the electrostatic potential in one point within the

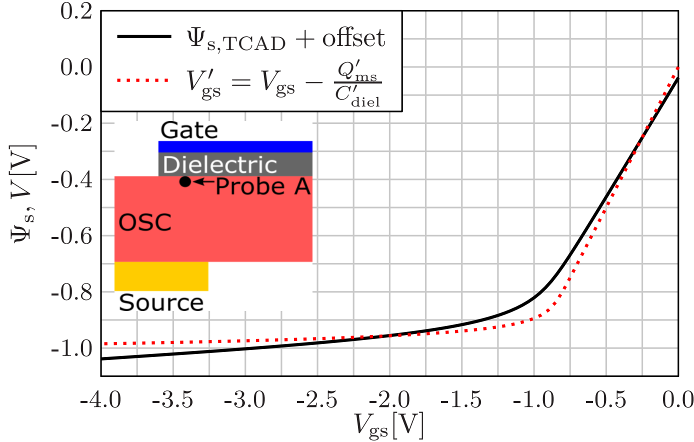

Figure 4.9.: 2D Sentaurus TCAD simulation of the electrostatic potential in the gate-to-source overlap region of a staggered OTFT (solid black line). As depicted by the inset, the potential is probed in direct proximity to the gate dielectric and is thus denoted as the surface potential Ψ_{s}. An offset is added to the simulated potential. In addition, the shape of the function V'_{gs} is shown which is similar to Ψ_{s}. In the TCAD simulation, a Gaussian DOS with a maximum number of states of $N_{\mathrm{t,DOS}} = 1 \times 10^{21}\,\mathrm{cm^{-3}}$, a standard deviation of $\sigma_{\mathrm{DOS}} = 0.05\,\mathrm{eV}$, and an energy shift of $(E_{\mathrm{V}} - E_{0,\mathrm{DOS}}) = 0.05\,\mathrm{eV}$ is used. The relative dielectric permittivities of the gate dielectric and the depleted organic semiconductor are $\varepsilon_{\mathrm{r,diel}} = 3.9$ and $\varepsilon_{\mathrm{r,osc}} = 3$, respectively. The work functions of the source/drain electrodes are aligned with the highest occupied molecular orbital of the organic semiconductor and a constant mobility for holes and electrons of $\mu_{\mathrm{n}} = \mu_{\mathrm{p}} = 1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ is set.

organic semiconductor in the gate-to-source overlap region is shown. Since the potential is probed in direct proximity to the gate dielectric it is denoted as the surface potential Ψ_{s}. It can be seen that in the voltage range from $V_{\mathrm{gs}} = 0\,\mathrm{V}$ to $V_{\mathrm{gs}} = -1\,\mathrm{V}$, the surface potential linearly follows the gate-source voltage. Furthermore, it can be seen that with the gate voltage changing by an absolute amount of $\Delta V_{\mathrm{gs}} = 1\,\mathrm{V}$, the surface potential only exhibits a change of $\Delta\Psi_{\mathrm{s}} = 0.8\,\mathrm{V}$. This makes sense since the probe point is located between the two capacitors consisting of the depleted organic semiconductor and the gate dielectric. The voltage V_{gs} is split up at these two capacitors so that the voltage drop across each of them is smaller than V_{gs}.

With the gate voltage increasing to absolute values greater than 1 V, the organic semiconductor is driven into accumulation. It can be seen in Fig. 4.9 that the surface potential reaches some kind of saturation which is in agreement with the literature [31]. In this operation regime, it would lead to incorrect results if the organic semiconductor and the gate dielectric were still treated as a series connection of two capacitors. Therefore, the following requirements for the gate-to-source overlap region as modeled by the compact model can be formulated:

- In the sub-threshold regime of operation, the organic semiconductor is depleted. The charges stored in the gate-to-source overlap region have to be calculated by the product of the series capacitance and the gate-to-source voltage.
- At the transition to the above-threshold regime, the voltage drop over the series connection of the two capacitances has to start saturating.
- In the above-threshold regime of operation, the voltage drop across the series connection has to nearly saturate. The additional accumulation charges that are present now have to be added to the charges in the series connection of capacitances.

Similar thoughts can be made for the gate-to-drain overlap region where the saturation of the surface potential starts when V_{gd} surmounts the threshold voltage. Regarding the source side, the problem is solved by the definition of a voltage V'_{gs} that fulfills the requirements. Generally, in the above-threshold regime of operation, the density of quasi-mobile charges at the source end of the channel can be approximated as a function of the gate dielectric capacitance, the gate-source voltage, and the threshold voltage of the transistor [36]:

$$Q'_{\mathrm{ms}} = C'_{\mathrm{diel}} \left(V_{\mathrm{gs}} - V_{\mathrm{T0}}\right) \tag{4.25}$$

where $(V_{\mathrm{gs}} - V_{\mathrm{T0}})$ is denoted as the gate-overdrive voltage [5]. In the compact model, the charge density is not calculated based on this equation but based on the charge-based expression in Eq. (2.58). However, in strong accumulation, the charge-based expression in Eq. (2.58) will exhibit a similar trend as Eq. (4.25). Based on these thoughts, an effective gate voltage V'_{gs} is defined for the series connection of the capacitances at the gate-to-source overlap region:

$$V'_{\mathrm{gs}} = V_{\mathrm{gs}} - \frac{Q'_{\mathrm{ms}}}{C'_{\mathrm{diel}}}. \tag{4.26}$$

In the sub-threshold regime of operation, nearly no accumulation charges are present and hence, the charge density Q'_{ms} according to Eq. (2.58) is nearly zero. As a consequence, it can be said:

$$V'_{\mathrm{gs}} \approx V_{\mathrm{gs}}. \tag{4.27}$$

For gate-source voltages close to the threshold voltage, the charge density Q'_{ms} starts increasing rapidly, thus leading to a reduction of V'_{gs}. In the above-threshold regime, Q'_{ms} follows approximately the trend in Eq. (4.25). The consequence is the following:

$$\begin{aligned} V'_{\mathrm{gs}} &\approx V_{\mathrm{gs}} - \frac{C'_{\mathrm{diel}} \left(V_{\mathrm{gs}} - V_{\mathrm{T0}}\right)}{C'_{\mathrm{diel}}} \\ V'_{\mathrm{gs}} &\approx V_{\mathrm{T0}}. \end{aligned} \tag{4.28}$$

It can be seen that V'_{gs} approximately saturates to V_{T0}. The validity of this is proven in Fig. 4.9 where the trend of V'_{gs} is shown accompanied by the TCAD-simulated surface potential in the gate-to-source overlap region. As can be seen, both curves exhibit a similar form.

If the organic semiconductor is driven into accumulation, the charge density along the gate-to-source overlap length is nearly constant since at every position the electric field between the gate and the source electrode is equal. Therefore, the charge density Q'_{ms} that is present at the source end of the channel will be accumulated in the whole overlap region. Furthermore, as explained for the coplanar transistors, it is as well assumed that the charge density Q'_{ms} is present in the regions between the fingers and beyond the first and the last finger, similarly as depicted in Fig. 4.7.

The same explanation as presented for the source side is in principle also valid for the gate-to-drain overlap region. Here, the voltage V_{gd} determines the state in which the organic semiconductor is and the charge density Q'_{md} needs to be considered. A voltage V'_{gd} is defined:

$$V'_{\mathrm{gd}} = V_{\mathrm{gs}} - V_{\mathrm{ds}} - \frac{Q'_{\mathrm{md}}}{C'_{\mathrm{diel}}}. \tag{4.29}$$

Finally, the extrinsic charges in staggered transistors can be expressed as follows:

$$Q_{\mathrm{ex,S,stag}} = V'_{\mathrm{gs}} \frac{C_{\mathrm{diel,s}} C_{\mathrm{osc,s}}}{C_{\mathrm{diel,s}} + C_{\mathrm{osc,s}}} + Q'_{\mathrm{ms}} L_{\mathrm{ov,GS}} W_{\mathrm{ch,G}}, \tag{4.30}$$

$$Q_{\mathrm{ex,D,stag}} = V'_{\mathrm{gd}} \frac{C_{\mathrm{diel,d}} C_{\mathrm{osc,d}}}{C_{\mathrm{diel,d}} + C_{\mathrm{osc,d}}} + Q'_{\mathrm{md}} L_{\mathrm{ov,GD}} W_{\mathrm{ch,G}} \tag{4.31}$$

where $W_{\mathrm{ch,G}}$ is the total gate width as defined by Eq. (2.18) and the capacitances are defined as follows:

$$C_{\mathrm{diel,s}} = \frac{\varepsilon_{\mathrm{r,diel}} \cdot \varepsilon_0}{t_{\mathrm{diel}}} N_{\mathrm{fing}} W_{\mathrm{contact}} L_{\mathrm{ov,GS}}, \tag{4.32}$$

$$C_{\mathrm{diel,d}} = \frac{\varepsilon_{\mathrm{r,diel}} \cdot \varepsilon_0}{t_{\mathrm{diel}}} N_{\mathrm{fing}} W_{\mathrm{contact}} L_{\mathrm{ov,GD}}, \tag{4.33}$$

$$C_{\mathrm{osc,s}} = \frac{\varepsilon_{\mathrm{r,osc}} \cdot \varepsilon_0}{t_{\mathrm{osc}}} N_{\mathrm{fing}} W_{\mathrm{contact}} L_{\mathrm{ov,GS}}, \tag{4.34}$$

$$C_{\mathrm{osc,d}} = \frac{\varepsilon_{\mathrm{r,osc}} \cdot \varepsilon_0}{t_{\mathrm{osc}}} N_{\mathrm{fing}} W_{\mathrm{contact}} L_{\mathrm{ov,GD}} \tag{4.35}$$

where ε_0 is the electric field constant and $\varepsilon_{\mathrm{r,diel}}$ and $\varepsilon_{\mathrm{r,osc}}$ are the relative dielectric permittivities of the gate dielectric and of the organic semiconductor, respectively.

CHAPTER 5

Modeling of Low-Frequency Noise

5.1 Introduction

In every transistor, there occurs a phenomenon denoted as noise. This means that the drain current of a transistor operated under steady-state conditions is effectively not constant but fluctuates around a mean value [46]. Figure 5.1 shows the measured drain current of a transistor

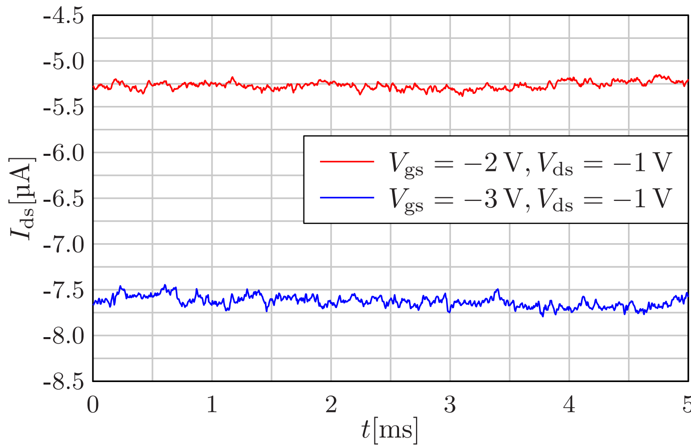

Figure 5.1.: Drain current of a staggered OTFT fabricated by the Max Planck Institute for Solid State Research and measured at the AdMOS GmbH. The current has been measured with the AdMOS noise measurement system. A small period of 5 ms is shown here. The transistor has been measured at two different voltages. The current exhibits the typical noisy shape.

over time where the noisy trend of the drain current versus time can be observed. In this chapter, a brief overview over the noise mechanisms are presented and subsequently, a charge-based compact noise model is derived.

From the plot of the noisy current, there arises the question of how to quantify the noise. The answer to this is a frequency-domain investigation of the noise [39]. A time-continuous signal which is sampled and converted to a digital signal (like the noisy current of the transistor) can be transformed into the frequency domain by means of a discrete Fourier transform [72, 73]. The result of the discrete Fourier transform is a frequency spectrum showing the amplitudes and phases of the sine waves with different frequencies that when being superposed yield the original signal. In the context of noise, usually the so-called power spectral density (PSD) is calculated [39] which shows the power of the signal components with the different frequencies that are contained in the original signal [74].

There exists a variety of different types of noise depending on the electronic device that is investigated. Here, the focus is put on the type of noise that is the most important for transistors which is the low-frequency or flicker noise [39]. The special property of this flicker noise is that its amplitude is inversely proportional to the frequency which means that the noise components with lower frequencies have higher amplitudes. This is the reason why this kind of noise is denoted as low-frequency noise. The PSD of a coplanar OTFT is shown in Fig. 5.2. As a guide

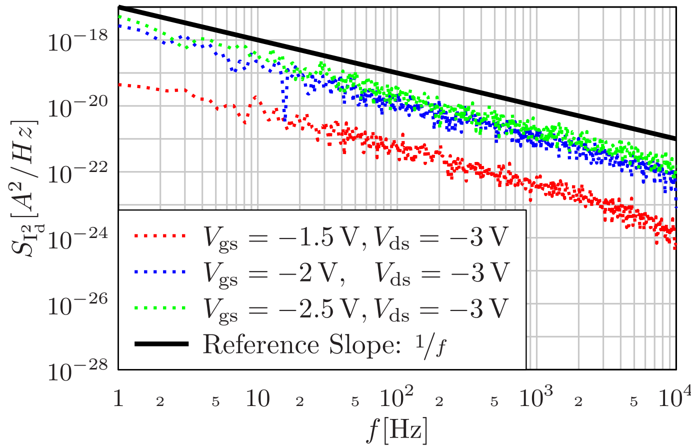

Figure 5.2.: PSD of a coplanar OTFT with a W/L ratio of 100 µm/20 µm measured at different voltages. The solid black line is a $1/f$ curve serving as a reference.

for the eye, a reference curve with a $1/f$ behavior is shown proving that the measured PSDs follow approximately the $1/f$ trend, as predicted. Often, the PSD is normalized with respect to the mean value of the DC current under the respective DC operation conditions. This is shown in Fig. 5.3 where the PSD values are divided by the drain current squared in the respective operation point.

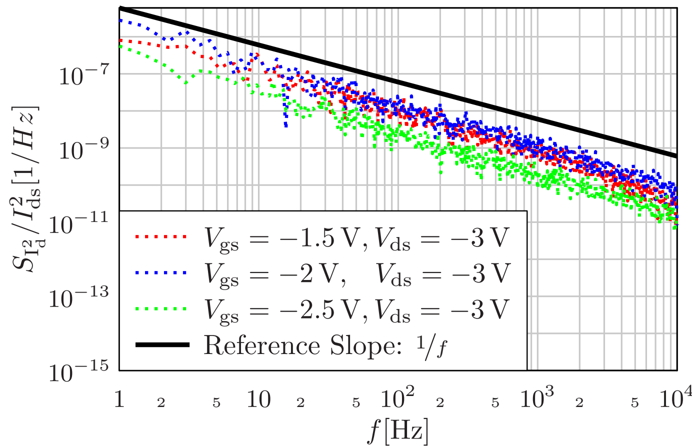

Figure 5.3.: PSD of a coplanar OTFT with a W/L ratio of 100 µm/20 µm measured at different voltages. This figure shows the same as Fig. 5.2, but here, the PSD is normalized with respect to the DC current in the respective operation points.

5.2 Flicker Noise

In transistors, there are basically two types of flicker noise that can occur in the intrinsic carrier channel which are the bulk mobility fluctuations and the carrier number fluctuations [75]. Both of these noise types lead to a $1/f$ behavior in the PSD and from this perspective, they are not distinguishable from each other. However, they show a different dependence of the noise on the drain current level. The main aspects of these two noise types will be outlined and it will be explained how to determine, based on measurement data, which noise type is dominant.

5.2.1 Mobility Fluctuations

The empirical Hooge model attributes the noise of the drain current to a fluctuation in the charge-carrier mobility [39, 75], which will briefly be reviewed in this section. According to [75], the drain-current normalized noise in a MOS transistor due to mobility fluctuations can be expressed as follows:

$$\frac{S_{I_d^2}}{I_{ds}^2} = \frac{\alpha_H}{f W_{ch} L_{ch}^2} \int_0^{L_{ch}} \frac{dx}{Q_i'(x)/q} \tag{5.1}$$

where α_H is the Hooge constant which serves as a fitting parameter, f is the frequency, W_{ch} is the channel width, L_{ch} is the channel length, $Q_i'(x)$ is the mobile inversion charge per gate area, and q is the elementary charge. Please note that here, in the subscript of the PSD ($S_{I_d^2}$), the current is written with an exponent of 2. This does not mean that the noise in reality is the squared noise but it shows that in order to normalize the PSD, it has to be divided by the drain current squared and not by the current to the power of one. Originally, in ref. [75], the

noise is written without the current exponent of 2, i.e. it is denoted as $S_{\mathrm{I_d}}$. In other pieces of literature, such as ref. [39], the exponent of 2 is contained. Applying the gradual-channel approximation and assuming a constant mobility μ_0, the drain-current normalized PSD of a MOS transistor reads as follows [75]:

$$\frac{S_{\mathrm{I_d^2}}}{I_{\mathrm{ds}}^2} = \frac{\alpha_{\mathrm{H}} q \mu_0 V_{\mathrm{ds}}}{f L_{\mathrm{ch}}^2 I_{\mathrm{ds}}}. \tag{5.2}$$

It can be assumed that in principle, this theory is also valid for organic transistors. In contrast to the MOS transistor, the inversion charge is an accumulation charge but the fact that a fluctuation in the effective mobility leads to a fluctuation in the drain-source current can easily be verified by observing the current equation for the organic TFTs Eq. (2.21). From Eq. (5.2), it can be concluded that the drain-current normalized PSD is inversely proportional to the drain current. Consequently, when probing the noise at a fixed frequency, a $1/I_{\mathrm{ds}}$ slope will be visible.

5.2.2 Charge-Carrier Number Fluctuations

Another phenomenon leading to a flicker noise are charge-carrier number fluctuations. It can happen that a charge carrier in the intrinsic carrier channel gets trapped in an oxide trap [75–77]. Due to this trapping action, the carrier does not contribute to the drain current anymore until finally, it gets released from the oxide trap. If a charge carrier gets trapped in an oxide trap, it behaves like a fixed oxide charge. According to the theory, oxide charges impose changes on the flat band voltage V_{fb} [46]. Please recall that the flatband voltage is the gate voltage that needs to be applied in order to have fully flat bands in the semiconductor along a cutline normal to the gate electrode. In case of a change in the flatband voltage, e.g. because of a charge that gets trapped in the gate dielectric, the gate voltage would have to change by the same amount in order to compensate for this. Assuming that the gate voltage is kept constant, such as in a steady-state operation point, then a fluctuation in the flatband voltage due to a trapping action is not compensated which leads to a fluctuation in the drain current. This fluctuation has the same magnitude independent of whether the flatband voltage fluctuates or the gate voltage fluctuates by the same amount (but with an opposite sign). The fluctuation in the drain current due to a fluctuation in the flatband voltage is then expressed as follows [75]:

$$\delta_{I_{\mathrm{ds}}} = \frac{dI_{\mathrm{ds}}}{dV_{\mathrm{fb}}} \cdot \delta V_{\mathrm{fb}} \tag{5.3}$$

where δV_{fb} is a fluctuation in the flatband voltage. It becomes evident that here the drain current has been derived with respect to the flatband voltage. This is reasonable since this derivative expresses the change in the drain current with respect to a change in the flatband voltage which multiplied by a change in V_{fb} yields the absolute change in the drain current.

Making use of the above-mentioned effect that $\delta V_{\mathrm{fb}} = -\delta V_{\mathrm{gs}}$, this equation can be rewritten as:

$$\delta_{I_{\mathrm{ds}}} = \left(-\frac{dI_{\mathrm{ds}}}{dV_{\mathrm{gs}}}\right)\delta V_{\mathrm{fb}}. \tag{5.4}$$

It can be made use of the fact that the derivative of the drain current with respect to the gate potential is called the transconductance of the transistor:

$$g_{\mathrm{m}} = \frac{dI_{\mathrm{ds}}}{dV_{\mathrm{gs}}}. \tag{5.5}$$

After some steps that will not be reviewed here, the current-normalized PSD of the noise can be expressed as follows [75, 76]:

$$\frac{S_{\mathrm{I_d^2}}}{I_{\mathrm{ds}}^2} = \left(\frac{g_{\mathrm{m}}}{I_{\mathrm{ds}}}\right)^2 \cdot S_{\mathrm{V_{fb}}} \tag{5.6}$$

where $S_{\mathrm{V_{fb}}}$ is the PSD of the flat band voltage which is assumed to be independent of the applied terminal voltages at the transistor. Furthermore, $S_{\mathrm{V_{fb}}}$ is inversely proportional to the frequency [76]. Even if this equation is valid for a conventional MOS transistor, it is assumed that the basic theory behind it is also valid for organic transistors. From Eq. (5.6), an interesting fact becomes visible: The noise when probed at a fixed frequency is proportional to $\left({}^{g_{\mathrm{m}}}/_{I_{\mathrm{ds}}}\right)^2$. This is in contrast to the noise due to mobility fluctuations which according to Eq. (5.2) is proportional to $1/I_{\mathrm{ds}}$. This can be used as a criterion to decide which type of noise is dominant in a transistor. Since both the mobility-fluctuation noise and the carrier-number-fluctuation noise are inversely proportional to the frequency, the dominant noise mechanism in a transistor cannot be determined by observing its PSD over frequency. A plot of the PSD at a fixed frequency over the drain current is necessary and based on this, it can be observed whether the noise follows a $1/I_{\mathrm{ds}}$ trend or a $\left({}^{g_{\mathrm{m}}}/_{I_{\mathrm{ds}}}\right)^2$ trend.

In the literature, there has been proposed an approach taking into account the effect that a trapping action of a charge carrier can induce a fluctuation of the scattering rate which leads to a fluctuation in the effective mobility [77]. The PSD of the noise including this correlated mobility fluctuation is given by the following equation [77]:

$$\frac{S_{\mathrm{I_d^2}}}{I_{\mathrm{ds}}^2} = \left(1 \mp \alpha_{\mathrm{corr}}\mu_{\mathrm{eff}}C'_{\mathrm{diel}}\frac{I_{\mathrm{ds}}}{g_{\mathrm{m}}}\right)^2 \cdot \left(\frac{g_{\mathrm{m}}}{I_{\mathrm{ds}}}\right)^2 \cdot S_{\mathrm{V_{fb}}} \tag{5.7}$$

where α_{corr} is a fitting parameter controlling the correlation between a trapping action and the induced mobility fluctuation. It becomes evident that the effect of a correlated mobility fluctuation is higher if ${}^{I_{\mathrm{ds}}}/_{g_{\mathrm{m}}}$ is larger. This is actually the case for high currents [39]. Therefore at lower currents, this noise model shows a similar behavior as the noise model taking into account only the charge-carrier-number fluctuations without correlated mobility fluctuations. Consequently, the noise according to Eq. (5.7) cannot unintentionally be mistaken with the bulk mobility fluctuation noise (Eq. (5.2)).

UNIVERSITAT ROVIRA I VIRGILI
CHARGE-BASED COMPACT MODELING OF CAPACITANCES AND LOW-FREQUENCY NOISE IN ORGANIC THIN-FILM TRANSISTORS
Jakob Simon Leise

5.3 Determining the Dominant Noise Mechanism

In this section, the measured noise of fabricated organic TFTs will be shown and it will be evaluated which is the dominant noise mechanism. The measurements under investigation in this work were presented by Muhea et al. in ref. [76]. The transistors are bottom-contact top-gate transistors (staggered) and were fabricated at the Laboratoire d'Innovation pour les Technologies des Energies Nouvelles et les Nanomatériaux (LITEN) at the Commissariat à l'Énergie Atomique et aux Énergies Alternatives (CEA). Transistors with various channel lengths were fabricated on a flexible plastic substrate using a spin-coating process for the organic semiconductor.

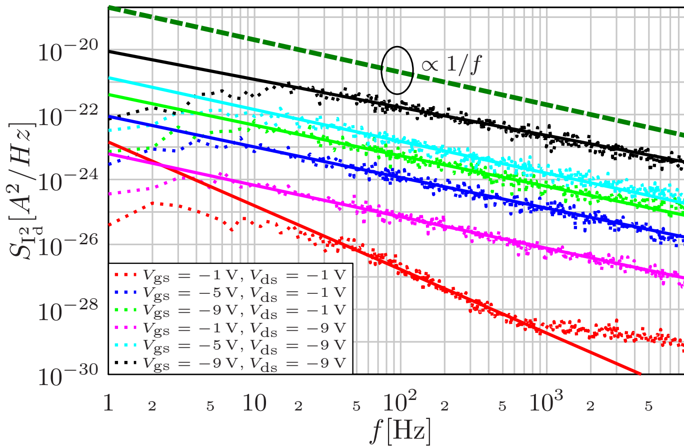

Figure 5.4.: PSD of a staggered OTFT with a W/L ratio of 1000 µm/10 µm measured at different voltages. The measurements are taken from ref. [76]. The dashed green line is a $1/f$ curve serving as a reference. The dotted lines show the measurements while the solid lines represent regression functions which were calculated for each curve in the frequency range $20\,\text{Hz} < f < 400\,\text{Hz}$.

In Fig. 5.4, the measured PSD of one transistor of the set is depicted for various combinations of the gate-source and the drain-source voltages. As usual, the measurements exhibit a noisy shape which makes the extraction of the noise at a fixed frequency inaccurate. In order to improve the noise extraction at a fixed frequency, regression functions are calculated by Matlab [71]. When extracting the noise at a fixed frequency, these regression functions are probed rather than the noisy shape of the measured PSD. In the figure, a reference slope with a $1/f$ behavior is plotted which proves the adherence of the measurements to this slope. Except for the measurements at the lowest V_{gs} and V_{ds}, all data follow approximately a $1/f$ trend.

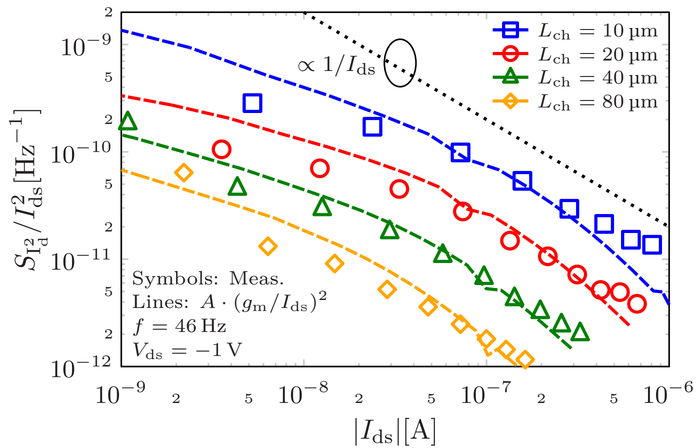

Figure 5.5.: Drain-current normalized noise of the staggered organic TFTs presented in ref. [76] plotted against the drain current. The transistors have a channel width of $W_{ch,SD} = 1000\,\mu m$ and different channel lengths as shown in the legend. The noise is extracted from the plot versus frequency by probing the regression functions shown in Fig. 5.4 at a frequency of $f = 46\,Hz$. The drain-source voltage is $V_{ds} = -1\,V$. The measurements (symbols) are shown in comparison to the transconductance ratio $(g_m/I_{ds})^2$ multiplied by an individual constant A for each curve. For comparison purposes, a curve proportional to $1/I_{ds}$ is shown.

In Figs. 5.5 and 5.6, the drain-current normalized noise of several transistors of the set is shown versus the drain current. These plots are generated from the noise PSDs by probing the regression functions at a fixed frequency of $f = 46\,Hz$. In the plots, the measured noise is shown in comparison to $(g_m/I_{ds})^2$ which is multiplied by an individual constant A for each transistor. Furthermore, a function exhibiting a $1/I_{ds}$ slope is shown. As stated above, the dominant noise mechanism can be determined by comparing the measured noise to $(g_m/I_{ds})^2$ and to $1/I_{ds}$. In this case, as can be seen well in Fig. 5.6, the measured noise has a larger agreement with $(g_m/I_{ds})^2$ than with $1/I_{ds}$. This reveals that the dominant noise mechanism in these transistors is the charge-carrier number fluctuation. Thus, in the following sections, a compact model for this kind of noise is presented. For the sake of completeness, a compact model describing the bulk mobility fluctuations will be derived as well.

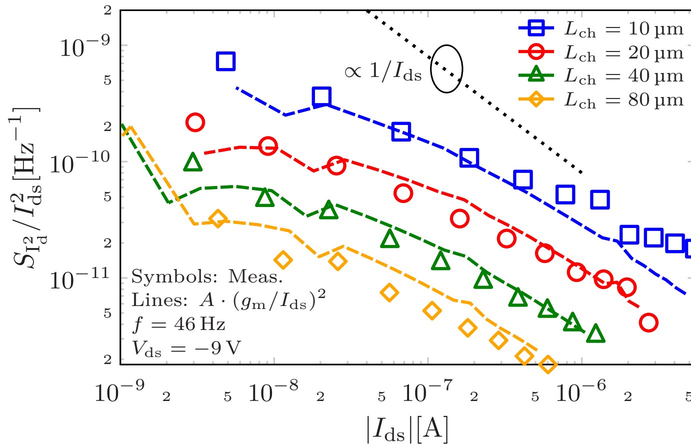

Figure 5.6.: Drain-current normalized noise of the staggered organic TFTs presented in ref. [76] plotted against the drain current. The plot shows the same as Fig. 5.5 but at a drain-source voltage of $V_{ds} = -9\,\mathrm{V}$. The measurements (symbols) are shown in comparison to the transconductance ratio $(g_m/I_{ds})^2$ multiplied by an individual constant A for each curve. For comparison purposes, a curve proportional to $1/I_{ds}$ is shown.

5.4 Compact Modeling of the Noise

In this chapter, a charge-based compact model for the description of the noise in the intrinsic carrier-channel is derived. In the literature, many noise models for different transistor types have been proposed such as for MOSFETs [52, 75, 77–79] or different types of thin-film transistors [80, 81]. The origin of noise in OTFTs has been investigated in the literature and different standard approaches originally developed for MOSFETs or other types of TFTs are used in order to quantify the noise [76, 82–85]. A comprehensive model for the description of the noise in OTFTs originating from trapping of charge carriers in the gate dielectric and the organic semiconductor was developed by Han et al. [85]. In this section, a charge-based compact model for the low-frequency noise will be derived. The advantage of this model is that it provides a full description of both the charge-carrier number fluctuations and bulk mobility fluctuations and that it is entirely charge-based. The derivation of this model is based on the procedure in ref. [39]. There, the noise model is derived for conventional MOSFETs incorporating a charge-based DC model that serves as a basis. Reference [39] will not be cited after each paragraph but it shall be noted that the complete derivation process is based on it.

5.4.1 Normalization of the DC Model

The charge-based compact DC model [36] that serves as a basis for the noise model is explained in Chap. 2. In ref. [39], the charge densities and the drain current are normalized with respect to a specific charge and a specific current, respectively. The advantage of working with normalized currents and charges is that the derivation is easier and that it can easily be transferred to other models that also use normalizations. In the following, the normalizations that are used for the model are presented. For this purpose, some of the equations of the DC model are depicted again. To start with, the charge density at the source end of the channel according to Eq. (2.58) is reviewed:

$$Q'_{\mathrm{ms}} = \frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)} \cdot C'_{\mathrm{diel}} \cdot \mathcal{L}\left\{\exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}} - \Delta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right\}. \tag{5.8}$$

The charge density at the drain end of the channel according to Eq. (2.59) reads as follows:

$$Q'_{\mathrm{md,barr}} = \frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)} \cdot C'_{\mathrm{diel}} \cdot \mathcal{L}\left\{\exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{T0}} - V_{\mathrm{ds}} + V_{\mathrm{sb,d}} - \Delta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right\}. \tag{5.9}$$

In these two equations, the Lambert W function returns a unitless value and the prefactors then provide the unit. Therefore, a specific charge Q_{sp} is defined as follows:

$$Q_{\mathrm{sp}} = \frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)} \cdot C'_{\mathrm{diel}} = (\beta+1)\cdot\alpha\cdot\frac{k_{\mathrm{B}}T}{q}\cdot C'_{\mathrm{diel}} \;\left[\mathrm{A\,s\,cm^{-2}}\right] \tag{5.10}$$

where α is the slope degradation factor as defined in ref. [36]. With this specific charge, the charge densities are normalized. By convention, the normalized charges are now written in small letters. Furthermore, in order to simplify the subsequent derivation, the subscript *barr* in the charge density at the drain is omitted. The normalized charges are defined as follows:

$$q_{\mathrm{m}} = q_{\mathrm{c}} = \frac{Q'_{\mathrm{m}}}{Q_{\mathrm{sp}}}, \tag{5.11}$$

$$q_{\mathrm{s}} = \frac{Q'_{\mathrm{ms}}}{Q_{\mathrm{sp}}}, \tag{5.12}$$

$$q_{\mathrm{d}} = \frac{Q'_{\mathrm{md,barr}}}{Q_{\mathrm{sp}}} \tag{5.13}$$

where the mobile charge q_{m} is also denoted as the channel charge q_{c}. The two values are identical. For convenience, the drain-current equation of the DC model according to Eq. (2.21) is reviewed here as well:

$$I_{\mathrm{ds}} = \mu_{\mathrm{eff}}\cdot W_{\mathrm{ch,eff}}\cdot\left(\frac{k_{\mathrm{B}}\cdot T}{q}\cdot\frac{Q'_{\mathrm{ms}} - Q'_{\mathrm{md,barr}}}{L_{\mathrm{ch}}} + \frac{Q'^{2}_{\mathrm{ms}} - Q'^{2}_{\mathrm{md,barr}}}{2\cdot L_{\mathrm{ch}}\cdot C'_{\mathrm{diel}}}\right)\cdot\left(1 + \lambda\cdot(V_{\mathrm{ds}} - V_{\mathrm{dsx}})\right).$$

Similarly as the specific charge, a specific current is defined as follows:

$$I_{\mathrm{sp}} = \mu_{\mathrm{eff}} \cdot (\beta+1)^2 \cdot \alpha^2 \cdot \left(\frac{k_{\mathrm{B}}T}{q}\right)^2 \cdot C'_{\mathrm{diel}} \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \; [\mathrm{A}] \tag{5.14}$$

and with this, the drain current is normalized:

$$i_{\mathrm{ds}} = \frac{I_{\mathrm{ds}}}{I_{\mathrm{sp}}}. \tag{5.15}$$

Therefore, the drain current can be formulated in terms of the following expression:

$$i_{\mathrm{ds}} = \left(\frac{1}{2}\left(q_{\mathrm{s}}^2 - q_{\mathrm{d}}^2\right) + \frac{1}{(\beta+1)\cdot\alpha}\left(q_{\mathrm{s}} - q_{\mathrm{d}}\right)\right) \tag{5.16}$$

where the channel-length modulation is omitted because the noise model will be derived only for transistors with longer channels. If the current and the charge densities are denormalized, the standard current equation according to ref. [36] is yielded again.

Now, the DC model has been transformed into a normalized version which will simplify the further derivation process. It shall be noted that in spite of using the charge density $Q'_{\mathrm{md,barr}}$, which is reduced by a voltage drop across the drain barrier, the derivation steps in the following section are performed without a closer look at short-channel effects.

5.4.2 Preparational Steps for the Noise Model

In this section, some preparational steps for the calculation of noise in a transistor are explained. This section is valid for every type of noise that can occur along the intrinsic carrier channel. After the preparational steps, the equations for the carrier-number-fluctuation noise or for the bulk mobility fluctuations can be incorporated. The starting point in ref. [39] is to imagine the

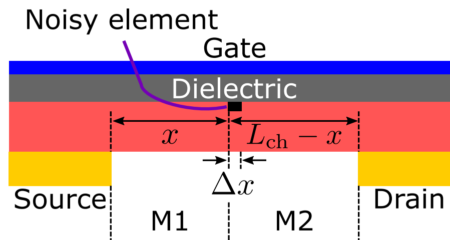

Figure 5.7.: Schematic of a staggered OTFT containing a small noise element in the channel at position x. The channel segment to the left and to the right of this noisy element is regarded as a new transistor of channel length x and $L_{\mathrm{ch}} - x$, respectively. This picture is drawn in analogy to ref. [39].

noise as a contribution of an infinite number of infinitesimally small noise elements distributed along the channel. One of these noisy elements is depicted in Fig. 5.7 which is located at position x and has a length Δx. It is assumed that this noisy element is a little current source

causing local fluctuations of the channel current. However, the local fluctuation does not directly propagate to the transistor terminals but has to travel through the channel segments to the left and the right. The channel segment to the left of the noisy element is of length x and is supposed to behave like a transistor denoted as M1. Accordingly, the channel segment to the right is of length $L_{\mathrm{ch}} - x$ and is denoted as M2. The influence of the local noisy element is then translated by the transistors M1 and M2 into a fluctuation of the total drain current. The equivalent circuit of the small noise element located between the two transistors M1 and

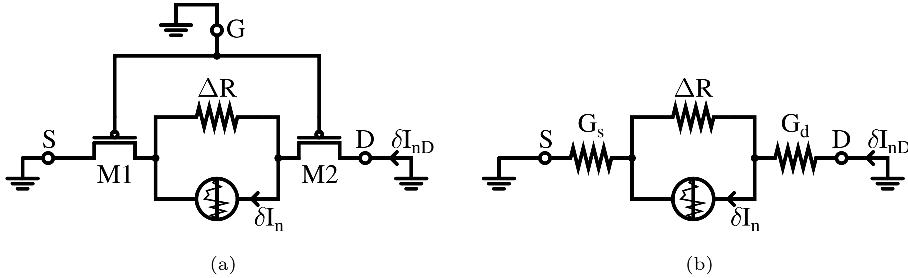

Figure 5.8.: (a) Equivalent circuit of a noisy element located between two transistors. The local noise current is denoted as δI_{n} and its contribution to the total drain current is denoted as δI_{nD}. (b) Simplification of the circuit by linearization of the transistors in the operation point and describing them by their channel conductances. Both circuits are drawn in analogy to ref. [39].

M2 is depicted in Fig. 5.8(a). In accordance with ref. [39], the noisy element is modeled as a current source in parallel to a resistance ΔR. The local noise current is denoted as δI_{n}. The fluctuation of the drain current that is induced due to the small noisy element is denoted as δI_{nD}. It is now assumed that the voltage that is induced in the channel due to δI_{n} is very small in comparison to the thermal voltage ($k_{\mathrm{B}}T/q$) so that the transistors M1 and M2 can be linearized in their DC operation points. This is depicted in Fig. 5.8(b) where the two transistors are only represented by their channel conductances G_{s} and G_{d}. Now, the current δI_{nD} has to be calculated. This can be done, for example, by converting the noisy current source with its parallel resistance ΔR into an equivalent voltage source and then calculating the total current in the series connection of ΔR and the two transistors. Now, another assumption is made: ΔR is very small in comparison to $1/G_{\mathrm{s}}$ and $1/G_{\mathrm{d}}$. Therefore, when summing up all three values, ΔR is negligible. Consequently, the contribution of δI_{n} to δI_{nD} can be expressed as follows:

$$\delta I_{\mathrm{nD}} = G_{\mathrm{ch}}(x) \cdot \Delta R \cdot \delta I_{\mathrm{n}} \tag{5.17}$$

where

$$\frac{1}{G_{\mathrm{ch}}(x)} = \frac{1}{G_{\mathrm{s}}(x)} + \frac{1}{G_{\mathrm{d}}(x)}. \tag{5.18}$$

It shall be emphasized that the quantities depend on the position x in the channel. Next, the PSD of δI_{nD} is calculated as follows [39]:

$$S_{\delta \mathrm{I}^2_{\mathrm{nD}}}(\omega, x) = G^2_{\mathrm{ch}}(x) \cdot \Delta R^2(x) \cdot S_{\delta \mathrm{I}^2_{\mathrm{n}}}(\omega, x) \tag{5.19}$$

where ω is the angular frequency of the noise. As mentioned above, it is a convention that the current in the subscript of the PSDs appears in a squared form. $S_{\delta \mathrm{I}^2_{\mathrm{nD}}}$ is the PSD of the drain current that originates from the small noisy current source in the channel. However, the goal is to calculate the PSD of the total drain current. For this purpose, the contributions of all the noisy elements in the channel have to be summed up by an integration:

$$S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega) = \int_0^{L_{\mathrm{ch}}} G^2_{\mathrm{ch}}(x) \Delta R^2(x) \frac{S_{\delta \mathrm{I}^2_{\mathrm{n}}}(\omega,x)}{\Delta x} dx \tag{5.20}$$

where $S_{\delta \mathrm{I}^2_{\mathrm{n}}}$ is divided by Δx so that it is a contribution per unit length. In order to come closer towards a solution of this equation, a long-channel simplification is performed. In general, the resistance of a channel element can be expressed as

$$\Delta R = \frac{\Delta V}{I_{\mathrm{ds}}} \tag{5.21}$$

where ΔV is a voltage drop in the direction of the channel. Adapting the drift-diffusion model similarly as in Eq. (4.4), it can be written

$$I_{\mathrm{ds}} = \mu_{\mathrm{eff}} \cdot W_{\mathrm{ch,eff}} \cdot Q'_{\mathrm{m}}(x) \frac{\Delta V}{\Delta x} \tag{5.22}$$

which can be rearranged for ΔR:

$$\Delta R = \frac{\Delta V}{I_{\mathrm{ds}}} = \frac{\Delta x}{\mu_{\mathrm{eff}} \cdot W_{\mathrm{ch,eff}} \cdot Q'_{\mathrm{m}}(x)}. \tag{5.23}$$

The next step is to find expressions for the local channel conductances. For this, a step back is taken and the equations for the density of quasi-mobile charges are observed again (Eqs. (5.8), (5.9)). For the further derivation, the voltage drop $V_{\mathrm{sb,d}}$ across the drain-to-semiconductor junction is omitted because the noise model presented here is valid only for long-channel devices. The two aforementioned equations allow for a calculation of the density of quasi-mobile charges at the source and drain end of the channel, respectively. It would be desirable to be able to calculate the charge densities at any arbitrary position along the channel but the exact propagation of the applied drain-source voltage V_{ds} is not known. Only at the source and drain electrodes, the boundary conditions are known. However, the charge densities can also be expressed for any arbitrary position in the channel by defining a channel voltage V_{ch} which reflects the quasi-Fermi potential. With the definition of the channel voltage, the charge density is expressed as follows:

$$Q'_{\mathrm{m}} = \frac{(\beta+1)\cdot S_{\mathrm{obs}}}{\ln(10)} \cdot C'_{\mathrm{diel}} \cdot \mathcal{L}\left\{\exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{ch}} - V_{\mathrm{T0}} - \Delta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right\}. \tag{5.24}$$

Now, the charge is normalized with respect to Q_{sp}:

$$q_{\mathrm{m}} = \mathcal{L}\left\{\exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{ch}} - V_{\mathrm{T0}} - \Delta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right)\right\}. \tag{5.25}$$

Recalling the definition of the Lambert W function

$$x = \mathcal{L}(y) \tag{5.26}$$

as the inverse of the problem according to Eq. (2.25)

$$y = x \cdot \exp(x), \tag{5.27}$$

Eq. (5.25) can be reformulated as follows:

$$\exp\left(\frac{V_{\mathrm{gs}} - V_{\mathrm{ch}} - V_{\mathrm{T0}} - \Delta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)}\right) = q_{\mathrm{m}} \cdot \exp(q_{\mathrm{m}}). \tag{5.28}$$

Calculating the natural logarithm of both sides of the equations leads to:

$$\frac{V_{\mathrm{gs}} - V_{\mathrm{ch}} - V_{\mathrm{T0}} - \Delta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)} = \ln(q_{\mathrm{m}}) + q_{\mathrm{m}}. \tag{5.29}$$

In strong inversion, the linear q_{m} term dominates over the logarithmic term and therefore, the strong inversion approximation is used leading to

$$\frac{V_{\mathrm{gs}} - V_{\mathrm{ch}} - V_{\mathrm{T0}} - \Delta V_{\mathrm{T0}}}{(\beta+1)\cdot S_{\mathrm{obs}}/\ln(10)} \approx q_{\mathrm{m}}. \tag{5.30}$$

Finally, the charges are denormalized again with respect to Q_{sp} and the equation is rearranged. The result is:

$$V_{\mathrm{gs}} - V_{\mathrm{ch}} - V_{\mathrm{T0}} - \Delta V_{\mathrm{T0}} = \frac{Q'_{\mathrm{m}}}{C'_{\mathrm{diel}}}. \tag{5.31}$$

All the equations presented so far are just a result of some assumptions in combination with rearrangements of the original charge density equation. The benefit of Eq. (5.31) is that for the case of strong inversion, the charge density divided by C'_{diel} can schematically be plotted versus the channel voltage which is useful for the further derivation of the noise model.

In Fig. 5.9, $Q'_{\mathrm{m}}(x)/C'_{\mathrm{diel}}$ is plotted over V_{ch}. In this plot, the function hits the V_{ch}-axis at a voltage called the pinch-off voltage V_{p}. In reality, the charge density does not really become zero but converges to zero. Since the strong inversion approximation is depicted here the function is only linear and the logarithmic term is neglected. An interesting fact is that the area below the curve is proportional to the drain current [39] which is a consequence

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CHARGE-BASED COMPACT MODELING OF CAPACITANCES AND LOW-FREQUENCY NOISE IN ORGANIC THIN-FILM TRANSISTORS
Jakob Simon Leise

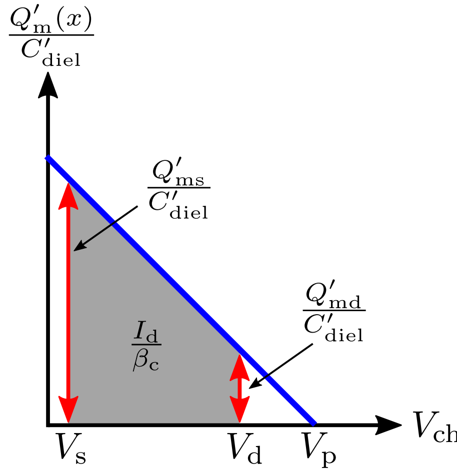

Figure 5.9.: Schematic plot of $Q'_\mathrm{m}(x)/C'_\mathrm{diel}$ vs. the channel voltage V_ch. It is possible to calculate the charge densities explicitly only at the source and drain end of the channel where the potentials V_s and V_d are present, respectively. The function $Q'_\mathrm{m}(x)/C'_\mathrm{diel}$ is pinched off at a voltage V_p. The drain current is proportional to the area below the curve. The factor β_c is defined as: $\beta_\mathrm{c} = \mu_\mathrm{eff} \cdot C'_\mathrm{diel} \cdot W_\mathrm{ch,eff}/L_\mathrm{ch}$. This picture is drawn in analogy to ref. [39].

of the drift-diffusion model. With this knowledge, the channel conductance at an arbitrary channel voltage V_ch can be calculated: Small variations of the source and drain potentials result in a change of the area below the curve. Hence, multiplying a change in V_s and V_d by the corresponding value $Q'_\mathrm{m}(x)/C'_\mathrm{diel}$ yields this change in the area. Theoretically, the change of the area would have to be calculated by taking into account the slope of the function $Q'_\mathrm{m}(x)/C'_\mathrm{diel}$ but here, the slope is disregarded. This is done because it is assumed that the voltage change is only small so that a rectangular approximation of the areal change, which is in fact a rectangle with a small triangular top, is regarded as sufficient. The following expressions for the transconductances at the source and drain end of the channel can be obtained:

$$G_\mathrm{ms} = \beta_\mathrm{c} \cdot \frac{Q'_\mathrm{ms}}{C'_\mathrm{diel}} \tag{5.32}$$

$$G_\mathrm{md} = \beta_\mathrm{c} \cdot \frac{Q'_\mathrm{md}}{C'_\mathrm{diel}} \tag{5.33}$$

where

$$\beta_\mathrm{c} = \mu_\mathrm{eff} \cdot C'_\mathrm{diel} \cdot \frac{W_\mathrm{ch,eff}}{L_\mathrm{ch}}. \tag{5.34}$$

Now, there arises the question of how to calculate the channel conductance $G_\mathrm{ch}(x)$ based on the transconductances of the transistors M1 and M2 in Fig. 5.8(a). The series connection of the two transistors is visualized in Fig. 5.10. They are interfacing each other at position x in the channel where the channel voltage has a value of V_x. A variation of the voltage V_x leads to a change in the areas below the $Q'_\mathrm{m}(x)/C'_\mathrm{diel}$ curve and hence to change in the current.

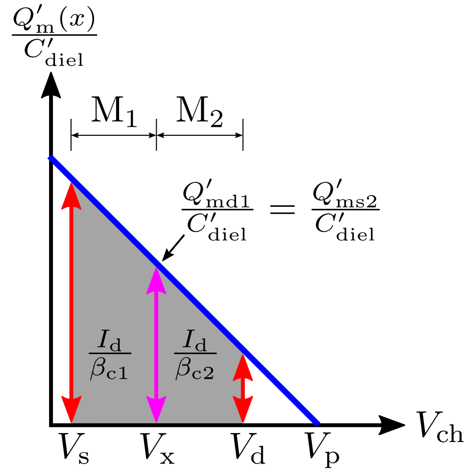

Figure 5.10.: Schematic plot of $Q'_{\mathrm{m}}(x)/C'_{\mathrm{diel}}$ vs. the channel voltage V_{ch}. The two transistors M1 and M2 are interfacing each other at the position x in the channel, where the voltage V_x can be found. $\beta_c = \mu_{\mathrm{eff}} \cdot C'_{\mathrm{diel}} \cdot W_{\mathrm{ch,eff}}/L_{\mathrm{ch}}$. This picture is drawn in analogy to ref. [39].

At position x, the conductances of the two transistors M1 and M2 are expressed as:

$$G_{\mathrm{md1}} = \beta_{\mathrm{c1}} \cdot \frac{Q'_{\mathrm{md1}}}{C'_{\mathrm{diel}}} = \mu_{\mathrm{eff}} \cdot \frac{W_{\mathrm{ch,eff}}}{x} \cdot Q'_{\mathrm{md1}} \tag{5.35}$$

$$G_{\mathrm{ms2}} = \beta_{\mathrm{c2}} \cdot \frac{Q'_{\mathrm{ms2}}}{C'_{\mathrm{diel}}} = \mu_{\mathrm{eff}} \cdot \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}} - x} \cdot Q'_{\mathrm{ms2}}. \tag{5.36}$$

As can be seen in Fig. 5.10, the charge density at the drain end of transistor M1 equals the charge density at the source end of transistor M2: $Q'_{\mathrm{md1}} = Q'_{\mathrm{ms2}} = Q'_{\mathrm{m}}(x)$. Based on this, the channel conductance $G_{\mathrm{ch}}(x)$ which is needed for the calculation of the noise according to Eq. (5.20) can be calculated:

$$\begin{aligned} G_{\mathrm{ch}}(x) &= \frac{1}{\frac{1}{G_{\mathrm{md1}}} + \frac{1}{G_{\mathrm{ms2}}}} \\ &= \mu_{\mathrm{eff}} \cdot W_{\mathrm{ch,eff}} \cdot Q'_{\mathrm{m}}(x) \cdot \frac{1}{x + L_{\mathrm{ch}} - x} \\ &= \frac{\mu_{\mathrm{eff}} \cdot W_{\mathrm{ch,eff}} \cdot Q'_{\mathrm{m}}(x)}{L_{\mathrm{ch}}}. \end{aligned} \tag{5.37}$$

This equation is in accordance with ref. [39]. A short summary will be drawn now: In the last paragraphs, analytical equations for the resistance of a small channel segment (ΔR) and for the channel conductance as seen from point x in the channel ($G_{\mathrm{ch}}(x)$) were derived. The purpose of this is that the noise equation (Eq. (5.20)) also includes the product $\Delta R \cdot G_{\mathrm{ch}}(x)$. Based on the equations derived above, this product can be evaluated as:

$$G_{\mathrm{ch}}(x) \cdot \Delta R = \frac{\mu_{\mathrm{eff}} \cdot W_{\mathrm{ch,eff}} \cdot Q'_{\mathrm{m}}(x)}{L_{\mathrm{ch}}} \cdot \frac{\Delta x}{\mu_{\mathrm{eff}} \cdot W_{\mathrm{ch,eff}} \cdot Q'_{\mathrm{m}}(x)} = \frac{\Delta x}{L_{\mathrm{ch}}}. \tag{5.38}$$

Incorporating this into Eq. (5.20) leads to

$$S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega) = \int_0^{L_{\mathrm{ch}}} \left(\frac{\Delta x}{L_{\mathrm{ch}}}\right)^2 \frac{S_{\delta \mathrm{I}^2_{\mathrm{n}}}(\omega,x)}{\Delta x} dx$$
$$= \frac{1}{L^2_{\mathrm{ch}}} \cdot \int_0^{L_{\mathrm{ch}}} \Delta x S_{\delta \mathrm{I}^2_{\mathrm{n}}}(\omega,x) dx. \tag{5.39}$$

Now, all preparational steps have been performed. As can be seen, a solution of Eq. (5.39) requires an analytical description of the PSDs of the local noise sources which are distributed along the channel. In principle, every arbitrary type of noise which is distributed along the channel and causes local fluctuations can be incorporated into the above-mentioned equation.

5.4.3 Modeling of Carrier Number Fluctuations

In this section, an analytical description of the local PSD due to carrier-number fluctuations is presented. The starting point is again the drift-diffusion model which, even if already presented before, will be shown here again:

$$I_{\mathrm{ds}} = \mu_{\mathrm{eff}} W_{\mathrm{ch,eff}} Q'_{\mathrm{m}}(x) \frac{dV}{dx} = \mu_{\mathrm{eff}} W_{\mathrm{ch,eff}} q N'(x) \frac{dV}{dx} \tag{5.40}$$

where $N'(x) = Q'_{\mathrm{m}}(x)/q$ is the number of charge carriers per gate area which is simply the charge density per gate area divided by the elementary charge q. If a charge carrier gets trapped in an interface or gate dielectric trap or if it gets released from such a trap, the density of charge carriers ($N'(x)$) is slightly reduced or increased, resulting in a small change in the local current according to Eq. (5.40). Furthermore, it is assumed that a trapping or a detrapping action has an influence on the scattering mechanism in that area and causes a carrier-trapping-induced mobility fluctuation [77]. This mobility fluctuation may not be confused with the mobility fluctuations according to the Hooge model for flicker noise [75]. The drain-current fluctuation due to the carrier trapping and the correlated mobility fluctuation is defined as [39]:

$$\frac{\delta I_{\mathrm{D}}}{I_D} = \frac{\delta N'}{N'} + \frac{\delta \mu_{\mathrm{eff}}}{\mu_{\mathrm{eff}}}. \tag{5.41}$$

Instead of using the charge-carrier number per gate area, this equation can also be written based on the charge density:

$$\frac{\delta I_{\mathrm{D}}}{I_D} = \frac{\delta Q'_{\mathrm{m}}}{Q'_{\mathrm{m}}} + \frac{\delta \mu_{\mathrm{eff}}}{\mu_{\mathrm{eff}}}. \tag{5.42}$$

The correlation of the trapping actions and the mobility is expressed by the following equation:

$$\frac{1}{\mu_{\mathrm{eff}}} = \frac{1}{\mu_{\mathrm{low}}} + \tilde{\alpha_{\mathrm{c}}} \cdot N'_{\mathrm{tc}} = \frac{1}{\mu_{\mathrm{low}}} + \alpha_{\mathrm{c}} \cdot Q'_{\mathrm{t}} \tag{5.43}$$

where N'_{tc} is the number of trapped charge carriers per gate area, Q'_{t} is accordingly the amount of trapped charges per gate area, μ_{eff} is the effective mobility from the DC model, $\alpha_{\mathrm{c}} = \tilde{\alpha_{\mathrm{c}}}/q$ is called the Coulomb scattering coefficient, and μ_{low} is denoted as the low-field mobility in ref. [39]. However, it cannot directly be related to the low-field mobility κ from the DC model. Hence, μ_{low} is regarded as a fitting parameter. Nevertheless, this is uncritical since no value for μ_{low} needs to be provided. α_{c} characterizes the influence of a certain amount of trapped charges on the mobility. In the model, it will be regarded as a fitting parameter. In the next step, Eq. (5.43) is rearranged for μ_{eff}:

$$\mu_{\mathrm{eff}} = \frac{\mu_{\mathrm{low}}}{1 + \alpha_{\mathrm{c}} \cdot Q'_{\mathrm{t}} \cdot \mu_{\mathrm{low}}}. \tag{5.44}$$

Deriving μ_{eff} with respect to Q'_{t} leads to

$$\frac{\delta \mu_{\mathrm{eff}}}{\delta Q'_{\mathrm{t}}} = -\frac{\alpha_{\mathrm{c}} \cdot \mu_{\mathrm{low}}^2}{(1 + \alpha_{\mathrm{c}} \cdot Q'_{\mathrm{t}} \cdot \mu_{\mathrm{low}})^2} \tag{5.45}$$

where it can be observed that the right-hand side of Eq. (5.44) appears again. With this, Eq. (5.45) can be rewritten:

$$\frac{\delta \mu_{\mathrm{eff}}}{\delta Q'_{\mathrm{t}}} = -\alpha_{\mathrm{c}} \cdot \mu_{\mathrm{eff}}^2. \tag{5.46}$$

After these preparational steps, Eq. (5.42) is expanded by $\delta Q'_{\mathrm{t}}/\delta Q'_{\mathrm{t}}$:

$$\frac{\delta I_{\mathrm{D}}}{I_D} = \left(\frac{1}{Q'_{\mathrm{m}}} \cdot \frac{\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{t}}} + \frac{1}{\mu_{\mathrm{eff}}} \cdot \frac{\delta \mu_{\mathrm{eff}}}{\delta Q'_{\mathrm{t}}} \right) \cdot \delta Q'_{\mathrm{t}}. \tag{5.47}$$

Now, Eq. (5.46) is substituted in Eq. (5.47) which leads to

$$\frac{\delta I_{\mathrm{D}}}{I_D} = \left(\frac{1}{Q'_{\mathrm{m}}} \cdot \frac{\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{t}}} - \frac{1}{\mu_{\mathrm{eff}}} \cdot \alpha_{\mathrm{c}} \cdot \mu_{\mathrm{eff}}^2 \right) \cdot \delta Q'_{\mathrm{t}}$$

$$\frac{\delta I_{\mathrm{D}}}{I_D} = \left(\frac{1}{Q'_{\mathrm{m}}} \cdot \frac{\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{t}}} - \alpha_{\mathrm{c}} \cdot \mu_{\mathrm{eff}} \right) \cdot \delta Q'_{\mathrm{t}}. \tag{5.48}$$

In order to solve this equation, the change of the channel charge density due to a change in the trapped charge density has to be found. In ref. [39], the following thoughts lead to such an expression: It is assumed that a trapping action and accordingly a change in Q'_{t} induces a small variation $\delta \Psi_{\mathrm{s}}$ of the surface potential. Such a variation directly influences all other charges that directly depend on the surface potential. In ref. [39], the calculations are shown for a bulk MOSFET comprising a bulk terminal but here, the results for a three-terminal transistor are shown. According to the principle of charge conservation, the change in Q'_{t} will directly result in a change in the gate charge Q'_{g} and the channel charge Q'_{m}. The charge conversation principle reads as:

$$\delta Q'_{\mathrm{g}} + \delta Q'_{\mathrm{m}} = -\delta Q'_{\mathrm{t}}. \tag{5.49}$$

The changes in the gate and channel charges are now linked to the changes in the surface potential:

$$\delta Q'_{\mathrm{g}} = -C'_{\mathrm{diel}} \cdot \delta \Psi_{\mathrm{s}} \tag{5.50}$$

$$\delta Q'_{\mathrm{m}} = -C'_{\mathrm{ch}} \cdot \delta \Psi_{\mathrm{s}}, \tag{5.51}$$

where C'_{ch} is the channel charge capacitance. Next, the charge conservation equation (Eq. (5.49)) is rearranged:

$$\begin{aligned} -\frac{\delta Q'_{\mathrm{t}}}{\delta Q'_{\mathrm{m}}} &= \frac{\delta Q'_{\mathrm{g}}}{\delta Q'_{\mathrm{m}}} + 1 \\ \frac{\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{t}}} &= \frac{-1}{\frac{\delta Q'_{\mathrm{g}}}{\delta Q'_{\mathrm{m}}} + 1} \\ \frac{\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{t}}} &= \frac{-1}{\frac{\delta Q'_{\mathrm{g}}}{\delta Q'_{\mathrm{m}}} + \frac{\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{m}}}} \\ \frac{\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{t}}} &= \frac{-\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{g}} + \delta Q'_{\mathrm{m}}}. \end{aligned} \tag{5.52}$$

Now, Eqs. (5.50) and (5.51) are inserted in this equation, which leads to

$$\begin{aligned} \frac{\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{t}}} &= \frac{C'_{\mathrm{ch}} \cdot \delta \Psi_{\mathrm{s}}}{-C'_{\mathrm{diel}} \cdot \delta \Psi_{\mathrm{s}} - C'_{\mathrm{ch}} \cdot \delta \Psi_{\mathrm{s}}} \\ \frac{\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{t}}} &= \frac{C'_{\mathrm{ch}}}{-C'_{\mathrm{diel}} - C'_{\mathrm{ch}}} \end{aligned} \tag{5.53}$$

where now the minus sign is ignored by defining a factor R_{noise} as follows:

$$R_{\mathrm{noise}} = \left| \frac{\delta Q'_{\mathrm{m}}}{\delta Q'_{\mathrm{t}}} \right| = \frac{C'_{\mathrm{ch}}}{C'_{\mathrm{diel}} + C'_{\mathrm{ch}}}. \tag{5.54}$$

The next step is to find an expression for the channel charge capacitance C'_{ch}. In Chap. 4, a model for the total charges associated with the channel, the drain, and the source terminals is derived. In principle, the capacitance of the channel regarded as a whole can be expressed based on the total charge Q_{c} which could be derived with respect to the gate potential. However, this is not what is needed here. The channel charge capacitance rather describes the capacitive behavior of the channel at a certain position x in dependence on the surface potential Ψ_{s}. In order to come to the same expression as presented in ref. [39], the following thoughts are made: According to ref. [36], the density of quasi-mobile accumulation charges Q'_{m} is given by

$$Q'_{\mathrm{m}} = q \cdot d_{\mathrm{m}} \cdot N_{\mathrm{st}} \cdot \exp\left(\frac{q \cdot (\Psi_{\mathrm{s}} - V_{\mathrm{ch}}) - \frac{E_{\mathrm{g}}}{2}}{k_{\mathrm{B}} T} \right) \tag{5.55}$$

where d_{m} is the thickness of the accumulation channel, N_{st} is a fitting parameter, Ψ_{s} is the channel mid-gap potential representing the difference between the actual Fermi level and the mid of the bandgap, V_{ch} is the channel voltage, and E_{g} is the bandgap. Originally, the the channel-midgap potential is denoted as Φ_{c} in ref. [36] but it is in principle equal to the surface potential in ref. [39]. Therefore, these two quantities are treated equivalently. Deriving the charge density in Eq. (5.55) with respect to the surface potential leads to the channel charge capacitance:

$$C'_{\mathrm{ch}} = \frac{dQ'_{\mathrm{m}}}{d\Psi_{\mathrm{s}}} = \frac{q}{k_{\mathrm{B}}T} \cdot q \cdot d_{\mathrm{m}} \cdot N_{\mathrm{st}} \cdot \exp\left(\frac{q \cdot (\Psi_{\mathrm{s}} - V_{\mathrm{ch}}) - \frac{E_{\mathrm{g}}}{2}}{k_{\mathrm{B}}T}\right). \tag{5.56}$$

Due to the nature of the exponential function, the equation is nearly completely reproduced during the derivation and the only change is that the pre-factor of the surface potential appears now as a pre-factor of the whole equation. Thus, the following can be written:

$$C'_{\mathrm{ch}} = \frac{dQ'_{\mathrm{m}}}{d\Psi_{\mathrm{s}}} = \frac{q}{k_{\mathrm{B}}T} \cdot Q'_{\mathrm{m}}. \tag{5.57}$$

This result is now incorporated into the factor R_{noise} (Eq. (5.54)) which leads to:

$$R_{\mathrm{noise}} = \frac{\frac{q}{k_{\mathrm{B}}T} \cdot Q'_{\mathrm{m}}}{C'_{\mathrm{diel}} + \frac{q}{k_{\mathrm{B}}T} \cdot Q'_{\mathrm{m}}} = \frac{Q'_{\mathrm{m}}}{\frac{k_{\mathrm{B}}T}{q} \cdot C'_{\mathrm{diel}} + Q'_{\mathrm{m}}}. \tag{5.58}$$

Now, it is made use of the fact that $(k_{\mathrm{B}}T/q) \cdot C'_{\mathrm{diel}}$ is also contained in the specific charge according to Eq. (5.10). With this, the factor R_{noise} is rewritten as follows:

$$R_{\mathrm{noise}} = \frac{Q'_{\mathrm{m}}}{\frac{Q_{\mathrm{sp}}}{(\beta+1)\cdot\alpha} + Q'_{\mathrm{m}}} = \frac{\frac{Q'_{\mathrm{m}}}{Q_{\mathrm{sp}}}}{\frac{1}{(\beta+1)\cdot\alpha} + \frac{Q'_{\mathrm{m}}}{Q_{\mathrm{sp}}}} \tag{5.59}$$

where the fraction $Q'_{\mathrm{m}}/Q_{\mathrm{sp}}$ can be expressed as the normalized charge q_{m}:

$$R_{\mathrm{noise}} = \frac{q_{\mathrm{m}}}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}}. \tag{5.60}$$

Recalling that $R_{\mathrm{noise}} = |\delta Q'_{\mathrm{m}}/\delta Q'_{\mathrm{t}}|$, Eq. (5.60) can be inserted into Eq. (5.48):

$$\begin{aligned}
\frac{\delta I_{\mathrm{D}}}{I_D} &= \left(\frac{1}{Q'_{\mathrm{m}}} \cdot \frac{q_{\mathrm{m}}}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}} - \alpha_{\mathrm{c}} \cdot \mu_{\mathrm{eff}}\right) \cdot \delta Q'_{\mathrm{t}} \\
&= \left(\frac{1}{Q_{\mathrm{sp}} \cdot q_{\mathrm{m}}} \cdot \frac{q_{\mathrm{m}}}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}} - \alpha_{\mathrm{c}} \cdot \mu_{\mathrm{eff}}\right) \cdot \delta Q'_{\mathrm{t}} \\
&= \left(\frac{1}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}} + \alpha^{\star} \cdot \mu_{\mathrm{eff}}\right) \cdot \frac{\delta Q'_{\mathrm{t}}}{Q_{\mathrm{sp}}}
\end{aligned} \tag{5.61}$$

where $\alpha^{\star} = -Q_{\mathrm{sp}} \cdot \alpha_{\mathrm{c}}$. It shall be emphasized again that this equation provides information about the relative local fluctuation of the drain current in dependence on a change in the amount of trapped charge carriers which induces a correlated mobility fluctuation. For the next steps, rather than the relative fluctuation, the PSD of this local fluctuation is used. Since the local fluctuation of the drain current is equal to the noisy current δI_{n} which is depicted in Fig. 5.8 in the following δI_{n} will be used instead of δI_{D}. Following the principles in ref. [39], the current-normalized PSD of the relative local fluctuation can easily be obtained from Eq. (5.61) by squaring it and taking the PSD of $\delta Q_{\mathrm{t}}'$:

$$\frac{S_{\delta \mathrm{I}_\mathrm{n}^2}}{I_{\mathrm{ds}}^2} = \left(\frac{1}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}} + \alpha^{\star} \cdot \mu_{\mathrm{eff}} \right)^2 \cdot \frac{S_{\delta \mathrm{Q}_\mathrm{t}^2}}{Q_{\mathrm{sp}}^2}. \tag{5.62}$$

From theory, the PSD of the trapping charge density fluctuation is known. Charge carriers within the organic semiconductor can tunnel to traps in the gate dielectric and can be released again which causes the fluctuation of the carriers. The PSD expressed in terms of the charges and not in terms of the charge-carrier number reads as [39]:

$$S_{\delta \mathrm{Q}_\mathrm{t}^2} = \frac{k_{\mathrm{B}} \cdot T \cdot q^2 \cdot \lambda_{\mathrm{Tun}} \cdot N_{\mathrm{t}}'}{W_{\mathrm{ch,eff}} \cdot \Delta x \cdot (f/1\,\mathrm{Hz})^{\sigma} \cdot 1\,\mathrm{Hz}} \tag{5.63}$$

where λ_{Tun} is the tunneling attenuation distance, N_{t}' is the density of traps in the gate dielectric close to the interface to the OSC, and f is the frequency. Here, it becomes visible that the noise follows a $1/f^{\sigma}$ behavior. Please note that an exponent σ has been added to the frequency. The reason for this is that the measured PSD of a transistor may deviate from the ideal $1/f$ behavior which may be corrected by σ. This equation is now inserted into Eq. (5.62) which yields

$$\frac{S_{\delta \mathrm{I}_\mathrm{n}^2}}{I_{\mathrm{ds}}^2} = \left(\frac{1}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}} + \alpha^{\star} \cdot \mu_{\mathrm{eff}} \right)^2 \cdot \frac{1}{Q_{\mathrm{sp}}^2} \cdot \frac{k_{\mathrm{B}} \cdot T \cdot q^2 \cdot \lambda_{\mathrm{Tun}} \cdot N_{\mathrm{t}}'}{W_{\mathrm{ch,eff}} \cdot \Delta x \cdot (f/1\,\mathrm{Hz})^{\sigma} \cdot 1\,\mathrm{Hz}}. \tag{5.64}$$

Next, the PSD of the local fluctuation can be used in the long-channel simplification of the total noise of the drain current according to Eq. (5.39). For simplification purposes, this equation is presented here again:

$$S_{\Delta \mathrm{I}_\mathrm{nD}^2}(\omega) = \frac{1}{L_{\mathrm{ch}}^2} \cdot \int_0^{L_{\mathrm{ch}}} \Delta x \cdot S_{\delta \mathrm{I}_\mathrm{n}^2}(\omega, x) dx.$$

Now, both sides of this equation are divided by the drain current squared in order to represent the drain-current-normalized noise:

$$\frac{S_{\Delta \mathrm{I}_\mathrm{nD}^2}(\omega)}{I_{\mathrm{ds}}^2} = \frac{1}{L_{\mathrm{ch}}^2} \cdot \int_0^{L_{\mathrm{ch}}} \frac{\Delta x \cdot S_{\delta \mathrm{I}_\mathrm{n}^2}(\omega, x)}{I_{\mathrm{ds}}^2} dx. \tag{5.65}$$

Finally, the PSD of the local fluctuation (Eq. (5.64)) is inserted in this total PSD leading to:

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = \frac{1}{L^2_{\mathrm{ch}}} \cdot \int\limits_0^{L_{\mathrm{ch}}} \left(\frac{1}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}} + \alpha^\star \cdot \mu_{\mathrm{eff}} \right)^2 \cdot \frac{1}{Q^2_{\mathrm{sp}}} \cdot \frac{k_{\mathrm{B}} \cdot T \cdot q^2 \cdot \lambda_{\mathrm{Tun}} \cdot N'_{\mathrm{t}}}{W_{\mathrm{ch,eff}} \cdot (f/1\,\mathrm{Hz})^\sigma \cdot 1\,\mathrm{Hz}} dx. \quad (5.66)$$

Every factor that is independent of the position x is now factored out of the integral:

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = \frac{k_{\mathrm{B}} \cdot T \cdot q^2 \cdot \lambda_{\mathrm{Tun}} \cdot N'_{\mathrm{t}}}{Q^2_{\mathrm{sp}} \cdot W_{\mathrm{ch,eff}} \cdot L^2_{\mathrm{ch}} \cdot (f/1\,\mathrm{Hz})^\sigma \cdot 1\,\mathrm{Hz}} \cdot \int\limits_0^{L_{\mathrm{ch}}} \left(\frac{1}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}} + \alpha^\star \cdot \mu_{\mathrm{eff}} \right)^2 dx. \quad (5.67)$$

In order to improve the readability, a factor K_1 is defined:

$$K_1 = \frac{k_{\mathrm{B}} \cdot T \cdot q^2 \cdot \lambda_{\mathrm{Tun}} \cdot N'_{\mathrm{t}}}{Q^2_{\mathrm{sp}} \cdot W_{\mathrm{ch,eff}} \cdot L^2_{\mathrm{ch}} \cdot (f/1\,\mathrm{Hz})^\sigma \cdot 1\,\mathrm{Hz}} \quad (5.68)$$

and with this, Eq. (5.67) is written as

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = K_1 \cdot \int\limits_0^{L_{\mathrm{ch}}} \left(\frac{1}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}} + \alpha^\star \cdot \mu_{\mathrm{eff}} \right)^2 dx. \quad (5.69)$$

In order to solve this equation, the integration variable needs to be changed so that an integration over the charges rather than the channel length is conducted. A similar substitution is already incorporated for the modeling approach of the total charges in Eq. (4.7). This substitution approach is used again but instead of $\tilde{\alpha}$ the original α is taken. Furthermore, the de-coupling of the sub-threshold swing from the power-law mobility is included by multiplying α by $(\beta+1)$:

$$dx = -\frac{W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{I_{\mathrm{ds}}} \cdot \left((\beta+1) \cdot \alpha \cdot \frac{k_{\mathrm{B}} T}{q} + \frac{Q'_{\mathrm{m}}}{C'_{\mathrm{diel}}} \right) \cdot dQ'_{\mathrm{m}}. \quad (5.70)$$

However, before this equation can be used in the noise model the normalizations have to be performed:

$$dx = -\frac{W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{I_{\mathrm{sp}} \cdot i_{\mathrm{ds}}} \cdot \left((\beta+1) \cdot \alpha \cdot \frac{k_{\mathrm{B}} T}{q} + \frac{Q_{\mathrm{sp}} \cdot q_{\mathrm{m}}}{C'_{\mathrm{diel}}} \right) \cdot Q_{\mathrm{sp}} \cdot dq_{\mathrm{m}} \quad (5.71)$$

where the definitions of Q_{sp} and I_{sp} are inserted according to Eq. (5.10) and Eq. (5.14), respectively:

$$dx = -\frac{W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{\mu_{\mathrm{eff}} \cdot (\beta+1)^2 \cdot \alpha^2 \cdot \left(\frac{k_{\mathrm{B}} T}{q}\right)^2 \cdot C'_{\mathrm{diel}} \frac{W_{\mathrm{ch,eff}}}{L_{\mathrm{ch}}} \cdot i_{\mathrm{ds}}} \times \left((\beta+1)\,\alpha \cdot \frac{k_{\mathrm{B}} T}{q} + \frac{(\beta+1) \cdot \alpha \cdot \frac{k_{\mathrm{B}} T}{q} \cdot C'_{\mathrm{diel}} \cdot q_{\mathrm{m}}}{C'_{\mathrm{diel}}} \right) \cdot (\beta+1) \cdot \alpha \cdot \frac{k_{\mathrm{B}} T}{q} \cdot C'_{\mathrm{diel}} \cdot dq_{\mathrm{m}} \quad (5.72)$$

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which after several simplification steps leads to

$$dx = -\frac{L_{\mathrm{ch}}}{i_{\mathrm{ds}}} \cdot (1 + q_{\mathrm{m}}) \cdot dq_{\mathrm{m}}. \tag{5.73}$$

This equation is now substituted in Eq. (5.69) and the limits of integration are changed to q_{s} and q_{d} so that a charge-based integral results:

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = -K_1 \cdot \int_{q_{\mathrm{s}}}^{q_{\mathrm{d}}} \left(\frac{1}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}} + \alpha^\star \cdot \mu_{\mathrm{eff}} \right)^2 \cdot \frac{L_{\mathrm{ch}}}{i_{\mathrm{ds}}} \cdot (1 + q_{\mathrm{m}}) \cdot dq_{\mathrm{m}}. \tag{5.74}$$

A factor K_2 is defined in order to again improve the readability:

$$K_2 = -L_{\mathrm{ch}} \cdot K_1 = -\frac{k_{\mathrm{B}} \cdot T \cdot q^2 \cdot \lambda_{\mathrm{Tun}} \cdot N'_{\mathrm{t}}}{Q^2_{\mathrm{sp}} \cdot W_{\mathrm{ch,eff}} \cdot L_{\mathrm{ch}} \cdot (f/1\,\mathrm{Hz})^\sigma \cdot 1\,\mathrm{Hz}} \tag{5.75}$$

which then allows for a slightly easier way of writing Eq. (5.74):

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = \frac{K_2}{i_{\mathrm{ds}}} \cdot \int_{q_{\mathrm{s}}}^{q_{\mathrm{d}}} \left(\frac{1}{\frac{1}{(\beta+1)\cdot\alpha} + q_{\mathrm{m}}} + \alpha^\star \cdot \mu_{\mathrm{eff}} \right)^2 \cdot (1 + q_{\mathrm{m}}) \cdot dq_{\mathrm{m}}. \tag{5.76}$$

Carrying out the integration using Wolfram Alpha [86] leads to:

$$\begin{aligned}\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} =& \frac{K_2}{i_{\mathrm{ds}}} \cdot \left(\left(1 + \frac{2 \cdot \alpha^\star \cdot \mu_{\mathrm{eff}} \cdot ((\beta+1)\cdot\alpha - 1)}{(\beta+1)\cdot\alpha} \right) \cdot \ln\left(\frac{1 + (\beta+1)\cdot\alpha\cdot q_{\mathrm{d}}}{1 + (\beta+1)\cdot\alpha\cdot q_{\mathrm{s}}} \right) \right. \\ &+ (1 - (\beta+1)\cdot\alpha) \cdot \left(\frac{1}{1 + (\beta+1)\cdot\alpha\cdot q_{\mathrm{d}}} - \frac{1}{1 + (\beta+1)\cdot\alpha\cdot q_{\mathrm{s}}} \right) \\ &\left. + \frac{1}{2} \cdot (\alpha^\star \cdot \mu_{\mathrm{eff}})^2 \cdot \left(q^2_{\mathrm{d}} + 2 \cdot q_{\mathrm{d}} - q^2_{\mathrm{s}} - 2 \cdot q_{\mathrm{s}} \right) + 2 \cdot \alpha^\star \cdot \mu_{\mathrm{eff}} \cdot (q_{\mathrm{d}} - q_{\mathrm{s}}) \right). \end{aligned} \tag{5.77}$$

Please note that in this equation, α and $\alpha^\star$ appear. These two quantities may not be confused with each other. α is the slope degradation factor with respect to an ideal slope of $\approx 60\,\mathrm{mV/dec}$ at room temperature while $\alpha^\star = -Q_{\mathrm{sp}} \cdot \alpha_{\mathrm{c}}$ is a parameter related to the Coulomb scattering coefficient. The benefit of Eq. (5.77) is that it is a fully charge-based model incorporating only a small number of fitting parameters.

5.4.4 Modeling of Bulk Mobility Fluctuations

In Sec. 5.3, it has been revealed that the dominant noise mechanism in the transistors under investigation is the fluctuation of the charge-carrier number. However, in order to provide a full picture, a model describing the bulk mobility fluctuations of organic TFTs is derived, as well. The starting point for the compact model is the same as for the model of the charge-carrier-number fluctuations: the integral that sums up the contributions of the local noise sources along the channel incorporating the long-channel simplification. This equation is Eq. (5.39)

but divided by the drain current squared which leads to Eq. (5.65). For a better readability of this work, this equation is presented here again:

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = \frac{1}{L^2_{\mathrm{ch}}} \cdot \int_0^{L_{\mathrm{ch}}} \frac{\Delta x \cdot S_{\delta \mathrm{I}^2_{\mathrm{n}}}(\omega, x)}{I^2_{\mathrm{ds}}} dx. \tag{5.78}$$

The difference between the carrier-number fluctuation model and the fluctuation of the bulk mobility is the PSD of the local noise sources. Whereas in the carrier-number fluctuation model, the local PSD was derived based on the trapping and de-trapping of charge carriers inducing a correlated mobility fluctuation in the bulk-mobility fluctuation model, the local PSD is given by the empirical Hooge model [39]:

$$\frac{S_{\delta \mathrm{I}^2_{\mathrm{n}}}}{I^2_{\mathrm{ds}}} = \frac{\alpha_{\mathrm{H}} \cdot q}{W_{\mathrm{ch,eff}} \cdot \Delta x \cdot Q'_{\mathrm{m}}(x) \cdot (f/1\,\mathrm{Hz})^{\sigma} \cdot 1\,\mathrm{Hz}} \tag{5.79}$$

where α_{H} is the empirical Hooge parameter. Originally, the frequency is only contained with an exponent of $\sigma = 1$ but in order to reproduce the results of measured devices which may exhibit frequency slopes slightly different from unity, σ is defined as a fitting parameter. The local PSD is now inserted into Eq. (5.78) which leads to:

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = \frac{1}{L^2_{\mathrm{ch}}} \cdot \int_0^{L_{\mathrm{ch}}} \frac{\Delta x \cdot \alpha_{\mathrm{H}} \cdot q}{W_{\mathrm{ch,eff}} \cdot \Delta x \cdot Q'_{\mathrm{m}}(x) \cdot (f/1\,\mathrm{Hz})^{\sigma} \cdot 1\,\mathrm{Hz}} \tag{5.80}$$

which can be rearranged to

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = \frac{\alpha_{\mathrm{H}} \cdot q}{L^2_{\mathrm{ch}} \cdot W_{\mathrm{ch,eff}} \cdot (f/1\,\mathrm{Hz})^{\sigma} \cdot 1\,\mathrm{Hz}} \cdot \int_0^{L_{\mathrm{ch}}} \frac{1}{Q'_{\mathrm{m}}(x)} dx. \tag{5.81}$$

Now, the same procedure as for the carrier-number fluctuations is used: The charge density $Q'_{\mathrm{m}}(x)$ is normalized according to Eq. (5.11) and the integration variable is changed to q_{m} by applying the substitution according to Eq. (5.73) which leads to:

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = \frac{\alpha_{\mathrm{H}} \cdot q}{L^2_{\mathrm{ch}} \cdot W_{\mathrm{ch,eff}} \cdot (f/1\,\mathrm{Hz})^{\sigma} \cdot 1\,\mathrm{Hz}} \cdot \int_{q_{\mathrm{s}}}^{q_{\mathrm{d}}} \frac{1}{q_{\mathrm{m}} \cdot Q_{\mathrm{sp}}} \cdot \frac{-L_{\mathrm{ch}}}{i_{\mathrm{ds}}} \cdot (1 + q_{\mathrm{m}})\, dq_{\mathrm{m}}. \tag{5.82}$$

After some rearrangements, this leads to:

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = -\frac{\alpha_{\mathrm{H}} \cdot q}{L_{\mathrm{ch}} \cdot W_{\mathrm{ch,eff}} \cdot (f/1\,\mathrm{Hz})^{\sigma} \cdot 1\,\mathrm{Hz} \cdot Q_{\mathrm{sp}}} \cdot \frac{1}{i_{\mathrm{ds}}} \cdot \int_{q_{\mathrm{s}}}^{q_{\mathrm{d}}} \left(\frac{1}{q_{\mathrm{m}}} + 1 \right) dq_{\mathrm{m}}. \tag{5.83}$$

In order to improve the readability of this equation, a factor K_3 is defined as follows:

$$K_3 = -\frac{\alpha_{\mathrm{H}} \cdot q}{L_{\mathrm{ch}} \cdot W_{\mathrm{ch,eff}} \cdot (f/1\,\mathrm{Hz})^{\sigma} \cdot 1\,\mathrm{Hz} \cdot Q_{\mathrm{sp}}}. \tag{5.84}$$

With this definition and after carrying out the simple integration in Eq. (5.83), the final result is obtained:

$$\frac{S_{\Delta \mathrm{I}^2_{\mathrm{nD}}}(\omega)}{I^2_{\mathrm{ds}}} = \frac{K_3}{i_{\mathrm{ds}}} \cdot \left(\ln\left(\frac{q_{\mathrm{d}}}{q_{\mathrm{s}}}\right) + q_{\mathrm{d}} - q_{\mathrm{s}} \right). \tag{5.85}$$

CHAPTER 6

Model Verification and Discussion

6.1 Introductory Information

This chapter is dedicated to the verification of the models presented in the previous chapters. The chapter is organized as follows: First, the extension to the DC model incorporating fringe currents is verified for staggered transistors by means of a TCAD Sentaurus simulation. Subsequently, the quasistatic capacitance models are verified with respect to TCAD Sentaurus simulations and measurements of staggered long-channel transistors. The next step is the verification of a simple circuit simulation of staggered transistors incorporating the quasistatic capacitance model. After the verification of the staggered geometry, coplanar transistors are investigated. For this architecture, only TCAD simulations of the quasistatic capacitances are available.

During the verification, several issues of the compact model will be revealed: the equations presented so far are only valid for a quasistatic operation of the model and furthermore, transistors with high contact resistances (which are the transistors comprising shorter channel lengths) cannot be described properly by the model. This will eventually lead to extensions of the model which will be explained and verified in Chap. 7.

The last step of this chapter is the verification of the noise model. The compact model will be verified with respect to measurements an TCAD simulation results.

6.2 Fringe Current Model

In this section, the fringe current model presented in Chap. 2 is verified by means of a TCAD Sentaurus simulation. To start with, the TCAD simulation setup is introduced. Different transistors were simulated and their corresponding parameters are listed in Tab. 6.1 where χ_{osc} is the electron affinity of the organic semiconductor, E_{g} is the band gap of the organic

Table 6.1.: Parameters of TCAD simulations of staggered transistors. Column (a) corresponds to the 2D simulation of a staggered OTFT using a standard square-root DOS. Column (b) corresponds to the 2D simulation of a staggered OTFT using a Gaussian DOS. Column (c) corresponds to a 3D simulation of a staggered OTFT consisting of one source/drain finger. Column (d) corresponds to a 3D simulation of a staggered OTFT consisting of two source/drain fingers.

TCAD Param.	(a) 2D sqrt.	(b) 2D Gauss.	(c) 3D single	(d) 3D double
χ_{osc} [eV]	1.81	1.81	1.81	1.81
E_{g} [eV]	3.38	3.38	3.38	3.38
μ_{n} [cm^2 V^{-1} s^{-1}]	1	1	1e-10	1e-10
μ_{p} [cm^2 V^{-1} s^{-1}]	1	1	1	1
$\varepsilon_{\mathrm{r,osc}}$ [−]	3	3	3	3
$\varepsilon_{\mathrm{r,diel}}$ [−]	3.9	3.9	3.9	3.9
$\Phi_{\mathrm{m,g}}$ [eV]	4.1	4.1	4.1	4.1
$\Phi_{\mathrm{m,sd}}$ [eV]	5.19	5.19	5	5
L_{ch} [µm]	200	200	20	20
W_{contact} [µm]	1	1	1	1
$L_{\mathrm{ov,GS}}$ [µm]	10	10	5	5
$L_{\mathrm{ov,GD}}$ [µm]	10	10	5	5
t_{diel} [nm]	5.3	5.3	5.3	5.3
t_{osc} [nm]	25	25	25	25
w_{ovl} [µm]	0	0	variable	variable
N_{fing} [−]	1	1	1	2
d_{fing} [µm]	-	-	-	variable

semiconductor, μ_{n} and μ_{p} are the mobilities for electrons and holes, $\varepsilon_{\mathrm{r,osc}}$ is the relative dielectric permittivity of the depleted organic semiconductor, $\varepsilon_{\mathrm{r,diel}}$ is the relative dielectric permittivity of the gate dielectric, $\Phi_{\mathrm{m,g}}$ is the work function of the gate metal, $\Phi_{\mathrm{m,sd}}$ is the work function of the source/drain electrode metal, L_{ch} is the channel length, W_{contact} is the width of one source/drain contact, $L_{\mathrm{ov,GS}}$ and $L_{\mathrm{ov,GD}}$ are the gate-to-source and gate-to-drain overlap lengths, t_{diel} is the gate dielectric thickness, t_{osc} is the thickness of the organic-semiconductor layer, w_{ovl} is the fringe width beyond the first and the last finger in case of a 3D simulation, N_{fing} is the number of parallel source/drain fingers, and d_{fing} is the distance between two fingers.

In order to simulate the fringe effects, a 3D simulation was necessary. Such a simulation imposes a high computational load on the computer on which the simulation is executed and the probability of getting convergent results is smaller than for a 2D simulation. Therefore, the simulation was kept as simple as possible. As explained in Chap. 2, DOS in organic semiconductors is assumed to be Gaussian-shaped. However, it turned out that setting up a Gaussian DOS for a 3D simulation leads to a quite unstable behavior of the simulator. Therefore, a standard square-root DOS is assumed. In Fig. 6.1, the simulated transfer curves

of three 2D simulations are shown where one simulation exhibits a standard square-root DOS and the other two exhibit Gaussian densities of states with different standard deviations and shifts of the center position of the DOS. Apart from the differences in the DOS, the three 2D simulations use the same simulation setup as listed in Tab. 6.1. It can be seen that for high absolute values of V_{gs} the three curves look very similar. However, the steepnesses of

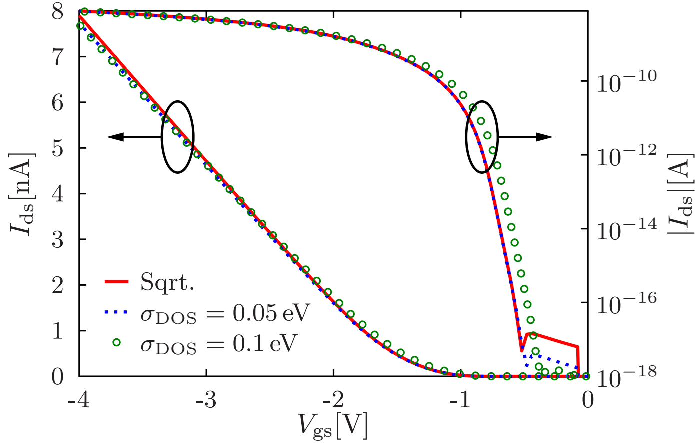


Figure 6.1.: Transfer curves of a staggered OTFT as simulated by Sentaurus TCAD at $V_{ds} = -1$ V. All important settings of the simulations are equal and listed in Tab. 6.1. The only difference is that for one transistor a standard square-root DOS with an effective hole density of $N_v = 1 \times 10^{21}$ cm^{-3} has been used (solid red line) whereas for the other transistors, Gaussian-distributed densities of states with different standard deviations are assumed. The total number of $N_{t,DOS} = 1 \times 10^{21}$ cm^{-3} is equal for both transistors. A standard deviation of $\sigma_{DOS} = 0.05$ eV, and a center position of $E_{0,DOS} = E_V - 0.05$ eV is used (blue dotted line). For the other transistor, a standard deviation of $\sigma_{DOS} = 0.1$ eV, and a center position of $E_{0,DOS} = E_V - 0.1$ eV i used (green circles). The currents are plotted both in linear and logarithmic scale. For high absolute values of V_{gs}, the curves are very similar except for slightly different steepnesses. For V_{gs} values close to zero, the curve where σ_{DOS} is large exhibits a longer transition from the sub-threshold to the above-threshold regime.

the curves becomes slightly smaller for higher σ_{DOS}. The differences between the curves are more pronounced in the transition regime from sub-threshold to above-threshold. Whereas the simulation with $\sigma_{DOS} = 0.05$ eV is almost perfectly aligned with the simulation using a standard square-root DOS, the curve with $\sigma_{DOS} = 0.1$ eV deviates from that. It seems as if the threshold voltage of the curve is shifted closer to zero. However, this is in contradiction to the fact that in the above-threshold regime the curve is almost aligned with the other two curves. An extraction of the threshold voltage based on the on-state current would not lead to such a pronounced shift as the curves exhibit in the sub-threshold regime. The DC compact model can also be used to fit the simulation with $\sigma_{DOS} = 0.1$ eV by assuming a threshold voltage such that the sub-threshold curves match and then adjusting the on-state characteristics using the power-law mobility model. Based on these observations, the usage of a square-root DOS for the complex 3D simulations is justified because the basic results will not be diminished by this assumption. Furthermore, in the literature it is described that organic transistors with

long channels often adhere to a more crystalline-like behavior which effectively means that the exponent of the power-law mobility can be set to values close to zero [28]. Thus, for the verification of long-channel transistors, the influence of the Gaussian DOS on the current-voltage characteristics will be of minor importance.

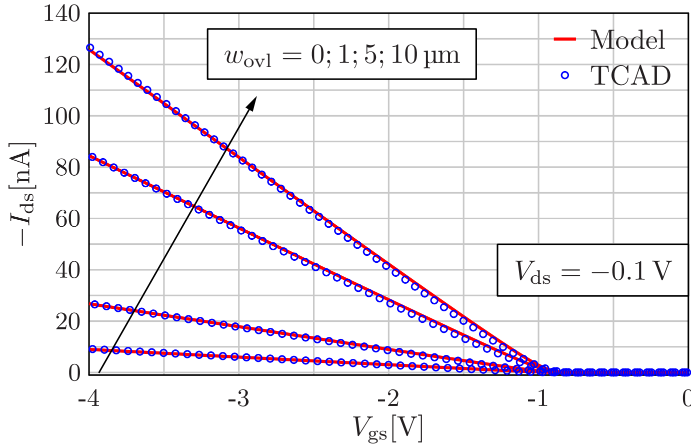


Figure 6.2.: Transfer curves of a staggered OTFT as simulated in a 3D simulation by Sentaurus TCAD at $V_{ds} = -0.1\,V$ (blue symbols) in comparison to the compact model (solid red lines). The transistor consists of one source/drain finger and a varying overlap width w_{ovl} beyond the finger. The compact model is fitted to the different overlap widths only by a variation of δ_{fit}. The parameters of the simulation are listed in column (c) of Tab. 6.1. The mobility in the compact model is set to $\kappa = 0.93\,cm^2V^{-\beta-1}s^{-1}$ with $\beta = 0$. This picture was published in ref. [54] and was slightly modified.

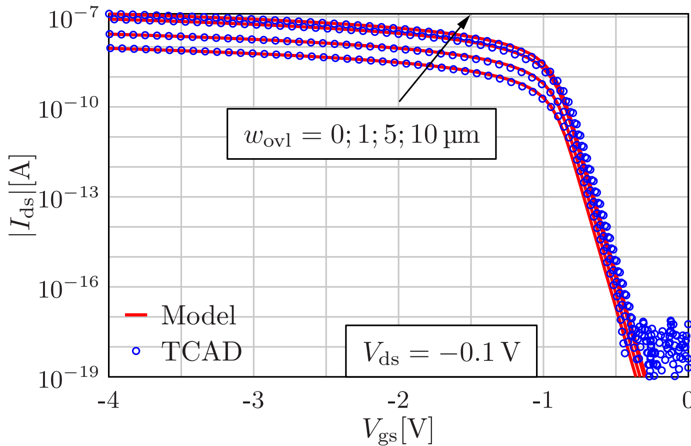


Figure 6.3.: Transfer curves of a staggered OTFT as simulated in a 3D simulation by Sentaurus TCAD at $V_{ds} = -0.1\,V$ (blue symbols) in comparison to the compact model (solid red lines). This figure shows the same as Fig. 6.2 but the current is plotted in logarithmic scale.

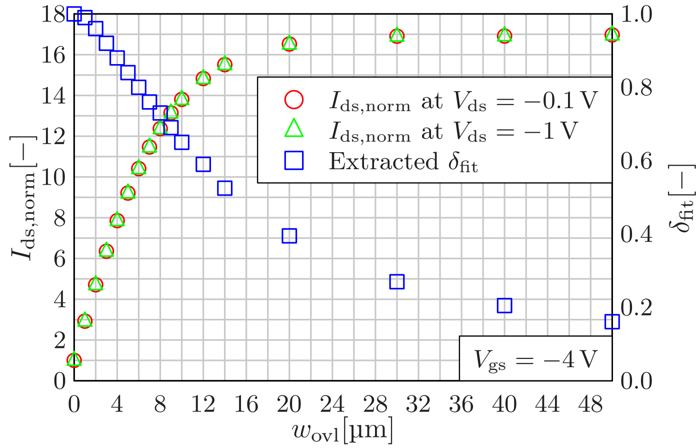


Figure 6.4.: Drain current of a staggered OTFT as simulated in a 3D simulation by Sentaurus TCAD at $V_{\text{ds}} = -0.1\,\text{V}$ (red circles) and at $V_{\text{ds}} = -1\,\text{V}$ (green triangles). In every simulation, $V_{\text{gs}} = -4\,\text{V}$. The transistor consists of one source/drain finger and a varying overlap width w_{ovl} beyond the finger. The current is normalized with respect to the current of a transistor with $w_{\text{ovl}} = 0\,\mu\text{m}$ for each of the two drain-source voltages. For each w_{ovl}, a value for the fitting parameter δ_{fit} is determined by the compact model. These extracted values are plotted (blue squares). Since δ_{fit} is bias-independent the same values for both drain-source voltages are valid. The parameters of the simulation are listed in column (c) of Tab. 6.1. This figure was published in ref. [54] and was slightly modified.

After this evaluation, it will be proceeded with the fringe current model. Due to the massive amount of time that the 3D simulations need only transfer curves have been simulated. The fringe current model was investigated by means of the following simulations: A transistor with one finger of width W_{contact} comprising a variable fringe width w_{ovl} ranging between $0\,\mu\text{m}$ and $50\,\mu\text{m}$ was simulated. This fringe width is symmetrically present to both sides of the source/drain finger. The fitting process is conducted as follows:

1. The DC model is fitted to the transistor where $w_{\text{ovl}} = 0\,\mu\text{m}$. From this, the mobility, the threshold voltage and the sub-threshold swing are extracted.

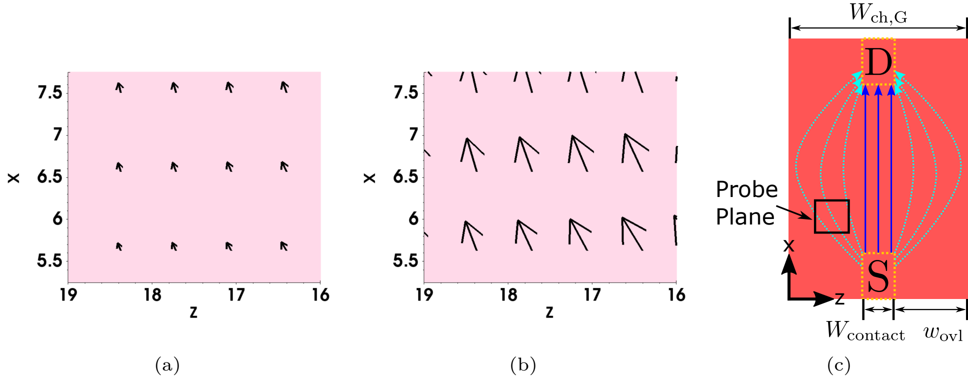
2. A simulation where $w_{\text{ovl}} \neq 0\,\mu\text{m}$ is taken. The correct w_{ovl} is entered in the model parameters while all other fitting parameters are kept to the values extracted in point 1. Only the fitting parameter δ_{fit} is used in order to manually adjust the current so that model and simulation agree.

3. Step 2 is repeated for every simulated w_{ovl} and the resulting values are noted down.

As explained in Chap. 2, the fringe model is an empirical approach. The consequence is that the parameter δ_{fit} cannot be calculated analytically but serves as a fitting parameter. There might arise the question why such a model is used whereas the effect of the fringe currents could simply be captured by a higher mobility such as described in ref. [60]. The reason why the fringe current model is used is that the parameter δ_{fit} does not have an influence on the model for the total charges and capacitances, as explained in Chap. 4. However, the exact geometry of the transistor consisting of all intrinsic channel regions and extrinsic regions is necessary. This information would be lost if the fringe regions were ignored in the model equations. In Fig. 6.2, the compact model is shown in comparison to the results of a 3D TCAD simulation of a transistor comprising one source/drain finger with varying fringe widths w_{ovl}. Figure 6.3 shows the same but here the current is plotted in logarithmic scale. The compact model is fitted according to the procedure explained above by only adjusting the fitting parameter δ_{fit} in order to capture the current for the different fringe widths.

As can be seen in Figs. 6.2 and 6.3, the empirical model agrees well with the TCAD simulations. This proves that the model assumption of an effective channel width $W_{\text{ch,eff}}$ is sufficient to capture the effect of current spreading. Please note that in the TCAD simulation setup a small Schottky barrier between the source electrode and the organic semiconductor is present. The effect of a Schottky barrier lowering is not taken into account in the simulation. Hence, the reversely operated Schottky barrier at the source behaves similar as an Ohmic contact resistance. This contact resistance is the reason why the mobility in the compact model is set to a value which is slightly smaller than the value which is set in the TCAD simulation.

Figure 6.4 shows the drain currents of the 3D TCAD simulation of the staggered single-finger OTFT versus the overlap width w_{ovl}. The currents are probed at one gate-source voltage and at two drain-source voltages. Furthermore, the current is normalized with respect to the current of a transistor without any fringe regions ($w_{\text{ovl}} = 0\,\mu\text{m}$) at each of the two drain-source voltages. It is clearly visible that the current spreading is independent of the chosen drain-source voltage since in both cases the normalized current is the same. Furthermore, the plot shows the extracted δ_{fit} which is needed in order to fit the compact model to the simulated data. Since the current spreading is independent of the drain-source voltages, δ_{fit} is the same for both V_{ds}. Furthermore, it can be verified that the current spreading is also independent of the gate-source voltage. In Fig. 6.5, the current vectors of a 3D staggered transistor are shown in a fringe region for two different gate-source voltages. The current vectors are probed in a cutplane in the organic semiconductor close to the gate-dielectric interface, as indicated in Fig. 6.5(c). It can be seen that due to the increased gate-source voltage the length of the current vectors increases which results in a higher current (as usual when V_{gs} is increased). However, the direction of the vectors is not altered due to the higher voltage. This proves that the paths that charge carriers travel in the fringe region are independent of the gate-source voltage. From the observations presented so far, it can be concluded that the current spreading is entirely bias-independent.



(a) (b) (c)

Figure 6.5.: Electric field vectors in a fringe region in a small cutplane close to the interface between OSC and the gate dielectric of a single-finger staggered OTFT. The simulation has been carried out with Sentaurus TCAD. The parameters of the simulation are listed in column (c) of Tab. 6.1. (a) $V_{\text{gs}} = -1.333\,\text{V}$ and (b) $V_{\text{gs}} = -4\,\text{V}$. The drain voltage is $V_{\text{ds}} = -1\,\text{V}$ in (a) and (b). In (c), the location of the probed cutplane is depicted. For both gate voltages, the arrows point in the same directions but their lengths are different. This shows that a higher gate bias does not influence the orientation of the field lines. The two pictures in (a) and (b) were published in ref. [54].

The verification presented so far only covers transistors comprising one single source/drain finger and fringe regions next to this finger. However, in the fringe model presented in Chap. 2, it is postulated that the model is also applicable to multi-finger transistors. In Fig. 6.6, the results of a 3D TCAD simulation of a staggered transistor comprising two source/drain fingers are shown. The current is normalized with respect to a transistor with no distance between the fingers ($d_{\text{fing}} = 0\,\mu\text{m}$) and no fringe regions beyond the first and the last finger ($w_{\text{ovl}} = 0\,\mu\text{m}$). Just as for the transistor comprising one single finger, the compact model is fitted to the TCAD simulation of this two-finger transistor by only adapting the parameter δ_{fit}. The extracted values for δ_{fit} are also plotted. By comparing Fig. 6.6 to Fig. 6.4, it can be seen that the two-finger transistor behaves similarly as the single-finger transistor.

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Jakob Simon Leise

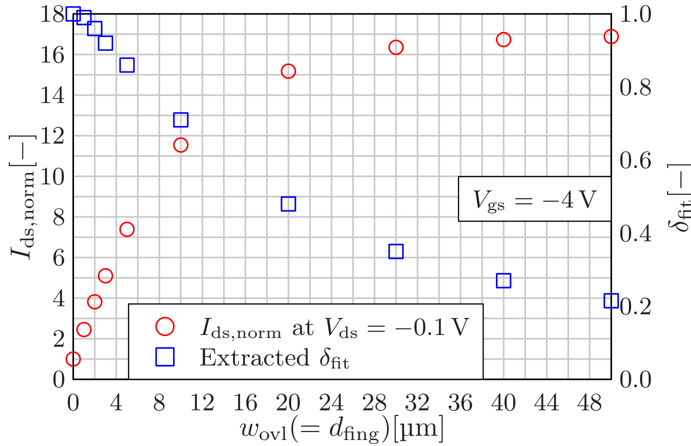

Figure 6.6.: Drain current of a staggered OTFT as simulated in a 3D simulation by Sentaurus TCAD at the operation point $V_{ds} = -0.1$ V and $V_{gs} = -4$ V. The current is normalized with respect to the current of a transistor with $w_{ovl} = d_{fing} = 0\,\mu m$. The transistor consists of two source/drain fingers with a varying distance d_{fing} between the fingers and a varying overlap width w_{ovl} beyond the first finger and the last finger. d_{fing} and w_{ovl} are varied simultaneously in this simulation. For each w_{ovl}, a value for the fitting parameter δ_{fit} is determined by the compact model. These extracted values are plotted (blue squares). The parameters of the simulation are listed in column (d) of Tab. 6.1. This picture was published in ref. [54] and was slightly modified.

6.3 Quasistatic Capacitances

6.3.1 Introductory Information

In this section, the quasistatic capacitance model is verified with respect to both coplanar and staggered architectures. The staggered transistors are verified by the measured quasistatic capacitances presented by Zaki et al. in ref. [40] and by Sentaurus TCAD simulation results. For the verification of the coplanar architecture, only simulations are available. In Chap. 4, a compact model for the calculation of the total charges in organic transistors is presented. More precisely speaking, the model analytically calculates the total amount of charge Q_c which is stored in the channel region of the transistor and it applies the Ward-Dutton partitioning scheme [65] allowing for a calculation of the charges Q_s and Q_d which are under control by the source and drain terminal, respectively. Furthermore, the charges which are stored in the gate-to-contact overlap regions and fringe areas are calculated and added to the corresponding intrinsic charges. However, when transistors are characterized, usually the capacitances are measured and plotted [38]. In principle, the equations for the total charges (Eqs. (A.1), (A.2), and (A.3) in the Appendix) could be derived with respect to the terminal voltages. However, the results would be rather large equations. Furthermore, for an implementation in the hardware description language Verilog-A, only equations for the total charges are needed. Therefore, the analytical derivation of the charge equations with respect to the voltages is circumvented by a

numerical approximation of the capacitances. Please recall that the capacitance C_{ij} where i,j represent the drain, source, or gate terminals can be calculated according to Eq. (3.16) as

$$C_{\mathrm{ij}} = \begin{cases} -\frac{\partial Q_{\mathrm{i}}}{\partial V_{\mathrm{j}}} & i \neq j \quad i,j = g,s,d \\ \frac{\partial Q_{\mathrm{i}}}{\partial V_{\mathrm{j}}}, & i = j \end{cases} . \tag{6.1}$$

If, for example, the capacitance C_{sg} has to be calculated, it is defined as

$$C_{\mathrm{sg}} = -\frac{\partial Q_{\mathrm{s}}}{\partial V_{\mathrm{g}}}. \tag{6.2}$$

The charge Q_{s} is dependent on the three terminal potentials V_{g}, V_{s} and V_{d}. As a numerical approximation, the gate potential is altered by a certain amount around its DC value and the source charge is calculated in both cases. Then, the difference of these charges is divided by the voltage change:

$$C_{\mathrm{sg}} \approx -\frac{Q_{\mathrm{s}}(V_{\mathrm{g}} + 0.5 \cdot \Delta V_{\mathrm{cap}}, V_{\mathrm{s}}, V_{\mathrm{d}}) - Q_{\mathrm{s}}(V_{\mathrm{g}} - 0.5 \cdot \Delta V_{\mathrm{cap}}, V_{\mathrm{s}}, V_{\mathrm{d}})}{\Delta V_{\mathrm{cap}}}. \tag{6.3}$$

Provided that ΔV_{cap} is sufficiently small (e.g. 1 mV), this approximation is very precise. For the verification of the compact model, this procedure is used in order to calculate the nine capacitances.

6.3.2 Staggered Transistors

In this section, the verification for staggered transistors is presented. Since the quasistatic charge and capacitance model is dependent on the underlying compact DC model, the first step is a fitting of the DC curves. Subsequently, the capacitances can be verified without the need of tuning other parameters. The model will be verified with respect to TCAD simulation data and measurements. In this section, only long-channel transistors with negligible contact resistances are regarded.

6.3.2.1 TCAD Simulations

2D and 3D Sentaurus TCAD simulations were conducted for transistors with different geometries. In order to obtain quasistatic capacitances, the frequency of the AC analysis was set to a very low value of $f = 0.01$ Hz.

2D simulation with a long channel

First, the fitting of the DC model is shown. In Fig. 6.7, the transfer curves as a result of a 2D TCAD simulation of a long-channel transistor ($L_{\mathrm{ch}} = 200$ µm) are compared to the compact model. The parameters of the TCAD simulation setup and the chosen parameter values for the compact model are listed in column (a) of Tab. 6.2. Figure 6.8 shows the corresponding transconductances of the same simulation. Finally, Fig. 6.9 shows the output curves of the

Table 6.2.: Parameters of TCAD simulations of staggered OTFTs and fitting parameters of the compact model. (a) 2D simulation of a long-channel transistor. (b) 2D simulation of a transistor with a shorter channel. (c) 3D simulation of a transistor comprising one source/drain electrode. (d) 3D simulation of a transistor consisting of two drain/source electrodes. For (a) and (b), a Gaussian DOS with a total number of $N_{\mathrm{t,DOS}} = 1 \times 10^{21}\,\mathrm{cm}^{-3}$, a standard deviation of $\sigma_{\mathrm{DOS}} = 0.05\,\mathrm{eV}$, and a center position of $E_{0,\mathrm{DOS}} = E_{\mathrm{V}} - 0.05\,\mathrm{eV}$ is used. For (c) and (d), a square-root DOS with an effective hole density of $N_{\mathrm{v}} = 1 \times 10^{21}\,\mathrm{cm}^{-3}$ is used.

TCAD Param.	(a) 2D long	(b) 2D short	(c) 3D single	(d) 3D double
χ_{osc} [eV]	1.81	1.81	1.81	1.81
E_{g} [eV]	3.38	3.38	3.38	3.38
μ_{n} [cm^2 V^{-1} s^{-1}]	1	1	1e-10	1e-10
μ_{p} [cm^2 V^{-1} s^{-1}]	1	1	1	1
$\varepsilon_{\mathrm{r,osc}}$ [−]	3	3	3	3
$\varepsilon_{\mathrm{r,diel}}$ [−]	3.9	3.9	3.9	3.9
$\Phi_{\mathrm{m,g}}$ [eV]	4.1	4.1	4.1	4.1
$\Phi_{\mathrm{m,sd}}$ [eV]	5.19	5.19	5	5
L_{ch} [µm]	200	20	20	20
W_{contact} [µm]	1	1	1	1
$L_{\mathrm{ov,GS}}$ [µm]	10	10	5	5
$L_{\mathrm{ov,GD}}$ [µm]	10	10	5	5
t_{diel} [nm]	5.3	5.3	5.3	5.3
t_{osc} [nm]	25	25	25	25
w_{ovl} [µm]	0	0	variable	variable
N_{fing} [−]	1	1	1	2
d_{fing} [µm]	-	-	-	variable
Compact Param.				
S_{obs} [mV/dec]	60	60	60	60
V_{T0} [V]	-0.86	-0.86	-0.86	-0.86
κ [cm^{2}V$^{-\beta-1}$s^{-1}]	0.9	0.91	0.93	0.93
β [−]	0.035	0.04	0	0
λ [V^{-1}]	0	8e-3	0	0

same simulation. As can be seen, the overall agreement is good which was to be expected since the transistor has a long channel and the basic DC model in ref. [36] is proven to reproduce the characteristics of long-channel transistors with good accuracy.

Figures 6.10, 6.11 and 6.12 show the results of the quasistatic capacitances. Again, the TCAD simulation is compared to the compact model. The capacitances are numerically calculated in the compact model using a voltage difference of $\Delta V_{\mathrm{cap}} = 1\,\mathrm{mV}$. The plots prove that there is a good overall agreement between the compact model and the TCAD simulation results. As explained in Chap. 3, a transistor comprising three terminals (gate, source and drain) has

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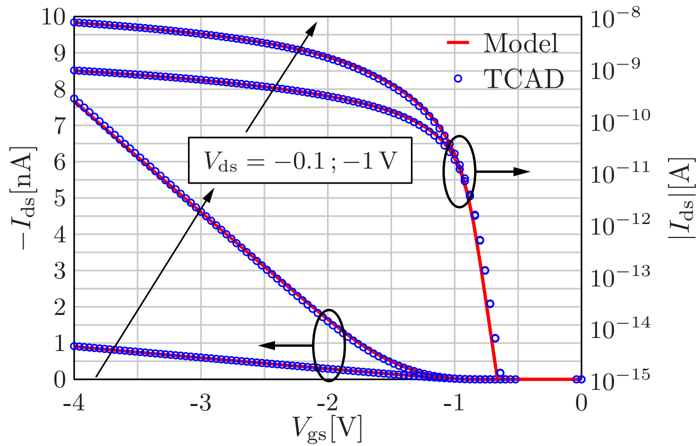

Figure 6.7.: Transfer curves of a staggered OTFT as simulated in a 2D simulation by Sentaurus TCAD (blue circles) at $V_{\mathrm{ds}} = -0.1\,\mathrm{V}$ and at $V_{\mathrm{ds}} = -1\,\mathrm{V}$ in comparison to the compact model (solid red lines). The transistor has a channel length of $L_{\mathrm{ch}} = 200\,\mu\mathrm{m}$. A Gaussian DOS with a total number of $N_{\mathrm{t,DOS}} = 1 \times 10^{21}\,\mathrm{cm}^{-3}$, a standard deviation of $\sigma_{\mathrm{DOS}} = 0.05\,\mathrm{eV}$, and a center position of $E_{0,\mathrm{DOS}} = E_{\mathrm{V}} - 0.05\,\mathrm{eV}$ is used. The TCAD simulation setup and the parameters of the compact model are depicted in column (a) of Tab. 6.2.

nine capacitances (Eq. (3.19)). However, due to the charge conservation principle some of these capacitances are dependent on each other. With the knowledge of only six of the nine capacitances, the remaining three capacitances can be calculated. Therefore, in the following only the trans-capacitances where the two indices are different will be plotted. However, for the sake of completeness, in Fig. 6.11 the three self-capacitances (i.e. the capacitances where the two indices are equal) are shown.

In Fig. 6.10, it becomes evident that the capacitances C_{gs}, C_{gd}, C_{sg} and C_{dg} are a little bit too steep in the voltage range $-2\,\mathrm{V} \leq V_{\mathrm{gs}} \leq -1\,\mathrm{V}$ but the overall agreement is very good. The transistor under investigation here has a comparatively long channel length of $L_{\mathrm{ch}} = 200\,\mu\mathrm{m}$ and in comparison to that small gate-to-contact overlap lengths of $L_{\mathrm{ov,GS}} = L_{\mathrm{ov,GD}} = 10\,\mu\mathrm{m}$. Consequently, a larger amount of charge is stored in the intrinsic carrier channel in comparison to the charges in the overlap regions. Therefore, the overall capacitive behavior of that transistor is dominated by the intrinsic carrier channel.

The simulated capacitances agree with the results that can be expected from theory [38] and they will briefly be discussed in the following. To start with, the quasistatic capacitances as plotted versus the gate-source voltage V_{gs} (Fig. 6.10) are observed. In order to simplify the discussion, the absolute values of the capacitances are referred to. At gate-source voltages close to zero, the transistor is turned off and the organic semiconductor is operated in depletion, i.e. there is no remarkable amount of accumulated charge carriers. Hence, even a change in

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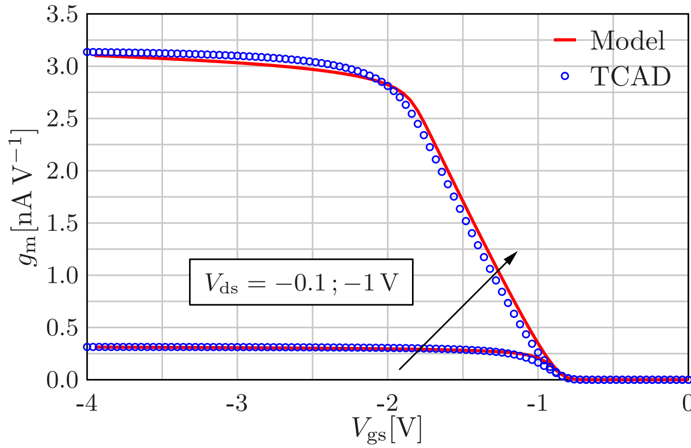

Figure 6.8.: Transconductance of the Sentaurus TCAD simulation (blue circles) in comparison to the compact model (solid red lines). These are the results of the same simulation and compact model setup as in Fig. 6.7.

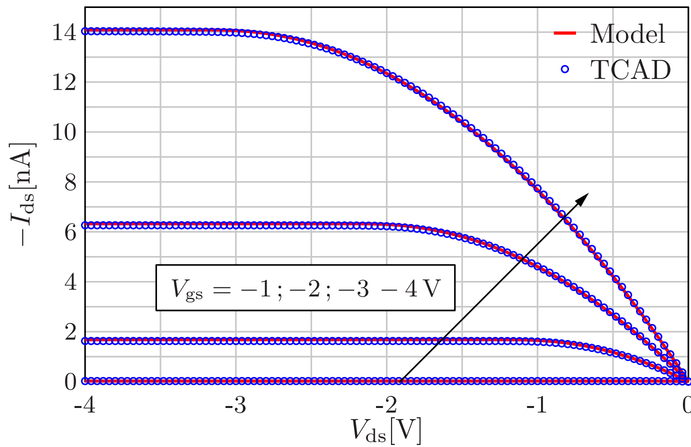

Figure 6.9.: Output curves of the Sentaurus TCAD simulation (blue circles) in comparison to the compact model (solid red lines) at different gate-source voltages as indicated in the figure. These are the results of the same simulation and compact model setup as in Fig. 6.7.

the surface potential does not lead to a notable change in the density of charge carriers, either. Consequently, the capacitances are nearly zero in this region. Only extrinsic capacitances are of importance then. However, as explained before, the extrinsic components (which are the overlap capacitances) are small in comparison to the intrinsic channel capacitances.

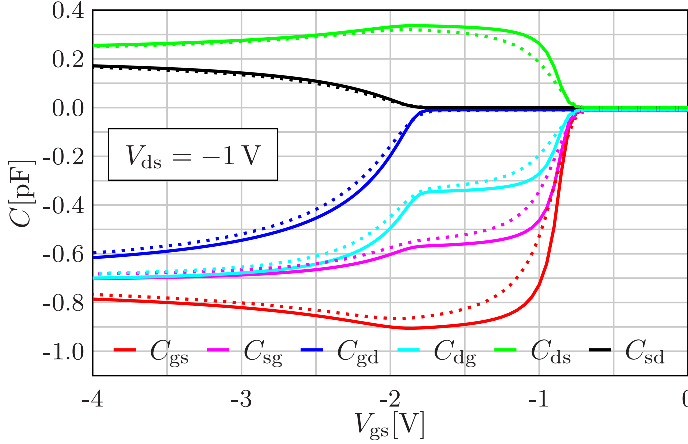

Figure 6.10.: Quasistatic trans-capacitances of a staggered OTFT with $L_{\mathrm{ch}} = 200\,\mu\mathrm{m}$. 2D Sentaurus TCAD simulation results (dashed lines) are shown in comparison to the compact model (solid lines). These are the results of the same simulation and compact model setup as in Fig. 6.7. The capacitances are plotted versus V_{gs} at a fixed drain voltage of $V_{\mathrm{ds}} = -1\,\mathrm{V}$.

If the absolute value of V_{gs} becomes greater, charges are accumulated in the organic semiconductor and a conductive channel is formed. The transistor leaves the sub-threshold regime and transits to the on-state. The drain-source voltage is $V_{\mathrm{ds}} = -1\,\mathrm{V}$ in this simulation. Please recall that the condition for a p-type transistor to be operated in the saturation regime of operation is the following [5]:

$$V_{\mathrm{ds}} \leq (V_{\mathrm{gs}} - V_{\mathrm{T0}})\,. \tag{6.4}$$

Looking at the voltages in Fig. 6.10, it can be concluded that the transistor is operated in the saturation regime approximately in the range $-2\,\mathrm{V} \leq V_{\mathrm{gs}} \leq -1\,\mathrm{V}$. It can be observed that the capacitance C_{gd} is still zero in this region whereas C_{gs} quickly reaches its maximum absolute value. This makes sense from the perspective that C_{gd} is the amount of charges at the gate which is altered due to a change in the drain potential. If a transistor is operated in saturation, the carrier-channel is pinched off somewhere in the channel before the drain electrode [39]. It is known that then, a change in V_{ds} does not lead to a further change in the current of the transistor which becomes visible in the output characteristics of a transistor at high absolute values of V_{ds}. There may occur short-channel effects such as a channel-length modulation [5] but they are neglected here. Similarly as the drain current is not under control of the drain terminal in this operation regime, the total charges in the device are not under control of the drain, either. In other words: A change in the drain potential does not change the amount of charges in the carrier channel. Since the charges are entirely under control of the source terminal the capacitance C_{gs} has its maximum value in the saturation regime of operation. Furthermore, it becomes evident that in the saturation regime of operation, the capacitances are non-reciprocal. For instance, C_{gs} has a larger absolute value than C_{sg}.

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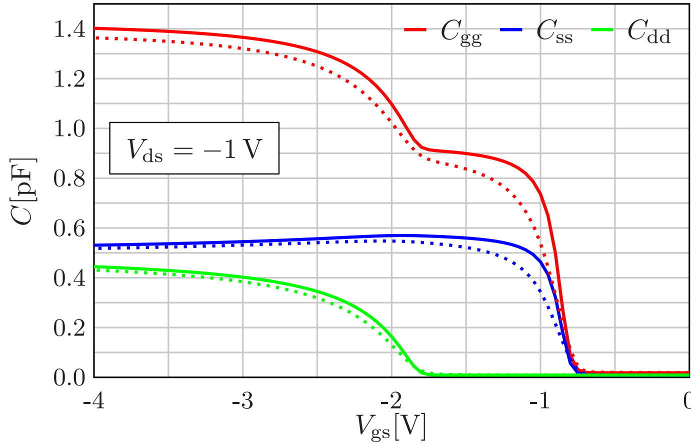

Figure 6.11.: Quasistatic self-capacitances of a staggered OTFT with $L_{ch} = 200\,\mu m$. 2D Sentaurus TCAD simulation results (dashed lines) are shown in comparison to the compact model (solid lines). These are the results of the same simulation and compact model setup as in Fig. 6.7. The capacitances are plotted versus V_{gs} at a fixed drain voltage of $V_{ds} = -1\,V$.

With the absolute value of V_{gs} further increasing beyond 2 V, the saturation regime of operation is left and the transistor enters the linear regime. In this regime, the channel is no longer pinched off before the drain electrode. Due to the influence of V_{ds}, there is still a gradient of the charge-carrier density in the channel. This is reflected in Fig. 6.10 by the fact that still C_{gs} is larger than C_{gd}. A change in the drain potential obviously does not alter the amount of total charges in the transistor as much as a change in the source potential does. If V_{gs} eventually becomes much larger than V_{ds}, the charges in the channel are nearly evenly distributed along the channel. In this operation regime, the total charges in the transistor are altered almost equally by a change in the drain potential or the source potential which can be seen in Fig. 6.10: The four capacitances C_{gs}, C_{sg}, C_{gd} and C_{dg} all converge to the same value. The trans-capacitances now show a nearly reciprocal behavior. According to the theory [38], the maximum capacitance that occurs in a transistor without extrinsic capacitances is the gate dielectric capacitance. When operated in the completely linear regime of operation, the four aforementioned capacitances then converge to $C'_{diel} \cdot W_{ch,G} \cdot L_{ch}/2$. This can easily be proven by a comparison to the setup values: According to column (a) of Tab. 6.2 and with the help of the electric field constant ε_0, the absolute value of the gate dielectric capacitance can be calculated as

$$C'_{diel} \cdot W_{ch,G} \cdot L_{ch} = \frac{\varepsilon_0 \cdot \varepsilon_{r,diel}}{t_{diel}} \cdot W_{ch,G} \cdot L_{ch} \tag{6.5}$$

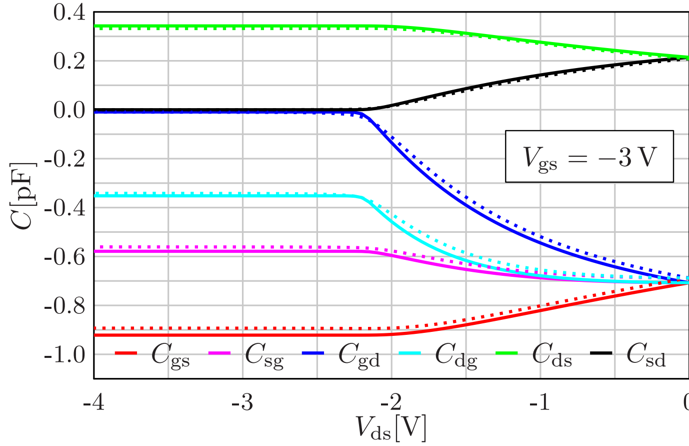

Figure 6.12.: Quasistatic trans-capacitances of a staggered OTFT with $L_{ch} = 200\,\mu m$. 2D Sentaurus TCAD simulation results (dashed lines) are shown in comparison to the compact model (solid lines). These are the results of the same simulation and compact model setup as in Fig. 6.7. The capacitances are plotted versus V_{ds} at a fixed gate voltage of $V_{gs} = -3\,V$.

where the specific values for that transistor can be entered. Since there are no fringe regions in this 2D simulation it can be said that $W_{ch,G} = W_{ch,SD}$:

$$C'_{diel} \cdot W_{ch,G} \cdot L_{ch} = \frac{8.854\,188 \times 10^{-12}\,\mathrm{A\,s\,V^{-1}\,m^{-1}} \cdot 3.9}{5.3 \times 10^{-9}\,\mathrm{m}} \cdot 1 \times 10^{-6}\,\mathrm{m} \cdot 200 \times 10^{-6}\,\mathrm{m} = 1.303\,\mathrm{pF}. \tag{6.6}$$

It can be verified by Fig. 6.10 that the four capacitances C_{gs}, C_{sg}, C_{gd} and C_{dg} really converge to the half of this value. It shall be emphasized again that the extrinsic gate-to-contact overlap capacitances have to be added to these intrinsic capacitances. However, as mentioned before, the extrinsic part is small in comparison to the intrinsic part in this transistor.

An interesting conclusion from Fig. 6.10 is that the capacitances are non-reciprocal, as outlined above. Especially in the saturation regime of operation, there are huge differences between the three pairs of trans-capacitances. Only in case of a completely linear point of operation, the trans-capacitances show a reciprocal behavior. This proves that the Meyer model [87] assuming the capacitances as lumped elements and thus neglecting any non-reciprocity is not sufficient for a proper AC characterization of long-channel OTFTs. The discussion of the capacitances also holds true for the plot of the trans-capacitances versus V_{ds} (Fig. 6.12). At the chosen gate-source voltage of $V_{gs} = -3\,V$, the transistor is operated in the linear regime in the range $-2\,V \leq V_{ds} \leq 0\,V$. It can be seen that for V_{ds} converging to zero the four capacitances C_{gs}, C_{sg}, C_{gd} and C_{dg} tend to the same value. If the transistor is operated in saturation, the drain potential does not have any control over the charges, which can be proven by the fact that both capacitances with "d" as the second index converge to zero.

2D simulation with a shorter channel

As explained above, the transistor with a long channel and in comparison to that small gate-to-contact overlap lengths is dominated by its intrinsic channel capacitances. However, organic transistors fabricated for a high-frequency operation are usually scaled down with respect to their channel length. Furthermore, the gate-to-contact overlap lengths are often process-related and in case of staggered transistors, they are important for the current injection [59]. Therefore, even with a tremendous down-scaling of the channel length, the gate-to-contact

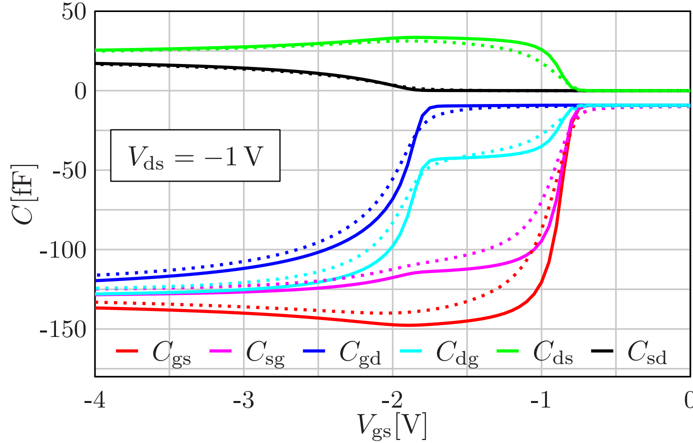

Figure 6.13.: Quasistatic trans-capacitances of a staggered OTFT with $L_{ch} = 20\,\mu m$. 2D Sentaurus TCAD simulation results (dashed lines) are shown in comparison to the compact model (solid lines). The capacitances are plotted versus V_{gs} at a fixed drain voltage of $V_{ds} = -1\,V$. The TCAD simulation setup and the fitting parameters of the compact model are depicted in column (b) of Tab. 6.2.

overlap lengths cannot be reduced beyond certain limits. Organic transistors for high-frequency operation which are reported in the literature often have gate-to-contact overlap lengths which are in the same order of magnitude as the channel lengths or even larger than the channel length [13, 43, 59, 88, 89]. Consequently, the gate-to-contact-overlap capacitances will become very important in comparison to the intrinsic channel capacitances, as was outlined in ref. [55]. In order to verify the correct implementation, a transistor with a shorter channel length of $L_{ch} = 20\,\mu m$ and comparatively large gate-to-contact overlaps of $L_{ov,GS} = L_{ov,GD} = 10\,\mu m$ is simulated in Sentaurus TCAD. The fitting procedure of this transistor is the same as for the transistor with the longer channel presented in the section before. The DC fitting will not be shown here.

Figures 6.13 and 6.14 show the quasistatic trans-capacitances of the transistor plotted versus V_{gs} and V_{ds}. The results are similar to those of the transistor with the longer channel length but they will be discussed briefly. Again, the absolute values of the capacitances will be referred to. In Fig. 6.13, it can be observed that in the off-state ($-1\,V \leq V_{gs} \leq 0\,V$) the four capacitances

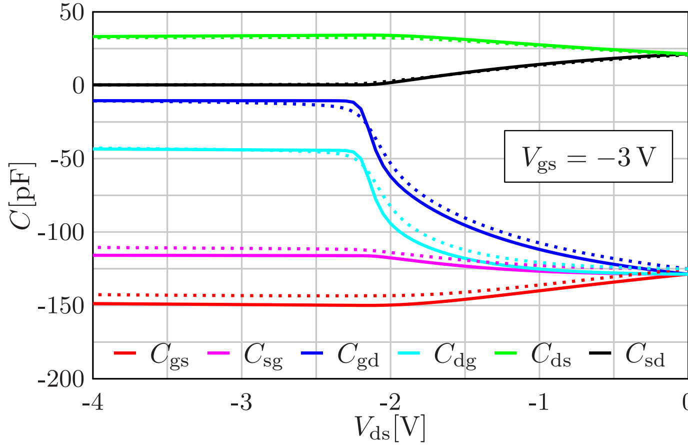

Figure 6.14.: Quasistatic trans-capacitances of a staggered OTFT with $L_{ch} = 20\,\mu m$. 2D Sentaurus TCAD simulation results (dashed lines) are shown in comparison to the compact model (solid lines). These are the results of the same simulation and compact model setup as in Fig. 6.13. The capacitances are plotted versus V_{ds} at a fixed gate voltage of $V_{gs} = -3\,V$.

C_{gs}, C_{sg}, C_{gd} and C_{dg} do not converge to zero but to a value larger than that. Since the organic semiconductor is operated in depletion it behaves like an insulator with a certain dielectric permittivity. The gate-to-contact overlap region then behaves as a series connection of the gate dielectric and the depleted organic semiconductor. With the transistor transiting to the saturation regime of operation ($-2\,V \leq V_{gs} \leq -1\,V$), the capacitance C_{gd} remains at its constant value whereas C_{gs} rapidly increases. Finally, the four capacitances C_{gs}, C_{sg}, C_{gd} and C_{dg} converge to the same value in the very linear regime of operation. Since the organic semiconductor is operated completely in accumulation the gate dielectric capacitance is the only capacitance that can be measured then. However, which is quite important: The area in the gate-to-contact overlap regions has to be taken into account because here the charges are accumulated as well.

It can be seen that the overall agreement between the TCAD-simulated capacitances and the compact model is good but the deviations are higher in comparison to the long-channel transistor.

3D Simulation with one Finger

The verification of the fringe current model has already been shown above. In this section, the capacitance model is shown at the basis of the capacitance C_{gs}. The quasistatic capacitances of the transistor comprising different fringe widths w_{ovl} were simulated at two different V_{ds}. The fitting procedure for the capacitance model is the same as for the 2D transistors. First, a proper DC fitting is performed. In Fig. 6.4, the value for the fringe-current fitting parameter that is used for each of the overlap widths is depicted. As outlined before, δ_{fit} does not

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have an influence on the quasistatic capacitances since it effectively cancels out in the final charge equations. Figures 6.15 and 6.16 show the capacitance C_{gs} as simulated in a 3D TCAD simulation in comparison to the compact model for varying overlap widths w_{ovl}. As can be seen, a good overall agreement is achievable. This proves that the equations for the total charges really have to be calculated based on the total gate width ($W_{ch,G}$) and not only on the width of the electrodes ($W_{ch,SD}$).

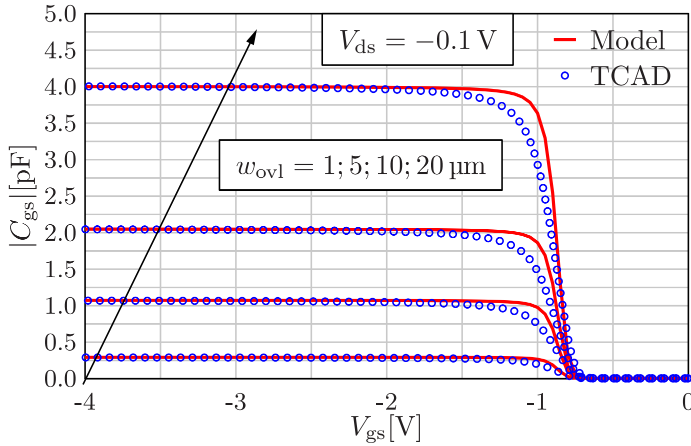

Figure 6.15.: Quasistatic capacitance C_{gs} of a staggered single-finger OTFT. 3D Sentaurus TCAD simulation results (blue circles) are shown in comparison to the compact model (solid red lines) where the fringe width w_{ovl} is varied. The capacitances are plotted versus V_{gs} at a fixed drain voltage of $V_{ds} = -0.1$ V. The channel length is $L_{ch} = 20$ µm. The TCAD simulation setup and the fitting parameters of the compact model are depicted in column (c) of Tab. 6.2.

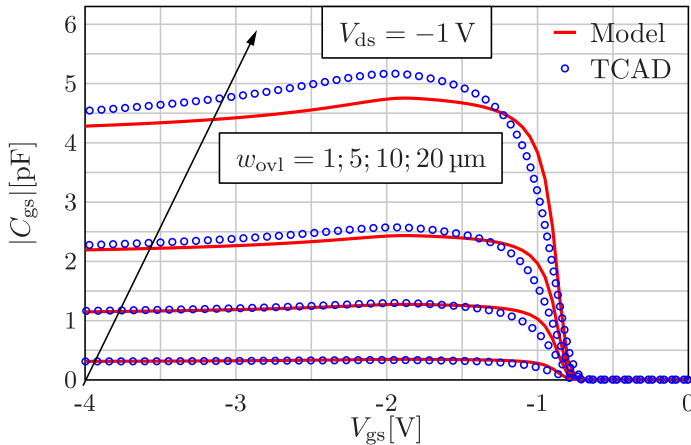

Figure 6.16.: Quasistatic capacitance C_{gs} of a staggered single-finger OTFT. 3D Sentaurus TCAD simulation results (blue circles) are shown in comparison to the compact model (solid red lines) where the fringe width w_{ovl} is varied. The capacitances are plotted versus V_{gs} at a fixed drain voltage of $V_{ds} = -1$ V. These results correspond to the results depicted in Fig. 6.15.

In Fig. 6.16, it is observable that at high V_{ds} the compact model slightly underestimates the capacitance C_{gs} if the fringe width is large. This inaccuracy is attributed to a simplification in the compact model. Observing the plot where the charge distribution in a cutplane of a staggered OTFT is shown (Fig. 4.2), it can be concluded that in the electrode regions (i.e. the regions next to the gate-to-contact-overlap regions) the charge density is in part dependent on the z position. For reasons of simplicity, in the compact model the charge density is assumed constant for every z position in the whole gate plane. Whereas this assumption may hold true in the channel region, it is not completely correct in the electrode region. If w_{ovl} is short, the z dependence of the charge density in the electrode regions is not pronounced. However, for large w_{ovl}, a more sophisticated approach for the calculation of the spatial distribution of the charges around the electrodes could be developed. Anyway, the agreement shown in Fig. 6.16 is regarded as sufficient.

3D Simulation with two Fingers

Similarly as the simulation of a transistor comprising one single source/drain finger and fringe regions next to it, the simulation of a transistor consisting of two source/drain fingers with fringe regions between them and beyond the first and the second finger has been fitted by the compact model. As shown in Sec. 6.2, the fringe current model works properly also for this architecture by assuming the two fingers as a parallel connection of two independent fingers. As shown in Fig. 6.6, the parameter δ_{fit} can be used to fit the current of the compact model to the TCAD-simulated current.

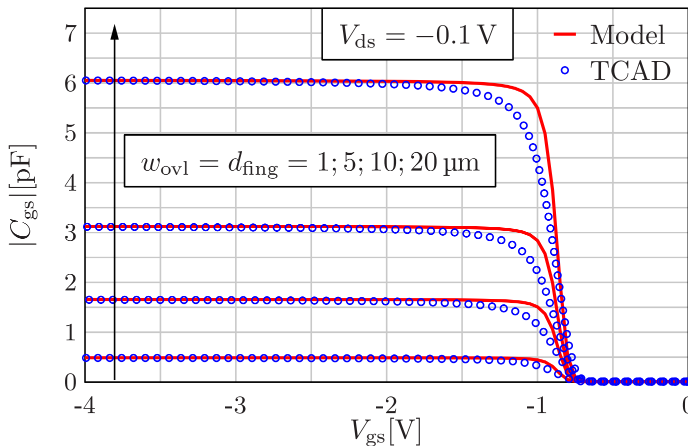

Figure 6.17.: Quasistatic capacitance C_{gs} of a staggered double-finger OTFT. 3D Sentaurus TCAD simulation results (blue circles) are shown in comparison to the compact model (solid red lines) where the fringe width w_{ovl} is varied simultaneously with the distance d_{fing} between the two source/drain fingers. The capacitances are plotted versus V_{gs} at a fixed drain voltage of $V_{\mathrm{ds}} = -0.1\,\mathrm{V}$. The channel length is $L_{\mathrm{ch}} = 20\,\mu\mathrm{m}$. The TCAD simulation setup and the fitting parameters of the compact model are depicted in column (d) of Tab. 6.2.

Due to the high complexity of the 3D TCAD simulations the capacitances of the double-finger transistor are simulated versus V_{gs} only at a small drain-source voltage of $V_{ds} = -0.1\,V$. In Fig. 6.17, the TCAD-simulated quasistatic capacitance C_{gs} is shown in comparison to the compact model. As can be seen, there is an excellent agreement. Also here, it can be proven that the assumption of the total gate width $W_{ch,G}$ is correct for the calculation of the total charges.

6.3.2.2 Capacitance Measurements

In this section, the capacitances will be verified by quasistatic measurements. The data used for verification are the measured results published by Zaki et al. in ref. [40]. OTFTs based on the small-molecule semiconductor dinaphto[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DNTT) were fabricated by vacuum deposition of the different layers and by creating a hybrid gate-dielectric by an oxidization of the gate-metal (aluminum) and subsequently allowing a self-assembling monolayer of n-tedradecylphosphonic acid to form on top of the aluminum oxide. The geometric values and parameters of the transistor including some fitting parameters of the compact model are shown in Tab. 6.3.

Table 6.3.: Geometry values and parameters of the transistor presented by Zaki et al. in ref. [40]. Some fitting parameters of the compact model are shown as well.

Device Param.	Value
L_{ch} [µm]	200
$W_{contact}$ [µm]	400
$L_{ov,GS}$ [µm]	10
$L_{ov,GD}$ [µm]	10
t_{diel} [nm]	5.3
t_{osc} [nm]	11
w_{ovl} [µm]	30
N_{fing} [−]	1
d_{fing} [µm]	-
$\varepsilon_{r,osc}$ [−]	2.84
$\varepsilon_{r,diel}$ [−]	3.37
Compact Param.	
S_{obs} [mV/dec]	70
κ [$cm^2V^{-\beta-1}s^{-1}$]	2.05
β [−]	0.03
λ [V^{-1}]	0
δ_{fit} [−]	0.27

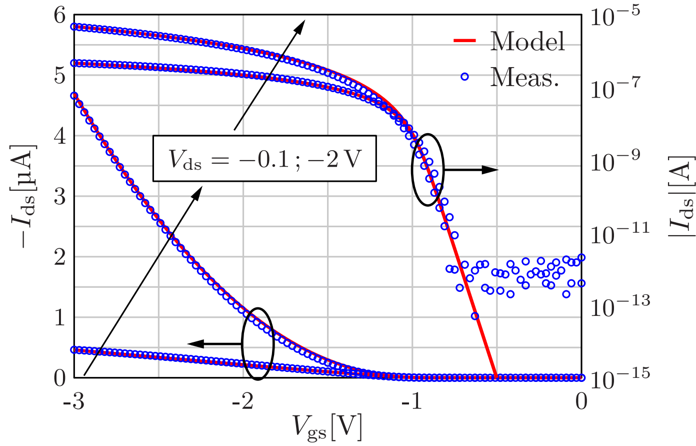

Figure 6.18.: Transfer curves of a staggered OTFT at $V_{ds} = -0.1\,V$ and at $V_{ds} = -2\,V$. The measurement results of a single-finger OTFT presented in ref. [40] (blue circles) are shown in comparison to the compact model (solid red lines). The parameters of the transistor are listed in Tab. 6.3. Here, a threshold voltage of $V_{T0} = -0.94\,V$ is used.

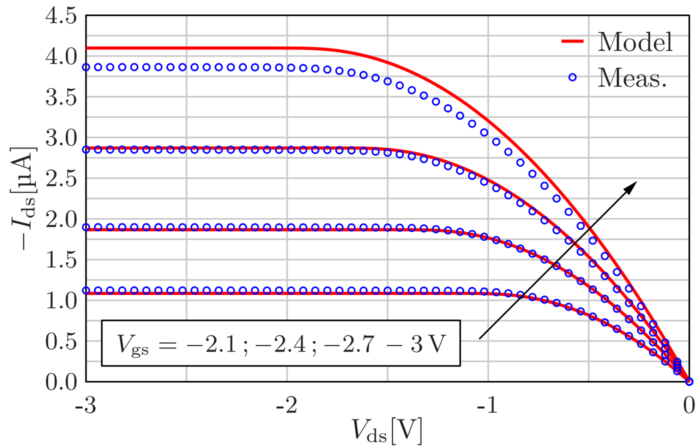

Figure 6.19.: Output curves of a staggered OTFT at different gate-source voltages. The measurement results of a single-finger OTFT presented in ref. [40] (blue circles) are shown in comparison to the compact model (solid red lines). The parameters of the transistor are listed in ref. Tab. 6.3. Due to a bias-stressed-induced threshold voltage shift a different threshold voltage than for the transfer curves has to be assumed. Here, a value of $V_{T0} = -1.07\,V$ is set.

The transistor under investigation is a long-channel transistor ($L_{ch} = 200\,\mu m$). DC measurements were conducted and subsequently, the capacitances C_{gs} and C_{gd} were measured using an LCR meter which can measure the complex admittance between two terminals. Since this measurement system is able to measure inductive, capacitive and resistive circuit components the three formula symbols of the inductance (L), the capacitance (C) and the resistance (R) are used to describe its name. The LCR meter applies a DC bias and superimposes an AC

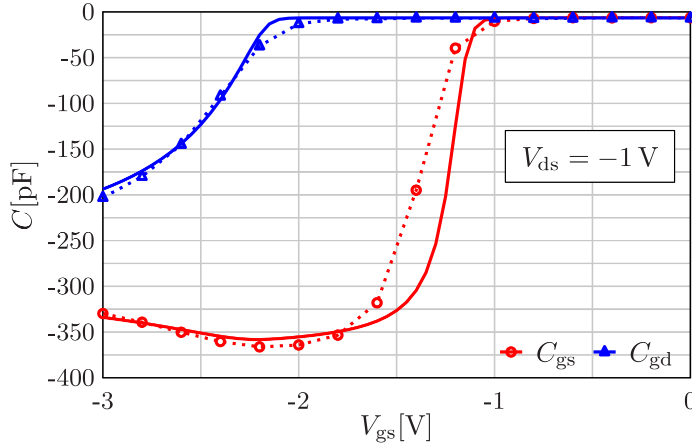

Figure 6.20.: Internodal capacitances of a staggered OTFT at $V_{ds} = -1\,V$ plotted versus V_{gs}. The low-frequency ($f = 500\,Hz$) measurement results of a single-finger OTFT presented in ref. [40] (dotted lines with symbols) are shown in comparison to the compact model (solid lines). The parameters of the transistor are listed in Tab. 6.3. Due to a bias-stressed-induced threshold voltage shift a different threshold voltage than for the transfer curves has to be assumed. Here, a value of $V_{T0} = -1.2\,V$ is set.

signal with a small magnitude and varying frequencies. Then, the complex admittance between the two terminals of the LCR meter is measured. During the measurement, the gate electrode is connected to the low-potential connector of the LCR meter while the source and drain electrodes - dependent on whether C_{gs} or C_{gd} is measured - are connected to the high-potential connector or to a DC voltage source. Based on the measured admittance $\underline{Y}$, the following calculations are performed:

$$C = \mathrm{Im}\left(\underline{Y}/\omega\right) \tag{6.7}$$

$$G = \mathrm{Re}\left(\underline{Y}\right) \tag{6.8}$$

where ω is the angular frequency of the applied signal. C is the capacitance between the two terminals and G is the conductance. Similarly as explained in the section before, the AC model is verified by previously fitting the DC compact model to the measured transfer and output curves. Figures 6.18 and 6.19 depict these curves in comparison to the compact model. OTFTs are sensitive to bias stress which is the application of terminal voltages for a certain amount of time. A prolonged application of a gate-source and a drain-source voltage causes a filling or emptying of mid-term and long-term traps in the organic semiconductor which results in a shift of the threshold voltage [90]. These trapping effects occur also during the sweeps of the voltages which leads to a hysteresis effect in the measured curves. Furthermore, V_{gs} and V_{ds} have different influences on the trapping behavior. The consequence of this is that the measured curves will look different depending on which curves are recorded first. Therefore,

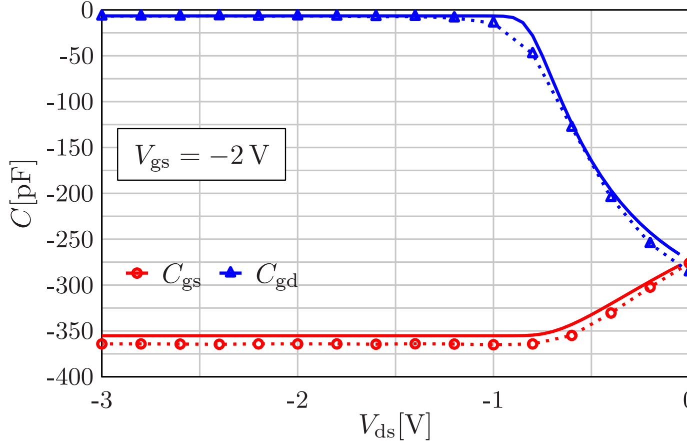

Figure 6.21.: Internodal capacitances of a staggered OTFT at $V_{gs} = -2$ V plotted versus V_{ds}. The low-frequency ($f = 500$ Hz) measurement results of a single-finger TFT presented in ref. [40] (dotted lines with symbols) are shown in comparison to the compact model (solid lines). The parameters of the transistors are the same as in Fig. 6.18. Due to a bias-stressed-induced threshold voltage shift a different threshold voltage than for the transfer curves has to be assumed. Here, a value of $V_{T0} = -1.2$ V is set.

the threshold voltage of the transistor is regarded as a fitting parameter which may vary by some hundreds of millivolts. Please note that in order to fit both the transfer and the output curves, slightly different threshold voltages V_{T0} have to be assumed.

As depicted in Tab. 6.3, the power-law exponent β has a value close to zero. According to theory, the power-law mobility is used to describe the degree of crystallinity of the semiconductor [91]. If the semiconductor is quite disordered (non-crystalline) and has thus a Gaussian DOS with a high standard deviation, this leads to a non-linear behavior in the transfer curves. The power-law mobility is then used as an empirical correction in order to represent this non-linear trend [28].

After the fitting of the charge-based DC model, the results of the capacitance model are compared. Also here, the threshold voltage is assumed to fluctuate a little bit due to the charge trap dynamics [90]. The capacitances were measured at a low frequency of $f = 500$ Hz, which is a quasistatic operation. In Fig. 6.20, the two internodal capacitances C_{gs} and C_{gd} are plotted versus V_{gs} for a fixed V_{ds}. As can be seen, a good agreement is obtainable. Due to the effects already mentioned, the charge-trapping dynamics will cause threshold voltage shifts. It is thus possible that the threshold voltage of the transistor is different for both of the curves depicted here. However, one constant threshold voltage is assumed for both curves. The overall agreement of the measured versus modeled quasistatic capacitances is very high. Since the transistor has fringe regions beyond the source/drain electrodes and since the agreement is

good it can be concluded that it is the proper way to use the total gate width $W_{\mathrm{ch,G}}$ for the calculation of the total charges. In Fig. 6.21, the quasistatic capacitances are shown versus V_{ds} for a fixed V_{gs}. Also here, a high level of agreement is obtainable proving the validity of the model for a quasistatic operation.

6.3.2.3 Differential Amplifiers

In ref. [92], two differential amplifiers based on organic thin-film transistors are presented by Seifaei et al. The transistors are fabricated in the same manner and based on the same materials as the transistors in the former section for which the quasistatic capacitances have been shown. In Fig. 6.22, the circuit schematic of a differential amplifier is shown and in Tab. 6.4, the pa-

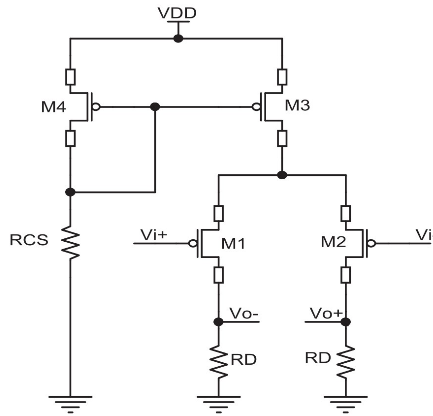

Figure 6.22.: Circuit schematic of a differential amplifier. This image is taken from ref. [92].

rameters of the transistors in that circuit are shown. The parameters where no special reference to some of the transistors is made are valid for all transistors in the circuit. Furthermore, in the table some fitting parameters of the compact model are shown which will be used for the simulation of the circuits.

Transistors M3 and M4 are equal and so are M1 and M2. Transistor M4 stabilizes itself by the resistance R_{CS}. In case that the DC current flowing through the transistor is reduced by a bias-stress-induced threshold-voltage shift or a mobility degradation, the voltage drop across R_{CS} decreases and pulls down the gate potential. Consequently, the absolute value of the gate-source voltage of M4 increases which leads to an increase in the current. This principle is used in ref. [92] in order to achieve a self-stabilizing effect. As can be seen, the gates of transistors M3 and M4 are interconnected and furthermore the source terminals of both transistors are connected to the same DC voltage V_{dd}. Consequently, the gate-source voltage of M4 is mirrored to transistor M3. Thus, M3 and M4 constitute a current mirror provided that both are operated in the saturation regime of operation. A differential pair

consisting of transistors M1 and M2 is used as the amplifying part of the circuit. The geometric channel width of M1 and M2 is chosen to be half the geometric channel width of M3 and M4. Transistors M1 and M2 are biased by a common DC voltage denoted as V_{iCM} and a superimposed AC voltage:

$$V_{\mathrm{i+}} = V_{\mathrm{iCM}} + v_{\mathrm{AC}} \tag{6.9}$$

where v_{AC} is the AC signal. Since a differential amplifier is regarded the voltage difference at the two inputs of the transistors M1 and M2 shall be amplified. Thus, the voltage difference between the gates of M1 and M2 is regarded as the input of the amplifier. The AC stimulus is added positively to the gate of M1 and negatively (i.e. with a phase shift of 180°) at the gate of M2. The output voltage of the amplifier is defined as the voltage difference between $V_{\mathrm{0-}}$ and $V_{\mathrm{0+}}$. As can be seen, the voltage drop depends on the resistance R_{D} of the series resistors. The outputs of the two differential amplifiers are loaded by a load capacitance of 20 pF. However, the connector cables and the external circuitry also have a capacitance which is not known from measurements. Therefore, the load capacitance of the amplifiers is regarded as a fitting parameter.

In ref. [92], the differential amplifiers are measured by means of an AC analysis. Fixed DC voltages V_{dd} and V_{iCM} are applied and an AC signal with a small amplitude is applied. Then, an AC sweep over a range of frequencies is conducted. The authors of ref. [92] use the compact model by Marinov and Deen [66] in order to reproduce the results. Even if this compact model only provides a quasistatic description of the OTFTs, it is capable of reproducing the measured results at least with a certain accuracy. In order to test the compact model developed in this dissertation, the model equations are implemented in the hardware description language Verilog-A and the model is executed in the analog design environment Cadence Virtuoso [70]. The circuit of the differential amplifier is reproduced and an AC sweep is conducted. Since only AC measurements of the fabricated circuits are available the DC characteristics of the transistors cannot be fitted prior to conducting the AC simulation. Therefore, the fitting parameters of the DC model are used in order to tune the simulated AC results. In Cadence Virtuoso, the magnitude of the output signal (A_{AC}) is calculated based on the magnitudes of the small-signal voltages of the input in relation to the output:

$$A_{\mathrm{AC}} = 20 \cdot \lg\left(\frac{|V_{\mathrm{0+}}|}{|v_{\mathrm{AC}}|}\right) \tag{6.10}$$

where lg is the logarithm to base 10. Please note that here only the voltage $V_{\mathrm{0+}}$ is set in relation to v_{AC}. In principle, the voltage difference between $V_{\mathrm{0+}}$ and $V_{\mathrm{0-}}$ could have been set in relation to the voltage difference of $V_{\mathrm{i+}}$ and $V_{\mathrm{i-}}$. However, this would result in the same gain.

Table 6.4.: Parameters of the two differential amplifiers. The parameters of the transistors are shown along with fitting parameters of the compact model.

Device Param.	Diff. Amp. 1	Diff. Amp. 2
$W_{\mathrm{ch,SD,M3/M4}}\,[\mu\mathrm{m}]$	2000	1000
$W_{\mathrm{ch,SD,M1/M2}}\,[\mu\mathrm{m}]$	1000	500
$w_{\mathrm{ovl}}\,[\mu\mathrm{m}]$	50	50
$N_{\mathrm{fing,M3/M4}}\,[-]$	20	10
$N_{\mathrm{fing,M1/M2}}\,[-]$	10	5
$d_{\mathrm{fing}}\,[\mu\mathrm{m}]$	50	50
$L_{\mathrm{ov,GS}}\,[\mu\mathrm{m}]$	30	30
$L_{\mathrm{ov,GD}}\,[\mu\mathrm{m}]$	30	30
$R_{\mathrm{D}}\,[\mathrm{M\Omega}]$	22	4
$R_{\mathrm{CS}}\,[\mathrm{M\Omega}]$	22	4
$L_{\mathrm{ch}}\,[\mu\mathrm{m}]$	20	20
$t_{\mathrm{diel}}\,[\mathrm{nm}]$	5.3	5.3
$t_{\mathrm{osc}}\,[\mathrm{nm}]$	25	25
$\varepsilon_{\mathrm{r,diel}}\,[-]$	3.9	3.9
$\varepsilon_{\mathrm{r,osc}}\,[-]$	5.5	5.5
Compact Param.		
$\delta_{\mathrm{fit}}\,[-]$	0.215	0.215
$S_{\mathrm{obs}}\,[\mathrm{mV/dec}]$	140	160
$\kappa\,[\mathrm{cm^2V^{-\beta-1}s^{-1}}]$	2	2
$\beta\,[-]$	0	0
$R_{\mathrm{contact}}\,[\mathrm{k\Omega}]$	20	25
$C_{\mathrm{load}}\,[\mathrm{pF}]$	95	105

The phase shift of the amplifier (ϕ_{AC}) is determined by relating the phase of the signal V_{0+} to the phase of the input signal $V_{\mathrm{i+}}$:

$$\phi_{\mathrm{AC}} = \phi\left(V_{0+}\right) - \phi\left(V_{\mathrm{i+}}\right). \tag{6.11}$$

Based on these definitions, the AC sweep can be conducted in Cadence Virtuoso. Figures 6.23 and 6.24 show the measured results of ref. [92] in comparison to the AC simulation of the compact model in Cadence Virtuoso. It should be noted that, as indicated by Tab. 6.4, a constant Ohmic contact resistance has been used. The sheet resistance model according to Eq. (2.10) is not used. It can be seen that there is an excellent agreement between measured and simulated curves, even better than the agreement that was obtained in ref. [92] based on the Marinov-Deen model [66]. It is an interesting fact that the compact model provides a good agreement, even though it is only a quasistatic compact model without the coverage of non-quasistatic effects. An explanation for this behavior is that the differential amplifier

consists of several transistors and of the fixed resistances R_{CS} and R_{D}. As a consequence, the simulator has to account for the correct charging and discharging of the transistor capacitances through adjacent circuit elements. If, for example, the gate voltage of transistor M1 in Fig. 6.22 is slightly increased due to the AC stimulus, the total amount of charge in the channel increases. Since charges cannot be created or disappear but have to enter or leave the device through the gate, source and drain ports the charging current of M1 has to flow through transistor M3 and through the series resistor R_{D}. Even if the time-dependent distribution of the charges in the channel of M1 is neglected, the effect of charging currents flowing through adjacent circuit elements seems to be sufficient to capture the non-quasistatic effects that occur in the circuit. However, in Chap. 7, a more sophisticated macro model accounting for the charge distribution in the channel of a transistor will be derived.

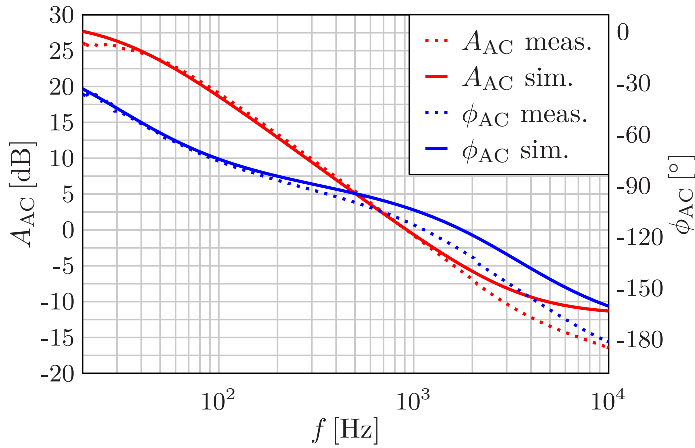

Figure 6.23.: Magnitude and phase response of the differential amplifier 1. The measurements [92] (dotted lines) are compared to the compact model (solid lines). The parameters of the transistors and the compact model are depicted in Tab. 6.4. The operation voltage of the circuit is $V_{\mathrm{dd}} = 5\,\mathrm{V}$ and the common-mode voltage is set to $V_{\mathrm{iCM}} = 2\,\mathrm{V}$. The magnitude of the AC signal is set to $v_{\mathrm{AC}} = 100\,\mathrm{mV}$. This picture was published in [54] and was slightly modified.

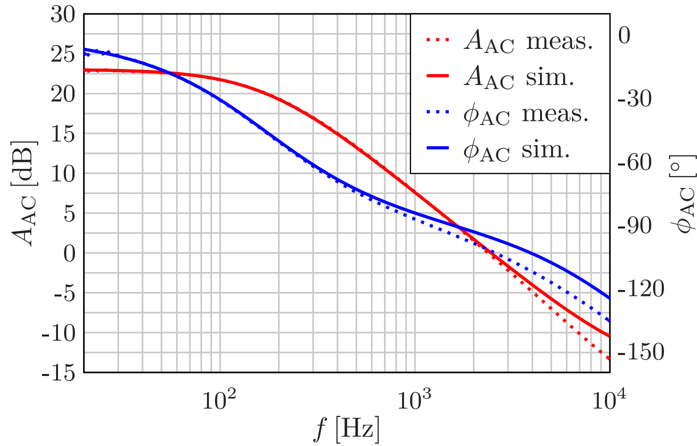

Figure 6.24.: Magnitude and phase response of the differential amplifier 2. The measurements [92] (dotted lines) are compared to the compact model (solid lines). The parameters of the transistors and the compact model are depicted in Tab. 6.4. The operation voltage of the circuit is $V_{dd} = 5\,V$ and the common-mode voltage is set to $V_{iCM} = 2\,V$. The magnitude of the AC signal is set to $v_{AC} = 100\,mV$. This picture was published in [54] and was slightly modified.

6.3.3 Coplanar Transistors

6.3.3.1 TCAD Simulations

Transistors in the coplanar device architecture were simulated in Sentaurus TCAD. The verification is very similar as for the staggered transistors. In Tab. 6.5, the parameters of the TCAD simulations are depicted and in addition the fitting parameters of the compact model are shown.

The charges in the intrinsic carrier channel and in the fringe regions are calculated in the same manner for staggered and coplanar transistors. The difference between both architectures is only the way that charges in the gate-to-contact overlap regions are calculated. In order to visualize the influence of the overlap regions, a transistor with a a mid-long channel length of $L_{ch} = 20\,\mu m$ and comparatively large gate-to-contact overlap lengths of $L_{ov,GS} = L_{ov,GD} = 10\,\mu m$ is considered. Prior to the simulation of the quasistatic capacitances the DC model is fitted. Figures 6.25 and 6.26 show the DC fitting of the compact model in comparison to the TCAD simulation results.

UNIVERSITAT ROVIRA I VIRGILI
CHARGE-BASED COMPACT MODELING OF CAPACITANCES AND LOW-FREQUENCY NOISE IN ORGANIC THIN-FILM TRANSISTORS
Jakob Simon Leise

Table 6.5.: Parameters of TCAD simulations of a coplanar transistor and fitting parameters of the compact model. Column (a) shows the parameters of a 2D-simulation where a Gaussian DOS with a total number of $N_{t,DOS} = 1 \times 10^{21}$ cm^{-3}, a standard deviation of $\sigma_{DOS} = 0.05$ eV, and a center position of $E_{0,DOS} = E_V - 0.05$ eV is used and column (b) shows the parameters of a 3D-simulation where a square-root DOS with an effective hole density of $N_v = 1 \times 10^{21}$ cm^{-3} is used.

TCAD Param.	(a) 2D Gauss.	(b) 3D sqrt.
χ_{osc} [eV]	1.81	1.81
E_g [eV]	3.38	3.38
μ_n [cm^2 V^{-1} s^{-1}]	1e-10	1e-10
μ_p [cm^2 V^{-1} s^{-1}]	1	3
$\varepsilon_{r,osc}$ [−]	3	3
$\varepsilon_{r,diel}$ [−]	3.9	4
$\Phi_{m,g}$ [eV]	4.1	4.1
$\Phi_{m,sd}$ [eV]	5.19	5.19
L_{ch} [µm]	20	20
$W_{contact}$ [µm]	1	1
$L_{ov,GS}$ [µm]	10	5
$L_{ov,GD}$ [µm]	10	5
t_{diel} [nm]	5.3	5.3
t_{osc} [nm]	1	25
w_{ovl} [µm]	0	variable
N_{fing} [−]	1	1
d_{fing} [µm]	-	-
Compact Param.		
S_{obs} [mV/dec]	60	60
V_{T0} [V]	-0.86	-0.84
κ [cm^{2}V$^{-\beta-1}$s^{-1}]	0.97	2.8
β [−]	0	0.03
λ [V^{-1}]	0	0

As can be seen, there is a good agreement. The fitting of the quasistatic capacitance model is depicted in Figs. 6.27 and 6.28. Also here, the agreement is good. Deviations between measured and simulated curves occur in the same voltage ranges as for the staggered transistor. Observing the capacitances versus V_{gs} in the sub-threshold regime of operation (Fig. 6.27), an interesting difference between the coplanar and the staggered architecture becomes visible: The absolute values of the off-state capacitances C_{gs}, C_{sg}, C_{gd} and C_{dg} are much larger than the capacitances of the corresponding staggered transistor (Fig. 6.13). This fact is explainable by the differences in the gate-to-contact overlap regions. In a coplanar transistor, these regions show a behavior comparable to a parallel-plate capacitor. In staggered transistors, by contrast, the gate-to-contact overlap region can be regarded as a series connection of two capacitors

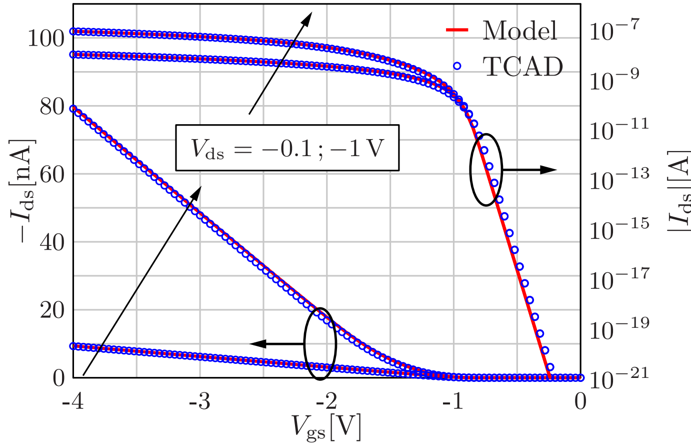

Figure 6.25.: Transfer curves of a coplanar OTFT as simulated in a 2D simulation by Sentaurus TCAD (blue circles) at $V_{ds} = -0.1\,V$ and at $V_{ds} = -1\,V$ in comparison to the compact model (solid red lines). The transistor has a channel length of $L_{ch} = 20\,\mu m$. The setup of the TCAD simulation and the chosen values of the fitting parameters of the compact model are depicted in column (a) of Tab. 6.5.

if the organic semiconductor is depleted. Since the gate dielectric capacitance is equal for the simulation of the staggered and the coplanar transistor it makes sense that the off-state capacitance of the staggered transistor is smaller than that of the coplanar transistor.

In addition to the 2D simulations, coplanar OTFTs were simulated in a 3D simulation in order to verify the model for the extrinsic charges including fringe regions as presented in Sec. 4.2.1. In a similar manner as for the staggered transistors, the capacitances in the 3D coplanar transistors were verified by first fitting the DC characteristics of the compact model to the simulation results. In Fig. 6.29, the transfer curves at $V_{ds} = -1\,V$ of two coplanar OTFTs with different fringe widths are shown. By means of the fitting parameter δ_{fit}, the current can be fitted well for the transistor comprising a fringe region. As mentioned before for the staggered transistors, in the 3D TCAD simulation a square-root DOS has been assumed in order to improve the numerical stability of the simulation. As can be seen in Tab. 6.5, a power-law mobility with $\beta = 0.03$ is assumed even if the DOS is square-root shaped and no mobility models are turned on. In principle, the power-law exponent could be chosen as zero but the agreement is a little better when using the value of 0.03. In Fig. 6.30, the capacitance C_{gs} is compared for the two transistors comprising different fringe widths. It can be seen that at $w_{ovl} = 10\,\mu m$ the compact model does not perfectly agree with the simulation results. This behavior can be attributed to the fact that the charge distribution in the direction of the channel width next to the source/drain electrodes is not perfectly constant which is, however, one of the assumptions in the compact model.

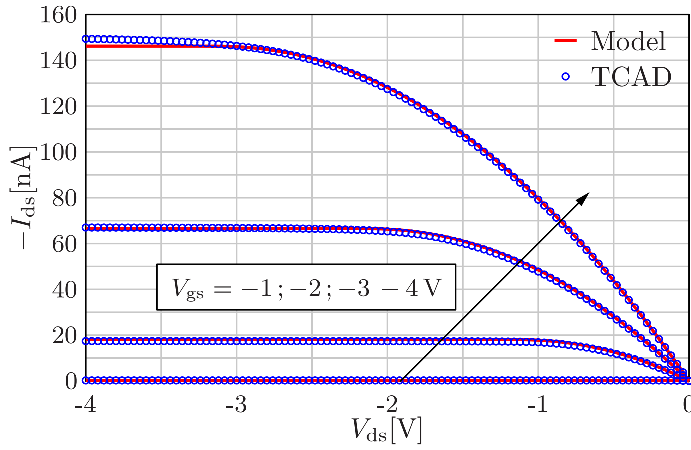

Figure 6.26.: Output curves of the Sentaurus TCAD simulation of a coplanar OTFT with $L_{ch} = 20\,\mu m$ (blue circles) in comparison to the compact model (solid red lines) at different gate-source voltages as indicated in the figure. These are the results of the same simulation and compact model setup as in Fig. 6.25.

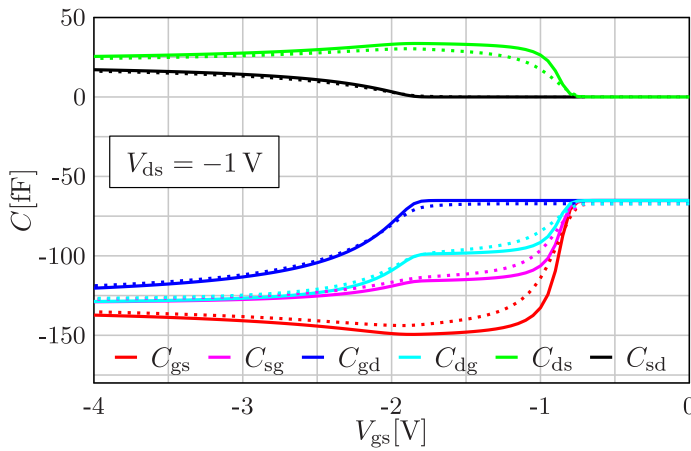

Figure 6.27.: Quasistatic trans-capacitances of a coplanar OTFT with $L_{ch} = 20\,\mu m$. 2D Sentaurus TCAD simulation results (dashed lines) are shown in comparison to the compact model (solid lines). These are the results of the same simulation and compact model setup as in Fig. 6.25. The capacitances are plotted versus V_{gs} at a fixed drain voltage of $V_{ds} = -1\,$V.

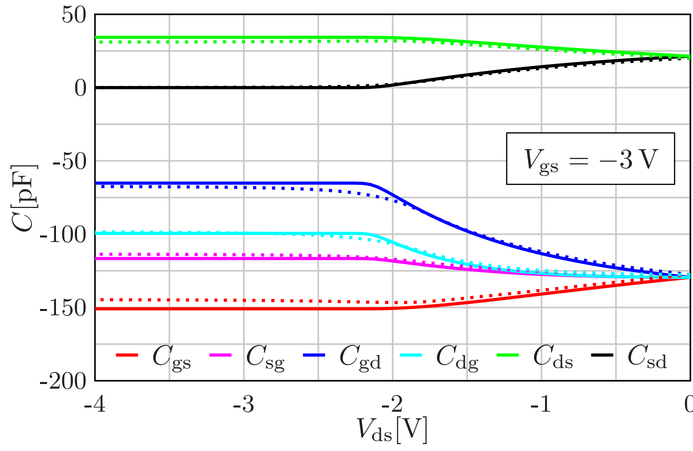

Figure 6.28.: Quasistatic trans-capacitances of a coplanar OTFT with $L_{ch} = 20\,\mu m$. 2D Sentaurus TCAD simulation results (dashed lines) are shown in comparison to the compact model (solid lines). These are the results of the same simulation and compact model setup as in Fig. 6.25. The capacitances are plotted versus V_{ds} at a fixed gate voltage of $V_{gs} = -3\,V$.

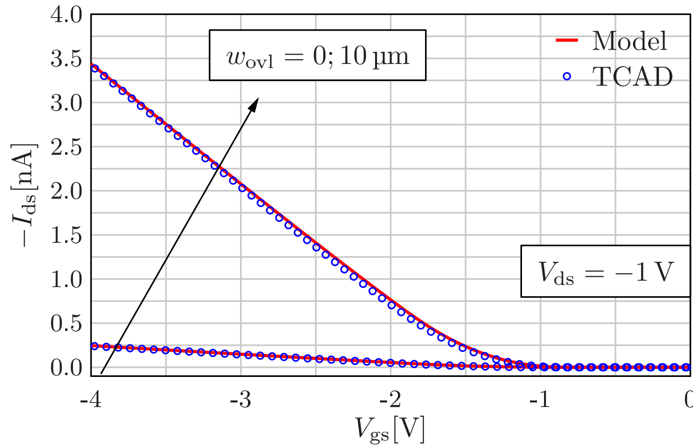

Figure 6.29.: Transfer curves of a coplanar OTFT as simulated in a 3D simulation by Sentaurus TCAD at $V_{ds} = -1\,V$ (blue symbols) in comparison to the compact model (solid red lines). The transistor has a channel length of $L_{ch} = 20\,\mu m$ and consists of one source/drain finger and a varying overlap width w_{ovl} beyond the finger. The compact model is fitted to the different overlap widths only by a variation of δ_{fit}. For $w_{ovl} = 10\,\mu m$, a value of $\delta_{fit} = 0.65$ is assumed. The setup of the TCAD simulation and the chosen values of the fitting parameters of the compact model are depicted in column (b) of Tab. 6.5.

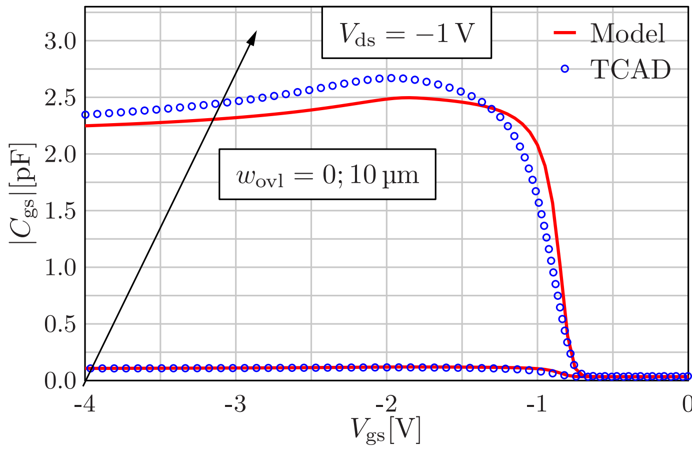

Figure 6.30.: Quasistatic capacitance C_{gs} of a coplanar single-finger OTFT. 3D Sentaurus TCAD simulation results (blue circles) are shown in comparison to the compact model (solid red lines) where the fringe width w_{ovl} is varied. The transistor has a channel length of $L_{ch} = 20\,\mu m$. The capacitances are plotted versus V_{gs} at a fixed drain voltage of $V_{ds} = -1\,V$. This plot corresponds to Fig. 6.29.

6.4 Low-Frequency Noise

6.4.1 Transistors Fabricated at CEA-LITEN

In this section, the noise model will be verified. Similarly as for the capacitance model, the first step is a fitting of the static DC curves. The verification is done based on bottom-contact top-gate transistors (staggered) as presented by Muhea et al. in ref. [76] which were fabricated at the Innovation Laboratory for New Energy Technologies and Nanomaterials (LITEN) at the Commissariat à l'Énergie Atomique et aux Énergies Alternatives (CEA) as explained in Chap. 5. Transistors with different channel lengths were fabricated. In Fig. 6.31, the transfer

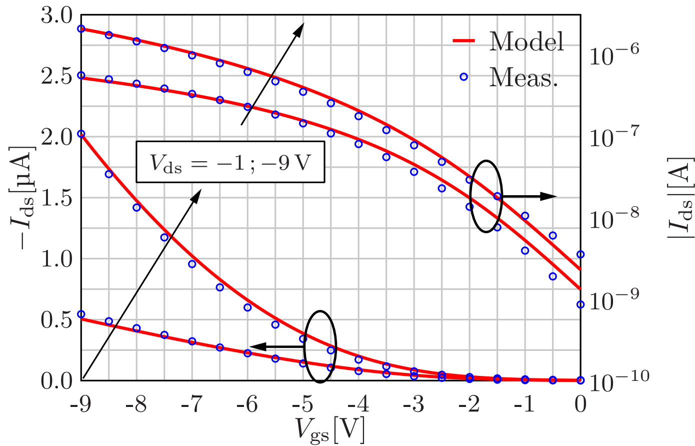

Figure 6.31.: Transfer curves of a staggered OTFT. The measurements (symbols) are compared to the results of the compact model (solid lines). The transistor has a channel length of $L_{ch} = 20\,\mu m$. The measurements are taken from ref. [76].

curves of one of the transistors comprising a channel length of $L_{ch} = 20\,\mu m$ are depicted. The measurements are compared to the compact model. It can be seen that a reasonable agreement is obtainable. Due to the large gate-dielectric thickness of approx. 800 nm the electrostatic control of the gate over the channel is poor. The transistors exhibit sub-threshold swings of about 2500 mV/dec which might be unacceptable for practical applications but for the noise study, the transistor exhibit excellent characteristics. In Fig. 6.32, the output curves of the same transistor as mentioned before are shown. It can be seen that the output and the transfer curves are consistent with each other meaning that they can both be fitted using one parameter set. Obviously, no pronounced hysteresis or short-term degradation effects took place.

In Tab. 6.6, some structural parameters of the transistors and the fitting parameters of the compact model are listed. In ref. [76], not every parameter of the transistors is reported. For example, the information about the gate-to-contact overlap length is missing. However, this is not of importance since the contact resistances are not pronounced in these transistors so

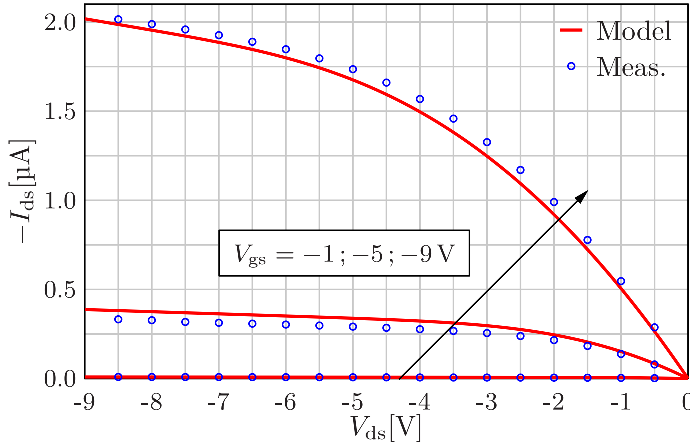

Figure 6.32.: Output curves of a staggered OTFT. The measurements (symbols) are compared to the results of the compact model (solid lines). The transistor has a channel length of $L_{ch} = 20\,\mu m$. The measurements are taken from ref. [76].

that no sheet resistance has to be assumed. Furthermore, for the noise model no capacitances or total charges are needed. Thus, the gate-to-contact overlap lengths are not important. Furthermore, some other information like the gate dielectric constant or the presence of fringe regions is not reported. However, this is not of importance either since by assuming a constant $\varepsilon_{r,diel}$ and neglecting fringe currents, the DC characteristics can be fitted tuning the mobility.

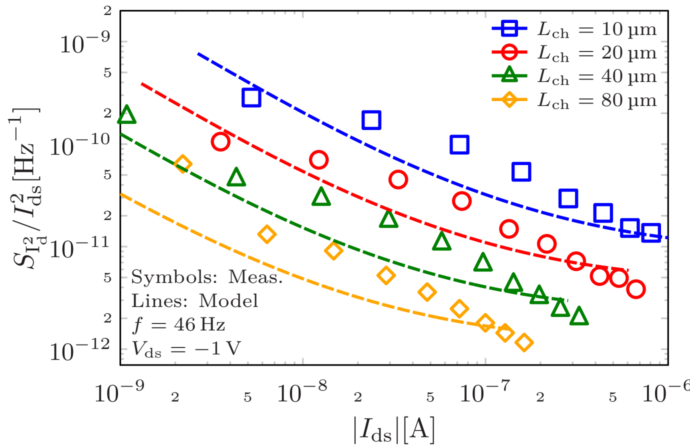

Figure 6.33.: Drain-current normalized noise of the staggered OTFTs presented in ref. [76] plotted against the drain current. The transistors have a channel width of $W_{ch,SD} = 1000\,\mu m$ and different channel lengths, as shown in the legend. The noise has been extracted from the plot versus frequency by probing the regression functions shown in Fig. 5.4 at a frequency of $f = 46\,Hz$. The drain-source voltage is $V_{ds} = -1\,V$. The measurements (symbols) are shown in comparison to the compact model (dashed lines).

Table 6.6.: Geometry values and parameters of the transistors presented in ref. [76]. The fitting parameters of compact model are shown as well.

Device Param.	$L_{ch} = 10\,\mu m$	$L_{ch} = 20\,\mu m$	$L_{ch} = 40\,\mu m$	$L_{ch} = 80\,\mu m$
$W_{contact}\,[\mu m]$	1000	1000	1000	1000
$L_{ov,GS}\,[\mu m]$	N/A	N/A	N/A	N/A
$L_{ov,GD}\,[\mu m]$	N/A	N/A	N/A	N/A
$t_{diel}\,[nm]$	800	800	800	800
$t_{osc}\,[nm]$	60	60	60	60
$w_{ovl}\,[\mu m]$	N/A	N/A	N/A	N/A
$N_{fing}\,[-]$	1	1	1	1
$d_{fing}\,[\mu m]$	-	-	-	-
$\varepsilon_{r,osc}\,[-]$	3	3	3	3
$\varepsilon_{r,diel}\,[-]$	2.2	2.2	2.2	2.2
Compact Param.				
$V_{T0}\,[V]$	-2.1	-2.1	-2.5	-2.6
$S_{obs}\,[mV/dec]$	2500	2500	2500	2500
$\kappa\,[cm^2 V^{-\beta-1} s^{-1}]$	1.05	1.05	1.05	1.07
$\beta\,[-]$	0	0	0	0
$\lambda\,[V^{-1}]$	0.06	0.04	0.04	0.04
$\lambda_{Tun}\,[nm]$	0.1	0.1	0.1	0.1
$N_t'\,[eV^{-1}\,cm^{-3}]$	$2 \cdot 10^{15}$	$2 \cdot 10^{15}$	$2 \cdot 10^{15}$	$2 \cdot 10^{15}$
$\alpha_c\,[V\,s\,C^{-1}]$	$1.6 \cdot 10^{9}$	$1.6 \cdot 10^{9}$	$1.6 \cdot 10^{9}$	$1.6 \cdot 10^{9}$
$\sigma\,[-]$	0.97	0.97	0.97	0.97

In Fig. 6.33, the drain-current-normalized noise is depicted at a drain-source voltage of $V_{ds} = -1\,V$ which causes the transistors to be operated mainly in the linear regime of operation. The measurement results are compared to the results of the compact model. As described in Sec. 5.3, the noise is extracted from the frequency spectrum by applying regression functions for the various bias points at which the noise has been measured. Then, the regression functions are probed at a fixed frequency. It can be seen in Fig. 6.33 that the compact model has a reasonable agreement with the measurement data. However, there are deviations in the medium current regime. The achievable agreement is better when comparing the compact model to the measurements at $V_{ds} = -9\,V$ which is depicted in Fig. 6.34. In principle, the compact model follows the trend $(g_m/I_{ds})^2$ but since the transistors have a poor sub-threshold swing of $S_{obs} = 2500\,mV/dec$ the compact model slightly deviates from this behavior. This is the reason why especially at low currents the compact-modeled noise does not exhibit the plateau that $(g_m/I_{ds})^2$ forms in Figs. 5.5 and 5.6. For all four transistors under investigation, the same fitting parameters of the noise model are used. This shows that the noise model scales well with the channel length.

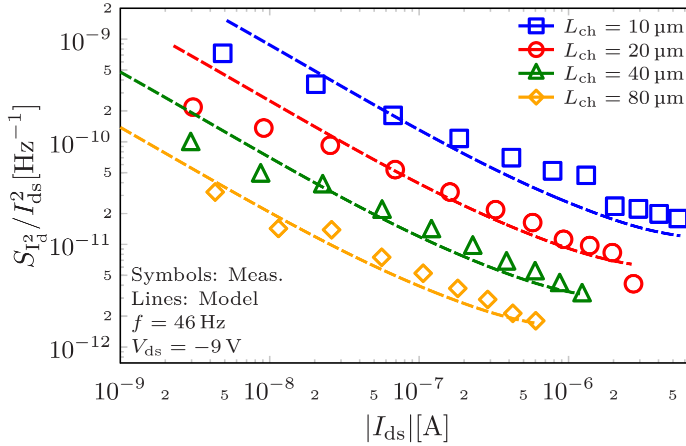

Figure 6.34.: Drain-current normalized noise of the staggered OTFTs presented in ref. [76] plotted against the drain current. The plot shows the same as Fig. 6.33 but at $V_{ds} = -9\,V$. The measurements (symbols) are compared to the compact model (dashed lines).

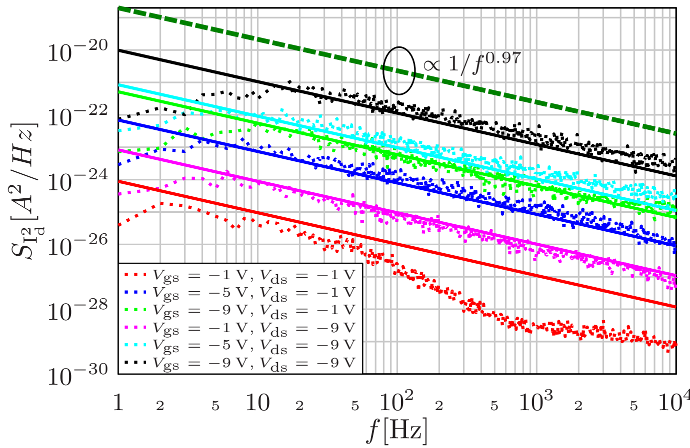

Figure 6.35.: Drain-current normalized noise of the staggered OTFT with $L_{ch} = 10\,\mu m$ presented in ref. [76] plotted against the frequency. The measurements (dotted lines) are shown in comparison to the compact model results (solid lines) at different gate-source and drain-source voltages. The exponent of the frequency is assumed as 0.97 such that the noise follows a $1/f^{\sigma}$ trend. Such a reference curve is depicted (dashed line).

In Fig. 6.35, the noise is shown versus the frequency for one arbitrary transistor of the set. The noise is not normalized with respect to the drain current in this plot. Since the noise does not exhibit a perfect $1/f$ trend, the frequency is taken to the power of the exponent σ so that the noise follows a $1/f^{\sigma}$ trend. However, σ is very close to unity. In the compact model, a value of $\sigma = 0.97$ is assumed. The figure also shows a slope of this function as a reference. It can be seen that the slope agrees well with the measured slope. As explained in Chap. 5, the

compact model describes the noise as a charge-carrier-number fluctuation including correlated mobility fluctuations. In agreement with [39], these correlated mobility fluctuations are mainly dominant at higher drain-source currents. Thus, the Coulomb scattering coefficient can be used to tune the shape of the model curve at high currents.

6.4.2 Transistors Fabricated at the MPI

In this section, the noise model is verified for transistors fabricated at the Max Planck Institute (MPI) for Solid State Research. Anticipating the results, it can be said that the transistors show an unexpected noise behavior which cannot be captured by a model, yet. OTFTs were fabricated in the bottom-gate bottom-contact (coplanar) device architecture using the process described in Sec. 1.4.1. Prior to the verification of the noise model, the DC characteristics were fitted using the charge-based DC model incorporating the non-linear contact resistances at the source and the drain [47]. DPh-DNTT is employed as the organic semiconductor. The

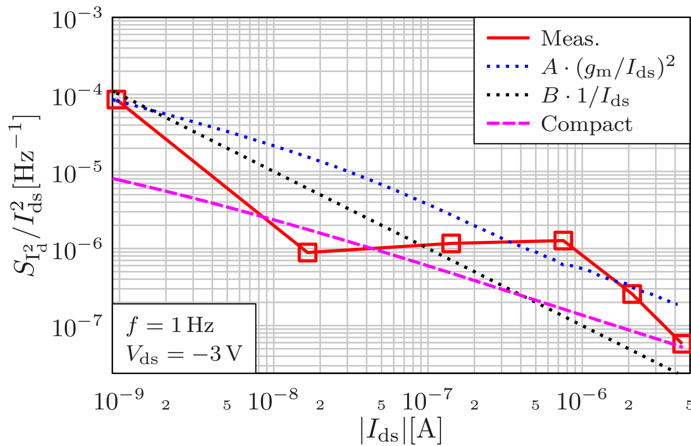

Figure 6.36.: Drain-current normalized noise of coplanar OTFTs with a $W_{ch,SD}/L_{ch}$ ratio of 100 µm/40 µm plotted against the drain current. The average of 19 measured transistors is shown. The noise is plotted at a drain-source voltage of $V_{ds} = -3\,\text{V}$. The measurements (solid red line with symbols) are shown in comparison to $(g_m/I_{ds})^2$ (dotted blue line) and $1/I_{ds}$ (dotted black line), each multiplied by a constant. The results of the compact model are shown as well (dashed magenta-colored line).

flexible substrate contains several areas in which the TFTs are grouped. Among them are 130 nominally identical transistors with a $W_{ch,SD}/L_{ch}$ ratio of 100 µm/40 µm and 130 nominally identical transistors with a $W_{ch,SD}/L_{ch}$ ratio of 100 µm/20 µm. The transistors consist of one single source/drain finger. Fringe regions are not paid special attention to and their influence is captured in terms of an increased mobility [60]. In each of the two areas, several transistors were measured. Static DC transfer and output characteristics were measured and the noise was determined using the noise measurement equipment by the AdMOS GmbH in Frickenhausen,

Table 6.7.: Geometry values and parameters of the fabricated coplanar organic transistors. The fitting parameters of compact model are shown as well.

Param.	$L_{\text{ch}} = 20\,\mu\text{m}$	$L_{\text{ch}} = 40\,\mu\text{m}$
$W_{\text{contact}}\,[\mu\text{m}]$	100	100
$L_{\text{ov,GS}}\,[\mu\text{m}]$	5	5
$L_{\text{ov,GD}}\,[\mu\text{m}]$	5	5
$t_{\text{diel}}\,[\text{nm}]$	7	7
$t_{\text{osc}}\,[\text{nm}]$	20	20
$w_{\text{ovl}}\,[\mu\text{m}]$	N/A	N/A
$N_{\text{fing}}\,[-]$	1	1
$d_{\text{fing}}\,[\mu\text{m}]$	-	-
$\varepsilon_{\text{r,osc}}\,[-]$	9	9
$\varepsilon_{\text{r,diel}}\,[-]$	5.37	5.37
Compact Param.		
$V_{\text{T0}}\,[\text{V}]$	-1.02	-1.02
$S_{\text{obs}}\,[\text{mV/dec}]$	80	90
$\kappa[\text{cm}^2\text{V}^{-\beta-1}\text{s}^{-1}]$	1.5	1.75
$\beta[-]$	0.85	0.78
$\lambda[\text{V}^{-1}]$	0.03	0.03
$\eta[-]$	1.07	1.06
$\theta[-]$	1.5	1.5
$d_{\text{m}}\,[\text{nm}]$	2	2
$d_{\text{B}}\,[\text{nm}]$	0.6	0.6
$\lambda_{\text{Tun}}\,[\text{nm}]$	0.1	0.1
$N'_{\text{t}}\,[\text{eV}^{-1}\,\text{cm}^{-3}]$	$3 \cdot 10^{22}$	$3 \cdot 10^{22}$
$\alpha_{\text{c}}[\text{V}\,\text{s}\,\text{C}^{-1}]$	$5 \cdot 10^{5}$	$5 \cdot 10^{5}$
$\sigma[-]$	0.97	0.97

Germany. The geometric and material parameters of the transistors as well as the fitting parameters of the compact model are depicted in Tab. 6.7 where d_{m} is the thickness of the accumulation channel and d_{B} is a fitting parameter in the non-linear injection model for coplanar transistors representing the distance from the gate dielectric to the position where the representative barrier is located [47]. Similarly as for the CEA-LITEN devices presented above, the noise versus the current is obtained by converting the noise spectrum versus frequency. The noisy shape of the power spectral density (PSD) is smoothed by removing outliers and the noise is multiplied by the frequency at each data point. Then, the noise is averaged over a frequency range of $10\,\text{Hz} < f < 20\,\text{Hz}$. Due to the multiplication by the frequency the resulting average can be interpreted as the noise at a frequency of $f = 1\,\text{Hz}$. This procedure is slightly different from the method using regression functions but it leads to qualitatively similar results.

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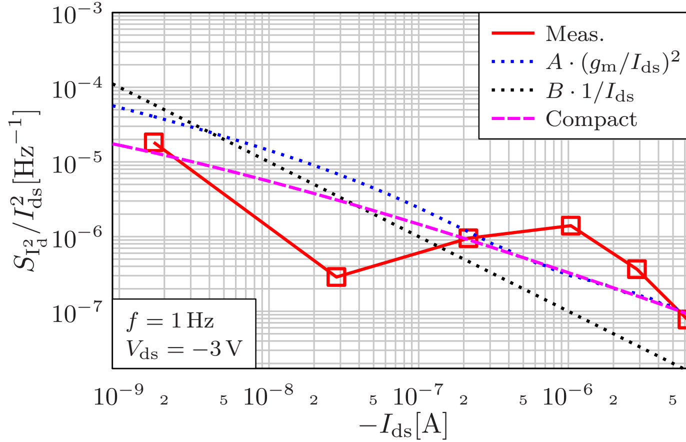

Figure 6.37.: Drain-current normalized noise of coplanar OTFTs with a $W_{ch,SD}/L_{ch}$ ratio of 100 µm/20 µm plotted against the drain current. The average of 21 measured transistors is shown. The noise is plotted at a drain-source voltage of $V_{ds} = -3\,\text{V}$. The measurements (solid red line with symbols) are shown in comparison to $(g_m/I_{ds})^2$ (dotted blue line) and $1/I_{ds}$ (dotted black line), each multiplied by a constant. The results of the compact model are shown as well (dashed magenta-colored line).

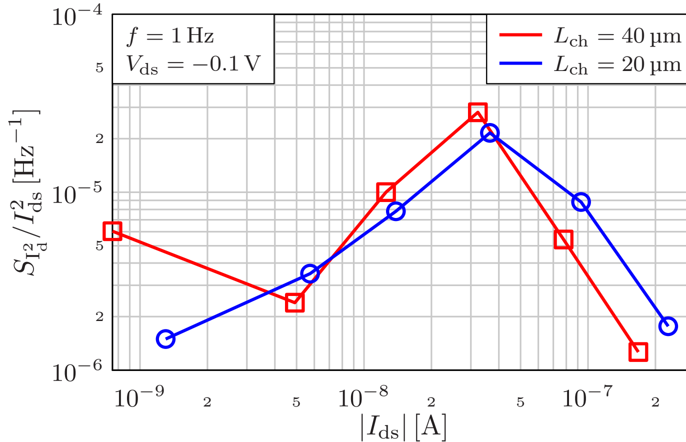

Figure 6.38.: Drain-current normalized noise of coplanar OTFTs with a $W_{ch,SD}/L_{ch}$ of 100 µm/40 µm (red line) and $W_{ch,SD}/L_{ch}$ of 100 µm/20 µm (blue line) plotted against the drain current. The average of 19 (21) measured transistors is shown. The noise is plotted at a drain-source voltage of $V_{ds} = -0.1\,\text{V}$.

In Fig. 6.36, the drain-current normalized noise of the transistors with the $W_{ch,SD}/L_{ch}$ ratio of 100 µm/40 µm is depicted at $V_{ds} = -3\,\text{V}$. The average noise of the 19 measured transistors was calculated and divided by the average current squared. Furthermore, the plot shows the trends $(g_m/I_{ds})^2$ and $1/I_{ds}$, each multiplied by a constant. As explained in Sec. 5.3, such a plot can assist in determining the dominant noise mechanism. It can be seen that the measured

noise does not follow the $(g_m/I_{ds})^2$ or the $1/I_{ds}$ trends. The measured noise does not meet the expectations in the sense that it exhibits an inflection point at moderate currents. The plot also shows the results of the compact model which assumes the carrier-number fluctuations. It can be seen that the model follows a similar trend as the $(g_m/I_{ds})^2$ curve and cannot reproduce the pronounced non-linearity of the measured noise. The same behavior is revealed when investigating the transistors with the shorter channel lengths as depicted in Fig. 6.37. Here, the non-linear behavior of the noise-versus-current curve is even more pronounced. The problematic behavior occurs not only at large absolute values of V_{ds} but also at small values. In Fig. 6.38, the drain-current-normalized noise of the transistors of the two different areas on the substrate is shown in comparison to each other at $V_{ds} = -0.1\,\text{V}$. It can be seen that the noise exhibits a highly non-linear shape. As explained before, the noise model cannot capture such a trend.

The observations so far show that the noise in these transistors cannot be captured by the standard theory. As a consequence, a full compact model for the noise description of these transistors cannot be provided, yet. In the following, possible reasons for the trends are discussed by observing the DC characteristics of the transistors and identifying deviations from the expected behavior. Since the two sets of transistors with the different $W_{ch,SD}/L_{ch}$ ratios show the same kind of behavior, the analysis will be performed based on the transistors with the $W_{ch,SD}/L_{ch}$ ratio of 100 µm/40 µm.

Output characteristics

A first and important investigation targets on the current output characteristics of the OTFTs. The shape of the output characteristics provides information on whether contact resistances are important [47]. In Fig. 6.39, the measured output curves of the transistors with the $W_{ch,SD}/L_{ch}$

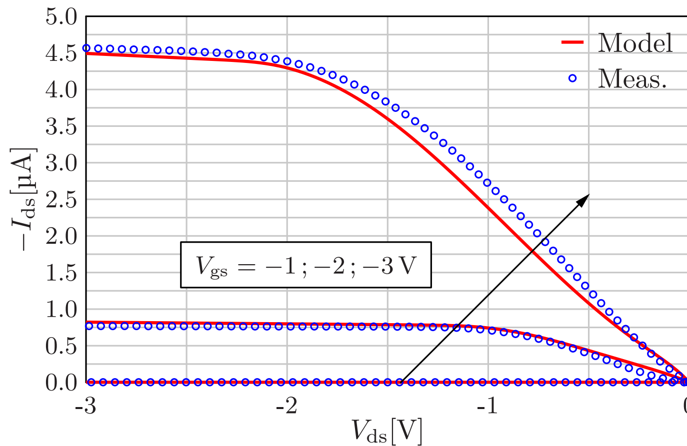

Figure 6.39.: Output characteristics of coplanar OTFTs with a $W_{ch,SD}/L_{ch}$ ratio of 100 µm/40 µm. The average of 19 measured transistors (blue circles) is shown at different gate-source voltages in comparison to the compact model results (solid red lines).

ratio of 100 µm/40 µm are depicted in comparison to the results of the compact model. It can be seen that the curves exhibit a non-linear behavior at low absolute values of the drain-source voltage. This S-shape effect is a hint for the presence of non-negligible contact resistances [47]. It might be expected that the contact resistances are of importance only at transistors with small channel lengths but the measurements reveal that these coplanar transistors obviously suffer from comparatively high contact resistances which are, however, more pronounced in the linear regime of operation [47]. The presence of contact resistances will lead to additional noise components [93, 94].

Transfer Characteristics

Another investigation targets on the transfer characteristics. In Fig. 6.40, the transfer characteristics of the transistors are shown in logarithmic and linear scale. Measurements are compared to the compact model. The transistors exhibit sub-threshold swings of approx. 90 mV/dec which can be understood as a hint for a comparatively low number of traps.

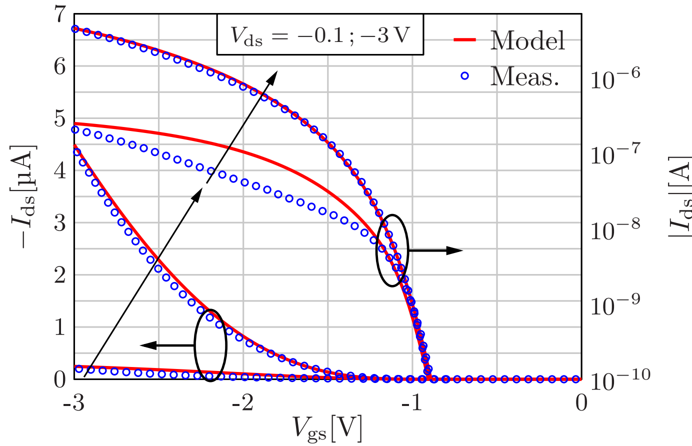

Figure 6.40.: Transfer characteristics of coplanar OTFTs with a $W_{ch,SD}/L_{ch}$ of 100 µm/40 µm. The average of 19 measured transistors (blue circles) is shown at different gate-source voltages in comparison to the compact model results (solid red line).

While the transfer curves recorded at $V_{\mathrm{ds}} = -3\,\mathrm{V}$ show a behavior as can be expected the transfer curves at $V_{\mathrm{ds}} = -0.1\,\mathrm{V}$ show an unusual behavior. Observing the curves in logarithmic scale, it can be seen that the transfer curve at low absolute value of V_{ds} shows a nearly linear trend in a range of $-2.5\,\mathrm{V} \leq V_{\mathrm{gs}} \leq -1.5\,\mathrm{V}$. A curve exhibiting a linear shape in a diagram with logarithmic y-axis has an exponential shape when plotted in the linear scale. The observed behavior is untypical since in the V_{gs} range mentioned, it could be expected that the transistor shows a linear current-voltage dependence. It can be seen that the compact model only agrees well with the measurements ar large absolute values of V_{ds}.

Transconductance

An observation of the transfer characteristics alone does not provide a full picture of the transistors' behavior. The derivative of the transfer curve, i.e. the transconductance is of importance, as well. In Fig. 6.41, the transconductance at a low absolute value of V_{ds} is shown.

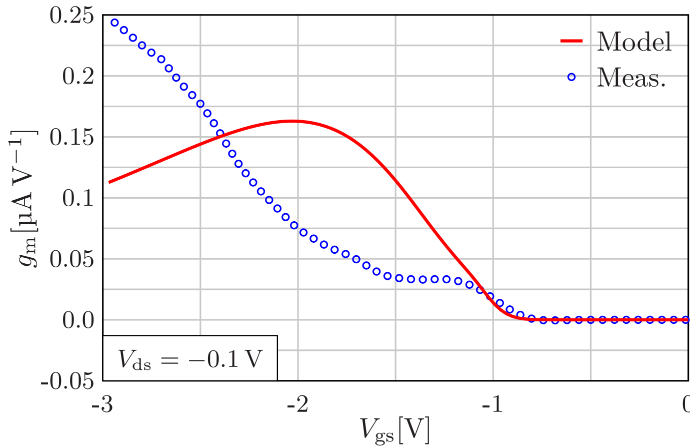

Figure 6.41.: Transconductance of coplanar OTFTs with a $W_{\mathrm{ch,SD}}/L_{\mathrm{ch}}$ ratio of 100 µm/40 µm at $V_{\mathrm{ds}} = -0.1\,\mathrm{V}$. The average transfer curves of 19 measured transistors as shown in Fig. 6.40 are smoothed using a filter function in Matlab [71] and then, the transconductance is numerically calculated. The measurements (blue circles) are compared to the compact model (solid red lines). The compact model fails to reproduce the measurements.

The transconductance as extracted from the measurements is compared to that of the compact model. Since the measured transfer curves exhibit several non-linearities and humps, the average transfer curve was smoothed by a filter function in Matlab. The transconductance was then calculated based on the smoothed transfer curve. It can be seen that the transconductance at $V_{\mathrm{ds}} = -0.1\,\mathrm{V}$ exhibits a rather untypical behavior which cannot be captured at all by the compact DC model. With V_{gs} increasing from zero towards larger absolute values, the transconductance exhibits several non-linearities. When leaving the sub-threshold regime at approx. $V_{\mathrm{gs}} = -0.9\,\mathrm{V}$, the transconductance sharply increases and then it forms a plateau. However, at approx. $V_{\mathrm{gs}} = -1.5\,\mathrm{V}$, the transconductance starts increasing again. This be-

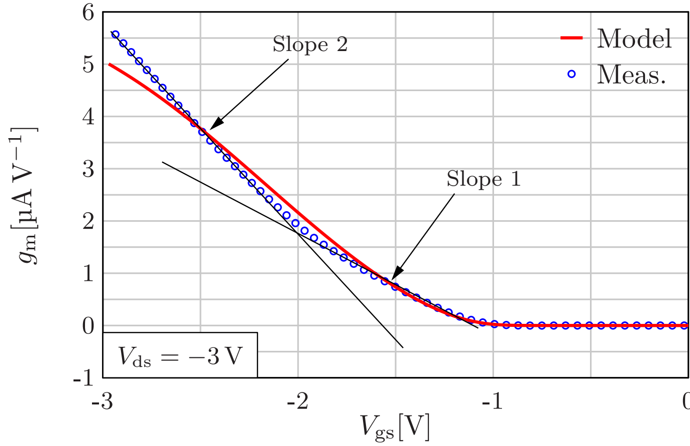

Figure 6.42.: Transconductance of coplanar OTFTs with a $W_{ch,SD}/L_{ch}$ ratio of $100\,\mu m/40\,\mu m$ at $V_{ds} = -3\,V$. The average transfer curves of 19 measured transistors as shown in Fig. 6.40 are smoothed using a filter function in Matlab [71] and then, the transconductance is numerically calculated. The measurements (blue circles) are compared to the compact model (solid red lines). The black lines are guides for the eye in order to emphasize the different slopes of the measurement curve.

havior is unusual since a conventional long-channel OTFT would exhibit a rather constant transconductance in the entire linear regime of operation such as depicted in Fig. 6.8. A similar behavior of the transconductance has been reported in refs. [95, 96] for nanocrystalline silicon TFTs. The authors explain the behavior by means of a high density of defect states (traps) in the semiconductor. Utilizing finite-element simulations they show that a high density of trap states in the bandgap of the semiconductor causes a continuous filling of the trap states with increasing gate-source voltage. If the density of trap states is large in comparison to the density of mobile states, an increase in the gate-source voltage results in an increase of both the density of free and trapped charge carriers. If the gate-source voltage is chosen so high that all of the trap states are filled, the transconductance will follow the expected trend again and saturate to a constant value in the linear regime of operation. Even if the transistors under investigation in this thesis are different from the nanocrystalline silicon TFTs presented in refs. [95, 96], the conclusions drawn by the authors may also be correct for the OTFTs. The problematic behavior of the transistors in the transconductance and the noise is likely related to traps.

In Fig. 6.42, the transconductance at a large absolute value of V_{ds} is depicted. Also in this case, the average transfer curve of the 19 transistors was calculated, smoothed out by a filter function and afterwards numerically derived with respect to V_{gs}. It can be seen that in the on-state, the transconductance exhibits two different slopes. In the range $-2\,V \leq V_{gs} \leq -1\,V$ which corresponds to the saturation regime of operation, the slope is less steep than in the range $-3\,V \leq V_{gs} \leq -2\,V$ which corresponds to the linear regime. According to the standard MOS-

FET model, an ideal transistor can be expected to have a quadratic dependence on V_{gs} in the saturation regime and a linear dependence on V_{gs} in the linear regime of operation [5, 25]. Thus, the transconductance of this standard model shows a linear trend in the saturation regime of operation and is simply constant in the linear regime of operation. This theory agrees well with the findings of the long-channel TCAD simulations as shown in Fig. 6.8. There, the transconductance at large absolute values of V_{ds} is indeed linear in the V_{gs} range where the transistor is operated in saturation and it saturates to a constant value. However, it can be observed that the transconductance shown in Fig. 6.42 does not obey this theory. By contrast, the slope of the transconductance becomes even steeper when the transistor enters the linear regime of operation. The compact model does not capture the two different slopes but the overall agreement between compact model and measurements is much better than at the plot at a low absolute value of V_{ds}.

Discussion

The above-explained investigations reveal that the transistors do not show a typical behavior. A possible explanation for this behavior may be non-linear contact resistances [97]. However, it can be expected that the influence of these contact resistances is more pronounced in the linear regime of operation, i.e. at low absolute values of V_{ds} [97]. In the OTFTs investigated in this work, the non-linear behavior of the noise-versus-I_{ds} curves occurs also at large absolute values of V_{ds}. Furthermore, OTFTs exhibit slightly exponentially-shaped transfer characteristics due to the disorder of the molecules of the organic semiconductor [28]. This degree of disorder can be incorporated into a transistor model by defining a voltage-dependent power-law mobility [28] which is also performed in the DC model that serves as a basis for the work presented here [36]. In order to fit the DC characteristics of the transistors under investigation in this section, comparatively high values have to be assumed for the power-law exponent β. This could be interpreted in such a way that there is a high degree of energetic disorder in the organic semiconductor [28] or that there is a high field-dependence of the mobility such as described in ref. [98] as a Poole-Frenkel mobility.

In the literature, there have been reported other types of transistors that exhibit a non-linear trend in the noise-versus-I_{ds} curves. In ref. [99], the noise in cadmium-selenide TFTs is investigated. Two sets of transistors are fabricated: one set on a silicon substrate and one set on a glass substrate. Whereas the TFTs fabricated on the silicon substrate show a more textbook-like noise the transistors fabricated on the glass substrate exhibit a non-linear trend in the noise-versus-I_{ds} curves. The curves resemble the noise spectra of the transistors under investigation in this thesis to a certain degree. The authors of ref. [99] assume that local states (i.e. traps) are the reason for this behavior. Observing the transconductance of the transistors under investigation in this work, it is reasonable to assume traps as one of the main contributors to the observed behavior [95, 96].

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6.4.3 TCAD Simulation

In Sec. 5.4.4, a compact model for the calculation of the noise originating from bulk mobility fluctuations is presented. The fabricated transistors under investigation do not exhibit this type of noise but by means of a TCAD simulation, the bulk mobility fluctuations can be verified, as well.

Staggered Transistors

The TCAD simulation of a staggered OTFT comprising a channel length of 20 µm as depicted in column (b) of Tab. 6.2 was extended by the setup of a bulk flicker noise. In TCAD, this noise is also denoted as flicker generation-recombination noise and it is the type of noise that resembles the bulk mobility fluctuations [50]. A fitting parameter similar as the Hooge parameter [39] can be set and two time constants. This Hooge parameter is set to $\alpha_{\mathrm{H,TCAD}} = 2 \cdot 10^{-3}$ and the time constants are set to $\tau_0 = 1 \times 10^{-6}$ s and $\tau_1 = 1$ s, respectively. With increasing frequency, the noise transits from a constant behavior to a $1/f$ behavior and afterwards to a $1/f^2$ behavior. The time constants determine the transition frequencies. The time constants are chosen such that in the observed frequency range, the noise follows a $1/f$ trend. The Hooge parameter in the TCAD setup does not represent exactly the Hooge parameter in the compact model since the noise in TCAD is described by an expression slightly different from the Hooge mobility-fluctuation noise [50]. In Fig. 6.43, the noise as simulated by Sentaurus TCAD is

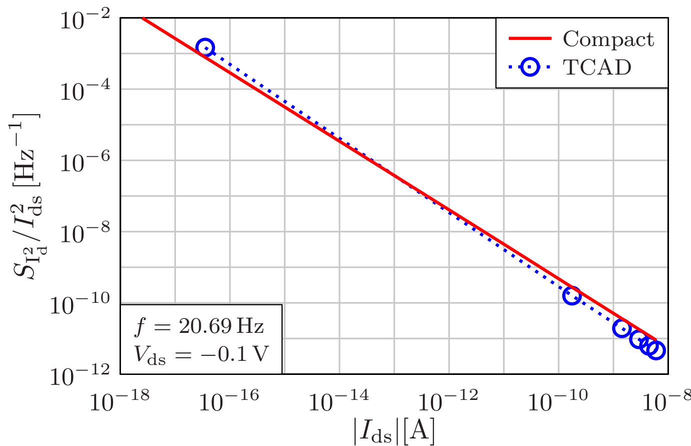

Figure 6.43.: Drain-current normalized noise of a staggered OTFT at a drain-source voltage of $V_{\mathrm{ds}} = -0.1$ V and a frequency of $f = 20.69$ Hz. The results of a TCAD simulation (dotted blue line) are compared to the results of the compact model (solid red line). The transistor has a channel length of $L_{\mathrm{ch}} = 20$ µm. The setup of the TCAD simulation and the fitting parameters of the DC compact model are depicted in column (b) of Tab. 6.2. In the compact model, the empirical Hooge parameter is set to $\alpha_{\mathrm{H}} = 3 \cdot 10^{-4}$.

compared to the compact model at a drain-source voltage of $V_{\mathrm{ds}} = -0.1$ V. It can be seen that there is a good overall agreement. The slope of the two curves slightly deviate but the agreement over the entire range of drain-source voltages is good. Furthermore, it can be seen

that the compact model follows a $1/I_{ds}$ trend since with every decade of increase in the drain current, the noise is decreased by one decade. This is in agreement with the postulation that the bulk mobility noise follows a $1/I_{ds}$ trend [76]. In Fig. 6.44, the TCAD-simulated noise is

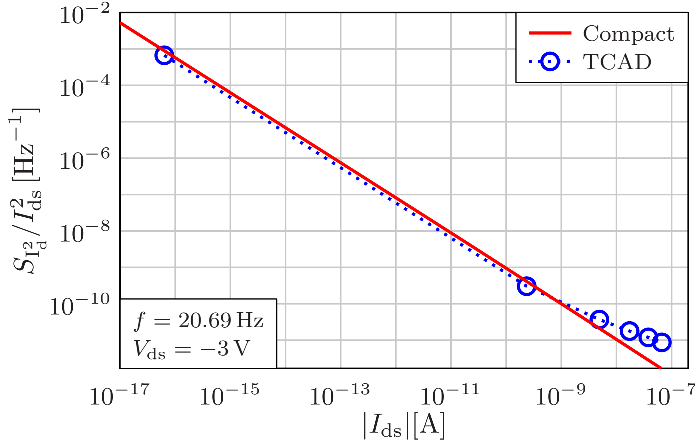

Figure 6.44.: Drain-current normalized noise of a staggered OTFT at a drain-source voltage of $V_{ds} = -3\,\mathrm{V}$ and a frequency of $f = 20.69\,\mathrm{Hz}$. The results of a TCAD simulation (dotted blue line) are compared to the results of the compact model (solid red line). The transistor has a channel length of $L_{ch} = 20\,\mu\mathrm{m}$. The setup of the TCAD simulation and the fitting parameters of the DC compact model are depicted in column (b) of Tab. 6.2. In the compact model, the empirical Hooge parameter is set to $\alpha_H = 2 \cdot 10^{-5}$.

compared to the compact model for the case of a drain-source voltage of $V_{ds} = -3\,\mathrm{V}$. At low currents, the agreement between the compact model and the TCAD simulation results is good but at higher currents, the TACD simulation results do not follow a clear $1/I_{ds}$ trend.

Coplanar Transistors

Equally as for the staggered transistors, a TCAD simulation of a coplanar OTFT was conducted. The transistor has a channel length of $L_{ch} = 20\,\mu\mathrm{m}$ and the setup of the simulation along with the fitting parameters of the DC compact model is depicted in Tab. 6.5. The TCAD simulation of the noise was set up just as for the staggered transistors. In Fig. 6.45, the drain-current-normalized noise of the coplanar transistor is shown at a drain-source voltage of $V_{ds} = -0.1\,\mathrm{V}$. The TCAD simulation results are compared to the compact model. It can be seen that there is a very good agreement. However, as can be seen at Fig. 6.46, at large currents, the noise at a drain-source voltage of $V_{ds} = -3\,\mathrm{V}$ does not follow the $1/I_{ds}$ trend any longer, similarly as for the staggered OTFTs.

Even if the noise model describing the bulk mobility fluctuations cannot be verified by means of measurements, it can at least be shown that the noise model indeed follows the proclaimed $1/I_{ds}$ trend. Furthermore, a reasonable agreement with TCAD simulations in both transistor architectures is achievable. However, it has to be emphasized that this type of noise simulation

in TCAD is not a physical simulation and does not perfectly represent the bulk mobility fluctuations described by the Hooge model. Thus, it is regarded as legitimate to choose different values for the Hooge parameter in the compact model for the different drain-source voltages. In principle, it could be expected to have a voltage-independent Hooge parameter in the model.

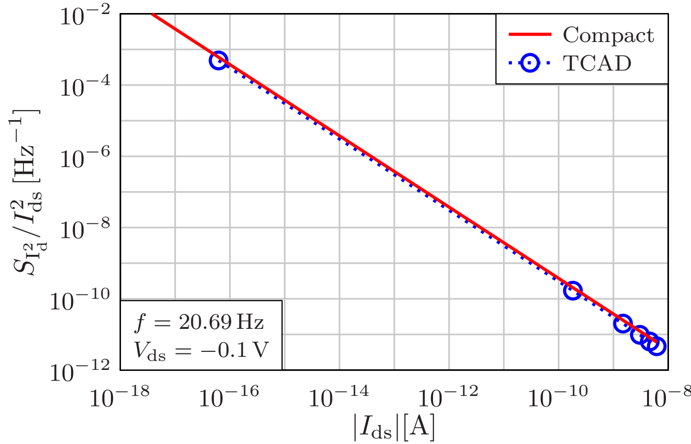

Figure 6.45.: Drain-current normalized noise of a coplanar OTFT at a drain-source voltage of $V_{\mathrm{ds}} = -0.1\,\mathrm{V}$ and a frequency of $f = 20.69\,\mathrm{Hz}$. The results of a TCAD simulation (dotted blue line) are compared to the results of the compact model (solid red line). The transistor has a channel length of $L_{\mathrm{ch}} = 20\,\mu\mathrm{m}$. The setup of the TCAD simulation and the fitting parameters of the DC compact model are depicted in column (a) of Tab. 6.5. In the compact model, the empirical Hooge parameter is set to $\alpha_{\mathrm{H}} = 2 \cdot 10^{-4}$.

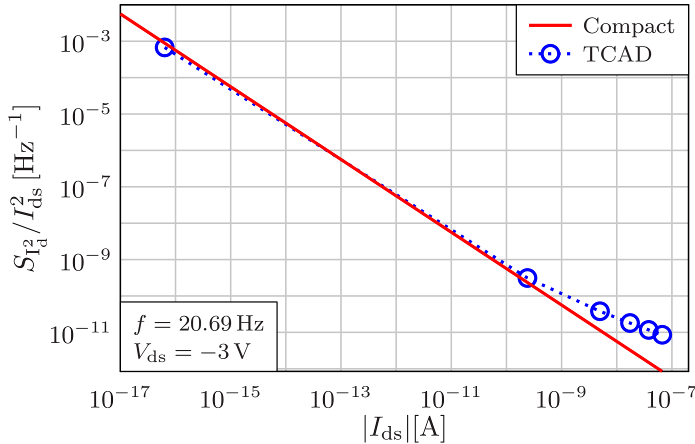

Figure 6.46.: Drain-current normalized noise of a coplanar OTFT at a drain-source voltage of $V_{\mathrm{ds}} = -3\,\mathrm{V}$ and a frequency of $f = 20.69\,\mathrm{Hz}$. The results of a TCAD simulation (dotted blue line) are compared to the results of the compact model (solid red line). The transistor has a channel length of $L_{\mathrm{ch}} = 20\,\mu\mathrm{m}$. The setup of the TCAD simulation and the fitting parameters of the DC compact model are depicted in column (a) of Tab. 6.5. In the compact model, the empirical Hooge parameter is set to $\alpha_{\mathrm{H}} = 1 \cdot 10^{-5}$.

CHAPTER 7

Model Extensions

7.1 Introductory Information

In this chapter, extensions to the quasistatic charge and capacitance model are described. The model described in Chap. 4 allows for an accurate reproduction of the measured and simulated quasistatic capacitances of staggered and coplanar transistors which are subject to the following restrictions:

- The frequencies of the applied AC signals are small so that the charges in the transistor respond immediately to a change in the voltages. This is the condition for a quasistatic operation [38].
- The contact resistances have to be much smaller than the intrinsic channel resistance so that they can be neglected. This is typically the case for long-channel transistors since the DC current of the intrinsic carrier channel is inversely proportional to L_{ch} as can be seen in the DC equation of the model (Eq. (2.21)). If the channel lengths are decreased, the intrinsic carrier channel could conduct a larger current and thus the role of contact resistances becomes more important [18].

These conditions will not be fulfilled for every use case. For instance, real electric circuits such as amplifiers consisting of transistors are not limited to only low frequencies. Furthermore, the contact resistance cannot be neglected in transistors the channel lengths of which are significantly decreased in order to achieve a higher switching speed. Such a channel-length reduction leads to a reduction of the total gate area and thus to a smaller amount of charges that are stored in the transistor which is a pre-requisite for a transistor with high-speed capabilities. Furthermore, which will be shown in the course of this chapter, contact resistance alter the density of accumulated charges at the source/drain end of the transistor. In this chapter, different approaches are provided to include those effects. The chapter is organized in the following way: Firstly, the high-frequency behavior of long-channel transistors is described by the channel segmentation approach which is valid for transistors comprising relatively small

contact resistances. Secondly, the model for the total charges in the quasistatic case is enhanced to capture the influence of contact resistances on the AC behavior of the transistors. Thirdly, an empirical closed-form model for the high-frequency behavior of short-channel transistors is shown. In addition to the frequency and short-channel models, this chapter contains an investigation of the influence of the temperature on the DC behavior of the transistors.

7.2 Channel Segmentation

In this section, the channel segmentation model is presented and verified by means of measurements and TCAD simulation results.

7.2.1 Modeling

The assumption of a quasistatic operation is only valid at comparatively low frequencies. Transistors with large channel lengths suffer from a low channel conductivity and high capacitances. Hence, the propagation of charges along the channel is much slower for long-channel transistors in comparison to their short-channel counterparts. In ref. [40], the frequency-dependent capacitances of transistors with different channel lengths were measured. The measurement procedure is similar as described in Sec. 6.3.2.2. However, during this measurement the source and drain terminals were shorted and connected to the low-potential connector of the LCR meter while the gate electrode was connected to the high-potential connector. In Figs. 7.1 and 7.2, the measured capacitance C_{gg} and the conductance G_{gg} divided by the frequency, which is denoted as the loss, are displayed.

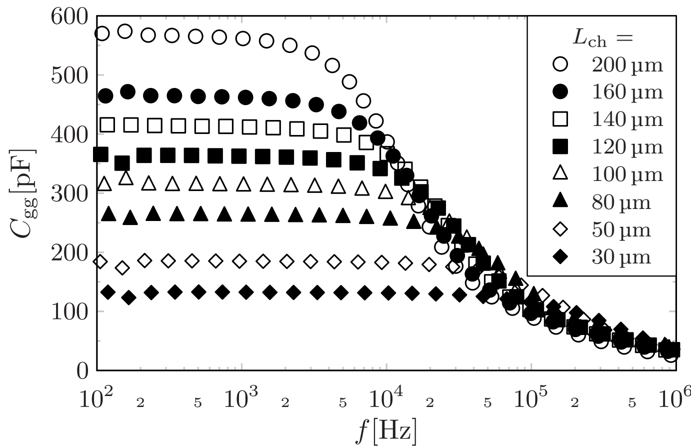

Figure 7.1.: Measured capacitance characteristics of transistors with different channel lengths versus frequency as presented in ref. [40]. The capacitance is extracted at a gate-source voltage of $V_{\mathrm{gs}} = -3\,\mathrm{V}$. Due to the shorting of the drain and source terminals, $V_{\mathrm{ds}} = 0\,\mathrm{V}$. The amplitude of the superimposed AC signal is 100 mV. The transistors have a channel width of $W_{\mathrm{ch,SD}} = 400\,\mathrm{\mu m}$.

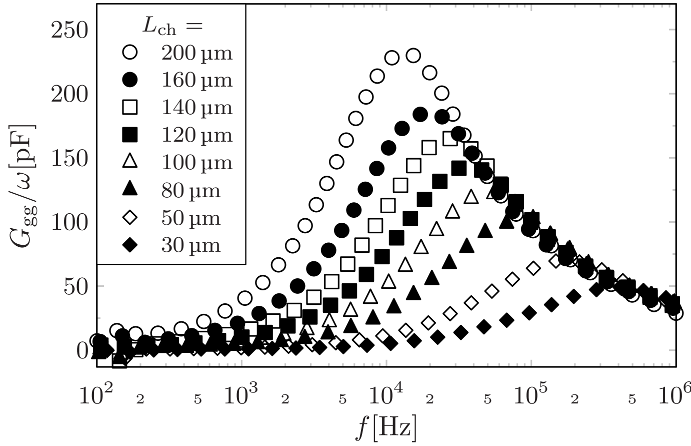

Figure 7.2.: Measured loss G_{gg}/ω, where ω is the angular frequency, of the same transistors as examined in Fig. 7.1. The data were presented originally in ref. [40].

It can be seen that the low-frequency capacitance of the transistors comprising large channel lengths is generally larger compared to the short-channel transistors. Furthermore, the drop of the capacitance with increasing frequency starts at significantly lower frequencies of several kilohertz for the transistors with large channel lengths. The transistor with the largest channel length ($L_{ch} = 200\,\mu m$), for example, shows a notable decrease its capacitance already at approximately 20 kHz whereas for the transistor with the shortest channel length ($L_{ch} = 30\,\mu m$), the decay becomes important at much higher frequencies of about 100 kHz.

Figure 7.3(a) shows a schematic cross section of a staggered OTFT where small sections of the intrinsic carrier channel are characterized by their resistance and their capacitance. The carrier channel of the transistor behaves similar to a distributed *RC* transmission line [64]. Since the propagation of charge carriers through this transmission line does not occur with infinite speed the transistor shows a non-quasistatic behavior which significantly deviates from the quasistatic case above a particular frequency. In order to capture this behavior and to enhance the compact model, the well-known model approach of the channel segmentation is applied [39]. This model describes a transistor as a series connection of several transistors where each of them represents only a small segment of the total channel. The sum of the channel lengths of these transistors is equal to the channel length of the whole transistor. In Fig. 7.3(b), the circuit symbol of a p-type transistor is shown and in Fig. 7.3(c), the series connection of transistors with interconnected gates is shown. This model approach is denoted as a macro model since it does not describe the time-dependent current by means of analytical equations but rather models one single device by an electronic substitute circuit that needs to be solved numerically, e.g. by a circuit simulator like Cadence Virtuoso [70].

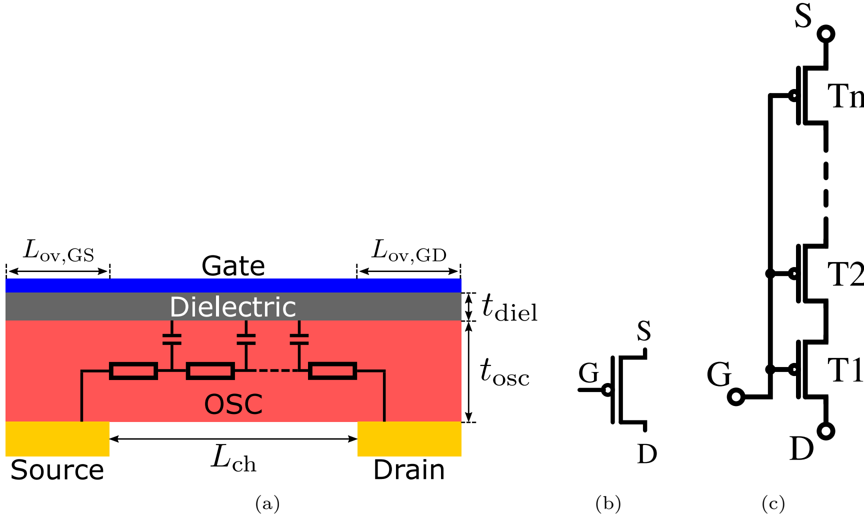

Figure 7.3.: (a) Schematic cross section of a staggered OTFT where small sections of the channel are depicted as resistor-capacitor segments. (b) Symbol of OTFT. (c) Circuit diagram of the transistor in (a) which is modeled by N transistors connected in series. The sum of the channel lengths of the N single transistors equals the channel length of the transistor in (b).

In contrast to the approach of a channel segmentation in a macro model, there is also the option of analytically calculating the impedance of the *RC* transmission line of the transistor. In the literature, this approach is described for different transistors such as single-crystalline silicon MOSFETs [100] or polycrystalline silicon TFTs [64]. In ref. [18], this approach is used for the description of non-quasistatic capacitances in OTFTs including contact resistances. The benefit of this approach is that analytical equations can be derived for the capacitances which are explicitly dependent on the frequency of the applied AC signal. This is beneficial for a reproduction of measured capacitances at an arbitrary frequency. For a circuit simulation, the model can be implemented in the hardware description language Verilog-A. Unfortunately, a Verilog-A model in SPICE simulations is not aware of the frequency of the AC input signal. In ref. [18], this problem is circumvented by passing the frequency as an external parameter to the model. The disadvantage of this procedure is that the model cannot be used in an AC sweep in the circuit simulation since for every new simulation, the model parameter would have to be updated. A further drawback of such an analytical solution is that the model can only be used for perfectly sinusoidal signals that are applied during an AC analysis. However, during a transient analysis such as described in refs. [101, 102], the voltages applied to the transistor terminals can have any arbitrary wave forms. In order for this model to properly account for that general case, the Fourier transform of the input signal would have to be calculated and the reaction of the system to every single frequency would have to be evaluated. As a consequence, the model in ref. [18] is not easily applicable to every kind of circuit simulation

despite its advantages pertaining to the fact that it presents a closed-form description. In order to overcome these difficulties, Valletta et al. developed a model for the large-signal non-quasistatic behavior of OTFTs which is based on the discretization of the current continuity equation based on a spline collocation method [103, 104]. The frequency dependence of the transistor currents are accounted for implicitly by the numerical integration that is performed in the Verilog-A code and thus this model provides a high flexibility. In this regard, this model resembles a macro model. In comparison to the channel segmentation model there is the advantage of a closer link to the physical effects that occur in the transistor but at the cost of a higher complexity of the model. Thus, the macro model incorporating the channel segmentation will be used in the following since it is easier to use and can directly be built in a SPICE simulator by interconnecting several instances of the Verilog-A model of a single transistor.

The channel segmentation model in this simple form is only suitable for transistors in which the contact resistances can be neglected (second condition in Sec. 7.1). Otherwise, the charge distribution in a transistor is altered which cannot easily be captured by the model without any modifications as will be discussed later.

7.2.2 Implementation in Verilog-A

In this section, it will be briefly outlined how the model is implemented in the hardware description language Verilog-A. The Verilog-A module of a single transistor contains the equations of both the compact DC model and the model for the total charges. Please recall that the total charges associated with the gate, the drain and the source are functions of the three terminal potentials:

$$Q_{\mathrm{g}} = -Q_{\mathrm{c}} = f_1\left(V_{\mathrm{g}}, V_{\mathrm{s}}, V_{\mathrm{d}}\right), \tag{7.1}$$

$$Q_{\mathrm{s}} = f_2\left(V_{\mathrm{g}}, V_{\mathrm{s}}, V_{\mathrm{d}}\right), \tag{7.2}$$

$$Q_{\mathrm{d}} = f_3\left(V_{\mathrm{g}}, V_{\mathrm{s}}, V_{\mathrm{d}}\right). \tag{7.3}$$

If any of the potentials V_{g}, V_{s} or V_{d} is changed, as a consequence the charges associated with the transistor terminals are changed. As explained in Chap. 3, the change in these charges results in charging or discharging currents:

$$i_{\mathrm{g}} = -\frac{\partial Q_{\mathrm{c}}}{\partial t}, \tag{7.4}$$

$$i_{\mathrm{s}} = \frac{\partial Q_{\mathrm{s}}}{\partial t}, \tag{7.5}$$

$$i_{\mathrm{d}} = \frac{\partial Q_{\mathrm{d}}}{\partial t}. \tag{7.6}$$

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In the Verilog-A code of the OTFT, these charging and discharging currents can be added to the DC currents by using the *ddt* operator [70]:

$$I_{\mathrm{g}} = -ddt\left(Q_{\mathrm{c}}\right), \tag{7.7}$$

$$I_{\mathrm{s}} = I_{\mathrm{s,DC}} + ddt\left(Q_{\mathrm{s}}\right), \tag{7.8}$$

$$I_{\mathrm{d}} = I_{\mathrm{d,DC}} + ddt\left(Q_{\mathrm{d}}\right), \tag{7.9}$$

$$I_{\mathrm{d,DC}} = -I_{\mathrm{s,DC}} \tag{7.10}$$

where $I_{\mathrm{d,DC}}$ and $I_{\mathrm{s,DC}}$ are calculated by the compact DC model. The usage of the *ddt* operator leads to a correct handling of the charging and discharging of the capacitive currents.

The channel-segmentation model could in principle be instantiated by interconnecting several instances of the single transistor model to a circuit. However, this procedure is inconvenient since the circuit schematics would become confusing with every single transistor being displayed as an interconnection of several transistors. In Verilog-A, there exists the possibility to create a netlist in a module and to define ports that are connected to the outer circuit. This is achieved by defining a parent module in the Verilog-A code which has three electrical ports for the gate, source and drain electrodes. In the same Verilog-A code, it is possible to define several other modules that can be called in the parent module. The module of the single transistor is implemented and in the parent module, several instances of this single transistor module are called and interconnected in a netlist.

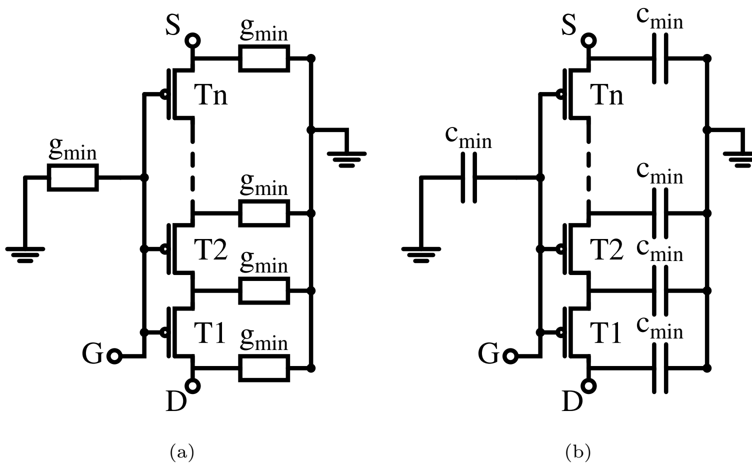

Figure 7.4.: Circuit schematic of several transistors interconnected in the channel-segmentation model. (a) In order to improve the convergence of the solver algorithm, Cadence Virtuoso automatically connects a small conductance g_{min} between each circuit node and ground during a DC and an AC analysis. (b) During a transient analysis, Cadence Virtuoso automatically connects each circuit node to ground by a capacitance c_{min} in order to improve convergence.

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One important point is to capture the gate-to-contact overlap capacitances only at the transistors T1 and Tn in Fig. 7.3(c). T1 is the only transistor in the circuit which has a gate-to-drain overlap region and accordingly, transistor Tn is the only transistor comprising a gate-to-source overlap region. The transistors along the channel region are computed without any overlap region. In the model, this is achieved by deactivating the contributions of the non-necessary gate-to-contact overlap capacitances in the single-transistor module.

When a circuit is simulated in Cadence Virtuoso, the non-linear circuit equations are solved numerically by the solver Spectre [70]. Cadence Virtuoso uses auxiliary methods to achieve a better convergence. In Fig. 7.4(a), a schematic of several transistors that are interconnected in a circuit is shown. As can be seen, each node of the circuit is connected to the ground level through a small conductance denoted as g_{min}. This procedure assists the solver in determining a convergent solution but at the cost of a reduced overall accuracy of the circuit. Such an auxiliary conductance is included automatically by Cadence Virtuoso if a DC or an AC analysis is performed. If, by contrast, a transient analysis is performed, Cadence Virtuoso uses small auxiliary capacitors that are connected between each node and the ground level, see Fig. 7.4(b). Without these capacitances no convergence can be achieved but they will diminish the accuracy of the circuit.

7.2.3 Verification

In this section, the verification of the channel-segmentation approach will be presented by means of AC measurements of OTFTs and by TCAD simulations. In addition, the compact model is used in a transient simulation and compared to the results of a transient simulation in TCAD.

7.2.3.1 AC Measurements

The data used for verification are the AC measurements of ref. [40]. The longest transistor presented has a channel length of $L_{\text{ch}} = 200\,\mu\text{m}$ which can be regarded as a long-channel transistor. The geometric values and material parameters of this transistor are depicted in Tab. 6.3. Similarly as for the verification of the quasistatic capacitances, the threshold voltage is regarded as a fitting parameter fluctuating due to the bias-stress-induced filling and emptying of traps [90]. During the AC measurements the drain and source terminals are shorted. The complex admittance $\underline{Y}$ is measured and according to Eqs. (6.7) and (6.8) the capacitance and the conductance between the two terminals are calculated. Due to the shorting of the drain and source terminals, the measured capacitance and conductance can be interpreted as C_{gg} and G_{gg}, respectively. However, in the simulations with Cadence Virtuoso, a better numerical stability is achieved if $V_{\text{ds}} \neq 0$. Therefore, the simulations presented in this work are computed at $V_{\text{ds}} = -1\,\text{mV}$.

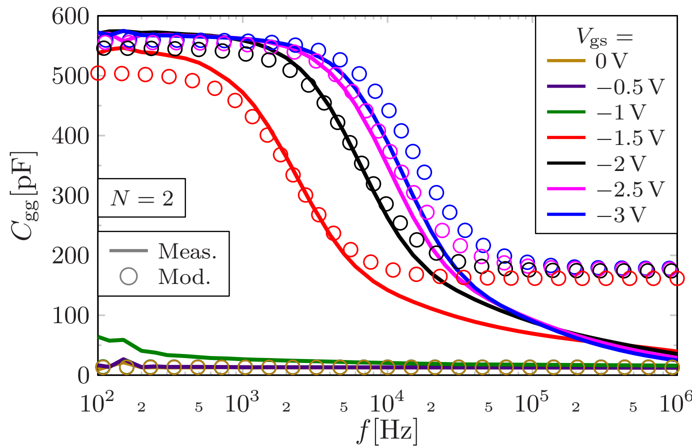

Figure 7.5.: Capacitance C_{gg} versus frequency of the staggered OTFT with $L_{\text{ch}} = 200\,\mu\text{m}$ presented in ref. [40]. The measurements (solid lines) are compared to the channel-segmentation model (circles) at different gate-source voltages. The amplitude of the superimposed AC signal is 100 mV in both the measurements and the SPICE simulations. The channel-segmentation model consists of $N = 2$ transistors that are interconnected. The drain-source voltage V_{ds} is 0 V for the measurement data and −1 mV for the model. The threshold voltage is set to $V_{\text{T0}} = -1.2\,\text{V}$ and a conductance $g_{\text{min}} = 1 \times 10^{-15}\,\text{S}$ is used. This figure shows similar results as presented in ref. [105].

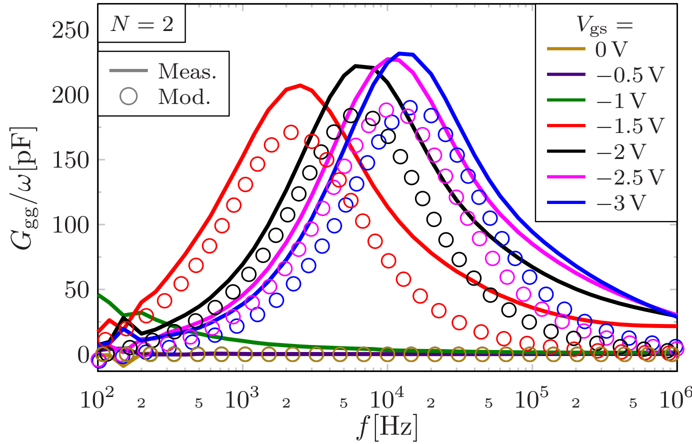

Figure 7.6.: Loss G_{gg}/ω versus frequency of the staggered OTFT with $L_{ch} = 200\,\mu m$ presented in ref. [40]. The measurements (solid lines) are compared to the channel-segmentation model (circles) at different gate-source voltages. The channel-segmentation model consists of $N = 2$ transistors that are interconnected. The simulation setup is the same as in Fig. 7.5. This figure shows similar results as presented in ref. [105].

In Cadence Virtuoso, the complex admittance between gate and drain is determined by dividing the AC part of the drain current by the AC part of the gate voltage. Based on this complex admittance, again Eqs. (6.7) and (6.8) are used for the calculation of the capacitance and conductance. As a consequence of the very small drain-source voltage the charges along the channel can be assumed as evenly distributed. Therefore, the following expressions can be formulated for the capacitances and the conductances of the transistor:

$$C_{sg} \approx C_{dg} \approx C_{gs} \approx C_{gd} \approx 1/2 \cdot C_{gg}, \tag{7.11}$$

$$G_{sg} \approx G_{dg} \approx G_{gs} \approx G_{gd} \approx 1/2 \cdot G_{gg}. \tag{7.12}$$

Thus, by multiplying the simulated capacitance and conductance by a factor of 2, the capacitance C_{gg} and the conductance G_{gg} are yielded.

Figures 7.5 and 7.6 show the measured and simulated capacitance C_{gg} and loss G_{gg}/ω. In the model, a very simple transmission line of only $N = 2$ transistors is used. It can be seen that there is already a certain goodness of fit even if a small number of only $N = 2$ transistors are interconnected. As it might be assumed, the quality of fit becomes better if more transistors are interconnected. This is shown in Fig. 7.7 where the capacitance C_{gg} and the loss G_{gg}/ω are displayed at a gate-source voltage of $V_{gs} = -3\,V$ with varying numbers of transistors that are interconnected. It becomes evident that when using a higher number of transistors the model agrees better with the measured data since the distribution of the charges and the charging through adjacent channel elements are captured more accurately in a finer mesh.

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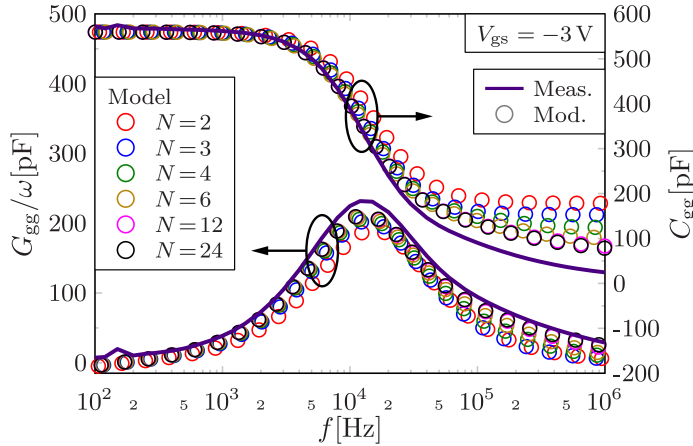

Figure 7.7.: Capacitance C_{gg} (right y-axis) and loss G_{gg}/ω (left y-axis) versus frequency of the staggered OTFT with $L_{ch} = 200\,\mu m$ presented in ref. [40]. The measurements (solid lines) are compared to the channel-segmentation model (circles) at a fixed gate-source voltage of $V_{gs} = -3\,V$. The number of transistor interconnected in the model is varied from $N = 2$ to $N = 24$. The simulation setup is the same as in Fig. 7.5. This figure shows similar results as presented in ref. [105].

7.2.3.2 AC TCAD Simulation

In this section, the channel-segmentation model is verified against Sentaurus TCAD simulation results. A staggered OTFT with a long channel of $L_{ch} = 200\,\mu m$ was simulated by means of an AC analysis with varying frequencies at distinct gate-source voltages with a fixed drain-source voltage of $V_{ds} = -1\,mV$. The simulation setup and the fitting parameters of the DC compact model are equal to the setup depicted in column (a) of Tab. 6.2. The reason for simulating a long-channel transistor is that the channel-segmentation model shall capture the effect of the charge propagation along the channel of the transistor. This effect is more pronounced in a transistor with a large channel length. After the fitting of the DC compact model which is presented in Sec. 6.3.2.1, an AC analysis is conducted in Cadence Virtuoso. As in the previous section the complex admittance $\underline{Y}$ between the gate and the drain terminal is determined. The capacitance and the conductance can be calculated from this and due to the nearly-zero drain voltage the condition $C_{gs} \approx C_{gd}$ is fulfilled which, for example, can be seen in Fig. 6.12. As a consequence, the simulated capacitance and conductance are interpreted as C_{gs} and G_{gs}.

The verification of the compact model by TCAD simulations is performed in the same manner as for the measurements presented in the previous section. In Fig. 7.8, the capacitance C_{gs} is compared at different gate-source voltages with the channel segmentation consisting of only $N = 2$ transistors. A certain level of agreement can be observed but at higher frequencies the model consisting of $N = 2$ transistors cannot represent the TCAD simulation results.

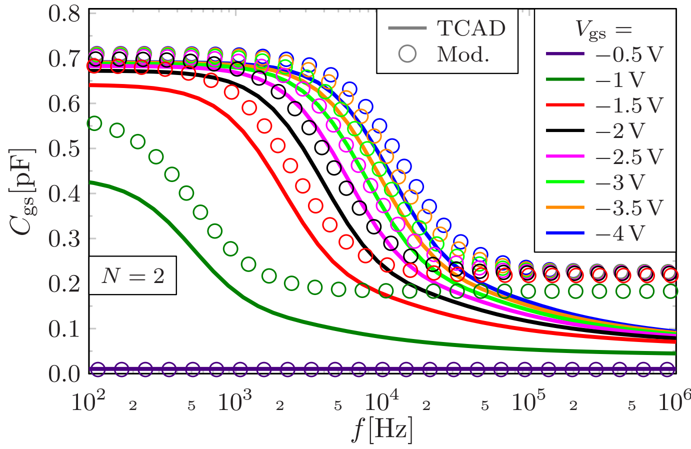

Figure 7.8.: Capacitance C_{gs} versus frequency of a staggered OTFT with $L_{ch} = 200\,\mu m$. The results of a Sentaurus TCAD simulation (solid lines) are compared to the channel-segmentation model (circles) at different gate-source voltages and a fixed drain-source voltage of $V_{ds} = -1\,mV$. The amplitude of the superimposed AC signal is 100 mV in the model. The model consists of $N = 2$ transistors that are interconnected. In Cadence Virtuoso, a conductance $g_{min} = 1 \times 10^{-15}$ S is used. This figure shows similar results as presented in ref. [105].

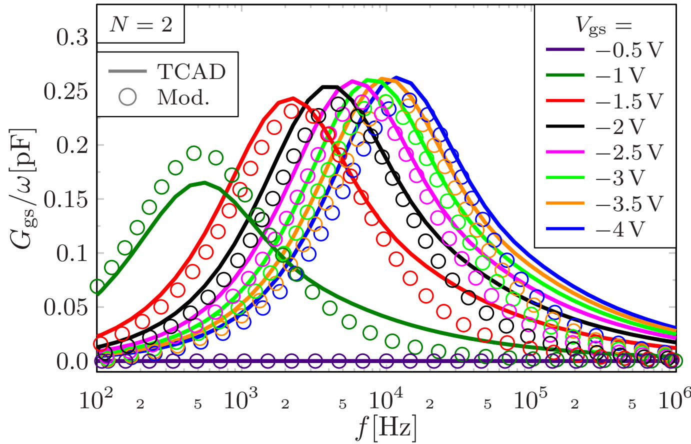

Figure 7.9.: Loss G_{gs}/ω versus frequency of a staggered OTFT with $L_{ch} = 200\,\mu m$. The results of a Sentaurus TCAD simulation (solid lines) are compared to the channel-segmentation model (circles) at different gate-source voltages and a fixed drain-source voltage of $V_{ds} = -1\,mV$. The model consists of $N = 2$ transistors that are interconnected. The simulation setup is the same as in Fig. 7.8. This figure shows similar results as presented in ref. [105].

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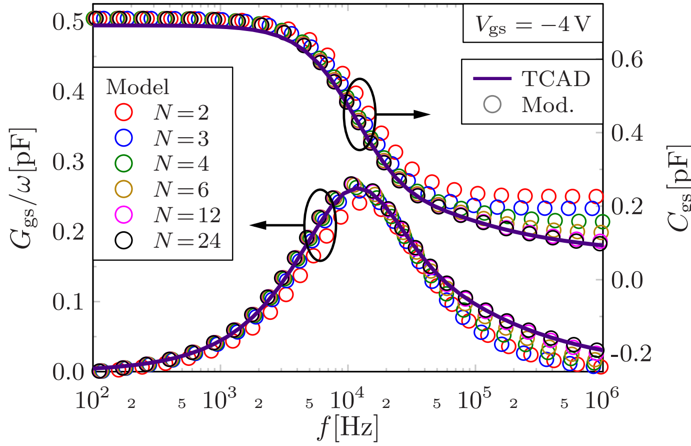

Figure 7.10.: Capacitance C_{gs} (right y-axis) and loss G_{gs}/ω (left y-axis) versus frequency of of a staggered OTFT with $L_{ch} = 200\,\mu m$. The results of a Sentaurus TCAD simulation (solid lines) are compared to the channel-segmentation model (circles) at a fixed gate-source voltage of $V_{gs} = -4$ V and a fixed drain-source voltage of $V_{ds} = -1$ mV. The number of transistors interconnected in the model is varied from $N = 2$ to $N = 24$. The simulation setup is the same as in Fig. 7.8. This figure shows similar results as presented in ref. [105].

A similar comparison is shown in Fig. 7.9 where for $N = 2$ the loss G_{gs}/ω is shown. The level of agreement is already comparatively high but the compact model again leads to wrong results at frequencies larger than the maximum of the loss curve.

The accuracy of the channel-segmentation model can be improved by increasing the number of transistors which are interconnected. Figure 7.10 depicts the capacitance C_{gs} and the loss G_{gs}/ω at a gate-source voltage of $V_{gs} = -4$ V for varying numbers of transistors. It can be observed that the agreement improves with an increasing number of transistors. As the plot shows the channel-segmentation model can very accurately describe the frequency-dependent capacitance and loss of the TCAD-simulated transistor. Since the computation time of the model increases with the number of transistors a proper number must be chosen to find a trade-off between simulation speed and accuracy. For instance, if the transistor is operated below the maximum of the loss curve, a number of $N = 4$ is totally sufficient.

7.2.3.3 Transient TCAD Simulation

In this section, the functionality of the model will be verified by means of a transient analysis which tests the large-signal behavior of the model. During a transient analysis a time-dependent signal is applied to the gate and the time response of the model is observed. In TCAD, a 2D transient simulation of a staggered OTFT has been conducted. The setup is similar as the one depicted in column (a) of Tab. 6.2 but here a transistor with a channel length of $L_{ch} = 120\,\mu m$ is used. Prior to conducting the transient analysis in Cadence Virtuoso, a DC fitting of the

compact model with regard to the TCAD simulation results is performed. Due to the good scalability of the compact model the same DC fitting parameters as for the transistor with $L_{\mathrm{ch}} = 200\,\mu\mathrm{m}$ can be used. These are depicted in column (a) of Tab. 6.2.

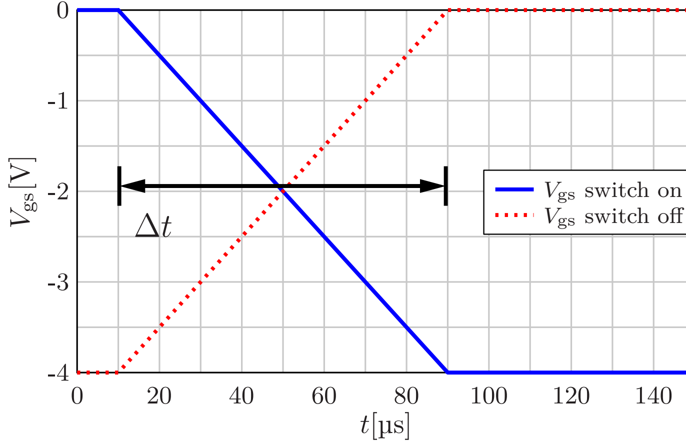

Figure 7.11.: Time-dependent gate-source voltage used as the input for the TCAD simulations of the transistors' switch-on process (solid blue line) and the switch-off-process (dotted red line). After a time of 10 µs the voltage is ramped to its final value within a time of $\Delta t = 80\,\mu\mathrm{s}$. This figure shows the same data as presented in ref. [105].

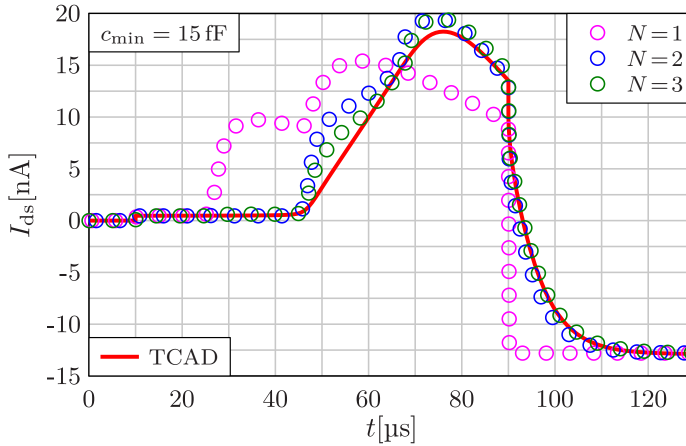

Figure 7.12.: Drain current transient predicted by the channel-segmentation model (symbols) in comparison to the TCAD simulation results (solid line) during the switch-on process. In the model, different numbers of transistors are used. This figure shows nearly the same data as presented in ref. [105].

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During the transient analysis the drain-source voltage is set to a constant value of $V_{ds} = -1\,V$ and the gate voltage is ramped once from $V_{gs} = 0\,V$ to $V_{gs} = -4\,V$ in order to simulate a switch-on process and once from $V_{gs} = -4\,V$ to $V_{gs} = 0\,V$ for the simulation of a switch-off process. In Fig. 7.11, the input profile of the gate-source voltage is shown versus time. For the first 10 µs, V_{gs} is held constant at its initial value. Then, it is ramped linearly in a time $\Delta t = 80\,\mu s$ to its final value where it is again kept for a certain amount of time until the simulation is over.

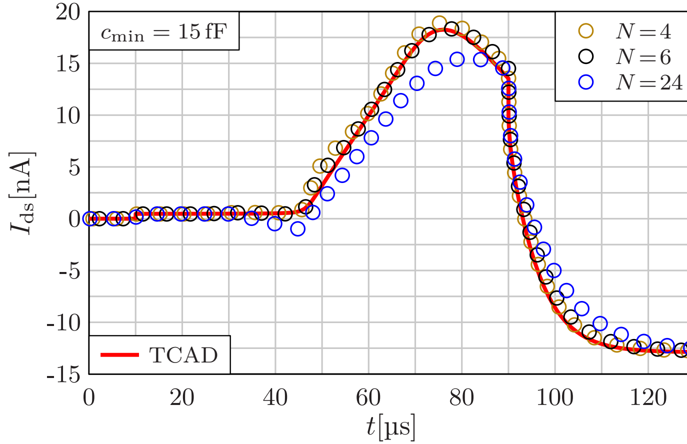

Figure 7.13.: Drain current transient predicted by the channel-segmentation model (symbols) in comparison to the TCAD simulation results (solid line) during the switch-on process. In the model, different numbers of transistors are used. This figure shows nearly the same data as presented in ref. [105].

Figures 7.12 and 7.13 show the drain current during the switch-on process versus time of the channel-segmentation model in comparison to the TCAD simulation results for varying numbers of transistors incorporated in the model. For a better distinction of the data, the curves are displayed in two different plots for two sets of numbers. Whereas during the AC analysis in the former section the conclusion was that more transistors lead to a higher accuracy this conclusion does not hold for the transient analysis. It can be seen in Fig. 7.13 that the model incorporating $N = 24$ transistors leads to a lower agreement than the model incorporating $N = 6$ transistors. The reason for this can be found by looking at the auxiliary components that Cadence Virtuoso automatically connects to the circuit in order to improve convergence. As described in Sec. 7.2.2, Cadence Virtuoso connects every node in the circuit to the ground level by a small capacitance c_{min}. In order to achieve convergence, a comparatively high value for c_{min} of 15 fF has to be used. The total gate capacitance of the transistor in the linear regime of operation converges to the capacitance defined by the gate dielectric:

$$C_{gg} = (L_{ch} + L_{ov,GD} + L_{ov,GS}) \cdot W_{contact} \cdot C'_{diel} \approx 912\,fF. \tag{7.13}$$

Since the capacitance c_{min} is a per-node value it means that with a higher number of transistors a higher number of capacitors c_{min} is added. A single capacitance c_{min} only slightly changes the capacitance of the transistor to be modeled but a high number can significantly change the results. This is the reason for the reduced goodness of fit with the number of transistors becoming too high. Overall, a good agreement is achieved if the model is computed with $N = 6$ transistors.

In the following, the results of the transient analysis will be discussed. During the first 10 µs, the drain current is nearly zero since V_{gs} is still zero and apart from the small diffusion current in the off-state and leakage currents, no DC current flows. This is equivalent with the case depicted in Fig. 3.2(a) where the comparison of a transistor and a water system is presented. At the time point $t = 10\,\mu\text{s}$, a small upward jump is visible in the current in Figs. 7.12 and 7.13. At this moment, the linear increase of the gate-source voltage from $V_{\text{gs}} = 0\,\text{V}$ towards $V_{\text{gs}} = -4\,\text{V}$ starts. The transistor is still not turned on until V_{gs} reaches the threshold voltage. The small upward jump in the drain current is the abruptly starting current that charges the gate-to-drain overlap capacitance. Since the organic semiconductor is depleted in the sub-threshold regime of operation the overlap capacitance is nearly constant and can be characterized as the series connection of the gate dielectric and the organic semiconductor. Very generally, the current I_{c} flowing through a capacitance is defined by [106]:

$$I_{\text{c}} = C \cdot \frac{dV_{\text{c}}}{dt}, \tag{7.14}$$

where V_{c} is the voltage applied to the capacitance. Since the gate-source voltage is varied linearly starting at $t = 10\,\mu\text{s}$, also the gate-drain voltage $V_{\text{gd}} = V_{\text{gs}} - V_{\text{ds}}$ is varied linearly. Accordingly, the current flowing in the gate-to-drain overlap capacitance is constant and nearly instantly jumps upward when the gate-voltage ramp starts. It can be seen that this charging current has a different polarity than the drain current that flows under DC conditions. Since a p-type transistor is regarded the DC drain current is negative. In other words: If the transistor is operated above the threshold voltage in steady-state DC conditions, holes are flowing into the source terminal and flowing out of the drain terminal. However, since the transistor is still operated in the sub-threshold regime of operation only the capacitive charging current of the gate-to-drain overlap region is present. The positive drain current in this operation point implies that rather than holes coming out of the drain they are flowing into the drain. This can be explained by the change of the potentials at the gate-to-drain overlap capacitance: since the gate potential is decreasing electrons are flowing through the gate terminal to the gate electrode. In order to fulfill the principle of charge conservation, an equal amount of holes has to be present at the drain electrode. Since the organic semiconductor is still depleted the necessary holes for this charge conversation cannot come from the channel region. The holes have to enter through the drain electrode constituting a positive drain current which charges this series capacitance.

At $t = 30\,\mu s$, the gate-source voltage reaches a value of $V_{gs} = -1\,V$. The organic semiconductor is now driven into accumulation at the gate-dielectric/semiconductor interface. However, it can be seen in Fig. 7.12 that the TCAD-simulated current does not exhibit any changes at that time point. The reason for this behavior is that the channel only gradually becomes more conductive with higher gate-source voltages and that the charges need to propagate along the channel. With the channel conductivity reaching a certain value at $t \approx 45\,\mu s$ the charging current rapidly increases and a substantial overshoot current results. Now, the charging of channel capacitance segments through adjacent channel resistance elements is dominant. There are as well accumulation charges in the gate-to-contact overlap regions. However, since the overlap regions are short in comparison to the channel length of the transistor the time-dependent charging of the overlap regions is of minor importance here. Under steady-state conditions, the holes are entirely injected at the source end of the channel and are extracted from the channel at the drain end. However, it can be observed that the overshoot current has a positive sign which means that even more holes are entering the drain terminal in order to fill the channel capacitance segments. This case is equivalent with Fig. 3.2(b). At $t \approx 76\,\mu s$, the overshoot current reaches its maximum and starts decreasing even if the gate-source voltage has still not reached its end value. The decrease in the overshoot current can be explained by the fact that during the gate-voltage ramp already a certain amount of channel charge capacitances are being charged. It has to be mentioned that in addition to the capacitive charging currents, the normal DC current is also starting to flow. The total current at the drain terminal is thus a superposition of the DC current and the capacitive charging current. Obviously, the charging currents are starting to decrease which causes the overshoot current to decrease.

At $t = 90\,\mu s$, the gate-source voltage reaches its final value of $V_{gs} = -4\,V$. It can be seen in Fig. 7.12 that the drain current which is still positive rapidly starts to decrease. Still, not all charging processes of the intrinsic channel charge capacitances have finished which is the reason why the negative DC current does not instantly take over. However, the charging of the channel charge capacitances is slowing down. At $t \approx 92\,\mu s$, the direction of the drain current is reversed and it starts converging to the steady-state DC value. This is comparable to the water system as displayed in Figs. 3.2(c) and 3.2(d). Then, the drain current converges to the DC value which is theoretically never completely reached, similarly as the charging of a capacitor through a resistor is never fully finished. However, as can be seen, at $t = 120\,\mu s$, the current nearly does not exhibit any further changes. This case is represented by the water system in Fig. 3.2(e).

Similarly as for the switch-on process, Figs. 7.14 and 7.15 show the results of the channel-segmentation model in comparison to the TCAD simulation results for a switch-off process. Also here, for a better visibility, the curves are split up into two plots. Similarly as in the switch-on process, the best agreement is not obtained by the model consisting of $N = 24$ transistors. Rather, a number of $N = 6$ transistors produces the best results. A short discussion of the switch-off process will follow.

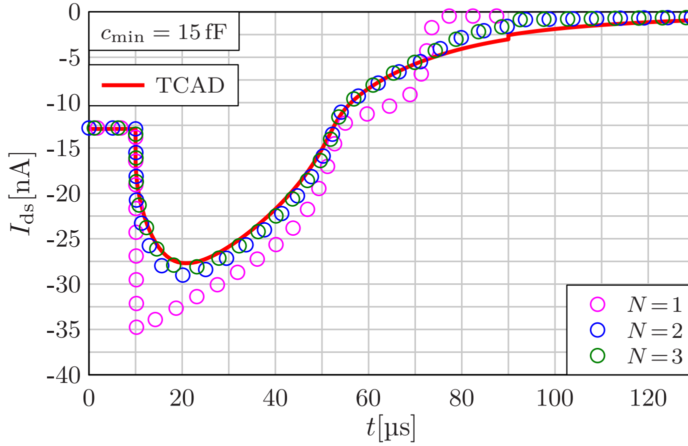

Figure 7.14.: Drain current transient predicted by the channel-segmentation model (symbols) in comparison to the TCAD simulation results (solid line) during the switch-off process. In the model, different numbers of transistors are used. This figure shows nearly the same data as presented in ref. [105].

At $t = 10\,\mu\text{s}$, the ramping of V_{gs} from its on-state value of $V_{\text{gs}} = -4\,\text{V}$ to $V_{\text{gs}} = 0\,\text{V}$ starts. As can be seen, the drain current now produces a substantial undershoot. Figuratively speaking, it means that even if the transistor is being turned off, even more holes are coming out of the drain terminal. The reason is that with a reduction in the absolute value of V_{gs}, the total amount of charges which the organic semiconductor can store is reduced. The charges cannot disappear but they have to leave the transistor through the terminals. Thus, the undershoot current is a consequence of the discharging of the channel charge capacitances.

At $t \approx 20\,\mu\text{s}$, the absolute value of the undershoot current reaches its maximum and starts decreasing. Due to the further reduction of V_{gs}, the static DC current is further reduced and a certain amount of charges has already been discharged from the channel charge capacitances. Therefore, the absolute value of the drain current is further reduced. However, with the absolute value of V_{gs} being reduced, the conductance of the carrier channel decreases. Consequently, the charge carriers that still have to be discharged from the channel charge capacitances have to travel through a higher-conductive region. Thus, the absolute value of the drain current does not converge quickly to its off-state value.

At $t = 90\,\mu\text{s}$, V_{gs} reaches its final value of $0\,\text{V}$. It can be seen that the drain current is still not zero. However, a small jump towards zero is observable. The reason for this is the stop of the discharging of the gate-to-drain overlap capacitance. Since the organic semiconductor is depleted now the gate-to-drain overlap capacitance again behaves like a series connection of two parallel-plate capacitors. Thus, the capacitive discharging current of the overlap region stops abruptly. As can be seen, the current very slowly converges to zero. The convergence

rate is much slower in comparison to convergence rate of the drain current to its on-state DC value during the switch-on process after the gate-source voltage ramp is finished. This behavior can be attributed to the fact that the intrinsic carrier channel is very low-conductive because the transistor is already turned off. However, still some charges have to be discharged from the channel charge capacitances. Due to the low conductivity of the channel, the charges can reach the drain terminal very slowly.

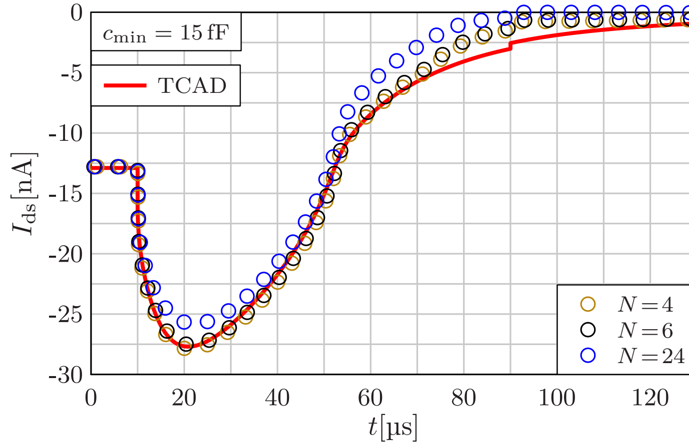

Figure 7.15.: Drain current transient predicted by the channel-segmentation model (symbols) in comparison to the TCAD simulation results (solid line) during the switch-off process. In the model, different numbers of transistors are used. This figure shows nearly the same data as presented in ref. [105].

In conclusion, it can be said that the channel-segmentation model reproduces the TCAD-simulated transient responses of the transistors with very good accuracy if a number of $N = 6$ transistors is used in the series connection.

7.3 Capacitances in Short-Channel Transistors

In this section, an empirical enhancement of the compact model for the total charges in a quasistatic operation point is presented. Based on investigations of TCAD simulations, fitting functions are proposed and verified with respect to simulated quasistatic capacitances of short-channel transistors comprising comparatively large Schottky barriers.

7.3.1 Observations Based on TCAD

The model for the total charges presented in Chap. 4 is only suitable for transistors with negligible contact resistances with regard to the intrinsic channel resistance of the transistor. Thus, it is worth investigating how the charge model behaves if applied in short-channel transistors. For this purpose, a Sentaurus TCAD simulation of a staggered OTFT with a channel length of 2 µm has been conducted. The simulation uses slightly different parameters

than the TCAD simulations presented so far. Here, the parameters are chosen similar as in fabricated OTFTs at the Max Planck Institute so that the simulations show a certain degree of agreement with measured current-voltage characteristics.

The setup of the TCAD simulation will be outlined in the following. An organic semiconductor with an electron affinity of $\chi_{\mathrm{osc}} = 1.81\,\mathrm{eV}$, a bandgap of $E_{\mathrm{g}} = 3.38\,\mathrm{eV}$, a constant electron mobility of $\mu_{\mathrm{n}} = 1 \times 10^{-10}\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$, and a constant hole mobility of $\mu_{\mathrm{p}} = 1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ is simulated. For simplicity, the density of states is assumed as a square-root function such as in crystalline semiconductors with an effective density of $N_{\mathrm{v}} = 1 \times 10^{21}\,\mathrm{cm^{-3}}$. The relative dielectric permittivities of the depleted organic semiconductor and the gate dielectric are set as $\varepsilon_{\mathrm{r,osc}} = 3$ and $\varepsilon_{\mathrm{r,diel}} = 4.88$, respectively. The work function of the gate electrode is set to $\varPhi_{\mathrm{m,g}} = 4.1\,\mathrm{eV}$ and the work function of the source/drain electrodes is altered between $\varPhi_{\mathrm{m,sd}} = 5.19\,\mathrm{eV}$ and $\varPhi_{\mathrm{m,sd}} = 4.7\,\mathrm{eV}$ in order to simulate one transistor with only Ohmic contacts and one with Schottky barriers at the metal-to-semiconductor junctions. In case of the transistor comprising Schottky barriers, the Schottky-barrier-lowering effect is activated. The channel length is chosen as $L_{\mathrm{ch}} = 2\,\mu\mathrm{m}$, the channel width is chosen as $W_{\mathrm{contact}} = W_{\mathrm{ch,SD}} = 1\,\mu\mathrm{m}$, the gate-to-contact overlap lengths are set to $L_{\mathrm{ov,GD}} = L_{\mathrm{ov,GS}} = 2\,\mu\mathrm{m}$, the gate-dielectric thickness is set to $t_{\mathrm{diel}} = 5.3\,\mathrm{nm}$, and a thickness of the organic semiconductor of $t_{\mathrm{osc}} = 25\,\mathrm{nm}$ is used.

The TCAD simulations are conducted using the Poole-Frenkel mobility model which captures the influence of the electric field in the organic semiconductor on the mobility. The resulting effective mobility for holes that is used in this setup has the following formulation [50]:

$$\mu_{\mathrm{PF}} = \mu_{\mathrm{p}} \cdot \exp\left(\sqrt{F} \cdot \left(\frac{\beta_{\mathrm{PF}}}{T} - \gamma_{\mathrm{PF}}\right)\right) \tag{7.15}$$

where F is the electric field in the organic semiconductor and β_{PF} and γ_{PF} are fitting parameters of the Poole-Frenkel model. The simulation is computed with $\beta_{\mathrm{PF}} = 0.5\,K\sqrt{(m/V)}$ and $\gamma_{\mathrm{PF}} = 1 \cdot 10^{-3}\,\sqrt{(m/V)}$. In addition to the Poole-Frenkel mobility, another effect that plays an important role in organic semiconcudtors is considered in the TCAD simulation: parasitic traps in the semiconductor. Traps have an influence on the device electrostatics and change the sub-threshold swing and the threshold voltage of a transistor [36]. In this simulation, traps in the bandgap of the organic semiconductors are assumed with a Gaussian distribution. The peak of this distribution is 0.2 eV above the valence band energy. A trap concentration of $N_{0,\mathrm{trap}} = 1 \times 10^{19}\,\mathrm{cm^{-3}\,eV^{-1}}$ and a standard deviation of $\sigma_{\mathrm{trap}} = 0.1\,\mathrm{eV}$ is used.

As usual when observing the charge/capacitance model, the charge-based DC compact model is fitted to the current-voltage characteristics of the TCAD simulations and subsequently the quasistatic capacitances are compared. Figure 7.16 shows the quasistatic trans-capacitances of the compact model in comparison to the TCAD simulation where no Schottky barrier between the source/drain electrodes and the organic semiconductor is present. The agreement is not

perfect but in general, the simulated capacitances are reproduced well. Even in the absence of Schottky barriers the contact resistances have to be considered in the compact model. The reason is that in a transistor with such short channel lengths, the sheet resistance of the organic semiconductor becomes important. It can be seen that the capacitances C_{sg} (magenta) and C_{dg} (cyan) cross each other at high absolute values of V_{gs}. Despite the inaccuracies the overall fitting of the quasistatic capacitance model is still sufficient. However, the TCAD-simulated transistor

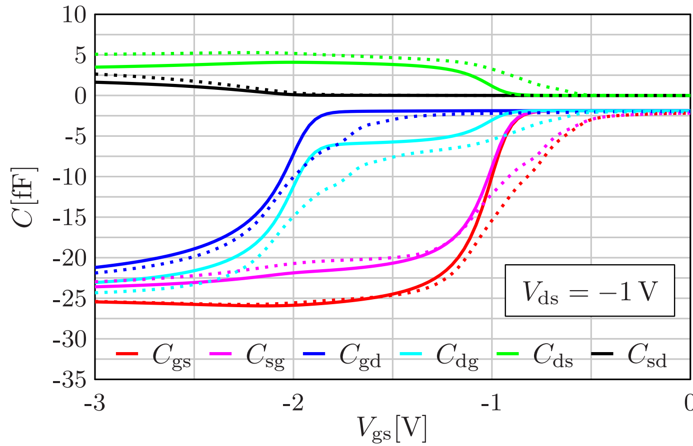

Figure 7.16.: Quasistatic capacitances of a short-channel staggered OTFT at a fixed drain-source voltage of $V_{ds} = -1\,V$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The channel length of the transistor is $L_{ch} = 2\,\mu m$. The work function of the source/drain electrodes is chosen to match the HOMO of the organic semiconductor. Thus, there is no Schottky barrier: $\Phi_{B0} = 0\,eV$. In the compact model, the following fitting parameters are used: $V_{T0} = -1.01\,V$, $S_{obs} = 100\,mV/dec$, $R_{sheet}/W_{contact} = 1 \times 10^{13}\,\Omega/cm$, $L_T = 1.4\,\mu m$, $\kappa = 0.9\,cm^2V^{-\beta-1}s^{-1}$, $\beta = 0.035$, $\lambda = 0.012\,V^{-1}$.

has an ideal Ohmic contact at the source/drain-to-semiconductor interfaces. If, by contrast, the work function of the metal is not aligned with the HOMO of the organic semiconductor, Schottky barriers are present which have a high influence on the contact resistances [47]. Under the presence of high Schottky barriers, the capacitances of the transistor behave quite different from the capacitances without Schottky barriers. This is visualized in Fig. 7.17 where the quasistatic capacitances of a transistor with a high Schottky barrier of $\Phi_{B0} = 0.49\,eV$ are depicted. The DC model is fitted by making use of the non-linear injection model presented in ref. [47]. It can be seen that there is only a low level of agreement between the TCAD-simulated capacitances and the compact model. The capacitances C_{gs} (red) and C_{gd} (blue) cross each other at high absolute values of V_{gs}, and the two capacitances C_{sg} and C_{dg} also do. Please recall that C_{gs} and C_{gd} are the change of the total gate charges with respect to a change in the source or drain potential, respectively. In Sec. 6.3.2.1, it is shown that typically C_{gs} has a higher absolute value than C_{gd} for every voltage that is applied. The total charges in the channel (which are the same as the total gate charges but with different sign) are always more under control of the source terminal than of the drain terminal since the application of a

drain-source voltage causes a reduction of the charge density along the channel towards the drain end. The crossing of C_{gs} and C_{gd} (Fig. 7.17) implies that the channel charges are more under control of the drain terminal at large absolute values of V_{gs}. Similarly, these effects are reflected in C_{sg} and C_{dg}. Please recall that these capacitances reflect the change of the source or drain charges, respectively, if the gate potential is changed. If C_{dg} has a larger absolute value than C_{sg}, it can be interpreted that a change in the gate potential has more influence on the charge associated with the drain in comparison to the charge associated with the source. Also this result is striking and in contradiction to the verification of the long-channel transistors presented so far.

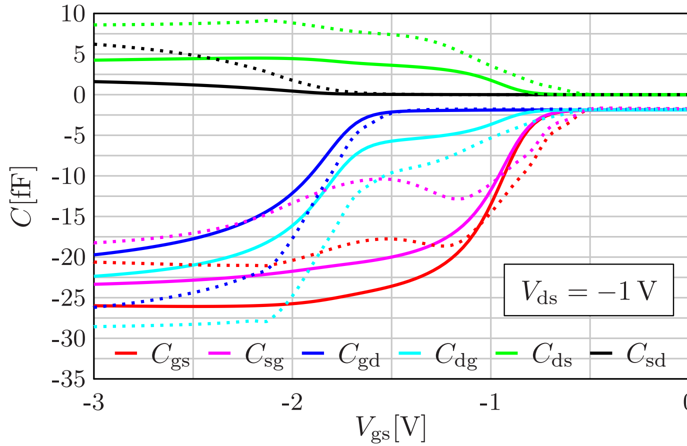

Figure 7.17.: Quasistatic capacitances of a short-channel staggered OTFT at a fixed drain-source voltage of $V_{\mathrm{ds}} = -1\,\mathrm{V}$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The channel length of the transistor is $L_{\mathrm{ch}} = 2\,\mu\mathrm{m}$. The work function of the source/drain electrodes is chosen to obtain a Schottky barrier of $\Phi_{\mathrm{B0}} = 0.49\,\mathrm{eV}$. In the compact model, the following fitting parameters are used: $V_{\mathrm{T0}} = -0.99\,\mathrm{V}$, $S_{\mathrm{obs}} = 100\,\mathrm{mV/dec}$, $R_{\mathrm{sheet}}/W_{\mathrm{contact}} = 3.0776 \times 10^{13}\,\Omega/\mathrm{cm}$, $L_{\mathrm{T}} = 1.4\,\mu\mathrm{m}$, $\kappa = 0.63\,\mathrm{cm^2V^{-\beta-1}s^{-1}}$, $\beta = 0.54$, $\lambda = 0.003\,\mathrm{V^{-1}}$. The non-linear injection model is fitted using the following parameters: $\eta = 1.0096$, $\theta = 2$, $w_{\mathrm{sat}} = 2$.

Another investigation leads to an important information for the compact model: In Fig. 7.18, the density of accumulated holes in the organic semiconductor along a cutline very close to the gate dielectric is shown. The results of two transistors with different Schottky barriers at the source/drain-to-semiconductor junctions are depicted and it is revealed that the presence of Schottky barriers significantly alters the charge densities. Even if the non-linear injection model presented in ref. [47] correctly accounts for the influence of the Schottky barriers on the drain current, it cannot completely capture the influence which they have on the charge densities. In principle, the charge density Q'_{ms} would have to be recalculated to reflect the influence of the Schottky barrier at the source contact. However, an accurate expression for the voltage drop across the barrier is missing and analytically not solvable. Therefore, in ref. [47] an equivalent non-linear resistance of the Schottky barrier is derived and incorporated

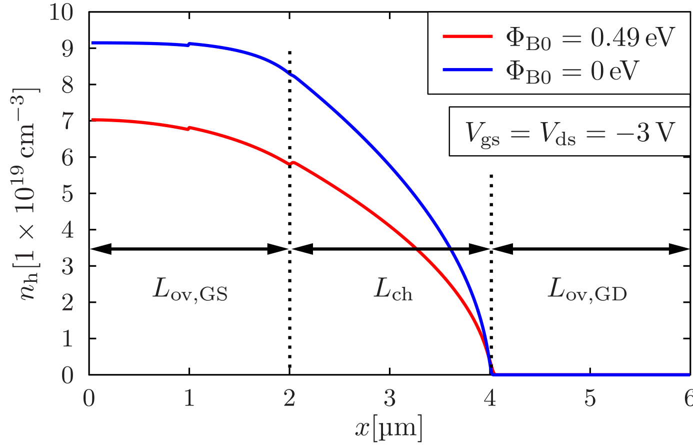

Figure 7.18.: Density of accumulated holes in the organic semiconductor of a staggered OTFT along a cutline close the gate dielectric as simulated by TCAD. In one simulation, no Schottky barrier between the source/drain electrodes and the organic semiconductor is present (blue line) whereas in the other simulation, a high Schottky barrier of $\Phi_{B0} = 0.49\,eV$ is present (red line). It can be seen that the barrier alters the charge densities significantly. The channel length of the transistor is $L_{ch} = 2\,\mu m$. This figure was published in ref. [55].

into an effective mobility. As the resistance of the source Schottky barrier increases, the effective mobility is reduced. In contrast to this procedure, the influence of the Schottky barrier at the drain is captured by its voltage drop $V_{sb,d}$ and based on this, a new charge density $Q'_{md,barr}$ is calculated. This procedure is totally sufficient to reproduce measured and simulated current-voltage characteristics of OTFTs with good accuracy but without any further modifications the compact model for the total charges fails. The reason is that the total charges in the transistor are calculated based on an integration of the charge density along the channel, as presented in Chap. 4. Thus, if the model equations describing the charge densities do not reflect the properties of the OTFT accurately, the model for the total charges cannot produce correct results even if the DC model has a good fitting. Furthermore, the injection model in ref. [47] does not claim to correctly calculate the different voltage drops over the source and drain Schottky barriers explicitly. The main goal is to obtain a model that can be fitted to current-voltage characteristics as accurately as possible.

7.3.2 Derivation of the Model Equations

In this section, the derivation of correction functions are presented based on the observations from TCAD simulations. These correction functions lead at least to a better agreement between the compact model for the total charges and the TCAD simulation results.

7.3.2.1 Influence of the Contact Resistances

The first concern is to account for the contact resistances. As outlined in the last section, the non-linear injection model presented in ref. [47] is able to reproduce simulated or measured current-voltage characteristics of OTFT incorporating the non-linear influence of the Schottky barriers at the source and the drain contacts. In the injection model, a significantly approximated expression for the voltage drop $V_{\mathrm{sb,s}}$ across the Schottky barrier at the source contact is defined. This is sufficiently accurate for the definition of an equivalent barrier resistance $R_{\mathrm{sb,s}}$ with the help of which the non-linear influence of the barrier on the current-voltage characteristics can be captured. An explicit, analytical solution of the voltage drop across the source Schottky barrier is not available since this would require the numerical solution of the series connection of an inversely operated Schottky barrier and the transistor. The voltage drop $V_{\mathrm{sb,d}}$ over the drain Schottky barrier is calculated explicitly. However, this voltage drop is assumed in ref. [47] to be a linear function of the drain-source voltage for values below the voltage at which the voltage drop across the barrier saturates. Despite this strong approximation the influence of the Schottky barrier at the drain contact on the output characteristics in the form of a shift of the output curves along the V_{ds}-axis is captured with sufficient accuracy by the model.

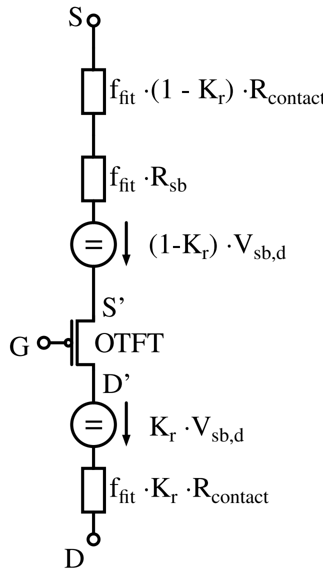

Figure 7.19.: Equivalent circuit of the transistor comprising contact resistances. The voltage drops over the contact elements are needed for the charge model. This picture is similar as published in ref. [55].

In addition to the resistances of the Schottky barriers described in ref. [47], the DC model also includes an Ohmic component of the contact resistance which is denoted as R_{contact}. In case of staggered transistors, this Ohmic resistance is calculated based on the sheet resistance (Eq. (2.10)) and in case of coplanar transistors, it is simply a constant. The nonlinear resistance $R_{\text{sb,s}}$ of the source Schottky barrier is added to the Ohmic contact resistance and both are used in the effective mobility according to Eq. (2.8) or Eq. (2.22). Also the Ohmic contact resistance has to be included in the discussion of the contact resistances in the context of the model for the total charges. In Fig. 7.19, an equivalent circuit of a transistor comprising contact resistances is shown. At the intrinsic transistor, different voltages $V_{\text{gs}'}$ and $V_{\text{gd}'}$ are found than at the outer terminals. The contact resistances in Fig. 7.19 are multiplied by a fitting function which will be explained in the following. The idea is to calculate the voltage drops over the contact elements at the source and at the drain separately by making use of the DC current incorporating the non-linear injection model. After the calculation of these contact voltages $V_{\text{s,contact}}$ and $V_{\text{d,contact}}$, the charge densities Q'_{ms} and Q'_{md} are recalculated. At this point, two sets of charge densities exist in the model: the ones used for the DC model and the newly calculated charge densities containing the voltage drops $V_{\text{s,contact}}$ and $V_{\text{d,contact}}$. The latter are then used in the charge integrals according to Eqs. (A.1), (A.2), and (A.3). Furthermore, the auxiliary voltages V'_{gs} and V'_{gd} according to Eqs. (4.26) and (4.29) which are used in the calculation of the gate-to-contact overlap capacitances in staggered transistors are also calculated based on the new charge densities. The evolution of the correction functions is presented in the next paragraphs.

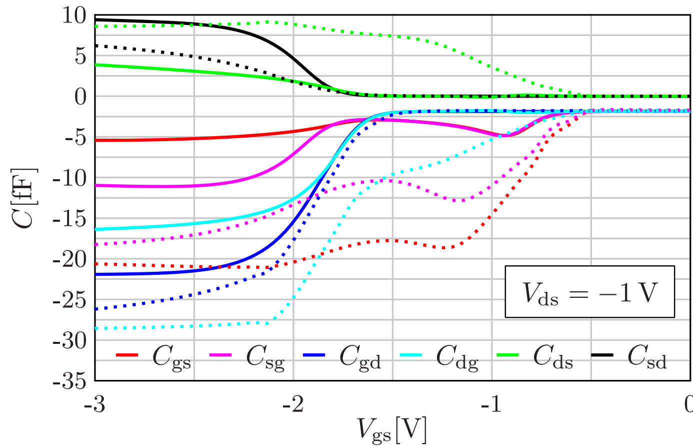

Figure 7.20.: Quasistatic capacitances of a short-channel staggered OTFT at a fixed drain-source voltage of $V_{\text{ds}} = -1\,\text{V}$. The channel length of the transistor is $L_{\text{ch}} = 2\,\mu\text{m}$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The parameters of the TCAD setup and the compact model are the same as in Fig. 7.17. Here, the contact voltages are calculated according to experiment 1: $V_{\text{s,contact}} = V_{\text{sb,s}}$ and $V_{\text{d,contact}} = V_{\text{sb,d}} + |I_{\text{ds}}| \cdot R_{\text{contact}}$.

Experiment 1: Usage of $V_{\mathrm{sb,s}}$ and $V_{\mathrm{sb,d}}$

The first experiment is to directly use the voltage drops $V_{\mathrm{sb,s}}$ and $V_{\mathrm{sb,d}}$ as they are defined in ref. [47]. Furthermore, the Ohmic part R_{contact} of the contact resistance is completely attributed to belong to the drain contact voltage. The two contact voltage drops are defined as:

$$V_{\mathrm{s,contact}} = V_{\mathrm{sb,s}}, \tag{7.16}$$

$$V_{\mathrm{d,contact}} = V_{\mathrm{sb,d}} + |I_{\mathrm{ds}}| \cdot R_{\mathrm{contact}} \tag{7.17}$$

where I_{ds} is the DC drain current as calculated by the compact DC model incorporating the non-linear injection model [47]. As can be seen in Fig. 7.20, this experiment does not lead to proper results. Even if the capacitance C_{gd} shows some kind of agreement with the TCAD simulation results, the other capacitances fail entirely. This experiment proves that $V_{\mathrm{sb,s}}$ and $V_{\mathrm{sb,d}}$ serve as auxiliary values in the non-linear injection model [47] which are only suitable to reproduce the static current-voltage characteristics of OTFTs.

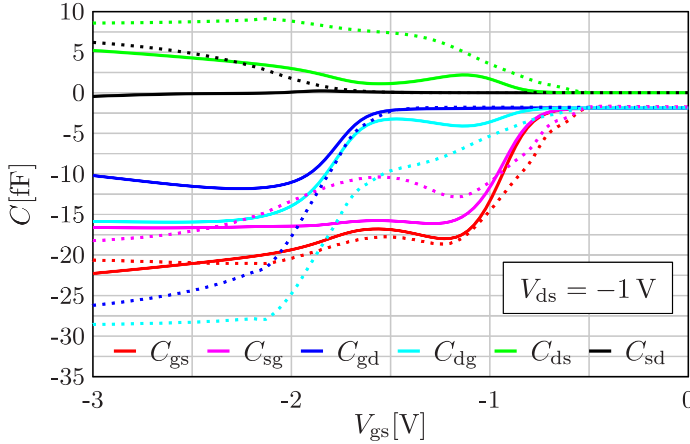

Figure 7.21.: Quasistatic capacitances of a short-channel staggered OTFT at a fixed drain-source voltage of $V_{\mathrm{ds}} = -1\,\mathrm{V}$. The channel length of the transistor is $L_{\mathrm{ch}} = 2\,\mu\mathrm{m}$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The parameters of the TCAD setup and the compact model are the same as in Fig. 7.17. Here, the contact voltages are calculated according to experiment 2: $V_{\mathrm{s,contact}} = |I_{\mathrm{ds}}| \cdot R_{\mathrm{sb,s}}$ and $V_{\mathrm{d,contact}} = V_{\mathrm{sb,d}} + |I_{\mathrm{ds}}| \cdot R_{\mathrm{contact}}$.

Experiment 2: Usage of $V_{\mathrm{sb,d}}$ and $R_{\mathrm{sb,s}}$

The next experiment is to use the equivalent resistance $R_{\mathrm{sb,s}}$ of the Schottky barrier at the source in order to define the contact voltage drop at the source. The contact voltage drop at the drain is the same as in experiment 1. The voltages are defined as:

$$V_{\mathrm{s,contact}} = |I_{\mathrm{ds}}| \cdot R_{\mathrm{sb,s}}, \tag{7.18}$$

$$V_{\mathrm{d,contact}} = V_{\mathrm{sb,d}} + |I_{\mathrm{ds}}| \cdot R_{\mathrm{contact}}. \tag{7.19}$$

Figure 7.21 shows the result for the case that experiment 2 is conducted. It can be seen that C_{gs} now shows a better agreement whereas C_{gd} has become worse in comparison to experiment 1. Since the modeled capacitance C_{gd} has a too low absolute value at high absolute values of V_{gs} the consequence is that the influence of the drain contact resistance is too high. A change in the drain potential obviously leads to a smaller change in the total gate charges than necessary. Even if the capacitance C_{gs} shows a good agreement, the contact voltages are re-engineered in a third experiment.

Experiment 3: Redistribution of the Contact Voltages

The next experiment is to introduce a redistribution of the contact voltages. It is assumed that both the voltage drops over the Ohmic contact resistance and the voltage $V_{\mathrm{sb,d}}$, which are theoretically only present at the drain, may be redistributed between the source and the drain:

$$V_{\mathrm{s,contact}} = |I_{\mathrm{ds}}| \cdot (R_{\mathrm{sb,s}} + (1 - K_{\mathrm{r}}) \cdot R_{\mathrm{contact}}) + (1 - K_{\mathrm{r}}) \cdot V_{\mathrm{sb,d}}, \tag{7.20}$$

$$V_{\mathrm{d,contact}} = |I_{\mathrm{ds}}| \cdot K_{\mathrm{r}} \cdot R_{\mathrm{contact}} + K_{\mathrm{r}} \cdot V_{\mathrm{sb,d}} \tag{7.21}$$

where K_{r} is a fitting parameter which is denoted as the redistribution factor. As can be seen, if $K_{\mathrm{r}} = 1$, the model behaves as in experiment 2. If, by contrast $K_{\mathrm{r}} = 0$, the complete voltage drop at the drain contact is assigned to the source. In Fig. 7.22, the results of the model in comparison to the TCAD simulations are shown where experiment 3 is conducted. The parameter K_{r} has been assigned a value of 0.25. It can be seen that with the help of param-

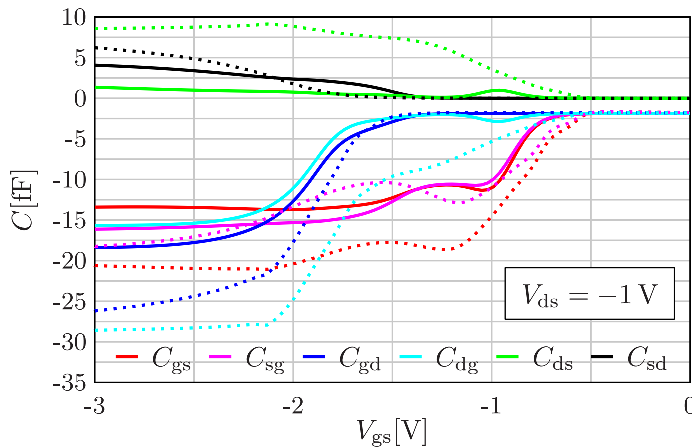

Figure 7.22.: Quasistatic capacitances of a short-channel staggered OTFT at a fixed drain-source voltage of $V_{\mathrm{ds}} = -1\,\mathrm{V}$. The channel length of the transistor is $L_{\mathrm{ch}} = 2\,\mu\mathrm{m}$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The parameters of the TCAD setup and the compact model are the same as in Fig. 7.17. Here, the contact voltages are calculated according to experiment 3: $V_{\mathrm{s,contact}} = |I_{\mathrm{ds}}| \cdot \left(R_{\mathrm{sb,s}} + (1 - K_{\mathrm{r}}) \cdot R_{\mathrm{contact}}\right) + (1 - K_{\mathrm{r}}) \cdot V_{\mathrm{sb,d}}$ and $V_{\mathrm{d,contact}} = |I_{\mathrm{ds}}| \cdot K_{\mathrm{r}} \cdot R_{\mathrm{contact}} + K_{\mathrm{r}} \cdot V_{\mathrm{sb,d}}$. The parameter K_{r} is chosen as 0.25.

eter K_r, the model is capable of realizing the crossing of C_gs and C_gd. However, the overall agreement is still very low. Please recall that due to the principle of charge conservation, the capacitances C_gs and C_gd sum up to the capacitance C_gg. Looking at the results of experiments 1 and 2 (Figs. 7.21 and 7.22), it can be seen that at high absolute values of V_gs, the sum of the capacitances C_gs and C_gd according to the compact model has a too low absolute value compared to the TCAD simulation results. In other words: Even, if the redistribution factor K_r allows for a redistribution of the contact voltages (and consequently for a redistribution of C_gs and C_gd), there remains the problem that especially at high absolute values of V_gs the capacitances are calculated too small by the compact model.

Experiment 4: Redistribution of the Contact Voltages and Introduction of a Fitting Function

The observations so far show that the redistribution factor K_r is useful for the control of the crossing of the capacitances C_gs and C_gd at the plot versus V_gs. In this experiment, a fitting function is derived which helps to solve the problem of the sum of C_gs and C_gd being too small in the linear regime of operation. Looking at the results of experiment 2 in Fig. 7.21, it becomes evident that the capacitances C_gs and C_gd show a rather good agreement in the off-state ($-1\,\mathrm{V} \leq V_\mathrm{gs} \leq 0\,\mathrm{V}$) and in the saturation regime of operation ($-2\,\mathrm{V} \leq V_\mathrm{gs} \leq -1\,\mathrm{V}$). Therefore, a function has to be found that alters the influence of the contact resistances only in the linear regime of operation. The following function is defined as a fitting function:

$$f_\mathrm{fit} = K_\mathrm{fit} \cdot \frac{Q'_\mathrm{ms} - Q'_\mathrm{md,barr}}{Q'_\mathrm{ms}}, \tag{7.22}$$

where K_fit is a fitting parameter and Q'_ms and $Q'_\mathrm{md,barr}$ are the charge densities per gate area at the source/drain end of the channel according to the DC model. The fitting function has the following properties:

- In the sub-threshold regime, the charge densities Q'_ms and $Q'_\mathrm{md,barr}$ are exponentially dependent on the voltage V_gs or $V_\mathrm{gd} = V_\mathrm{gs} - V_\mathrm{ds}$, see Eq. (2.29). If a drain-source voltage is applied, the charge density $Q'_\mathrm{md,barr}$ becomes some orders of magnitude smaller than Q'_ms. Consequently, f_fit converges to K_fit.
- In the saturation regime of operation, the carrier channel is pinched off before the drain electrode [39]. Consequently, $Q'_\mathrm{md,barr} << Q'_\mathrm{ms}$. Similarly as in the sub-threshold regime of operation, f_fit is nearly constant and converges to K_fit.
- In the linear regime of operation, the charge densities Q'_ms and $Q'_\mathrm{md,barr}$ are similar. In case of $V_\mathrm{ds} = 0\,\mathrm{V}$, they become equal. Consequently, f_fit converges to zero.

This function is used in order to define the voltage drops across the contacts:

$$V_{\mathrm{s,contact}} = |I_{\mathrm{ds}}| \cdot (f_{\mathrm{fit}} \cdot R_{\mathrm{sb,s}} + (1 - K_{\mathrm{r}}) \cdot f_{\mathrm{fit}} \cdot R_{\mathrm{contact}}) + (1 - K_{\mathrm{r}}) \cdot V_{\mathrm{sb,d}}, \tag{7.23}$$

$$V_{\mathrm{d,contact}} = |I_{\mathrm{ds}}| \cdot K_{\mathrm{r}} \cdot f_{\mathrm{fit}} \cdot R_{\mathrm{contact}} + K_{\mathrm{r}} \cdot V_{\mathrm{sb,d}}. \tag{7.24}$$

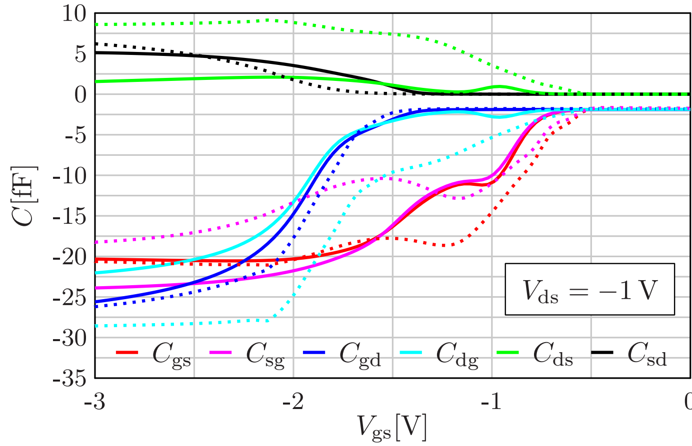

Figure 7.23.: Quasistatic capacitances of a short-channel staggered OTFT at a fixed drain-source voltage of $V_{\mathrm{ds}} = -1\,\mathrm{V}$. The channel length of the transistor is $L_{\mathrm{ch}} = 2\,\mu\mathrm{m}$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The parameters of the TCAD setup and the compact model are the same as in Fig. 7.17. Here, the contact voltages are calculated according to experiment 4: $V_{\mathrm{s,contact}} = |I_{\mathrm{ds}}| \cdot \left(f_{\mathrm{fit}} \cdot R_{\mathrm{sb,s}} + (1 - K_{\mathrm{r}}) \cdot f_{\mathrm{fit}} \cdot R_{\mathrm{contact}}\right) + (1 - K_{\mathrm{r}}) \cdot V_{\mathrm{sb,d}}$ and $V_{\mathrm{d,contact}} = |I_{\mathrm{ds}}| \cdot K_{\mathrm{r}} \cdot f_{\mathrm{fit}} \cdot R_{\mathrm{contact}} + K_{\mathrm{r}} \cdot V_{\mathrm{sb,d}}$. The parameters are chosen as follows: $K_{\mathrm{r}} = 0.15$ and $K_{\mathrm{fit}} = 0.24$.

Figure 7.23 depicts the results for the case that experiment 4 is conducted. As can be seen, the capacitances C_{gs} and C_{gd} now show a better agreement. The fitting function is a proper way of masking the linear regime of operation and conducting an operation-point dependent multiplication of different components of the contact resistance. It can be seen that the capacitance C_{gs} now shows less agreement in the saturation regime of operation ($-2\,\mathrm{V} \leq V_{\mathrm{gs}} \leq -1\,\mathrm{V}$) when compared to experiment 2 but the overall agreement over the whole voltage range is improved. Even if there is still room for improvement, this is the version of the model that will be taken for further analyses.

Observing the plots of experiments 1 to 4, an important fact becomes visible: Even if the capacitances C_{gs} and C_{gd} now show a better agreement, the other capacitances still need to be re-engineered. Especially with regard to C_{sg} and C_{dg}, it can be concluded that the charge partitioning scheme needs to be investigated. In the model, the partitioning scheme according to Ward and Dutton [65] is used. However, the problems of the capacitances C_{sg} and C_{dg} reveal that the charge partitioning does not work completely correctly.

7.3.2.2 Re-Engineering of the Charge-Partitioning Scheme

In this section, the charge-partitioning scheme will be re-engineered. If the OTFT is operated at high V_{gs}, more charge has to be attributed to be under control of the drain than under the control of the source terminal since the capacitance C_{dg} exhibits a larger absolute value than C_{sg}. For this purpose, the weighting functions of the Ward-Dutton-partitioning scheme are

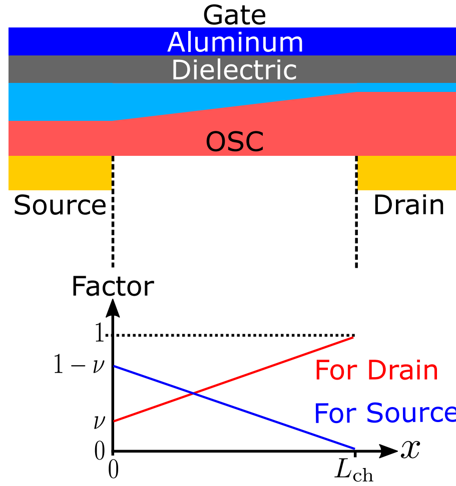

Figure 7.24.: Weighting functions of the partitioning scheme according to Ward and Dutton [65] which are modified by different starting points at the source end of the channel. The total channel charges are multiplied by the functions that are plotted below the sketch of the transistor.

modified as depicted in Fig. 7.24. In order to give less weight to the source and more weight to the drain, the weighting function for the charges associated with the source does not start at a value of 1 at the source end of the channel but at a reduced value of $1-\nu$ where $\nu \in [0,1]$ is a fitting parameter. In order to stick to the principle of charge conservation, the weighting function for the drain is increased by the same amount that the weighting function for the source is decreased. Therefore, the weighting function for the drain starts no longer at a value of 0 at the source end of the channel but at a value of ν. In other words: Charges that are located directly at the source end of the channel are attributed to a certain degree to be under control of the drain potential. The two weighting functions read as follows:

$$w_{\mathrm{s}}(x) = -\frac{1-\nu}{L_{\mathrm{ch}}} \cdot x + 1 - \nu, \tag{7.25}$$

$$w_{\mathrm{d}}(x) = \frac{1-\nu}{L_{\mathrm{ch}}} \cdot x + \nu. \tag{7.26}$$

Incorporating these charge partitioning equations, the integrals for the source and drain charges are recalculated:

$$Q_{\mathrm{d}} = W_{\mathrm{ch,G}} \int_{0}^{L_{\mathrm{ch}}} w_{\mathrm{d}}(x) \cdot Q'_{\mathrm{m}}(x)\, dx, \tag{7.27}$$

$$Q_{\mathrm{s}} = W_{\mathrm{ch,G}} \int_{0}^{L_{\mathrm{ch}}} w_{\mathrm{s}}(x) \cdot Q'_{\mathrm{m}}(x)\, dx. \tag{7.28}$$

The solutions of these two integrals are calculated based on the same substitutions as presented in Chap. 4. Since the resulting expressions are rather long they are presented in Appendix A. The new charge partitioning is introduced to capture the asymmetric influences of the Schottky barriers at the source and drain contacts on the capacitances. Since the resistance of the Schottky barrier at the source contact is larger than that at the drain contact the source terminal has less control over the charges than in a transistor without Schottky barriers. Equally as in Chap. 4, the asymptotic switching of the charges for $V_{\mathrm{ds}} = 0\,\mathrm{V}$ has to be accounted for. In this case, the charge densities Q'_{ms} and Q'_{md} at the source and drain end of the channel are nearly equal. Since no current flows, the voltage drops across the contact elements can be assumed as zero and the charge density Q'_{m} can be assumed to be independent of the position x in the channel. As a consequence, the charge integrals for the zero case reduce to:

$$Q_{\mathrm{d,zero}} = W_{\mathrm{ch,G}} \cdot Q'_{\mathrm{ms}} \cdot \int_{0}^{L_{\mathrm{ch}}} \left(\frac{1-\nu}{L_{\mathrm{ch}}} \cdot x + \nu \right) dx, \tag{7.29}$$

$$Q_{\mathrm{s,zero}} = W_{\mathrm{ch,G}} \cdot Q'_{\mathrm{ms}} \cdot \int_{0}^{L_{\mathrm{ch}}} \left(-\frac{1-\nu}{L_{\mathrm{ch}}} \cdot x + 1 - \nu \right) dx. \tag{7.30}$$

These two equations can be evaluated as:

$$Q_{\mathrm{d,zero}} = W_{\mathrm{ch,G}} \cdot Q'_{\mathrm{ms}} \cdot \frac{1}{2} \cdot L_{\mathrm{ch}} \cdot (1+\nu)\,, \tag{7.31}$$

$$Q_{\mathrm{s,zero}} = W_{\mathrm{ch,G}} \cdot Q'_{\mathrm{ms}} \cdot \frac{1}{2} \cdot L_{\mathrm{ch}} \cdot (1-\nu)\,. \tag{7.32}$$

$$\tag{7.33}$$

Finally, the smooth switching functions defined in Eqs. (4.18) and (4.19) are used to connect the non-zero-case charge in Eqs. (7.27) and (7.28) to the newly defined zero-case charges.

In staggered transistors, the charge density Q'_{ms} is not only present at the source end of the channel but in the whole gate-to-source overlap region. A certain amount of these overlap charges is as well assumed to be under control of the drain. Consequently, the expressions for the extrinsic charges in staggered transistors (Eqs. (4.30) and (4.31)) need to be modified as follows:

$$Q_{\mathrm{ex,S,stag,new}} = (1-\nu)\cdot Q_{\mathrm{ex,S,stag}} \tag{7.34}$$

$$Q_{\mathrm{ex,D,stag,new}} = Q_{\mathrm{ex,D,stag}} + \nu\cdot Q_{\mathrm{ex,S,stag}}. \tag{7.35}$$

In coplanar transistors, a redistribution of the extrinsic charges is not necessary since the source and drain electrodes are directly interfacing the gate dielectric. Thus, the contact resistances have no influence on the capacitance arising from the gate-to-contact overlaps. It could be considered, whether in coplanar transistors under the presence of fringe regions the accumulated charges next to the source/drain electrodes could be redistributed, as well, but this has not been investigated in more detail.

Figure 7.25 shows the quasistatic capacitance model incorporating the new charge partitioning scheme and the contact voltage drops according to experiment 4 (Sec. 7.3.2.1) in comparison to the TCAD simulation results. It can be seen that the agreement of the modeled and TCAD-simulated capacitances C_{sg}, C_{dg}, C_{sg} and C_{ds} has improved in comparison to the initial model equations (Fig. 7.17). For the sake of completeness, in Fig. 7.26, the capacitances are shown with respect to V_{ds}. Also here, it can be seen that there is some agreement but still the results can be improved in the future.

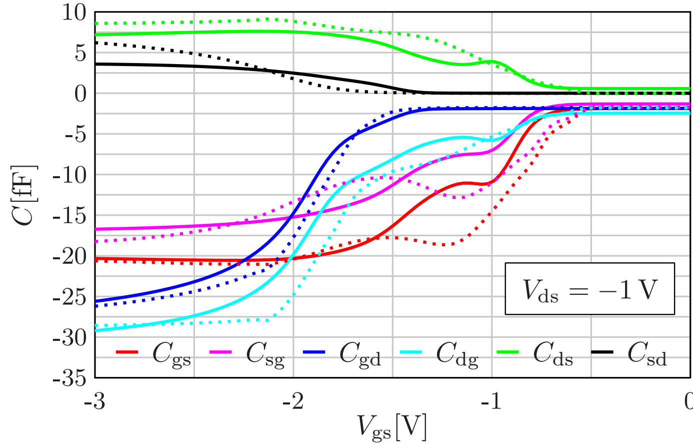

Figure 7.25.: Quasistatic capacitances of a short-channel ($L_{ch} = 2\,\mu m$) staggered OTFT at a fixed drain-source voltage of $V_{ds} = -1\,V$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The parameters of the TCAD setup and the compact model are the same as in Fig. 7.17. Here, the contact voltages are calculated according to experiment 4 (Sec. 7.3.2.1) and the new charge partitioning scheme is used. The parameters are chosen as follows: $K_r = 0.15$, $K_{fit} = 0.24$, and $\nu = 0.3$.

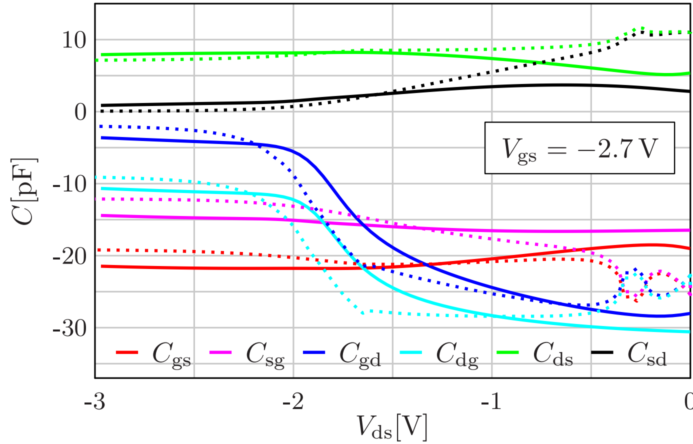

Figure 7.26.: Quasistatic capacitances of a short-channel ($L_{ch} = 2\,\mu m$) staggered OTFT at a fixed gate-source voltage of $V_{gs} = -2.7\,V$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The parameters of the TCAD setup and the compact model are the same as in Fig. 7.17. Here, the contact voltages are calculated according to experiment 4 (Sec. 7.3.2.1) and the new charge partitioning scheme is used. The parameters are chosen as follows: $K_r = 0.15$, $K_{fit} = 0.24$, and $\nu = 0.3$.

The investigation on short-channel transistors presented so far is based on staggered transistors. However, the influence of the contact resistances on the total charges are the same in coplanar and staggered transistors. A 2D Sentaurus TCAD simulation of a coplanar transistor with the following parameters is set up: An organic semiconductor with an electron affinity of $\chi_{\mathrm{osc}} = 1.81\,\mathrm{eV}$, a bandgap of $E_{\mathrm{g}} = 3.38\,\mathrm{eV}$, a constant electron mobility of $\mu_{\mathrm{n}} = 1 \times 10^{-10}\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$, and a constant hole mobility of $\mu_{\mathrm{p}} = 6\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ is conducted. For simplicity, the density of states is assumed as a square-root function such as in crystalline semiconductors with an effective density of $N_{\mathrm{v}} = 6 \times 10^{21}\,\mathrm{cm}^{-3}$. The relative dielectric permittivities of the organic semiconductor in the case of depletion and the gate dielectric are set as $\varepsilon_{\mathrm{r,osc}} = 3$ and $\varepsilon_{\mathrm{r,diel}} = 4$, respectively. The work function of the gate electrode is set to $\Phi_{\mathrm{m,g}} = 4.1\,\mathrm{eV}$ and the work function of the source/drain electrodes is altered between $\Phi_{\mathrm{m,sd}} = 5.19\,\mathrm{eV}$ and $\Phi_{\mathrm{m,sd}} = 4.7\,\mathrm{eV}$ in order to simulate one transistor with only Ohmic contacts and one transistor with Schottky barriers at the metal-to-semiconductor junctions. In case of the transistor comprising Schottky barriers, the Schottky-barrier-lowering effect is activated. The channel length and width are chosen as $L_{\mathrm{ch}} = W_{\mathrm{contact}} = W_{\mathrm{ch,SD}} = 1\,\mu\mathrm{m}$, the gate-to-contact overlap lengths are set to $L_{\mathrm{ov,GD}} = L_{\mathrm{ov,GS}} = 0.035\,\mu\mathrm{m}$, the gate-dielectric thickness is set to $t_{\mathrm{diel}} = 5.3\,\mathrm{nm}$, and a thickness of the organic semiconductor of $t_{\mathrm{osc}} = 25\,\mathrm{nm}$ is used. A constant Ohmic contact resistance at the source and drain electrodes of $R_{\mathrm{c}} = 6 \times 10^4\,\Omega$ is set.

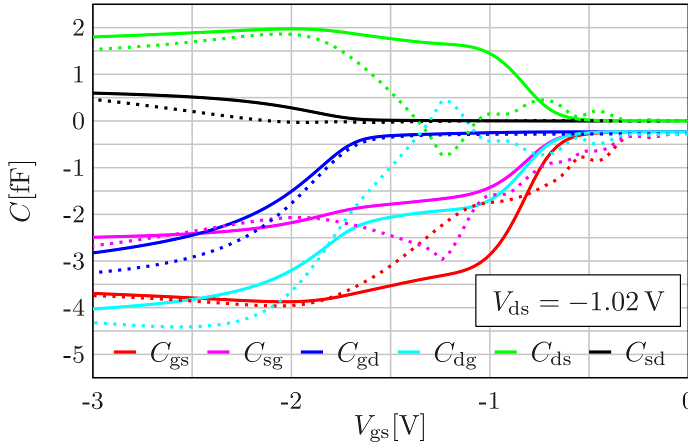

Figure 7.27.: Quasistatic capacitances of a short-channel coplanar OTFT at a fixed drain-source voltage of $V_{\mathrm{ds}} = -1.02\,\mathrm{V}$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines) with a channel length of $L_{\mathrm{ch}} = 1\,\mu\mathrm{m}$ and Schottky barriers at the source/drain electrodes of $\Phi_{\mathrm{B0}} = 0.49\,\mathrm{eV}$. In the compact model, the following fitting parameters are used: $V_{\mathrm{T0}} = -0.9\,\mathrm{V}$, $S_{\mathrm{obs}} = 80\,\mathrm{mV/dec}$, $R_{\mathrm{contact}} = 1.2819 \times 10^5\,\Omega$, $\kappa = 3.4313\,\mathrm{cm}^2\mathrm{V}^{-\beta-1}\mathrm{s}^{-1}$, $\beta = 1.1173$, $\lambda = 0.0345\,\mathrm{V}^{-1}$. The non-linear injection model [47] is fitted using the following parameters: $\eta = 2$, $\theta = 2$, $w_{\mathrm{sat}} = 0.7543$. The distance from the gate dielectric to the representative barrier height is chosen as $d_{\mathrm{B}} = 1.7644\,\mathrm{nm}$ and the thickness of the accumulation channel is assumed as $d_{\mathrm{m}} = 5\,\mathrm{nm}$. Here, the contact voltages are calculated according to experiment 4 (Sec. 7.3.2.1) and the new charge partitioning scheme is used. The parameters are chosen as follows: $K_{\mathrm{r}} = 0.8$, $K_{\mathrm{fit}} = 0.1$, and $\nu = 0.28$.

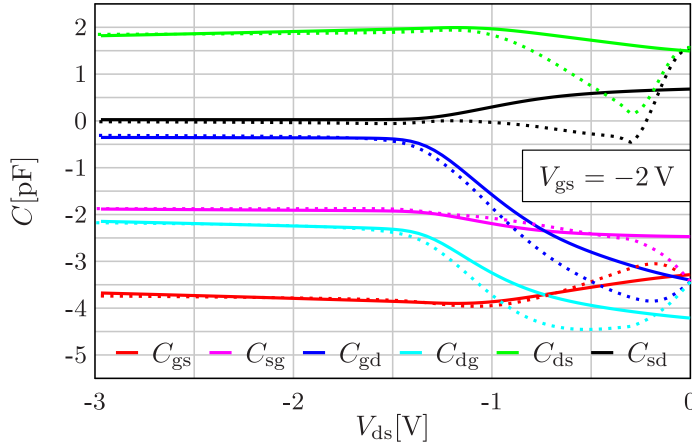

Figure 7.28.: Quasistatic capacitances of a short-channel coplanar OTFT at a fixed gate-source voltage of $V_{gs} = -2\,V$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The parameters of the TCAD setup and the compact model are the same as in Fig. 7.27. Here, the contact voltages are calculated according to experiment 4 (Sec. 7.3.2.1) and the new charge partitioning scheme is used. The parameters are chosen as follows: $K_r = 0.8$, $K_{fit} = 0.1$, and $\nu = 0.28$.

A frequency of $f = 1 \times 10^{-3}\,Hz$ is chosen in order to obtain the quasistatic capacitances. Figures 7.27 and 7.28 show the quasistatic capacitance model in comparison to the TCAD simulation results once versus V_{gs} and once versus V_{ds}. Since the gate-to-contact overlap capacitances have a big impact in coplanar transistors the overlap lengths $L_{ov,GS}$ and $L_{ov,GD}$ are chosen quite small in this simulation. It can be seen that the model shows a good agreement with the simulation results at large values of V_{ds} and V_{gs} but for quite small voltages, there is still room for improvement.

7.3.3 Parameter Extraction

In this section, the procedure of fitting the newly defined models to the results of a TCAD simulation will be explained based on a staggered transistor. This process is also known as the parameter extraction. The challenge during the fitting process is that both K_{fit} and K_r have an influence on the capacitances. As a consequence, a sufficient agreement between the model and the TCAD simulation results can be obtained using several combinations of the parameter values. However, a procedure will be presented that leads to a reasonable fitting.

1. Observing C_{gs} and C_{gd}

The first step is to determine a reasonable fitting of the capacitances C_{gs} and C_{gd} by adjusting K_{fit} and K_r. These two capacitances are independent of the charge partitioning scheme since they are based on the total gate charges and hence on the total channel charges. Figure 7.29 shows the capacitances C_{gs} and C_{gd} of a staggered short-channel OTFT. The model is compared

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Jakob Simon Leise

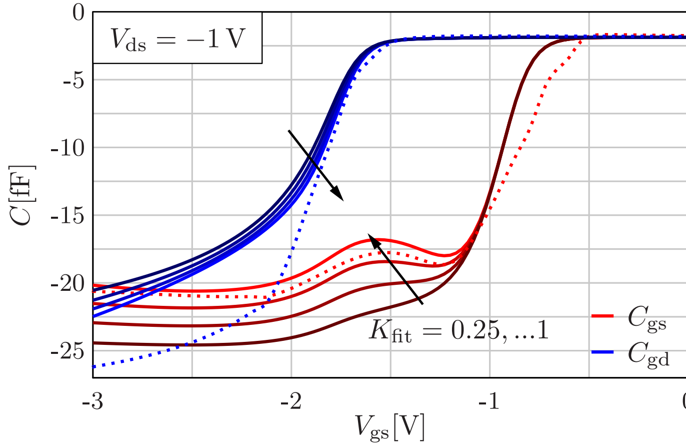

Figure 7.29.: Quasistatic capacitances C_{gs} and C_{gd} of a staggered short-channel ($L_{ch} = 2\,\mu m$) OTFT at a fixed drain-source voltage of $V_{ds} = -1\,V$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The parameters of the TCAD setup and the compact model are the same as in Fig. 7.17. Here, the contact voltages are calculated according to experiment 4 (Sec. 7.3.2.1) and the new charge partitioning scheme is used. The curves are shown for various values of the fitting parameter K_{fit} between 0.25 and 1 while a constant value of $K_r = 1$ is chosen. The arrows indicate the direction in which the curves are shifted with increasing K_{fit}.

to the TCAD simulation results and the parameter K_{fit} is varied. The arrows indicate the direction in which the curves are shifted when increasing K_{fit} from 0.25 to 1 with K_r held constant at a value of 1. It can be seen that the capacitance C_{gs} exhibits a greater dependence on K_{fit} than C_{gd}. Both of the curves are shifted towards each other with greater K_{fit}. Even if a reasonable fitting of the C_{gs} curves can be achieved, the modeled C_{gd} has a poor agreement at higher absolute values of V_{gs}. As the next step, Fig. 7.30 shows the investigation of the influence of the parameter K_r on the capacitances C_{gs} and C_{gd} with a constant value of $K_{fit} = 0.25$. K_r is altered between 0.25 and 1. It can be seen that both capacitances are greatly influenced by K_r. The curves are shifted in the direction of the arrows with increasing K_r. This investigation shows that the distinction between the influences of K_{fit} and K_r is somewhat difficult. It can be seen that both of the capacitances C_{gs} and C_{gd} show the best overall agreement for lower values of K_{fit} and K_r in this case. Even if the modeled C_{gs} deviates a little more for V_{gs} in the interval between $-1.5\,V$ and $-1\,V$, the overall agreement is good. Generally, the following procedure can be proposed for determining K_{fit} and K_r:

1. Set $K_r = 1$ and set $K_{fit} = 1$ as an initial guess.

2. Keep K_r constant and decrease K_{fit}. This will increase the absolute value of the modeled C_{gs} and decrease the absolute value of the modeled C_{gd}, see Fig. 7.29. Continue decreasing K_{fit} until the modeled C_{gs} has slightly larger value than the TCAD-simulated C_{gs} at large absolute values of V_{gs}. In case that the TCAD-simulated C_{gs} and C_{gd} do not cross

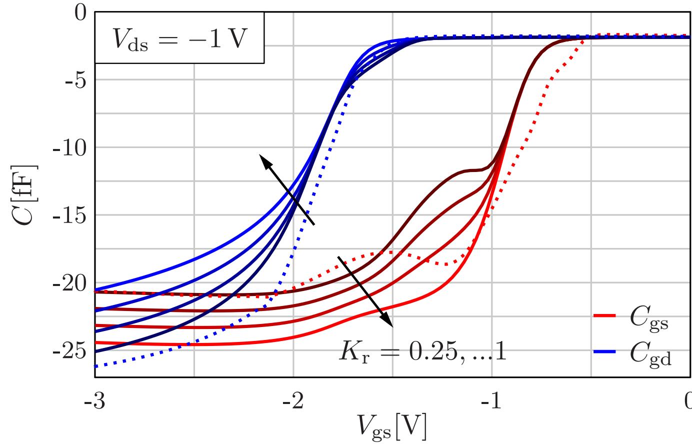

Figure 7.30.: Quasistatic capacitances C_{gs} and C_{gd} of a staggered short-channel ($L_{ch} = 2\,\mu m$) OTFT at a fixed drain-source voltage of $V_{ds} = -1$ V. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The parameters of the TCAD setup and the compact model are the same as in Fig. 7.17. Here, the contact voltages are calculated according to experiment 4 (Sec. 7.3.2.1) and the new charge partitioning scheme is used. The curves are shown for various values of the fitting parameter K_r between 0.25 and 1 while a constant value of $K_{fit} = 0.25$ is chosen. The arrows indicate the direction in which the curves are shifted with increasing K_r.

each other (which can happen in coplanar transistors), it may be impossible to increase the absolute value of C_{gs} to be larger than the TCAD-simulated value. In this case, it is sufficient if the modeled C_{gs} is almost identical to the simulated value.

3. Decrease K_r. In accordance with Fig. 7.30, this will shift the absolute value of the modeled C_{gs} towards smaller values and shift the absolute value of the modeled C_{gd} towards larger values. Continue decreasing K_r until a sufficient fitting is reached. If the fitting is not acceptable, repeat this step once with K_{fit} increased by 0.1 and once with K_{fit} decreased by 0.1. If any of the cases provides a better fitting, continue by setting K_{fit} again a little further in the direction that provided the better fitting.

2. Observing C_{sg} and C_{dg}

Having determined meaningful values of K_{fit} and K_r, the next step is to determine the proper value of the parameter ν. This is much simpler since ν is the only parameter that alters the charge partitioning scheme. Since C_{sg} and C_{dg} are dependent on the charges associated with the source and the drain terminals they can be used in order to observe the charge partitioning scheme. Figure 7.31 shows the capacitances C_{sg} and C_{dg} with increasing values for the parameter ν. The goal of this step is to obtain a good agreement of both capacitances at high absolute values of V_{gs}.

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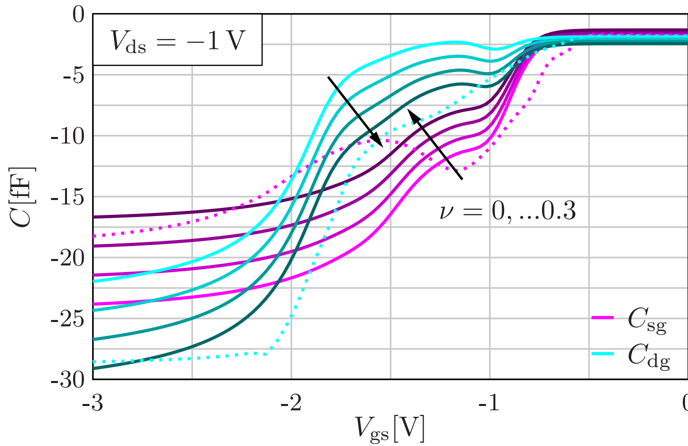

Figure 7.31.: Quasistatic capacitances C_{sg} and C_{dg} of a staggered short-channel ($L_{ch} = 2\,\mu m$) OTFT at a fixed drain-source voltage of $V_{ds} = -1\,V$. The compact model (solid lines) is compared to the results of a TCAD simulation (dotted lines). The parameters of the TCAD setup and the compact model are the same as in Fig. 7.17. Here, the contact voltages are calculated according to experiment 4 (Sec. 7.3.2.1) and the new charge partitioning scheme is used. The curves are shown for various values of the fitting parameter ν between 0 and 0.3 with the other two fitting parameters held constant at $K_{fit} = 0.25$ and $K_r = 0.25$. The arrows indicate the direction in which the curves are shifted with increasing ν.

7.4 High-Frequency Investigation of Short-Channel Transistors

7.4.1 Basic discussion

In this section, a model for the description of the high-frequency behavior in OTFTs comprising short channel lengths and larger contact resistances is shown. In Sec. 7.2, the channel segmentation approach is used to capture the high-frequency behavior of long-channel transistors. As outlined, the model only provides a suitable description if the channel is comparatively long so that the charging and discharging of channel segments through adjacent channel segments is the dominating time-dependent effect. Furthermore, only transistors with small contact resistances can be described properly by this model since the influence of the contact resistances on the charge densities (compare Fig. 7.18) is not considered. Accordingly, for a proper description of the high-frequency behavior of short-channel transistor, an additional way has to be found. An empirical, yet closed-form model for the frequency-dependent small-signal gain of staggered and coplanar OTFTs has been developed and presented in ref. [55].

One option to measure the high-frequency behavior of transistors is to measure the capacitance-voltage characteristics such as in ref. [40]. However, when the transistor is operated in an electric circuit, it might be more interesting to investigate the frequency-dependent amplification behavior. If, for instance, the gate-source voltage of a transistor is quickly altered, it is of

interest how the drain current reacts. Often, the so-called small-signal current gain h_{21} is used as the measure for the small-signal amplification behavior. It is defined as the ratio of the small-signal drain current and the small-signal gate current [107]:

$$h_{21} = \frac{i_{\mathrm{d}}}{i_{\mathrm{g}}} \tag{7.36}$$

where i_{d} and i_{g} are the small-signal components of the drain current and the gate current, respectively. Under steady-state DC conditions, the gate current I_{g} of a transistor is nearly zero due to the insulating properties of the gate dielectric which may conduct a small leakage current. However, if the transistor is operated under AC conditions, capacitive charging currents come into play. The amounts of charges at the gate electrode and in the channel of the transistor are always equal. Consequently, the capacitive charging currents of the gate electrode constitute the small-signal gate current i_{g}.

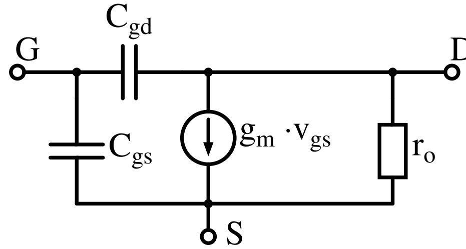

Figure 7.32.: Equivalent small-signal circuit of a TFT. Here, the capacitances are assumed as lumped elements. This figure was published in ref. [55].

In Fig. 7.32, a simplified small-signal circuit of a TFT is depicted. The capacitances between the gate and the source/drain electrodes are depicted as lumped elements and the drain current is described by the transconductance g_{m} multiplied by the small-signal gate-source voltage. Furthermore, there may be an output resistance r_{o} representing the effect of a channel-length modulation. From Chap. 3, it is known that in principle, the capacitances of a transistor are non-reciprocal, i.e. $C_{\mathrm{gs}} \neq C_{\mathrm{sg}}$ and $C_{\mathrm{gd}} \neq C_{\mathrm{dg}}$. This non-reciprocity cannot be described in an equivalent circuit and thus, closed-form equations cannot be derived if this non-reciprocity has to be accounted for. However, an advantage of the transistors presented in ref. [55] is that their gate-to-contact overlap lengths are large in comparison to their channel lengths. In contrast to the intrinsic capacitances, the overlap capacitances are reciprocal since it does not make a difference for the charge carriers, whether the potential at the gate or at the source/drain electrode is changed. Therefore, the simplified view of reciprocal, lumped capacitors is still valid. Based on the equivalent circuit depicted in Fig. 7.32, an analysis of the mesh and node equations can be conducted leading to a closed-form expression for the small-signal gain:

$$h_{21} = \frac{g_{\mathrm{m}} - j2\pi f C_{\mathrm{gd}}}{j2\pi f\left(C_{\mathrm{gs}} + C_{\mathrm{gd}}\right)}. \tag{7.37}$$

This rather simple equation provides a full picture of the small-signal amplification behavior of an ideal TFT. In the literature, most often the so-called transit frequency f_{T} is used as the unit of measure for the small-signal behavior of a transistor [46]. It is defined as the frequency at which the absolute value of h_{21} becomes one. In case of a standard MOSFET or TFT, an analytical expressiion for f_{T} can be derived. For this purpose, the transconductance can be calculated by deriving the MOSFET current equation [5] with respect to the gate-source voltage. Furthermore, as explained in Chap. 3, the capacitances of a transistor in a simplified form can be expressed by the Meyer model [38, 87]. Based on this, the transit frequency of an ideal TFT comprising parallel-plate capacitors as gate-to-contact overlap capacitances can be expressed as follows [42]:

$$f_{\mathrm{T}} = \frac{\mu_{\mathrm{eff}} \left(V_{\mathrm{gs}} - V_{\mathrm{T0}} \right)}{2\pi L_{\mathrm{ch}} \left(\frac{2}{3} L_{\mathrm{ch}} + L_{\mathrm{ov,GS}} + L_{\mathrm{ov,GD}} \right)}. \tag{7.38}$$

However, in sub-micrometer-channel-length OTFTs, the simplifications made in this equation do not hold true. In the course of this chapter, it has been shown that the contact effects arising from Schottky barriers at the source-to-semiconductor and drain-to-semiconductor junctions require a detailed model for an accurate capturing of the capacitive behavior. The Meyer model may be sufficient for transistors with a high degree of ideality and for some applications it may not be an issue if the non-reciprocity of the capacitances is neglected. However, under the presence of contact resistances, the Meyer model cannot produce accurate results. The usage of the Meyer model is not the only drawback of Eq. (7.38). As stated above, the standard MOSFET DC current equation is analytically derived with respect to the voltage V_{gs} in order to obtain an expression for g_{m}. However, this standard model is not capable of capturing the effects that occur in OTFTs such as the effects of traps [36] or the non-linear injection at the source-to-semiconductor junction [47]. In principle, contact resistances lead to a reduction of the effective mobility (μ_{eff}) which according to Eq. (7.38) also leads to a reduction of the transit frequency. However, the equation cannot capture the effect that the charge densities in the transistor are varied due to the contact resistances, see Fig. 7.18. The Meyer model cannot take into account the voltage drop across the contact resistances in the calculation of the total charges. Another critical point about Eq. (7.38) is that the contribution of the overlap capacitances is included in a very simplified form. It is assumed that the overlap capacitances behave like parallel-plate capacitors consisting of the source/drain electrode and the gate electrode which are separated from each other by the gate dielectric. As explained in Chap. 4, this assumption may be made for coplanar transistors without fringe regions. However, transistors fabricated in the staggered architecture show a different behavior since the gate-to-contact overlap regions consist of a stack of the organic semiconductor and the gate dielectric. In dependence on the applied voltages, the behavior of these overlap regions significantly differs from that of a coplanar transistor, see Chap. 4. Furthermore, fringe regions between the source/drain fingers (in case of a multi-finger layout) and beyond the first and the last electrode have an influence on the extrinsic capacitances so that the simplified assumption

in Eq. (7.38) does not accurately describe the properties of OTFTs. The points mentioned in this discussion directly limit the increase in f_T that could theoretically be expected from a miniaturization of the device geometry. In the research community, it is thus always of great interest to reduce the contact resistances of the transistors. Recent developments of materials [19, 20] and new processing approaches [21] have lead to a massive improvement of the contact resistances. Width-normalized contact resistances ($R_C W$) of less than 100 Ωcm, often in combination with measured transit frequencies of several tens of megahertz have been reported [13, 43, 59, 108]. Table B.1 in Appendix B gives a literature overview over OTFTs for which a transit frequency of at least 3.5 MHz has been measured.

7.4.2 Modeling

In this section, a closed-form model for the description of the non-quasistatic effects is discussed as presented in ref. [55]. For the compact model describing the total charges, it has been assumed so far that the charges are independent of the position along the z-axis of the device (Fig. 4.2) where the z-axis points in the direction of the channel width. In other words: The investigations on 3D TCAD simulations have revealed that the density of accumulated quasi-mobile charges is nearly constant for every position along the channel width independent of whether a point in the geometric channel center or beyond the channel center in the fringe regions is regarded. This assumption is also made for the charges in the fringe regions directly next to the electrodes. These regions are denoted as electrode regions in Fig. 4.2. For a quasistatic operation, these assumptions can safely be made which is verified in Sec. 6.3.2.1. However, in case of a high-frequency operation, the location of the charges in the transistor is of importance. Since accumulation charges cannot be created or disappear by recombination, they have to enter or leave the device through the device terminals. Consequently, points farther

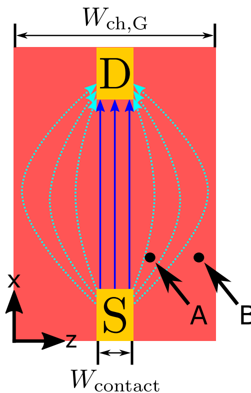

Figure 7.33.: Schematic of a cutplane in a coplanar transistor where the effect of current spreading is shown. Under quasistatic operation conditions, the charge densities in the two probe points are assumed to be equal. However, when operated at high frequencies, the change of the charge in point B is smaller than in point A. This picture was published ref. [54] and was slightly modified.

away from the channel center are charged or discharged more slowly than points in the in the channel center. This is visualized in Fig. 7.33 where the current in a cutplane close to the gate dielectric of a coplanar transistor is shown. Under quasistatic conditions, the charge densities in points A and B are equal. However, under high-frequency conditions, the change of the charge density in point A is higher than the change of the charge density in point B. In ref. [109], the change of the capacitances with increasing frequencies is modeled as a frequency-dependent change in the relative permittivity of the gate dielectric. However, as depicted in Fig. 7.34,

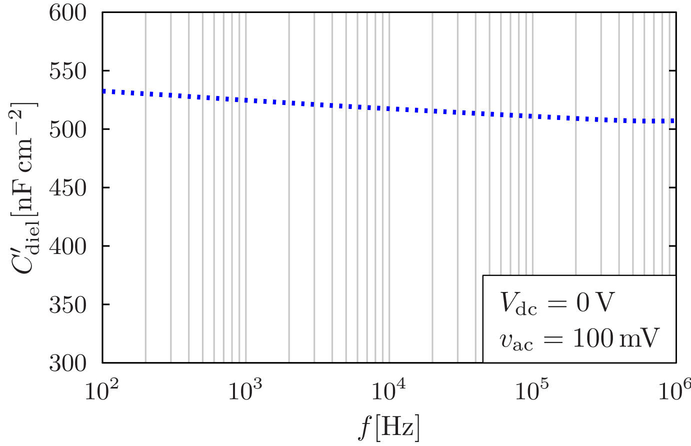

Figure 7.34.: Measured capacitance per area of the gate dielectric used in this investigation (aluminum oxide and self-assembled monolayer of n-tetradecylphosphonic acid). This figure was published in ref. [55].

the dielectric capacitance of the gate dielectric does not exhibit major changes with increasing frequency. The gate dielectric is a hybrid gate dielectric consisting of aluminum oxide and a self-assembled monolayer of n-tetradecylphosphonic acid which is used for the transistors under investigation in this chapter. Due to the high stability of the gate dielectric with increasing frequency the change of the capacitances is modeled as a frequency-dependent reduction of the part of the channel width that is used for the calculation of the total charges. In analogy to the function defined in ref. [109], the following scaling function is used:

$$C_{\text{scale}} = C_{\text{scale,high}} + \frac{C_{\text{scale,low}} - C_{\text{scale,high}}}{(1 + f \cdot \tau_{\text{scale}})^{p_{\text{scale}}}}. \tag{7.39}$$

The function C_{scale} converges to $C_{\text{scale,low}}$ if the frequency converges to zero and to $C_{\text{scale,high}}$ if the frequency converges to infinity. τ_{scale} is a time constant which controls the transition from the low-frequency regime to the high-frequency regime and p_{scale} is the exponent of the denominator which also influences the steepness of the transition. In Fig. 7.35, the function C_{scale} is plotted versus the frequency for an arbitrary set of fitting parameters. C_{scale} is used in the charge equations as a scaling factor for the part of the channel width that constitutes the fringe parts. This is visualized in Fig. 7.36 where the influence of C_{scale} on the channel

width that is used for the total charge calculation is shown. If $C_{\text{scale}} = 1$, the complete gate width $W_{\text{ch,G}}$ is used as the channel width. With C_{scale} decreasing, the fringe width between the fingers and beyond the first and the last finger which is taken into account is reduced. If $C_{\text{scale}} = 0$, only the geometric channel width $W_{\text{ch,SD}} = N_{\text{fing}} \cdot W_{\text{contact}}$ is used for the calculation of the charges.

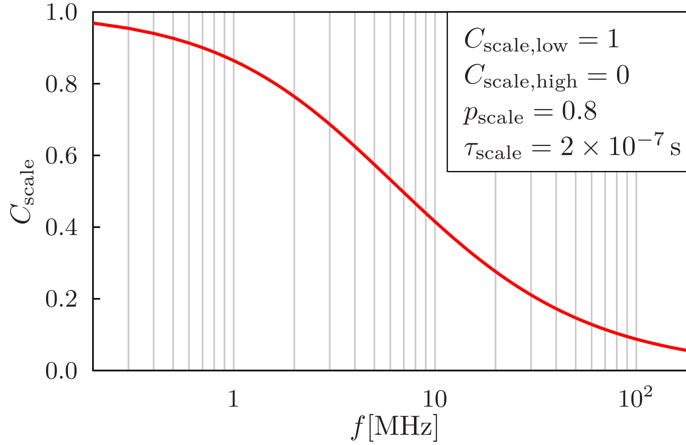

Figure 7.35.: Shape of the function C_{scale} for an arbitrary set of parameters. This figure was published in ref. [55].

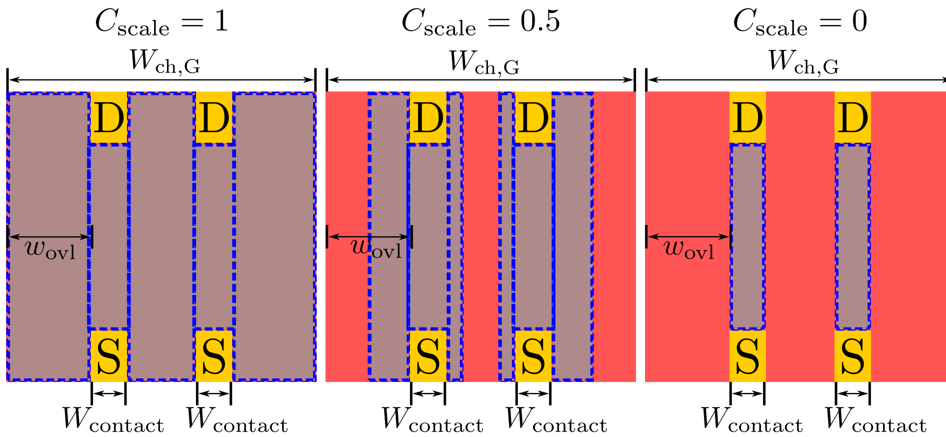

Figure 7.36.: Illustration of the influence of the function C_{scale} on the fringe areas which are used for the charge calculation. If $C_{\text{scale}} = 1$, all of the fringing charges are used for the charge calculation. If $C_{\text{scale}} = 0$, only the intrinsic and overlap charges are used whereas the fringe regions are neglected. This picture was published in ref. [55].

In addition to the charges in fringe regions, the charges in the channel center will also have a frequency-dependent behavior. Based on the same argumentation as for the fringe regions, it could be said that charges farther away from the source/drain electrodes will exhibit a more-pronounced frequency dependence whereas charges close to the source/drain electrodes can be charged easily. Assuming that the transistor is operated at such a frequency that only half of the intrinsic channel charges are effectively taken into account for the capacitance calculation, this would mean that starting at each the source and the drain electrode a region with a length of $1/4 \cdot L_{\mathrm{ch}}$ in the direction of the channel length (x) would have to be taken into account with an unmodulated region of length $1/2 \cdot L_{\mathrm{ch}}$ in the middle. For that purpose, the charge densities per gate area at the positions $x = 1/4 \cdot L_{\mathrm{ch}}$ and $x = 3/4 \cdot L_{\mathrm{ch}}$ would be required. However, the DC compact model only provides equations for the charge densities per gate area at the source end and the drain end of the channel but not at any position within the channel. In order to find an easy way to include the frequency dependence of the channel charges, rather than the channel length, the channel width of the geometric channel is scaled. A scaling function of exactly the same type as for the fringe charges is defined:

$$C_{\mathrm{scale2}} = C_{\mathrm{scale2,high}} + \frac{C_{\mathrm{scale2,low}} - C_{\mathrm{scale2,high}}}{(1 + f \cdot \tau_{\mathrm{scale2}})^{p_{\mathrm{scale2}}}}. \tag{7.40}$$

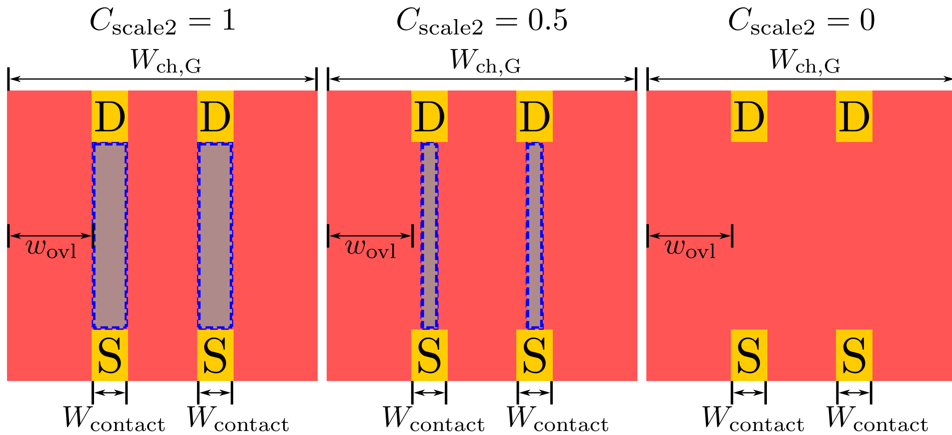

Figure 7.37.: Illustration of the geometric channel areas which are used for the charge calculation depending on the value of C_{scale2}. If $C_{\mathrm{scale2}} = 1$, all of the charges in the channel center and in case of staggered transistors the overlap charges are used for the charge calculation. If $C_{\mathrm{scale2}} = 0$, no charges in the channel center and in case of staggered transistors the overlap charges are used. This picture was published in ref. [55].

In staggered transistors, there are also accumulation charges between the gate electrode and the source/drain electrodes. These charges will also exhibit a frequency-dependence which is not necessarily the same as that of the charges in the channel. In principle, the gate-to-contact overlap regions in staggered transistor could be described as a metal-insulator-semiconductor-

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metal structure. For such structures, there exist frequency-dependent capacitance models in the literature [110] but in order to keep the model simple, the function C_{scale2} is used also as a scaling factor for the overlap charges in staggered transistors. In spite of this simplification it will be shown that this procedure leads to reasonable results. Figure 7.37 visualizes the influence of the function C_{scale2} on the parts of the channel which are taken into account for the calculation of the total charges.

Having defined the two scaling functions C_{scale} and C_{scale2}, they are incorporated into the equations for the total charges. The total amount of accumulation charges in the channel is expressed as:

$$Q_{\text{c}} = \left(C_{\text{scale}} \cdot (2w_{\text{ovl}} + (N_{\text{fing}} - 1)\, d_{\text{fing}}) + C_{\text{scale2}} \cdot N_{\text{fing}} W_{\text{contact}}\right) \cdot \int_{0}^{L_{\text{ch}}} Q'_{\text{m}}(x)\, dx. \tag{7.41}$$

This only changes the pre-factor of the solution of the equations shown in Appendix A. The integrals for the total charges associated with the source and the drain terminals (Eqs. (7.27) and (7.28)) are modified in the same way. In addition to the equations for the total charges, the expressions for the extrinsic charges in the two different transistor architectures need to be modified by means of the scaling functions as well. For coplanar transistors, the part of the extrinsic charges that is present in fringe regions needs to be multiplied by C_{scale}:

$$\begin{aligned} Q_{\text{ex,S,copl}} =& V_{\text{gs}} C'_{\text{diel}} L_{\text{ov,GS}} N_{\text{fing}} W_{\text{contact}} \\ &+ C_{\text{scale}} \left(2w_{\text{ovl}} + (N_{\text{fing}} - 1)\, d_{\text{fing}}\right) L_{\text{ov,GS}} Q'_{\text{ms}}, \end{aligned} \tag{7.42}$$

$$\begin{aligned} Q_{\text{ex,D,copl}} =& V_{\text{gd}} C'_{\text{diel}} L_{\text{ov,GD}} N_{\text{fing}} W_{\text{contact}} \\ &+ C_{\text{scale}} \left(2w_{\text{ovl}} + (N_{\text{fing}} - 1)\, d_{\text{fing}}\right) L_{\text{ov,GD}} Q'_{\text{md}}. \end{aligned} \tag{7.43}$$

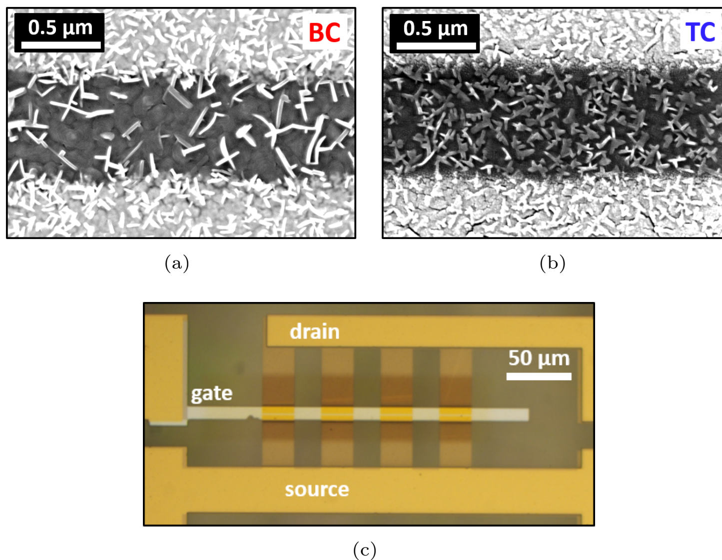
In staggered transistors, the overlap charges consist of three parts: the geometric capacitance consisting of the series connection of the gate dielectric and the depleted organic semiconductor, the accumulation charges in the overlap region and the charges in fringe regions next to the electrodes. For the charges in the fringe regions, C_{scale} is used and for the accumulation charges in the overlap region, C_{scale2} is taken:

$$\begin{aligned} Q_{\text{ex,S,stag}} =& \frac{C_{\text{diel,s}} C_{\text{osc,s}}}{C_{\text{diel,s}} + C_{\text{osc,s}}} \left(V_{\text{gs}} - \frac{Q'_{\text{ms}}}{C'_{\text{diel}}}\right) \\ &+ \left(C_{\text{scale}} \left(2w_{\text{ovl}} + (N_{\text{fing}} - 1)\, d_{\text{fing}}\right) + C_{\text{scale2}} N_{\text{fing}} W_{\text{contact}}\right) Q'_{\text{ms}} L_{\text{ov,GS}} W_{\text{ch,G}}, \end{aligned} \tag{7.44}$$

$$\begin{aligned} Q_{\text{ex,D,stag}} =& \frac{C_{\text{diel,d}} C_{\text{osc,d}}}{C_{\text{diel,d}} + C_{\text{osc,d}}} \left(V_{\text{gs}} - V_{\text{ds}} - \frac{Q'_{\text{md,barr}}}{C'_{\text{diel}}}\right) \\ &+ \left(C_{\text{scale}} \left(2w_{\text{ovl}} + (N_{\text{fing}} - 1)\, d_{\text{fing}}\right) + C_{\text{scale2}} N_{\text{fing}} W_{\text{contact}}\right) Q'_{\text{md}} L_{\text{ov,GD}} W_{\text{ch,G}}. \end{aligned} \tag{7.45}$$

7.4.3 Verification

In this section, the verification procedure of the model is explained as was presented in ref. [55]. Coplanar (bottom-contact, BC) and staggered (top-contact, TC) transistors were fabricated on flexible substrates consisting of polyethylenenaphtalate (PEN) with a thickness of 125 µm (Teonex Q65 PEN; provided by W. A. MacDonald, DuPont Teijin Films, Wilton, UK) by making use of high-resolution silicon stencil mask lithography. The gate electrodes, the source and drain contacts, the organic semiconductor and the interconnects were patterned by different masks. The gate dielectric is a hybrid gate dielectric consisting of an oxygen-plasma-grown layer of aluminum oxide (Oxford Instruments, 30 sccm oxygen, 10 mTorr, 200 W, 30 s) on top of the gate electrode consisting of aluminum. The substrate is subsequently immersed into a 1 mM 2-propanol solution of n-tetradecylphosphonic acid (TDPA; PCI Synthesis, Newburyport, MA, USA) which allows for a formation of a self-assembled monolayer (SAM). For the fabrication of the coplanar TFTs, the golden source and drain electrodes were deposited by thermal evaporation in a vacuum chamber, and afterwards, the substrates were immersed into a 10 mM solution of pentafluorobenzenethiol (PFBT; Santa Cruz Biotechnology, Heidelberg, Germany) in ethanol (nondenatured) for 30 min in a covered container at room temperature. The small-molecule organic semiconductor 2,9-diphenyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DPh-DNTT; Nippon Kayaku, kindly provided by K. Ikeda[111]) is then thermally sublimated in the vacuum (base pressure of 1×10^{-6} mbar) at a substrate temperature of 90 °C and serves as the active layer of the devices. For the fabrication of the staggered transistors, the golden source and



(a) (b) (c)

Figure 7.38.: SEM images of the channel regions of (a) a coplanar (BC) OTFT and (b) a staggered (TC) OTFT. (c) Photograph of an OTFT fabricated in a multi-finger layout. The channel length is approximately 0.7 µm. These pictures were published in ref. [55].

drain electrodes were deposited on top of the layer of DPh-DNTT using thermal evaporation in vacuum (base pressure of 1×10^{-7} mbar). The channel regions of the transistor were observed by scanning electron microscopy (SEM). In Figs. 7.38(a) and 7.38(b), the SEM images of the channel regions of a coplanar and a staggered transistor are shown.

In Fig. 7.38(c), the photo of a fully fabricated OTFT is shown. As can be seen, the transistor is fabricated in a multi-finger structure which is in this case the parallel connection of four identical TFTs where each has a width of $W_{\mathrm{contact}} = 25\,\mu\mathrm{m}$. Summed up, the geometrical channel width of the whole transistor is $W_{\mathrm{ch,SD}} = 100\,\mu\mathrm{m}$. According to the SEM images, the channel lengths of the transistors are approximately 0.7 µm. The gate-to-contact overlap lengths are varied asymmetrically. The sum of the gate-to-contact-overlap lengths, $L_{\mathrm{ov,GS}} + L_{\mathrm{ov,GD}}$, is held constant at 10 µm but $L_{\mathrm{ov,GS}}$ varies between 1 and 9 µm and $L_{\mathrm{ov,GD}}$ accordingly varies between 9 and 1 µm. With this set of transistors, the geometry-dependent influences of the gate-to-contact overlap capacitances on the high-frequency behavior can be investigated systematically.

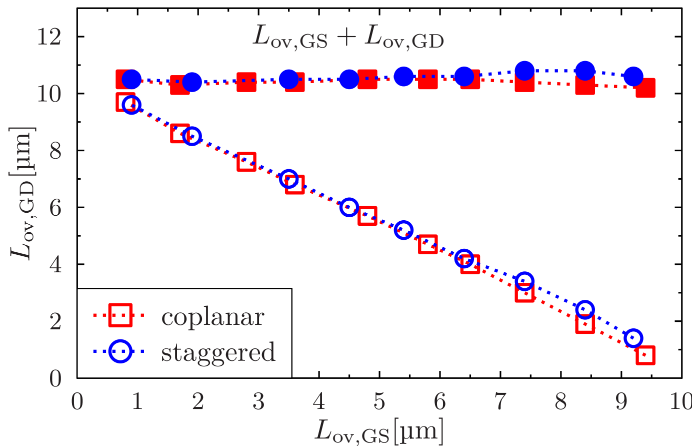


Figure 7.39.: Measured gate-to-drain overlap length in dependence of the measured gate-to-source overlap length. The sum of $L_{\mathrm{ov,GS}}$ and $L_{\mathrm{ov,GD}}$ is also depicted. The plot proves the quality of the fabrication process. The process works well for coplanar and staggered transistors. This figure was published in ref. [55].

In Fig. 7.39, the measured gate-to-drain overlap length ($L_{\mathrm{ov,GD}}$) of the fabricated coplanar and staggered transistors is shown in dependence of the measured gate-to-source overlap length ($L_{\mathrm{ov,GS}}$). Furthermore, the sum of $L_{\mathrm{ov,GS}}$ and $L_{\mathrm{ov,GD}}$ is plotted. It can be seen that the process is well-controlled and provides a very constant sum of the overlap lengths.

The DC transfer and output characteristics were measured at room temperature (292 K) using an Agilent 4156 C Semiconductor Parameter Analyzer and a custom LabView program. Furthermore, scattering parameters (S-parameters) were measured using a Keysight N5231A

Vector Network Analyzer connected to Cascade Microtech GS-SG |Z| high-frequency probes. These scattering parameters relate the incident waves of the different ports of a network to the corresponding reflected waves [112]. Methods that allow for a conversion of the S-parameters to other parameters of the network theory are presented in ref. [113]. Based on these conversions, the measured S-parameters can be transformed into the small-signal h-parameters. Thus, the small-signal gain h_{21} can be calculated directly from the measured S-parameters.

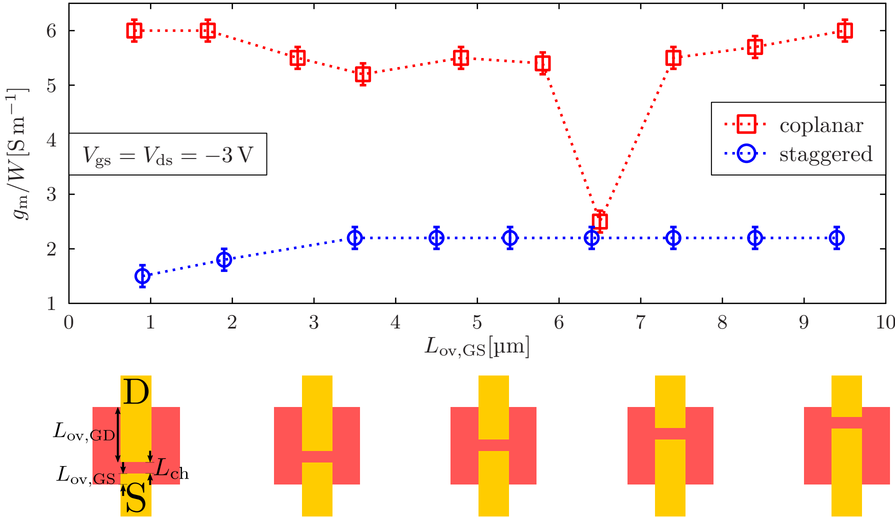


Figure 7.40.: Measured transconductances of the various fabricated coplanar and staggered transistors at an operation point of $V_{gs} = V_{ds} = -3\,V$ plotted versus the measured gate-to-source overlap length. The transconductances are normalized with respect to the geometrical channel width $W_{ch,SD} = 100\,\mu m$. The little pictogram shows the asymmetry between the two overlaps. This figure was published in ref. [55].

Figure 7.40 shows the measured width-normalized transconductances of the various fabricated OTFTs. It can be seen that the coplanar transistors show an overall higher transconductance than their staggered counterparts (except for one outlier). The reason for the larger transconductances in the coplanar technology is the notably lower contact resistance and a higher mobility which were determined as $R_C W = 35\,\Omega cm$ and $\mu_0 = 4.3\,cm^2\,V^{-1}\,s^{-1}$ by the so-called transmission-line method (TLM) in ref. [43]. A TLM analysis of the staggered transistors yields a width-normalized contact resistance of $R_C W = 61\,\Omega cm$ and a mobility of $\mu_0 = 2.7\,cm^2\,V^{-1}\,s^{-1}$. The corresponding plots of the TLM analysis of the staggered transistors and additional information are shown in Appendix B. Furthermore, as can be seen in Fig. 7.40, the transconductance of the coplanar transistors is independent of the gate-to-source overlap length. In staggered transistors, by contrast, the gate-to-source overlap length plays a role. At small $L_{ov,GS}$, a drop in the transconductance is visible. This can be attributed to the contact resistance, since the injection becomes limited at such small geometries [59, 114, 115], especially if the gate-to-source overlap length is notably shorter than the transfer length (L_T).

In agreement with previous reports [17, 43], the coplanar transistors exhibit much steeper sub-threshold swings than their staggered counterparts. In this work, the coplanar transistors exhibit sub-threshold swings as small as 70 mV/dec whereas the staggered TFTs have swings of about 230 mV/dec.

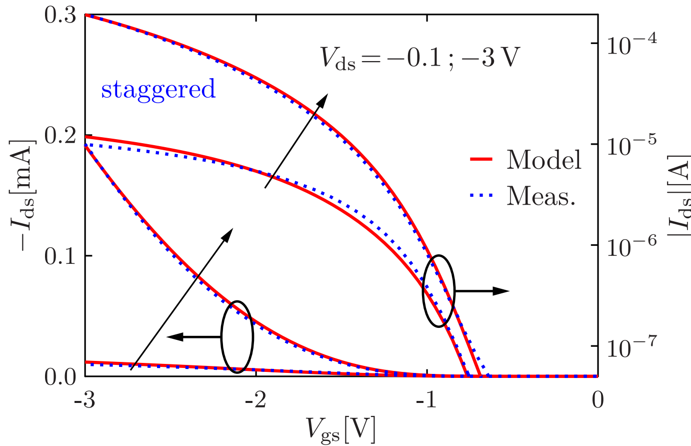


Figure 7.41.: Transfer characteristics of a staggered OTFT with $L_{ov,GS} = 5.4\,\mu m$, $L_{ov,GD} = 5.2\,\mu m$, and $L_{ch} = 0.67\,\mu m$. The measurements (dotted lines) are compared to the compact model (solid lines). This figure was published in ref. [55].

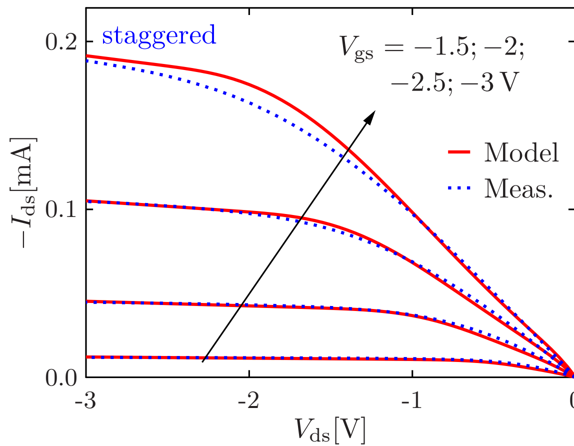


Figure 7.42.: Output characteristics of a staggered OTFT with $L_{ov,GS} = 5.4\,\mu m$, $L_{ov,GD} = 5.2\,\mu m$, and $L_{ch} = 0.67\,\mu m$. The measurements (dotted lines) are compared to the compact model (solid lines). This figure was published in ref. [55].

The compact model is fitted to each of the staggered and coplanar transistors in the population. First, a fitting of the charge-based DC model [36] and the non-linear injection model [47] to the measured transfer and output characteristics is performed. Later, the fitting parameters of the model for the total charges (such as K_r, K_{fit}) are used in order to have a good agreement

between the measured and modeled small-signal gain h_{21}. In Figs. 7.41 and 7.42, the DC model is compared to the measured transfer and output characteristics of one of the staggered transistors in the population. As can be seen, there is an overall good agreement. Small deviations in the transfer curves at $V_{ds} = -0.1\,V$ do not diminish the accuracy of the model since the fitting in the operation point $V_{gs} = V_{ds} = -3\,V$ is good.

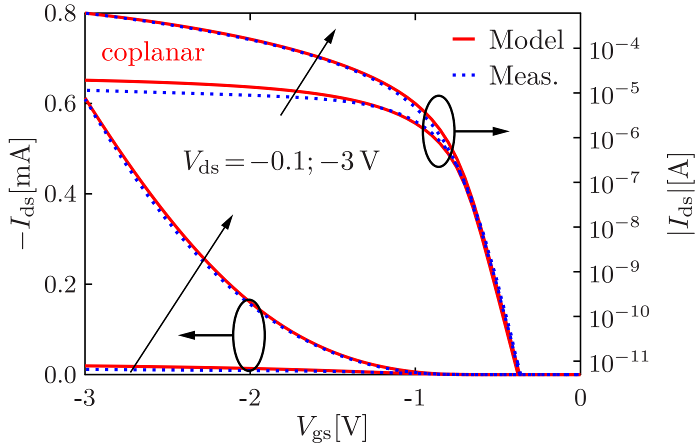


Figure 7.43.: Transfer characteristics of a coplanar OTFT with $L_{ov,GS} = 7.4\,\mu m$, $L_{ov,GD} = 3.0\,\mu m$, and $L_{ch} = 0.66\,\mu m$. The measurements (dotted lines) are compared to the compact model (solid lines). This figure was published in ref. [55].

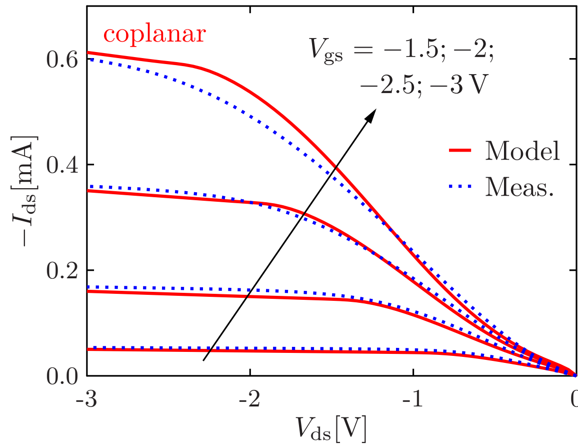


Figure 7.44.: Output characteristics of a coplanar OTFT with $L_{ov,GS} = 7.4\,\mu m$, $L_{ov,GD} = 3.0\,\mu m$, and $L_{ch} = 0.66\,\mu m$. The measurements (dotted lines) are compared to the compact model (solid lines). This figure was published in ref. [55].

Similarly, in Figs. 7.43 and 7.44, the static transfer and output characteristics of one of the coplanar transistors are shown. Despite some deviations at low absolute values of V_{ds} the agreement between the model and the measurements is good.

The S-parameters were measured at a DC operation point of $V_{\mathrm{gs}} = V_{\mathrm{ds}} = -3\,\mathrm{V}$ with superimposed small-signal voltages of $v_{\mathrm{gs}} = v_{\mathrm{ds}} = 0.2\,\mathrm{V}$. Thereby, the transistors are operated in the saturation regime of operation since their threshold voltages are about $V_{\mathrm{T0}} \approx -0.8\,\mathrm{V}$ and the condition $V_{\mathrm{ds}} < V_{\mathrm{gs}} - V_{\mathrm{T0}}$ is fulfilled. The small-signal gain h_{21} was calculated from the measured S-parameters according to the conversions presented in ref. [113]. Next, the small-signal gain is calculated based on the compact model. Before continuing with this, some points about Eq. (7.37) need to be discussed. As outlined before, the problem is that the intrinsic capacitances of a TFT are non-reciprocal, i.e. $C_{\mathrm{gs}} \neq C_{\mathrm{sg}}$ and $C_{\mathrm{gd}} \neq C_{\mathrm{dg}}$. By contrast, the gate-to-contact overlap capacitances are reciprocal. Figuratively speaking, it makes no difference for the parallel-plate capacitor, whether the voltage at one plate or at the other plate is changed. The capacitors consist of the gate and the source/drain electrodes separated from each other by the gate dielectric (in case of coplanar transistors) or by a stack of the gate dielectric and the organic semiconductor (in case of the staggered transistors). The influence on the charges stored in the capacitance is the same. This also holds true for the charges which are accumulated in the organic semiconductor layer in case of the gate-to-contact-overlap regions in staggered transistors. The position of the Fermi level in comparison to the valence band edge of the organic semiconductor is a consequence of the gate-to-contact voltage. Thus, it is not of importance, whether the potential at the gate electrode is changed or the potential at the source/drain electrode. From this, an interesting conclusion can be drawn: If a transistor comprises large gate-to-contact overlap regions in comparison to the channel length, the extrinsic gate-to-contact overlap capacitances will be dominant over the intrinsic channel capacitances. Thus, the capacitances of this transistor will show a nearly reciprocal behavior. The transistors under investigation in this work have a huge sum of the overlap lengths ($L_{\mathrm{ov,GS}} + L_{\mathrm{ov,GD}} \approx 10\,\mu\mathrm{m}$) in comparison to the channel length which is approximately $0.7\,\mu\mathrm{m}$. Consequently, a reciprocal behavior is assumed for the capacitances.

The capacitances of the compact model are calculated based on the new charge densities at the source/drain end of the channel where the contact voltage drops are included according to the principles described in Sec. 7.3.2.1. The compact model originally allows for a calculation of the total charges in the channel (Q_{c}) and associated with the source terminal (Q_{s}) and the drain terminal (Q_{d}). Based on these charges, the capacitances are calculated numerically according to the approach shown in Sec. 6.3.1. Furthermore, in order to solve Eq. (7.37), the transconductance g_{m} of the compact model is needed. The transconductance could be calculated by analytically deriving the drain-current equation (Eq. (2.21)) with respect to the voltage V_{gs}. However, this would result in a rather complicated term. Therefore, the transconductance is numerically calculated in the model in a similar manner as the capacitance: The current is calculated at two gate-source voltages around the operation point and the transconductance is defined as the change in the current divided by the change in V_{gs}. With these definitions, the complex small-signal gain h_{21} can be calculated according to Eq. (7.37). In order to compare it to the measurements, the absolute value of this complex value is taken.

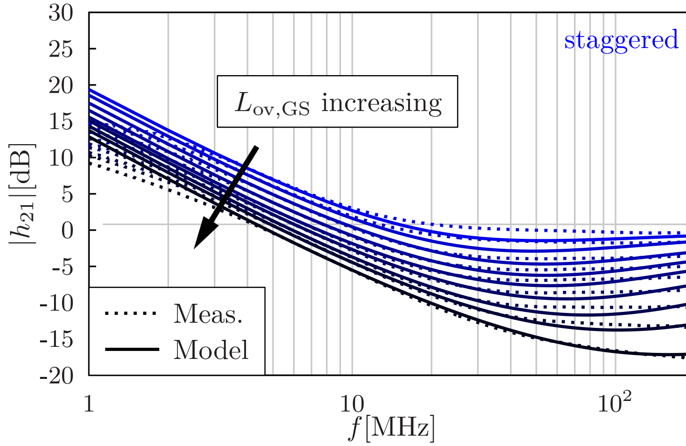


Figure 7.45.: Small-signal gain ($|h_{21}|$) of the staggered OTFTs. The measurements are depicted as dotted lines and the compact model results are shown as solid lines. For low frequencies, the measurement system is operated close to its resolution limit which is the reason for the slightly visible saturation of h_{21} for low frequencies. This figure was published in ref. [55].

Figure 7.45 depicts the measured absolute values of the small-signal gains h_{21} of the staggered transistors in comparison to the results of the compact model. The parameters chosen for the capacitance model such as the fitting parameters of the functions C_{scale} are depicted in Tab. B.2 and Tab. B.3 in Appendix B. It can be seen that there is an overall good agreement between model and measurements. The gate-to-contact overlap asymmetry has a notable influence on the curves. With $L_{\mathrm{ov,GS}}$ increasing (and $L_{\mathrm{ov,GD}}$ accordingly decreasing), the amplification of the transistor is becoming smaller. It can be seen that the measured curves show the formation of a plateau at low frequencies. This behavior can be attributed to the measurement system and not to a property of the transistors. In principle, gate-to-contact leakage currents can lead to a drop in the amplification behavior which becomes clear by observing the definition of h_{21} according to Eq. (7.36). If the gate dielectric conducts a leakage current, there will also be a small-signal gate leakage current which is added to the total small-signal current i_{g} at the gate, thus reducing the small-signal gain. However, the gate leakage currents are found to be so low in these transistors ($< 1\,\mathrm{pA}$) that they cannot justify such a degradation of the curves. The problem is rather that the admittance between the gate contacts and the other contacts becomes very low at the lowest measured frequencies ($\approx 30\,\mu\mathrm{S}$), which brings the vector network analyzer close to its resolution limit. Consequently, a meaningful evaluation of the measured h_{21} trends is only possible for higher frequency regions starting where ${}^{d|h_{21}|}/_{d\log(f)} \approx -20\,\mathrm{dB/dec}$.

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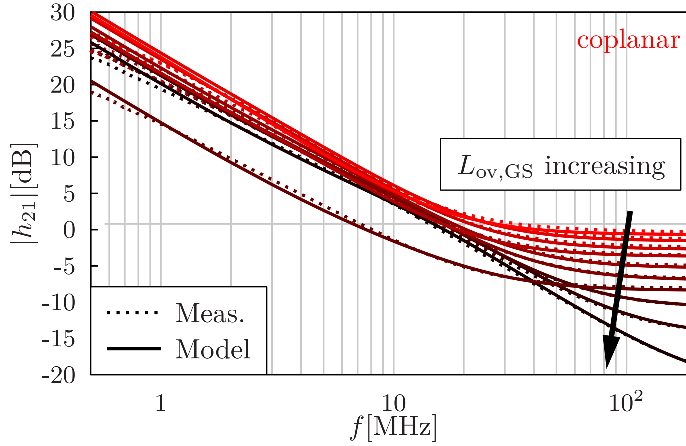

Figure 7.46.: Small-signal gain ($|h_{21}|$) of the coplanar OTFTs. The measurements are depicted as dotted lines and the compact model results are shown as solid lines. For low frequencies, the measurement system is operated close to its resolution limit which is the reason for the slightly visible saturation of h_{21} for low frequencies. This figure was published in ref. [55].

Figure 7.46 shows the measured absolute values of the small-signal gains h_{21} of the coplanar transistors in comparison to the results of the compact model. The model parameters are listed in Tab. B.2 and Tab. B.4 in Appendix B. It can be seen that the coplanar transistors show an overall higher small-signal gain owing to their higher transconductances. Furthermore, the dependence of the small-signal gain on the overlap asymmetry is much less pronounced than for the staggered transistors. Before the small-signal gains for both transistor architectures saturate at higher frequencies, they follow approximately trends of $-20\,\mathrm{dB/dec}$ [42, 107, 116]. This is because the gate electrode (as can be seen in Fig. 7.32) is coupled to the other terminals only through the capacitances C_{gs} and C_{gd}.

Comparing the trends of the small signal gain h_{21} of the staggered transistors and the coplanar transistors (Figs. 7.45 and 7.46), it can clearly be observed that the staggered transistors are much more sensitive to an asymmetry in the gate-to-contact overlap lengths. Except for the two staggered transistors with the shortest $L_{\mathrm{ov,GS}}$, they all exhibit a rather constant transconductance. Thus, when observing the analytical equation for h_{21} (Eq. (7.37)), the transconductance g_{m} cannot be the parameter that explains the differences in the curves with varying overlap asymmetry. Rather, the capacitances and especially their extrinsic parts vary between the two architectures (staggered and coplanar) and have a different dependence on the gate-to-contact overlap lengths. In the following, the contributions of the extrinsic capacitances to the observed results will be investigated in more detail.

Analysis of the source side

First, the focus will be put on the source side of the transistors. At the applied gate-source voltage of $V_{\mathrm{gs}} = -3\,\mathrm{V}$, the transistors are operated in the on-state. Consequently, at the source end of the channel, a high density Q'_{ms} of accumulated quasi-mobile holes is present. Independent of whether the coplanar or the staggered architecture is observed, the charge density Q'_{ms} is found everywhere in the fringe regions next to the electrodes. In Fig. 7.47, this

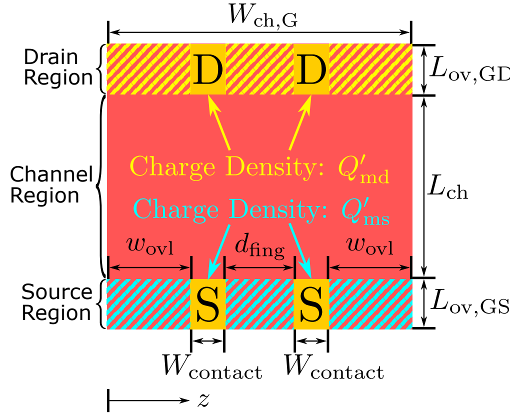

Figure 7.47.: Cutplane of a two-finger coplanar OTFT. This picture is the same as Fig. 4.7 and it is repeated here for better readability of the work. This picture was published in ref. [55].

is emphasized by the red/cyan-hashed region. Everywhere in this region, the charge density Q'_{ms} is present. According to the DC model [36], the density of quasi-mobile charges at the source end can be approximated in case of a strong accumulation by the following equation:

$$Q'_{\mathrm{ms}} = C'_{\mathrm{diel}} \left(V_{\mathrm{gs}} - V_{\mathrm{T0}}\right). \tag{7.46}$$

The consequence from this simple equation is that the charge density is proportional to the dielectric capacitance C'_{diel}. In dependence on the transistor architecture, there are differences in the gate-to-contact overlap regions, as already explained in Chap. 4:

- In coplanar (BC) transistors, the gate-to-contact overlap regions behave like simple parallel-plate capacitors with a capacitance of $N_{\mathrm{fing}} \cdot W_{\mathrm{contact}} \cdot L_{\mathrm{ov,GS}} \cdot C'_{\mathrm{diel}}$ at the source side. Thus, the extrinsic charges at the source side are a composition of the fringe charges in the cyan/red-hashed area in Fig. 7.47 and these charges in the overlap capacitor. According to Eq. (7.46), the charge density Q'_{ms} is proportional to C'_{diel}, just as the gate-to-source overlap capacitance. As a consequence, the extrinsic charges in coplanar transistors are entirely proportional to C'_{diel}.

- In staggered (TC) transistors, the gate-to-contact-overlap regions consist of a stack of the organic semiconductor and the gate dielectric. If the organic semiconductor is operated in depletion, the overlap regions can be regarded as a series connection of capacitors. If, by

contrast, the organic semiconductor is operated in accumulation (such as it is in this case), the voltage drop across the series connection is limited (see Fig. 4.9) and the accumulation of charge carriers sets on. Under strong accumulation, again Eq. (7.46) is valid. As a consequence, the gate-to-source overlap capacitance is proportional to C'_{diel}, as well. Equally as for the coplanar transistors, the fringe charges in the cyan/red-hashed area in Fig. 7.47 have to be added to the overlap charges. Since these charges are proportional to Q'_{ms} and therefore also proportional to C'_{diel}, the same conclusion as for the coplanar transistors can be drawn: The extrinsic charges in staggered transistors are entirely proportional to C'_{diel}.

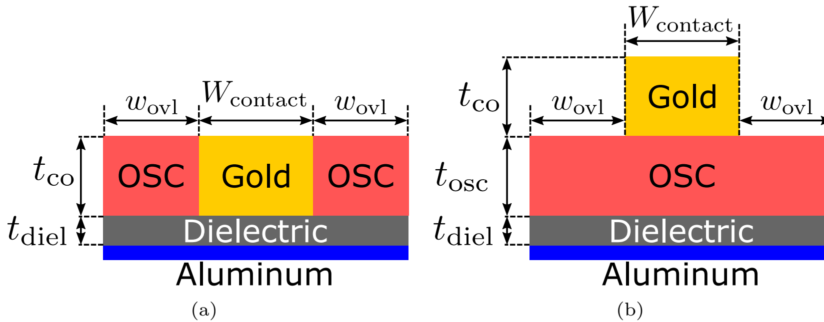

Figure 7.48.: (a) Sketch of a metal-insulator-metal (MIM) structure including fringe regions. An equivalent structure is found in coplanar transistors in a cutplane in the source/drain regions. (b) Sketch of a metal-insulator-semiconductor-metal (MISM) structure including fringing regions. An equivalent structure is found in staggered transistors in a cutplane in the source/drain regions. These pictures were published in ref. [55].

This leads to the interesting conclusion that the gate-to-source overlap capacitances of the two architectures will have the same values if the organic semiconductor is operated in strong accumulation. This assumption can be verified by a TCAD simulation of the gate-to-contact-overlap region. For a coplanar transistor, this can be modeled as a metal-insulator-metal (MIM) region including fringe regions, see Fig. 7.48(a). For a staggered transistor, the gate-to-source overlap region is modeled as a metal-insulator-semiconductor-metal (MISM) region, also including fringe regions, see Fig. 7.48(b). In Fig. 7.49, the results of a quasistatic capacitance simulation of the MIM and the MISM structures in TCAD are shown. Since the work function of the gold electrode interfacing the organic semiconductor is aligned with the HOMO of the organic semiconductor, negative voltages have to be applied in order to enter the accumulation regime. It can be seen that at small absolute values of the voltage, the capacitances of the two structures are quite different. This will be important for the analysis of the drain side of the transistors in the next section. At a high absolute voltage, the capacitances of the two structures converge to the same value. This is in agreement with the theoretical analysis of the gate-to-contact overlap region of the source side.

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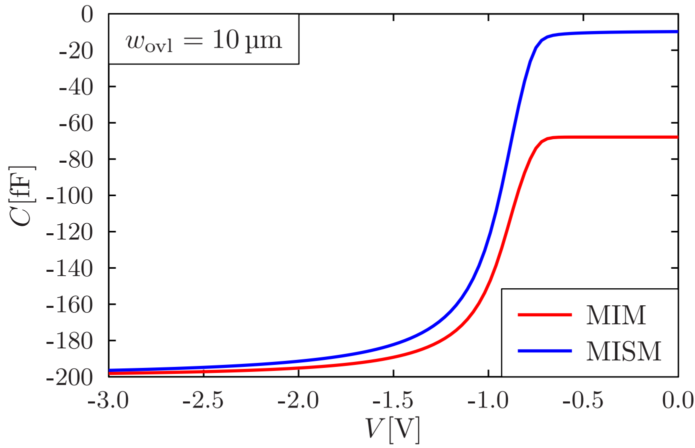

Figure 7.49.: Quasistatic capacitance-voltage characteristics of the MIM and MISM structures as a result of a TCAD Sentaurus simulation. The dimensions are: $L_{\mathrm{co}} = 10\,\mu\mathrm{m}$, $w_{\mathrm{ovl}} = 10\,\mu\mathrm{m}$, $t_{\mathrm{co}} = 40\,\mathrm{nm}$, $t_{\mathrm{diel}} = 5.3\,\mathrm{nm}$, $t_{\mathrm{osc}} = 25\,\mathrm{nm}$. In depletion, both structures show different capacitances but in accumulation, both converge to the same value, as predicted. This figure was published in ref. [55].

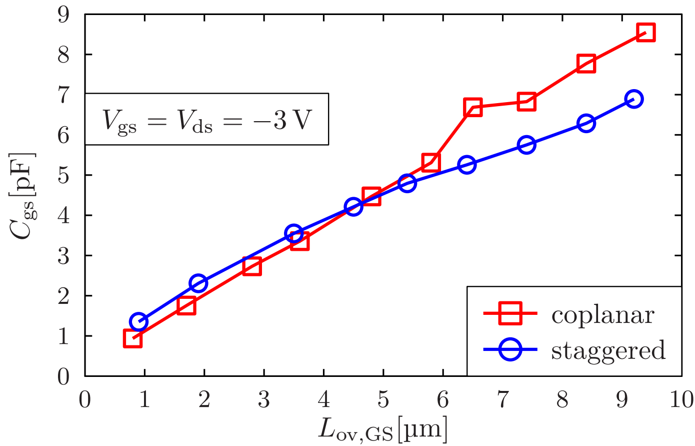

Figure 7.50.: Quasistatic gate-source capacitance (C_{gs}) in staggered and coplanar OTFTs calculated using the compact model and plotted against the measured gate-to-source overlap length ($L_{\mathrm{ov,GS}}$). For each $L_{\mathrm{ov,GS}}$, the quasistatic gate-source capacitance (C_{gs}) of the staggered TFTs is nearly identical to that of the coplanar TFTs despite the differences in the device architecture. This figure was published in ref. [55].

These thoughts can be further proven by observing the quasistatic capacitances of the transistors. Since no quasistatic capacitance measurements are available, only the results of the compact model can be shown. In the quasistatic case, the entire fringe and channel regions are taken into account for the capacitance calculation. Figure 7.50 depicts the quasistatic capacitance C_{gs} as calculated by the compact model versus the measured gate-to-source overlap length $L_{\mathrm{ov,GS}}$. It

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can be seen that despite the differences in the device architecture, the capacitance is nearly the same for both structures. As explained before, the extrinsic capacitances are dominant in these transistors due to their much larger gate-to-contact overlap lengths in comparison to the intrinsic channel length. Consequently, a comparison of the overlap capacitances is sufficient for a proper evaluation of the capacitances of both architectures. If the capacitance C_{gs} is the same for both transistor architectures, the capacitance C_{gd} at the drain needs to be investigated in more detail.

Analysis of the drain side

Having discussed the capacitance C_{gs} for both transistor architectures, now the capacitance C_{gd} at the drain side needs to be investigated. In the chosen operation point ($V_{\mathrm{gs}} = V_{\mathrm{ds}} = -3\,\mathrm{V}$), the gate-drain voltage V_{gd} is zero and the organic semiconductor is operated in depletion. As a consequence, no accumulation charges are present (Q'_{md} converges to zero) at the drain end of the channel and in the fringe regions next to the drain electrodes. Thus, in the yellow/red-hashed region in Fig. 7.47, no notable amount of charges is present. Furthermore, since in the chosen operation point the transistor is operated in the saturation regime of operation, the intrinsic channel charges are not under control of the drain terminal. Therefore, only extrinsic capacitances are measurable at the drain terminal at this operation point. Again, the two structures (coplanar and staggered) are regarded separately:

- In a coplanar transistor, only the gate-to-drain overlap capacitance is of importance. The gate dielectric capacitance is the only capacitance measurable in this operation point. The capacitance C_{gd} is thus defined by $C_{\mathrm{gd}} = N_{\mathrm{fing}} \cdot W_{\mathrm{contact}} \cdot L_{\mathrm{ov,GD}} \cdot C'_{\mathrm{diel}}$.

- In a staggered transistor, the gate-to-drain overlap capacitance is the only important contributor to the gate-drain capacitance, too. Since the organic semiconductor is depleted, it behaves as an insulator with a dielectric constant $\varepsilon_{\mathrm{r,osc}}$. The gate-to-drain-overlap capacitance is then in principle a series connection of the gate dielectric and the depleted organic semiconductor. Connecting two capacitances in a series, the overall capacitance of that series connection is smaller than any of the single capacitances. Consequently, C_{gd} is smaller in staggered transistors than in coplanar transistors in that operation point.

These claims can be verified by observing Fig. 7.49. It can be seen that for voltages close to zero, the MIM structure indeed shows a notably higher absolute value of the capacitance than the MISM structure. Please recall that the MIM structure is equivalent to the gate-to-contact-overlap region of a coplanar transistor whereas the MISM structure represents that of a staggered transistor. Furthermore, in Fig. 7.51, the quasistatic gate-drain capacitance C_{gd} is plotted for all of the coplanar and staggered transistors under investigation. It can be seen that the staggered transistors show an overall smaller and less $L_{\mathrm{ov,GD}}$-dependent C_{gd}. This proves the assumptions.

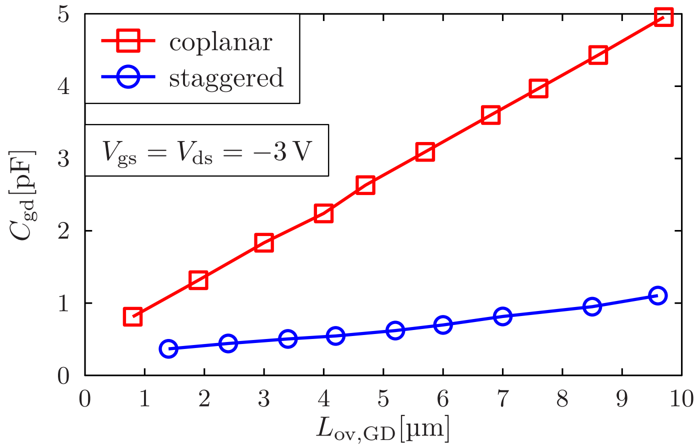

Figure 7.51.: Quasistatic gate-drain capacitance (C_{gd}) in staggered and coplanar TFTs calculated using the compact model and plotted against the measured gate-to-drain overlap length ($L_{ov,GD}$). It can be seen that C_{gd} is quite different in both architectures. This figure was published in ref. [55].

Further discussion

The analysis of the capacitances at the source and at the drain side of the transistors has revealed that the capacitance at the drain side is the reason for the different behavior of the measured small-signal gain h_{21} of the two different transistor architectures. In Fig. 7.52, the measured small-signal parameter Y_{11} of the OTFT with the smallest $L_{ov,GS}$ for each transistor architecture is depicted. Y_{11} is defined as the quotient of the small-signal gate current divided

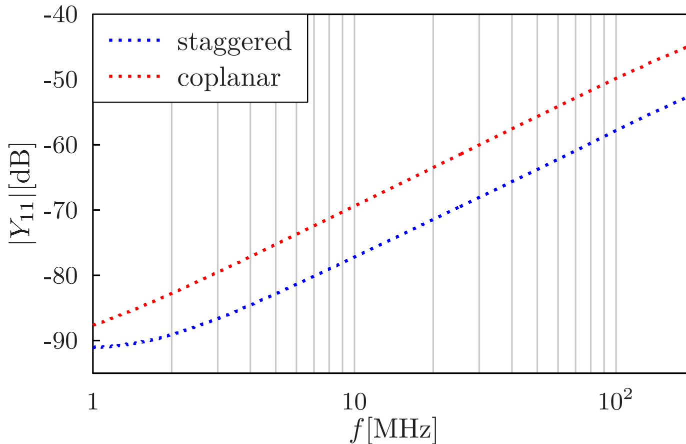

Figure 7.52.: Measured small-signal admittance Y_{11} of the TFT with the smallest $L_{ov,GS}$ of each architecture showing the difference in the overall capacitance. This figure was published in ref. [55].

by the small-signal gate-source voltage. From the circuit analysis of the circuit depicted in Fig. 7.32, it can be shown that Y_{11} depends only on the capacitances:

$$Y_{11} = \left.\frac{i_{\mathrm{g}}}{v_{\mathrm{gs}}}\right|_{v_{\mathrm{ds}}=0} = j2\pi f\left(C_{\mathrm{gs}} + C_{\mathrm{gd}}\right). \tag{7.47}$$

Thus, an overall larger absolute value of Y_{11} can be interpreted as a higher sum of the capacitances C_{gs} and C_{gd}. The discussion so far has shown that while the gate-source capacitances C_{gs} are equal for the staggered and coplanar transistors, the gate-drain capacitances C_{gd} are overall larger in the coplanar transistors. This is in agreement with the observation of Y_{11} in Fig. 7.52 where it becomes visible that the sum of C_{gs} and C_{gd} is higher for a coplanar transistor than for a staggered transistor with same geometrical dimensions.

Based on the evaluation that coplanar transistors show an overall larger sum of the capacitances C_{gs} and C_{gd}, there might be drawn the conclusion that they will show an overall worse small-signal amplification behavior than otherwise equivalent staggered transistors. However, the measured small-signal gains h_{21} of the coplanar transistors are better than those of the staggered transistors, as depicted in Figs. 7.45 and 7.46. The reason for this is that the transconductance of the coplanar transistors is much higher than that of their staggered counterparts. Furthermore, one might come to the conclusion that by decreasing the gate-to-source overlap length $L_{\mathrm{ov,GS}}$, the small-signal amplification capabilities can be increased a lot, especially with regard to the staggered transistors. However, the staggered transistors have a strong dependence of the charge injection on the transfer length and thus also on $L_{\mathrm{ov,GS}}$ [59]. Consequently, a brutal down-scaling of $L_{\mathrm{ov,GS}}$ in staggered transistors will lead to a worse transconductance, thus negating any benefits from the reduction of the capacitance C_{gs}. As can be seen in Fig. 7.46, the coplanar transistors show a much weaker dependence of h_{21} on the asymmetry of the gate-to-contact overlaps. The benefit of this transistor architecture is that the injection occurs only at the corner where the source electrode and the organic semiconductor are interfacing and hence, a shortening of $L_{\mathrm{ov,GS}}$ does not lead to a worse transconductance. Thus, it can be concluded that despite their larger gate-to-contact overlap capacitances the coplanar transistors have a better overall small-signal amplification behavior.

7.4.4 Parameter Extraction

In this section, the extraction procedure for the fitting parameters will be explained based on the measurements presented above. The model for the current gain h_{21} employs several fitting parameters. The difficulty of determining meaningful values for these parameters is that they are interdependent, i.e. the parameters do not have influence only on an isolated region of the curve but they all change the entire curve. However, there is a useful procedure of determining a set of parameters that leads to a good agreement. The basic requirement is that before the AC fitting a proper DC fitting has been determined.

7.4.4.1 Staggered Transistors

1. Determining First Guesses for K_{fit} and K_{r}

Here, the extraction of the fitting parameters will be described at the example of the staggered transistor with $L_{\mathrm{ov,GS}} = 5.4\,\mu\mathrm{m}$ and $L_{\mathrm{ov,GD}} = 5.2\,\mu\mathrm{m}$. The starting point is to turn off the models for the frequency-dependent change in the channel widths for the fringe regions and the channel regions (and overlap regions in staggered transistors). This can be achieved by setting $C_{\mathrm{scale,low}}$, $C_{\mathrm{scale,high}}$, $C_{\mathrm{scale2,low}}$, and $C_{\mathrm{scale2,high}}$ all to a value of 1. As a consequence, C_{scale} and C_{scale2} are always 1 for the entire range of frequencies. Furthermore, the short-channel AC model is set to an initial state by setting $K_{\mathrm{fit}} = 1$ and $K_{\mathrm{r}} = 1$. Based on this, the trend of the

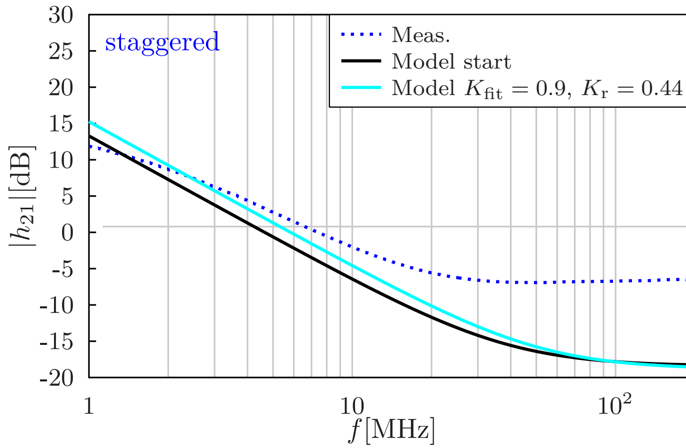

Figure 7.53.: First step of the fitting procedure for the small-signal current gain h_{21}. The measurements of the staggered OTFT with $L_{\mathrm{ov,GS}} = 5.4\,\mu\mathrm{m}$ and $L_{\mathrm{ov,GD}} = 5.2\,\mu\mathrm{m}$ (dotted blue line) are shown in comparison to the initial model state where $K_{\mathrm{fit}} = 1$ and $K_{\mathrm{r}} = 1$ (solid black line) and the model where $K_{\mathrm{fit}} = 0.9$ and $K_{\mathrm{r}} = 0.44$ (solid cyan-colored line).

modeled h_{21} is compared to the measurements which is depicted in Fig. 7.53. The next step is to set the two model parameters K_{fit} and K_{r} to values smaller than 1. In principle, the values for these fitting parameters could be determined from quasistatic capacitance measurements but these are not available. Here, the parameter K_{r} has a much greater influence on the resulting curves than the parameter K_{fit}. It is recommended to set the parameters to such values that the modeled h_{21} nearly agrees with the measurements at the beginning of the "linear" piece of the curve. In principle, K_{fit} and K_{r} could be chosen so that the modeled curve has larger values but as it will become clear in the further fitting progress, it is reasonable to tune the model curve in such a way that it underestimates the measured values since in the other fitting steps the curve will be shifted up again.

2. Determining the Parameters of C_{scale}

The next step is to activate the function C_{scale} by setting $C_{\text{scale,high}} = 0$. Effectively, C_{scale} changes the fringe width that is taken into account for the capacitance calculation. The function C_{scale} has the two fitting parameters τ_{scale} and p_{scale}. The parameter τ_{scale} mainly influences

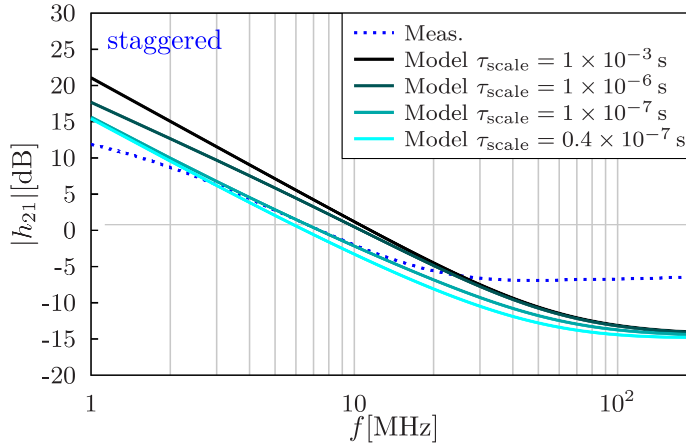

Figure 7.54.: Second step of the fitting procedure for the small-signal current gain h_{21}. The measurements of the staggered OTFT with $L_{\text{ov,GS}} = 5.4\,\mu\text{m}$ and $L_{\text{ov,GD}} = 5.2\,\mu\text{m}$ (dotted blue line) are shown in comparison to the compact model where $K_{\text{fit}} = 0.9$ and $K_{\text{r}} = 0.44$ for different values of the fitting parameter τ_{scale} (solid lines). The parameter p_{scale} is set to 1.

the magnitude of the curve for the lower frequencies and the parameter p_{scale} can change the curvature. Thus, it is recommended to first set $p_{\text{scale}} = 1$ and manually tune the parameter τ_{scale}. In Fig. 7.54, the compact model is shown in comparison to the measured h_{21} for different values of τ_{scale} with a constant p_{scale} of 1. It can be seen that setting $\tau_{\text{scale}} = 1 \times 10^{-7}$ s leads to a good agreement in the linear region of the measurement data. However, similarly as in step 1, it is recommended to fit the model in such a way that the compact model slightly underestimates the measurements since the next modeling steps will shift the curve up again. Since the curvature is sufficiently well captured p_{scale} can keep the value of 1. As can be seen in Fig. 7.54, the model incorporating the function C_{scale} is only able to tune the curves in the medium-frequency range. However, for high frequencies, the model curves all converge to the same value. This is the observation leading to the claim that in the high-frequency regime additional effects have to be taken into account which is accomplished by the function C_{scale2}.

3. Determining the Parameters of C_{scale2}

In this step, the function C_{scale2} is activated, as well. Similarly as the other function (C_{scale}), C_{scale2} also has a time constant (τ_{scale2}) and an exponent (p_{scale2}). The difficulty in determining parameter sets for C_{scale} and C_{scale2} is that also C_{scale2} has a small influence on the medium-frequency regime, although its main purpose is to find a proper description of the high-frequency regime. The parameter τ_{scale2} is set to an arbitrary value smaller than τ_{scale}

since it is assumed that the decay of the intrinsic channel width and the width in which charges in the overlap regions start to behave slowly is a little smaller and later than the decay of the fringe width. As a first experiment, the parameter p_{scale2} can be set to 1. In Fig. 7.55, the compact model is compared to the measurements where different values for the exponent p_{scale2} are assumed. It can be seen that a value of $p_{\mathrm{scale2}} = 1$ does not perfectly represent the curvature of the measurements in the high-frequency regime. Setting a value of $p_{\mathrm{scale2}} = 2.5$ leads to a better agreement. However, it can be seen that now, the compact model generally overestimates the measurements a little bit. Thus, a last refinement of the model has to be performed.

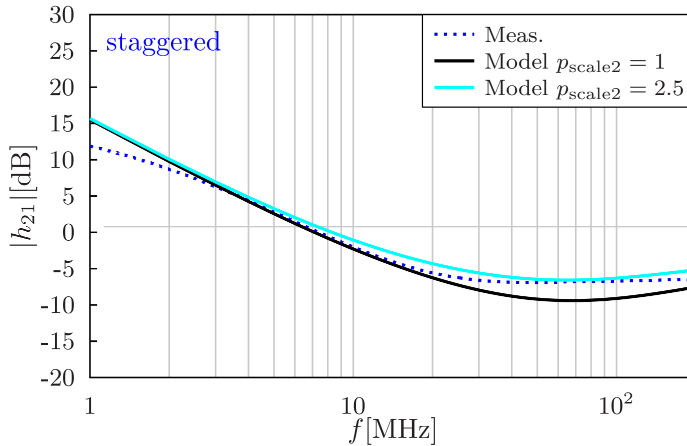

Figure 7.55.: Third step of the fitting procedure for the small-signal current gain h_{21}. The measurements of the staggered OTFT with $L_{\mathrm{ov,GS}} = 5.4\,\mu\mathrm{m}$ and $L_{\mathrm{ov,GD}} = 5.2\,\mu\mathrm{m}$ (dotted blue line) are shown in comparison to the compact model where $K_{\mathrm{fit}} = 0.9$ and $K_{\mathrm{r}} = 0.44$ for different values of the fitting parameter p_{scale2} (solid lines). The parameters of the other models are: $\tau_{\mathrm{scale}} = 0.4 \times 10^{-7}\,\mathrm{s}$, $p_{\mathrm{scale}} = 1$, $\tau_{\mathrm{scale2}} = 0.3 \times 10^{-7}\,\mathrm{s}$.

4. Refinements

In order to shift the model curve depicted in Fig. 7.55 down, there are several options such as tuning K_{r}, τ_{scale} or τ_{scale2}. Here, it is decided to use the parameter τ_{scale2}. Setting this parameter to a smaller value shifts the curve down. The final result is shown in Fig. 7.56. There is a good agreement between the measured and the modeled curve. However, the agreement is not perfect for very high frequencies. In order to properly model this regime of operation, further model extensions would be required. However, it has to be highlighted that the model has a good agreement in the region where $|h_{21}|$ is greater than zero. This is actually the frequency range in which a transistor will be operated in an electric circuit. Operating the transistor at frequencies well above the transit frequency (i.e. the frequency, where $|h_{21}|$ becomes one) means using it in a regime where the drain current response is smaller than the capacitive gate charging current. It can be doubted whether such an operation point is useful from a practical point of view.

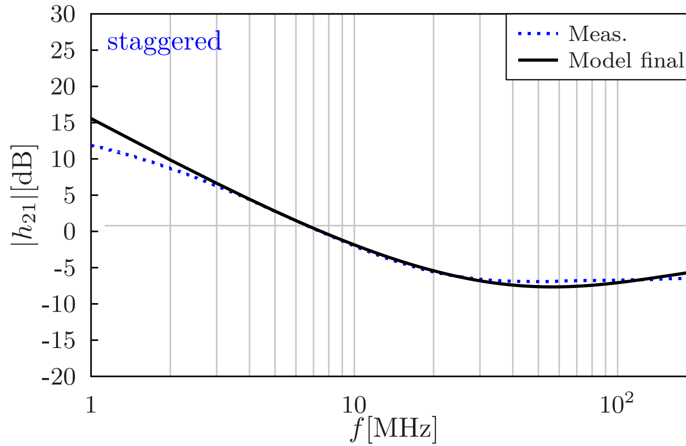

Figure 7.56.: Fourth and final step of the fitting procedure for the small-signal current gain h_{21}. The measurements of the staggered OTFT with $L_{\mathrm{ov,GS}} = 5.4\,\mu\mathrm{m}$ and $L_{\mathrm{ov,GD}} = 5.2\,\mu\mathrm{m}$ (dotted blue line) are shown in comparison to the final fitting of the compact model where $K_{\mathrm{fit}} = 0.9$, $K_{\mathrm{r}} = 0.44$, $\tau_{\mathrm{scale}} = 0.4 \times 10^{-7}\,\mathrm{s}$, $p_{\mathrm{scale}} = 1$, $\tau_{\mathrm{scale2}} = 0.17 \times 10^{-7}\,\mathrm{s}$, and $p_{\mathrm{scale2}} = 2.5$ (solid black line).

7.4.4.2 Coplanar Transistors

The parameter extraction is in principle independent of the transistor architecture. However, staggered and coplanar transistors behave differently under high-frequency conditions. In ref. [55], it has been shown that coplanar transistors show a more textbook-like behavior owing to their overlap-independent transconductance and the higher simplicity of the gate-to-contact overlap regions. Nevertheless, in this section, the parameter extraction process for the h_{21} model is presented in brief.

1. Determining First Guesses for K_{fit} and K_{r}

Exactly as for the staggered transistors, the first step is to determine meaningful values for the parameters K_{fit} and K_{r}. This is accomplished by setting K_{fit} and K_{r} to such values that the modeled h_{21} curve agrees with the measurements at a low frequency where the measured curves start to behave somehow linearly. This first fitting step is shown in Fig. 7.57.

2. Determining the Parameters of C_{scale}

The determination of the parameters of the scaling function C_{scale} starts by setting the exponent p_{scale} to 1 and then trying different time constants τ_{scale}. As can be seen in Fig. 7.58, setting the time constant alone does not lead to a good reproduction of the curvature of the measured h_{21} curve in the linear regime. Therefore, in contrast to the staggered transistors, the parameter p_{scale} needs to be tuned. In Fig. 7.59, the compact model is shown in comparison to the measurements again but here, an exponent of $p_{\mathrm{scale}} = 50$ is chosen. It can be seen that there

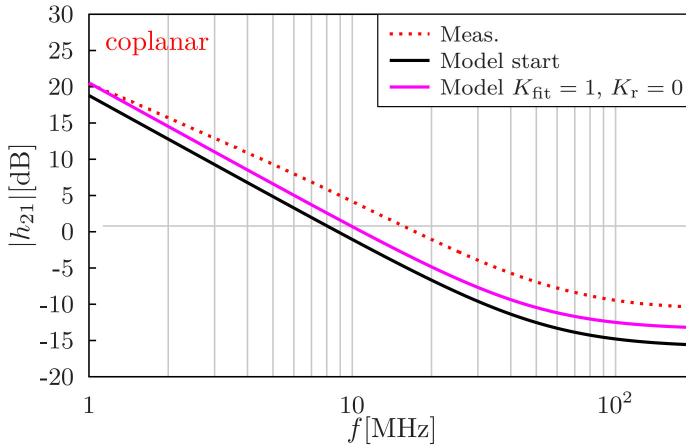

Figure 7.57.: First step of the fitting procedure for the small-signal current gain h_{21}. The measurements of the coplanar OTFT with $L_{\text{ov,GS}} = 7.4\,\mu\text{m}$ and $L_{\text{ov,GD}} = 3\,\mu\text{m}$ (dotted red line) are shown in comparison to the initial model state where $K_{\text{fit}} = 1$ and $K_{\text{r}} = 1$ (solid black line) and the model, where $K_{\text{fit}} = 1$ and $K_{\text{r}} = 0$ (solid magenta-colored line).

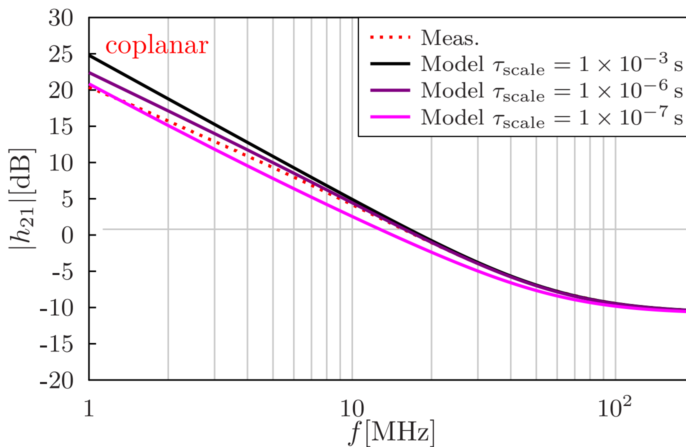

Figure 7.58.: Second step of the fitting procedure for the small-signal current gain h_{21}. The measurements of the coplanar OTFT with $L_{\text{ov,GS}} = 7.4\,\mu\text{m}$ and $L_{\text{ov,GD}} = 3\,\mu\text{m}$ (dotted red line) are shown in comparison to the compact model where $K_{\text{fit}} = 1$ and $K_{\text{r}} = 0$ for different values of the fitting parameter τ_{scale} (solid lines). The parameter p_{scale} is set to 1.

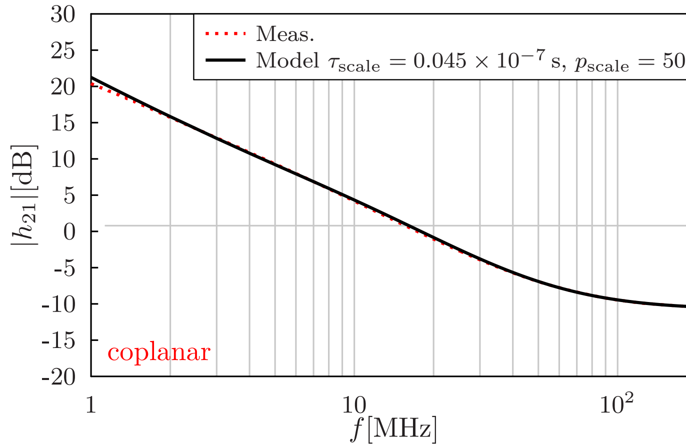

Figure 7.59.: Second step of the fitting procedure for the small-signal current gain h_{21}. The measurements of the coplanar OTFT with $L_{\text{ov,GS}} = 7.4\,\mu\text{m}$ and $L_{\text{ov,GD}} = 3\,\mu\text{m}$ (dotted red line) are shown in comparison to the compact model where $K_{\text{fit}} = 1$ and $K_{\text{r}} = 0$, $\tau_{\text{scale}} = 0.045 \times 10^{-7}$ s, and $p_{\text{scale}} = 50$ (solid black line). Even without the usage of the function C_{scale2}, the agreement is already very good.

is already a very good agreement between the model and the measurement. The model now accurately represents the slightly non-linear behavior of the h_{21} curve at low and medium frequencies. At this stage, the fitting of the model could already stop due to the good agreement. It has to be mentioned that activating the function C_{scale2} only has a very small influence on the final curves. The reason is that the gate-to-contact overlap capacitances in coplanar transistors are simpler than in staggered transistors and just consist of parasitic parallel-plate capacitors which are not subject to a frequency dependence in the frequency regime observed here. Therefore, in coplanar transistors, the function C_{scale2} only has an influence on the intrinsic channel charges which are minor in comparison to the overlap charges.

3. and 4. Determining the Parameters of $C_{\text{scale}}2$ and Fine Tuning

Although the fitting of the coplanar transistors can already be regarded as sufficient, the function C_{scale2} can be activated. Due to the small influence, however, it is not worth investigation the differences for various parameters of this function. For the staggered transistors, special emphasis has been put on the fact that the time constant of the function C_{scale2} should be greater than that of C_{scale}. However, due to the minor influence of the function C_{scale2} in the context of coplanar transistors, this condition is not regarded as necessary. In Fig. 7.60, the final fitting of the BC transistor is shown. A further fine tuning is not necessary in this case. The exponent p_{scale2} is chosen to match that of the TC transistors and the time constant τ_{scale2} is arbitrarily chosen. It can be seen that there is hardly any difference between the fittings shown in Figs. 7.59 and 7.60. This emphasizes the small influence of C_{scale2} on the results.

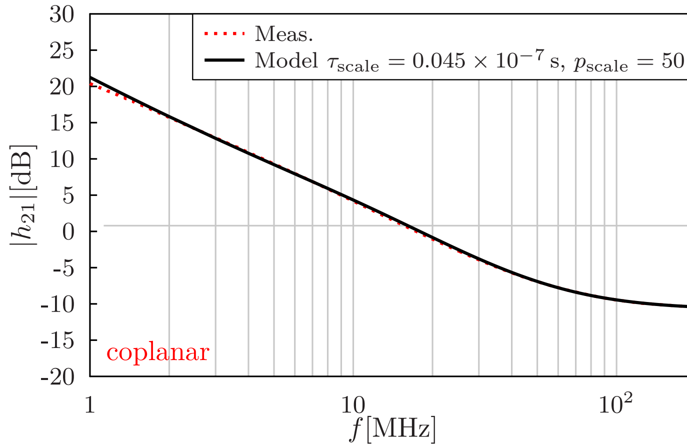

Figure 7.60.: Final steps of the fitting procedure for the small-signal current gain h_{21}. The measurements of the coplanar OTFT with $L_{ov,GS} = 7.4\,\mu m$ and $L_{ov,GD} = 3\,\mu m$ (dotted red line) are shown in comparison to the compact model where $K_{fit} = 1$ and $K_r = 0$, $\tau_{scale} = 0.045 \times 10^{-7}$ s, $p_{scale} = 50$, $\tau_{scale2} = 0.5 \times 10^{-7}$ s, and $p_{scale2} = 2.5$ (solid black line).

7.5 Temperature Effects

7.5.1 General Information

This section contains an investigation of temperature effects. Staggered OTFTs were fabricated according to the same process as described in Sec. 7.4. The source/drain electrodes consist of 22 nm thick gold located on top of a 20 nm thick layer of 2,9-diphenyl-dinaphtho[2,3-b:2',3'-f]thieno[3,2-b]thiophene (DPh-DNTT). The gate electrode consists of a 25 nm thick layer of aluminum and the hybrid gate dielectric consists of aluminum oxide and a self-assembled monolayer of n-tetradecylphosphonic acid with a total thickness of approx. 7 nm. Transistors in the single-finger layout with different channel lengths were fabricated.

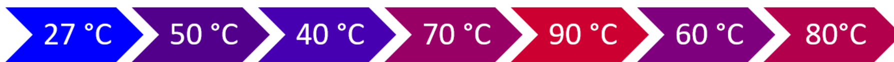

Figure 7.61.: Temperature profile of the measurement setup. The temperatures are set in the order as depicted here.

For the electrical measurements, the fully fabricated substrate was placed on a close-loop controlled Peltier element which allowed for the setting of temperatures. Different temperatures as depicted in Fig. 7.61 were used. As can be seen, the temperatures were not swept linearly but according to a temperature profile with several temperature jumps in different directions. The reason for choosing such a temperature profile is that there has to be a distinction between temperature-dependent effects and degradation effects. If in the observed results any trends with the temperature are visible, there is a higher probability that these trends are really due

to temperature effects. After setting a new temperature, several transistors were measured meaning that every transistor was exposed to the set temperature for a time of approx. one hour. DC transfer and output characteristics were measured using an Agilent B1500A device parameter analyzer. During the transfer curves, the gate-source voltage was swept in both directions, i.e. from $V_{gs} = 0\,V$ to $-3\,V$ and back to $0\,V$. The probing station was covered by a black cloth in order to prevent light influences. Due to charge trapping effects, the transfer curves exhibit a small hysteresis between the forward and the backward sweep and the transfer curves are not perfectly consistent with the output curves. In order to reduce these effects, the transfer curves were recorded three times and only the results of the backward sweep of the last sweep were evaluated. The output curves were also swept three times but for the analysis of the temperature effects, only the transfer curves are taken into account.

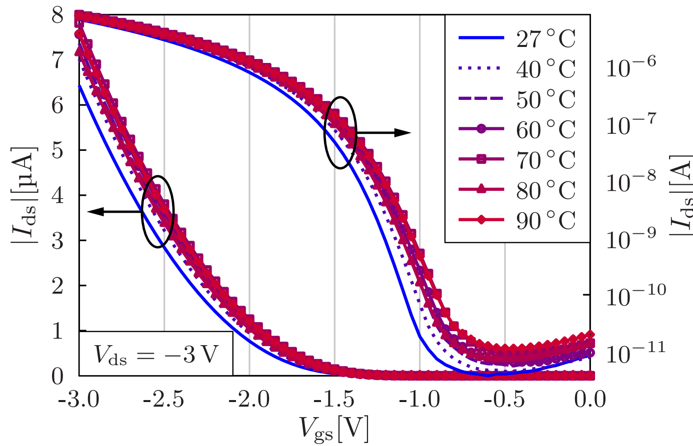

Figure 7.62.: Measured transfer characteristics of a staggered OTFT at different temperatures as indicated by the legend. The drain-source voltage is $V_{ds} = -3\,V$. The transistor has a channel length of $L_{ch} = 100\,\mu m$ and a symmetric gate-to-contact overlap length of $L_{ov,GS} = L_{ov,GD} = L_{ov} = 50\,\mu m$.

Figure 7.62 shows the measured transfer characteristics of one transistor of the population at different temperatures. The backward sweeps of the curves at a large absolute value of V_{ds} are shown. It can be seen that the temperature has a notable influence on the curves. In general, at higher temperatures, the sub-threshold swing becomes less steep. Furthermore, a shift in the threshold voltage becomes visible. The behavior of the transistor at the two temperature points 80 °C and 90 °C, however, does not agree with the the observed trends. While the threshold voltage monotonically shifts towards zero for temperatures increasing in the range $27\,°C \leq T \leq 70\,°C$ it jumps forward and backward at the two highest temperatures. This behavior was observed in the whole population of the transistors. However, in the range of $27\,°C \leq T \leq 70\,°C$, the transistors show a quite predictable behavior. Possible problems at the higher temperatures might be due to the convection of the air at the surface of the substrate or due to reversible short-term or mid-term degradation effects which might be more pronounced

at higher temperatures. These degradation effects can be assumed to be reversible because the curves show a predictable behavior at a temperature of 60 °C which was set after one hour of temperature stress at 90 °C. Possible changes during the 90 °C phase must have been reversed. The measurement setup and possible physical explanations for this behavior have to be part of future work. In order to come to plausible closed-form solutions for the temperature dependence of the model parameters, only the temperature range of $27\,^\circ\mathrm{C} \leq T \leq 70\,^\circ\mathrm{C}$ is evaluated in the following.

The influence of the temperature on the parameters of the compact DC model is investigated. For each temperature, the compact model is fitted to the backward sweep of the last transfer curve. The compact model is fitted to simultaneously agree with the transfer curves in the linear regime ($V_{\mathrm{ds}} = -0.1\,\mathrm{V}$) and in the saturation regime ($V_{\mathrm{ds}} = -3\,\mathrm{V}$). It turned out that the threshold voltage (V_{T0}), the low-field mobility (κ), and the sub-threshold swing (S_{obs}) are the model parameters which can capture the temperature effects. For each temperature, these three parameters are adapted in order to agree with the measured transfer curves using the following procedure:

1. The sub-threshold swing is calculated by probing the current I_1 and I_2 at two gate-source voltages V_{gs1} and V_{gs2} in the sub-threshold regime of operation. The swing is then calculated as $S_{\mathrm{meas}} = |V_{\mathrm{gs2}} - V_{\mathrm{gs1}}|/(\lg(I_2) - \lg(I_1))$, where lg is the logarithm to base 10. The extracted swing is set as the model parameter S_{obs}.

2. The threshold voltage is tuned so that the compact model and the measured curves agree in the sub-threshold regime of operation.

3. The low-field mobility κ is tuned so that the curves agree at high absolute values of V_{gs}.

The power-law-mobility exponent β is set to a constant value. Since the transfer curves all exhibit a similar curvature at the different temperatures, it is not necessary to model β temperature dependent.

In principle, it is imaginable that also other parameters of the transistors exhibit changes. The contact resistances, for example, may also change in dependence on the temperature. However, it is difficult to distinguish between the different parameters that may vary. For example, the change in the magnitude of the on-state current might be captured in the compact model either by a change in the mobility or in the contact resistance. Since the transistors under investigation in this section have very large gate-to-contact overlap lengths (20 µm and 50 µm) the contact resistances are very small. Thus, it is decided to capture the effect of the temperature-dependent change in terms of a mobility change. However, as will be shown by means of a TLM analysis, the contact resistance also exhibits changes with the temperature.

7.5.2 Modeling of the Temperature Dependence

Temperature Dependence of the Threshold Voltage

According to ref. [36], the threshold voltage has a dependence on the trap densities and the temperature:

$$V_{T0} = V_{fb} + E_g/(2q) + qN'_{t,max}/C'_{diel} - \alpha \frac{k_B T}{q} \ln\left(\frac{q d_m N_{st}}{C'_{diel} \alpha k_B T/q}\right) \tag{7.48}$$

where V_{fb} is the flatband voltage, E_g is the band gap of the organic semiconductor, q is the elementary charge, $N'_{t,max}$ is the density of deep bulk and interface states which are filled in accumulation, C'_{diel} is the gate dielectric capacitance per gate area, α is the slope degradation factor, k_B is the Boltzmann constant, d_m is the thickness of the accumulation channel, and N_{st} is a fitting parameter representing the equivalent shallow trap density, i.e. the density of states that can be occupied by quasi-mobile charges. Since this equation has many unknown values

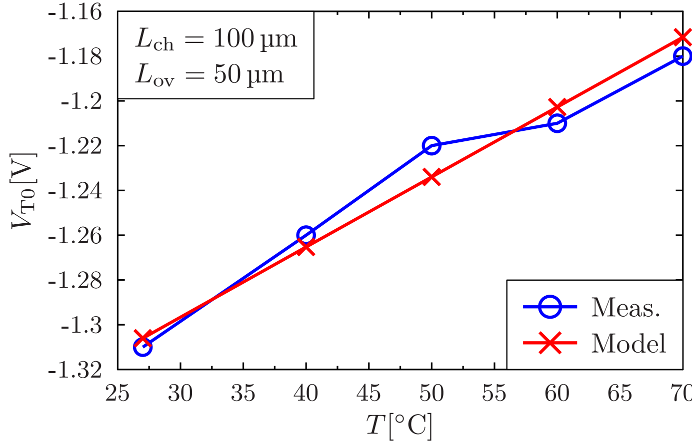

Figure 7.63.: Threshold voltage of a staggered OTFT. The values extracted from the backward sweep of the measured curves (blue line with circles) are compared to the modeled values (red line with crosses). Equation (7.49) is used as the model with the following parameter values: $A_v = 2.3$ and $B_v = 1e7$. The value for α is calculated at a temperature of $T = 27\,°C$. The transistor has a channel length of $L_{ch} = 100\,\mu m$ and a symmetric gate-to-contact overlap length of $L_{ov,GS} = L_{ov,GD} = L_{ov} = 50\,\mu m$.

and since in the derivation presented in ref. [36] some inaccurate assumptions are made, the threshold voltage cannot be calculated analytically. However, the above-presented equation can be used in order to derive an expression for the temperature dependence of the transistors. By summing up the unknown values in constants A_v and B_v, the threshold voltage can be expressed in a simplified form as:

$$V_{T0} = A_v - \alpha \frac{k_B T}{q} \ln\left(\frac{B_v}{\alpha k_B T/q}\right). \tag{7.49}$$

In Fig. 7.63, the extracted threshold voltage is shown in comparison to the model equation where A_v and B_v are treated as fitting parameters. With this procedure, it is possible to reproduce the measured change of the threshold voltage well. It has to be pointed out that the change in the threshold voltage is only small but obviously not negligible.

Temperature Dependence of the Sub-Threshold Swing

The sub-threshold swing is degraded as traps are present in the bandgap of the semiconductor or at the interface between semiconductor and gate dielectric. In ref. [36], this is reflected by the temperature-independent slope degradation factor α. The following equation relates the sub-threshold swing to the slope degradation factor [36]:

$$S_\mathrm{obs} = \alpha \ln(10) \frac{k_\mathrm{B} T}{q}. \tag{7.50}$$

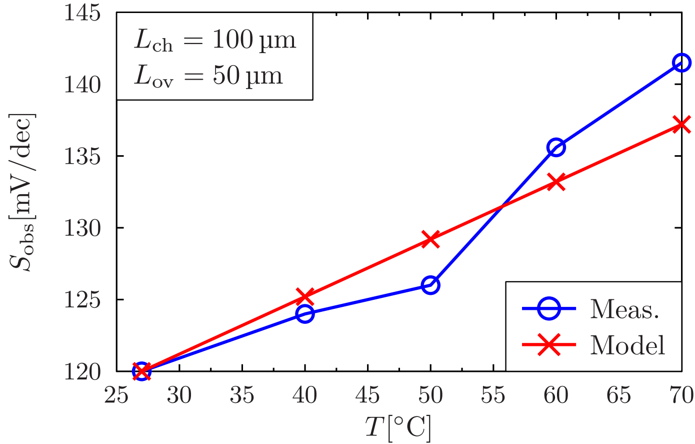

Figure 7.64.: Sub-threshold swing of a staggered OTFT. The values extracted from the backward sweep of the measured curves (blue line with circles) are compared to the modeled values (red line with crosses). Equation (7.52) is used as the model. The transistor has a channel length of $L_\mathrm{ch} = 100\,\mu\mathrm{m}$ and a symmetric gate-to-contact overlap length of $L_\mathrm{ov,GS} = L_\mathrm{ov,GD} = L_\mathrm{ov} = 50\,\mu\mathrm{m}$.

Accordingly, if the sub-threshold swing at $T = 27\,°\mathrm{C} = 300\,\mathrm{K}$ is known, it can be related to the swing at another temperature:

$$\frac{S_\mathrm{new}}{S_{300}} = \frac{T_\mathrm{new}}{300\,\mathrm{K}} \tag{7.51}$$

where the temperature T_new has to be entered in units of Kelvin. Rearranging this equation for the new sub-threshold swing leads to:

$$S_\mathrm{new} = S_{300} \frac{T_\mathrm{new}}{300\,\mathrm{K}}. \tag{7.52}$$

This equation is used as a very simple approach to calculate the swing based on the knowledge of the swing at $T = 27\,^{\circ}\mathrm{C} = 300\,\mathrm{K}$. As can be seen in Fig. 7.64, this simple model has an acceptable agreement with the sub-threshold swing extracted from the measurements.

Temperature dependence of the mobility

The low-field mobility of the compact model needs to be changed in order to fit the compact model to the different transfer curves. In the literature, it has been reported that the power-law exponent can as well be modeled as temperature-dependent [117] but a change in the power-law exponent changes the curvature of the transfer curves. However, the curvature does not need to be changed in this case. It is sufficient to change the low-field mobility κ. In order to capture the influence of the temperature on the low-field mobility, the Arrhenius mobility law is used which reads as follows [118]:

$$\kappa = \mu_{\mathrm{Arrh}} \exp\left(-\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}T}\right), \tag{7.53}$$

where μ_{Arrh} is the mobility at very high temperatures and E_{a} is the activation energy. With the temperature increasing, the value of the exponential function converges to unity. Thus, κ converges to μ_{Arrh} which can be imagined as the mobility in the fully activated case. This simple model is used in order to capture the temperature dependence of the mobility. As can be seen in Fig. 7.65, the model is able to capture the extracted low-field mobility with acceptable accuracy.

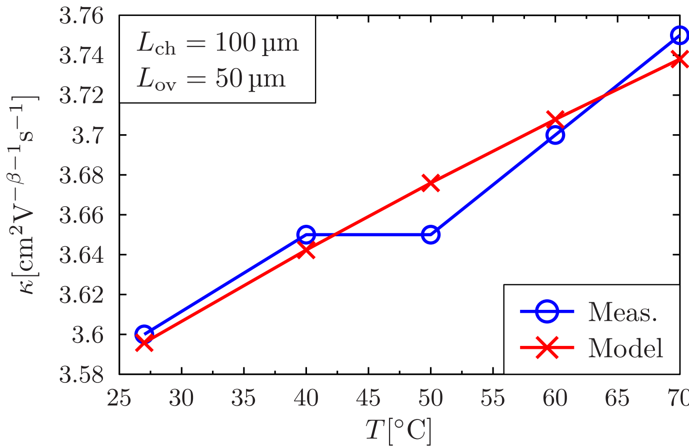

Figure 7.65.: Low-field mobility of a staggered OTFT. The values extracted from the backward sweep of the measured curves (blue line with circles) are compared to the modeled values (red line with crosses). Equation (7.53) is used as the model with the following parameters: $\mu_{\mathrm{Arrh}} = 4.9\,\mathrm{cm^2V^{-\beta-1}s^{-1}}$ and $E_{\mathrm{a}} = 8\,\mathrm{meV}$. The transistor has a channel length of $L_{\mathrm{ch}} = 100\,\mu\mathrm{m}$ and a symmetric gate-to-contact overlap length of $L_{\mathrm{ov,GS}} = L_{\mathrm{ov,GD}} = L_{\mathrm{ov}} = 50\,\mu\mathrm{m}$.

7.5.3 Investigation of the Contact Resistance

The transistors under investigation in this section only have small contact resistances in comparison to the intrinsic channel resistances. The reason is that the gate-to-contact overlap lengths are long (20 µm and 50 µm) so that the injection in the source region does not become limited. However, although it is only of small magnitude, it is worth investigating the temperature dependence of the contact resistance. A common method for the separation of the contact resistance and the channel resistance is the transmission-line method (TLM) [17]. This method was also used for the transistors presented in Sec. 7.4. Here, some more details about the TLM analysis will be presented.

For the TLM method, the transistor is assumed to consist of a series connection of an inner transistor and contact resistances. The contact resistance R_{C} is defined as the sum of all source and drain contact resistances. The resistance of the intrinsic transistor channel is assumed to be proportional to the channel length L_{ch} [17] which is in agreement with the DC current equation (Eq. (2.21)) where I_{ds} is inversely proportional to L_{ch}. In order to separate the contact resistances from the channel resistances, a set of transistors with equal gate-to-contact overlap lengths but different channel lengths is fabricated. The transistor for which the temperature-dependent modeling of some model parameters is presented above is part of this set of transistors.

For each transistor, transfer curves at a low drain-source voltage ($V_{\mathrm{ds}} = -0.1\,\mathrm{V}$) are measured at different temperatures in the order as depicted in Fig. 7.61. For each temperature, the TLM analysis is conducted by the following procedure:

1. For each transistor with the different channel lengths, the threshold voltage is determined at each of the measured temperatures. This is achieved by applying a tangent in a very linearly shaped region of the transfer curve and then extrapolating it to the V_{gs}-axis. The voltage at which the intersection occurs is $V_{\mathrm{T0}} + 0.5 \cdot V_{\mathrm{ds}}$ [5].

2. For each temperature, the current of each transistor is probed at various gate-overdrive voltages. The gate-overdrive voltage is defined as the amount by which V_{gs} extends the threshold voltage: $V_{\mathrm{odr}} = V_{\mathrm{gs}} - V_{\mathrm{T0}}$. At each V_{odr}, the resistance between drain and source of the transistor comprising contact resistances is calculated and normalized with respect to the channel width $W_{\mathrm{ch,SD}}$. This resistance is denoted as RW and is calculated as $RW = (V_{\mathrm{ds}}/I_{\mathrm{ds}}) \cdot W_{\mathrm{ch,SD}}$. It contains the influence of the contact resistances and of the intrinsic transistor channel.

3. For each temperature and each gate-overdrive voltage, the contact resistance can now be calculated by performing a linear regression for the RW values versus the channel length and extrapolating this regression function towards $L_{\mathrm{ch}} = 0\,\mathrm{\mu m}$. A device without a channel does not have a channel resistance and hence, the only resistance remaining is the contact resistance. Of course, a transistor without a channel cannot be fabricated.

However, the extrapolation of the RW values towards $L_{\mathrm{ch}} = 0\,\mu\mathrm{m}$ estimates the resistance that such a theoretical device would have. By assuming that all the transistors have the same contact resistances, the regression thus leads to the width-normalized contact resistance $R_{\mathrm{C}}W$.

4. The width-normalized contact resistance $R_{\mathrm{C}}W$ is probed at a fixed gate-overdrive voltage for different temperatures.

For a fixed V_{odr}, the width-normalized resistances RW as mentioned in point 2.) can be plotted for the various transistors with the different channel lengths. This is shown in Fig. 7.66 where RW is plotted for a set of transistors with $L_{\mathrm{ov,GS}} = L_{\mathrm{ov,GD}} = 20\,\mu\mathrm{m}$ at three arbitrarily chosen gate-overdrive voltages. Here, the results at $T = 27\,°\mathrm{C}$ are shown. The linear functions are the regression functions through the different RW values. As predicted, the total resistance of the series connection consisting of the transistor and the contact resistance is decreasing at smaller channel lengths.

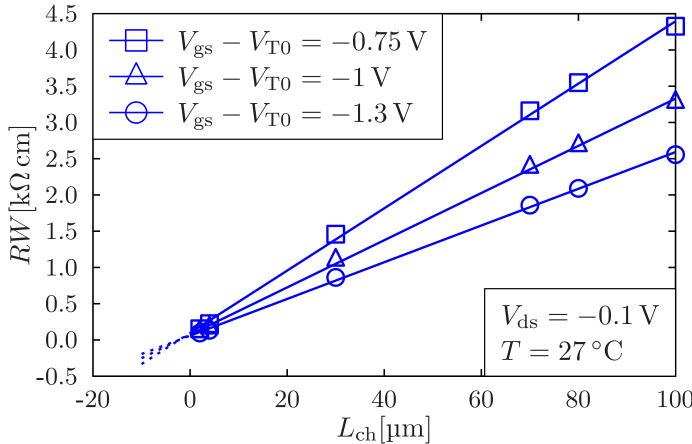

Figure 7.66.: RW plotted against the channel length for the transistors with a symmetric gate-to-contact overlap length of $L_{\mathrm{ov,GS}} = L_{\mathrm{ov,GD}} = 20\,\mu\mathrm{m}$. The resistances RW are shown for three arbitrarily chosen gate-overdrive voltages $V_{\mathrm{odr}} = V_{\mathrm{gs}} - V_{\mathrm{T0}}$ at a temperature of $T = 27\,°\mathrm{C}$.

Figure 7.67 depicts the width-normalized contact resistances $R_{\mathrm{C}}W$ versus the gate-overdrive voltage at a fixed temperature of $T = 27\,°\mathrm{C}$ as mentioned in point 3.). It can be seen that the contact resistance is not constant but varies with the applied voltages. This is in accordance with the findings in ref. [47] that the contact resistances are a non-linear function of the voltages due to the effect of the Schottky barrier lowering.

In order to visualize the influence of the temperature on the contact resistances, $R_{\mathrm{C}}W$ is plotted against the temperature at a fixed gate-overdrive voltage as mentioned in point 4.). In Fig. 7.68, the results of the transistors with a gate-to-contact overlap length of $L_{\mathrm{ov,GS}} = L_{\mathrm{ov,GD}} = 20\,\mu\mathrm{m}$ and with $L_{\mathrm{ov,GS}} = L_{\mathrm{ov,GD}} = 50\,\mu\mathrm{m}$ are depicted. It becomes visible that the transistors with the

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longer gate-to-contact overlap length have an overall smaller contact resistance. Furthermore, the curves of both transistor sets show the general trend that with higher temperature the contact resistance is decreasing. However, the contact resistance at $T = 60\,^{\circ}\mathrm{C}$ does not agree with the other data points. This behavior is attributed to the order in which the temperatures are swept. The temperature profile is defined as depicted in Fig. 7.61. It can be seen that prior to measuring the transistors at $T = 60\,^{\circ}\mathrm{C}$, a high temperature of $T = 90\,^{\circ}\mathrm{C}$ is applied. The observable trend in the $R_{\mathrm{C}}W$ curves leads to the assumption that at the application of this high temperature, a mid-term degradation effect must have changed the contact resistance. This has to be subject to future research.

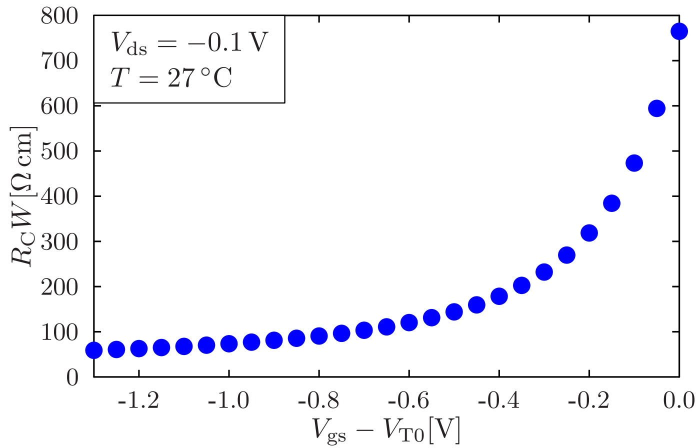

Figure 7.67.: $R_{\mathrm{C}}W$ plotted against the gate-overdrive voltage $V_{\mathrm{odr}} = V_{\mathrm{gs}} - V_{\mathrm{T0}}$ at a temperature of $T = 27\,^{\circ}\mathrm{C}$ for the transistors with a symmetric gate-to-contact overlap length of $L_{\mathrm{ov,GS}} = L_{\mathrm{ov,GD}} = 20\,\mu\mathrm{m}$.

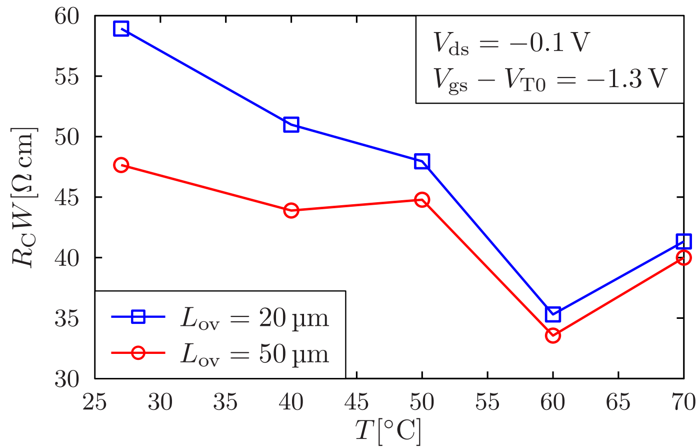

Figure 7.68.: $R_{\mathrm{C}}W$ plotted against the temperature at a fixed gate-overdrive voltage of $V_{\mathrm{odr}} = V_{\mathrm{gs}} - V_{\mathrm{T0}} = -1.3\,\mathrm{V}$ for the transistors with a symmetric gate-to-contact overlap length of $L_{\mathrm{ov,GS}} = L_{\mathrm{ov,GD}} = 20\,\mu\mathrm{m}$ (blue squares) and with $L_{\mathrm{ov,GS}} = L_{\mathrm{ov,GD}} = 50\,\mu\mathrm{m}$ (red circles).

CHAPTER 8

State of the Art

There already exists a variety of compact models that include a description of the capacitive behavior of OTFTs. Furthermore, there also exist models describing the low-frequency noise in OTFTs. In this section, a summary of some models found in the literature will be given. All of the capacitance models are based on an underlying DC compact model which will briefly be described as well.

8.1 Capacitance

8.1.1 Model by Castro-Carranza

Castro-Carranza et al. developed a compact model for the capacitances in OTFTs [109, 119] which will be described in the following. The underlying DC compact model is based on the unified model and parameter extraction method (UMEM) [120] which defines a parameter-based compact model. The compact model uses empirical fitting parameters for the calculation of effective gate-overdrive and effective drain-source voltages. The drain-source current consists of a two-piece expression where the sub-threshold and the above-threshold components are calculated separately and then merged into a combined equation by a transition function. The current equation is valid for the linear and the saturation regime of operation.

The capacitances are calculated following a similar approach as it is done in this work: the total gate charge is defined as the integral over the mobile charge per gate area from the source to the drain, comparable to Eq. (4.1). The mobile charge per gate area is expressed as

$$Q'_{\mathrm{m}} = C'_{\mathrm{diel}} \cdot (V_{\mathrm{odr}} - V)\,, \tag{8.1}$$

where C'_{diel} is the gate dielectric capacitance per gate area, V_{odr} is the gate-overdrive voltage, and V is the channel voltage. The voltage V_{odr} is in principle the difference of $V_{\mathrm{gs}} - V_{\mathrm{T0}}$. However, in order to avoid numerical problems in the sub-threshold regime, an empirical function

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prevents V_{odr} from becoming negative. The above-defined equation for the mobile charges is in principle equivalent with the expression defined in ref. [36] which is, however, an approximation only valid in the above-threshold regime. Even if V_{odr} is prevented from becoming negative in the compact model, the value that is yielded for Q'_{m} is no longer valid. Similarly as in the compact model presented in this thesis, Castro-Carranza et al. substitute the variable x in the charge integral by making use of the drift-diffusion differential, see Eq. (4.5). Based on this, a closed-form equation for the total charges in the channel is yielded. Using the Ward-Dutton partitioning scheme [65], the charges are attributed to a certain degree to belong to the drain and the source terminals of the transistor. The charge equations are analytically derived with respect to the terminal voltages which leads to the capacitances. Since the resulting charge equations are based on Eq. (8.1) which is only valid in the above-threshold regime they are also valid only in this regime. For this purpose, in ref. [109], a capacitance for the depletion (sub-threshold) region of operation is defined. Similarly as for the DC current model, the two capacitances for the sub-threshold regime and the above-threshold regime are merged by an empirical fitting function. This leads again to an equation valid in for all regimes of operation.

In addition to the intrinsic channel charges, the model also includes a very basic description of the extrinsic gate-to-contact-overlap charges for coplanar OTFTs, similar as in Eqs. (4.23) and (4.24). However, charges in fringe regions are not accounted for. The model is only valid for transistors comprising negligible contact resistances since a voltage drop across contact elements is not considered. The charge conservation, however, is ensured since the model does not treat the capacitances as lumped elements. In this regard, the capacitance model can be denoted as a charge-based model but the underlying DC model is not charge-based, as explained above.

When it comes to high-frequency operation, the charges cannot follow the applied voltages and non-quasistatic effects become important. These non-quasistatic effects are taken into account in ref. [109] by the definition of a frequency-dependent decay of the dielectric constant of the gate insulator. This equation served as the inspiration for the scaling function C_{scale} in Eq. (7.39). A reasonable agreement with the measured total gate capacitance of OTFTs is achieved.

The main features of the model are summed up in the following:

- No charge-based model
- Closed-form description
- Continuous model but only with the help of transition functions for different operation regimes
- Overlap charges for coplanar transistors are included

- Overlap charges for staggered transistors are not included
- Voltage drop at contact elements is not considered and thus, only long-channel transistors are accurately modeled
- The charges are conserved
- Fringe effects from layout perspective are not accounted for
- Non-quasistatic effects are not considered

8.1.2 Model by Marinov and Deen

Marinov and Deen developed a comprehensive compact model for the quasistatic DC and AC characterization of OTFTs [66]. The model uses the DC description derived in refs. [121, 122]. This model has similarities with the model by Castro-Carranza et al. [109, 119] in the regard that both are parameter-based models. The Marinov-Deen model is a charge-drift dependent model that also uses effective overdrive voltages. The overdrive voltages are defined by a fitting function that provides a smooth transition from the sub-threshold to the above-threshold regime. Furthermore, the model contains a power-law mobility that is exponentially dependent on the gate-overdrive voltage. In contrast to the DC model developed in the TH Mittelhessen group [36] where the power-law mobility is dependent on Q'_{ms} and thus on the gate-source voltage, the power-law mobility in the Marinov-Deen model is changing along the channel in dependence of the channel potential.

The intrinsic channel capacitances are calculated following the same basic concept as in the work by Castro-Carranza et al. [109, 119] and in the model presented in this thesis: again, the charge integral like in Eq. (4.1) is used and the Ward-Dutton partitioning scheme [65] is employed. Afterwards, the variable x is again replaced making use of the drift-diffusion model so that the integration is performed over the voltages rather than the position in the channel. As a result, the total charges associated with the gate, drain and source are yielded. The resulting equations have some similarities with the equations derived in this work but since the underlying DC compact model is a parameter-based model and since the power-law mobility behaves different from the power-law mobility in the model developed in this thesis, there are differences.

The Marinov-Deen model is not charge-based since it is a parameter-based drift-model but since the total charges are correctly calculated and the simple Meyer model is not used the total charges are conserved.

The gate-to-contact overlap capacitances are only accounted for in coplanar transistors in a similar manner as in Eqs. (4.23) and (4.24) in the work presented in this thesis. However, with an extension presented by Scheinert et al., the overlap capacitances in staggered transistors

can be calculated, as well [61]. Furthermore, the Marinov-Deen model does not include fringe capacitances from the layout perspective as they appear in the transistor architecture under investigation in this work. In the Marinov-Deen model, there is also an inclusion of extrinsic capacitances denoted as fringe capacitances which originate from a capacitance on the back of the TFT film. Scheinert et al. proposed a numerical inclusion of the fringe capacitance in the transistors fabricated at the Max Planck Institute for Solid State Research by simply defining a multiplication factor for the charges [61]. Non-quasistatic effects are not captured by the model.

The main features of the model are summed up in the following:

- No charge-based model
- Closed-form description
- Continuous model but only with the help of a transition function calculating the effective overdrive voltages from the deep sub-threshold regime to the above-threshold regime
- Overlap charges for coplanar transistors are included
- Overlap charges for staggered transistors are not included but an extension of the model has been proposed [61]
- Voltage drop at contact elements is considered and thus, transistors with shorter channels could in principle be modeled
- The charges are conserved
- Fringe effects from layout perspective are not accounted for with regard to the structures under investigation in this work
- Non-quasistatic effects are not considered

8.1.3 Model by Valletta

Valletta et al. developed a compact model following a quite different approach from what has been presented so far. In ref. [18], a model for the complete description of the DC and AC behavior of OTFTs is proposed, even valid for the high-frequency regime of operation.

The DC description incorporates the special properties of an inversely-operated Schottky barrier at the source-to-semiconductor junction. The compact model treats an OTFT as a series connection of an ideal TFT (i.e. a TFT following the gradual channel approximation) and an inversely-operated Schottky diode at the source. As a consequence of the voltage drop across the Schottky barrier, the ideal transistor has reduced voltages. In Fig. 8.1, the equivalent

circuit that the model is based on is shown. For the inner transistor, the current is formulated based on the outer terminal voltages and the contact voltage drop V_{cs}:

$$I_{\mathrm{TFT,ideal}} = f\left(V_{\mathrm{gs}}, V_{\mathrm{ds}}, V_{\mathrm{cs}}\right). \tag{8.2}$$

The current flowing through the inversely-operated Schottky diode is expressed based on the well-known Schottky-diode relationship including the effect of the Schottky barrier lowering [18]:

$$I_{\mathrm{diode}} = -I_0 \cdot \exp\left[\left(\frac{V_{\mathrm{cs}}}{V_0}\right)^{\alpha}\right] \cdot \left(\exp\left[-\left(\frac{qV_{\mathrm{cs}}}{\eta k_{\mathrm{B}} T}\right)\right] - 1\right), \tag{8.3}$$

where α, V_0, and η are fitting parameters that must not be mistaken with the fitting parameters of the compact models presented in this thesis. The reverse saturation current I_0 of the diode is expressed as [18]:

$$I_0 = I_{00} \cdot \left(\frac{V_{\mathrm{gs}}}{V_{00}}\right)^{\beta}, \tag{8.4}$$

where I_{00} and β are fitting parameters and V_{00} has a constant value of 1 V in order to ensure a unitless value in the parentheses. Since both the diode current and the current of the ideal TFT are dependent on the voltage V_{cs}, there is no closed-form solution for the current flowing through the series connection consisting of the Schottky diode and the TFT. The condition is that the diode current (I_{diode}) has to equal the current flowing through the transistor ($I_{\mathrm{TFT,ideal}}$). Valletta et al. thus have the voltage V_{cs} numerically computed by the SPICE simulator. Afterwards, V_{cs} is inserted either in the transistor or in the diode equation which then leads to the DC current. Due to the lack of a closed-form description of the DC behavior, the model can be denoted as an implicit model.

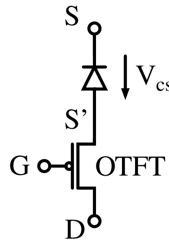

Figure 8.1.: Equivalent circuit that the implicitly-defined model by Valletta et al. is based on [18]. The transistor is assumed as a series connection of an ideal TFT and a reversely-operated Schottky diode at the source.

For the small-signal AC model, Valletta et al. use the transmission-line approach [64] that is also discussed in Chap. 7.2. In ref. [64], the channel of a transistor is treated as a distributed *RC* transmission line and the complex impedance of this transmission line is expressed in dependence on the voltage-dependent channel conductance. This approach is also used in the literature in order to characterize the non-quasistatic behavior of OTFTs [40, 123].

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Since the DC model by Valletta et al. is only implicitly defined, there is no closed-form solution for the channel conductance. Therefore, the channel conductance is calculated for an ideal TFT which is then inserted into the transmission-line equation. Thus, the important properties of the reversely-operated Schottky barrier are neglected at this stage. Valletta et al. now use the transmission line model to calculate the impedance in several regions of the transistor. The contact resistances are then included in a numerical way by defining the conductance G_{c} and the capacitance C_{c} of the metal-to-semiconductor junctions as fitting parameters. Finally, the total admittance between the gate and the source contact (Y_{gs}) and between the gate contact and the drain contact (Y_{gd}) are obtained by summing up all the single admittances that contribute to it. This eventually leads to the capacitances C_{gs} and C_{gd}. Since the model is based on an admittance which is dependent on the frequency the capacitances are also automatically dependent on the frequency. Therefore, the non-quasistatic behavior can be captured. However, the drawback is that the capacitances are assumed to be reciprocal which leads to the problem of charge-non-conservation which also occurs in the Meyer model [38].

Extrinsic capacitances are also taken into account in this model. In principle, the structure under investigation is a multi-finger OTFT in the staggered architecture. However, the exact layout is different from the transistors under investigation in this thesis. Valletta et al. include the gate-to-contact overlap capacitances which they calculate as for a coplanar TFT even if the layout is staggered. Therefore, the model will produce inaccurate results if the overlap capacitances dominate over the intrinsic channel capacitances. Fringe capacitances that occur in the used layout are included in the model.

The main features of the model are summed up in the following:

- No charge-based model
- No closed-form description
- Continuous model but only with the help of a transition function calculating the effective overdrive voltages from the deep sub-threshold regime to the above-threshold regime
- Overlap charges for coplanar transistors are included
- Overlap charges for staggered transistors are not included
- Voltage drop at contact elements is considered by defining the contact admittance as a fitting parameter
- The charges are not conserved since the capacitances are reciprocal
- Fringe effects from layout perspective are taken into account but they differ from the layout investigated in this thesis
- Non-quasistatic effects are considered

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8.1.4 Model by Torricelli

Torricelli et al. proposed a compact model for the DC and quasistatic capacitances in OTFTs [69]. The variable-range-hopping theory as mentioned in Chap. 1 serves as the basis for this model. The conductivity of the organic semiconductor is expressed based on the density of accumulated charges and the drain current is obtained by an integration over this conductivity. The density of accumulated quasi-mobile charges is expressed in terms of the surface potential which is the electrostatic potential in the organic semiconductor close to the interface with the gate insulator. Performing several substitutions, the drain current is expressed based on the charge densities at the source and the drain end of the channel. In this regard, the model by Torricelli et al. [69] is comparable to the DC compact model of the TH Mittelhessen group [36]. However, the difference is that Torricelli et al. use a different way for the calculation of the charge densities at the source/drain end of the channel. For the calculation of these charge densities, the surface potential at the source/drain end is needed explicitly. However, the surface potential is an implicit function which cannot be solved analytically. In order to overcome this deficiency, a case distinction is performed and the surface potential is approximated by simple expressions in dependence on the regime of operation. However, the potential can only be approximated accurately if the transistor is operated in the above-threshold regime. Thus, the model does not provide a description for the full range of possible bias conditions.

For the calculation of the quasistatic capacitances, the model follows in principle the same approach as the compact model developed in this thesis: the charges are yielded by an integration over the charge density per gate area along the channel. Equally as in the model presented in this work, the drift-diffusion differential like in Eq. (4.5) is used. A change in the gate potential is then linked to the change in the accumulated charge density which leads to nearly the same differential as in ref. [36]. Consequently, the derivation of the total charges according to Torricelli et al. is very similar to the model that was developed in this thesis. The total charges associated with the source and the drain terminals are yielded by applying the Ward-Dutton partitioning scheme [65]. In this approach, the charges are conserved properly. The capacitances are calculated explicitly by deriving the charges with respect to the terminal potentials. However, the model does not contain any contributions to the capacitances by extrinsic factors such as gate-to-contact overlap regions or fringe effects.

The capacitance model does not include frequency-dependent effects so that it is not suitable for a non-quasistatic operation. However, Valletta et al. extended the model by Torricelli et al. so that it can be used in a large-signal analysis [103, 104]. There, the current continuity equation is used and discretized by a spline collocation which finally leads to a system of ordinary differential equations which can numerically solved in the SPICE simulator.

The main features of the model are summed up in the following:

- Charge-based model
- Closed-form description only by approximation of the surface potential in different operation regimes
- If the closed-form description is used, the model may show a discontinuous behavior at the transition between the linear and the saturation regime of operation
- Overlap charges for coplanar transistors are not included but in the large-signal extension in [103, 104], overlap charges for simple gate-to-contact overlap regions are accounted for
- Overlap charges for staggered transistors are not included
- Voltage drop at contact elements is not considered
- The charges are conserved
- Fringe effects from layout perspective are not taken into account but in the extension in [103, 104] they are included
- Non-quasistatic effects not considered but are contained in the extension [103, 104]

8.1.5 Model by Colalongo

L. Colalongo proposed a model denoted as the symmetric quadrature method [30]. This model has similarities with the compact model by Torricelli et al. [69] in the regard that both use the variable-range-hopping model as the basis. The model by Colalongo expresses the charge density per gate area as an integral function of the surface potential which is, however, not analytically solvable. An approximation is performed so that this function can be evaluated in a closed form. However, the difficulty is that the surface potential is an implicit function of the applied terminal voltages. Thus, it is solved numerically and approximated by a function.

Observing the plot of the charge density versus the surface potential, the following observation is made in ref. [30]: The charge density is not a linear function of the surface potential but resembles a quadratic function. Therefore, the charge density is modeled as a quadratic function the center of with is at the so-called surface potential midpoint which is the average of the surface potential at the source end and the drain end of the channel. The parameters of the quadratic function are defined by forcing the function to have the same function values at the source end, the drain end and the mid-point as the full numerical solution of the charge-density function versus the surface potential. After the approximations are performed, the drift-diffusion model is used and the quadratic approximation of the charge density versus the surface potential is incorporated. This leads to a continuous model for the drain current.

For the derivation of a quasistatic capacitance model, the well-known charge integrals incorporating the Ward-Dutton partitioning scheme [65] are used as in Eqs. (4.2) and (4.3) in this work. However, the substitution of the integration variable x is performed slightly differently. Again adapting the drift-diffusion model, a differential linking a change in the position in the channel to the surface potential is obtained which is then substituted in the charge integrals. During the integration, the charge density per gate area is evaluated at the source and the drain end of the channel, and also at the above-mentioned channel-potential midpoint. Therefore, the final results of this model are equations for the total charges in dependence on the charge densities per gate area. In this regard, the model by Colalongo has similarities with the approach that is followed in this thesis. Since the surface potential at the source/drain end is known in the model, the overlap charges in staggered transistors can be included properly. However, non-quasistatic effects are not accounted for.

The main features of the model are summed up in the following:

- Model based on the surface potential
- Closed-form description only by approximation of the surface potential and also by an approximation of the relation between the charge density and the surface potential
- Continuous model valid for all regimes of operation from sub-threshold to above-threshold including linear and saturation regimes
- Overlap charges for coplanar transistors are not included but since the more-complicated staggered transistors are accounted for the coplanar counterparts could easily be added as well
- Overlap charges for staggered transistors are included by making use of the surface potential in the gate-to-contact overlap region
- Voltage drop at contact elements is not considered
- The charges are conserved
- Fringe effects from layout perspective are not taken into account
- Non-quasistatic effects are not considered

8.1.6 Other Approaches

In this section, additional approaches are briefly reviewed.

Wang et al. proposed a surface-potential-based compact model for the description of the DC behavior and the quasistatic capacitances in OTFTs [31]. A Gaussian density of states is assumed and the Gaussian law linking the electric field and the charges is applied. This leads to an implicit function for the surface potential. In order to come to a closed-form solution, the surface potential is approximated for the two extreme cases of a very strong and a very weak accumulation and the two approximation functions are connected in a transition function. Incorporating a power-law mobility and the drift-diffusion model, an expression for the drain current is yielded which depends on the terminal voltages and the surface potential. The total charges in the transistor are again calculated based on the three charge integrals as in Eqs. (4.1), (4.2) and (4.3) in this work. The integration variable x is substituted so that the integration is performed over the surface potential. Finally, the total charges are yielded.

Li et al. proposed a compact model based on the percolation theory [32]. The model is based on the approximation of the density of states by a sum of two exponential functions representing deep tail states and states in the higher concentration. The percolation theory combines the carrier concentration and the conductivity of the channel. Applying the gradual channel approximation and using a power-law mobility, closed-form expressions for the drain current are obtained. However, the model is only capable of calculating the sub-threshold current and the current in the linear regime of operation. The saturation regime is not covered. Furthermore, the sub-threshold and the linear current have to be combined by a transition function since no one-piece expression can be defined. Finally, the total charges associated with the gate, the drain, and the source terminals are obtained again by the integrals as in Eqs. (4.1), (4.2) and (4.3) in this work. The drift-diffusion model is used and the integration variable is changed from x to the voltage. The Ward-Dutton partitioning scheme [65] is used and finally, voltage-based charge equations valid only in the linear regime of operation are yielded.

Both above-mentioned models [31, 32] do not contain extrinsic charges such as the gate-to-contact overlap charges. Fringe effects and non-quasistatic effects are not contained.

In ref. [98], another model is proposed. There, the basic starting point is the assumption of two superposed exponential density-of-states functions describing the states in which charge carriers behave as immobile or mobile charges, respectively. Introducing a surface potential, the amount of charge can be calculated. The voltage-dependent Poole-Frenkel mobility is used and making use of the drift-diffusion model, the drain current can be calculated. The effect of a non-linear contact resistances due to the Schottky barriers is taken into account as well. However, no closed-form solution for the model is given. Rather, the transistor is treated as

a macro model consisting of an inner transistor and parasitic contact elements, which has to be solved numerically, e.g. by a circuit solver. Furthermore, the DC model is dependent on the surface potentials at the drain and the source end of the channel. No closed-form calculation method for the surface potential is presented. The model in ref. [98] also contains a description of the quasistatic capacitances. Similarly as for most of the models reviewed here, the charges are calculated based on the charge integrals as in Eqs. (4.1), (4.2) and (4.3). The integration variable is replaced by the surface potential. The advantage of this model is that the influence of the contact resistances is taken into account since the numerical solution of the series connection of an inner transistor and contact elements correctly calculates the surface potential at the source and the drain end of the channel. However, as explained before, the model does not contain a closed-form description.

8.2 Models for the Low-Frequency Noise

There exists a variety of literature where the noise in OTFTs is investigated or modeled. However, the difficulty is that due to the huge diversity in the methods of fabricating OTFTs, there are many different types of noise behavior and it is thus unlikely that a model can be developed that is generally valid for all types of OTFTs [84].

8.2.1 General Investigation of Noise Models

Marinov and Deen presented a comprehensive literature summary of various models describing the noise behavior of OTFTs [84]. In this section, some of the most important points and other pieces of literature will be reviewed. To start with, it can be said that due to the variety in OTFTs and their fabrication methods, there are different types of noise which these devices exhibit. Comprehensive compact models for the low-frequency noise in OTFTs can hardly be found in the literature. Often, the standard models for Hooge mobility fluctuations or charge-carrier number fluctuations as described in MOSFETs are used with small modifications in order to describe the measured noise of fabricated OTFTs [76, 82, 83, 124–127]. Han et al. developed a full comprehensive model for the noise originating from carrier-number fluctuations in pentacene-based OTFTs [85]. This model will be described in more detail because it has many similarities with the approach pursued in this thesis. There exists another approach which has been described in ref. [128]. There, the noise is described by a tunneling of charge carriers between the mono-layers of the semiconductor. This model only works if the semiconductor can really be assumed as a homogeneous film consisting of several monolayers. Marinov and Deen developed a numerical model for the description of low-frequency noise due to the variable-range hopping in OTFTs. This model will briefly be reviewed, as well.

8.2.2 Model by Han

Han et al. proposed an analytical, closed form model for the low-frequency noise in pentacene-based OTFTs [85]. Carrier generation-recombination processes are chosen as the origin for the noise. Han et al. describe that in OTFTs there may occur the phenomenon that the low-frequency noise does not follow a $1/f$ trend when plotted against the frequency, but more a $1/f^2$ trend. They attribute this behavior to the fact that charge carriers can be trapped not only in the gate dielectric but also in the organic semiconductor. These two noise components show a different behavior with respect to the frequency:

- When carriers get trapped in or released from traps located in the gate dielectric, the resulting noise spectrum exhibits the typical $1/f$ trend.
- When carriers get trapped in or released from traps located in the organic semiconductor, the resulting noise spectrum shows a $1/f^2$ behavior.

Combining the two noise components is a novelty and it enables the capturing of different slopes in the noise spectrum without the necessity of the definition of an empirical fitting parameter as the exponent of the frequency. The model incorporates physics-based fitting parameters such as the density of traps in the gate dielectric and the organic semiconductor and the decay times of the traps.

The model, however, is not charge-based and depends on the total number of carriers in the channel as calculated for the simple MOSFET model. Thus, the model is only applicable to OTFTs exhibiting low contact resistances. Anyway, the authors achieve a good agreement between the model and measured OTFTs comprising pentacene as the organic semiconductor and different gate dielectrics. The model is only suitable if the noise origin in the transistors under investigation is the trapping and de-trapping of charge carriers. In case that the bulk mobility fluctuations are dominant, a different approach needs to be pursued.

8.2.3 Model by Marinov and Deen

Marinov and Deen proposed a numerical model describing the noise in OTFTs based on the VRH theory [129] according to which the current conduction in OTFTs occurs by a hopping of charge carriers between localized states. The interesting fact about the noise model proposed by Marinov and Deen is that it takes into account the noise originating from the distribution of the different hopping times.

The model can be denoted as a modeling scheme since it allows the inclusion of different types of noise such as mobility fluctuations and the fluctuation of the charge-carrier number. Depending on the type of noise, the distribution of the hopping times varies. The noise model itself is based on the empirical Hooge model which originally only describes the fluctuation

of the bulk mobility. However, due to the different distributions of the hopping times, the model can reproduce different types of noise. The model is no closed-form model but needs the numerical simulation e.g. in a finite-element simulator.

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CHAPTER 9

Conclusion

In this thesis, an existing charge-based DC compact model has been extended to describe the quasistatic charges in the channel and the low-frequency flicker noise in OTFTs. The basic channel-charge model performs an integration over the density of accumulated quasi-mobile charges. By means of several substitutions, the integral is solvable and the total amount of charges is dependent on the density of quasi-mobile accumulated charges at the source and the drain end of the channel. Applying a charge-partitioning scheme, the charges can be separated into a portion belonging to the source and the drain terminal. The intrinsic channel charges are independent of the transistor architecture (staggered or coplanar) and are valid only for the case that no remarkable contact resistances in comparison to the intrinsic channel resistance are present.

In addition to the intrinsic charges, the charge model also accounts for extrinsic gate-to-contact-overlap charges and fringe charges. In dependence on the transistor architecture, closed-form equations for the overlap charges are derived. Furthermore, the model is extended by a description for the charges in three-dimensional transistors with parasitic fringe regions. Combining the total channel charges and the extrinsic components leads to the first model state valid for the total charges in long-channel transistors in either the staggered or the coplanar device architecture. A verification of the model by means of capacitance measurements and finite-element simulations has been presented.

It is shown that the compact model without further modifications is also capable of reproducing the frequency-dependent signal-amplification gain of differential amplifiers. By implementing the model into the module-description language Verilog-A and reconstructing the circuit of the differential amplifier, a frequency dependence of the channel charges is implicitly accounted for by the interconnection of several transistors in the circuit.

Furthermore, it is shown that under the presence of contact resistances the distribution of the accumulated quasi-mobile charges is altered. A semi-empirical model has been introduced that can calculate the voltage drops over the contact resistances and can correctly alter the density of accumulated charges. In addition, a modification to the charge partitioning scheme is introduced which allows the attribution of more charges to the drain terminal. Incorporating these extensions, the model is capable of reproducing the simulation results of OTFTs comprising large Schottky barriers at the electrode-to-semiconductor junctions.

The compact model is then extended by a description of non-quasistatic effects which play a key role in OTFTs. For transistors comprising large channel lengths and negligibly small contact resistances, the channel-segmentation method is utilized by interconnecting a finite number of transistors with shorter channel lengths which taken as a whole represent one transistor. The interconnection of several transistors in such a transmission line is a macro model that automatically accounts for the frequency-dependent charging and discharging of channel capacitances through adjacent channel elements. Using this approach, the measured complex admittance of a long-channel transistor can excellently be reproduced. Furthermore, the model shows a very good agreement when compared to transient simulations of long-channel transistors in Sentaurus TCAD.

If the contact resistances are large in comparison to the intrinsic channel charges, the channel-segmentation model does not provide a proper description of the transistors. The contact resistances usually play a role in transistors comprising small channel lengths. The transistors under investigation in this work usually have comparatively large gate-to-contact overlap regions which are inevitable in the fabrication process. Therefore, the capacitive effects of short-channel transistors are often dominated by their gate-to-contact overlap regions while the intrinsic channel charge is only of minor importance. For the proper capturing of this property in OTFTs, an empirical model is proposed describing the frequency dependence of the charges by means of frequency-dependent scaling functions. It is found that special emphasis has to be put on the charges in fringe regions since they respond to the applied signals much slower than charges in the center of the channel. The model is fitted to the measured small-signal-current gain h_{21} which has been measured for coplanar as well as staggered transistors.

As an addition to the work on the capacitances, some effects of the temperature on the DC characteristics are shown and equations are proposed to capture the influence on the basic DC model.

Besides the modeling of quasistatic and non-quasistatic charges in the OTFTs, a charge-based compact model describing the low-frequency noise in OTFTs is presented. Following a standard procedure also valid for MOSFETs, equations describing two different types of noise are presented: the bulk mobility fluctuations according to the Hooge model and the fluctuations originating from the trapping and de-trapping of charge carriers according to the Mc Worther

model extended by the correlated mobility fluctuations according to the Ghibaudo model. The latter model is verified by noise measurements on OTFTs and the bulk mobility fluctuation model is verified by means of a TCAD simulation.

There are several open points that have to be addressed in the future:

- For the verification of the quasistatic capacitances, only measurements of a staggered long-channel OTFT were available. Since the capacitances of short-channel OTFTs are small they are difficult to measure. There are no such measurements available and therefore, the short-channel capacitance model was only verified by means of a TCAD simulation. A further verification based on measurements is desirable.

- The short-channel capacitance model explicitly needs the frequency of an applied signal as a parameter. Therefore, it is not suitable for the implementation into a circuit simulator such as Cadence Virtuoso where the AC frequency is applied during a sweep.

- The noise model could only be verified on a small data basis. Retrieving good results from a noise analysis is a complicated task and thus the noise model should be verified in the future by means of further measurements.

- The definition of fitting parameters is inevitable for a correct reproduction of measured or simulated results. However, some fitting parameters used in the model are not based on the device physics and rather play the role of empirical fitting parameters. The model could be improved by formulating different equations that are even more dependent on the device physics.

- The influence of the temperature on the device behavior was only investigated with special focus on the basic DC model. An investigation of the influence of the temperature on the dynamic behavior of the transistors should be performed in the future.

Despite the open points, it can be concluded that the compact model developed in this work provides a comprehensive description of OTFTs that is able to capture many effects. A good agreement with respect to different scenarios (e.g. capacitance measurements, admittance measurements of long-channel transistors, simulations of simple circuits, high-frequency measurements of short-channel transistors) is achievable with only a small number of fitting parameters.

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APPENDIX A

Equation package

The solution of the three charge integrals in Eqs. (4.1), (4.2), and (4.3) is:

$$Q_{\mathrm{c}} = -\frac{W_{\mathrm{ch,G}} \cdot W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{I_{\mathrm{ds}}} \left(\frac{Q'^3_{\mathrm{md}}}{3C'_{\mathrm{diel}}} - \frac{Q'^3_{\mathrm{ms}}}{3C'_{\mathrm{diel}}} + \frac{Q'^2_{\mathrm{md}} V_{\mathrm{th}} \tilde{\alpha}}{2} - \frac{Q'^2_{\mathrm{ms}} V_{\mathrm{th}} \tilde{\alpha}}{2} \right). \tag{A.1}$$

$$\begin{aligned} Q_{\mathrm{d}} = &-\frac{W_{\mathrm{ch,G}} \cdot W^2_{\mathrm{ch,eff}} \cdot \mu^2_{\mathrm{eff}}}{I^2_{\mathrm{ds}} \cdot L_{\mathrm{ch}}} \left(\frac{Q'^3_{\mathrm{md}} Q'^2_{\mathrm{ms}}}{6C'^2_{\mathrm{diel}}} - \frac{Q'^5_{\mathrm{ms}}}{15C'^2_{\mathrm{diel}}} - \frac{Q'^5_{\mathrm{md}}}{10C'^2_{\mathrm{diel}}} - \frac{Q'^3_{\mathrm{md}} V^2_{\mathrm{th}} \tilde{\alpha}^2}{3} - \frac{Q'^3_{\mathrm{ms}} V^2_{\mathrm{th}} \tilde{\alpha}^2}{6} \right. \\ &\left. - \frac{3Q'^4_{\mathrm{md}} V_{\mathrm{th}} \tilde{\alpha}}{8C'_{\mathrm{diel}}} - \frac{5Q'^4_{\mathrm{ms}} V_{\mathrm{th}} \tilde{\alpha}}{24C'_{\mathrm{diel}}} + \frac{Q'^2_{\mathrm{md}} Q'_{\mathrm{ms}} V^2_{\mathrm{th}} \tilde{\alpha}^2}{2} + \frac{Q'^2_{\mathrm{md}} Q'^2_{\mathrm{ms}} V_{\mathrm{th}} \tilde{\alpha}}{4C'_{\mathrm{diel}}} + \frac{Q'^3_{\mathrm{md}} Q'_{\mathrm{ms}} V_{\mathrm{th}} \tilde{\alpha}}{3C'_{\mathrm{diel}}} \right). \end{aligned} \tag{A.2}$$

$$\begin{aligned} Q_{\mathrm{s}} = &-\frac{W_{\mathrm{ch,G}} \cdot W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}} \cdot}{I_{\mathrm{ds}}} \left[\frac{W_{\mathrm{ch,eff}} \cdot \mu_{\mathrm{eff}}}{L_{\mathrm{ch}} \cdot I_{\mathrm{ds}}} \cdot \left(\frac{Q'^5_{\mathrm{md}}}{10C'^2_{\mathrm{diel}}} + \frac{Q'^5_{\mathrm{ms}}}{15C'^2_{\mathrm{diel}}} - \frac{Q'^3_{\mathrm{md}} Q'^2_{\mathrm{ms}}}{6C'^2_{\mathrm{diel}}} \right. \right. \\ &+ \frac{Q'^3_{\mathrm{md}} V^2_{\mathrm{th}} \tilde{\alpha}^2}{3} + \frac{Q'^3_{\mathrm{ms}} V^2_{\mathrm{th}} \tilde{\alpha}^2}{6} + \frac{3Q'^4_{\mathrm{md}} V_{\mathrm{th}} \tilde{\alpha}}{8C'_{\mathrm{diel}}} + \frac{5Q'^4_{\mathrm{ms}} V_{\mathrm{th}} \tilde{\alpha}}{24C'_{\mathrm{diel}}} - \frac{Q'^2_{\mathrm{md}} Q'_{\mathrm{ms}} V^2_{\mathrm{th}} \tilde{\alpha}^2}{2} \\ &\left. \left. - \frac{Q'^2_{\mathrm{md}} Q'^2_{\mathrm{ms}} V_{\mathrm{th}} \tilde{\alpha}}{4C'_{\mathrm{diel}}} - \frac{Q'^3_{\mathrm{md}} Q'_{\mathrm{ms}} V_{\mathrm{th}} \tilde{\alpha}}{3C'_{\mathrm{diel}}} \right) + \frac{Q'^2_{\mathrm{md}} \tilde{\alpha} V_{\mathrm{th}}}{2} + \frac{Q'^3_{\mathrm{md}}}{3C'_{\mathrm{diel}}} - \frac{Q'^2_{\mathrm{ms}} \tilde{\alpha} V_{\mathrm{th}}}{2} - \frac{Q'^3_{\mathrm{ms}}}{3C'_{\mathrm{diel}}} \right] \end{aligned} \tag{A.3}$$

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The solution of the charge integrals (Eqs. (7.27) and (7.28)) incorporating the new partitioning scheme is as follows:

$$\begin{aligned} Q_\mathrm{d} = -\frac{W_\mathrm{ch,G}\cdot W_\mathrm{ch,eff}\cdot\mu_\mathrm{eff}}{I_\mathrm{ds}}\Bigg[&\frac{(1-\nu)\cdot W_\mathrm{ch,eff}\cdot\mu_\mathrm{eff}}{L_\mathrm{ch}\cdot I_\mathrm{ds}}\cdot\Bigg(\frac{Q'^3_\mathrm{md}Q'^2_\mathrm{ms}}{6C'^2_\mathrm{diel}}-\frac{Q'^5_\mathrm{ms}}{15C'^2_\mathrm{diel}}-\frac{Q'^5_\mathrm{md}}{10C'^2_\mathrm{diel}} \\ &-\frac{Q'^3_\mathrm{md}V^2_\mathrm{th}\tilde{\alpha}^2}{3}-\frac{Q'^3_\mathrm{ms}V^2_\mathrm{th}\tilde{\alpha}^2}{6}-\frac{3Q'^4_\mathrm{md}V_\mathrm{th}\tilde{\alpha}}{8C'_\mathrm{diel}}-\frac{5Q'^4_\mathrm{ms}V_\mathrm{th}\tilde{\alpha}}{24C'_\mathrm{diel}}+\frac{Q'^2_\mathrm{md}Q'_\mathrm{ms}V^2_\mathrm{th}\tilde{\alpha}^2}{2} \\ &+\frac{Q'^2_\mathrm{md}Q'^2_\mathrm{ms}V_\mathrm{th}\tilde{\alpha}}{4C'_\mathrm{diel}}+\frac{Q'^3_\mathrm{md}Q'_\mathrm{ms}V_\mathrm{th}\tilde{\alpha}}{3C'_\mathrm{diel}}\Bigg)+\frac{\nu Q'^2_\mathrm{md}\tilde{\alpha}V_\mathrm{th}}{2}+\frac{\nu Q'^3_\mathrm{md}}{3C'_\mathrm{diel}}-\frac{\nu Q'^2_\mathrm{ms}\tilde{\alpha}V_\mathrm{th}}{2}-\frac{\nu Q'^3_\mathrm{ms}}{3C'_\mathrm{diel}}\Bigg] \end{aligned} \tag{A.4}$$

$$\begin{aligned} Q_\mathrm{s} = -\frac{W_\mathrm{ch,G}\cdot W_\mathrm{ch,eff}\cdot\mu_\mathrm{eff}\cdot(1-\nu)}{I_\mathrm{ds}}\Bigg[&\frac{W_\mathrm{ch,eff}\cdot\mu_\mathrm{eff}}{L_\mathrm{ch}\cdot I_\mathrm{ds}}\cdot\Bigg(\frac{Q'^5_\mathrm{md}}{10C'^2_\mathrm{diel}}+\frac{Q'^5_\mathrm{ms}}{15C'^2_\mathrm{diel}}-\frac{Q'^3_\mathrm{md}Q'^2_\mathrm{ms}}{6C'^2_\mathrm{diel}} \\ &+\frac{Q'^3_\mathrm{md}V^2_\mathrm{th}\tilde{\alpha}^2}{3}+\frac{Q'^3_\mathrm{ms}V^2_\mathrm{th}\tilde{\alpha}^2}{6}+\frac{3Q'^4_\mathrm{md}V_\mathrm{th}\tilde{\alpha}}{8C'_\mathrm{diel}}+\frac{5Q'^4_\mathrm{ms}V_\mathrm{th}\tilde{\alpha}}{24C'_\mathrm{diel}}-\frac{Q'^2_\mathrm{md}Q'_\mathrm{ms}V^2_\mathrm{th}\tilde{\alpha}^2}{2} \\ &-\frac{Q'^2_\mathrm{md}Q'^2_\mathrm{ms}V_\mathrm{th}\tilde{\alpha}}{4C'_\mathrm{diel}}-\frac{Q'^3_\mathrm{md}Q'_\mathrm{ms}V_\mathrm{th}\tilde{\alpha}}{3C'_\mathrm{diel}}\Bigg)+\frac{Q'^2_\mathrm{md}\tilde{\alpha}V_\mathrm{th}}{2}+\frac{Q'^3_\mathrm{md}}{3C'_\mathrm{diel}}-\frac{Q'^2_\mathrm{ms}\tilde{\alpha}V_\mathrm{th}}{2}-\frac{Q'^3_\mathrm{ms}}{3C'_\mathrm{diel}}\Bigg] \end{aligned} \tag{A.5}$$

APPENDIX B

Additions to the Small-Signal Analysis

B.1 Literature Summary of High-Frequency Organic TFTs

In Tab. B.1, a literature summary of organic TFTs with a measured unity-current-gain transit frequency of at least 3.5 MHz is shown.

Table B.1.: Literature summary of organic TFTs with a measured transit frequency of at least 3.5 MHz. This table was published in ref. [55].

ref.	f_T [MHz]	μ_{eff} [cm^2/(Vs)]	V_{gs} [V]	V_{T0} [V]	L_{ch} [µm]	$L_{ov,GS}$ [µm]	$L_{ov,GD}$ [µm]	C'_{diel} [nF/cm^2]	comment
[130]	160	0.62	40	0	1.2	0.21	0.13	8.54	n-chan.
[59]	45	1.9	-7	1	1.5	1	1	130	p-chan.
[131]	40	n/a	8.6	n/a	0.2	n/a	n/a	n/a	vertical OPBT
[132]	38	4.2	-15	-3	1.5	2	2	36	p-chan.
[88]	27.7	2.22	20	9	2	2.5	2.5	29	n-chan.
[89]	24	2	-15	0	1.4	2.7	2.7	8	p-chan.
[89]	22	1.58	-12	0	1.2	2.3	2.3	8	p-chan.
[43]	21	2.7	-3	-1	0.6	1.7	8.3	700	p-chan.
[133]	20	1.11	20	8.6	2	1	1	20	n-chan.
[134]	20	0.4	-20	0	2.5	0.5	0.5	24	p-chan.
[135]	20	0.44	-15	0	0.8	n/a	n/a	23	vertical transist.
[108]	20	0.82	30	0	1.75	3	3	6	n-chan.
[13]	20	2.7	-10	-5	3	2.25	2.25	80	p-chan.
[136]	19	2.5	-10	0	2	1	3	77	p-chan.
[107]	19	1	12	1	1.2	2.3	2.3	27	n-chan.
[137]	14.4	0.3	7	0.5	1	1.7	1.7	39	n-chan.
[88]	11.4	0.73	-20	-4	2	2.5	2.5	20	p-chan.
[138]	10.4	2.2	-3	-0.7	0.85	5	5	700	p-chan.
[139]	9.7	n/a	-8.2	-3	0.4	n/a	n/a	50	vertical transis.
[140]	6.7	2	-3	-1.2	0.6	5	5	700	p-chan.
[141]	4.9	0.11	30	5	1.8	3	3	10	n-chan.
[142]	4.3	0.58	20	5	6	4.5	4.5	27.5	n-chan.
[116]	4.1	0.5	-3	-1.2	1	1	9	700	p-chan.
[42]	3.7	0.5	-3	-1.2	0.6	5	5	700	p-chan.

B.2 TLM Measurements

In this section, some background information about the transmission-line-measurement (TLM) analysis of the staggered transistors presented in Sec. 7.4 is given. A transistor can be regarded as the sum of a channel-length independent, Ohmic contact resistance (R_C), and an intrinsic transistor comprising a channel resistance [17]. If transistors with different channel lengths but otherwise equal geometry parameters and materials are fabricated, the channel resistance can be separated from the contact resistance. In Fig. B.1, the total width-normalized resistance of the transmission lines consisting of the contact resistance and the intrinsic transistor are depicted for different gate-overdrive voltages. The gate-overdrive voltage is defined as $V_{gs} - V_{T0}$. The resistance RW is calculated by I_{ds}/V_{ds}. The linear functions are regression functions. If the linear regression functions are extrapolated to a channel length of 0 µm, the result is the contact resistance since then, the transmission line does not contain any intrinsic channel. In Fig. B.2, the resulting width-normalized contact resistance $R_C W$ is plotted versus the gate-overdrive voltage. Based on the contact resistance and by assuming the standard MOSFET equation for the linear regime of operation, the mobility of the intrinsic carrier-channel can be extracted. This is shown in Fig. B.3 where the mobility is plotted versus the gate-overdrive voltage.

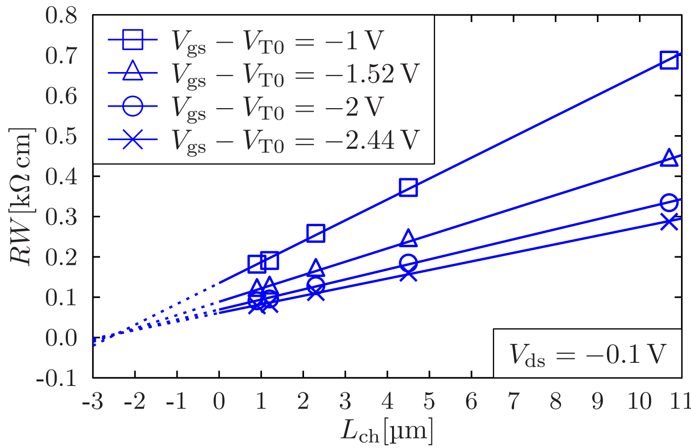

Figure B.1.: Measured width-normalized resistance of the transmission line consisting of a transistor and a contact resistance at different gate-overdrive voltages and at a fixed V_{ds} of −0.1 V. The resistance is plotted versus the channel length. This picture was published in ref. [55].

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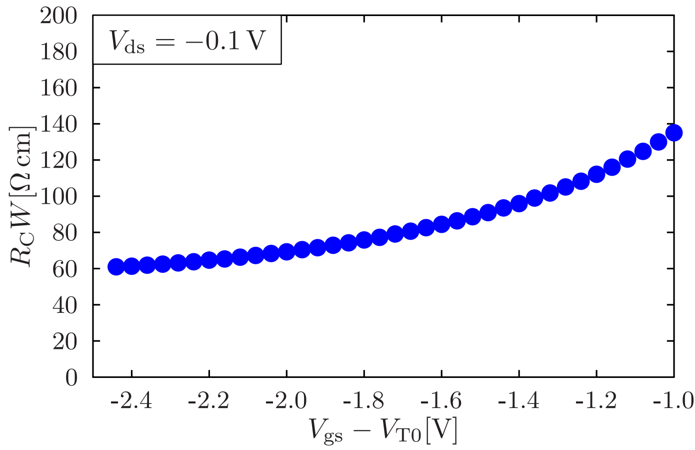

Figure B.2.: Extracted width-normalized contact resistance of the transmission line consisting of a transistor and a contact resistance at different gate-overdrive voltages and at a fixed V_{ds} of -0.1 V. This is a result of the extrapolated regression functions shown in Fig. B.1. The contact resistance is plotted versus the channel length. This picture was published in ref. [55].

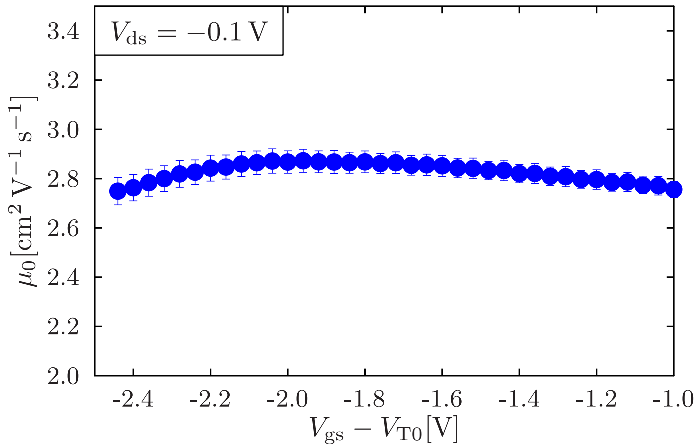

Figure B.3.: Extracted mobility of the transmission line at different gate-overdrive voltages and at a fixed V_{ds} of -0.1 V. The mobility is plotted versus the channel length. This picture was published in ref. [55].

B.3 Fitting Parameters of the Transistors

In this section, the fitting parameters of the transistors verified in Sec. 7.4 are shown. All transistors are fitted by a shared basic parameter set that is equal for all transistors of one technology. These parameters are depicted in Tab. B.2 for the staggered (TC) and coplanar (BC) transistors. Afterwards, the single transistors of each technology are fitted to the measured DC transfer and output characteristics and to the measured small-signal gain h_{21} by a subset of variable parameters. In Tab. B.3, the parameters used for the staggered (TC) transistors are shown and in Tab. B.4, the specific fitting parameters used for the coplanar (BC) transistors are shown. It shall be emphasized that the coplanar transistor with $L_{\mathrm{ov,GS}} = 6.5\,\mu\mathrm{m}$ is an outlier for which a much lower low-field mobility of $\kappa = 0.7\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ has been assumed. The channel lengths of the transistors were measured but in a range of $\mp 50\,\mathrm{nm}$ they are regarded as fitting parameters for the compact model. For the fitting of the non-linear injection model [47], in principle, the initial height of the Schottky barrier (Φ_{B0}) as defined in Fig. 2.3 is needed. This Schottky barrier is defined by the band diagram of the transistor. However, the exact work functions of the materials at the junctions are not known and an exact determination of Φ_{B0} is not essential for the correct reproduction of measured DC curves. Therefore, Φ_{B0} is also regarded as a fitting parameter. Since no quasistatic capacitance measurements are available the short-channel capacitance fitting parameters K_{fit} and K_{r} cannot be determined for each transistors. Rather, the values of these two parameters are treated as fitting parameters in order to provide a good fitting of the measured small-signal gain h_{21}. For the staggered transistors, a transfer length of $L_{\mathrm{T}} = 1.16\,\mu\mathrm{m}$ and a sheet resistance of $R_{\mathrm{sheet}} = 5800\,\Omega$ is used.

Table B.2.: Basic fitting parameters for staggered (TC) and coplanar (BC). This table was published in ref. [55].

Parameter	Staggered	Coplanar
$C'_{\mathsf{diel}}\,[\mathrm{nF\,cm^{-2}}]$	500	500
$\kappa[\mathsf{cm^2V^{-\beta-1}s^{-1}}]$	1.1	2.1
$\beta[-]$	0.4	0.5
$\lambda[\mathrm{V^{-1}}]$	0.07	0.07
$N_{\mathsf{fing}}\,[-]$	4	4
$W_{\mathsf{contact}}\,[\mathrm{\mu m}]$	25	25
$d_{\mathsf{fing}}\,[\mathrm{\mu m}]$	20	20
$w_{\mathsf{ovl}}\,[\mathrm{\mu m}]$	30	30
$\Phi_{\mathsf{B0}}\,[\mathrm{eV}]$	0.4	0.4
$\eta[-]$	0.9855	1.3047
$\theta[-]$	1.7	1
$d_{\mathsf{m}}\,[\mathrm{nm}]$	-	5
$d_{\mathsf{B}}\,[\mathrm{nm}]$	-	3.2187
$w_{\mathsf{sat}}\,[-]$	0.63	1.3
$C_{\mathsf{scale,high}}\,[-]$	0	0
$C_{\mathsf{scale,low}}\,[-]$	1	1
$p_{\mathsf{scale}}\,[-]$	1	50
$\tau_{\mathsf{scale}}\,[\mathrm{s}]$	0.4×10^{-7}	variable
$C_{\mathsf{scale2,high}}\,[-]$	0	0
$C_{\mathsf{scale2,low}}\,[-]$	1	1
$p_{\mathsf{scale2}}\,[-]$	2.5	2.5
$\tau_{\mathsf{scale2}}\,[\mathrm{s}]$	variable	0.5×10^{-7}
$K_{\mathsf{fit}}\,[-]$	0.9	1
$K_{\mathsf{r}}\,[-]$	variable	0

Table B.3.: Specific fitting parameters for the staggered (TC) transistors along with the measured gate-to-contact overlap lengths. This table was published in ref. [55].

$L_{\mathrm{ov,GS}}$	$L_{\mathrm{ov,GD}}$	L_{ch}	S_{obs}	V_{T0}	δ_{fit}	K_{r}	τ_{scale2}
[µm]	[µm]	[µm]	[mV/dec]	[V]	[−]	[−]	[s]
9.2	1.4	0.69	250	-0.87	0.6	0.07	$0.04 \cdot 10^{-7}$
8.4	2.4	0.67	240	-0.87	0.6	0.07	$0.063 \cdot 10^{-7}$
7.4	3.4	0.67	240	-0.88	0.6	0.15	$0.08 \cdot 10^{-7}$
6.4	4.2	0.66	230	-0.9	0.6	0.27	$0.12 \cdot 10^{-7}$
5.4	5.2	0.67	230	-0.92	0.6	0.44	$0.17 \cdot 10^{-7}$
4.5	6.0	0.66	230	-0.92	0.6	0.55	$0.2 \cdot 10^{-7}$
3.5	7.0	0.66	230	-0.93	0.6	0.7	$0.25 \cdot 10^{-7}$
1.9	8.5	0.67	230	-1	0.36	0.95	$0.3 \cdot 10^{-7}$
0.9	9.6	0.68	230	-1	0.26	0.95	$0.45 \cdot 10^{-7}$

Table B.4.: Specific fitting parameters for the coplanar (BC) transistors along with the measured gate-to-contact overlap lengths. This table was published in ref. [55].

$L_{\mathrm{ov,GS}}$	$L_{\mathrm{ov,GD}}$	L_{ch}	S_{obs}	V_{T0}	R_{contact}	δ_{fit}	τ_{scale}
[µm]	[µm]	[µm]	[mV/dec]	[V]	[Ω]	[−]	[s]
9.4	0.8	0.67	72	-0.69	630	0.65	$0.037 \cdot 10^{-7}$
8.4	1.9	0.64	71	-0.7	540	0.65	$0.04 \cdot 10^{-7}$
7.4	3.0	0.66	70	-0.7	580	0.65	$0.045 \cdot 10^{-7}$
6.5	4.0	0.66	80	-0.67	560	0.65	$0.032 \cdot 10^{-7}$
5.8	4.7	0.66	71	-0.7	640	0.65	$0.055 \cdot 10^{-7}$
4.8	5.7	0.66	71	-0.71	590	0.65	$0.06 \cdot 10^{-7}$
3.6	6.8	0.69	72	-0.7	730	0.45	$0.11 \cdot 10^{-7}$
2.8	7.6	0.63	71	-0.69	530	0.45	$0.11 \cdot 10^{-7}$
1.7	8.6	0.63	71	-0.69	470	0.45	$0.1 \cdot 10^{-7}$
0.8	9.7	0.66	71	-0.68	500	0.3	$0.27 \cdot 10^{-7}$

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