Universitat Politècnica de Catalunya

Departament d'Enginyeria Elèctrica

PhD Thesis

Advance Control of Multilevel Converters for Integration of Distributed Generation Resources into AC Grid

Autor: **Edris Pouresmaeil**

Directors: **Dr. Daniel Montesinos i Miracle**
Dr. Oriol Gomis i Bellmunt

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Universitat Politècnica de Catalunya
Departament d'Enginyeria Elèctrica
Centre d'Innovació Tecnològica en Convertidors Estàtics i Accionaments
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Abstract

Distributed generation (DG) with a converter interface to the power grid is found in many of the green power resources applications. This dissertation describes a multi-objective control technique of voltage source converter (VSC) based on multilevel converter topologies, for integration of DG resources based on renewable energy (and non-renewable energy)to the power grid.

The aims have been set to maintain a stable operation of the power grid, in case of different types of grid-connected loads. The proposed method provides compensation for active, reactive, and harmonic load current components. A proportional-integral (PI) control law is derived through linearization of the inherently non-linear DG system model, so that the tasks of current control dynamics and dc capacitor voltage dynamics become decoupled. This decoupling allows us to control the DG output currents and the dc bus voltage independently of each other, thereby providing either one of these decoupled subsystems a dynamic response that significantly slower than that of the other. To overcome the drawbacks of the conventional method, a computational control delay compensation method, which delaylessly and accurately generates the DG reference currents, is proposed. The first step is to extract the DG reference currents from the sensed load currents by applying the stationary reference frame and then transferred into synchronous reference frame method, and then, the reference currents are modified, so that the delay will be compensated.

The transformed variables are used in control of the multilevel voltage source converter as the heart of the interfacing system between DG resources and power grid. By setting appropriate compensation current references from the sensed load currents in control circuit loop of DG link, the active, reactive, and harmonic load current components will be compensated with fast dynamic response, thereby achieving sinusoidal grid currents in phase with load voltages while required power of loads is more than the maximum injected power of the DG resources. The converter, which is controlled by the described control strategy, guarantees maximum injection of active power to the grid continuously, unity displacement power factor of power grid, and reduced harmonic load currents in the common coupling point. In addition, high current overshoot does not exist during connection of DG link to the power grid, and the proposed integration strategy is insensitive to grid overload.

Resum

La Generació Distribuïda (DG) injectada a la xarxa amb un convertidor estàtic és una solució molt freqüent en l'ús de molts dels recursos renovables. Aquesta tesis descriu una técnica de control multi-objectiu del convertidor en font de tensió (VSC), basat en les topologies de convertidor multinivell, per a la integració de les fonts distribuïdes basades en energies renovables i també de no renovables. Els objectius fixats van encaminats a mantenir un funcionament estable de la xarxa eléctrica en el cas de la connexió de diferents tipus de càrregues. El mètode de control proposat ofereix la possibilitat de compensació de les components actives i reactives de la potencia, i les components harmòniques del corrent consumit per les càrregues. La llei de control proporcional-Integral (PI) s'obté de la linearització del model inherentment no lineal del sistema, de forma que el problema de control del corrent injectat i de la tensió d'entrada del convertidor queden desacoblats. Aquest desacoblament permet el control dels corrents de sortida i la tensió del bus de forma independent, però amb un d'ells amb una dinàmica inferior. Per superar els inconvenients del mètode convencional, s'usa un retard computacional, que genera les senyals de referència de forma acurada i sense retard. El primer pas es calcular els corrents de referència a partir de les mesures de corrent. Aquest càlcul es fa primer transformant les mesures a la referència estacionaria per després transformar aquests valors a la referència síncrona. En aquest punt es on es poden compensar els retards. Les variables transformades son usades en els llacos de control del convertidor multinivell. Mitjancant aquests llacos de control i les referències adequades, el convertidor és capac de compensar la potencia activa, reactiva i els corrents harmònics de la càrrega amb una elevada resposta dinàmica, obtenint uns corrents de la xarxa de forma completament sinusoïdal, i en fase amb les tensions. El convertidor, controlat amb el mètode descrit, garanteix la màxima injecció de la potencia activa, la injecció de la potencia reactiva per compensar el factor de potencia de la càrrega, i la reducció de les components harmòniques dels corrents consumits per la còrrega. A més, garanteix una connexió suau entre la font d'energia i la xarxa. El sistema proposat es insensible en front de la sobrecarrega de la xarxa.

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Nomenclature

Roman symbols

$\overrightarrow{m}$	Reference vector
$\overrightarrow{p_i}$	Projection from reference vector
d_i	Duty cycle
D_{ni}	Switching state function
E_L	line-to-line RMS voltage of grid
f	Fundamental frequency
f_c	Filter cut-off frequency
i_{ci}	DG Current
i_{dc}	dc side current
i_{lk}	Load current
i_{sk}	Grid current
k_1	Proportional gain
k_2	Integral gain
k_i	Integral gain
k_p	Proportional gain
L_c	Equivalent inductance of the ac filter, coupling transformer, and connection cables
l_i	Length of the vectors
L_l	Load inductance
L_s	Grid inductance up to the PCC

m	Modulation index
p_{ac}	Power of ac side
p_{dc}	Power of dc side
P_l	Load active power
P_{ref}	Reference power of DG
Q_l	Load reactive power
R_c	Equivalent resistance of the ac filter, coupling transformer, and connection cables
R_l	Grid resistance up to the PCC
R_s	Load resistance
S_{ci3L}	Switching matrix of NPC converter
S_{ci}	Switching matrix
S_l	Load power
$T_{0dq}^{\alpha\beta}$	Clarke to Park transformation matrix
$T_{0\alpha\beta}^{abc}$	Clarke variable transformation matrix
T_{0dq}^{abc}	Park variable transformation matrix
T_i	Switching time
T_m	Modulation period
v_{c3L}	Voltage of cascaded capacitors in NPC converter
v_{dc}	dc side voltage
v_{iM}	Voltage between converter terminals and dc bus neutral
v_k	Load voltage
v_{NM}	Neutral point voltage
v_{sk}	Grid voltage

a	$e^{j\frac{2\pi}{3}}$ complex rotation operator

Greek symbols

α	Clarke horizontal axis
β	Clarke vertical axis
ω	Grid voltage angular speed
ω_n	Natural un-damped angular frequency
ω_p	Angular frequency of modulation carrier wave
τ	Parameter of function F
θ	Instantaneous angle of voltages
ζ	Damping factor

Superscripts

$\alpha\beta 0$	Vector of $\alpha\beta$ components
’	Equivalent element in other side
*	Reference value
abc	Vector of abc components
dq0	Vector of dq components
j	Complex value
ss	Steady state value

Acronyms

BESS	Batteries Energy Storage System
CHB	Cascaded H-Bridge
CHP	Combined Heat and Power
CITCEA	Centre d’Innovació Tecnològica en Convertidors Estàtics i Accionaments

DG Distributed Generation

DPGR Distributed Power Generation Resources

DSP Digital Signal Processor

EMC Electro-Magnetic Compatibility

EMF Electromotive Force

EMI Electromagnetic Interface

EPROM Erasable Programmable Read Only Memory

ESL Equivalent Series Inductance

ESR Equivalent Series Resistance

FC Flying Capacitor

FC Fuel Cell

FPGA Field Programmable Gate Array

HPF High Pass Filter

HVDC High Voltage Direct Current

IGBT Isolated Gate Bipolar Transistor

LPF Low Pass Filter

MPHPF Minimal Phase High Pass Filter

NP Neutral Point

NPC Neutral Point Clamped

PCC Point of Common Coupling

PF Power factor

PI Proportional Integral

PLL Phase Locked Loop

PR Proportional Resonant

PV Photovoltaic

PWM Pulse Width Modulation

SDCS Separate DC Source

SHE Selective Harmonic Elimination

SMES Superconducting Magnetic Energy Storage

SVC Static Var Compensation

SVM Space Vector Modulation

SVPWM Space Vector Pulse Width Modulation

THD Total Harmonic Distortion

UPC Universitat Politècnica de Catalunya

VSC Voltage Source Converter

ZOH Zero Order Hold

Chapter 1

Introduction

1.1 Background

The term Distributed Generation (DG) refers to any electric power generation technology that is on-site or close to the load center and is integrated to the utility power grid. Distributed Power Generation Resources (DPGR) based on renewable energy like wind power, photovoltaic (PV), and hydro turbines are seen as a reliable alternative to the traditional energy resources based on fossil fuel sources such as oil, natural gas, or coal. The electricity business restructuring and necessity of producing more electrical energy [1, 2], combined with the environmental regulations due to green house gas emission [3], and the recent improvement in small scale resources of electrical power generation are the main factors driving the energy sector into a new era of power generation, where large portions of increases in electrical energy demand will be met through widespread installation of distributed power generation resources or what's known as distributed generation resources [4, 5, 6, 7, 8].

DG technology has the potential of being less costly, more efficient, more reliable, and facilitates the generation of electrical energy in proximity of load centers. Therefore, DG technology can give industrial consumers various options in a wider range of high reliability and low price combinations [9]. This type of clean, reliable and on-site power generation technique is based on technologies such as turbines and engines powered by natural gas, biogas, propane, wind, and small-scale hydropower resources as well as hydrogen-powered fuel cells and photovoltaic panels.

Rural and household consumers are the cases which are mostly concerned with the improvement of DG technology because of the overwhelming investments required to connect to a distant electrical network. For these consumers, use of DG system especially based on renewable energy resources (even the non-renewable energy resources) is more economical and efficient than the central power station system plus associated transmission and dis-

tribution line expansion. On the other hand, because of high reliability and low cost effectiveness of DG system, many industrial companies, and commercial consumers may decide to install DG system as a match with the electric main source for their electrical consumptions. This can happen when the particular application is of very low reliability and low cost or very high reliability and high cost [5]. Moreover, DG system could appear as an independent power system, which meets both the local loads and main grid requirements, such as injection of active power into the utility grid, compensation of higher harmonic components and reactive power of grid-connected non-linear loads, power factor correction of main grid, backup generation during overload condition, compensation of power quality events during disturbances, peak shaving, and voltage reliability enhancement, in a right way that is not possible with centralized generation [10].

Normally, environmental-friendly sources of energy, such as wind and solar are commonly used as a source of energy to empower the DG systems. These resources of energy meet both the increasing demand of electric power from consumer side and environmental regulations. In addition, synchronous generators empowered by diesel engines or gas-fired can be used in DG systems for power generation. But, the application of the DG technology in electrical network is principally dependent on whether the interfacing scheme is based on the direct coupling of rotary machines, such as asynchronous and synchronous generators, or whether the DG system is interfaced by a converter based on power electronic devices. Unlike large scale generators, which are almost entirely based on 50 or 60 Hz synchronous machines, DG system include high speed or frequency energy resources such as micro-turbines, variable speed or frequency energy resources such as wind energy, and direct energy conversion resources which producing dc voltages or currents directly, such as photovoltaic and fuel cells energy resources.

Most of DG resources are interfaced to the electrical power grid or local loads by using of dc-ac Pulse Width Modulated (PWM) current controlled Voltage Source Converter (VSC), for its fast dynamic response, accurate performance, ease of implementation and its inherent closed loop control for the current to guarantee the required operating point [10]. Power electronics are a crucial enabling technology which facilitates interfacing of different sizes of DG units, ranging from few kW up to 1.6 MW [11, 12]. In addition, modular construction of interfaced converters can increase the power capacity; for example a 50 MW high voltage dc (HVDC) light system, based on insulated gate bipolar transistors (IGBT), has been commissioned in 1999 [13].

Generally, power electronic converter interfaces make the DG resources

more flexible in their control and operation in comparison with the conventional induction and synchronous generators. These interfacing systems introduce new issues, such as the limited overload capability, switching loses and harmonics generation, absence of the physical inertia, susceptibility to parameters variation, and wide-band of dynamics. It should be noted that, when DG is installed in a weak or micro-grid network, a converter-based DG system will be subjected to considerable grid disturbances and parameter fluctuations caused by the unexpected nature of the power grid. These disturbances remarkably challenge the stability and control effectiveness of a converter-based generator in DG system [14].

1.2 The Main Purposes of DG Technology

As mentioned in previous section, DG technology considered as a flexible alternative in electrical power system and consumers, especially in many industrial companies and commercial centers during recent years. Several potential applications and purposes of DG technology in electrical network and their consumers are discussed in the following sub-sections.

1.2.1 Continuous Power Source

The DG system can be used for a long time to generate electrical energy for consumers on a relatively continuous basis. By considering this capability of DG system, it can be utilized most often in a continuous power capacity for industrial and commercial applications and supply the sensitive loads because of high reliability.

1.2.2 Security

This includes issues of the system reliability and power quality factor. For this case, DG technology can be used to generate electrical energy at a higher level of reliability and power quality than typically available from the utility grid. When one on-site generator fails, the spare capacity in the remaining system resources can provide instantaneous reserve power which typically known as spinning reserve. Even if the primary generator fails, critical loads can be supported from on-site generators or overall system capacity. DG system support power quality by preventing system wide problems and mitigating grid problems before a grid-connected load detects them.

1.2.3 High Efficiency and Low Cost

Normally, main grid source has developed energy-efficient technologies such as natural gas combined-cycle systems. Therefore, these technologies require continuous, reliable, and low-cost access to a natural gas fuel source and are unsuited for small-scale deployment. As mentioned in previous section, normally renewable energy resources with high efficiencies are used in DG system. Renewable energy technologies use fundamentally local energy supplies, and some non-renewable based DG technologies use easily transported fuels other than natural gas. Other resources of energies such as energy storage, co-generation, and demand-control devices help improve the efficiency of whatever source of generation is being used. Therefore, increased energy efficiency decreases both energy costs and greenhouse gas emissions per unit of power generation.

1.2.4 Low Emissions

It is completely clear that, DG system based on renewable energy resources is inherently greenhouse gas emissions free. However, some developed DG technologies can also reduce emissions of conventional fuels which are based on fossil fuels. DG system performs this through increased efficiency and alternative energy conversion processes, such as found in a fuel cell, CO sequestration reform, and production of gas. This application can be used by energy companies to supply customers who want to purchase power generated with low emissions.

1.2.5 Combined Heat and Power (CHP)

To reduce energy losses, it is necessary to increase the fuel-to-electricity efficiency of the generation plant or to use the waste heat during power generation and transmission. The use of waste heat in DG close to the user increases further the overall efficiency for water heating, space heating, steam generation or other thermal needs. The ability to avoid transmission losses and make effective use of waste heat makes on-site co-generation or combined heat and power (CHP) systems 70 to 80 percent efficient. CHP is most commonly used by industry customers, with a small portion of overall installations in the commercial sector.

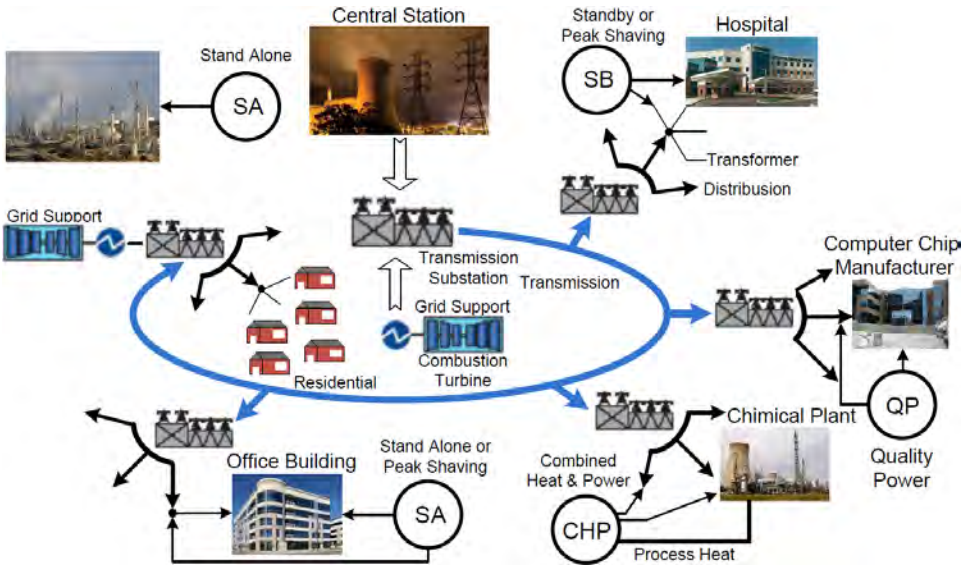


Figure 1.1: Summary of DG applications in electrical networks

1.2.6 Load Management

One of the main objectives of DG operation in this case is to reduce overall electricity costs. DG units can be applied to reduce the main utility's demand charges, to defer buying electricity during high-price periods, or to allow for lower rates from power providers by smoothing site demand. This technique can improve system efficiency with on-site DG and economic efficiency through demand-side management. This type of application can be offered by energy generation companies to clients who want to reduce the cost of buying electricity during high-price periods.

1.2.7 Transmission and Distribution Deferral

As mentioned in first section, installing DG units in rural and strategic locations which are far from the electrical network can help delay the purchase of new and separate distribution or transmission line. A detailed analysis of the life-cycle costs of the various alternatives is critical and issues relating to equipment deferrals must also be examined closely.

Figure 1.1 briefly summarizes the different types of DG applications in electrical network.

1.3 Technical Challenges of Converter-Based DG Interface

Increasing the number of DG units in electrical networks requires new techniques for the operation and management of the power networks in order to maintain or even to improve the power supply reliability and quality in future. In addition, the dynamic and unpredicted nature of a power grid challenges the reliability, stability and control of the DG interface system. The fact that a typical power grid is faced with inevitable disturbances and uncertainties complicates the design of a practical converter-based DG interface. Most of unpredictable disturbances in an electrical network are related to the utility grid due to the relatively small size of DG energy resources. Several different types of grid disturbances can be imposed on a converter-based DG interface system. Different problems occur in the following ways [14, 15]:

1. According to the grid configuration, a large set of grid impedance value is yielded as DG system is commonly installed in weak grids with long radial distribution feeders. Furthermore, effects of temperature, saturation and cable overload are all the most important reasons for possible fluctuations in the interfacing impedance seen by the interfaced converter. The stability of the inner control circuit loops of the converter-based DG interface, directly affected by variation in interfacing impedance. Also, the grid impedance interaction with the ac-side filter of the interfaced converter might excite high-frequency resonance dynamics. In this case, the injected currents from converter will be highly distorted and it can propagate through the system and drive other voltage and current harmonics [16].

2. There is a high trend toward the use of current control technique for PWM converters in DG systems which offer the possibility of high power quality injection from the converters when it is properly designed. In this case, it is commonly desired to design the inner current control loop circuit with high bandwidth characteristics to ensure accurate current tracking, shorten the transient period as much as possible, and force the interfaced converter to act equivalently as a current source amplifier within the current loop bandwidth. Nevertheless, if the current control loop is designed with high bandwidth characteristics (e.g. deadbeat control performance), the sensitivity of the dominant poles of the closed loop current controller becomes very

high to uncertainties in the total interfacing impedance (the value of impedance seen by the interfaced converter at the point of common coupling (PCC), which is a function of the ac grid impedance). The instability of the current control loop accompanied by the saturation effect of the pulse width modulator leads to sustained oscillations in the injected current from converter to the power grid or local loads. This situation is addressed as the low-frequency instability in DG system.

3. The control performance of the interfaced converter in DG unit is directly affected by the load voltage or voltage at the PCC. Due to the high propagation of grid-connected non-linear loads, the voltage at the PCC is more likely to be distorted; especially in weak grids with long radial distribution feeders. The grid voltage distortion and unbalance drive harmonic currents and increase the distortion in the exported power.

4. Severe and random current component disturbances in utility power sources might be initiated by non-linear and time-varying grid-connected loads, grid faults, voltage transients caused by capacitor switching and associated with parallel connected loads, and non-dispatchable power generation. The DG interface should offer high inviolability and the ability to revoke these disturbances; especially in case of utility sources with high sensitive connected loads.

1.4 Research Motivations

As mentioned in previous section, the unpredicted behaviour and dynamic nature of the power grid challenges the stability, reliability, security and control effectiveness of a grid-connected converter-based DG interface. Usually, disturbances in electrical power grid appear in the form of unbalance currents and voltages, voltage disturbances, interfacing parameter variations and grid impedance, and interaction with existing grid harmonic components during connection of non-linear load to the grid. Therefore, robust control of DG interface system is an important issue in the presence of grid interconnection. To facilitate a safe integration technique and larger penetration of DG units to the power grid, a robust control technique of DG system should be improved to meet the requirements for the electrical network and overcome these challenges.

Generally, the DG system should offer the following characteristics:

1. Fast dynamic response in tracking reference components according to the grid characteristics and conditions.
2. Accurate and robust current control performance with a strong ability of compensating the grid current distortion and voltage disturbances caused by interfacing parameters mismatch.
3. Strong ability of compensating for converter system delays.
4. Insensitivity to ac-side filter parameters and power system.
5. Flexible operation to reduce the total cost of proposes system and increases the reliability and accuracy of DG link.
6. Stable and high power quality grid operation along the whole loading trajectories of grid.

1.5 Research Objectives

This project aims at broadly developing an advance control technique of multilevel converter for integration of DG resources to the power grid. The proposed control technique can:

1. Connects DG resources to the medium and high voltage ac grid via multilevel converter.
2. Injects the maximum available active power of DG resources to the power grid continuously.
3. Provides load active power with accurate and fast dynamic response.
4. Compensates load reactive power and increase the power factor of power grid.
5. Supply load harmonic current components.
6. Guarantees balanced overall grid currents of unbalanced load.
7. Fast dynamic response in tracking rapid variations in load active and reactive powers.
8. Contribute to compensate load voltage drops.

To be fulfilled, the above objectives need to evolve and builds upon a number of tasks. Key tasks are:

1. Development of a grid-monitoring system for monitoring and measuring the currents of grid-connected loads and voltages at the point of common coupling.

2. Development of an effective interfacing system for the DG unit for injection of current components under the connection of DG resources to the medium and high power grid.

3. Development of an effective references system for the DG interfacing system, by setting appropriate references of DG control loop circuit.

4. Development of an effective current control technique for the DG interface capable of high power quality current injection of the grid under the presence of grid current distortion, interfacing parameter variation, and converter system delays.

5. Development of an interface-monitoring unit along with a grid-current and grid-voltage interfacing scheme for converter-based DG units.

6. Development of a voltage control system for the DG interface featuring fast grid voltage regulation and effective mitigation of fast and dynamic voltage disturbances.

7. Integration of the developed control algorithms to realize a robust DG interface for gird-connected interfacing systems.

1.6 Thesis Outline

This thesis presents a multi-objective control technique of multilevel converter topologies for integration of distributed generation resources based on renewable energy (and non-renewable energy) resources to the power grid. The proposed control technique of DG interfacing system is used to improve the quality of power grid by injection of active and reactive current components during integration of DG resources to the grid. In this dissertation we review and organize all pertinent subjects in an orderly way. The remainder of this thesis is structured as follows:

Chapter 2 describes the state of the art and a critical literature review on DG technology and different control techniques of converter-based DG system. Initially, we chose to explore the most common DG resources, such as wind turbines, photovoltaic systems, micro-turbines, and fuel cells. After we cover the basis of the primary DG resources, our approach is to show

how to integrate these sources of energy for electrical power generation and power injection into the power grid.

Chapter 3 is, in essence, an extended introduction that describes and discusses the state of the art of multilevel power converter main technologies. The main applications and advantages of these topologies, and a briefly reviews the attractive features and drawbacks of different types of multilevel converter topologies are presented in this chapter. In addition, different structures are presented in different levels for each topology.

Chapter 4 describes the proposed system model and proposed control schemes for the interfacing system between DG resources and power grid. The dynamic model of the proposed model is first elaborated in the stationary reference frame and then transformed into the synchronous orthogonal reference frame. Therefore, the state-space model of the proposed model is obtained and the large-signal and small-signal mathematical equations and models in ac side and dc side of the model based on multilevel converter as a general case, and a three-level NPC converter as a case study are developed, so that proper control circuit loops can be designed. In addition, the reference current components are designed in this chapter for injection of maximum available active power of DG resources to the power grid, provide enough robustness against grid current disturbances during connection of non-linear and unbalance loads to the grid; and retrain the full compatibility with digital platforms to maintain design flexibility.

Chapter 5 describes the principles of Space Vector Pules Width Modulation (SVPWM) technique for multilevel converter topologies. The general and basic concepts of the SVPWM switching method and its evolutions, advantages and limitations are investigated in this chapter. Subsequently, some important contributions are presented in order to achieve efficient SVPWM algorithms able to be implemented in a digital signal processor (DSP). By using the SVPWM switching strategy, the multilevel space vector block diagram is derived, and the switching time calculation is described. The basic steps in designing a switching sequence or sequence of vectors are defined so that minimum switching frequencies in the devices are achieved. In addition, the various parameters considered in the design stage to minimize the current ripple are considered. Finally, the multilevel SVPWM algorithm for a three-level NPC converter is developed and investigated by extracting all possible switching states.

Chapter 6 describes a current controller for a VSC-based DG interface, and a voltage regulator for dc bus voltage regulation of a NPC converter. In addition, a technique for balancing the voltage of dc bus cascaded capacitors is presented. The proposed current controller is designed for different topolo-

gies of the ac-filter to achieve accurate current regulation performance in the presence of grid uncertainties, converter system delays, and unexpected events in power grid. In this chapter, the proposed current controller and dc voltage regulator will be applied to the case of NPC converter output current control, and dc bus voltage regulation, during connection of DG resources to the power grid.

Chapter 7 presents the performances of the proposed control technique for integration of DG resources to the power grid by means of simulation results. In this case, the complete system model was simulated using the "*Power System Blockset*" simulator operating under the Matlab/Simulink environment. At first, capabilities of DG resources and flexibility of control strategy for control of VSC in providing active, reactive, unbalanced and harmonic current components of different grid-connected loads are presented, and the capabilities of control method on reactive power tracking with constant output active power are considered. In addition, the simulated results have been used to analyze the Total Harmonic Distortion (THD) of the utility grid current amid severe varying load conditions.

Chapter 8 describes hardware structure of the proposed control technique for integration of DG resources to the grid. The proposed control technique is digitally controlled by TMS320F2808 fixed-point digital signal processor (DSP) for hardware implementation and real-time code generation of the proposed control algorithm. The obtained results will verify the high potential of this topology for control of VSC during integration of DG resource into the power grid.

Chapter 9 describes the thesis conclusions, contributions, and directions for future work.

Chapter 2

Review of Previous Research

2.1 Introduction

This chapter describes a short background on common types of DG resources, based on renewable and non-renewable energy resources, and a detailed literature review on the converter-based DG interface system. The chapter is organized as follows: in section 2.2, different types of DG resources are presented, and some of their main characteristics are described briefly. Section 2.3 presents the DG interface system, particularly in case of voltage source converter (VSC) and other related components. In addition, a review of different current control techniques of DG interface system, effect of grid impedance and harmonic excitation, and some other limitation are presented in this section.

2.2 Distributed Generation Resources

DG technology is the application of small generators, scattered throughout a system to provide electrical energy closer to consumers. Different and common types of the source of energies that can be used in DG technology shows in figure 2.1. The general features of these types of energy resources are shortly introduced in the following subsections.

2.2.1 Wind Power

One of the most important reasons for continuing development of modern countries is contingent on the sustainability of energy. The vulnerability of the current energy resources chain, based on fossil fuel and non-renewable energy resources, will provoke a collapse in society with the exhaustion of its natural reserves. That is why generation of electrical energy from wind power is highly advised in electrical power generating networks, where the following factors are considered [5]

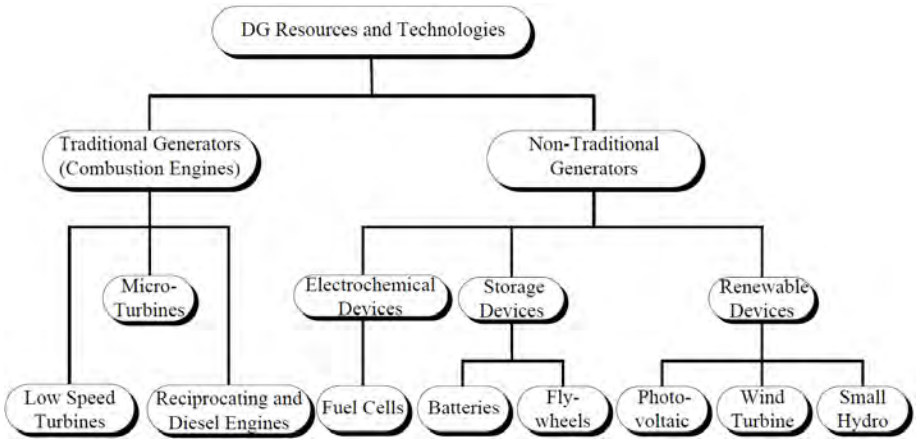


Figure 2.1: Different DG resources and technologies

1. High cost of energy based on thermo and hydro-electrical generation.
2. Plenty of areas with fairly high average wind speeds (> 3 m/s).
3. Need to supply remote loads, where a new transmission line is uneconomical.
4. Non-existence of rivers or other energetic hydro resources in close proximity.
5. Need for clean and renewable energy resources.

Base of wind power energy is derived from solar energy, due to uneven distribution of temperatures in different areas of the earth. The resulting movement of air mass is the source of mechanical energy that drives wind turbines and the respective generators. A wind turbine consists of turbine blades (usually two or three blades), a rotor, generator, coupling device or drive, shaft, and the nacelle (the turbine head) that contains the gearbox and the generator drive. Modern wind turbines can provide electricity as wind farms or as individuals. Electricity capacity is limited by the amount of wind, therefore; the wind plants should be installed in windy areas [17]. It has expected electrical efficiency of 20-40%, and the expected power sizes are in the range of 0.3 kW to 5 MW [18].

Structures of wind turbines are based on four types; they are: Type A, B, C and D. Between these four types technology, types A, B, and C are connected to the power grid or to the local loads via a rotary machine, which

is normally based on an induction generator. But in turbine type D, power electronic based converter, (usually a voltage source converter), used for grid interfacing system.

Generally, wind turbine farms have been found in areas with heavy wind profile. Large ratings such as 108 MW have been reported in some real projects [19]. Due to the extensive penetration of wind turbines technology and the chaotic nature of wind power generation, the effects of the wind power generation on electrical network performances are so significant. Currently, several extensive research efforts are running in addressing and mitigating the effects of wind power generation on power system operation [20], stability [21], planning and reliability [22], power quality [23], economic and market [24].

2.2.2 Photovoltaic

Sunlight is converted to electrical energy directly with modules consisting of many photovoltaic solar cells. Such solar cells are usually square or round in shape, and made of doped silicon crystal. These semiconductor based devices have the capabilities of converting incident solar energy into dc current, with efficiencies varying from 3 to 31%, which depending on the technology of design, the temperature and light spectrum, and the material of the solar cell [5]. Normally, the ratings of solar energy power based on PV vary from 0.3 kW to few MW. Nonetheless, because of the high cost of PV lands, weak sunlight intensity in many areas and climate changes leading to uncertain sun exposure, the larger sizes of PV generation units are limited [25, 26, 27]. Close to one acre of land is needed to generate 150 kW of electrical power based on photovoltaic technology. Currently, the cost per kW of a PV system is around $6000, whereas it is $900 in micro-turbine and $2800 in wind power generation [14]. Until the 1990s, the creation of photovoltaic farms (in analogy to wind farms) has been considered the preferred solution to increase the penetration of PV arrays. However, up to now, manufacturing costs and the relatively low electrical power efficiency of PV farms have been major impediments to its widespread use. On the other hand, use of small scale distributed PV panels (1-100 kW) yield cost effective solutions with higher reliability.

Recently, some interests appear in use of large scale PV farms by many countries, under the adoption of green energy policies. In general, the impact of PV generation profile on the system level, mainly voltage fluctuations and possible harmonic injection, is weak and it can be mitigated by injecting a controlled-reactive power through the PV converter itself or via nearby con-

trolled reactive power sources [28]. Therefore, the majority of photovoltaic energy system studies are directed either towards the internal controls of the PV generation system for better energy processing and precise power tracking or towards the development of more exotic solar cell technology for greater efficiency and to lower the overall power generation cost [29, 30].

Normally, large scale PV and wind farms are connected at the transmission or sub-transmission power levels, where the grid stiffness is higher and the impacts are less pronounced. Hence, research and studies related to PV and wind farms in the context of distribution systems are not practical and will lead to imperfect results [31]. Similar to the wind power generation system, PV based generator is interfaced to the power grid or a local load via a power electronic based converter; usually a voltage source converter [14].

2.2.3 Micro-turbine

Micro-turbines are small capacity combustion turbines, which can burn a variety of fuels, including natural gas, gasoline, diesel, kerosene, naphtha, alcohol, propane, methane, and digester gas. The majority of commercial devices presently available use natural gas as the primary fuel. They are small and use power electronics to interface with the load. Generally, micro-turbines consist of a compressor, combustor, recuperator, small turbine, and generator [5]& [32].

The main advantages of the Micro-turbines over conventional fossil-fueled power systems are as follows [5]:

1. They are light generator sets and they have very low in weight per horsepower.
2. They demonstrate pure rotary motion as opposed to stroking, resulting in less vibration, low noise compared to diesel generators, high mechanical performance, and very high reliability.
3. A liquid cooling system is not required.
4. Some micro-turbines run on air bearings with very low maintenance.
5. They exhibit a very fast response to load variation, since they do not need to build up pressure as in steam turbines or have high momentum as in reciprocating engines.
6. They operate on a variety of fuels.
7. They produce very low emissions.

8. Even low-power micro-turbines can provide recoverable heat for water and space heating, and the larger units can be used for industrial purposes or in a combined cycle with other turbines.

Because of the low price of natural gas, low installation cost of micro turbine based system, and low maintenance cost during performance, micro turbine technology is one of the most assuring DG energy resources today [33]. Similar to the wind and PV power generation system, micro-turbine generator is interfaced to the power grid or local loads via a power electronic converter; usually a voltage source converter [14]. Being a dispatchable source, micro-turbines do not cause intermittent generation problems.

2.2.4 Fuel Cell

A fuel cell (FC) is an electrochemical energy conversion system, where chemical energy is converted directly into electrical energy and heat. Resulting advantages of this technology are high efficiency almost at partial load, low emissions, noiselessness (due to non existence of moving parts), and free adjustable ratio of electric and heat generation. The operation of a fuel cell is closely alike to that of a battery system, except that it consumes fuel. The energy savings results from the high conversion efficiency, typically 40% or higher, depending on the type of fuel cell. When utilized in a co-generation application by recovering the available thermal energy output, overall energy utilization efficiencies can be in the order of 85% or more [34].

Unlike batteries, fuel cells do not need to be charged for the consumed materials during the electrochemical process since these materials are continuously supplied [35].Fuel cell capacities vary from 1-kW to few MW for portable and stationary units, respectively. It provides clean power and heat for several applications by using gaseous and liquid fuels. Fuel cells can use a variety of hydrogen-rich fuels such as natural gas, gasoline, biogas or propane. They operate at different pressures and temperatures, which vary from atmospheric to hundreds of atmospheric pressure for a wide range of temperatures. Similar to the wind, PV, and micro turbine power generation system, fuel-cell generator is interfaced to the gird or local load via a power electronic converter; usually a voltage source converter [14]. Being a dispatchable source, fuel cells do not cause intermittent generation problems.

2.2.5 Other DG Resources

Other types of DG resources based on renewable energy resources, such as bio-energy, ocean wave power, micro-hydro power, ocean thermal power,

and geothermal power are not commonly used due to high cost of the initial investment and low efficiency reasons.

2.2.6 Energy Storage Devices

New technologies develop efficient means of energy storage devices. Supercapacitors, flywheels, batteries energy storage system (BESS), and superconducting magnetic energy storage system (SMES) are some general types of energy storage devices [36]. These devices can have important roles in DG technology, to enhancing the reliability, enabling fast load pick-up, and flatting the generation profile in non-dispatchable energy resources [37].

Similar to the previous cases, energy storage generators are interfaced to the power grid or local loads via a power electronic converter; which is usually a voltage source converter [14].

2.2.7 Hybrid Systems

Hybrid DG energy resources based on renewable energy and non-renewable energy resources have been proposed, to improve the energy efficiency and power generation characteristics. For example, a solid oxide fuel cell has been combined with a gas micro-turbine to form a combined cycle power plant. The proposed combined power plant has an electrical efficiency of greater than 70% with ratings range from 250 kW to 2.5 MW.

High efficiency power rate, such as 75%, can be obtained with combined heat plants as well. In addition, the wind power resources have been used with other DG resources, such as photovoltaic, micro-turbines, fuel cells, energy storage devices or diesel-fired generators, particularly in weak and isolated electrical networks [38].

2.3 DG Interface System

Unlike large generators, which are based on 50/60 Hz synchronous machines, DG units have several different types of energy resources which are normally based on renewable energy resources and work in different speeds and frequencies. For example, some DG resources such as micro-turbine generators are consist of high speed or frequency DG resources, and the other types such as wind power are consist of variable speed or frequency DG resources. In addition, other type of DG system which is based on direct energy conversion resources such as photovoltaic and fuel cells producing dc voltages and dc currents.

Generally, a Voltage Source Converter (VSC) is necessary as the heart of the interfacing system between DG resources and utility grid, for integration of DG resources to the power grid. In general DG units, the interfacing system (VSC) is considered as one of the most important functional block. Multilevel converters are a good trade-off solution between performance and cost in high-voltage and high-power systems. The main advantages of multilevel converters are reduced voltage ratings for the switches, good harmonic spectrum (making possible the use of smaller and less expensive filters), and good dynamic response. However, the control complexity increases compared to conventional VSC. Figure 2.2 shows the schematic diagram of a DG system based on three-level VSC interface and the related control algorithm. As it can be seen that, a three-level VSC with ac-side impedance as the filtering system, form the power circuit schema, whereas different control loops form the converter control structure for integration of DG resources to the power grid. In this case, the power management and control system of interface converter should be able of providing flexible operation during connection of DG link to the power grid. For instance, voltage regulation of utility grid might not be required if the grid voltage is strong enough during the grid connected mode of DG system. In this case, the DG system will behave as a PQ generator system and the voltage control will not be a correct option. On the other hand, if the stiffness of the utility grid is not strong enough, the DG system might support the voltage profile by working as a PV generator.

In other operation modes of DG system like micro-grid operation mode, voltage regulation might be critical in case of high power quality injection, whereas the system control and power management system should take care of close load sharing of micro-grid loads according to the ratings of individual converters in proposed system. Regardless of the DG operation mode in system, the inner current control loop is necessary in DG control system in order to achieving a close control characteristics on the injected current and to force the interfacing system to work as a current-source amplifier in range of the current control bandwidth. In addition, an accurate integration strategy is also needed to obtain a controllable power flow in proposed network.

PWM switching strategy would guarantee that the current components injected from the interfaced converter to the local loads and unpolluted power grid is free from low-order harmonic distortion components. Nevertheless, the high-frequency current distortion due to the switching frequency must be attenuated to cope with the power quality standards for connection of a converter to the power grid; which is the main function of the ac-side filter.

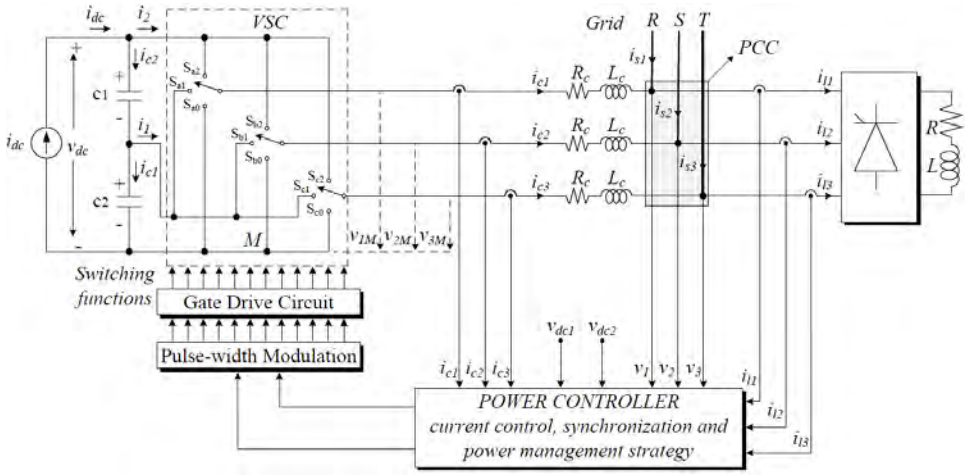


Figure 2.2: Schematic diagram and control functions of DG system based on three-level VSC

In fact, the behavior of interfacing system in DG system mainly based on the effectiveness of the proposed control loops. Moreover, it will be shown in this dissertation that many of system-level affects on the power generation performance of DG system and vice-versa (i.e., DG system affects on system operations) can be addressed by applying the appropriate mitigation strategy in the DG control circuit loop. As a similar case in the micro-grid operation mode, the frequency and voltage stability of the micro-grid system lies during the voltage and power controls of individual interface converters. The state-of-the-art of the controls of an interface converter in DG system is presented in the following subsections.

2.3.1 Current Control Technique in DG

The key element in the control scheme of a converter-based DG system is current control circuit loop of interfaced VSC.

The main objectives of the current controller in DG system are:

1. Provide a relatively high bandwidth to ensure accurate current tracking.

2. Reduce the transient time during DG integration and load compensation.

3. Force the VSC to act as a current source amplifier within the current loop bandwidth.

4. Responsible for the power quality of injected-current from DG link to the local loads and power grid, and over-current protection during sudden connection of local loads to the main grid.

Harmonic components in voltage of the utility grid, unbalance and non-linear grid-connected loads, grid parameters and switching transients directly affect the performances of DG current control circuit loop and might impair the power quality of injected power from DG unit to the unpolluted grid and loads, and even the stability of the interfacing system. Recently, the effects of grid harmonic components on the control effectiveness of DG interfacing system have begun to be investigated widely in many researches [39, 40]. Ref.[39] presents a robust control technique to regulate the grid current entering a distribution network from a three-phase VSC system via an LCL input filter. The presented results show that small distortion in the grid voltage highly increases the total harmonic distortion (THD) in the injected current from DG link to the power grid and eventually, converter instability can be reached due possible interaction between grid distortion and converter's power circuit filter. Therefore, grid disturbances suppression is one of the most important subjects that should be considered precisely in design the circuit loop of current controller in a converter-based DG system. The main strategies to regulate the injected current of a current-controlled VSC which is basically empowered by DG resources, include either a fixed-switching frequency schemes, such as the ramp comparison, stationary and synchronous frame proportional-integral (PI), and deadbeat predictive current control schemes or variable switching frequency such as the hysteresis control scheme [41]. Hysteresis current control techniques give fast transient response during transient times; but they are reported to impair from inter-phase distortion, and poor steady-state performance with high errors up to twice the hysteresis band. In addition, they result in unpredictable average converter switching frequency that varies with the load parameters and consequently the load current harmonics ripple is unpredictable. Even though some strategies are documented to constrain the variations in switching frequency, the incompatibility with full-digital platforms and the additional complexity make this scheme far from being practical. Ramp comparison control using a PI regulator in the stationary reference frame is used for a long time; but it has the problems of sensitivity to system parameters and steady-state phase errors [42].

Resonant stationary-frame controllers have been proposed to null the phase errors, however, resonant controllers provide internal model dynamics at preset frequency modes, and the tuning process of these controllers is not straightforward [43]. By using the synchronous rotating frame, the PI regulator can be used without the phase lag associated with stationary frame PI regulators [44, 45]. Yet, this scheme does not yield the optimal dynamic response from the converter due to its relatively slow transient response and the non-defined robustness properties. From the point of view of stabilities against grid disturbances, the compensation capability of the low-order harmonics in the case of PI controllers, either in the stationary or the synchronous reference frames, is very poor; yielding a major drawback when they are used in grid-connected and micro-grid operation mode. Resonant controllers, tuned for selective harmonics elimination, can relax this problem. However, these controllers are tuned at preset frequencies and the stability is not verifiably guaranteed for a large band of harmonic cancellations. These drawbacks are mentioned in [39], where a stationary-frame resonant controller for grid-side current regulation is proposed. The same mistakes can be traced in [40], where resonant synchronous-frame controllers are emerged in the current control structure to mitigate the effect of grid harmonics. An additional drawback of using the resonant controllers, either in the stationary or the synchronous reference frame is the interaction with variations in the grid impedance and ac-side filter parameters. Instability is created when a mismatch in the grid impedance or ac-side filter parameters shifts the bandwidth of the current controller to be lower than any of the resonant frequencies.

A robust high bandwidth current control technique of VSC can be used instead of using a resonant controller in DG system. Use of mentioned robust method can extend the capabilities of the converter control operations. The Important subject is the high disturbance rejection performance that can be obtained to reject low-order harmonic components caused by grid disturbances. In addition, the tracking ability of a high bandwidth current controller makes it feasible to be applied to regulate the injected current from DG link in the natural and stationary reference frames. Therefore, the negative effect of unbalanced grid voltages on the current injection performance of the DG link can be effectively reduced. Further, with a robust high bandwidth current control loop, current profiling can be made feasible. In addition, the internal current dynamics will appear almost ideal to the outer power sharing controls, hence, reducing the coupling among these loops; this is an important feature in power grid stability. However, the realization of a high bandwidth current regulation scheme, in the presence

of inherent system delays and plant uncertainties, is a challenging task.

If the applied current control loop is designed to yield a deadbeat response, a fast transient response of the current control loop can be achieved. Deadbeat current control techniques offer the potential of achieving the fastest transient response during integration time, more precise current control during tracking the reference currents, zero steady-state error after synchronization, and full-compatibility with digital-control platforms in a real time system test bed. In addition, this control scheme is found to provide the lowest distortion and the lowest current ripples; and, increasing the power quality of the injected currents from DG link to the local loads and polluted power grid [46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56]. However, inherent plant delays associated with the control voltage calculation, the nature of the PWM converter as a zero-order-hold (ZOH), and synchronous frame rotation limit the bandwidth of a deadbeat current regulation algorithm and eventually, the deadbeat gain, and accordingly the closed-loop bandwidth, should be reduced to account for system delays. In addition, as a model-based controller, conventional dead-beat current controllers show large sensitivity to plant unpredicted events. In the presence of grid harmonics and unbalance, there is no a priori information of plant dynamics; i.e. a complete plant model is not known in advance. Considering the delay issue, there are three approaches to implement a digital dead-beat current controller. First, it can be implemented with a relatively long control period, so that there will be enough space for control voltage calculation and dispatching the reference voltages to the modulator. This approach has been used in ref. [57] to implement a complex multi-variable state-feedback current controller strategy. However, in discrete-time control, it is always required to have a short control period to enhance the control precision and to increase the control bandwidth. Therefore, a longer control period results in lower control accuracy and lower bandwidth characteristics, hence, loosing some of the favorable features of the deadbeat control. In the second approach, the calculation of the control voltage is implemented on programmable logic devices such as erasable programmable read-only memory (EPROM) or field-programmable gate array (FPGA) [46]. In other cases, an FPGA co-processor structure is used in parallel with the main processor to give more computational resources [47]. By this way, the calculation time of the deadbeat algorithm is determined by the access time of the logic device, which is very small as compared to the control period. However, this approach requires additional hardware modules specific to the questioned application; and only simple control algorithm can be implemented due to the high engineering design costs associated with complex programmable logic devices. In the third approach, a small con-

trol period is selected and the deadbeat controller is implemented with a delay compensation method. In ref. [48], a delay compensation method employing a feedback of the summation of current errors is proposed. However, this method shows a large overshoot and long transient period. In ref. [49], digital deadbeat controllers for single and three-phase VSCs are proposed. The method compensates for the calculation and sampling delays by employing linear extrapolations for the line-voltage and a predictive observer for the current. However, the stability margin for parameter mismatch is poor. In ref. [50], a discrete-time predictive current controller is proposed. The controller employs a delay compensation method by adopting a predictive observer for the current. However, the algorithm is sensitive to parameter variation. Furthermore, the algorithm does not provide the necessary phase advance for the reference current in order to minimize the phase lag in the measured current. The nature of the deadbeat controller as a model-based controller makes it sensitive to plant uncertainties. In addition, the sensitivity of the deadbeat algorithm to plant uncertainties increases when the line voltage is estimated [51, 52]. In ref. [52], only 20% error in the load inductance can be tolerated when the back electromotive force (EMF) voltage is estimated. The parameter sensitivity issue is further addressed in ref. [53], where a PI regulator is connected in parallel to the deadbeat controller. However, the performance is un-satisfactory as the PI controller is working against unknown error dynamics. In ref. [54], a fuzzy-logic-tuned deadbeat controller is proposed to overcome the parameter sensitivity problems. However, the control algorithm is based on assuming a fundamental back EMF voltage component, and it is complex for real-time implementation. Improved robustness can be achieved by estimating the voltage disturbance, which is caused by uncertainties, and using the estimate in a feed-forward control manner. This technique is employed in ref. [55] and ref. [56]; where the disturbance is estimated using the disturbance observer theory in ref. [55] and the time delay control approach is used in ref. [56]. However, in both methods, the disturbance is estimated based on the inverse current dynamics, which yields a noise-prone estimate, and a low pass filter is adopted in the proposed estimators. The phase delay between the real voltage disturbance and the actual voltage disturbance degrades the compensation characteristics and limits the robustness range. Recently, an improved robustness against uncertainties in load inductance is reported in ref. [51] by assuming, instead of zero, the targeted current error at the end of the period k is equal to the difference between the previous two current errors. However, the robustness and stability range is up to 53% mismatch in the load inductance. Even though the robustness range has been extended,

the relative stability is still reduced with parameter variation; and there is a chance of instability for an unpredicted change in interfacing inductance and resistance, which remarkably vary with the grid impedance. A deadbeat current control technique that guarantees injection of the high power quality current under the presence of grid voltage distortion, interfacing parameters variation, and converter system delays demands special attention.

2.3.2 Effect of Grid Impedance and Harmonic Excitation

A DG system based on VSC interfacing system is a multi-input-multi-output non-linear power system with coupled dynamics. Wide range of dynamics can be yielded in a VSC interface system, which starting from the low frequency power generation sharing dynamics in the range of few Hz, to the high frequency dynamics of the ac-side filter in the range of few kHz. Based on the variable behaviour of electrical network, there is a possibility for dynamic interactions between the interfacing system and the power grid dynamics.

On the other hand, the grid impedance can shift the resonance frequency of the ac-side filter of the interfaced VSC. The presence of grid harmonics gives chances to harmonic excitation. In addition, instability in the interfacing impedance which is a function of the grid impedance affects the stability of the current control in DG system.

Up to now, just a few research projects and studies have addressed the interaction between the DG interface system and dynamics of electrical grid. The effect of impedance of electrical grid on the stability of the converter-based DG is addressed to some extent in [58]. However, the study considered only the case of resonant current controllers. Moreover, the proposed solution depends on accurate information of the grid impedance, which is an optimistic assumption.

2.3.3 Other Design Limitations

In the presence of the proposed system challenges in DG operation, some design limitations might be considered. Particularly, it is necessary to increase the power system reliability and reduce its cost calls for an interfacing plan with a reduced number of sensors. Along with the cost and reliability enhancements, huge performance developments can be achieved by omitting the grid voltage sensors in DG interface system. The grid voltage is key information in control of a DG interface system. Some functions based on signal processing techniques, such as phase locked loop (PLL) and sequence

detection are developed on the grid voltage signals.

Nevertheless, during measurement of the grid voltage in power system, some errors, such as an accumulated grid vector position and a residual negative sequence error are yielded.

Moreover, errors in the voltage measurement signals used for the feedback and close loop control can highly affect the power sharing in operation of power grid, due to the open loop nature of the power-sharing controllers. The errors occur by voltage measurement may result from the voltage sensors or sensor-filters not quite being precisely identical. Since the injected currents are highly sensitive to instance variations in the voltage command, which highly depends on the feed-forward components and the instantaneous angle of voltages at point of common coupling (PCC) or load voltages, it can be interesting to propose and design a control system for the interfacing without using sensors for grid-voltage. This is addressed as a grid-voltage sensor-less interfacing scheme, where the voltage information is estimated based on the current measurements. By this way, the extreme sensitivity to voltage measurements would be eliminated. Some research works are reported on the sensor-less operation of PWM rectifiers [59, 60]. The principle of direct power control is applied to realize voltage sensor-less control of a PWM rectifier system [59]. A direct control of instantaneous current of the converter, based on the direct power control and the estimation of the line voltage waveform, is proposed in ref. [60]. The mentioned voltage-sensor-less control technique, however, assume exact information of the grid impedance parameters at the point of common coupling. System parameters are time-varying on the distribution voltage level and directly affect the performance of the control system and estimation algorithms. Normally, any model-based grid-voltage estimator is by nature parameter-dependent. While the grid and interfacing parameters are time varying, the sensitivity of the interface control system to uncertainties in the interfacing impedance becomes higher as the voltage estimator dynamics is dependent on system parameters. The development of a robust grid voltage sensor-less interfacing scheme for converter-based DG demands special attention.

In addition, reliability and cost limitations might call for a functions-fusion feature during the DG interface system, where a single unit can works for multiple objectives, such as grid monitoring, synchronization, and self-commissioning/self-tuning control. A single unit that performs these functions in a computationally efficient manner has to be developed.

2.4 Conclusions of the Chapter

A critical literature review on the different types of DG resources, different control strategies used in the converter-based DG interface system and effects of different parameters of power grid in control system has been presented in this chapter. As mentioned in this chapter, the increasing number of DG units in electrical networks requires new techniques for the operation and management of the power networks in order to maintain or even to improve the power supply reliability and quality in future. As a consequence, the control of DG unit should be improved to meet the requirements for the electrical network. Therefore, design of a technique, which considers different situations of the electrical networks, become of high interest for connection of DG units to the electrical power system. The main objective of this chapter is to pinpoint the lack of robustness in existing control strategies against electrical network disturbances. Therefore, the development of flexible and multi-objective control strategies of DG interface system for integration of DG resources to the power grid, and overcome the aforementioned problems demands a special attention.

Chapter 3

Multilevel Power Converter Topologies

3.1 Introduction

Numerous multilevel converter topologies have been introduced in electrical systems during the last few years [61, 62, 63, 64, 65, 66]. Among the proposed power converter topologies for medium and high-power applications, the most common topologies are the Neutral-Point Clamped (NPC) converter (or neutral-clamped converter), the Flying Capacitor (FC) converter (or capacitor clamped converter), and the Cascaded H-Bridge (CHB) converter with separate dc sources (SDCS). Recently, many researchers have developed new topologies and unique modulation schemes. Several surveys of multilevel converters have been published to introduce these topologies [67, 68, 69, 70]. This chapter describes the attractive features of multilevel power converters in general.

This chapter is organized as follows: Multilevel converter topologies are reviewed and the fundamental operation of these structures is also presented in section 3.2. Different main topologies of multilevel converters are presented in section 3.3. In this section, main applications of different topologies in electrical systems, and their advantageous and drawbacks are presented briefly. The general characteristics of main multilevel converter topologies are summarized in section 3.4. Finally, several potential applications of multilevel converter topologies in electrical network are mentioned in section 3.5.

3.2 Multilevel Power Converter Features

Recently, multilevel power converters have received a great deal of attention in numerous high-power medium-voltage industrial applications [67, 68, 69] & [71, 72, 73, 74]. A multilevel converter uses a series of power semiconductor switches to perform the power conversion by synthesizing the ac output

terminal voltage from several dc voltage levels, and, as a result, staircase waveforms can be generated. Compared to standard two-level converter topology, multilevel converter topologies offer great advantages such as lower harmonic distortion, lower voltage stress on converter connected loads, lower common-mode voltage, and less electromagnetic interference. Therefore, by reducing filtering requirements, they not only improve the efficiency of converters, but also increase the load power and, hence, the load efficiency by improving the load voltage with a lower harmonic content.

Multilevel converters are basically developed to increase a nominal power in the converter. The higher number of voltage levels in these topologies results in higher quality output voltages. The concept of multilevel converters was introduced in 1975 [75], and the term "multilevel" first meant "three-level" [76] but now refers to converters with more than a two-level output voltage. Multilevel topologies have been developed by increasing the number of semiconductor switches or the number of power converter modules (i.e., multiple converter modules). The trend toward a greater number of voltage levels is necessary due to the benefits of higher voltage ratings with a very low total harmonic distortion (THD). By increasing the number of voltage levels, the converter's fundamental output voltage can be produced with a lower harmonic content, and will significantly improve the quality of the output voltage and eventually approach a desired sinusoidal waveform.

The conventional two-level converter can produce high-quality outputs for low-power applications by using a high switching frequency. However, for medium- and high power applications, the maximum switching frequency is limited by the switching devices due to the high switching losses. In this case, different topologies of multilevel converter can be used to lower the switching frequency, and a high quality output waveform can be produced. The superior features of multilevel converter topologies over two-level converter topology can be briefly summarized as follows [70, 72, 77, 78]:

1. They can generate output voltages with very low THD. Multilevel output PWM voltage can reduce the converter switches blocking voltage and the dv/dt stress on the load such as a motor. The lower voltage stress on a load can reduce the number of Electro-Magnetic Compatibility (EMC) problems.

2. They can produce a lower common-mode voltage. Therefore, the lifetime of a motor connected to a multilevel converter drive can be increased due to the reduced stress on the bearings of the motor.

3. By generating a staircase voltage waveform, they can produce lower

converter input current distortion. The lower current ripple can reduce the size of a capacitor filter in a dc-link.

4. They are capable of operating at both a fundamental switching frequency and a high switching frequency PWM. In high-power applications, a lower switching frequency can reduce the switching loss, resulting in an efficiency increase.

However, the trade-off for such increased performance in multilevel converters is that they require a greater number of power switching devices. The number of semiconductor switches together with their related gate drive circuits can increase the overall system cost and the control complexity. Therefore, they can be used only where the application and power level justify the choice of multilevel topologies. They have been selected as a preferred power converter topology for high-voltage and high-power applications.

3.3 Multilevel Power Converter Structures

The multilevel converters have different characteristics such as the number of components, the modularity, and the control complexity. Each converter topology can be chosen for a specific application. This section describes the major multilevel structures and their main applications in electrical power system.

3.3.1 Diode-Clamped Converter

In 1981, the first diode-clamped converter, also called a Neutral-Point Clamped (NPC) converter, was proposed by A. Nabae, I. Takahashi, and H. Akagi in [76]. The three-level NPC topology is based on a modification of the standard two-level converter topology by adding two new switching devices per phase, as shown in figure 3.1. The blocking voltage for each switching device of NPC is half the blocking voltage of the two-level converters with the same dc-link voltage. The multilevel output voltage is achieved by using clamping diodes and cascaded dc capacitors. This topology is extendable to higher number of voltage levels such as four- and five-level topologies. However, the three-level NPC has found wide applications in high-power medium-voltage drives. It can be seen in figure 3.1, to provide a floating neutral point; the two cascaded dc capacitors split the dc input voltage of the converter. The two diodes in each converter leg connected to the neutral point are called the clamping diodes. When switches S_1 and S_2 are turned

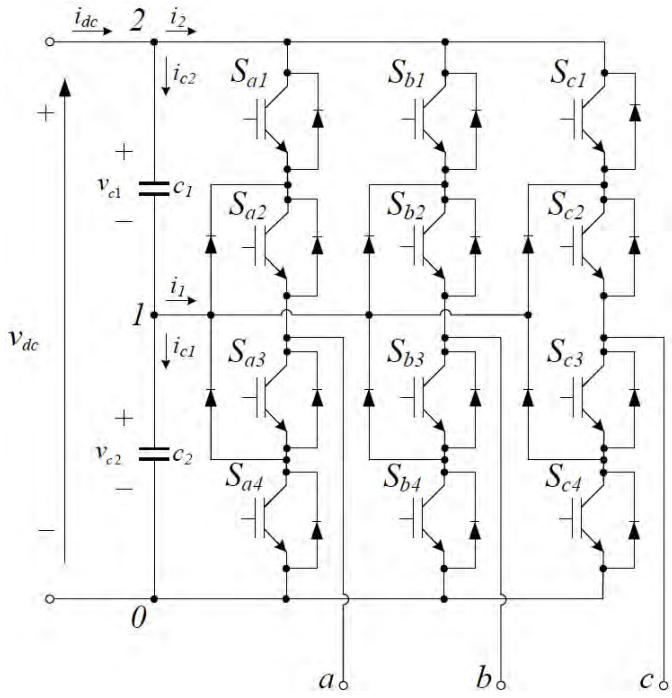


Figure 3.1: Three-level NPC converter

on and S_3 and S_4 are turned off, the converter output terminal is connected to the positive dc-link voltage $+v_{dc}$; when switches S_1 and S_2 are turned off and S_3 and S_4 are turned on, the converter output terminal is connected to the negative dc-link voltage $-v_{dc}$. When switches S_2 and S_3 are turned on, the converter output terminal is connected to the neutral point through one of the clamping diodes, depending on the direction of the load current. In this condition, the dc link capacitors (normally charged to $v_{dc}/2$) can be charged or discharged by the neutral current, causing a neutral-point voltage unbalance. Thus, the PWM control strategy is needed to balance the neutral-point voltage deviation, making the control algorithm complex. By using proper PWM switching, the average device switching frequency can also be increased to twice the actual switching frequency.

After a short time around the 1990s, several researchers published many articles that have reported experimental results for different levels diode-clamped converter for such uses as medium and high-power system integrations, static var compensation (SVC), and variable speed motor drives

[68, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91]. Figure 3.2 shows the schematic diagram of a three-phase six-level diode-clamped converter. It can be seen that, each of the three phases of the proposed converter shares a common dc bus, which has been subdivided by five cascaded dc capacitors into six levels. As shown in this figure, the voltage across each cascaded capacitor is v_{dc}, and the voltage stress across each switching device is limited to v_{dc} through the clamping diodes. Table 3.1 describes all the possibilities for output voltage levels for one phase of the proposed six level converter with the negative dc rail voltage v_0 as a reference point. The same as NPC converter, the term of state condition 1 declares the switch is on, and term 0 declares the switch is off. As shown in figure 3.2, five complementary switch pairs are in each phase, such that turning on one of the switches of the pair require that the other complementary switch be turned off. For example, the complementary switch pairs for phase leg (a) are (S_{a1}, S'_{a1}), (S_{a2}, S'_{a2}), (S_{a3}, S'_{a3}), (S_{a4}, S'_{a4}), and (S_{a5}, S'_{a5}). In addition, table 3.1 shows that in a diode-clamped converter, the switches that are on for particular phase legs are always adjacent and in series. For six-level converter, a set of five switches is on at any given time. Each active switching device is required to block only a voltage level of v_{dc}, the clamping diodes require different ratings for reverse voltage blocking. By considering phase (a) of figure 3.2 as an example, when all the lower switches S'_{a1} through S'_{a5} are turned on, D_4 must block four voltage levels, or $4v_{dc}$. Similarly, D_3 must block $3v_{dc}$, D_2 must block $2v_{dc}$, and D_1 must block v_{dc}.

In general case, for an n-level diode-clamped converter, (n-1) consecutive switches of each leg must be in the on-state. Therefore, a specified voltage level of the cascaded dc capacitors in dc-side of converter is connected to the output of converter. Figure 3.3 shows a three single-phase with n-throw switches, can carry out as a functional diagram of an n-level diode-clamped converter.

All of the possible combinations of proposed converter are summarized in equation (3.1). The control functions of the single-pole n-throw switches are defined by S_{ij}. These variables describe the position of the different switches, therefore they have the unity value when the i output is connected to the j point, otherwise they are zero (S_{ij}=[0,1]).

$$\sum_{j=0}^{n-1} S_{ij} = 1 \quad with \quad i = \{a, b, c\} \tag{3.1}$$

By referring all of the voltages to the lower dc-link voltage level (0 references), each output voltage consists of contributions by a determinate

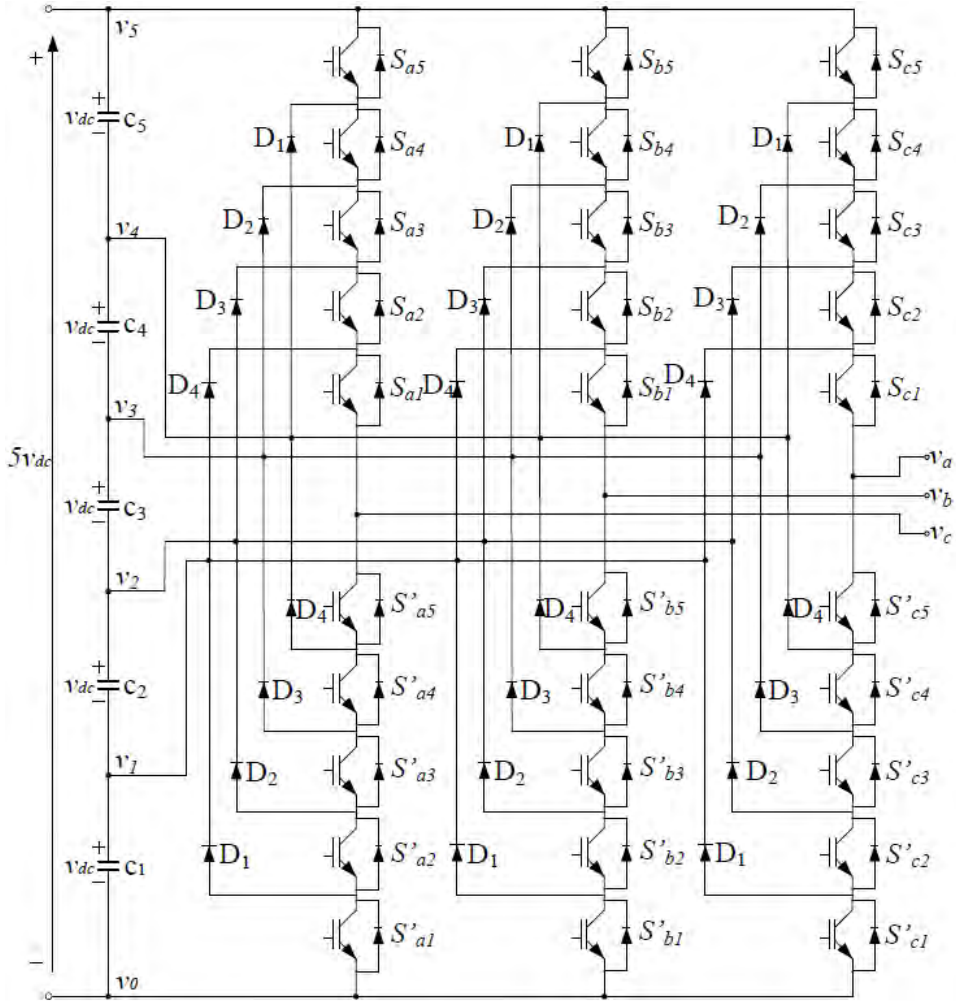


Figure 3.2: Schematic diagram of three-phase six-level diode-clamped converter

Voltage	Switch State									
v_{a0}	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	S'_{a5}	S'_{a4}	S'_{a3}	S'_{a2}	S'_{a1}
$v_5 = 5v_{dc}$	1	1	1	1	1	0	0	0	0	0
$v_4 = 4v_{dc}$	0	1	1	1	1	1	0	0	0	0
$v_3 = 3v_{dc}$	0	0	1	1	1	1	1	0	0	0
$v_2 = 2v_{dc}$	0	0	0	1	1	1	1	1	0	0
$v_1 = v_{dc}$	0	0	0	0	1	1	1	1	1	0
$v_0 = 0$	0	0	0	0	0	1	1	1	1	1

Table 3.1: Voltage levels and corresponding switch states for a six-level Diode-clamped converter

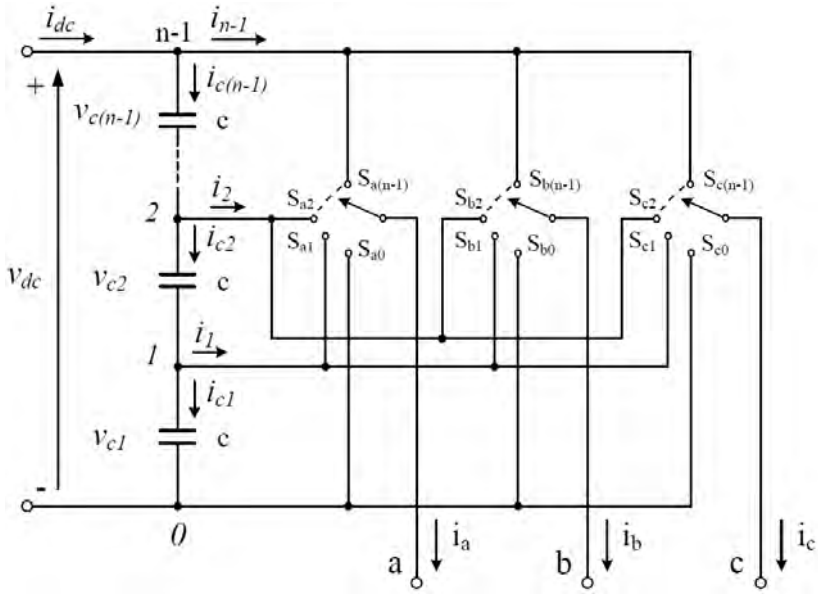


Figure 3.3: Schematic diagram of the n-level diode-clamped converter

number of consecutive capacitors will be obtained as:

$$v_{io} = \sum_{j=1}^{n-1}(S_{ij}\sum_{p=1}^{j} v_{cp}) \quad with \quad i = \{a, b, c\} \tag{3.2}$$

When balanced distribution of the dc-link voltage among the cascade dc capacitors is assumed, the output voltage can be expressed as:

$$v_{io} = \frac{v_{dc}}{n-1}\sum_{j=1}^{n-1} jS_{ij} \quad with \quad i = \{a, b, c\} \tag{3.3}$$

Under balanced condition, the maximum forward voltage applied to the switches of the bridge is the voltage of one single capacitor.

The three line-line voltage waveform for a three-phase n-level diode-clamped converter is shown in figure 3.4. The line voltage v_{ab} consists of voltage of phase-leg (a) and phase-leg (b). The resulting line voltage is an (2n-1)-level staircase waveform. This means that an n-level diode-clamped converter has an n-level output phase voltage and a (2n-1)-level output line voltage. Although each active switching device is required to block only a voltage level of v_{dc}, the clamping diodes require different ratings for reverse voltage blocking. For example, by considering phase (a) in figure 3.2, when all the lower switches S'_{a1} through S'_{a5} are turned on, D_4 must block four voltage levels, or $4v_{dc}$. Similarly, D_3 must block $3v_{dc}$, D_2 must block $2v_{dc}$, and D_1 must block v_{dc}.

If the converter is designed such that each blocking diode has the same voltage rating as the active switches, D_n will require n diodes in series; consequently, the number of diodes required for each phase would be $(n-1)\times(n-2)$. Therefore, the number of blocking diodes is quadratically related to the number of levels in a diode-clamped converter [68]. For the general case of a multilevel diode-clamped converter, (n-1) consecutive switches of each leg must be in the on-state. As a result, a defined voltage level of the cascade dc capacitors is connected to output of converter.

The main applications of multilevel diode-clamped converter are as follows:

- Can be use as an interface system between HVDC transmission line and ac transmission line [68].
- Interfacing between renewable energy resources and power grid.
- Can be use as a variable speed drive for high-power medium voltage motors [75, 86, 90, 91, 92].

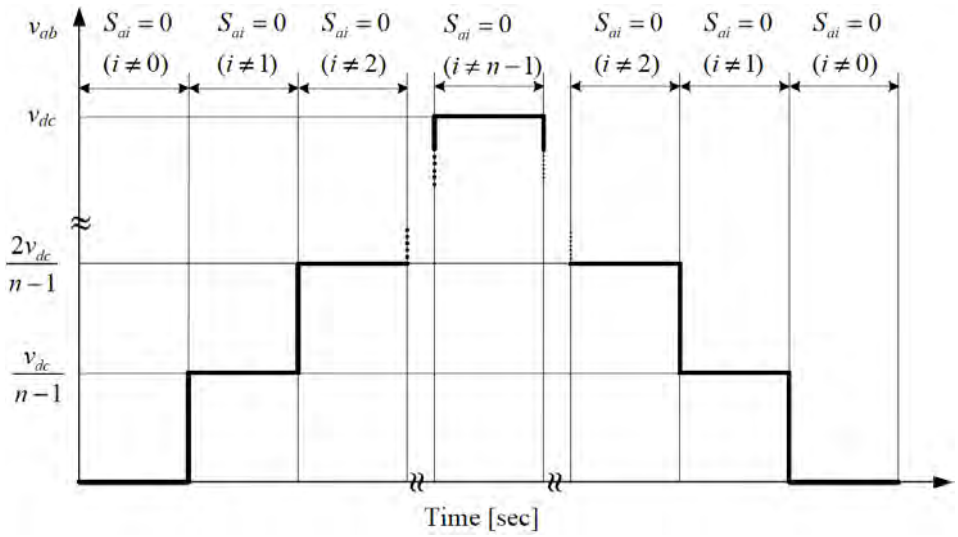


Figure 3.4: Line voltage waveform for an n-level diode-clamped converter

- Can be use as Static var compensation.

The main advantages of the diode-clamped topologies over the other topologies are as [67, 68, 92]:

- The switches can be selected with lower blocking voltages.
- Any number of voltage levels can be obtained by increasing the number of switches in this topology.
- Low number of capacitors is used in this topology, and the capacitors can be pre-charged as a group.
- Efficiency of this topology is high for fundamental frequency switching.

The main drawbacks of this topology are:

- The capacitor voltage deviation.
- The requirement for a complicated PWM switching strategy.
- The different blocking voltages of the additional clamping diodes.

3.3.2 Flying Capacitors Multilevel Converter

A Flying-Capacitor (FC) converter was proposed by Meynard and Foch in 1992 [93]. Figure 3.5 shows a typical configuration of a 3-level flying-capacitor converter. Compared to NPC, this topology uses dc capacitors connected to the cascaded switches instead of using clamping diodes. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage on each capacitor demonstrates the size of the voltage steps.

One advantage of the flying-capacitor-based converter is that it has redundancies for inner voltage levels; in other words, two or more valid switch combinations can synthesize an output voltage. Table 3.2 shows a list of all the combinations of phase voltage levels that are possible for the six-level circuit shown in figure 3.5.

Unlike the diode-clamped topology, the flying-capacitor converter does not require all of the switches that are on (conducting) be in a consecutive series. In addition, the flying-capacitor topology has phase redundancies, whereas the diode-clamped topology has only line-line redundancies [68, 92, 94]. These redundancies allow a choice of charging or discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels. In addition to the (n-1) dc-link capacitors, the n-level flying-capacitor multilevel converter will require $\frac{(n-1)(n-2)}{2}$ auxiliary capacitors per phase if the voltage rating of the capacitors is identical to that of the main switches.

The main application of multilevel flying capacitor converter is static var compensation.

The main advantages and disadvantages of multilevel flying capacitor converter topology are as follows [68, 92]:

- The large number of capacitors enables the converter to ride through short duration outages and deep voltage sags.
- Real and reactive power flow can be controlled by this topology.
- Phase redundancies are available for balancing the voltage levels of the capacitors.

and the main drawbacks of this topology are classified as:

- Control of this topology is complicated to track the voltage levels for all of the capacitors.

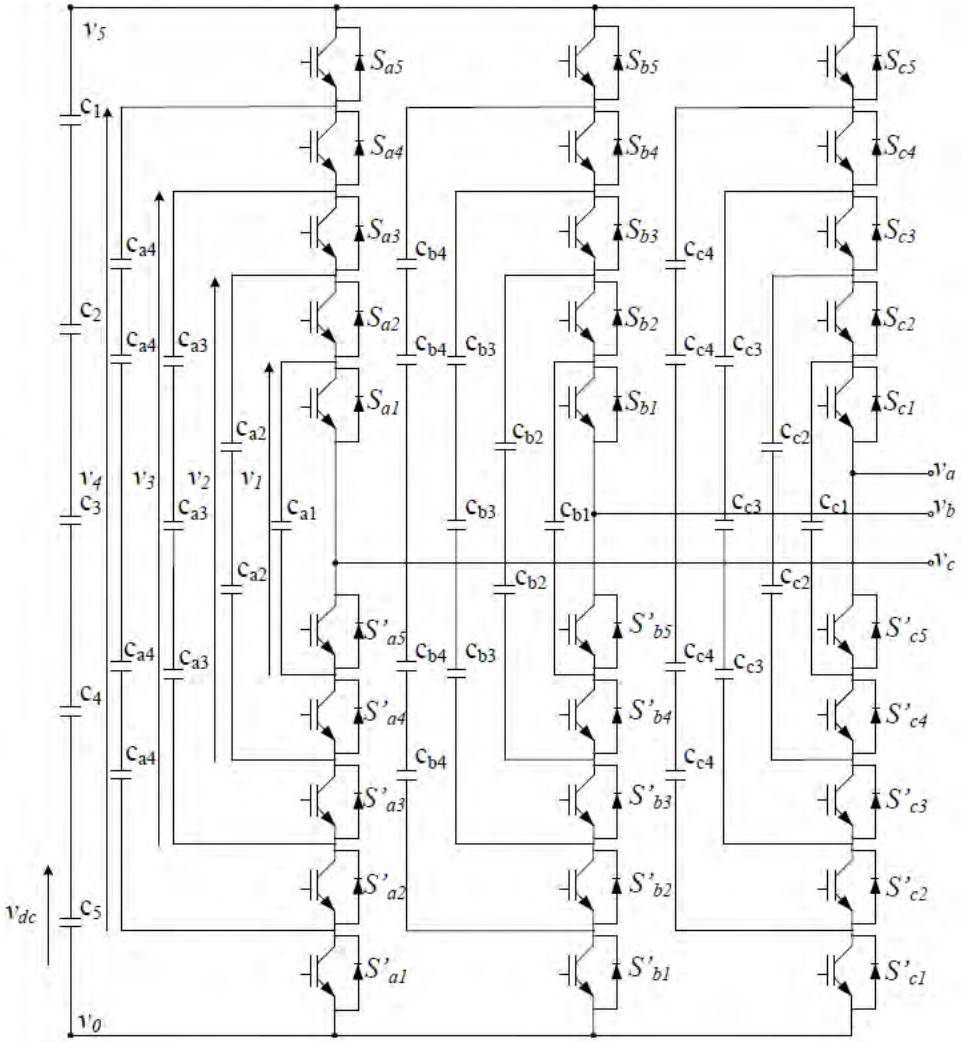


Figure 3.5: Schematic diagram of a six-level flying capacitor converter

Voltage	Switch State									
v_{a0}	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	S'_{a5}	S'_{a4}	S'_{a3}	S'_{a2}	S'_{a1}
$v_{a0} = 5_v dc$	(no redundancies)									
$5v_{dc}$	1	1	1	1	1	0	0	0	0	0
$v_{a0} = 4v_{dc}$	(4 redundancies)									
$5v_{dc} - v_{dc}$	1	1	1	1	0	0	0	0	0	1
$4v_{dc}$	0	1	1	1	1	1	0	0	0	0
$5v_{dc} - 4v_{dc} + 3v_{dc}$	1	0	1	1	1	0	1	0	0	0
$5v_{dc} - 3v_{dc} + 2v_{dc}$	1	1	0	1	1	0	0	1	0	0
$5v_{dc} - 2v_{dc} + v_{dc}$	1	1	1	0	1	0	0	0	1	0
$v_{a0} = 3v_{dc}$	(5 redundancies)									
$5v_{dc} - 2v_{dc}$	1	1	1	0	0	0	0	0	1	1
$4v_{dc} - v_{dc}$	0	1	1	1	0	1	0	0	0	1
$3v_{dc}$	0	0	1	1	1	1	1	0	0	0
$5v_{dc} - 4v_{dc}$ $+3v_{dc} - v_{dc}$	1	0	1	1	0	0	1	0	0	1
$5v_{dc} - 3v_{dc} + v_{dc}$	1	1	0	0	1	0	0	1	1	0
$4v_{dc} - 2v_{dc} + v_{dc}$	0	1	1	0	1	1	0	0	1	0
$v_{a0} = 2v_{dc}$	(6 redundancies)									
$5v_{dc} - 3v_{dc}$	1	1	0	0	0	0	0	1	1	1
$5v_{dc} - 4v_{dc} + v_{dc}$	1	0	0	0	1	0	1	1	1	0
$4v_{dc} - 2v_{dc}$	0	1	1	0	0	1	0	0	1	1
$4v_{dc} - 3v_{dc} + v_{dc}$	0	1	0	0	1	1	0	1	1	0
$3v_{dc} - v_{dc}$	0	0	1	1	0	1	1	0	0	1
$3v_{dc} - 2v_{dc} + v_{dc}$	0	0	1	0	1	1	1	0	1	0
$2v_{dc}$	0	0	0	1	1	1	1	1	0	0
$v_{a0} = v_{dc}$	(4 redundancies)									
$5v_{dc} - 4v_{dc}$	1	0	0	0	0	0	1	1	1	1
$4v_{dc} - 3v_{dc}$	0	1	0	0	0	1	0	1	1	1
$3v_{dc} - 2v_{dc}$	0	0	1	0	0	1	1	0	1	1
$2v_{dc} - v_{dc}$	0	0	0	1	0	1	1	1	0	1
v_{dc}	0	0	0	0	1	1	1	1	1	0
$v_{a0} = 0$	(no redundancies)									
0	0	0	0	0	0	1	1	1	1	1

Table 3.2: Redundant voltage level and corresponding switch states of six-level Flying-capacitor converter

- Precharging of all the capacitors to the same voltage level and start-up are complex.
- Switching utilization and efficiency of this topology are poor for real power transmission.
- The large numbers of capacitors are both more expensive and bulky in comparison with clamping diodes in multilevel diode-clamped converter topology.
- Packaging is also more difficult in this topology with a high number of levels.

3.3.3 Cascaded H-bridges Converter with Separate dc Sources

The cascaded H-bridge converter is composed of multiple units of single-phase H-bridge power cells as shown in figure 3.6. In this topology, each converter level can generate three different voltage outputs ($+v_{dc}$, 0, and $-v_{dc}$) by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. Switching states in figure 3.6, are define as:

$$\left\{\begin{array}{r} +v_{dc} \longrightarrow S_1, S_4 \;\; are \;\; ON \\ 0 \longrightarrow S_1, S_2 \;\; or \;\; S_3, S_4 \;\; are \;\; ON \\ -v_{dc} \longrightarrow S_2, S_3 \;\; are \;\; ON \end{array}\right\} \tag{3.4}$$

The ac outputs of each of the different full-bridge converter levels are connected in series such that the synthesized voltage waveform is the sum of the converter outputs. The number of output phase voltage levels (n) in a cascade converter is defined by $n = 2k + 1$, where k is the number of separate dc sources.

The main applications of multilevel cascaded converter are as follows:

- Static var generation.
- Interface between renewable energy resources and power grids.
- Battery-based applications.

As mentioned before, the cascaded topology is ideal for integrating renewable energy resources with a power grid, because of the need for separate dc sources (SDCS), which is the case in applications such as photovoltaic or fuel cell. Cascaded converters have also been proposed for use as the main

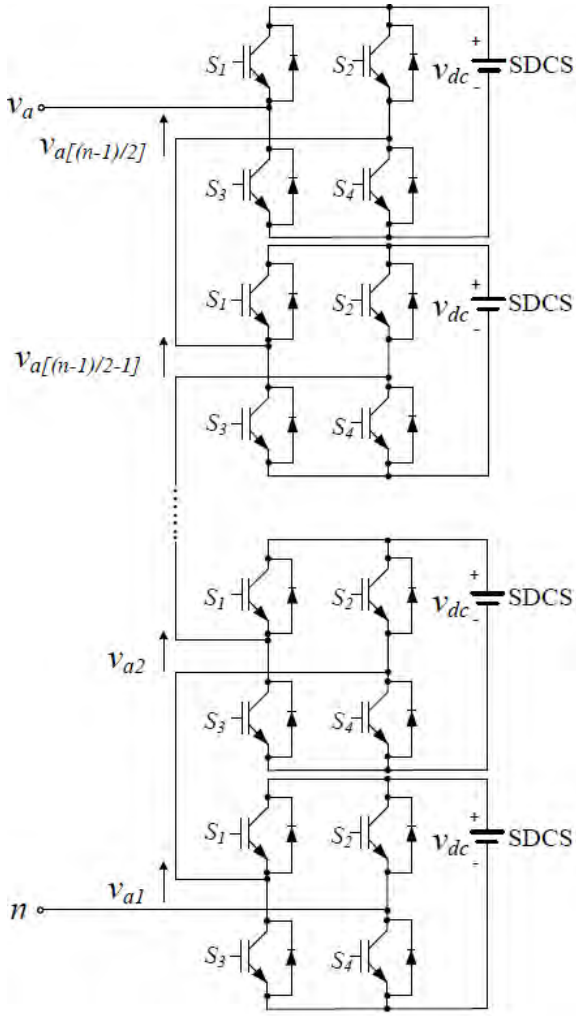


Figure 3.6: Single-phase schematic diagram of a multilevel cascaded H-bridges converter

traction drive in electric vehicles, where several batteries or ultra-capacitors are well suited to serve as SDCSs [80, 87]. The cascaded converter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply. Another application of cascade topology is, it is to act as a rectifier in a vehicle that uses regenerative braking.

The main benefits of the multilevel converter based on cascade topology are:

- Its modular structure and high voltage operation without switching devices in series, for these features eliminate the problem of equal voltage sharing for series-connected devices.
- The number of possible output voltage levels is more than twice the number of dc sources ($n = 2s + 1$).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

The drawbacks of cascade topology are:

- Its requirements for a large number of isolated dc supplies and a switching device count.

3.4 General Data for Basic Multilevel Topologies

The general characteristics of main multilevel converter topologies are summarized in table 3.3.

3.5 Application of Multilevel Converters

As we mentioned in previous sections, multilevel converters have been selected as a preferred power converter topology for high-voltage and high-power applications and they have several applications in medium- and high-power systems. These types of converter topologies can operate either as converters or as rectifiers. Several potential applications of multilevel converter topologies in electrical network are mentioned in the following subsections.

	Diode-Clamped	Flying Capacitor	Cascaded H-bridges
a	6(n-1)	6(n-1)	6(n-1)
b	6(n-2)	0	0
c	3(n-1)(n-2)	0	0
d	(n-1)	(3n-5)	$Even: \frac{(3n-3)}{2}, Odd: \frac{(3n-4)}{2}$
e	(n-1)	$(n-1)^2 + 3\sum_{i=1}^{n-2} i^2$	$Even: \frac{(3n-3)}{2}, Odd: \frac{(3n-4)}{2}$
f	$\frac{v_{dc}}{n-1}$	$\frac{v_{dc}}{n-1}$	$\frac{v_{dcequiv}}{n-1}$
g	$(2n-1)$	$(2n-1)$	$(2n-1)$
h	$(4n-3)$	$(4n-3)$	$(4n-3)$
i	n^3	$2^{3(n-1)}$	$2^{3(n-1)}$
j	$n^3-(n-1)^3$	$n^3-(n-1)^3$	$n^3-(n-1)^3$
n	Number of level		
a	Switches (with free-wheeling diodes)		
b	Independent diodes (with different reverse voltages possible)		
c	Independent diodes (series connection for same reverse voltage distribution)		
d	Capacitors (with different voltages possible)		
e	Real number of Capacitors		
f	Maximum voltage applied		
g	Line-to-Line output voltage levels		
h	Phase voltage levels for star load connection		
i	States of the converter (vectors of the SV diagram, including multiple ones)		
j	States of the converter with different line voltages		

Table 3.3: General characteristics of multilevel converter topologies

3.5.1 Boost Rectifier

They are the most popular power converter topologies used in high power motor drive applications and three-phase PFC rectifiers. Since the converter is reversible in this application, the rectifier allows bi-directional energy flux so that the mechanical energy from the motor can be recovered into the main source [95].

3.5.2 Superconducting Magnetic Storage Energy (SMSE) Systems

The reversibility property is highly important for the operation of SMSE systems, since the energy accumulated into superconducting coil must be recovered into the ac side whenever it is required [96].

3.5.3 High-Voltage DC (HVDC) Transmission System

For long-distance transmission of energy, HVDC systems may be less expensive and suffer lower electrical losses. HVDC allows power transmission between unsynchronized ac distribution systems, and can increase system stability by preventing cascading failures from propagating from one part of a wider power transmission grid to another. In addition, dynamic damping of electrical system oscillations may influence the selection of HVDC transmission system in preference to the ac transmission system. On the other hand, it is possible to integrate two ac systems with different frequencies by use of HVDC technique in transmission lines. Multilevel converter topologies are often proposed as a perfect solution for synthesizing HVDC systems [97].

3.5.4 Power Injection into the Power Grid

These types of the converter topologies are very good alternative for interfacing between the source of energies and the power grid. By this topology, it is possible to inject the electric energy into the electrical power grid. The produced energy is applied as a source of energy in dc form into the dc-side of the interfaced converter, and the ac side of the interface is connected into the power grid. Some practical applications of this topology include Distributed Generations (DG) technology based on renewable energy resources such as wind power and solar energies (Figure 3.7). The voltage generated by variable-speed wind power generators, PV generators, and fuel cells cannot be directly connected with the grid. Therefore, power electronics technology

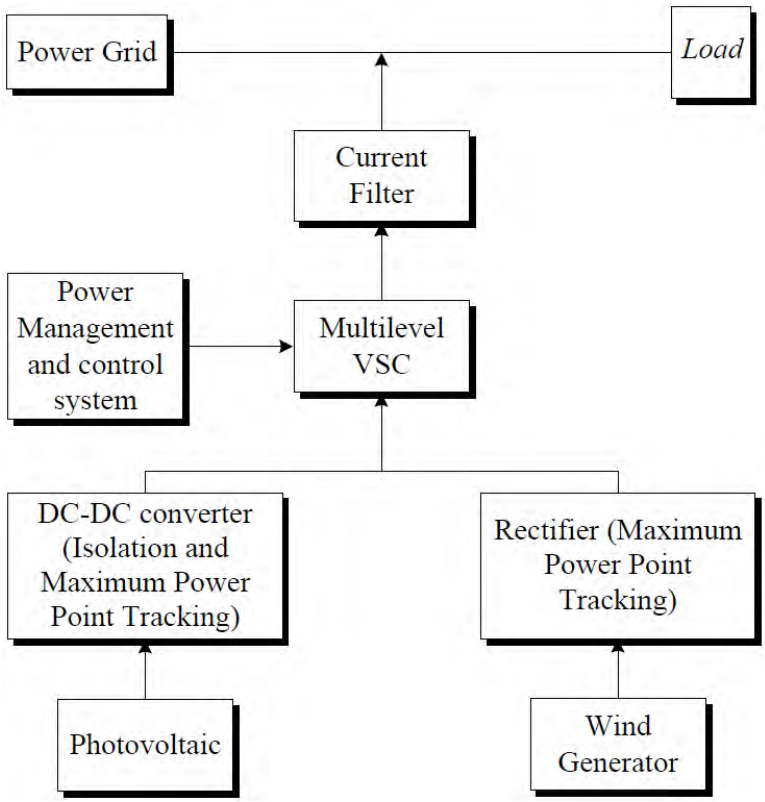


Figure 3.7: Power injection into the power grid by use of multilevel converter

plays a vital role in matching the characteristics of the dispersed generation units and the requirements of grid connection, including frequency, voltage, active and reactive power controls, and harmonic minimization [5].

3.6 Conclusions of the Chapter

This chapter has presented the state of the art of multilevel power converter main technologies. The basic principles of different multilevel converters topologies are discussed, and for each multilevel topology, different structures are presented. Most of the chapter focus has addressed modern and more practical industrial applications of different multilevel converters topologies. A procedure for calculating the required ratings for the active switches, clamping diodes, and dc-link capacitors with a design example has been explained. In addition, different advantages and disadvantages of dif-

ferent topologies have been described and main applications of them briefly presented. It should be noted that this chapter could not cover all multilevel power converter related applications and details; however the basic principles of different multilevel converter topologies have been discussed methodically.

Chapter 4

Analysis of Proposed DG Model Base on Multilevel Converter

4.1 Introduction

This chapter analyzes the modeling of the proposed DG system based on multilevel converter topologies and the dynamic model of the proposed model during integration of DG resources to the power grid. In this model, a voltage source converter which basically is a multilevel converter will be used as a heart of interfacing system between DG resources and power grid.

The high frequency switching capabilities of the IGBTs used in multilevel converter make it possible to use high frequency pulse-width modulation (PWM) techniques which allow high performance control of the current while minimizing the low frequency current harmonic components without the need of large passive filters. The high frequency modulation also makes it possible to use a low frequency model of the converter and to approximate the behaviour of the converter as ideal controllable voltage sources. This is possible thanks to the low pass nature of the physical systems connected to the converters, which have the ability to filter the high frequency content of the injected current by the interfaced converter. This allows applying the well known linear system analysis tools to study the system and design its controllers.

When studying the dynamic behaviours of proposed model and the design of the control of the interfaced converter, a common approach is to divide the design problem into a series of small problems. For example, as the capacitor of dc bus is large, its dynamic responses are usually slower than the dynamics of the current of the generator and the current on the ac grid side. Therefore the design of the generator current controllers, the ac grid side current and the dc side voltage is dealt separately.

This chapter is organized as follows: some general plans and information of proposed DG model is presented in section 4.2. In section 4.3, schematic

diagram of a three-phase system model based on multilevel converter for integration of DG resources to the power grid is presented. In addition the Park and Clarke transform matrix are presented in this section. In section 4.4, reference currents of the DG control loop are presented according to the DG objectives. The dynamic equations of the DG model in phase and line-to-line models are presented in section 4.5. The state-space model of the proposed DG model, and the large-signal and small-signal mathematical equations and models in ac side and dc side of the DG model based on multilevel and a three-level converter as a case study is developed in section 4.6. The steady-state analyzes and equivalent circuit model of DG model will be evaluated in this section to design a proper controller for this model.

4.2 Proposed DG Model Based on Multilevel Diode-Clamped Converter Topology

Different types of multilevel converter based DG systems are required large-signal model and small- signal model analysis for design an appropriate controller according to objectives of the DG system.

4.2.1 Large-signal Model

Large-signal modelling is a common analysis method used in electrical engineering to describe non-linear devices in terms of the underlying non-linear equations. In circuits containing non-linear elements such as transistors, and diodes, under large-signal conditions, ac signals have high enough magnitude that non-linear effects must be considered. In this chapter, large-signal mathematical models are used to obtain simulation results for the multilevel converter based DG model. They are mathematically analyzed and formulated in terms of control functions of the interfaced converter's switches in DG model. Therefore, if the switching states functions of converter are substituted by their duty cycles, the output waveforms obtained are free of certain components related to switching frequency of converter. Large-signal models can be interesting in terms of ability to analyze transitory averaged evolutions of current and voltage components, as well as to perform low-frequency analysis.

4.2.2 Small-signal Model

Small-signal modeling is a common analysis technique in electrical engineering which is used to approximate the behaviour of non-linear devices with

linear equations.

A small-signal model takes a circuit model and based on an operating point (bias) it linearizes all the non-linear components by some mathematical tools. Nothing changes in this model, because the assumption is that the signal is very small that the operating point does not change. Small-signal model of the system is needed to study and design different control loops techniques in proposed electric system. As the control stage must achieve the operation point of the system while disregarding high-frequency components of the variables (switching frequency of the converter), this mathematical model is formulated in terms of local averaged variables. In general case, state-space formulation models are used for the small-signal model of proposed electric system.

4.2.3 Control Structures for Grid-connected DG

The control structure applied to the grid-side interface converter consists mainly of two cascaded loops. In general case, there is a fast internal current control loop, which regulates the injected current from converter to the power grid, and an external voltage loop, which controls the dc-link voltage in dc side of the interfaced converter in DG model. The current control circuit loop is responsible for power quality issues and current protection in power grid; thus, harmonic and reactive current components compensation and dynamic behaviours of grid are the important properties of the current controller in DG system. In addition, the dc-link voltage controller is designed for balancing the power flow in the proposed model. Usually, the design of this controller aims for system stability having slow dynamic responses. In several research works and projects, the control of grid-side controller is based on a dc-link voltage loop cascaded with an inner power loop instead of a current control circuit loop. In this case, the injected current from DG link into the power grid is controlled indirectly. In addition, some control techniques employing an external power circuit loop and an internal current circuit loop are also documented.

4.3 Voltage and Current Components in Different Reference Frames

The proposed control technique of multilevel converter topologies in this dissertation is based on the analysis of voltage and current vector components in the special reference frames, e.g., 123(abc) to $\alpha\beta 0$ and $\alpha\beta 0$ to dq0

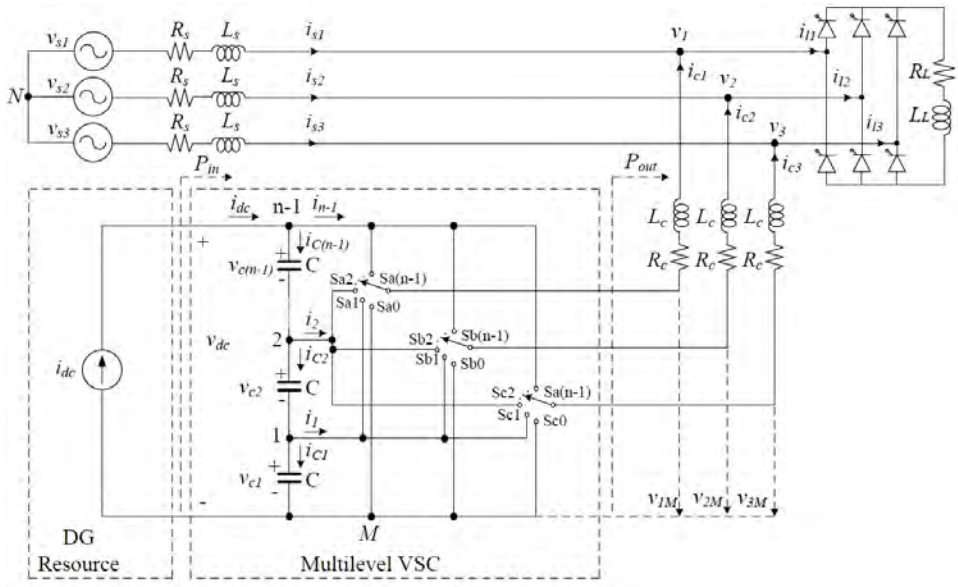


Figure 4.1: Schematic diagram of proposed DG model based on multilevel converter

transformation [98]. In this technique, synchronous reference frame control also called dq control frame uses a reference transformation frame module, e.g., abc⟶dq, to transform the grid current and voltage waveforms into a reference frame that rotates synchronously with the grid voltage. By means of this technique, the control variables values become dc values; thus, filtering and controlling can be achieved easily. Figure 4.1 shows the general schematic diagram for a network connection of a gird-connected VSC, based on multilevel converter topologies, used to interface a DG unit to the power grid. Conventional signs of voltages and currents components are also indicated in this schema, where R_c and L_c represent the equivalent resistance and inductance of the ac filter, coupling transformer, and connection cables; R_s and L_s represent the grid resistance and inductance up to the PCC, respectively; v_k $(k = 1, 2, 3)$is the supply voltage components at the PCC; v_{sk} (k=1,2,3) is the grid voltage components; v_{dc} is the dc-link voltage; and i_{sk}, i_{lk} , and i_{ck} are grid, load and DG current components respectively. In addition, the DG resources and additional components are represented as a dc current source which is connected to the dc side of the interfaced converter. It can be seen that, the line switching functions have been used instead of line-to-line switching functions for the switching model in figure 4.1.

4.3.1 Synchronous Reference Frame Control

The synchronous reference frame or the Park transformation system maps the three-phase current and voltage components in the abc phases into the current and voltage components on the dq0 reference frame. The Park variables transformation matrix applied to three-phase voltages and currents components is shown below in matrix form as:

$$T_{dq0}^{abc} = \frac{2}{3}\begin{bmatrix} \cos\theta & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3} \\ \sin\theta & sin(\theta - \frac{2\pi}{3}) & sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{4.1}$$

where θ is the rotating coordinate angle, which can be chosen as constant or linear time-varying for different objectives. The inverse matrix of (4.1) is calculated by (4.2).

$$T_{abc}^{dq0} = (T_{dq0}^{abc})^{-1} = (T_{dq0}^{abc})^{T} = \frac{2}{3}\begin{bmatrix} \cos\theta & \sin\theta & \frac{1}{2} \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & \frac{1}{2} \\ \cos(\theta + \frac{2\pi}{3} & \sin(\theta + \frac{2\pi}{3}) & \frac{1}{2} \end{bmatrix} \tag{4.2}$$

We define the Park transformed variables X^{dq0} of a three-phase abc signal X^{abc} as:

$$X^{dq0} = T_{dq0}^{abc} X^{abc} \tag{4.3}$$

As mentioned in previous section, by use of synchronous reference frame control, the grid current and voltage components transform into a reference frame that rotates synchronously with the grid voltage. By means of this technique, the control variables values become dc values; thus, filtering and controlling can be achieved easily. As an example, a simple schematic diagram of the synchronous reference frame control is shown in figure 4.2, [99]. As shown in this model, the dc side voltage is controlled and regulated in accordance to the necessary output power of converter in ac side. It can be seen that, its output is the reference current for the circuit of active current controller, whereas the reference current for the reactive current is usually set to zero, if the reactive power control is not allowed. On the other hand, in the case that the reactive power has to be controlled in structure of the proposed model, a reactive power reference must be imposed to the control loop.

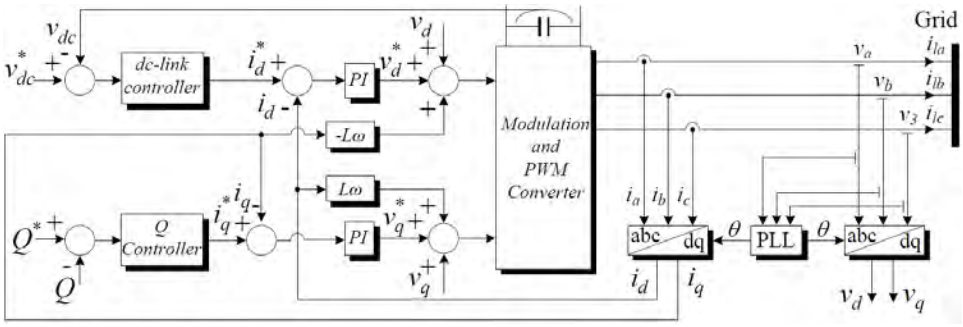


Figure 4.2: General schematic diagram for dq control structure

The dq control scheme is generally associated with proportional-integral (PI) controller since it has an acceptable behaviour when regulating dc variable components. The matrix transfer function of the controller in dq coordinates can be expressed as:

$$G_{PI}^{dq}(s) = \begin{bmatrix} k_p + \dfrac{k_i}{s} & 0 \\ 0 & k_p + \dfrac{k_i}{s} \end{bmatrix} \tag{4.4}$$

where k_p is the proportional gain and k_i is the integral gain of the PI controller.

4.3.2 Stationary Reference Frame Control

The Stationary reference frame or the Clarke transformation system maps the three-phase instantaneous current and voltage components in the abc phases into the instantaneous current and voltage components on the $\alpha\beta 0$ reference frame [98]. The Clarke variable transformation matrix of three-phase components is defined as:

$$T_{\alpha\beta 0}^{abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} \dfrac{1}{\sqrt{2}} & \dfrac{1}{\sqrt{2}} & \dfrac{1}{\sqrt{2}} \\ 1 & -\dfrac{1}{2} & -\dfrac{1}{2} \\ 0 & \dfrac{\sqrt{3}}{2} & -\dfrac{\sqrt{3}}{2} \end{bmatrix} \tag{4.5}$$

The inverse matrix of (4.5) can be expressed as:

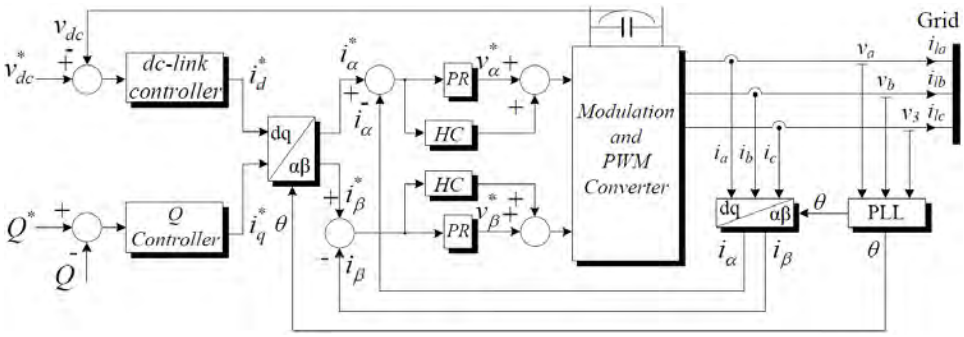


Figure 4.3: General schematic diagram for $\alpha\beta$ frame control strategy

$$T_{abc}^{\alpha\beta 0} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{4.6}$$

We define the Clarke transformed variables $Y^{\alpha\beta 0}$ of a three-phase abc signal Y^{abc} as:

$$Y^{\alpha\beta 0} = T_{\alpha\beta 0}^{abc} Y^{abc} \tag{4.7}$$

Stationary reference frame is a strong tool for structuring control circuit loops in converter-based DG system. As an example, a simple schematic diagram of the stationary reference frame control is shown in figure 4.3. By application of the $abc \longrightarrow \alpha\beta$ module, the grid current and voltage components are transformed into stationary reference frame. Therefore, the control variables are sinusoidal in this case. Some controllers such as proportional resonant (PR) controller gained a large popularity in the last decade in current regulation of grid-connected systems [99].

4.4 Calculation of Reference Currents for the DG Control Loop

Figure 4.4 shows the voltage and current components vectors of DG model which shown in figure 4.1, in stationary and rotating synchronous reference

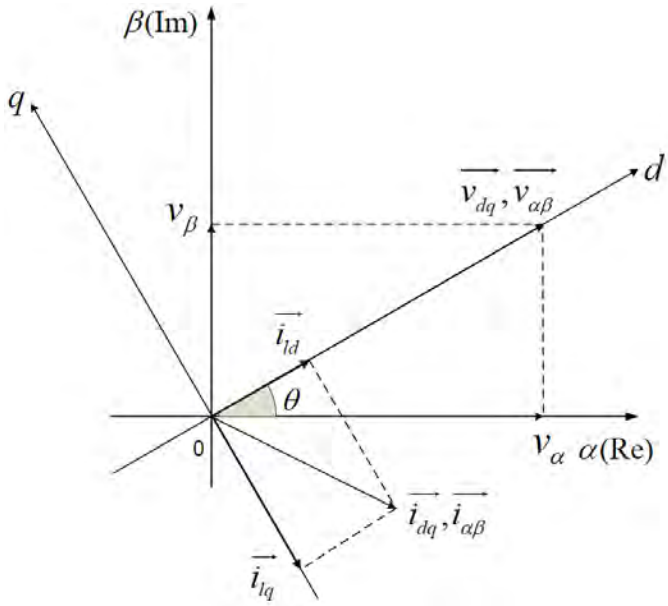


Figure 4.4: Voltage and current components in stationary and rotating synchronous reference frame

frames.

The transformed voltage and current components from $\alpha\beta$ to dq for a three-phase balanced system are obtained by:

$$\begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} = T_{dq}^{\alpha\beta} \begin{bmatrix} i_{l\alpha} \\ i_{l\beta} \end{bmatrix} \tag{4.8}$$

$$\begin{bmatrix} v_{ld} \\ v_{lq} \end{bmatrix} = T_{dq}^{\alpha\beta} \begin{bmatrix} v_{l\alpha} \\ v_{l\beta} \end{bmatrix} \tag{4.9}$$

where

$$T_{dq}^{\alpha\beta} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}$$

is transformation matrix ($\alpha\beta$/dq) which is based on park equations, i_{ld} and i_{lq} are direct and quadrature current components in rotating synchronous reference frame respectively; and θ is the instantaneous angle of load voltage or voltage at the PCC. Using the two-axis power theory [98], the injected instantaneous active and reactive power components of load can be obtained as a function of the instantaneous voltage and current components. The

instantaneous complex of load power (S_l) is defined as the product of the load voltage vector (V_l), and the conjugate of the load current vector (I_l*), given in the form of complex numbers. According to figure 4.4, and considering the instantaneous complex value of load power will be obtained by:

$$S = VI^* = P_L + jQ_L = \frac{3}{2}(v_d + jv_q)(i_{ld} - ji_{lq}) \tag{4.10}$$

$$S = \frac{3}{2}(v_d i_{ld} + v_q i_{lq}) + j(v_q i_{ld} - v_d i_{lq}) \tag{4.11}$$

$$P_L = \frac{3}{2}(v_d i_{ld} + v_q i_{lq}) \tag{4.12}$$

$$Q_L = \frac{3}{2}(v_q i_{ld} - v_d i_{lq}) \tag{4.13}$$

Equation (4.10) shows the total active and reactive powers injected from power grid to supply the grid-connected loads. Considering the power balance of the ac side of the converter, injected power from converter to the grid will be obtained by:

$$P_c = \frac{3}{2}(v_{Md}^{ss} i_{cd}^{ss} + v_{Mq}^{ss} i_{cq}^{ss}) = 3Re\{V_M I_c\} \tag{4.14}$$

$$Q_c = \frac{3}{2}(v_{Mq}^{ss} i_{cd}^{ss} - v_{Md}^{ss} i_{cq}^{ss}) = 3Im\{V_M I_c\} \tag{4.15}$$

Whilst for the grid connection point of the converter inductances we have:

$$P_z = \frac{3}{2}(v_{Md}^{ss} i_{zd}^{ss} + v_{Mq}^{ss} i_{zq}^{ss}) = 3Re\{V_M I_z\} \tag{4.16}$$

$$Q_z = \frac{3}{2}(v_{Mq}^{ss} i_{zd}^{ss} - v_{Md}^{ss} i_{zq}^{ss}) = 3Im\{V_M I_z\} \tag{4.17}$$

where different between S_c and S_z shows the losses caused by interfacing impedances between converter and power grid. Considering the reference voltage vector in direction of d-axis vector in this transformation, the vertical component of the load voltage (q-component of voltage) in the rotating synchronous reference frame is always zero (v_q=0). As shown in figure 4.4, instantaneous angle of load voltage can be calculated as:

$$\theta = tan^{-1}\frac{v_\beta}{v_\alpha} \tag{4.18}$$

In other word, if we consider the instantaneous angle of load voltage by (4.18), the reference voltage vector will be in direction of d-axis vector of

load voltage, and q-axis vector of load voltage will be zero (v_q=0) [10]. According to figure 4.4, d-component of load voltage in stationary and rotating synchronous reference frame can be calculated as:

$$v_d = |\overrightarrow{v_{dq}}| = |\overrightarrow{v_{\alpha\beta}}| = \sqrt{v_\alpha^2 + v_\beta^2} \tag{4.19}$$

In real system, the term v_d shows the magnitude of the voltage at the PCC.

In the next stage, injected current components of DG link to the power grid must be calculated according to the objectives of integrated system. For achieving this purpose, it is necessary to measure the load currents, and then transformed from abc frame to synchronously rotating reference frame, i.e., in dq components. By taking into considering i_{l1}=-(i_{l2}+i_{l3}) , and substituting (4.5) in (4.8), d and q-axis of load currents can be expressed as:

$$\begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} = \sqrt{2} \begin{bmatrix} \sin(\theta + \frac{\pi}{3}) & \sin\theta \\ \cos(\theta + \frac{\pi}{3}) & \cos\theta \end{bmatrix} \begin{bmatrix} i_{l1} \\ i_{l2} \end{bmatrix} \tag{4.20}$$

By (4.20), d and q-components of current in rotating synchronous reference frame can be calculated by means of current components in 123 variable system.

4.4.1 Calculation of Reference Current to Supply Load Active Power in Fundamental Frequency

As mentioned in previous section, in fundamental frequency (first harmonic), the active power injected from VSC to the power grid will be obtained by:

$$P_L = \frac{3}{2}(v_d I_{cd} + v_q I_{cq}) \tag{4.21}$$

where capital letter are related to fundamental frequency of current components. Also, terms of v_d and v_q are the voltage components in fundamental frequency at the PCC. According to the assumption mentioned in previous section regarding v_q=0, d-component of reference current to provide active current in fundamental frequency can be calculated by:

$$I_{cd}^* = \frac{2P_{ref}}{3v_d} \tag{4.22}$$

where P_{ref} is the power that VSC must provide and inject in fundamental frequency by connection of DG resources to the power grid. I_{cd}^* is the d-component reference current of DG link in fundamental frequency which

will be considered in current control circuit loop of DG system. Calculation of d-component of reference current with this method, and considering maximum capability of interfaced converter and DG resources makes it possible to control the maximum active power delivered to the power grid via DG resources and interface system by changing reference active power. Considering the physical constraints, the preceding model is subjected to the following limits. The injected current from DG to the power grid is limited to the maximum continuous current of the interfaced converter or to the maximum available current of the converter in a limited short-time operation. In addition, the load voltage is limited to the maximum available output voltage of the converter, depending on the dc-link voltage value. Since the power grid is uncertain and dynamic in nature and its parameters vary frequently due to factors such as cable overload, transformer saturation, and temperature effects, the uncertainty in system parameters should be considered in control system design.

4.4.2 Calculation of harmonic components of reference current of d-axis

Calculation of the load current in the dq reference frame by (4.20) makes it possible to separate fundamental and harmonic current components. d-component of the load current (i_{ld}) can be separated into dc and alternative current components as:

$$i_{ld} = \tilde{i_{ld}} + I_{ld} \tag{4.23}$$

where $\tilde{i_{ld}}$ is alternative d-component of load current in rotating synchronous reference frame which is related to harmonic components of load current and I_{ld} is the dc term of load current in this frame which is related to fundamental frequency of load current. To compensate harmonic current it is necessary to separate alternative and constant current components. For this purpose, a high pass filter (HPF) must be used. To minimize the influence of the HPF's phase responses, by means of a low-pass filter (LPF), a minimal phase high pass filter (MPHPF) can be obtained, the transfer function of this LPF has order and cut-off frequency the same as HPF. Therefore, the proposed MPHPF can be achieved simply by the difference between the input current signal and the filtered current, which is equivalent to performing:

$$H_{MPHPF}(s) = 1 - H_{LPF}(s) \tag{4.24}$$

A double-precision low-pass filter using the Chebyshev type-I fourth order low-pass filter is used for this purpose. The filter considered has a cut-off frequency $f_c = \frac{f}{2}(f = 50Hz)$ which promises the elimination of dc components in the non-linear load currents. Therefore, the harmonic components of load current at d-axis are obtained. To use the proposed distributed generation technology based on renewable energy resources as an active filter device in the proposed system, harmonic current components of load current must be supplied. For this purposes d-component of non-linear link reference current is achieved by doing the sum of currents in (4.22) and alternative terms of load current in (4.23):

$$i^*_{cd} = \tilde{i_{ld}} + I^*_{cd} \tag{4.25}$$

4.4.3 Calculation of Reference Current to Supply Load Reactive Power

As shown in figure 4.4, in a rotating synchronous reference frame, q-component of load current is perpendicular on d-component of load voltage ($v_d \perp i_{lq}$). Therefore, q-component of load current indicates required reactive power of the grid-connected loads. To compensate load reactive power, VSC must injects a current with q-component equal to i_{lq}. For this purpose, it is sufficient to set q-component of reference current in circuit loop of proposed control strategy equal to q-component of the load current as shown in (4.26).

$$i^*_{cq} = i_{lq} \tag{4.26}$$

where i^*_{cq} is the vertical component of DG link reference current that is shown. By this consideration, reactive current of grid-connected loads is compensated in fundamental frequency and harmonic reactive currents can also be provided by DG system [100]. These obtained reference currents will then be fed to a feedback current controller which will compare the desired currents with the measured one and will calculate the current component values to be applied to the power grid through PWM modulation of the dc bus voltage.

4.5 Dynamic Models of Multilevel Converter Based System

Schematic diagram of the proposed model based on multilevel converter topology is shown in figure 4.1. For the purposes of this dissertation, the electric power system grid is composed of the generation system, the transmission or, the distribution system, and the loads. The DG resources and additional components are represented as a dc current source connected to the dc side of the converter. To draw an appropriate plan to control the integration of DG resources to the power grid, a dynamic analytical model of the proposed power system should be developed.

4.5.1 Phase Model Analaysis of Proposed Multilevel Converter Based Model

Kirchoff's laws of voltages and currents applied to the DG model in figure 4.1, provide three differential equations in the stationary abc (123) reference frame as [101]

$$v_{1M} = L_c \frac{di_{c1}}{dt} + R_c i_{c1} + v_1 + v_{NM} \tag{4.27}$$

$$v_{2M} = L_c \frac{di_{c2}}{dt} + R_c i_{c2} + v_2 + v_{NM} \tag{4.28}$$

$$v_{3M} = L_c \frac{di_{c3}}{dt} + R_c i_{c3} + v_3 + v_{NM} \tag{4.29}$$

or it can be mentioned as:

$$v_{iM} = L_c \frac{di_{ci}}{dt} + R_c i_{ci} + v_i + v_{NM} \qquad i = 1, 2, 3 \tag{4.30}$$

where v_{iM} is the voltage between the converter terminals and the dc bus neutral, v_{NM} is the voltage of the neutral point, v_i is the voltage of the power grid or load voltage, i_{ci} is converter current, L_c and R_c are total inductance and resistance of interfacing system and isolation transformer. Summation of three equations in (4.27)-(4.29), it gives,

$$\sum_{i=1}^{3} v_{iM} = \sum_{i=1}^{3} (L_c \frac{di_c}{dt} + R_c i_{ci} + v_i + v_{MN}) \qquad i = 1, 2, 3 \tag{4.31}$$

A null value for the zero voltage component is assumed. Since the absence of neutral wire is considered, the zero current component is also null, and with the assumption that the ac source voltages are balanced, the following relation is obtained from (4.31).

$$(v_{1M}+v_{2M}+v_{3M}) = L_c\frac{d}{dt}(i_{c1}+i_{c2}+i_{c3}) + R_c(i_{c1}+i_{c2}+i_{c3}) + (v_1+v_2+v_3) + 3v_{NM} \tag{4.32}$$

Then ac neutral point voltage term (v_{NM}) can be obtained as:

$$v_{NM} = \frac{(v_{1M}+v_{2M}+v_{3M})}{3} = \frac{1}{3}\sum_{i=1}^{3} v_{iM} = \frac{1}{3}F(S_i).v_c \tag{4.33}$$

As shown in (4.33), the value of v_{NM} is depended to switching states of converter and voltage of dc side of converter.

By referring to the (4.27)-(4.29), a first-order matrix equation will be obtained which describes the ac side of the proposed multilevel based converter model, such that:

$$\frac{d}{dt}\begin{bmatrix} i_{c1} \\ i_{c2} \\ i_{c3} \end{bmatrix} = \frac{-R_c}{L_c}\begin{bmatrix} i_{c1} \\ i_{c2} \\ i_{c3} \end{bmatrix} - \frac{1}{L_c}\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} + \frac{1}{L_c}\begin{bmatrix} v_{1M} \\ v_{2M} \\ v_{3M} \end{bmatrix} - \frac{1}{L_c}\begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} v_{NM} \tag{4.34}$$

where (4.34) can be written as:

$$\frac{di_{ci}}{dt} = -\frac{R_c}{L_c}i_{ci} - \frac{1}{L_c}v_i + \frac{1}{L_c}v_{iM} - \frac{1}{L_c}U_3 v_{NM} \qquad i = 1,2,3 \tag{4.35}$$

The symbol U_3 in (4.35) is a conventional notation that defines for $[1\ 1\ 1]^T$. Figure 4.5 shows the dc side of multilevel converter which has been introduced as proposed model for interfacing between the DG resources and the power grid in figure 4.1. The following equation describes the current components through the cascaded capacitors in the dc side of the interfaced converter.

$$i_{cj} = c\frac{dv_{cj}}{dt} = i_{dc} - (i_1 + i_2 + ... + i_{n-1}) = i_{dc} - \sum_{k=j}^{n-1} i_k \tag{4.36}$$

or can be written as:

$$\frac{d}{dt}v_c = \frac{1}{c}U_{n-1}i_{dc} - \frac{1}{c}K_{NC}i_{NC} \tag{4.37}$$

where v_c, i_{NC}, and K_{NC} are defined as:

$$v_c = \begin{bmatrix} v_{c(n-1)} \\ v_{c(n-2)} \\ . \\ . \\ . \\ v_{c2} \\ v_{c1} \end{bmatrix}, K_{NC} = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ 1 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & 1 & \cdots & 1 & 0 \\ 1 & 1 & \cdots & 1 & 1 \end{bmatrix} and \quad i_{NC} = \begin{bmatrix} i_{n-1} \\ i_{n-2} \\ . \\ . \\ . \\ i_2 \\ i_1 \end{bmatrix} \tag{4.38}$$

Equations (4.35) and (4.37) present the total system equations expected for the switching stage of proposed model. The control functions of each single-pole n-throw switch can tie in current and voltage components between the ac side and the dc side of the converter as,

$$v_{iM} = S_{ci}v_c; \quad K_{NC}i_{NC} = S_{ci}^T i_{ci} \qquad i = 1, 2, 3 \tag{4.39}$$

As mentioned in previous chapter about switching states of multilevel converter topologies, and by considering the proposed DG model, the three-phase output voltage of multilevel converter will be obtained by:

$$v_{1M} = (S_{a(n-1)})v_{c(n-1)} + (S_{a(n-1)} + S_{a(n-2)})v_{c(n-2)} + ...+ (S_{a(n-1)} + S_{a(n-2)+...+S_{a2}+S_{a1}})v_{c1} \tag{4.40}$$

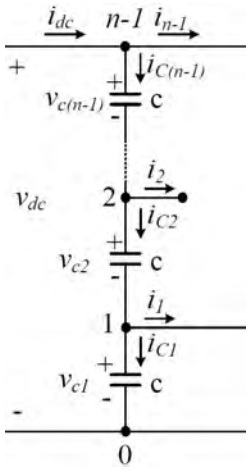


Figure 4.5: dc side of the proposed converter model

$$v_{2M} = (S_{b(n-1)})v_{c(n-1)} + (S_{b(n-1)} + S_{b(n-2)})v_{c(n-2)} + ...+ (S_{b(n-1)} + S_{b(n-2)+...+S_{b2}+S_{b1}})v_{c1} \tag{4.41}$$

$$v_{3M} = (S_{c(n-1)})v_{c(n-1)} + (S_{c(n-1)} + S_{c(n-2)})v_{c(n-2)} + ...+ (S_{c(n-1)} + S_{c(n-2)+...+S_{c2}+S_{c1}})v_{c1} \tag{4.42}$$

By comparison between equations (4.40-4.42) and equation (4.39), the switching matrix for a three-phase n-level diode-clamped converter topology for proposed DG model will be defined as:

$$S_{ci} = \begin{bmatrix} S_{a(n-1)} & S_{a(n-1)} + S_{a(n-2)} & \cdots & \sum_{i=2}^{n-1} S_{ai} & \sum_{i=1}^{n-1} S_{ai} \\ S_{b(n-1)} & S_{b(n-1)} + S_{b(n-2)} & \cdots & \sum_{i=2}^{n-1} S_{bi} & \sum_{i=1}^{n-1} S_{bi} \\ S_{c(n-1)} & S_{c(n-1)} + S_{c(n-2)} & \cdots & \sum_{i=2}^{n-1} S_{ci} & \sum_{i=1}^{n-1} S_{ci} \end{bmatrix} \tag{4.43}$$

By substituting (4.39) into (4.35) and (4.37), a general model of dynamic equations which describing the switching state model of the proposed multilevel converter based model is developed in (4.44) and (4.45). This is a general model and makes no assumptions other than the use of ideal switches in the structure of interfaced converter in DG system.

$$\frac{di_{ci}}{dt} = -\frac{R_c}{L_c}i_{ci} - \frac{1}{L_c}v_i + \frac{1}{L_c}S_{ci}v_c - \frac{1}{L_c}v_{NM} \qquad i = 1, 2, 3 \tag{4.44}$$

$$\frac{d}{dt}v_c = \frac{1}{c}U_{n-1}i_{dc} - \frac{1}{c}S_{ci}^{T}i_{ci} \qquad i = 1,2,3 \tag{4.45}$$

Although these mathematical models can be utilized for simulation modelling of the DG system, the term v_{NM} must be obtained during the simulation analyze, which involves solving for voltage terms v_{1M}, v_{2M}, and v_{3M}. For this case, it is necessary to transform the general equations of proposed model into the synchronous reference frame, which by this technique, the term v_{NM} no longer affects any current components. It occurs because the term v_{NM} is only involved in the homopolar current component equation, which is always zero during absence of neutral wire in the general mathematical model of proposed model. On the other hand, the voltage-balancing process of the cascaded capacitors in dc-side of converter will be performed by the modulation technique; therefore voltage v_{NM} does not provide any useful information for control of interfacing system. This term can be avoided if the converter is modelled from the standpoint of line-to-line components.

By substituting (4.33) in to (4.44), a set of dynamic equations describing the switching model of the proposed multilevel converter based model is developed in (4.46), as:

$$\frac{di_{ci}}{dt} = -\frac{R_c}{L_c}i_{ci} - \frac{1}{L_c}v_i + \frac{1}{L_c}(S_{ci} - \frac{1}{3}F(S_i))v_c \qquad i = 1,2,3 \tag{4.46}$$

Equation (4.46) represents phase i dynamic equation of the proposed multilevel converter based model. By this mathematical model, switching state function D_{ni} can be defined as:

$$D_{ni} = (S_{ci} - \frac{1}{3}F(S_i)) \qquad i = 1,2,3 \tag{4.47}$$

which is shows the value of D_{ni} depends simultaneously on the switching functions of the three legs of the interfaced multilevel converter. This shows the relation between the three phases in proposed model. By substituting (4.47) into (4.46), dynamic equations of the interfaced multilevel converter based model can be written as (4.48).

$$\frac{d}{dt}\begin{bmatrix} i_{c1} \\ i_{c2} \\ i_{c3} \end{bmatrix} = \frac{-R_c}{L_c}\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} i_{c1} \\ i_{c2} \\ i_{c3} \end{bmatrix} + \frac{1}{L_c}\begin{bmatrix} D_{n1} \\ D_{n2} \\ D_{n3} \end{bmatrix} v_c - \frac{1}{L_C}\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \tag{4.48}$$

Considering $i_{c1} + i_{c2} + i_{c3} = 0$, and a three-phase balanced voltage for the power grid, the general current dynamics equations of the proposed multilevel converter based model can be reasonably represented by the following equations:

$$\frac{d}{dt}\begin{bmatrix} i_{c1} \\ i_{c2} \end{bmatrix} = \begin{bmatrix} \frac{-R_c}{L_c} & 0 \\ 0 & \frac{-R_c}{L_c} \end{bmatrix}\begin{bmatrix} i_{c1} \\ i_{c2} \end{bmatrix} + \frac{1}{L_c}\begin{bmatrix} D_{n1} \\ D_{n2} \end{bmatrix} v_c - \frac{1}{L_C}\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{4.49}$$

Equation (4.49) is a general equation model which defines dynamic model of the DG model based on multilevel converter topologies.

4.5.2 Line-to-Line Model of Proposed Multilevel Converter Based Model

For line-to-line analyze of multilevel converter based model of figure 4.1, the voltage and current components of the consecutive equations in (4.27-4.29) are subtracted from each other, thus, the line-to-line model can be expressed as:

$$\begin{aligned} v_{12M} = v_{1M} - v_{2M} &= L_c\frac{d(i_{c1} - i_{c2})}{dt} + R_c(i_{c1} - i_{c2}) + (v_1 - v_2) \\ &= L_c\frac{di_{c12}}{dt} + R_c i_{c12} + v_{12} \end{aligned} \tag{4.50}$$

$$\begin{aligned} v_{23M} = v_{2M} - v_{3M} &= L_c\frac{d(i_{c2} - i_{c3})}{dt} + R_c(i_{c2} - i_{c3}) + (v_2 - v_3) \\ &= L_c\frac{di_{c23}}{dt} + R_c i_{c23} + v_{23} \end{aligned} \tag{4.51}$$

$$\begin{aligned} v_{31M} = v_{3M} - v_{1M} = L_c \frac{d(i_{c3} - i_{c1})}{dt} + R_c(i_{c3} - i_{c1}) + (v_3 - v_1) \\ = L_c \frac{di_{c31}}{dt} + R_c i_{c31} + v_{31} \end{aligned} \tag{4.52}$$

As shown in equations(4.50-4.52), the term of ac neutral point voltage has eliminated from the dynamic model equations of proposed DG model. By mathematical analysing in a way similar to that for the phase model of proposed model, the final equations of the line-to-line model of proposed multilevel converter based model can be expressed as:

$$\frac{d}{dt} i_{LL} = -\frac{R_c}{L_c} i_{cLL} - \frac{1}{L_c} v_{LL} + \frac{1}{L_c} S_{LL} v_c \tag{4.53}$$

And the dc side of the proposed model is obtained as:

$$\frac{d}{dt} v_c = \frac{1}{c} U_{n-1} i_{dc} - \frac{1}{3c} S_{LL}^T i_{LL} \tag{4.54}$$

where S_{LL} is the switching matrix of DG model which is calculated by subtracting the switching matrix of phase model, i_{LL}, and v_{LL} are line currents and voltages which are defined as:

$$S_{LL} = \begin{bmatrix} S_{ab(n-1)} & S_{ab(n-1)} + S_{ab(n-2)} & \cdots & \sum_{i=2}^{n-1} S_{abi} & \sum_{i=1}^{n-1} S_{abi} \\ S_{bc(n-1)} & S_{bc(n-1)} + S_{bc(n-2)} & \cdots & \sum_{i=2}^{n-1} S_{bci} & \sum_{i=1}^{n-1} S_{bci} \\ S_{ca(n-1)} & S_{ca(n-1)} + S_{ca(n-2)} & \cdots & \sum_{i=2}^{n-1} S_{cai} & \sum_{i=1}^{n-1} S_{cai} \end{bmatrix},$$
$$i_{LL} = \begin{bmatrix} i_{12} \\ i_{23} \\ i_{31} \end{bmatrix}, \quad and \quad v_{LL} = \begin{bmatrix} v_{12} \\ v_{23} \\ v_{31} \end{bmatrix} \tag{4.55}$$

In addition, S_{ijk}=S_{ik}-S_{jk}; $i, j = [a, b, c]$; and $k = [1, 2, ..., n-1]$.
The number three in (4.54) can be calculated as:

$$i_p = \frac{1}{3}(S_{abp} i_{12} + S_{bcp} i_{23} + S_{cap} i_{31}) \quad with \quad p = [1, 2, 3, ..., n-1] \tag{4.56}$$

which can be indicated from following equation.

$$i_p = S_{ap} i_1 + S_{bp} i_2 + S_{cp} i_3 \quad and \quad i_1 + i_2 + i_3 = 0 \tag{4.57}$$

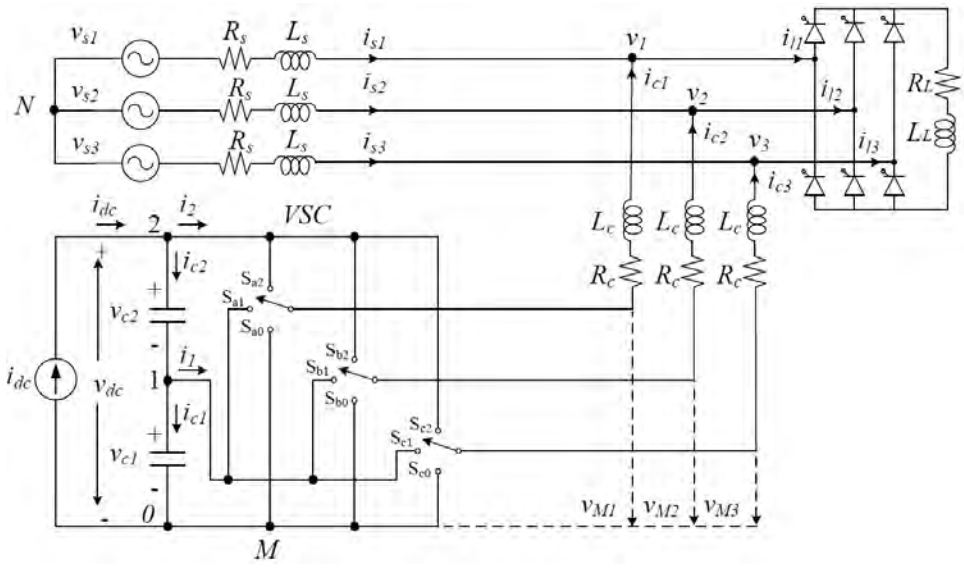


Figure 4.6: Proposed DG model based on three-level NPC converter

4.6 Three-Level Converter Based System

In this section, the general equations of multilevel converter based system which obtained in previous subsections will be applied to a three-level case study model. For this case, a three-level NPC converter is considered, for the interfacing system between DG resources and power grid. Figure 4.6 shows the schematic diagram of the DG model which is based on three-level NPC converter. Conventional signs of currents and voltages are also indicated. In addition, the DG source and additional components are represented as a dc current source which is connected to the dc side of the interfaced converter.

4.6.1 Phase Model Based on Three-level NPC Converter

The general phase model equations (4.44) and (4.45) of proposed DG model based on multilevel converters are now applied to a three-level NPC converter (n=3). The ac side and dc side equations of this model can be obtained as:

$$\frac{di_{ci}}{dt} = -\frac{R_c}{L_c} i_{ci} - \frac{1}{L_c} v_i + \frac{1}{L_c} S_{ci3L} v_{c3L} - \frac{1}{L_c} U_3 v_{NM} \qquad i = 1, 2, 3 \tag{4.58}$$

$$\frac{d}{dt}v_{c3L} = \frac{1}{c}U_2 i_{dc} - \frac{1}{c}S_{ci3L}^T i_{ci} \qquad i = 1, 2, 3 \tag{4.59}$$

where, the voltages of cascaded dc capacitors and the switching matrix for the NPC converter (n=3) are calculated as:

$$v_{c3L} = \begin{bmatrix} v_{c2} \\ v_{c1} \end{bmatrix} \tag{4.60}$$

and

$$S_{ci3L} = \begin{bmatrix} S_{a2} & S_{a2} + S_{a1} \\ S_{b2} & S_{b2} + S_{b1} \\ S_{c2} & S_{c2} + S_{c1} \end{bmatrix} \tag{4.61}$$

Since each single-pole three-throw switch only can take one position at any time,

$$\begin{aligned} S_{a0} + S_{a1} + S_{a2} &= 1 \\ S_{b0} + S_{b1} + S_{b2} &= 1 \\ S_{c0} + S_{c1} + S_{c2} &= 1 \end{aligned} \tag{4.62}$$

Therefore, the switching matrix for a three-level base model can be expressed as:

$$S_{ci3L} = \begin{bmatrix} S_{a2} & 1 - S_{a0} \\ S_{b2} & 1 - S_{b0} \\ S_{c2} & 1 - S_{c0} \end{bmatrix} \tag{4.63}$$

By substituting the switching matrix of proposed model in (4.63) into (4.58) and (4.62):

$$S_{ci3L} v_{c3L} = \begin{bmatrix} S_{a2} & -S_{a0} \\ S_{b2} & -S_{b0} \\ S_{c2} & -S_{c0} \end{bmatrix} \begin{bmatrix} v_{c2} \\ v_{c1} \end{bmatrix} + U_2 v_{c1} \tag{4.64}$$

$$S_{ci}^T i_{ci} = \begin{bmatrix} S_{a2} & S_{b2} & S_{c2} \\ -S_{a0} & -S_{b0} & -S_{c0} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{4.65}$$

Therefore, the general equations of dc side and ac side of the proposed DG model based on three-level NPC converter can be expressed as:

$$\frac{di_{ci}}{dt} = -\frac{R_c}{L_c} i_{ci} - \frac{1}{L_c} v_i + \frac{1}{L_c} S_{ci3L} v_{c3L} - \frac{1}{L_c} U_3 (v_{NM} - v_{c1}) \qquad i = 1, 2, 3 \tag{4.66}$$

$$\frac{d}{dt} v_{c3L} = \frac{1}{c} U_2 i_{dc} - \frac{1}{c} S_{ci3L}^T i_{ci} \qquad i = 1, 2, 3 \tag{4.67}$$

Therefore, the new switching matrix of DG model which is based on phase model of the three-level NPC converter, can be expressed as:

$$S_{ci3L} = \begin{bmatrix} S_{a2} & -S_{a0} \\ S_{b2} & -S_{b0} \\ S_{c2} & -S_{c0} \end{bmatrix} \tag{4.68}$$

Referring the AC NP potential ("N") with the NP of the dc-link ("1"), the general equation of ac side of the proposed DG model based on three-level NPC converter (4.66) can be expressed as:

$$\frac{di_{ci}}{dt} = -\frac{R_c}{L_c} i_{ci} - \frac{1}{L_c} v_i + \frac{1}{L_c} S_{ci3L} v_{c3L} - \frac{1}{L_c} U_3 v_{NM} \qquad i = 1, 2, 3 \tag{4.69}$$

This model is general, complete and makes no assumptions other than the use of ideal switches, for the DG model based on three-level converter.

4.6.2 Line-to-Line Model Based on Three-level NPC Converter

The general equations of the line-to-line model of proposed multilevel converter based system are applied now to the three-level NPC converter (n=3) which is shown in figure 4.6. According to the (4.44) and (4.5), the ac side and dc side equations of this model are obtained as:

$$\frac{di_{LL}}{dt} = -\frac{R_c}{L_c} i_{LL} - \frac{1}{L_c} v_{LL} + \frac{1}{L_c} S_{LL3L} v_{c3L} \tag{4.70}$$

$$\frac{d}{dt} v_{c3L} = \frac{1}{c} U_2 i_{dc} - \frac{1}{3c} S_{LL3L}^T i_{LL} \tag{4.71}$$

According to (4.38) and (4.55) dc voltage of converter and switching matrix for the three-level converter (n=3) are obtained by:

$$v_{c3L} = \begin{bmatrix} v_{c2} \\ v_{c1} \end{bmatrix} \tag{4.72}$$

and

$$S_{LL3L} = \begin{bmatrix} S_{ab2} & S_{ab2} + S_{ab1} \\ S_{bc2} & S_{bc2} + S_{bc1} \\ S_{ca2} & S_{ca2} + S_{ca1} \end{bmatrix} \tag{4.73}$$

If the switching matrix is preferred to contain switching functions of the higher and lower connection poles ("2" and "0" subscripts), it can be obtained as:

$$S_{LL3L} = \begin{bmatrix} S_{ab2} & -S_{ab0} \\ S_{bc2} & -S_{bc0} \\ S_{ca2} & -S_{ca0} \end{bmatrix} \tag{4.74}$$

4.7 Control Model of the Proposed DG Model

The large-signal and small-signal mathematical equations and small-signal circuit model of the DG model based on three-level converter are developed in this section so that proper control circuit loops can be designed for the DG model. The control model which is presented in this section mainly is based on the phase model of proposed DG model, but it could be based on the line-to-line model of proposed model without significant differences.

4.7.1 State-Space Model of Proposed DG Model

In order to facilitate the performance of proposed control strategy, and simplifying as much as possible the study of proposed DG model equations, usually the Park transformation matrix is applied to the variables, allowing to suppress one of the equations during absence of neutral wire, and also transforming the time varying sinusoidal signals in steady state in constants if the right parameters of the transformation are chosen. By use of Park transformation matrix, the dynamic model of proposed model can be transformed to the synchronous orthogonal frame rotating at the grid angular frequency, ω, where all ac variables become dc variables; thus, filtering and controlling can be easier achieved. From (4.34) the ac side of proposed model can be extended as:

$$\frac{d}{dt}\begin{bmatrix} i_{c1} \\ i_{c2} \\ i_{c3} \end{bmatrix} = \begin{bmatrix} \frac{-R_c}{L_c} & 0 & 0 \\ 0 & \frac{-R_c}{L_c} & 0 \\ 0 & 0 & \frac{-R_c}{L_c} \end{bmatrix} \begin{bmatrix} i_{c1} \\ i_{c2} \\ i_{c3} \end{bmatrix} + \begin{bmatrix} \frac{-1}{L_c} & 0 & 0 \\ 0 & \frac{-1}{L_c} & 0 \\ 0 & 0 & \frac{-1_c}{L_c} \end{bmatrix} \begin{bmatrix} v_1 - v_{1M} \\ v_2 - v_{2M} \\ v_3 - v_{3M} \end{bmatrix} + \begin{bmatrix} \frac{-1}{L_c} \\ \frac{-1}{L_c} \\ \frac{-1}{L_c} \end{bmatrix} v_{NM} \tag{4.75}$$

By transforming general dynamic equation of the proposed multilevel based model (4.75) into the rotating reference frame according to the dq0 transformation by applying the coordinate transformation to (4.75) the following is obtained:

$$\frac{d}{dt}\left[T_{123}^{dq0}\begin{bmatrix} i_{c1} \\ i_{c2} \\ i_{c3} \end{bmatrix}\right] = \begin{bmatrix} \frac{-R_c}{L_c} & 0 & 0 \\ 0 & \frac{-R_c}{L_c} & 0 \\ 0 & 0 & \frac{-R_c}{L_c} \end{bmatrix} T_{123}^{dq0}\begin{bmatrix} i_{cd} \\ i_{cq} \\ i_{c0} \end{bmatrix} + \begin{bmatrix} \frac{-1}{L_c} & 0 & 0 \\ 0 & \frac{-1}{L_c} & 0 \\ 0 & 0 & \frac{-1_c}{L_c} \end{bmatrix} T_{123}^{dq0}\begin{bmatrix} v_1 - v_{1M} \\ v_2 - v_{2M} \\ v_3 - v_{3M} \end{bmatrix} + T_{123}^{dq0}\begin{bmatrix} \frac{-1}{L_c} \\ \frac{-1}{L_c} \\ \frac{-1}{L_c} \end{bmatrix} v_{NM} \tag{4.76}$$

and considering the matrix differential property:

$$\frac{d}{dt}\left[T_{123}^{dq0}[i_{cdq0}]\right] = T_{123}^{dq0}\frac{d}{dt}[i_{cdq0}] + [\frac{d}{dt}T_{123}^{dq0}][i_{cdq0}] \tag{4.77}$$

Therefore, the general current and voltage dynamics model of proposed DG model in Park's d-q reference frame can be reasonably represented by the following equations:

$$\frac{d}{dt}\begin{bmatrix} i_{cd} \\ i_{cq} \\ i_{c0} \end{bmatrix} = \begin{bmatrix} \frac{-R_c}{L_c} & \omega & 0 \\ -\omega & \frac{-R_c}{L_c} & 0 \\ 0 & 0 & \frac{-R_c}{L_c} \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \\ i_{c0} \end{bmatrix} + \begin{bmatrix} \frac{-1}{L_c} & 0 & 0 \\ 0 & \frac{-1}{L_c} & 0 \\ 0 & 0 & \frac{-1_c}{L_c} \end{bmatrix} \begin{bmatrix} v_d - v_{dM} \\ v_q - v_{qM} \\ v_0 - v_{0M} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{-\sqrt{3}}{L_c} \end{bmatrix} v_{NM} \tag{4.78}$$

where ω is the grid voltage angular speed, and the transformed voltages and currents components are defined as:

$$\begin{bmatrix} i_{cd} \\ i_{cq} \\ i_{c0} \end{bmatrix} = T_{dq0}^{123} \begin{bmatrix} i_{c1} \\ i_{c2} \\ i_{c3} \end{bmatrix}, \begin{bmatrix} v_{dM} \\ v_{qM} \\ v_{0M} \end{bmatrix} = T_{dq0}^{123} \begin{bmatrix} v_{1M} \\ v_{2M} \\ v_{3M} \end{bmatrix}, and \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = T_{dq0}^{123} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \tag{4.79}$$

where v_{Md}, v_{Mq}, i_{cd}, i_{cq} are the d- and q-axis converter's voltages and currents; L_c is the coupling inductance; R_c is the coupling resistance; and v_d, v_q are the d- and q-axis components of the grid voltage at the PCC.

Since the absence of neutral wire is considered, the zero current component is also null, therefore; there is no homopolar current component (i_{c0}=0), thus, the AC NP voltage (v_{NM}) does not affect any transformed current. This voltage can be deduced from (4.78) as:

$$v_{NM} = \frac{v_0 - v_{0M}}{\sqrt{3}} \tag{4.80}$$

It can be seen that, the voltage v_{NM} (AC NP) only depends on homopolar voltage components of the converter and the power grid. In addition, when the voltage of power grid is balanced, the averaged value of v_0 is zero, therefore; voltage v_{NM} depends only on the homopolar component of the ac voltages of the interfaced converter. Considering the original position of the power grid voltages in d-axis, voltage component of q-axis will be zero (v_q=0), and the other component will be equal to E_L (v_d=E_L), which is the

value of the line-to-line RMS voltage of grid, therefore (4.78) can be written as:

$$\frac{d}{dt}\begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} = \begin{bmatrix} \frac{-R_c}{L_c} & \omega \\ -\omega & \frac{-R_c}{L_c} \end{bmatrix}\begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_c} & 0 \\ 0 & \frac{1}{L_c} \end{bmatrix}\begin{bmatrix} v_{dM} \\ v_{qM} \end{bmatrix} - \frac{1}{L_c}\begin{bmatrix} E_L \\ 0 \end{bmatrix} \tag{4.81}$$

By substituting the switching state functions of the proposed model, the equivalent model of (4.81) can be expressed as:

$$\frac{d}{dt}\begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} = \begin{bmatrix} \frac{-R_c}{L_c} & \omega \\ -\omega & \frac{-R_c}{L_c} \end{bmatrix}\begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \frac{1}{L_c}\begin{bmatrix} D_{nd} \\ D_{nq} \end{bmatrix} v_c - \frac{1}{L_c}\begin{bmatrix} v_d \\ 0 \end{bmatrix} \tag{4.82}$$

where the homopolar components of voltages and currents have been eliminated in both (4.81) and (4.82). On the other hand, from (4.37), the dc side of the proposed multilevel converter based model can be obtained as:

$$\frac{d}{dt}\begin{bmatrix} v_{c(n-1)} \\ v_{c(n-2)} \\ \vdots \\ v_{c2} \\ v_{c1} \end{bmatrix} = \frac{1}{c}\begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \\ 1 \end{bmatrix} i_{dc} - \frac{1}{c}\begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ 1 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 1 & 1 & \cdots & 1 & 0 \\ 1 & 1 & \cdots & 1 & 1 \end{bmatrix}\begin{bmatrix} i_{n-1} \\ i_{n-2} \\ \vdots \\ i_2 \\ i_1 \end{bmatrix} \tag{4.83}$$

To avoid the effects of switching functions, the general equation of the dc side in (4.83) can be related to the ac side (4.81) by the power-balance equation. Taking into account that the dq transformation is power conservative:

$$p = v_{1M}i_{c1} + v_{2M}i_{c2} + v_{3M}i_{c3} = v_{dM}i_{cd} + v_{qM}i_{cq} \tag{4.84}$$

and considering 100% efficiency for the proposed model, the instantaneous power of dc side can be obtained as:

$$\begin{aligned} p = (v_{c1} + v_{c2} + ... + v_{c(n-1)})i_{n-1} + ... + (v_{c2} + v_{c1})i_2 + v_{c1}i_1 \\ = v_{dM}i_{cd} + v_{qM}i_{cq} \end{aligned} \tag{4.85}$$

By making these two power values models equal to each other, current i_{n-1} can be expressed as:

$$i_{n-1} = \frac{(v_{dM}i_{cd} + v_{qM}i_{cq}) - (v_{c1} + v_{c2} + ... + v_{c(n-2)})i_{n-2}}{(v_{c1} + v_{c2} + ... + v_{c(n-1)})} - ... \\ - \frac{(v_{c1} + v_{c2})i_2 + v_{c1}i_1}{(v_{c1} + v_{c2} + ... + v_{c(n-1)})} \tag{4.86}$$

According to figure 4.1, the current through the capacitors in the dc side of the multilevel converter ($i_{c(n-1)}$) is obtained from (4.87):

$$c\frac{dv_{c(n-1)}}{dt} = i_{dc} - i_{n-1} \tag{4.87}$$

Therefore, one of the most important large-signal equations of the proposed DG model can be expressed by (4.88).

$$\frac{dv_{c(n-1)}}{dt} = \frac{i_{dc}}{c} - \frac{(v_{dM}i_{cd} + v_{qM}i_{cq}) - (v_{c1} + v_{c2} + ... + v_{c(n-2)})i_{n-2}}{c(v_{c1} + v_{c2} + ... + v_{c(n-1)})} \\ + ... + \frac{(v_{c1} + v_{c2})i_2 + v_{c1}i_1}{c(v_{c1} + v_{c2} + ... + v_{c(n-1)})} \tag{4.88}$$

The general equation of this multilevel converter based model (4.88) is applied to the three-level converter (n=3). Therefore, the dc side of the DG model based on three-level converter is obtained as:

$$\frac{d}{dt}\begin{bmatrix} v_{c2} \\ v_{c1} \end{bmatrix} = \frac{1}{c}i_{dc} - \frac{1}{c}\begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}\begin{bmatrix} i_2 \\ i_1 \end{bmatrix} \tag{4.89}$$

Like previous part, to avoid switching functions, the equation of the dc side (4.89) can be related to the ac side (4.81) by the power-balance equalization as:

$$p = v_{1M}i_{c1} + v_{2M}i_{c2} + v_{3M}i_{c3} = v_{dM}i_{cd} + v_{qM}i_{cq} \tag{4.90}$$

and by considering efficiency of 100% for this model, the dc side instantaneous power can be expressed as:

$$p = (v_{c1} + v_{c2})i_2 + v_{c1}i_1 = v_{dM}i_{cd} + v_{qM}i_{cq} \tag{4.91}$$

By making these two power values models equal to each other, current i_2 can be obtained as:

$$i_2 = \frac{v_{dM} i_{cd} + v_{qM} i_{cq} - v_{c1} i_1}{v_{c1} + v_{c2}} \tag{4.92}$$

and by substituting this current into (4.89), the voltage changes in cascaded capacitors will be obtained as:

$$\frac{dv_{c2}}{dt} = \frac{i_{dc}}{c} - \frac{(v_{dM} i_{cd} + v_{qM} i_{cq}) - v_{c1} i_1}{c(v_{c1} + v_{c2})} \tag{4.93}$$

$$\frac{dv_{c1}}{dt} = \frac{i_{dc}}{c} - \frac{(v_{dM} i_{cd} + v_{qM} i_{cq}) + v_{c2} i_1}{c(v_{c1} + v_{c2})} \tag{4.94}$$

The large-signal models of the proposed model based on n-level converter are defined by (4.82) and (4.88). In addition, equations (4.93) and (4.94) show these models for three-level converter based model. As mentioned before, the modulation strategy will balance the NP voltage of interfaced converter; hence, the control stage must only regulate the total dc-link voltage in dc side, and the ac currents in ac side of the interfaced converter. Consequently, the proposed model can be simplified considering balanced voltage in the cascaded capacitors ($v_{c1} = v_{c2} = \frac{v_{dc}}{2}$).

Therefore (4.82) can be expressed as:

$$\frac{d}{dt}\begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} = \begin{bmatrix} \frac{-R_c}{L_c} & \omega \\ -\omega & \frac{-R_c}{L_c} \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} + \frac{1}{L_c}\begin{bmatrix} D_{nd} \\ D_{nq} \end{bmatrix} v_c - \frac{1}{L_c}\begin{bmatrix} v_d \\ 0 \end{bmatrix} \tag{4.95}$$

summation of two equations in (4.93) and (4.94), it gives:

$$\frac{dv_{c1}}{dt} + \frac{dv_{c2}}{dt} = \frac{i_{dc}}{c} - \frac{(v_{dM} i_{cd} + v_{qM} i_{cq}) - v_{c1} i_1}{c(v_{c1} + v_{c2})} + \frac{i_{dc}}{c} - \frac{(v_{dM} i_{cd} + v_{qM} i_{cq}) + v_{c2} i_1}{c(v_{c1} + v_{c2})} \tag{4.96}$$

By considering $v_{c1} = v_{c2} = \frac{v_{dc}}{2}$ and substituting in (4.95) and (4.96), the following equation will be obtained:

$$\frac{dv_{dc}}{dt} = \frac{i_{dc}}{c} - \frac{(v_{dM}i_{cd} + v_{qM}i_{cq}) + \frac{v_{dc}}{2}i_1}{c(\frac{v_{dc}}{2} + \frac{v_{dc}}{2})} + \frac{i_{dc}}{c} - \frac{(v_{dM}i_{cd} + v_{qM}i_{cq}) - \frac{v_{dc}}{2}i_1}{c(\frac{v_{dc}}{2} + \frac{v_{dc}}{2})} \tag{4.97}$$

Therefore, the final equation of (4.97) will be obtained as:

$$\frac{dv_{dc}}{dt} = 2\frac{i_{dc}}{c} - 2\frac{v_{dM}i_{cd} + v_{qM}i_{cq}}{cv_{dc}} \tag{4.98}$$

Equation (4.98) is a non-linear equation; consequently, it should be linearized by some mathematical technique to obtain a useful control model for DG model. Averaged variables are assumed, according to the local averaging operator:

$$F\vec{(}t) = \frac{1}{T_m}\int_{t-T_m}^{t} F(\tau)d\tau \tag{4.99}$$

By applying this linear operator to the proposed DG model in (4.81) and (4.98), all components of the variables related to switching frequency will be vanished. The variables of the proposed DG model are assumed henceforth to be averaged variables. In case of the simplicity, no difference in notation has been included. By considering this assumption, the dc-link voltage and the reactive current component to be controlled:

$$I_{qM} = I_q^* \;\; and \;\; v_{dc} = v_{dc}^* \tag{4.100}$$

Where terms I_q^* and v_{dc}^* refer the reference values in control circuit loop of the proposed DG model.

In addition, the transformed ac voltages of the interfaced converter (v_{dM}, v_{qM}) are the control variables. Therefore, the DG model is simplified to a two-input-two-output three-order system.

4.7.2 Steady State Analysis for Proposed DG Model

The steady-state behaviour of the proposed multi-variable process system imposes certain necessary conditions on its dynamic behaviour, especially in case of any feedback control system containing integral action. The subscript

("ss") is added to the variables to identify the operating point of proposed model in steady state conditions. Considering:

$$v_{dss} = E_L, \quad v_{qss} = 0, \quad i_{cqss} = I_q^* \quad and \quad v_{dcss} = v_{dc}^* \tag{4.101}$$

The remaining steady-state variables are obtained by imposing zero into the dynamic model of the proposed model; in other words, the steady-state variables are obtained by making the derivatives of the variables equal zero, as follows:

$$\frac{di_{cdss}}{dt} = -\frac{R_c}{L_c} i_{cdss} + \omega I_q^* + \frac{1}{L_c} v_{dMss} - \frac{1}{L_c} E_L = 0 \tag{4.102}$$

$$\frac{di_{cqss}}{dt} = -\omega i_{cdss} - \frac{R_c}{L_c} I_q^* + \frac{1}{L_c} v_{qMss} = 0 \tag{4.103}$$

$$\frac{dv_{dcss}}{dt} = 2\frac{i_{dcss}}{c} - 2\frac{v_{dMss} i_{cdss} + v_{qMss} I_q^*}{c v_{dc}^*} = 0 \tag{4.104}$$

The steady-state variables values are obtained by solving the equations (4.102)-(4.104). Therefore, these values can be obtained as:

$$i_{cdss} = \sqrt{(\frac{E_L}{2R_c})^2 + \frac{v_{dc}^*}{R_c} i_{dcss} - I_q^{*2}} - \frac{E_L}{2R_c} \tag{4.105}$$

$$v_{dMSS} = E_L + R_c i_{cdss} - \omega L I_q^* \tag{4.106}$$

$$v_{qMSS} = \omega L i_{cdss} + R_c I_q^* \tag{4.107}$$

The proposed model is linearized by applying Taylor's series and expansion around the selected operating point, by ignoring high order terms. This is an acceptable low, if variations around the operating point are assumed to be small; hence, the state-space equation of the small-signal model for proposed system is obtained. In a general case, any function defined by $y = f(x_1, x_2, ..., x_n)$, which has the value $y_{ss} = f(x_{1ss}, x_{2ss}, ..., x_{nss})$, at the operating point, can be developed using Taylor's series around this operation point and by approximating to the first-order terms can be expressed as:

$$y \approx y_{ss} + \frac{\partial f}{\partial x_1}|_{ss}(x_1 - x_{1ss}) + \frac{\partial f}{\partial x_2}|_{ss}(x_2 - x_{2ss}) + ... + \frac{\partial f}{\partial x_n}|_{ss}(x_n - x_{nss}) \tag{4.108}$$

Then we can define a new set of states, inputs, and outputs as:

$$y-y_{ss} \approx \frac{\partial f}{\partial x_1}|_{ss}(x_1-x_{1ss})+\frac{\partial f}{\partial x_2}|_{ss}(x_2-x_{2ss})+...+\frac{\partial f}{\partial x_n}|_{ss}(x_n-x_{nss}) \quad (4.109)$$

or

$$\bar{y} \approx \frac{\partial f}{\partial x_1}|_{ss}\bar{x_1} + \frac{\partial f}{\partial x_2}|_{ss}\bar{x_2} + ... + \frac{\partial f}{\partial x_n}|_{ss}\bar{x_n} \quad (4.110)$$

where, the small variations around the operating point are defined as: $\bar{x_1} = x_1 - x_{1ss}$, $\bar{x_2} = x_2 - x_{2ss}$, $\bar{x_n} = x_n - x_{nss}$.

Finally, by applying this linearizing technique to large-signal model (4.81) and (4.97) around an operating point results in the small-signal model as:

$$\frac{d}{dt}\begin{bmatrix} \bar{i_{cd}} \\ \bar{i_{cq}} \\ \bar{i_{dc}} \end{bmatrix} = \begin{bmatrix} \frac{-R_c}{L_c} & \omega & 0 \\ -\omega & \frac{-R_c}{L_c} & 0 \\ -2\frac{v_{dMss}}{cv_{dc}^*} & -2\frac{v_{qMss}}{cv_{dc}^*} & \frac{2(v_{dMss}i_{dss}+v_{qMss}I^*)}{cv_{dc}^{*2}} \end{bmatrix} \begin{bmatrix} \bar{i_{cd}} \\ \bar{i_{cq}} \\ \bar{i_{dc}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_c} & 0 \\ 0 & \frac{1}{L_c} \\ -2\frac{i_{cdss}}{cv_{dc}^*} & -2\frac{I_q*}{cv_{dc}^*} \end{bmatrix} \begin{bmatrix} \bar{v_{dM}} \\ \bar{v_{qM}} \end{bmatrix} + \begin{bmatrix} \frac{-1}{L_c} & 0 \\ 0 & 0 \\ 0 & \frac{2}{c} \end{bmatrix} \begin{bmatrix} \bar{E}_L \\ \bar{i}_{dc} \end{bmatrix} \quad (4.111)$$

4.7.3 Design of Equivalent Circuit

According to the (4.111), the equations of the state-space representation can be calculated as:

$$\bar{v_{dM}} - \bar{E_L} = L_c\frac{d\bar{i_{cd}}}{dt} + R_c\bar{i_{cd}} - \omega L_c\bar{i_{cq}} \quad (4.112)$$

$$\bar{v_{qM}} = L_c\frac{d\bar{i_{cq}}}{dt} + R_c\bar{i_{cq}} + \omega L_c\bar{i_{cd}} \quad (4.113)$$

$$\bar{i_{cd}} = \frac{c}{2}\frac{d\bar{v_{dc}}}{dt} + \frac{v_{dMss}}{v_{dc}^*}\bar{i_{cd}} + \frac{v_{qMss}}{v_{dc}^*}\bar{i_{cq}} + \frac{i_{cdss}}{v_{dc}^*}\bar{v_{dM}} + \frac{I_q^*}{v_{dc}^*}\bar{v_{qM}} - \frac{(v_{dMss}i_{cdss}+v_{qMss}I_q^*)}{v_{dc}^{*2}}\bar{v_{dc}} \quad (4.114)$$

Therefore, the following equivalent circuits are achieved, which are based on the equivalent equations of proposed DG model in (4.112)-(4.114).

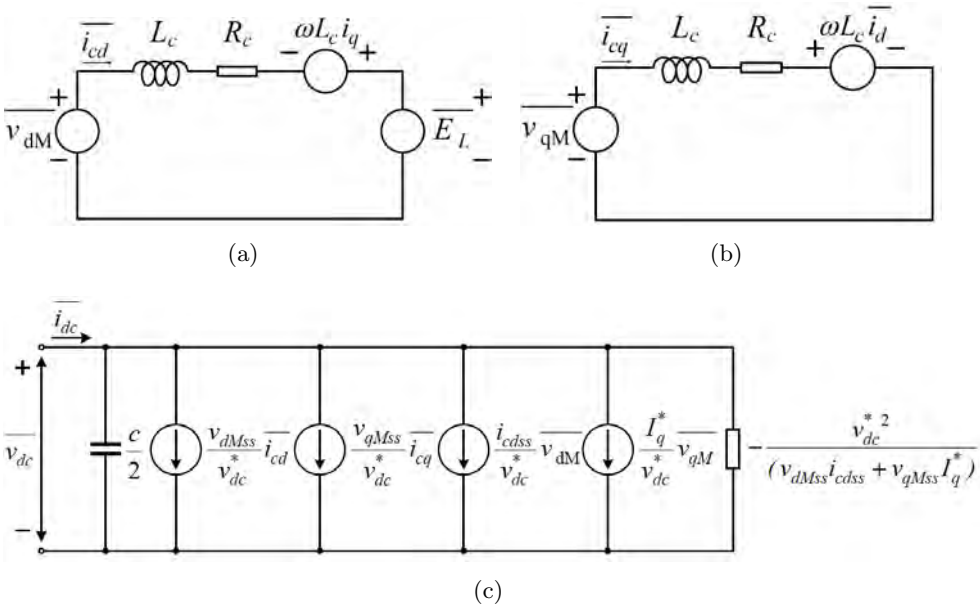


Figure 4.7: Equivalent small-signal circuit

As an example, by considering the reference value of the reactive current component equal to zero (I_q^*=0) in equivalent small-signal circuit model of the DG model (Figure 4.7), unity power factor will obtained. Therefore, the equivalent circuit model in figure 4.7 is simplified, as are its corresponding expressions. Figure 4.8 shows the simplified model of figure 4.7 for achieving unity power factor:

For the other values for power factor of system, the reference value of the reactive current will be obtained as:

$$I_q^* = \pm i_{cdss}\sqrt{\frac{1}{PF}-1} \tag{4.115}$$

In this equation, the negative sign is considered for the capacitive power factors, and positive sing is considered for inductive power factors.

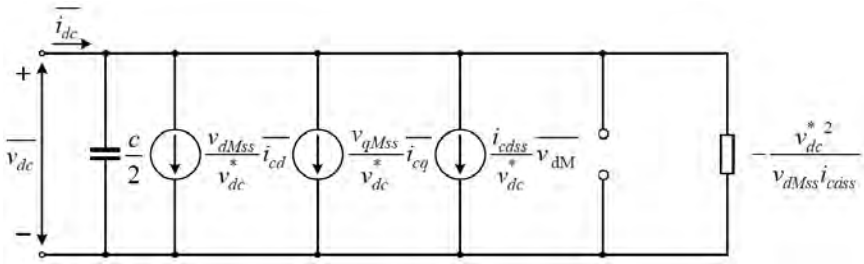


Figure 4.8: Equivalent small-signal circuit model for unity power factor

4.8 Conclusions of the Chapter

Three-phase schematic diagram of the proposed DG model has been presented in this chapter. The proposed model composed of the thevenin model of power grid, a full-wave thyristor converter which supplied an R-L load as a non-linear grid-connected load, a DG source and other components which has been shown by a dc current source, and multilevel converter as an interfacing system between the DG resources and power grid. The proposed interface model offers stable and high power quality injection from DG to the grid. At first step, a brief explanation about the synchronous reference frame control and the stationary reference frame control has been presented, and voltage and current components vectors shown in $\alpha\beta$ and dq reference frames. In the next stage, reference currents of DG control loop have been defined for compensation according to objective of integration. At the next step, dynamic model of the DG model has been elaborated in the stationary reference frame and then transformed into the synchronous orthogonal reference frame. The transformed variables are used in control of the multilevel voltage source converter as the heart of the interfacing system between DG resources and utility grid. The large-signal and small-signal mathematical model of the DG model have been analyzed, and an averaged small-signal model of the three-level converter described for the design of control loop circuit.

The proposed interface and control model provides a powerful infrastructure for DG units to meet the stricter demands for integrated system to the power grid.

Chapter 5

SVPWM for Multilevel Converter Topologies

5.1 Introduction

Several modulation techniques such as, Phase-shifted PWM, Selective Harmonic Elimination (SHE), and carrier-based PWM have been proposed and presented in many scientific reports. All these modulation techniques have some motivations and weakness during special situations. Among the proposed modulation algorithms, space-vector modulation (SVM) strategy stands out, because it offers significant flexibility to optimize switching waveforms and reduces the switching losses by limiting the switching to the two thirds of the pulse duty cycle, as a converter's gating signals generators. The space vector modulation (SVM) technique is originally a PWM technique with the difference that the switching times are computed based on the three-phase space vector representation of the reference and the converter switching states rather than the per-phase in time representation of the reference and the output levels [102]. Choi [103] was the first author to extend the two-level SVM technique to more than three levels for the diode-clamped converter. With the increase of the number of converter's levels in case of multilevel power converter topology, the number of allowable switching states in the proposed converters are also rapidly increasing. This situation places significant computational difficulties in front of the space vector PWM modulator, which is typically implemented in software and operating in real time and for high switching speeds.

This chapter describes the application of space vector modulation technique for multilevel three-phase converter topologies, and is organized as follows: First in section 5.2, the three-dimensional vector diagram of n-level converter is presented, and this diagram is considered for a three-level diode-clamped converter as a case study. Space vector model of the proposed converter and its output voltage components is presented in this section.

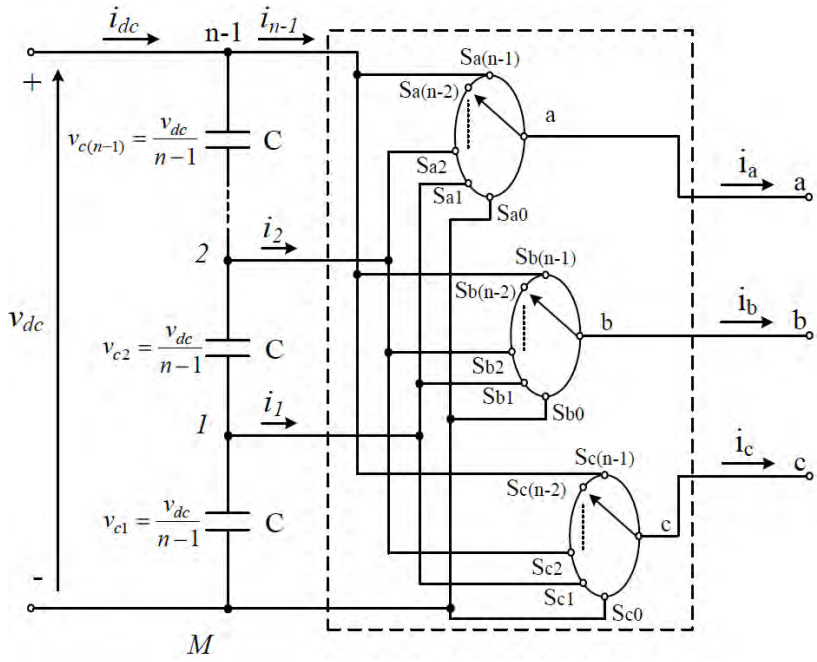


Figure 5.1: Schematic diagram of three-phase multilevel diode-clamped converter

The relationship between the space voltage vectors and switching states is presented in section 5.3, and some limitation area is discussed. In section 5.4, two methods for calculating duty cycles of vectors is presented. Some equations for calculation of sectors, and regions in sectors, are presented in sections 5.5, and 5.6. Section 5.7, describes the timing of switches, and sequence of switching for calculation of output voltage in proposed converter topology.

5.2 Representation of Three-Dimensional Vector

Basically, multilevel converter is a voltage synthesizer tool that generates its output voltage from many discrete voltage levels. Figure 5.1 shows the general functional diagram of multilevel diode-clamped converter topology, for the purpose studying of SVM switching technique.

It can be seen that, each phase leg of the converter can be represented by a single-pole n-throw switch. Each of the three phases of the n-level converter shares a common dc bus, which has been subdivided by (n-1)

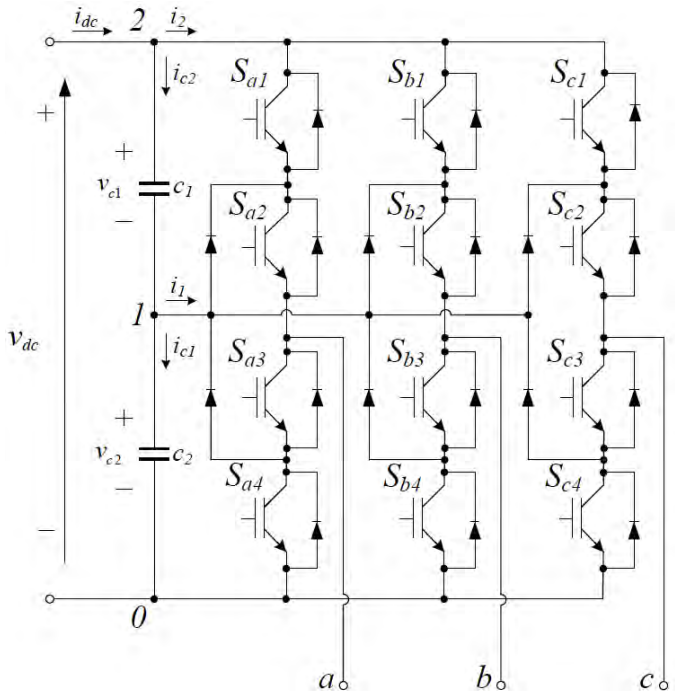


Figure 5.2: Schematic diagram of three-phase three-level diode-clamped converter

cascaded capacitors into n-levels. Therefore, the voltage across each cascaded capacitor in dc side of the converter is $(\frac{v_{dc}}{n-1})$ and the voltage stress across each switching device will be limited to $(\frac{v_{dc}}{n-1})$ through the clamping diodes in structure of converter. Figure 5.2 shows the schematic diagram of a three-level diode-clamped converter (NPC), (n=3) [104, 105]. As shown in this figure, dc-bus voltage in dc side of the NPC converter has been divided between two cascaded capacitors into three-levels, and the voltage across through each capacitors is $(\frac{v_{dc}}{2})$, therefore; the voltage stress across each switching device will be limited to $(\frac{v_{dc}}{2})$ through the clamping diodes.

Figure 5.3 shows Space Vectors in the three-dimensional Euclidean diagram, for a three-level diode-clamped converter, with their corresponding switching states, where each digit of the Space Vector identifier represents the voltage level to which the a, b, and c phase legs are, respectively, switched. The reason to naming the vectors with their corresponding switch-

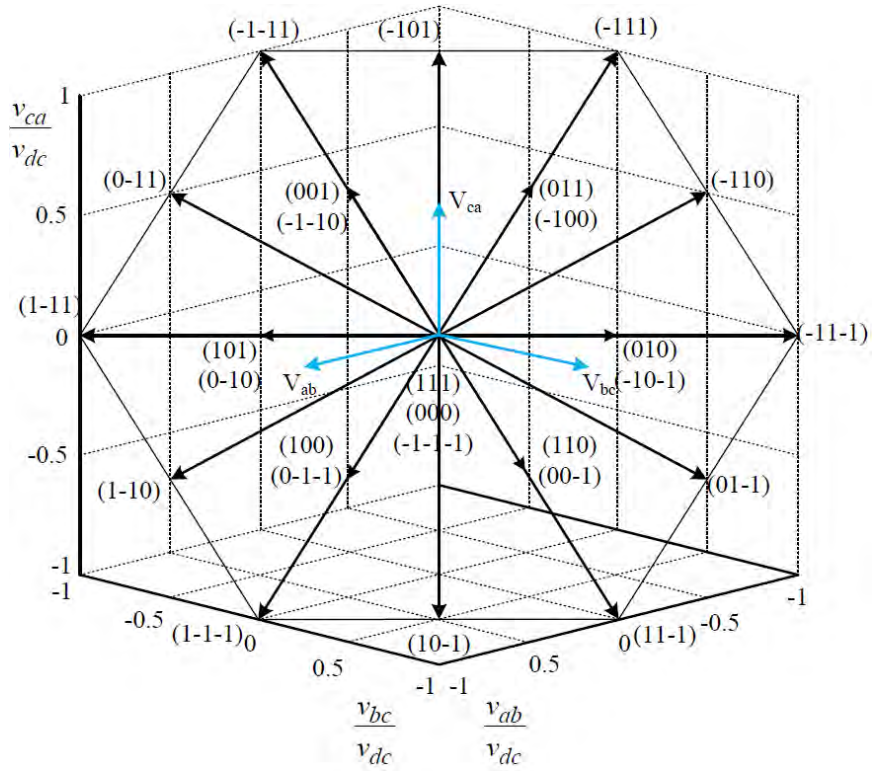


Figure 5.3: Switching states of a three-level converter

ing states is purely practical, because the converter switches are controlled on a per-phase basis, and a decision must be as to which vector to switch, as well as which switching state to select. On the other hand, representing vectors in the line voltage coordinate space is a nice mathematical abstraction to consistently explain the spatial relations between the switching vectors in proposed converter model.

By application of the Kirchof's voltage law, the sum of the line-to-line voltages in balance system always adds up to zero, which is really an equation of the plane in the line-to-line coordinate system. This means that all the switching vectors of a three-level converter lie in the plane, and that is how they are usually represented.

The voltage variables shown in figure 5.3 are the line-to-line voltages from a three-level converter topology, which are defined as follows:

$$\vec{v} = [v_{ab} \quad v_{bc} \quad v_{ca}]^T \tag{5.1}$$

if we define the positions of the equivalent phase switches of the phases a, b and c were in the locations i, j and k, respectively, where i,j,k ∈ [0, n-1], then that switching state could be represented by the switching vector as:

$$v(\vec{ijk}) = \frac{v_{dc}}{n-1}[i-j \quad j-k \quad k-i]^T \tag{5.2}$$

where $v(\vec{ijk}) = [v_{ab} \quad v_{bc} \quad v_{ca}]^T$.

These vectors are labeled in order to simplify their notation. It is somewhat important to make the distinction between switching states and switching vectors, in the sense that different switching vectors can be implemented with a various number of switching states. Note that, the NPC has three phase and three output levels or switching states per phase, resulting in 3^3 possible combinations, hence 27 state-space vectors indicating that each phase can have +1, 0 and -1 state. For the general n-level three-phase converter, there are n^3 switching state which make n_{vec}= 3n(n-1)+1 switching vectors [102, 106]. Figure 5.4 shows the representation of the space vectors for the three-level converter. According to figure 5.4, there are 24 active states including 12 single vectors, six double vectors and the remaining one triple vector are zero states (111,000,-1-1-1) that lie at the center of the hexagon because of their null lengths. However, only 19 are different, and eight are redundant.

Each integral point on the space vector plane has a fixed position in the complex plane, and represents a particular three-phase output voltage state of the converter. For example, the zero vector can be obtained in three ways, connecting the three-phase outputs to the positive bus bar ($v_{aN} = v_{bN} = v_{cN} = +v_{dc}/2$), or corresponding to the switching state (+1,+1,+1), or to the neutral point ($v_{aN} = v_{bN} = v_{cN} = 0$), corresponding to the state (0,0,0), or to the negative bus bar ($v_{aN} = v_{bN} = v_{cN} = -v_{dc}/2$), corresponding to the state(-1,-1,-1). From the load point of view, redundant vectors have the exact same influence, and it makes no difference which one is used. The point (+1, 0,-1) on the space vector plane means, phase (a) is connected to the positive bus ($v_{aN} = +v_{dc}/2$), phase (b) is connected to the neutral point ($v_{bN} = 0$) and phase (c) is connected to the negative bus ($v_{cN} = -v_{dc}/2$).

From the load point of view, redundant vectors have the exact same influence, and it makes no difference which one is used, but from the converter point of view, they are different switching states, and this can be used as an additional degree of freedom for other control purposes. It is worth mentioning that, since the possible output levels of the converters are fixed ($-v_{dc}/2$, 0, $+v_{dc}/2$), the state-space vectors are also fixed. Note that for a traditional two-level VSC, only seven different space vectors are obtained,

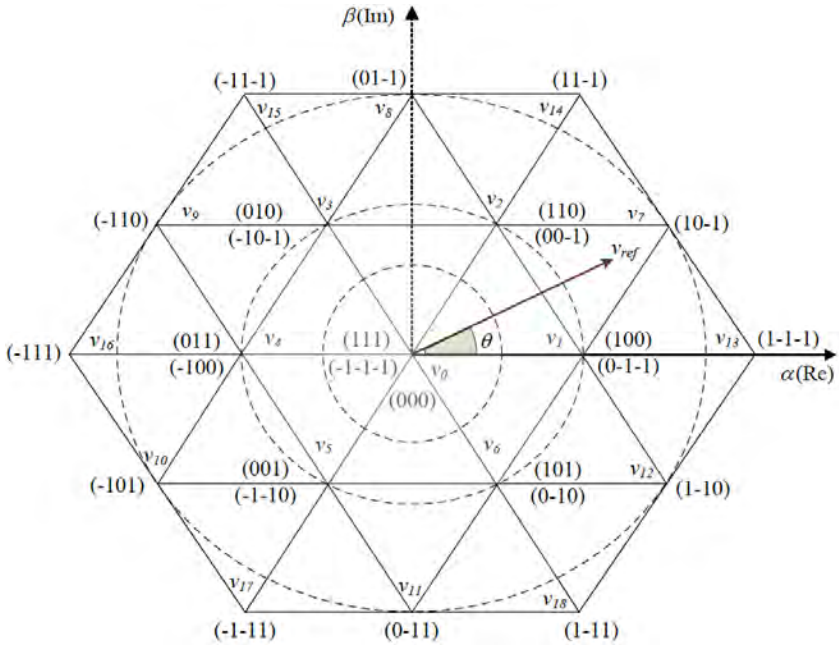


Figure 5.4: Space Vectors states for three-level NPC converter

while by just adding a third level like in NPC, 19 different can be generated. This increases over-proportionally in relation to the numbers of levels and is in direct accordance with the output power quality, as a denser state-space vector representation in the $\alpha - \beta$ plane is obtained, in the same way more levels are a more dense coverage of the amplitude range in the per-phase time representation.

Besides the output voltage state, the point (+1,0,-1) on the space vector plane can also represent the switching state of the converter and how many upper switches in each phase leg are ON for a three-level converter. By these considerations, the Switching states in figure 5.2 can be expressed as:

$$\left\{\begin{array}{r} S = (S_a, S_b, S_c), \quad S_{a,b,c} \in [+1, 0, -1] \\ State(+1) \longrightarrow S_{x1}, S_{x2} \;\; are \;\; ON \\ State(0) \longrightarrow S_{x2}, S_{x3} \;\; are \;\; ON \\ State(-1) \longrightarrow S_{x3}, S_{x4} \;\; are \;\; ON \end{array}\right\} \longrightarrow for \quad x = a, b, c \qquad (5.3)$$

$$\left.\begin{array}{l} State(+1) \longrightarrow v_{xN} = \dfrac{+v_{dc}}{2} \\ \qquad State(0) \longrightarrow v_{xN} = 0 \\ State(-1) \longrightarrow v_{xN} = \dfrac{-v_{dc}}{2} \end{array}\right\} \longrightarrow \quad for \quad x = a, b, c \tag{5.4}$$

5.3 Representation of Two-Dimensional Vector

In this section, the relationship between the space voltage vectors and switching states is derived. If we assume the three-phase balanced operation of the converter, the relationship between phase voltages a, b and c is as follows:

$$v_{aN}(t) + v_{bN}(t) + v_{cN}(t) = 0 \tag{5.5}$$

where v_{aN}, v_{bN}, and v_{cN} are the instantaneous grid or load phase voltages. A space vector voltage can be generally expressed in terms of the $\alpha - \beta$ voltages in the stationary coordination as:

$$\vec{v(t)} = v_\alpha(t) + jv_\beta(t) \tag{5.6}$$

where, by use of Clarke transformation matrix, the three-phase variables can be transformed into equivalent $\alpha - \beta$ variables as:

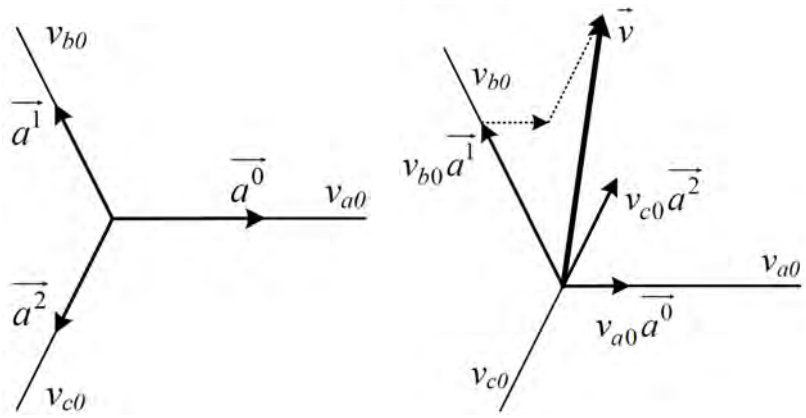
$$\begin{bmatrix} v_\alpha(t) \\ v_\beta(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{1}{2} & \frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{aN}(t) \\ v_{bN}(t) \\ v_{cN}(t) \end{bmatrix} \tag{5.7}$$

By substituting (5.7) into (5.6), we have

$$\vec{v(t)} = v_\alpha(t) + jv_\beta(t) = \frac{2}{3}[v_{aN}(t) + av_{bN}(t) + a^2 v_{cN}(t)] \tag{5.8}$$

where $a = e^{\frac{i2\pi}{3}} = -\frac{1}{2} + \mathrm{i}\frac{\sqrt{3}}{2}$ and $a^2 = e^{\frac{i4\pi}{3}} = -\frac{1}{2} - \mathrm{i}\frac{\sqrt{3}}{2}$ voltages of the converter (v_{aN}, v_{bN}, v_{cN}) for each possible switching state, the converter state-space vectors can be obtained. Figure 5.5(a) shows the three unitary director vectors of this transformation, while figure 5.5(b) shows an example for the case in which v_{a0}=100V, v_{b0}=300V, and v_{c0}=-200V.

The main objective of the SVPWM is to generate a reference vector ($\vec{m}$) in the same plane for each modulation cycle. As the reference vector may not be the same as any vector produced by the converter, its average value



(a) (b)

Figure 5.5: Clarke's Transformation: (a)director vectors and, (b)example of special vector

can be generated using more than one vector per modulation cycle by PWM-averaged approximation. By selecting right vectors and applying them in a suitable order helps the devices achieve low switching frequencies [104].Table 5.1 shows examples of mathematical equations to represent the phase output voltages or value of voltage vector of the three-level converter in terms of the switching states and dc-link cascaded capacitors.

The three-phase reference voltage vector can also be mapped to the $\alpha - \beta$ plane using the same transformation (5.8) but replacing the phase reference voltages instead of the phase output voltages. Since the references are not switched variables with fixed voltage values as the output phase voltages of the converter, the reference space vector v_{ref} can be mapped anywhere in the $\alpha - \beta$ plane and it is not necessarily coincide with any of the converter space vectors, analogous to the per-phase time representation, where the reference signal does not necessary match an converter output level. For balanced three-phase sinusoidal references, as is usual in power-converter systems, the resulting reference vector v_{ref} is a rotating space vector, with the same amplitude and angular speed (ω) of the sinusoidal references, with an instantaneous position with respect to the real axis α given by $\theta = \omega$t as the one illustrated in figure 5.4.

Figures [5.6] - [5.8] show the space vector model of the three-level diode-clamped converter which is shown in figure 5.2 and generation of voltage according to the switching state of the converter, and equation results of

Switching State	v_{aN}	v_{bN}	v_{cN}	$v_0 = \frac{2}{3}[v_{aN} + av_{bN} + a^2 v_{cN}]$	Voltage Vector
$(+1,+1,+1)$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$\frac{v_{dc}}{2}$	$v_0 = \frac{2}{3}[\frac{v_{dc}}{2} + a\frac{v_{dc}}{2} + a^2\frac{v_{dc}}{2}]$	$v_0 = 0$
$(0,0,0)$	0	0	0	$v_0 = \frac{2}{3}[0 + a0 + a^2 0]$	$v_0 = 0$
$(-1,-1,-1)$	$\frac{-v_{dc}}{2}$	$\frac{-v_{dc}}{2}$	$\frac{-v_{dc}}{2}$	$v_0 = \frac{2}{3}[\frac{-v_{dc}}{2} - a\frac{v_{dc}}{2} - a^2\frac{v_{dc}}{2}]$	$v_0 = 0$
$(+1,0,0)$	$\frac{v_{dc}}{2}$	0	0	$v_1 = \frac{2}{3}[\frac{v_{dc}}{2} + a0 + a^2 0]$	$v_1 = \frac{v_{dc}}{3}$
$(0,-1,-1)$	0	$\frac{-v_{dc}}{2}$	$\frac{-v_{dc}}{2}$	$v_1 = \frac{2}{3}[0 - a\frac{v_{dc}}{2} - a^2\frac{v_{dc}}{2}]$	$v_1 = \frac{v_{dc}}{3}$
$(+1,0,-1)$	$\frac{v_{dc}}{2}$	0	$\frac{-v_{dc}}{2}$	$v_7 = \frac{2}{3}[\frac{v_{dc}}{2} + a0 - a^2\frac{v_{dc}}{2}]$	$v_7 = \frac{v_{dc}}{\sqrt{3}} e^{i\frac{\pi}{6}}$
$(+1,-1,-1)$	$\frac{v_{dc}}{2}$	$\frac{-v_{dc}}{2}$	$\frac{-v_{dc}}{2}$	$v_{13} = \frac{2}{3}[\frac{v_{dc}}{2} - a\frac{v_{dc}}{2} - a^2\frac{v_{dc}}{2}]$	$v_{13} = \frac{2v_{dc}}{3}$

Table 5.1: Phase output voltages or value of voltage vectors of the NPC for each possible switching state

table 5.1. As mentioned before, each integer indicates how many upper switches in each phase leg are ON and how many lower switches are OFF, in three-level diode-clamped converter.

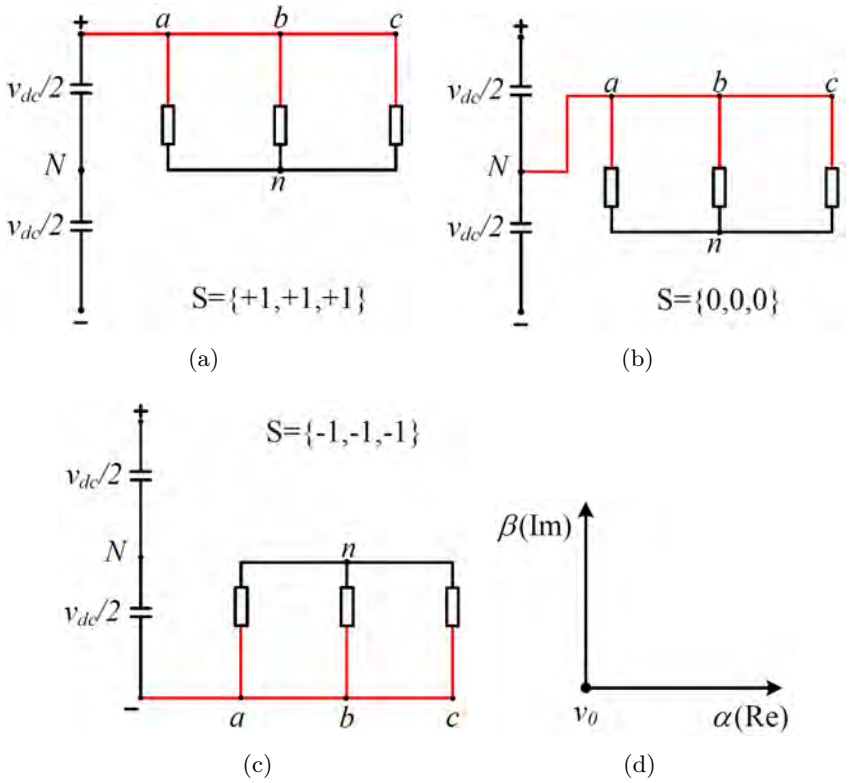


Figure 5.6: Generation of zero voltage vectors according to the switching states

Table 5.2 shows the magnitude of all different voltage vectors in three-level NPC converter. According to obtained results in table 5.2, v_0 generate the zero ac voltage as zero vectors in the origin of the diagram of space vector plan. As shown in figure 5.6, they connect all of the outputs of the converter to the same dc-link voltage level, and therefore, they don't produce any current in the dc side. Vectors (v_1-v_6) generate the $\frac{v_{dc}}{3}$ ac voltage as the output voltage state of the converter, and considered as internal vectors in space vector plan. These vectors connect the ac outputs to two consecutive dc-link voltage levels. As shown in figure 5.7, they are double vectors, which mean that two states of the converter can generate the same voltage vector

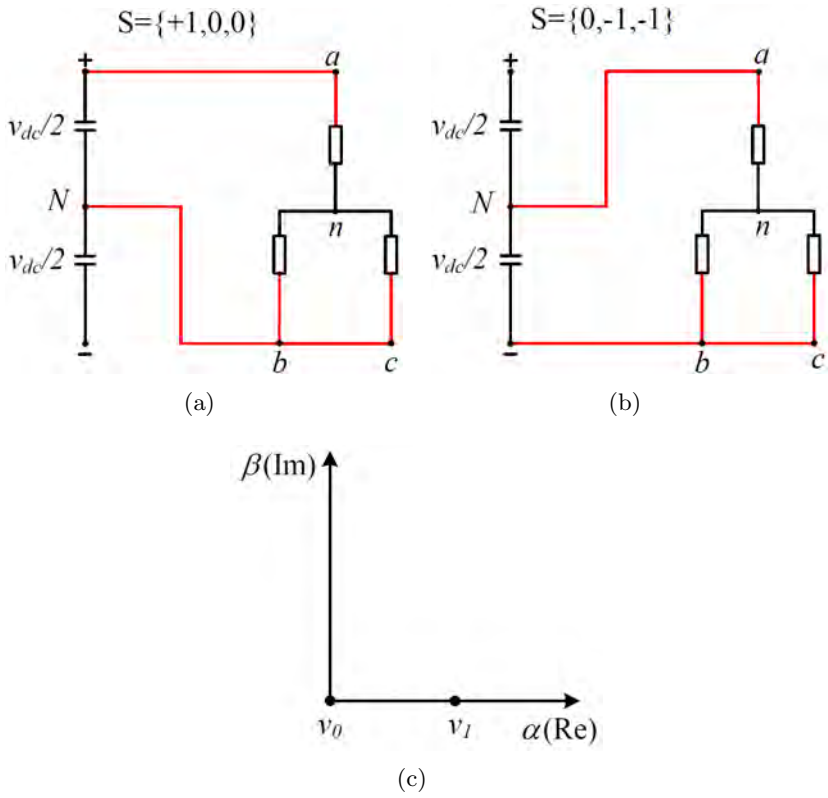


Figure 5.7: Generation of internal voltage vectors according to the switching states

in output of converter. In addition, as shown in figure 5.7, they affect the NP current in positive ways, therefore; proper utilization of these vectors will help the NP voltage to achieve balance.

Vectors, (v_7-v_{12}) generates the $\frac{v_{dc}}{\sqrt{3}}$ ac voltage as the output voltage state of the converter, and considered as middle vectors in space vector plan. These vectors connect each ac output to a different dc-link voltage level. Under a balanced system condition, their tip end in the middle of the segments that join two consecutive large vectors. The length of the middle vectors defines the maximum amplitude of the reference vector for linear modulation and steady-state conditions. As shown in figure 5.8, one output is always connected to the NP, therefore the corresponding output current will define the NP current (i_1). This connection produces voltage imbalances in the

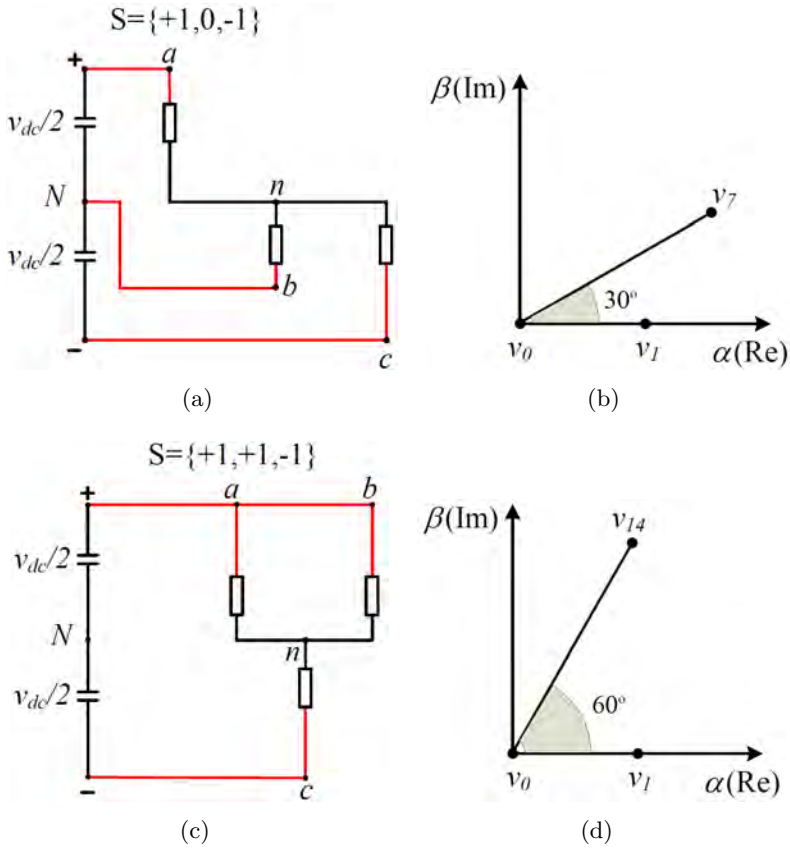


Figure 5.8: Generation of middle and external voltage vectors according to the switching states

cascaded capacitors, and these must be compensated. Vectors (v_{13}-v_{18}) generate the $\frac{2v_{dc}}{3}$ ac voltage as the large or external vectors assign the output voltages of the three-level converter to either the highest or the lowest dc voltage levels. Their length is double of the length of the small vectors in figure 5.7. As they don't connect any output to the NP, they don't affect the voltage balance of the cascaded capacitors. These vectors can generate the highest ac voltage amplitude because they have the greatest lengths. In fact, these six vectors are equivalent to the active ones of the two-level converters [107].

Type of Vectors	Vector's Number	Magnitude (V)
Zero Vector	$[v_0]$	0
Internal Vectors	$[v_1 - v_6]$	$\frac{v_{dc}}{3}$
Middle Vectors	$[v_7 - v_{12}]$	$\frac{v_{dc}}{\sqrt{3}}$
External Vectors	$[v_{13} - v_{18}]$	$\frac{2}{3}v_{dc}$

Table 5.2: Voltage vectors magnitude in three-level converter

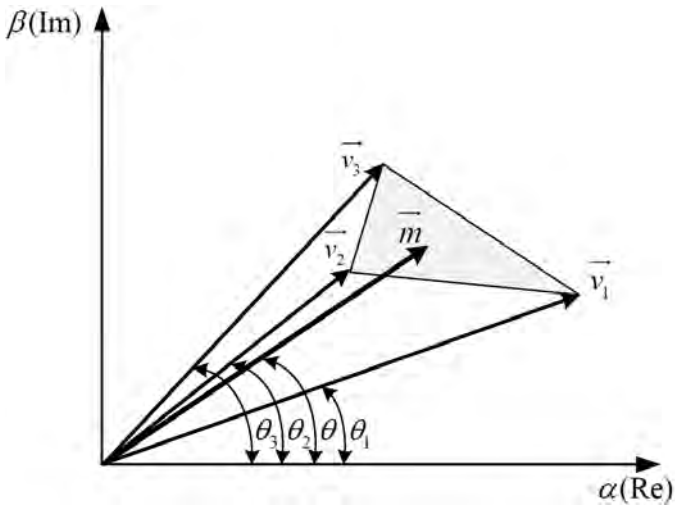


Figure 5.9: Limiting area to generate the reference vector by using the triangle connecting of three vectors

5.3.1 Limiting Area in Space Vector Plan

Figure 5.9 shows the set of three voltage vectors $\vec{v_1}$, $\vec{v_2}$ and $\vec{v_3}$ in space vector plan $(\alpha - \beta)$. As shown in this figure, the mentioned vectors can generate a reference vector $\vec{m}$ in the same plane by using PWM-averaged approximation, if the reference vector lies in the triangle connecting the tips of mentioned three voltage vectors.

The average value of reference vector can be calculated by consequentially applying these vectors in a modulation period in accordance with:

$$\frac{1}{T_m}\int_0^{T_m} \vec{m}dt = \frac{1}{T_m}\int_0^{T_1} \vec{v_1}dt + \frac{1}{T_m}\int_{T_1}^{T_1+T_2} \vec{v_2}dt + \frac{1}{T_m}\int_{T_1+T_2}^{T_m} \vec{v_3}dt \quad (5.9)$$

where T_m is the modulation period, and $T_1 + T_2 \leq T_m$.

Considering an approximately constant value for reference vector during a modulation period, which is acceptable if T_m is so smaller than the line period (T), then (5.9) can be expressed as:

$$\vec{m} = d_1\vec{v_1} + d_2\vec{v_2} + d_3\vec{v_3} \tag{5.10}$$

where terms d_1, d_2 and d_3 are the duty cycles of vectors $\vec{v_1}$, $\vec{v_2}$ and $\vec{v_3}$, respectively, with the following additional constraint on the duty cycles:

$$d_1 + d_2 + d_3 = 1 \tag{5.11}$$

using the nearest three vectors is the best way to synthesize the voltage reference vector. By imposing zero value to one of the duty cycles, the boundaries of the area that allows the reference vector to be generated can be determined. For example, considering d_3=0, and by using equations (5.10) and (5.11), the reference vector can be calculated as follows:

$$\vec{m} = d_1(\vec{v_1} - \vec{v_2}) + \vec{v_2} \tag{5.12}$$

Figure 5.10 shows the boundary of the area, which calculated when d_3=0. As all the duty cycles values could potentially utilize values in the interval [0, 1], the tip of the reference vector is on the line that joins the extremes of the vectors $\vec{v_1}$, and $\vec{v_2}$, which can be verified by simply making d_1 vary within that interval. Therefore, this segment is one boundary of the limiting area. The other two remaining segments of the triangular region in figure 5.9 can be calculated by imposing zero to two other duty cycle values (d_1 and d_2) separately.

For any other reference vector outside of this area requires that one or more duty cycles be negative value. In fact this assumption does not make physical sense; therefore, it cannot be generated by this set of three vectors in space vector plan.

5.4 Computation of Duty Cycles

5.4.1 General Method for Computation of Duty Cycles

This section describes a general strategy for calculation of duty cycles of voltage vectors. Equation (5.10) can be written by the following exponential equation:

$$\vec{m} = me^{j\theta} = d_1v_1e^{j\theta 1} + d_2v_2e^{j\theta 2} + d_3v_3e^{j\theta 3} \tag{5.13}$$

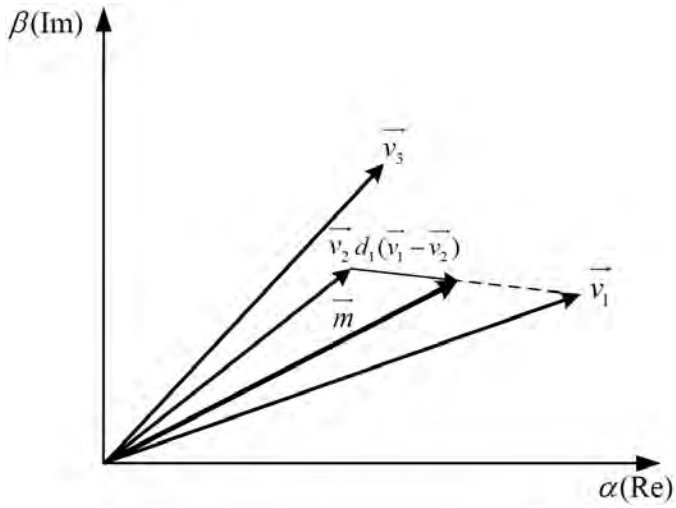


Figure 5.10: Boundary of the area, calculated by imposing zero value into the d_3

By this assumption, the duty cycle of the each voltage vectors can be determined according to either of the following equation systems:

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} v_1\cos\theta 1 & v_2\cos\theta 2 & v_3\cos\theta 3 \\ v_1\sin\theta 1 & v_2\sin\theta 2 & v_3\sin\theta 3 \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} m\cos\theta \\ m\sec\theta \\ 1 \end{bmatrix} \tag{5.14}$$

or by considering these vectors in real and imaginary systems, (5.14) can be written as:

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} Re(\vec{v_1}) & Re(\vec{v_2}) & Re(\vec{v_3}) \\ Im(\vec{v_1}) & Im(\vec{v_2}) & Im(\vec{v_3}) \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} Re(\vec{m}) \\ Im(\vec{m}) \\ 1 \end{bmatrix} \tag{5.15}$$

In general terms, given any bi-dimensional stationary base frame, orthogonal or not, the expression can be expressed as:

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} |\vec{v_1}|_x & |\vec{v_2}|_x & |\vec{v_3}|_x \\ |\vec{v_1}|_y & |\vec{v_2}|_y & |\vec{v_3}|_y \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} |\vec{m}|_x \\ |\vec{m}|_y \\ 1 \end{bmatrix} \tag{5.16}$$

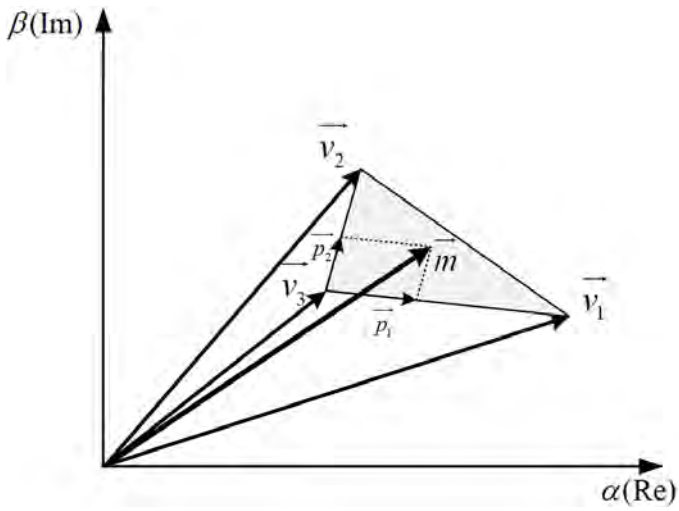


Figure 5.11: Projections of the reference vector $\vec{m}$ ($\vec{p_2}$ and $\vec{p_1}$)

The calculation of duty cycle values of vectors by this method requires inversing a matrix, which complicates the use of this technique to a real-time processor system. In addition, the equation system may need to be solved more than once per modulation period (T_m), since the region where the reference vector lies is previously unknown. Therefore, a simplified mathematical process should be developed for calculation of duty cycles values.

5.4.2 Calculation of Duty Cycles by Projections

This strategy is based on determining some projections of the reference vector, and it will be applied in order to simplify the modulation process.

Figure 5.11 shows the two vectors $\vec{p_1}$ and $\vec{p_2}$ which are the projections from the reference vector $\vec{m}$ into the segments that join the extreme of $\vec{v_3}$ to $\vec{v_1}$ and to $\vec{v_2}$, respectively.

By paying attention into the figure 5.11, the reference vector can be calculated as follows:

$$\vec{m} = \vec{p_1} + \vec{p_2} + \vec{v_3} \tag{5.17}$$

By considering the instantaneous position of the vectors, value of the reference vector can calculated as:

$$\vec{m} = p_1 \frac{\vec{v_1} - \vec{v_3}}{l_1} + p_2 \frac{\vec{v_2} - \vec{v_3}}{l_2} + \vec{v_3} \tag{5.18}$$

where l_1 and l_2 are the length of the vectors $\vec{v_1}$-$\vec{v_3}$ and $\vec{v_2}$-$\vec{v_3}$, respectively. At the end, the reference vector $\vec{m}$ can be calculated as:

$$\vec{m} = \frac{p_1}{l_1}\vec{v_1} + \frac{p_2}{l_2}\vec{v_2} + (1 - \frac{p_1}{l_1} - \frac{p_2}{l_2})\vec{v_3} \tag{5.19}$$

From (5.19), the duty cycles of the vectors can be directly calculated as follows:

$$d_1 = \frac{p_1}{l_1}, \quad d_2 = \frac{p_2}{l_2}, \quad d_3 = (1 - \frac{p_1}{l_1} - \frac{p_2}{l_2}) \tag{5.20}$$

If the balanced SV diagram is normalized to have triangular regions with unity lengths (l_1=l_2=1), the calculation of those duty cycles is simplified as:

$$d_1 = p_1, \quad d_2 = p_2, \quad and \quad d_3 = (1 - p_1 - p_2) \tag{5.21}$$

In fact, calculation of the duty cycle values by this technique is very functional. However, the former condition that all the areas must be equilateral triangles is only possible if the voltages of the dc-link capacitors are balanced. Thus, when dealing with the unbalanced case, these lengths can no longer be considered to be unity because they change according to the present imbalance. In that case, (5.20) must be applied [104].

5.5 Determination of the Sectors

The first step the modulator needs to perform is to determine the three nearest vectors, which is really to identify the sector, or triangle in which the tip of the reference vector, v_{ref} is located. The inner triangle is always within a certain sixty-degree region. For the sector selection, the angle θ of reference vector must be calculated. As shown in figure 5.4, the sectors where the reference vector lies can be directly found in a hexagon the area of the hexagon can be divided into six sectors (I-VI) and in case of three-level converter, each sector has four region altogether 24 regions of operation. From the value θ, the sextant where the reference vector lies can be directly found. These relationships between θ and sectors are illustrated in table 5.3.

5.6 Determining the Regions in Sectors

Coming back to the symmetry of all the sectors in previous section, it can be interesting to consider the reference vector into the first sector in order to reduce the number of relevant regions. Note that, they are (n^3-n) regions for

Angle	$0^o \leqslant \theta < 60^o$	$60^o \leqslant \theta < 120^o$	$120^o \leqslant \theta < 180^o$
Sector	(I)	(II)	(III)
Angle	$180^o \leqslant \theta < 240^o$	$240^o \leqslant \theta < 300^o$	$300^o \leqslant \theta < 360^o$
Sector	(IV)	(V)	(VI)

Table 5.3: Determination of the sectors according to reference voltage angle

an n-level converter, therefore each sector divided into the $\frac{(n^3-n)}{6}$ regions. In addition, the amplitude of the reference vector must be normalized to match into a vector-diagram in which the sector regions have half of unity lengths. Although, the maximum length of the normalized reference vector is the one-unity value in theoretical system, but, in steady- state conditions, its length is imitated to $\frac{\sqrt{3}}{2}$ due to the fact the longer of this vector will be outside of the vector-diagram hexagon, and thus cannot be generated by modulation. Figure 5.12 shows the maximum length of the normalized reference vector in steady-state condition. In addition, the over-modulation is occurred if the normalized reference vector assumes length longer than $\frac{\sqrt{3}}{2}$ for some positions of this vector, but it can never be outside of the hexagon.

By considering of term (m) as a modulation index which potentially uses values in the interval m $\in$ [0,1], for linear modulation, the length of the normalized reference vector can be calculated as:

$$m_n = \frac{\sqrt{3}}{2}m, \quad 0 \leq m_n \leq \frac{3}{2} \tag{5.22}$$

Figure 5.13(a) shows the normalized reference vector which is decomposed into the axes located at zero and sixty degrees, for obtaining projection m_1 and m_2 respectively. Figure 5.13(b) show different vectors which are needed for calculation of m_1 and m_2.

The lengths of the new vectors which have been shown in figure 5.13 can be calculated by:

$$b = m_2 sin(\pi/3) = \frac{\sqrt{3}}{2}m_2 \longrightarrow m_2 = \frac{2}{\sqrt{3}}b = \frac{2}{\sqrt{3}}m\sin\theta \tag{5.23}$$

and

$$m_1 = m\cos\theta - c \longrightarrow m\cos\theta - (a\cos(\frac{\pi}{3})) = m\cos\theta - \frac{a}{2} \tag{5.24}$$

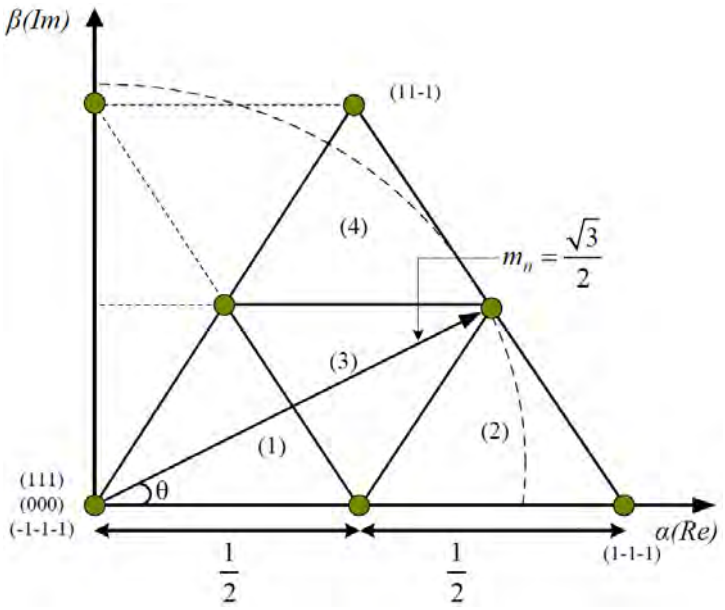


Figure 5.12: Maximum length of the normalized reference vector in steady-state condition

$$a = m_2 \longrightarrow m_1 = m\cos\theta - \frac{1}{\sqrt{3}} m\sin\theta \tag{5.25}$$

These values of m_1 and m_2 are the direct duty ratio of the vectors, as in the following:

$$\begin{aligned} d_{100/0-1-1} = m_1, \quad d_{110/00-1} = m_2 \quad and \\ d_{111/000/-1-1-1} = \frac{1}{2} - m_1 - m_2 \end{aligned} \tag{5.26}$$

Figure 5.14 shows the different cases for which the normalized reference vector is located in regions 1, 2, 3 and 4 of first sector [108].

Table 5.4 summarizes the information needed to ascertain the regions where the reference vector lies in the first sextant.

From the values of m_1 and m_2 and θ, the sextant where the reference voltage vector lies can be directly found, as can the components m_1 and m_2 of the equivalent reference voltage vector in the first sector.

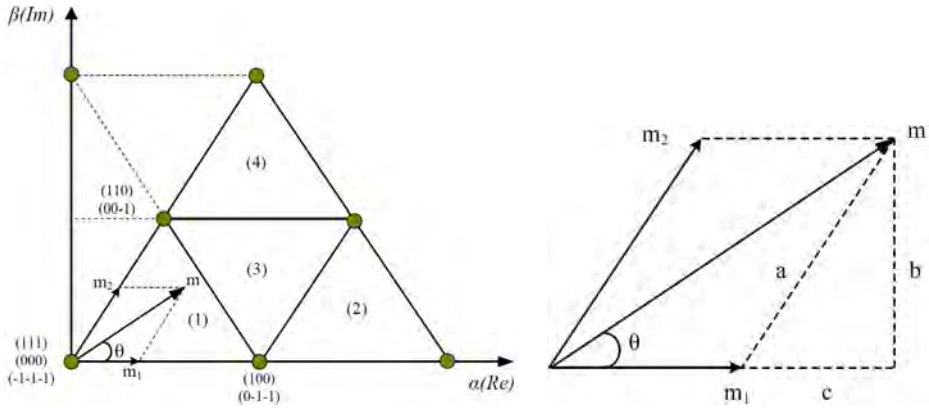


Figure 5.13: Projection of the normalized reference vector in the first sextant

Region	(1)	(2)	(3)	(4)
Case	$m_1 < 0.5$ $m_2 < 0.5$ $m_1 + m_2 < 0.5$	$m_1 > 0.5$	$m_1 < 0.5$ $m_2 < 0.5$ $m_1 + m_2 > 0.5$	$m_2 > 0.5$

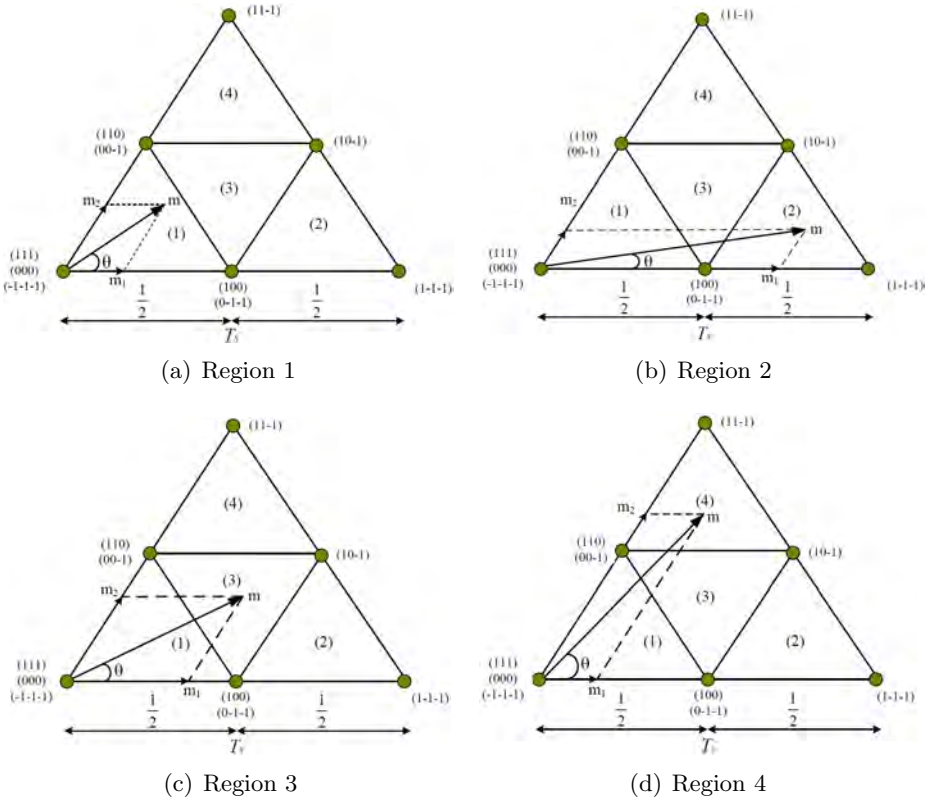
Table 5.4: Summary of information for the SVPWM

5.7 Switching Times Calculation

The basic idea of Space Vector PWM (SVPWM) is to use the state-space vector to combine or modulate three state-space vectors of the converter, so that their time average equals the reference space vector, in the same way PWM combines the levels to obtain a time average of the reference in the per-phase representation. The modulation principle of SVPWM in figure 5.4 can be summarized by (5.27), where the reference vector is located in region (3) in sector (1), and surrounded by v_1,v_2 and v_7.

$$v_1 T_a + v_7 T_b + v_2 T_c = v_{ref} \frac{T_s}{2} \tag{5.27}$$

where $\frac{T_s}{2}$=(T_a+T_b+T_c) is the switching time of the SVPWM control or fixed modulation period (analogous to the carrier period in PWM), v_1,v_2 and v_7 are the three closest vectors to the reference (highlighted in red in the qualitative example shown in figure 5.4). The vectors nearest to reference vector are the most appropriate selections in terms of their ability to



(a) Region 1 (b) Region 2

(c) Region 3 (d) Region 4

Figure 5.14: Projection for regions 1, 2, 3 and 4 of sector (I)

minimize the switching frequencies of the power devices, improve the quality of the output voltage spectra, and the electromagnetic interference (EMI). The problem is then reduced to finding an algorithm capable of finding the closest vectors to the reference and computing the ON times of each vector T_a, T_b and T_c. Once these are computed, each vector is generated during the corresponding time, achieving the desired time average over $\frac{T_s}{2}$ that equals the reference. In figure 5.4 the SV diagram of the three-level converter is divided into sextants, and each sextant is then divided into four triangular regions in order to show the vectors nearest to the reference. Figure 5.15 shows v_{ref} is located in the region (1) in sector (1) triangle, formed by the voltage vectors v_1,v_2 and v_7. For a given reference vector magnitude and position, the three closest vectors are used to generate the main value over the modulation period T_s. This strategy reduces distortion in voltage and

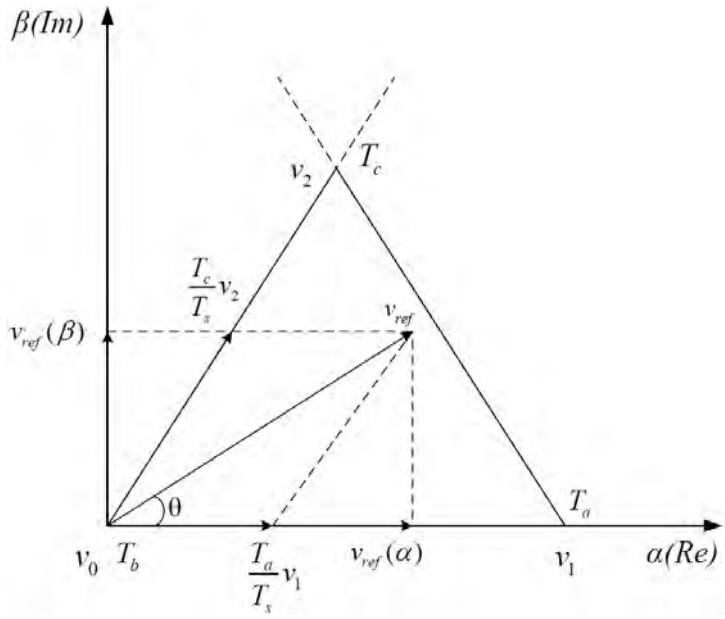


Figure 5.15: Switching times calculation for first region of sector (I)

current. The next step is to determine the amount of time that must be spent at each vector in order for the average voltage to be equal to the commanded voltage [109]. These time segments are then distributed in a certain sequence in the sampling period (T_s) so that the PWM wave is symmetrical and the neutral point voltage remains balanced. The transfer characteristic between the fundamental output voltage and the reference voltage is inherently linear in the whole under-modulation region. This can be done using some mathematical relationships. Following equations shows the analytical time expressions for T_b, T_a and T_c, where θ is instantaneous angle of load voltage, the rotating reference voltage vector v_{ref} is synthesized using the fixed vectors generated by the converter, and v_{dc} is dc link voltage of the converter. In steady-state conditions, the reference vector rotates at a constant angular speed (ω), which defines the frequency of the output voltages. The amplitude of the fundamentals of those voltages is proportional to the length of the reference vector.

Duration of the voltage vectors v_1,v_2 and v_7 which correspond to the apexes of the first triangle of first sector, T_b, T_a and T_c can be calculated by the following equations [110].

A. Calculation of T_c in first region of sector (I):

$$v_{ref}(\beta) = v_{ref}\sin\theta \longrightarrow v_{ref}(\beta) = \frac{T_c}{T_s}v_2\sin(\frac{\pi}{3}) = \frac{\sqrt{3}}{2}\frac{T_c}{T_s}v_2 \tag{5.28}$$

$$v_{ref}\sin\theta = \frac{\sqrt{3}}{2}\frac{T_c}{T_s}\frac{v_{dc}}{3} \longrightarrow T_c = 2\sqrt{3}\frac{v_{ref}}{v_{dc}}T_s\sin\theta \tag{5.29}$$

for $k = 2\sqrt{3}\frac{v_{ref}}{v_{dc}}$:

$$T_c = kT_s\sin\theta \tag{5.30}$$

B. Calculation of T_a in first region of sector (I):

$$\begin{aligned} v_{ref}(\alpha) = v_{ref}\cos\theta \longrightarrow v_{ref}(\alpha) &= \frac{T_a}{T_s}v_1 + \frac{T_c}{T_s}v_2\cos(\frac{\pi}{3}) \\ &= \frac{T_a}{T_s}v_1 + \frac{T_c}{2T_s}v_2 \end{aligned} \tag{5.31}$$

$$v_{ref}(\alpha) = \frac{T_a}{T_s}\frac{v_{dc}}{3} + \frac{T_c}{2T_s}\frac{v_{dc}}{3} = \frac{v_{dc}}{3T_s}(T_a + \frac{T_c}{2}) \tag{5.32}$$

$$3T_s\frac{v_{ref}}{v_{dc}}\cos\theta = (T_a + \frac{T_c}{2}) \longrightarrow T_a = 3T_s\frac{v_{ref}}{v_{dc}}\cos\theta - \frac{T_c}{2} \tag{5.33}$$

$$T_a = 3T_s\frac{v_{ref}}{v_{dc}}\cos\theta - \sqrt{3}\frac{v_{ref}}{v_{dc}}T_s\sin\theta \tag{5.34}$$

$$T_a = 2\sqrt{3}\frac{v_{ref}}{v_{dc}}T_s(\sqrt{\frac{3}{2}}\cos\theta - \frac{1}{2}\sin\theta) = kT_s(\frac{\sqrt{3}}{2}\cos\theta - \frac{1}{2}\sin\theta) \tag{5.35}$$

$$T_a = kT_s\sin(\frac{\pi}{3} - \theta) \tag{5.36}$$

C. Calculation of T_b in first region of sector (I):

$$T_a + T_b + T_c = \frac{T_s}{2} \longrightarrow T_b = \frac{T_s}{2} - T_a - T_c \tag{5.37}$$

$$\begin{aligned} T_b &= T_s[\frac{1}{2} - k\frac{\sqrt{3}}{2}\cos\theta + k\frac{1}{2}\sin\theta - k\sin\theta] \\ &= T_s[\frac{1}{2} - k\frac{\sqrt{3}}{2}\cos\theta - k\frac{1}{2}\sin\theta] \end{aligned} \tag{5.38}$$

$$T_b = \frac{T_s}{2}[1 - k(\sqrt{3}\cos\theta + \sin\theta)] = \frac{T_s}{2}[1 - 2k\sin(\theta + \frac{\pi}{3})] \tag{5.39}$$

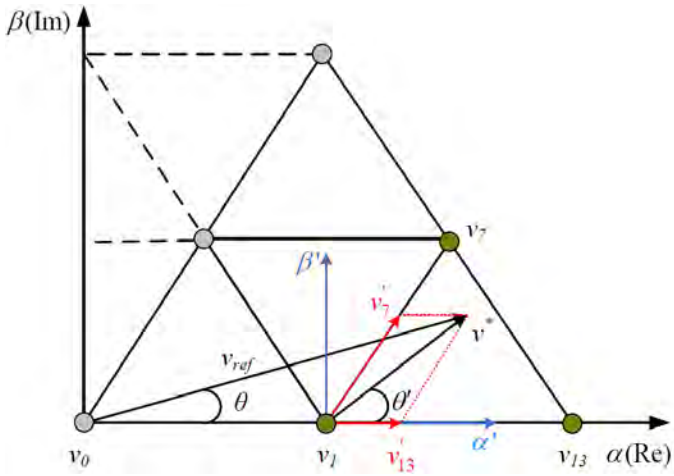


Figure 5.16: Switching times calculation for second region of sector (I)

for the position of reference vector in other regions, a new $\alpha^{'} - \beta^{'}$ plan with origin in one of the three vectors is defined, as shown in figure 5.16, where v^* is the new reference vector in the $\alpha' - \beta'$ plan.

Both references are related to each other by the $\alpha' - \beta'$ plan zero vector (v_1 in this case):

$$v^* = v_{ref} - v_1 \tag{5.40}$$

Then, the new mean value equation can be obtained as:

$$v^* = \frac{1}{T_s}[(v_{13} - v_1)T_c + (v_7 - v_1)T_b + (v_1 - v_1)T_a] \tag{5.41}$$

$$\frac{T_s}{2} = (T_a + T_b + T_c) \tag{5.42}$$

The vector composition in the $\alpha' - \beta'$ plane gives v^*=$v^{'}_{13}$+$v^{'}_{7}$. By matching the projections with the new mean value equation,

$$v^{'}_{7} = \frac{2T_b}{T_s}(v_7 - v_1) \longrightarrow T_b = \frac{|v^{'}_{7}|}{|v_7 - v_1|}\frac{T_s}{2} \tag{5.43}$$

$$|v_7 - v_1| = \frac{v_{dc}}{3} \longrightarrow T_b = \frac{3|v^{'}_{7}|}{v_{dc}}\frac{T_s}{2} \tag{5.44}$$

$$v^{'}_{13} = \frac{2T_c}{T_s}(v_{13} - v_1) \longrightarrow T_c = \frac{|v^{'}_{13}|}{|v_{13} - v_1|}\frac{T_s}{2} \tag{5.45}$$

$$|v_{13} - v_1| = \frac{v_{dc}}{3} \longrightarrow T_c = \frac{3|v_{13}^{'}|}{v_{dc}} \frac{T_s}{2} \tag{5.46}$$

$$T_a = \frac{T_s}{2} - T_b - T_c \tag{5.47}$$

From the geometric analysis,

$$|v_7^{'}| = |v^*| \cos\theta^{'} - 0.5|v_{13}^{'}| \tag{5.48}$$

$$|v_{13}^{'}| = \frac{2}{\sqrt{3}}|v^*| \sin\theta^{'} \tag{5.49}$$

Table 5.5 shows the analytical time expressions results for T_a, T_b and T_c for all the regions in the six sectors, where k=$2\sqrt{3}\frac{v_{ref}}{v_{dc}}$. These time intervals are distributed appropriately so as to generate symmetrical PWM pulses with neutral point voltage balancing.

Next step in the SVPWM scheme is to determine a sequence of switching for the voltage vectors or vector generation sequence. This sequence can be modified in order to reduce commutations, balance dc-link capacitors or reduce common mode voltages while the reference vector rotates trough the complex plane. For this case, the switching sequence in first region of first sector (when v_0, v_1, and v_2 are the closest vectors) will be from v_0-v_1-v_2-v_0-v_2-v_1-v_0. At the end of the sequence, the controller switching time T_s has elapsed and the process is repeated with updating the commanded voltage, identifying the three nearest vectors, calculating the switching times, and scheduling the switching sequence. Figure 5.17 shows the direction of the switching sequences for all regions in the six sectors [111].

Table 5.6 shows the summary of selected switching signals according to switching sequence of phase voltages for all the regions in the six sectors of converter. These sequences shows best minimize the switching frequencies of the devices. Table 5.7 shows the segmentation of time intervals and switching state in each phase, whenever voltage vector located in first region of first sextant.

Figure 5.18 shows the corresponding PWM waves of the three phases in first region of sector (1), where the switching states (+1,0,-1) for segments, T_a, T_b and T_c can be verified from figure 5.17. Each switching pattern during $\frac{T_s}{2}$ is repeated inversely in the next $\frac{T_s}{2}$ interval with appropriate segmentation of T_a, T_b and T_c intervals in order to generate symmetrical

Sector	Region-1	Region-2	Region-3	Region-4
1	$T_a = kT_s \sin(\frac{\pi}{3} - \theta)$ $T_b = \frac{T_s}{2}[1 - 2k \sin(\frac{\pi}{3} + \theta)]$ $T_c = kT_s \sin\theta$	$T_a = T_s[1 - k \sin(\frac{\pi}{3} + \theta)]$ $T_b = kT_s \sin\theta$ $T_c = \frac{T_s}{2}[2k \sin(\frac{\pi}{3} - \theta) - 1]$	$T_a = \frac{T_s}{2}[1 - 2k \sin\theta]$ $T_b = \frac{T_s}{2}[2k \sin(\frac{\pi}{3} + \theta) - 1]$ $T_c = \frac{T_s}{2}[2k \sin(\theta - \frac{\pi}{3}) + 1]$	$T_a = \frac{T_s}{2}[2k \sin\theta - 1]$ $T_b = kT_s \sin(\frac{\pi}{3} - \theta)$ $T_c = T_s[1 - k \sin(\frac{\pi}{3} + \theta)]$
2	$T_a = kT_s \sin(\theta - \pi 3)$ $T_b = \frac{T_s}{2}[1 - 2k \sin\theta]$ $T_c = kT_s \sin(\theta + \frac{\pi}{3})$	$T_a = \frac{T_s}{2}[2k \sin(\frac{\pi}{3} + \theta) - 1]$ $T_b = kT_s \sin(\theta - \frac{\pi}{3})$ $T_c = T_s[1 - k \sin\theta]$	$T_a = \frac{T_s}{2}[1 - 2k \sin(\theta + \frac{\pi}{3})]$ $T_b = \frac{T_s}{2}[2k \sin\theta - 1]$ $T_c = \frac{T_s}{2}[1 - 2k \sin(\theta - \frac{\pi}{3})]$	$T_a = T_s[1 - k \sin\theta]$ $T_b = kT_s \sin(\frac{\pi}{3} + \theta)$ $T_c = \frac{T_s}{2}[2k \sin(\theta - \frac{\pi}{3}) - 1]$
3	$T_a = kT_s \sin\theta$ $T_b = \frac{T_s}{2}[1 - 2k \sin(\theta - \frac{\pi}{3})]$ $T_c = -kT_s \sin(\theta + \frac{\pi}{3})$	$T_a = T_s[1 - k \sin(\theta - \frac{\pi}{3})]$ $T_b = -kT_s \sin(\theta + \frac{\pi}{3})$ $T_c = \frac{T_s}{2}[2k \sin\theta - 1]$	$T_a = \frac{T_s}{2}[1 + 2k \sin(\theta + \frac{\pi}{3})]$ $T_b = \frac{T_s}{2}[2k \sin(\theta - \frac{\pi}{3}) - 1]$ $T_c = \frac{T_s}{2}[1 - 2k \sin\theta]$	$T_a = \frac{-T_s}{2}[2k \sin(\theta + \frac{\pi}{3}) + 1]$ $T_b = kT_s \sin\theta$ $T_c = T_s[1 - k \sin(\theta - \frac{\pi}{3})]$
4	$T_a = -kT_s \sin\theta$ $T_b = \frac{T_s}{2}[1 + 2k \sin(\theta + \frac{\pi}{3})]$ $T_c = kT_s \sin(\theta - \frac{\pi}{3})$	$T_a = \frac{T_s}{2}[2k \sin(\theta - \frac{\pi}{3}) - 1]$ $T_b = -kT_s \sin\theta$ $T_c = T_s[1 + k \sin(\theta + \frac{\pi}{3})]$	$T_a = \frac{T_s}{2}[1 - 2k \sin(\theta - \frac{\pi}{3})]$ $T_b = \frac{-T_s}{2}[1 + 2k \sin(\theta + \frac{\pi}{3})]$ $T_c = \frac{T_s}{2}[1 + 2k \sin\theta]$	$T_a = T_s[1 + k \sin(\theta + \frac{\pi}{3})]$ $T_b = kT_s \sin(\theta - \frac{\pi}{3})$ $T_c = \frac{-T_s}{2}[1 + 2k \sin\theta]$
5	$T_a = -kT_s \sin(\theta + \frac{\pi}{3})$ $T_b = \frac{T_s}{2}[1 + 2k \sin\theta]$ $T_c = kT_s \sin(\frac{\pi}{3} - \theta)$	$T_a = T_s[1 + k \sin\theta]$ $T_b = kT_s \sin(\frac{\pi}{3} - \theta)$ $T_c = \frac{-T_s}{2}[1 + 2k \sin(\theta + \frac{\pi}{3})]$	$T_a = \frac{T_s}{2}[1 + 2k \sin(\theta - \frac{\pi}{3})]$ $T_b = \frac{-T_s}{2}[1 + 2k \sin\theta]$ $T_c = \frac{T_s}{2}[1 + 2k \sin(\theta + \frac{\pi}{3})]$	$T_a = \frac{T_s}{2}[2k \sin(\frac{\pi}{3} - \theta) - 1]$ $T_b = -kT_s \sin(\frac{\pi}{3} + \theta)$ $T_c = T_s(1 + k \sin\theta)$
6	$T_a = kT_s \sin(\theta + \frac{\pi}{3})$ $T_b = \frac{T_s}{2}[1 + 2k \sin(\theta - \frac{\pi}{3})]$ $T_c = -kT_s \sin\theta$	$T_a = \frac{-T_s}{2}[1 + 2k \sin\theta]$ $T_b = kT_s \sin(\frac{\pi}{3} + \theta)$ $T_c = T_s[1 + k \sin(\theta - \frac{\pi}{3})]$	$T_a = \frac{T_s}{2}[1 + 2k \sin\theta]$ $T_b = \frac{T_s}{2}[2k \sin(\frac{\pi}{3} - \theta) - 1]$ $T_c = \frac{T_s}{2}[1 - 2k \sin(\theta + \frac{\pi}{3})]$	$T_a = T_s[1 + k \sin(\theta - \frac{\pi}{3})]$ $T_b = -kT_s \sin\theta$ $T_c = \frac{T_s}{2}[2k \sin(\theta + \frac{\pi}{3}) - 1]$

Table 5.5: Analytical time expression of voltage vectors in different regions and sectors

Sector	Region-1	Region-2	Region-3	Region-4
1	(-1-1-1),(0-1-1), (00-1),(000),(100), (110)(111)	(0-1-1),(1-1-1), (10-1),(100)	(0-1-1),(00-1), (10-1),(100),(110)	(00-1),(10-1), (11-1),(110)
2	(111),(110),(010), (000),(00-1), (-10-1),(-1-1-1)	(110),(11-1), (01-1),(00-1))	(110),(010), (01-1),(00-1), (-10-1)	(010),(01-1), (-11-1),(-10-1)
3	(-1-1-1),(-10-1), (-100),(000),(010), (011),(111)	(-10-1),(-11-1), (-110),(010)	(-10-1),(-100), (-110),(010),(011)	(-100),(-110), (-111),(011)
4	(111),(011),(001), (000),(-100), (-1-10),(-1-1-1)	(011),(-111), (-101),(-100)	(011),(001),(-101), (-100),(-1-10)	(001),(-101), (-1-11),(-1-10)
5	(-1-1-1),(-1-10), (0-10),(000), (001),(011),(111)	(-1-10),(-1-11), (0-11),(001)	(-1-10),(0-10), (0-11),(001),(101)	(0-10),(0-11), (1-11),(101)
6	(111),(101),(100), (000),(0-10), (0-1-1),(-1-1-1)	(101),(1-11), (1-10),(0-10)	(101),(100),(1-10), (0-10),(0-1-1)	(100),(1-10), (1-1-1),(0-1-1)

Table 5.6: Sequence of vectors in different sextants and regions by symmetric modulation

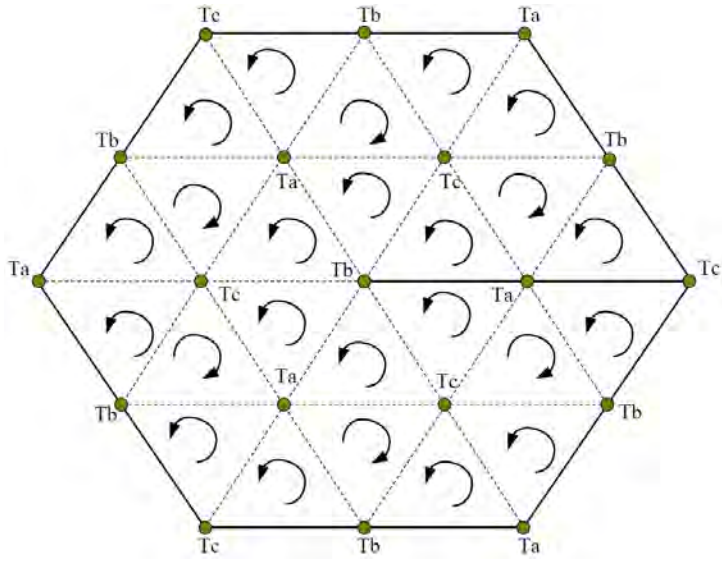


Figure 5.17: Switching sequence for three-level converter

$Voltage\ Vector$	v_0	v_1	v_2	v_0	v_1	v_2	v_0	v_2	v_1	v_0	v_2	v_1	v_0
$Switching\ Time$	$\frac{T_b}{4}$	$\frac{T_a}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_a}{2}$	$\frac{T_c}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_a}{2}$	$\frac{T_b}{2}$	$\frac{T_c}{2}$	$\frac{T_a}{2}$	$\frac{T_b}{4}$
$Switching\ state-phase\ (a)$	-1	0	0	0	+1	+1	+1	+1	+1	0	0	0	-1
$Switching\ state-phase\ (b)$	-1	-1	0	0	0	+1	+1	+1	0	0	0	-1	-1
$Switching\ state-phase\ (c)$	-1	-1	-1	0	0	0	+1	0	0	0	-1	-1	-1

Table 5.7: Time intervals and switching state of first region of first sector

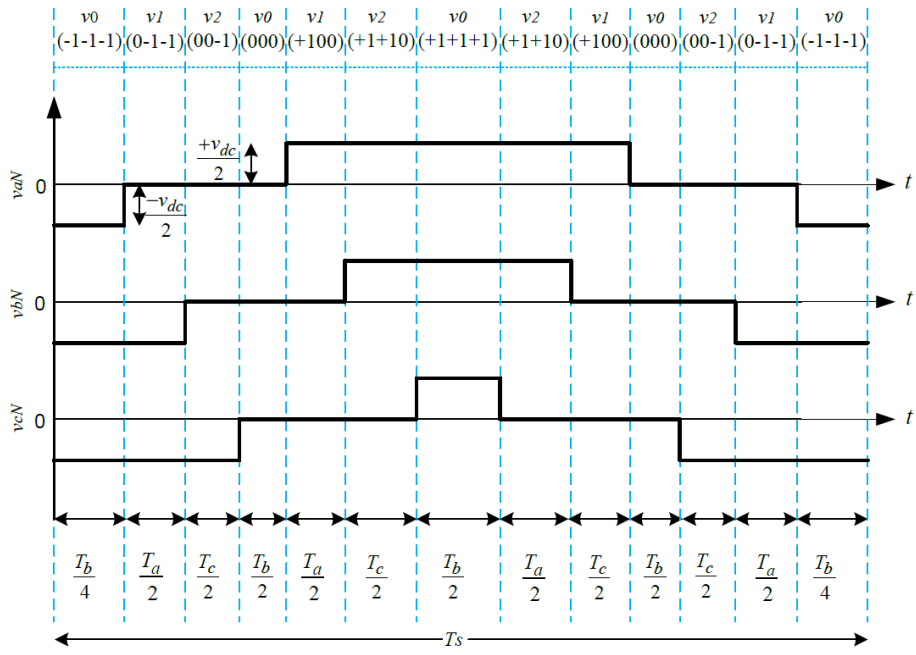


Figure 5.18: Sequence of voltage vectors for the first region of sector (I)

PWM waves. The Turn-on times for different phases can be derived with the help of table 5.5 and figure 5.18 for all the regions in the six sectors.

Table 5.8 shows the segmentation of time intervals and switching state in each phase, whenever voltage vector located in second region of sector (1).

Figure 5.19 shows the corresponding PWM waves of the three phases in second region of sector (1). As shown in figure 5.18 and figure 5.19, the transition from one switching state to the next involves only two switches in the same converter leg, one being turned on and the other turned off. The transition when v_{ref} moves from one sector (or one region) to the next, requires no, or few, additional commutations. Note that, the switching sequence design is not unique, but mentioned points should be satisfied for switching frequency minimization.

5.8 Simulation Results

Simulation results are obtained from the three-level NPC converter controlled by the described SVPWM algorithm, using the "*Power System Blockset*" simulator operating under the Matlab/Simulink environment. For this

Voltage Vector	v_1	v_{13}	v_7	v_1	v_7	v_{13}	v_1
Switching Time	$\frac{T_a}{2}$	T_c	T_b	T_a	T_b	T_c	$\frac{T_a}{2}$
Switchingstate phase(a)	0	+1	+1	+1	+1	+1	0
Switchingstate phase(b)	-1	-1	0	0	0	-1	-1
Switchingstate phase(c)	-1	-1	-1	0	-1	-1	-1

Table 5.8: Time intervals and switching state of second region of first sector

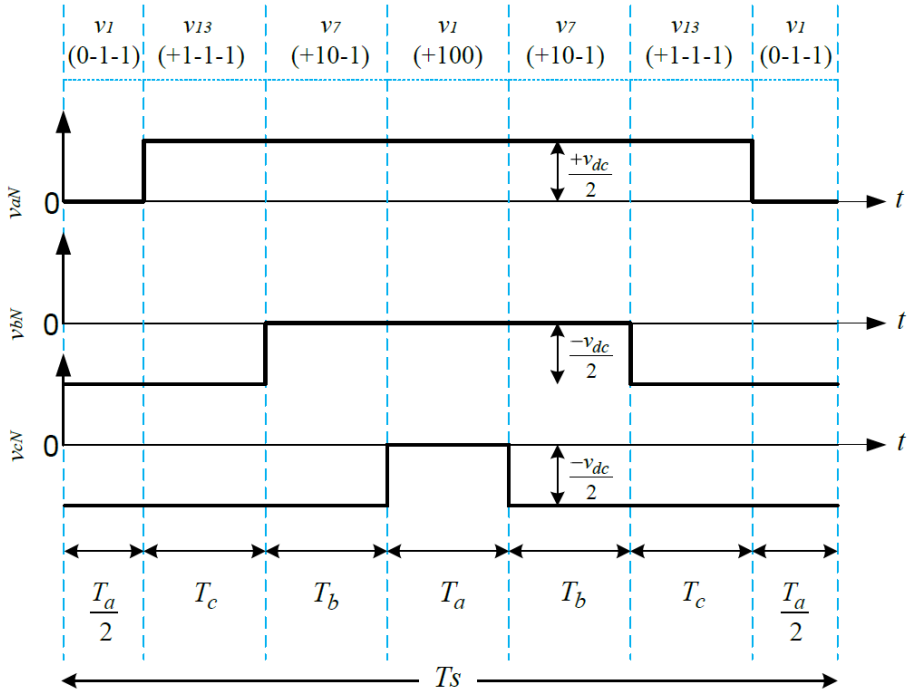


Figure 5.19: Sequence of voltage vectors for the second region of sector (I)

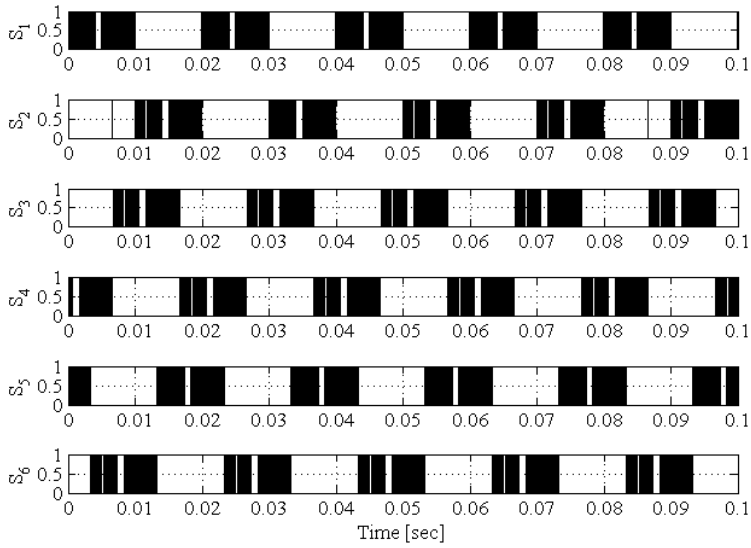


Figure 5.20: Switching state for six upper IGBTs in a NPC converter

example, the converter is supplied by a dc source v_{dc}=1000V, the dc-link capacitors are C=600μF and the switching frequency is f_s=15 kHz.

Figure 5.20 shows the switching states of six upper switches in proposed converter. Figure 5.21 shows the voltages of dc-link capacitors (v_{C1} and v_{C2}) tend to be equal when the modulation index is 0.86.

One of the most important part of implementation of SVPWM in multilevel converters is determines interval of the PWM period based on switching times. By application of the gate signals for each vector over the corresponding of time interval, and fallowing a specific sequence, finally the converter generates the three phase voltage. Figure 5.22 shows the output voltages of phase a (v_{aN}) and line ab (v_{ab}). As shown in figure 5.22, THD of phase and line voltages are 68.38% and 41.39% respectively.

5.9 Conclusions of the Chapter

This chapter introduced the Space Vector PWM switching algorithm for three-phase multilevel converter topologies. Different stages of this algorithm have been presented step by step in different sections. The proposed algorithm is general and applicable to different topologies of converters with

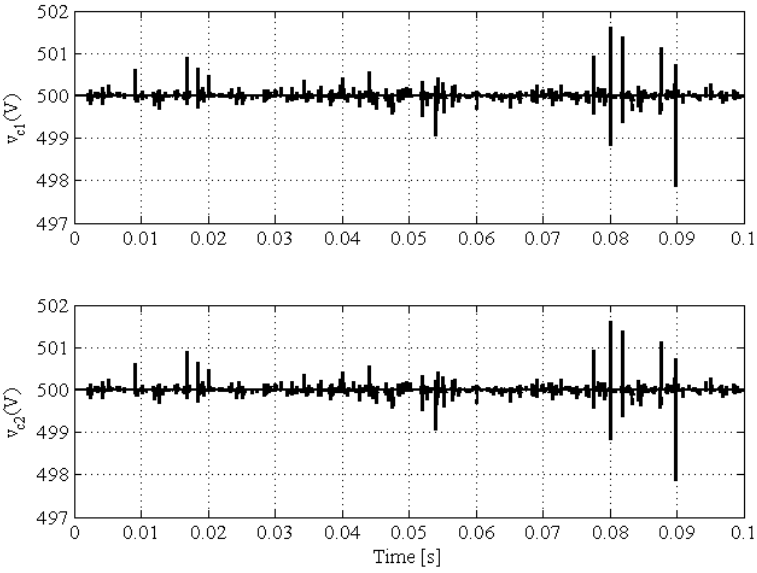


Figure 5.21: Voltage of dc capacitors in a NPC converter

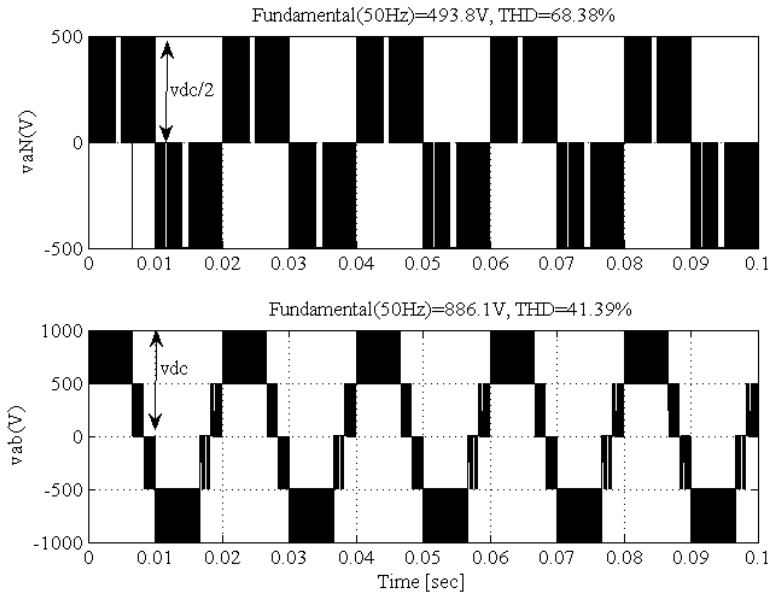


Figure 5.22: Phase and line voltages of NPC converter

any number of levels, since the number of steps involved in computation is always the same regardless of the location of the reference voltage vector. In addition, the efficiency and the ease of implementation of this algorithm make it well suited for software simulation and hardware implementation. Therefore, it can become a very useful tool in further exploration of the properties of multilevel power converters technology in electrical systems.

Chapter 6

ac-Side Current Control and dc-Side Voltage Regulation

6.1 Introduction

This chapter presents a current control approach for the control of the injected current from the ac side of the interfaced converter to the power grid, and also presents voltage regulation of the dc bus and balancing voltage of dc-bus capacitors of this converter.

The current controller is designed to obtain a desirable transient response (low overshoot, fast tracking,...), when compensating dynamic loads. The synchronous frame proportional-integral (PI) current regulator has become the standard for current regulation of the ac side of the DG interface system. As we mentioned in chapter (4), in a synchronous reference frame transformation system with the fundamental excitation, most of the system variables becomes a dc quantity in steady state, that is easily controlled and regulated to the desired value by using a PI controller or other well known controllers, meant to track the step-wise reference signals and reject step-wise disturbances, to control the current. In addition, a PI type compensator for regulate the voltage of dc bus (v_{dc}) at a fixed value in dc side of the converter is needed. In the next step, a technique for balancing the voltage of the dc-bus capacitors must be considered. The chapter is organized as follows: first the design of the current controller for the DG's model control loop is analyzed in section (6.2) using the equations obtained in chapter (4). In section (6.3), two possible modes of operation for dc voltage control unit is presented. In subsections (6.3.1) a technique for regulation of dc voltage of interfaced converter is presented. In addition, a technique for balancing the voltage of the dc-bus capacitors is presented in subsection (6.3.2). On the other hand, different effects of neutral point (NP) voltage oscillation are discussed in subsection (6.3.3). Finally, section (6.4) presents the Space Vector PWM representation of the NPC converter for integration

of DG resources to the power grid.

6.2 Proportional-Integral Current Control Technique

In order to obtain a low overshoot, high accuracy and fast dynamic response to provide load active and reactive power and also harmonic current components of different types of the grid-connected loads, two equations in the equivalent model of the proposed model (4.82) must be controlled in two different and independent loops. As we mentioned before, all the Park-transformed variables of the DG system will become constant value in steady state condition. By this technique, it is possible to design the current controllers using the well known controller design tools meant for regulation problems instead of having to design more complex controllers to track general time-varying reference signals. Therefore, by referring to (4.82) the DG's model equations can be express as:

$$L_c\frac{di_{cd}}{dt} = -R_c i_{cd} + L_c\omega i_{cq} + D_{nd}v_{dc} - v_d \tag{6.1}$$

$$L_c\frac{di_{cq}}{dt} = -L_c\omega i_{cd} - R_c i_{cq} + D_{nq}v_{dc} \tag{6.2}$$

where different terms have been defined before. By considering $\lambda_{dq} = L_c\frac{di_{cdq}}{dt} + R_c i_{cdq}$, the switching state function as the original control inputs of proposed model can be calculated in synchronous reference frame as:

$$D_{nd} = \frac{\lambda_d - L_c\omega i_{cq} + v_d}{v_{dc}} \tag{6.3}$$

$$D_{nd} = \frac{\lambda_q + L_c\omega i_{cd}}{v_{dc}} \tag{6.4}$$

As shown in (6.3) and (6.4), the cross-coupling terms $L_c\omega i_{cq}$ and $L_c\omega i_{cd}$ exist in circuit of current control loop, and the blocks that contain $L_c\omega$ have the objective of decoupling influenced between both current control loops in the d and q-axis. Note that, the original control inputs D_{nd} and D_{nq} consist of combination of a non-linearity cancellation part and a linear decoupling compensation part. To achieve a fast dynamic response and zero steady state errors, especially during connection of non-linear and unbalanced loads to the grid, which utility source is polluted by these types of loads, a PI-type regulator is needed. The parameter of the proposed regulator can be obtained as:

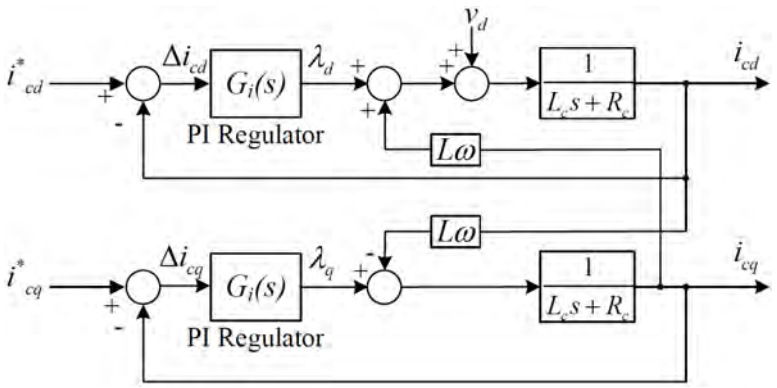


Figure 6.1: Complex vector block diagram of d and q-axis with a decoupling form of the synchronous frame PI current regulator

$$(\lambda_{dq}) = k_p(\Delta i_{cdq}) + k_i \int (\Delta i_{cdq})dt \tag{6.5}$$

where terms k_p and k_i are proportional and integral gains, respectively; and $\triangle(i_{cdq})=(i^*_{cdq}) - (i_{cdq})$ are comparison of the calculated reference currents and the actual DG injection currents generated by the interfaced VSC which create error signals and controls the switches of the converter according to objectives of the interconnection of DG resources to the utility grid. The transfer function of the PI-type regulator for the circuit of current control loops of the proposed strategy is given as:

$$G_i(s) = k_p + \frac{k_i}{s} \tag{6.6}$$

The block diagram of the decoupling form of the synchronous frame PI-type current regulator which is derived from (6.3), (6.4), and (6.6) is shown in figure 6.1 in a synchronous reference frame.

To design of PI regulator in circuit of current controller loops, it is necessary to decouple the proposed model which is shown in figure.6.1 by add the measured voltage of d-axis and cross-coupling terms to figure 6.2.

As shown in figure 6.2, the current loop of i_{cd} and i_{cq} are the same. Therefore, the inner current control loops can be simplified as shown in figure 6.3, [112].

According to the figure 6.3, the close loop transfer function of the current loop can be obtained as:

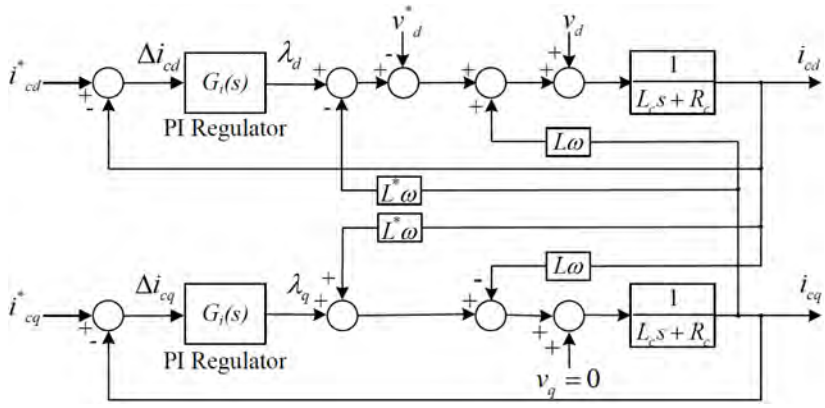


Figure 6.2: Control block diagram of d and q-axis current control loop

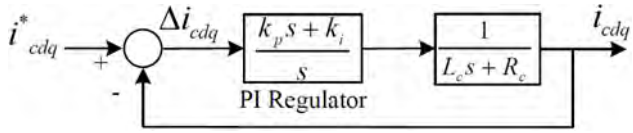


Figure 6.3: Equivalent block diagram of d and q-axis current control loop

$$T_{cdq}(s) = \frac{I_{cq}(s)}{I^*_{cq}(s)} = \frac{I_{cd}(s)}{I^*_{cd}(s)} = \frac{k_p}{L_c} \frac{s + \frac{k_i}{k_p}}{s^2 + \frac{(R_c + k_p)}{L_c} s + \frac{k_i}{L_c}} \tag{6.7}$$

The transient response of the currents will be affected by the presence of the zero in the close loop transfer function of the proposed current loop (6.7), (s=-$\frac{k_i}{k_p}$). To eliminate the effect of zero on transient response in this model a pre-filter $G_p(s)$=$\frac{1}{s + \frac{k_i}{k_p}}$ is added in equivalent block diagram of the proposed current controller as shown in figure 6.4.

Therefore, the response of the current loops becomes that of a second order transfer function with no zero. By comparison between the general equation of a second order transfer function ($\frac{\omega_n^2}{\omega_n^2 + 2\zeta\omega_n s + \omega_n^2}$) and the proposed model (6.7) leads in the following design relations,

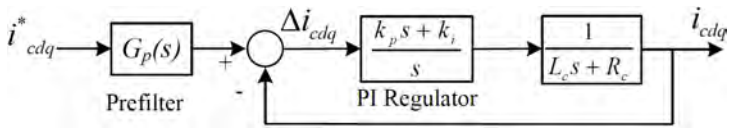


Figure 6.4: Equivalent block diagram of d and q-axis current control loop which added a pre-filter to eliminate the effect of zero on transient response

$$\frac{k_p}{L_c}\frac{s+\frac{k_i}{k_p}}{s^2+\frac{(R_c+k_p)}{L_c}s+\frac{k_i}{L_c}} = \frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \tag{6.8}$$

The transient response of the injected currents from VSC to the grid will be affected by the presence of the zero in (6.7) (s=-$\frac{k_i}{k_p}$). Particularly, the actual percent overshoot will be much higher than expected value. For the optimal value of the damping factor ζ=$\frac{\sqrt{2}}{2}$, the theoretical overshoot is 21%, which is very high [113]. To eliminate the effect of zero on transient response in (6.8) a pre-filter is added as shown in figure 6.4. The response of the current loops becomes that of a second order transfer function with no zero. Comparison between general equation of a second order transfer function ($\frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$) and (6.8) leads to the following design relations:

$$k_p = 2L_c\zeta\omega_n - R_c \;\; and \;\; k_i = L_c\omega_n^2 \tag{6.9}$$

where ζ is damping factor and ω_n is natural un-damped angular frequency and depends on the specific time response. Because of physical limitations, ω_n must be lower than the angular frequency ω_p (ω_p=$2\pi f_p$ with f_p=10kHz) of the modulation carrier wave, which will be the maximum switching frequency of the semiconductor devices. A value of ω_n=$\omega_p/5$ was adopted using based on the theorem of Shannon-Nyquist [114, 115].

A simulation is performed on the proposed model to test the performance obtained using the design controllers. The simulation parameters will be defined completely in chapter 7. The current response of controller to the reference currents is shown in figure 6.5. It can be seen that the actual current tracks the reference trajectory precisely with zero steady-state error and zero overshoot.

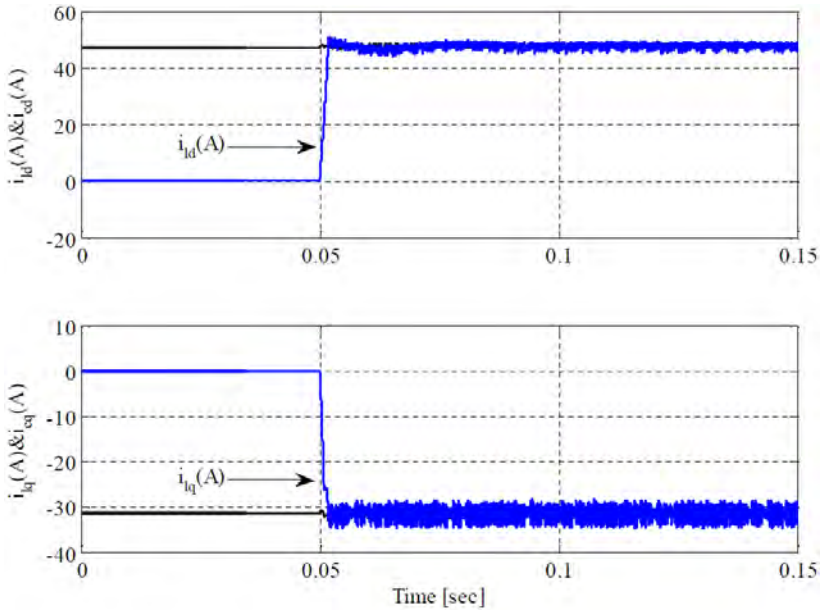


Figure 6.5: Reference and injected currents according to the dynamic performance of the controller

More details of the high performance of this current controller will be presented in the next chapters, during presentation of simulation and experimental results. Note that for the sake of completeness the proposed technique for calculation of the value of grid voltage angle which is presented in chapter (4) used to synchronize the reference frame of DG link to the power grid magnitudes.

6.3 Voltage Regulation

While an average current flows between the dc-bus neutral point and the ac line in a NPC converter topology, voltage unbalance is generated. The dc voltage control unit is designed in NPC converter in order to keep the voltage across the two capacitors balanced and equals to given reference. For this case, a PI regulator is performed, that its input is the capacitor voltage error ($\triangle v{=}v_{dc}^{*} - v_{dc}$). If the two voltages are different, it means that the blocking voltage of upper and lower controlled switches are not equals. They are two possible modes of operation for dc voltage control unit:

a. If the total dc-bus voltage needs to be adjusted.

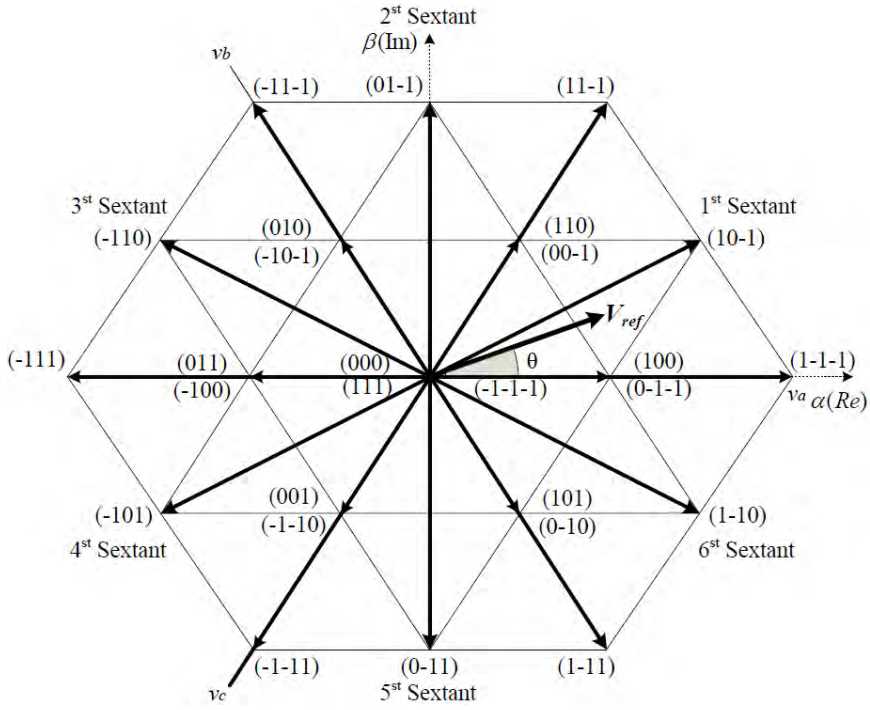


Figure 6.6: Space vector diagram of the three-level NPC converter

b. If only one of the voltage capacitor presents and error larger than a predefined value.

If the total voltage across the dc bus needs to be modified to follow the reference value, any of the 27 switching combinations shown in figure 6.6 can be applied to the NPC VSC. On the other hand, if it is necessary to change the voltage across the one of upper or lower capacitor, then the control scheme must select the switching combination that allows charging or discharging the given capacitor.

6.3.1 dc-Bus Voltage Regulation

The error value of the dc bus voltage ($\triangle v{=}v^*_{dc} - v_{dc}$) is passed through a PI type compensator for regulate the voltage of dc bus (v_{dc}) at a fixed value. Therefore, u_{dc} will be obtained as:

$$u_{dc} = k_1 \Delta v_{dc} + k_2 \int \Delta v_{dc} dt \tag{6.10}$$

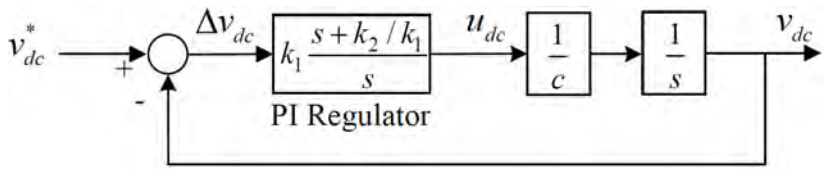


Figure 6.7: Control loop of the dc-bus voltage

where k_1 and k_2 are proportional and integral gains of PI regulator. Figure 6.7 shows the equivalent control circuit loop of the dc bus voltage for proposed converter. The closed loop transfer function of the dc voltage regulation loop, got from figure 6.7, has the following form,

$$\frac{v_{dc}(s)}{v^*_{dc}(s)} = 2\zeta\omega_{nv}\frac{s+\frac{\omega_{nv}}{2\zeta}}{s^2+2\zeta\omega_n s+\omega_n^2} \tag{6.11}$$

where the proportional and integral gains components are derived from:

$$k_1 = 2\zeta\omega_{nv}c \quad and \quad k_2 = \omega_{nv}^2 c \tag{6.12}$$

.

The control effort is obtained from (6.13) as:

$$i^*_{do} = \frac{u_{dc} - D_{nq}i_q}{D_{nd}} = \frac{u_{dc}v_{dc} - D_{nq}v_{dc}i_q}{D_{nd}v_{dc}} \tag{6.13}$$

However, by assuming an ideal condition for the current loop and in normal operation of the DG system, the following properties will be obtained as,

$$D_{nq}v_{dc} \approx v_q \quad and \quad D_{nd}v_{dc} \approx v_d \tag{6.14}$$

On the other hand, assuming the three-phase grid voltages are given by (6.15)-(6.17),

$$v_1 = v\cos(\omega t) \tag{6.15}$$

$$v_2 = v\cos(\omega t - \frac{2\pi}{3}) \tag{6.16}$$

$$v_3 = v\cos(\omega t - \frac{4\pi}{3}) \tag{6.17}$$

The transformation to the synchronous reference frame yields,

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = T_{dq}^{12} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \sqrt{\frac{3}{2}} \begin{bmatrix} v \\ 0 \end{bmatrix} \tag{6.18}$$

as a result, $D_{nq}v_{dc} \approx v_q{=}0$ and $D_{nd}v_{dc} \approx v_d{=}\sqrt{\frac{3}{2}}\ v$
hence, the control effort can be approximated by (6.19).

$$i_{d1h+} \approx \sqrt{\frac{2}{3}} \frac{v_{dc}}{v} u_{dc} \tag{6.19}$$

The reference current in (6.19) is added to the reference current of the loop of i_{ld}. i_{d1h+} is a dc component and it will force the DG system to generate or to draw a current at the fundamental frequency. Further, by designing the dc voltage loop much slower than the currents one, there would not be any interaction between the two loops [101].

6.3.2 Balancing Voltage of dc-Bus Capacitors

As mentioned in previous section, the two capacitors in series share the dc bus voltage equally between them, under ideal conditions. However, due to difference in bulk and leakage resistances of cascaded capacitors, the voltage sharing under steady state may not be equal. An electric equivalent schematic as shown in figure 6.8 of an electrolytic capacitor can be described as an equivalent series resistance (ESR), equivalent series inductance (ESL), the capacitance (C) and a parallel resistance for the leakage current (R_{leak}) depends on the quality of the dielectric. When using series connections, it is important to know the voltage across each capacitor. The tolerance of a capacitor can give a very high voltage on one capacitor while the others are subjected to lower voltages. To obtain correct voltage sharing between the capacitors, it is a good idea to use voltage sharing breeder resistors. The voltage sharing resistor (R_{eq}) can be calculated as:

$$R_{eq} = \frac{100}{0.015 \times c(\mu F)} k\Omega \tag{6.20}$$

where C is the capacitance in μF [116]. It is important to have a high quality resistor and the tolerances of the two breeder resistors should be better or equal to $\pm 5\%$. The connection diagram of voltage sharing resistors is shown in figure 6.8.

A simulation is performed on the proposed model to test the performance obtained using the design controllers. For this case, a dc voltage of 1000

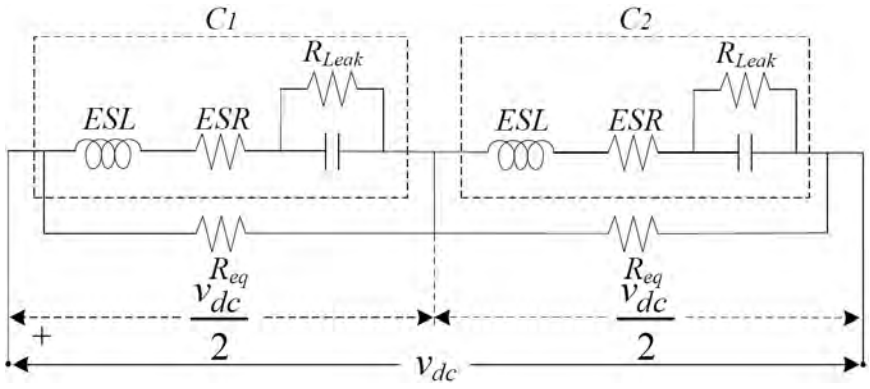


Figure 6.8: Equivalent circuit of capacitor with voltage sharing breeder resistance

(V) is applied to the dc side of converter. Figure 6.9 shows the voltages of dc-link capacitors (v_{c1} and v_{c2}) tend to be equal.

6.3.3 Effects of Neutral Point (NP) Voltage Oscillation

The low frequency distortion is generated in ac current by the oscillation in NP voltage. Such distortion can weaken by feed-forward modulation, but it will be impossible to keep this voltage at a constant value, while the converter controls the total the dc-link voltage. As a result, some oscillation will be generated in the reference of the transformed currents which it produce distortions in the ac currents of the interfaced converter. Hence, this distortion cannot be eliminated completely by feed-forward modulation, since it is inherent in the current references considered by controller. More details are indicated in following, according to current and voltage components, and power of each part in figure 6.10.

As mentioned in chapter 4, the instantaneous power of ac and dc-side of interfaced converter can be expressed as:

$$p_{ac} = v_{1M}i_{c1} + v_{2M}i_{c2} + v_{3M}i_{c3} = v_{dM}i_{cd} + v_{qM}i_{cq} \tag{6.21}$$

$$p_{dc} = v_{dc}i_{dc} \tag{6.22}$$

and by considering efficiency of 100% for proposed model, power of ac side will be calculated as:

$$p_{ac} = p_{dc} - \Delta p_c \tag{6.23}$$

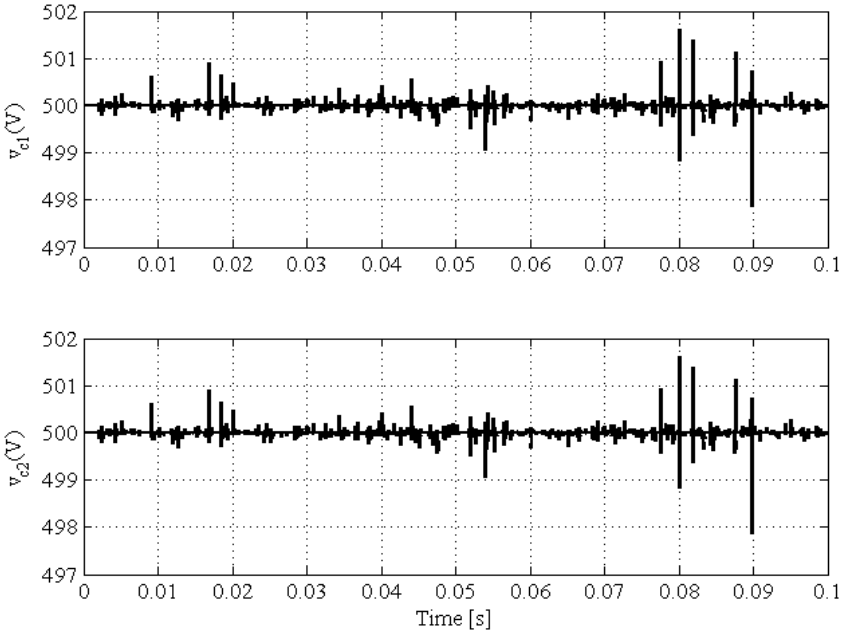


Figure 6.9: Voltage of dc bus capacitors

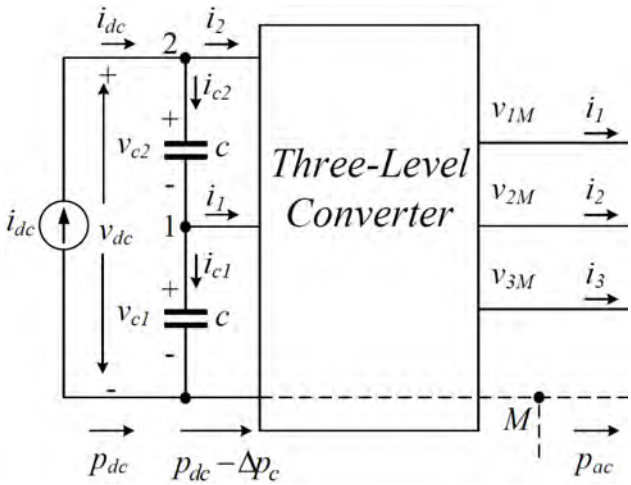


Figure 6.10: Voltage and current components in NPC converter

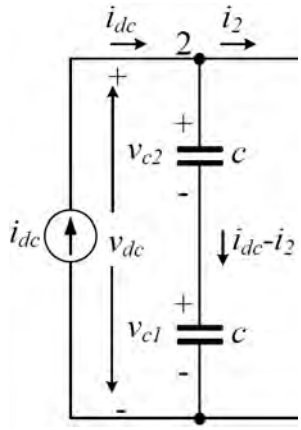


Figure 6.11: dc-side of interfaced converter while NP current is zero

where $\triangle p_c$ is related to the variation of energy in the cascaded capacitors in dc side of the converter. Therefore, this term can be considered as a term which is related to changes of energy and it is equal to:

$$\Delta p_c = \frac{d\varepsilon}{dt} = v_{dc}(i_{dc} - i_2) - v_{c1} i_1 \tag{6.24}$$

Neutral point current is zero($i_1 = 0$)

Figure 6.11 shows the schematic diagram of proposed converter while the NP current is zero. By this consideration, $\triangle p_c$ can be obtained as:

$$\Delta p_c = v_{dc}(i_{dc} - i_2) = v_{dc}\frac{c}{2}\frac{dv_{dc}}{dt} \tag{6.25}$$

By considering the dc-link voltage equal to a constant value, $\triangle p_c$ will be obtain equal to zero. Therefore, the variations of energy in the capacitors are zero, and by referring to (6.23), the value of instantaneous power p_{ac} and p_{dc} will be equal. In addition, by taking into considering a constant value for i_{dc} in the steady state condition:

$$p_{ac} = p_{dc} = v_{dc} i_{dc} = constant \tag{6.26}$$

Therefore, a constant value of instantaneous power will be obtained in ac side of the converter, and the ac injected currents will not include low frequency distortions. In this condition, the controller can achieve the constant dc-link voltage value and the ac currents with no distortion simultaneously.

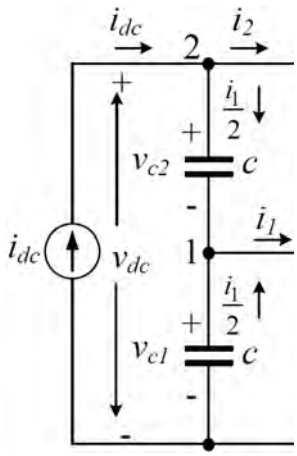


Figure 6.12: dc-side of proposed converter while NP current is not zero

Neutral point current is not constant ($i_1 \neq 0$)

Taking into considering a constant value for the dc-link voltage is achieved by controller, therefore; the currents in the upper and lower capacitors are equal to $\frac{i_1}{2}$. According to figure 6.12, $\triangle p_c$ can be calculated as:

$$\Delta p_c = v_{dc}\frac{i_1}{2} - v_{c1}i_1 = (\frac{v_{dc}}{2} - 2c\frac{di_1}{dt})i_1 \tag{6.27}$$

For this condition, the value of p_{dc} is not equal with p_{ac}. By considering a constant value for i_{dc} in steady-state condition, the values of p_{dc} and p_{ac} will be expressed as:

$$p_{dc} = v_{dc}i_{dc} = constant \tag{6.28}$$

$$p_{ac} = f(i_1) \neq constant \tag{6.29}$$

According to (6.29) we can conclude that p_{ac} is not constant, therefore; the injected ac currents will contain low-frequency distortions. As a result, the controller cannot achieve the dc-link voltage and the non-distortion in the ac currents simultaneously.

We can conclude that, it is impossible to keep the constant value for dc-link voltage without introducing distortions in the instantaneous ac power, while local average neutral point current is not zero.

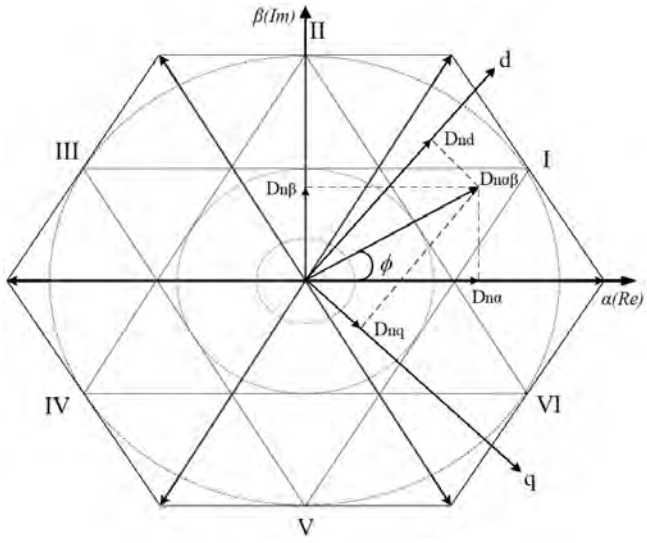


Figure 6.13: Voltage space phasors and related switching states

6.4 Space Vector PWM Representation of the Three-level VSC

Many modulation techniques are studied to realize switching state functions in a synchronous rotating reference frame i.e. D_{nd} and D_{nq} . Among several modulation strategies, in the three-phase three-wire systems to control NPC VSC, space-vector PWM (SVPWM) stands out, because it offers significant flexibility to optimize switching waveforms and reduces the switching losses by limiting the switching to the two thirds of the pulse duty cycle, as a converter's gating signals generators [100]. In order to make an appropriate selection of the D_{nd} and D_{nq}, the space phasor plane is first subdivided into six 60^o sectors 1,2,...,6. Figure 6.13 shows the instantaneous magnitude and angular velocity of switching states function, controlled by selecting a particular voltage vector depending on its present location. The vectors D_{nd} and D_{nq} are consisted of information of power grid during different conditions and they obtained by monitoring the grid current and voltage components continuously. After that, these components are applied to the control algorithm for compensation of the grid components according to the defined objectives. In the next step, D_{nd} and D_{nq} are transformed into the $\alpha\beta$ reference frame, as input components of SVPWM, for switching of transistors according to objectives.

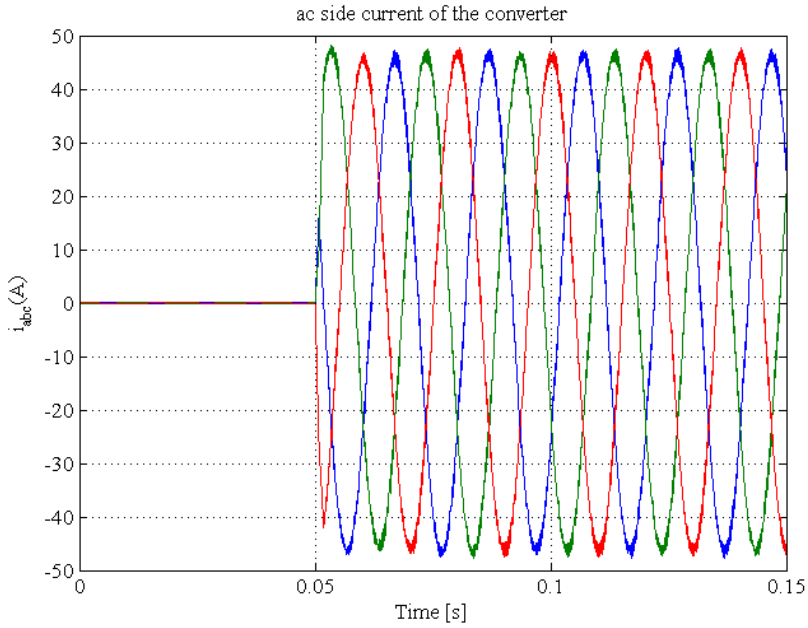


Figure 6.14: Evaluation of the ac side current of the interfaced converter in the abc reference frame

A simulation is performed on the proposed model to evaluate the performance of the control scheme. Figure 6.14 shows the injected currents of the grid connected converter for supply a linear RL load. As shown in this figure, a high power-quality current injection is yielded with the proposed current control scheme.

6.5 Conclusions of the chapter

This chapter has presented a designed current control algorithms for a VSC-based DG interface, and a voltage regulator for dc bus voltage regulation of interfaced converter. In addition, a technique for balancing the voltage of dc bus capacitors is presented. The current control algorithm and dc voltage regulator have been applied to the case of interfaced converter's output current control, and dc bus voltage regulation, during connection to the power grid. The proposed current controller is based on PI compensator of DG system using decoupled current loops in dq referential and the non-linear dc voltage loop is well suited to compensate for non-linear load current

components. The controller shows adequate tracking performance and good dynamic response during connection to the grid.

Chapter 7

Simulation Analysis and Results

7.1 Simulation Test Results

In order to demonstrate the high performance of the proposed non-linear control technique of the DG interface (NPC VSC) for integration of DG resources to the power grid, the complete system model was simulated using the "*Power System Blockset*" simulator operating under the Matlab/Simulink environment. The schematic diagram and principle of the proposed control technique in an ac grid is shown in figure 7.1. The network parameters, including the ratings and impedances of system components for simulation analysis, are given in table 7.1. The test model contains a power converter with power rating of 20 kVA. The maximum available value of DG source active power is of 8 kW, which is also the active power reference included in the simulations. The main purposes of the simulation are to study different performance aspects in different conditions. At first, capabilities of DG resources and flexibility of control strategy for control of interfaced VSC in providing active, reactive, unbalanced and harmonic current components of different loads are shown, and the capabilities of control method on reactive power tracking with constant output active power are considered. In addition, the simulated results have been used to analyze the Total Harmonic Distortion (THD) of the utility grid current amid severe varying load conditions. During the simulation process, constant dc voltage sources have been considered as a DG source. In addition the active power which is delivered from the DG resources via interfaced converter to the ac grid is considered to be constant. This assumption makes it possible to evaluate the capability of the control strategy to track the fast change in the active and reactive power, independent of each other. For this purpose, when one of them is changed, another one must be constant. To simulate a real ac grid, the load is connected and disconnected to power grid randomly and grid current waveform will be compared with each other under various loads and conditions.

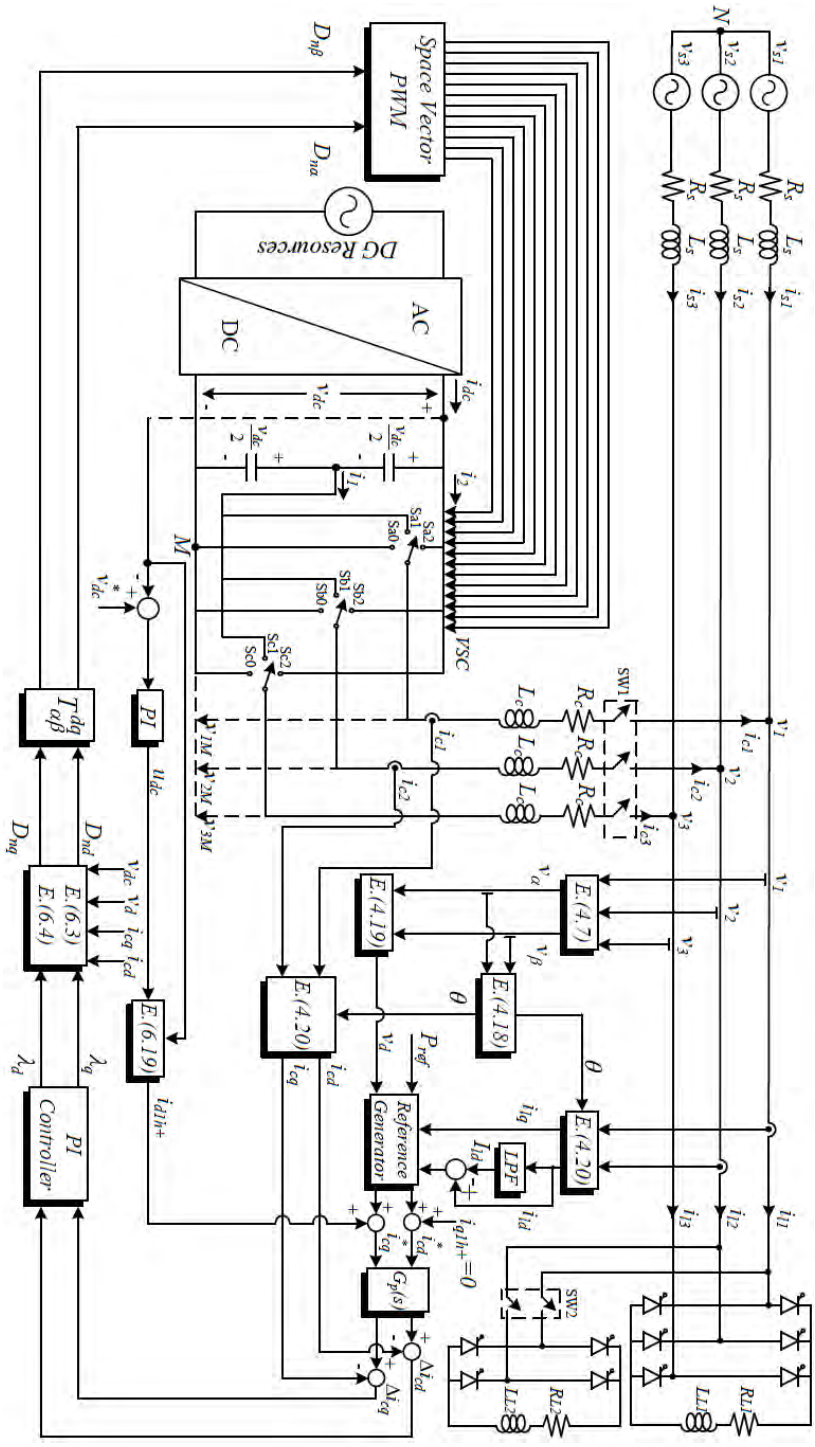


Figure 7.1: General schematic diagram of the proposed control method

Parameter	Value
Grid voltage (v_s)	400 V
dc-link voltage set-point (v_{dc})	800 V
Fundamental frequency	50 Hz
Switching/Sampling frequency	15 kHz
Interfacing inductance (L_c)	4.6 mH
Interfacing resistance (R_c)	0.1 Ω
Line resistance (R_s)	0.1 Ω
Line inductance (L_s)	0.1 mH
Linear load active power	8 kW
Linear load reactive power	6 kvar
Non-linear load resistance (R_L)	20 Ω
Non-linear load inductance (L_L)	10 mH
(S_{ref})	20 kVA
(P_{ref})	8 kW

Table 7.1: Simulation parameters

7.1.1 Connection of DG link to the power grid to supply harmonic currents components and non-linear load increment

In this mode, the system frequency is dictated by the utility grid, and the tracking and regulation performances of DG unit are examined in the grid-connected condition.

Prior to the connection of DG system to the ac grid, a full-wave thyristor converter supplies a load with resistance of 20 Ω and 10 mH inductor in each phase. This load is considered as a sensitive load that should be serviced continuously. This non-linear load draws harmonic current from the ac grid continuously. The DG link is connected to the ac grid at t=0.1 sec. This process is continued until t=0.2; at this moment another full-wave thyristor converter similar to the prior load is connected to the grid and it is disconnected from the grid at t=0.35 sec. Figure 7.2 shows the load voltage (v_l), load current (i_l), grid current (i_{grid}), and DG current (i_{DG}) in phase (a). As shown in this figure, after connection of DG link to the ac grid at t=0.1 sec, the grid current becomes zero and all the active and reactive current components including fundamental and harmonic frequencies are provided by DG link (i_{grid}=i_{load}-i_{DG}). In this case, the load current is completely equal to reference current of converter, therefore VSC injects the maximum available power of DG source to the power grid. Therefore, the injected

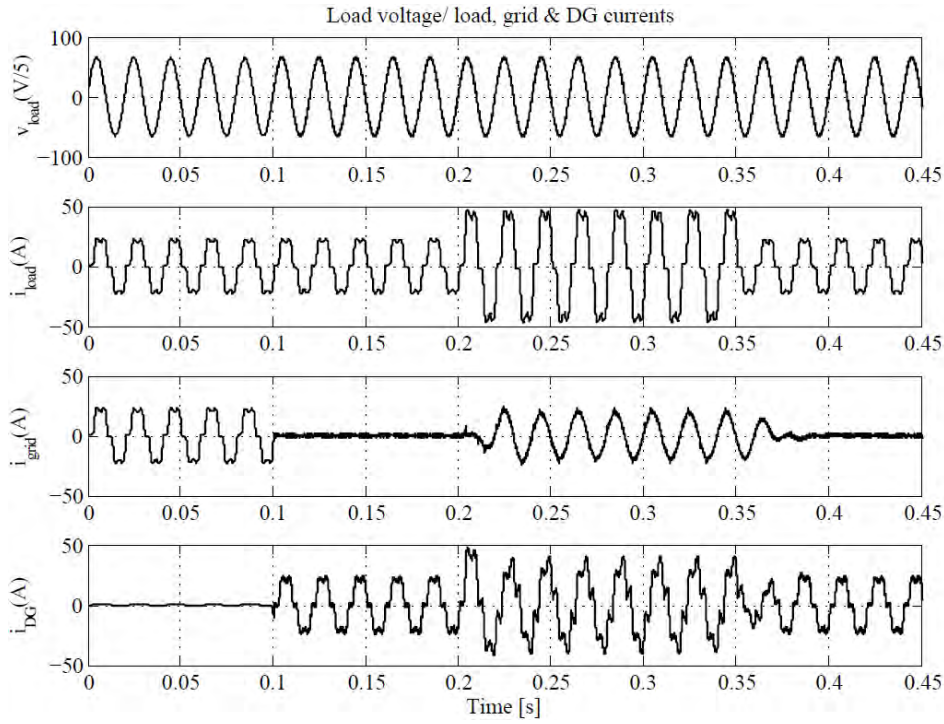


Figure 7.2: Load voltage, load, grid, and DG currents before and after connection of DG and before and after connection and disconnection of additional load to the grid

current from grid will be zero. The load current is fed from non-linear link continuously until connection of additional load similar to prior load to the grid.

Figure 7.3 shows, after connection of additional load to the power grid at t=0.2 sec, converter injects the maximum active and reactive power by connection of DG source to the grid. But, in this case the maximum power of interfaced converter is less than the power which is needed to supply the grid-connected loads. Therefore, remained power is injected by utility grid. As shown in this figure, the utility grid injects high power quality current waveforms even under the connection of non-linear loads to the grid, and load harmonic currents are provided by DG. There are some sharp edges on current waveforms which are related to high order harmonic frequencies and created during switching of thyristor converters. In addition, the production in control circuit of DG system is delayed for around one cycle. This is due

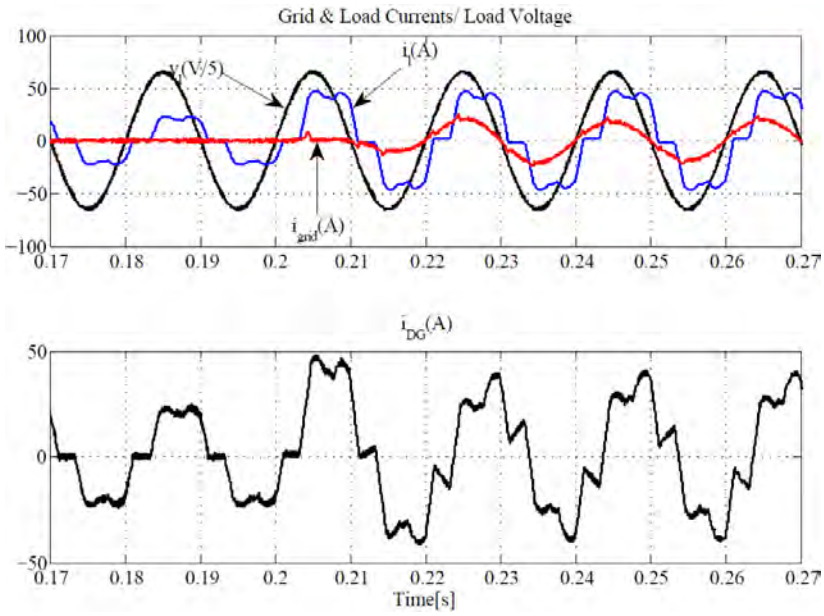


Figure 7.3: Grid, load, DG currents and load voltage before and after connection of additional load

to the settling time of MPHPF filter, which has been mentioned completely in chapter (4).

Figure 7.4 shows, with the same delay as before, additional load is removed at t=0.35 sec. As shown in this figure, after the pass of the transient times the injected current from grid to the load becomes zero, and DG link supplies all the required power for supply the non-linear load.

Figure 7.5 shows after the transient times during connection of additional load to the main grid, the load voltage and grid current are in phase and the grid does not need to provide reactive and harmonic currents for the load which is shown for three phases.

The ability of control loop to track the references current trajectories of d-axis and q-axis, for the duration of connection of DG link to the grid and for the period of connection of additional load to the grid, are shown in figures 7.6 and 7.7. Figure 7.6 shows, before connection of additional load to the grid, the actual d-axis and q-axis current components of DG's control loop track their reference trajectory precisely.

But, according to figure 7.7, after connection of additional load to the grid, the actual d-axis current component of DG tracks half of its reference

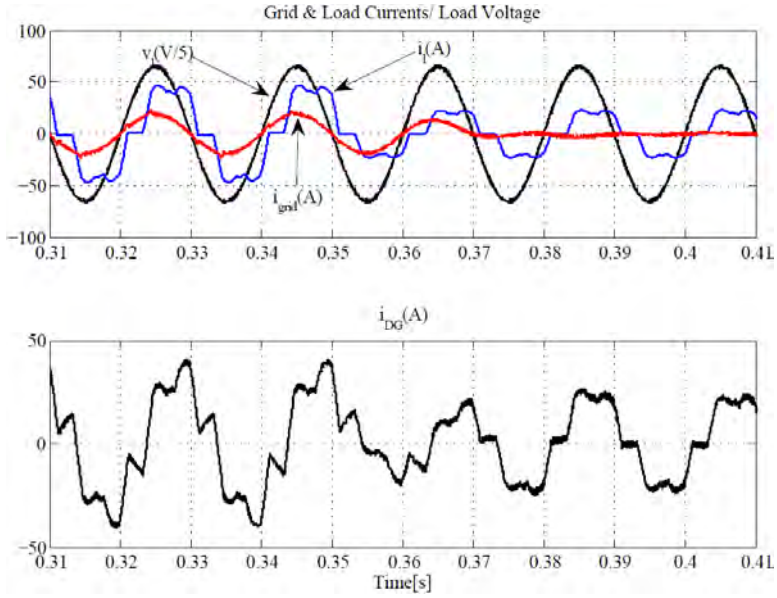


Figure 7.4: Grid, load, DG currents and load voltage before and after disconnection of additional load

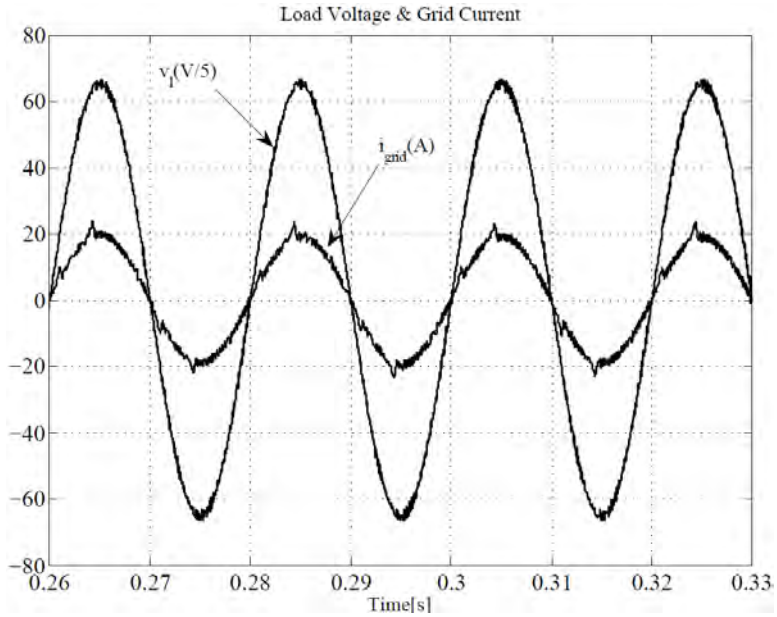


Figure 7.5: Phase-to-neutral voltage and grid current for phase (a)

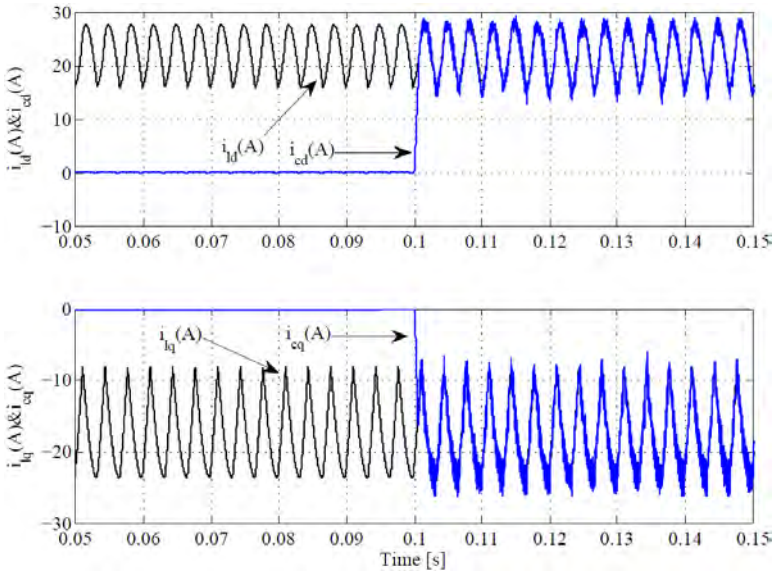


Figure 7.6: Reference currents track the load current after interconnection of DG resources to the grid

trajectory which is equal to its maximum active power (reference active power) and all the reference trajectory of reactive current changes. The other part of active power is injected by utility grid.

To evaluate the capabilities of DG link to compensate harmonic currents, the spectra of currents before and after connection of DG link and after connection of additional load are shown in figures 7.8-7.10. Figure 7.8 shows that before connection of additional load to the PCC, the THD of load currents which is supplied by utility grid is 22.97%. This value is also equal to the THD of grid currents. After connection of additional load to the PCC, this value is 21.35%, as figure 7.9 indicates. Figure 7.10 shows that the THD of grid current after connection of additional load is just 4.18%, and the other value injected by DG to the grid. The comparison between this information demonstrates capabilities of DG link to compensate harmonic currents of the non-linear grid-connected loads.

The trajectory of the load, grid, and DG currents in $\alpha\beta$ representation are shown in figures 7.11-7.13. Figure 7.11 shows the trajectory of the load currents in $\alpha\beta$ representation, which is required to supply the load, before and after connection of additional load to the PCC. It can be seen that, the ac currents are containing some harmonic currents distortion for feed

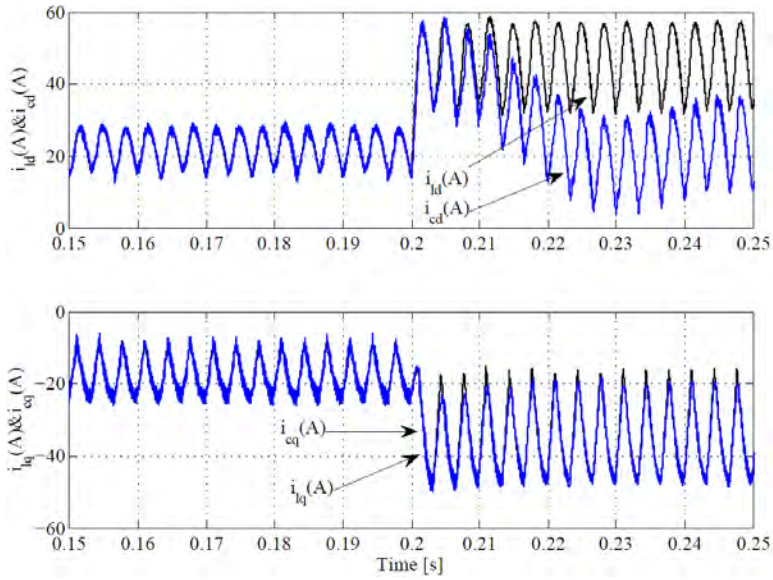


Figure 7.7: Reference currents track the load current after additional load increment

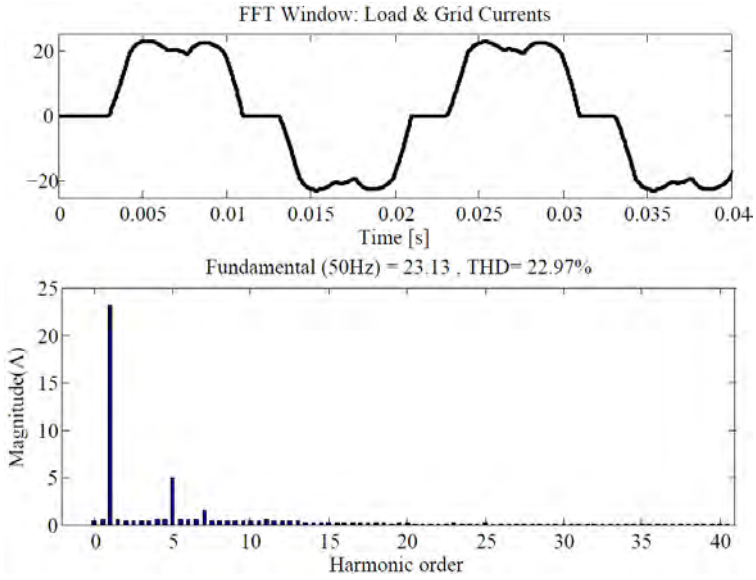


Figure 7.8: Load current spectra before connection of DG link to the grid

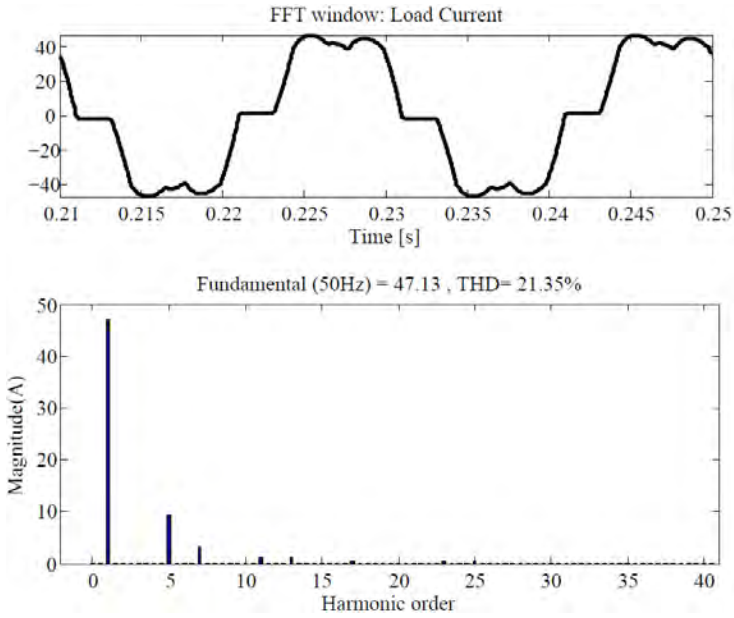


Figure 7.9: Load current spectra after connection of additional load to the grid

forward modulation, therefore the $\alpha\beta$ representation of those currents is not circular and is hexagonal. In addition, after the second load similar to first load is connected to the ac grid, radius of external hexagonal is exactly two times greater than radius of internal hexagonal. Figure 7.12 and figure 7.13 show the trajectory of the grid and DG currents in $\alpha\beta$ representation, after connection of additional load to the ac grid. As it can be seen in figure 7.12, after connection of additional load to the PCC, the grid current does not contain significant low-frequency distortion for feed forward modulation, since the $\alpha\beta$ representation of those currents is approximately circular. Figure 7.13 shows that, after connection of second load to the grid, DG link supplies the harmonic current components of d and q-axis and half of active power and whole the reactive power of the grid-connected loads.

The simulation results in figures 7.8-7.13 indicated that the proposed DG link can provide required harmonic load currents of non-linear loads. Therefore, by reducing THD of grid current it can act as an active power filter.

Figure 7.14 and figure 7.15 show the active and reactive power components which pass through the electrical network during integration of DG resources to the grid and during connection and disconnection of the additional load

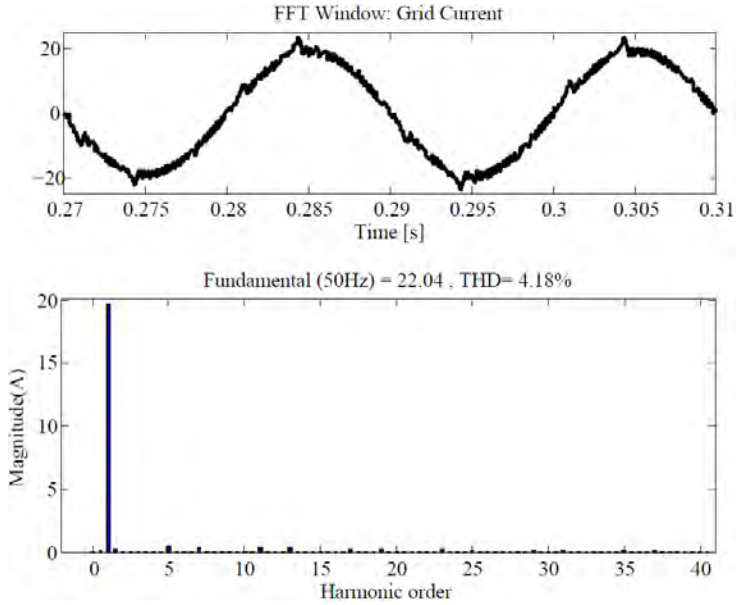


Figure 7.10: Grid current spectra after connection of additional load to the grid

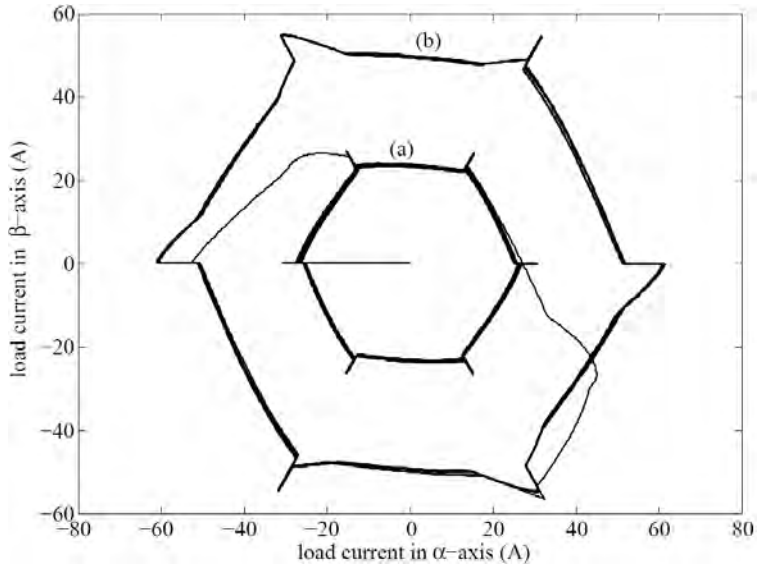


Figure 7.11: Trajectory of load current before and after connection of additional load to the grid in $\alpha\beta$ representation

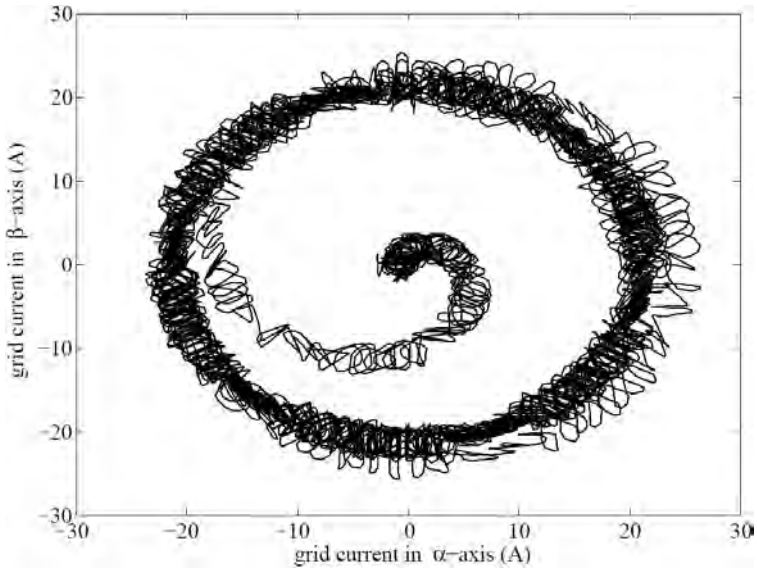


Figure 7.12: Trajectory of grid current after connection of additional load to the grid in $\alpha\beta$ representation

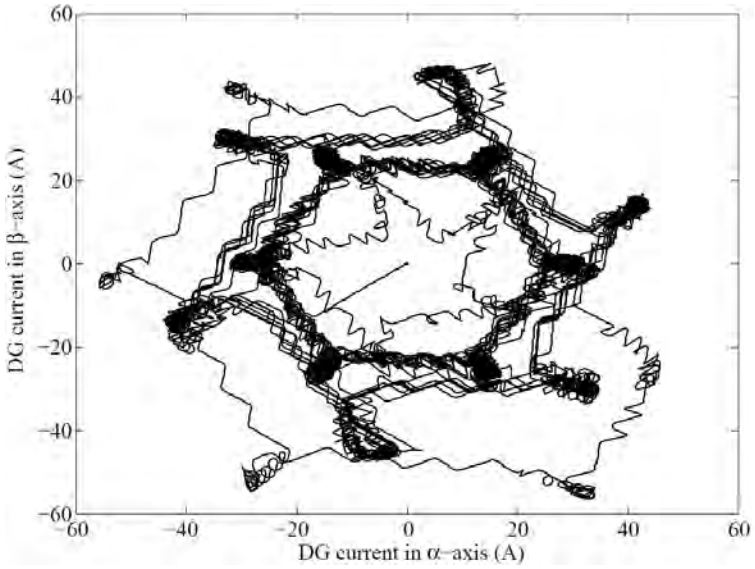


Figure 7.13: Trajectory of DG currents during connection of additional load to the grid in $\alpha\beta$ representation

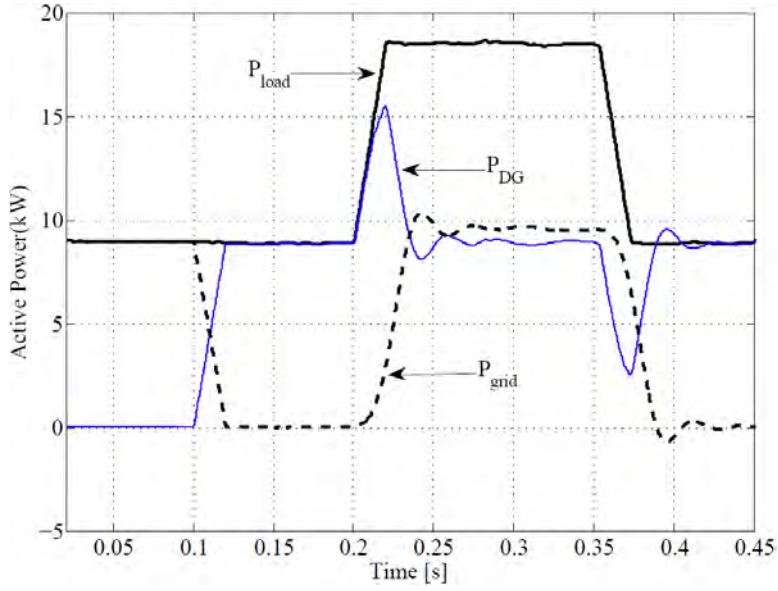


Figure 7.14: Grid, load and DG active power, during integration of DG resources to the grid, before and after connection and disconnection of additional load to the grid

to the grid. Figure 7.14 shows grid, load and DG link active power during integration of DG link and connection and disconnection of an additional load to the grid. As one can predict, the waveform of active power of DG link contains a step response which is related to MPHPF. Therefore, the delay and swings in this wave are due to the same reasons mentioned above. In addition, after connection of DG link to the grid the active power which is delivered from grid is decreased to the zero value and DG link delivered active power, completely tracking load active power precisely. Due to delay settling time of MPHPF, after connection of additional load at t=0.2 sec, some swings appear in active power waveform. The transient time takes around one cycle (0.02 sec). As shown in this figure, the rate of changes in active power of DG has fast slope at t=0.1 sec. That is due to, before interconnection of DG link to the grid, the DG control circuit has some information about the nature of grid-connected loads.

Figure 7.15 indicates grid, load and DG link reactive power which pass through the network during integration of DG link and connection and disconnection of an additional load to the grid. As mentioned before in chapter (4), there is no filter in the control loop of q-component of DG link reference

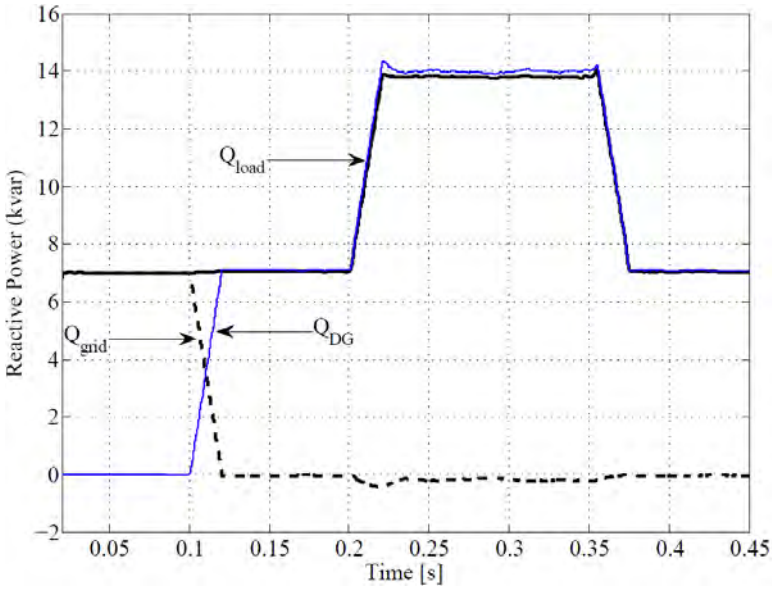


Figure 7.15: Grid, load and DG reactive power, during integration of DG resources to the grid, before and after connection and disconnection of additional load to the grid

current, therefore; the waveform of DG reactive power has better response than DG's active power response. This figure also shows the capability of DG system to track and compensate load reactive power, completely. In addition, this can prevent load voltage fluctuations in case of sudden change in load reactive power.

7.1.2 Linear load increment

In this section, to evaluate the DG link performance to track both harmonic and sinusoidal current components simultaneously, a linear RL load is connected to grid at t=0.45 sec in parallel with previous non-linear load, and it is removed at t=0.6 sec. The related simulation results are shown in figures 7.16-7.29.

In this case, additional load is a resistive-inductive load which is connected to the non-linear load in parallel. Maximum delivered power from DG system is considered constant ($P_{ref} = 8kW$). Considering that all required reactive power of additional load is provided by DG link, additional required load active power must be provided by the main grid.

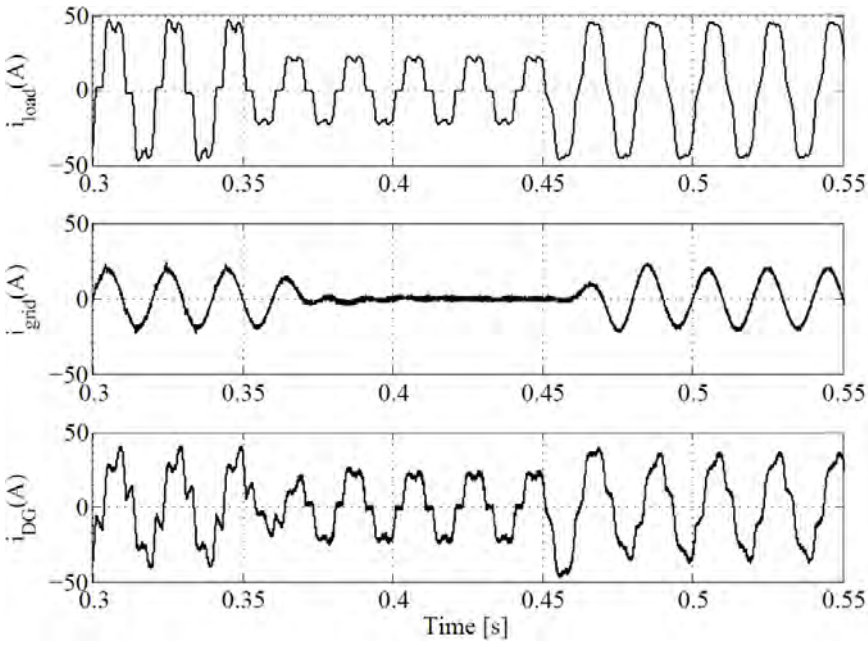


Figure 7.16: Load, grid and DG link currents before and after connection of additional RL load to the grid

Figure 7.16 shows load current, grid current and non-linear DG link current during linear load increment. As shown in this figure, at t=0.45 sec, an additional load is connected to the ac grid and due to delay settling time of MPHPF filter, production in DG link circuit is started around 0.02 second delay after linear load connection. According to figure 7.16, converter injects its maximum power to the grid, therefore some part of load active power, whole reactive power, and harmonic current components of the loads are provided by DG link. Therefore, remained active power is injected by utility grid. It can be seen that, the utility grid injects high power quality current waveforms even under the connection of linear and non-linear loads to the grid.

The reference currents in dq frame, which are equal to d and q-components of the load current, are shown in figure 7.17. The step response of the MPHPF which causes the delay in the control circuit of DG link is apparent from this shape.

After production in DG link control circuit, load voltage and grid current become in phase which is shown for phase (a) in figure 7.18. Therefore,

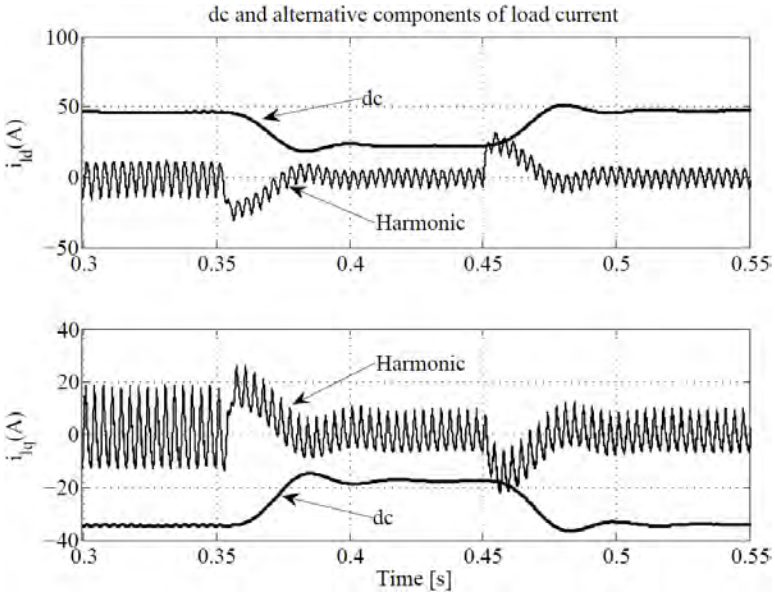


Figure 7.17: d and q- components of load currents before and after connection of additional RL load to the grid

utility grid does not provide reactive power components to supply the grid-connected loads.

The additional RL load is removed at t=0.6 sec. As shown in figure 7.19, after the pass of the transient times the grid current become zero, and DG link injects whole the required power to supply the grid-connected load.

Figure 7.20 shows the THD after connection of additional RL load to the ac grid is 12.92%.

Figure 7.21 shows that the grid current THD in this period is just 3.43% which illustrates the potential of DG link to compensate considerable amount of harmonic frequencies.

Figure 7.22 shows after disconnection of additional linear load at t=0.6 sec from the grid, the load, DG link and grid currents return to their prior values.

The reference currents in dq frame, which are equal to d and q-components of the load current, are shown in figure 7.23.

Figure 7.24 shows the trajectory of the load currents in $\alpha\beta$ representation, required to supply the load, after connection of additional load (R-L load) to the PCC. As shown in figure7.24, the ac currents are containing some harmonic currents distortion for feed forward modulation, therefore; the $\alpha\beta$

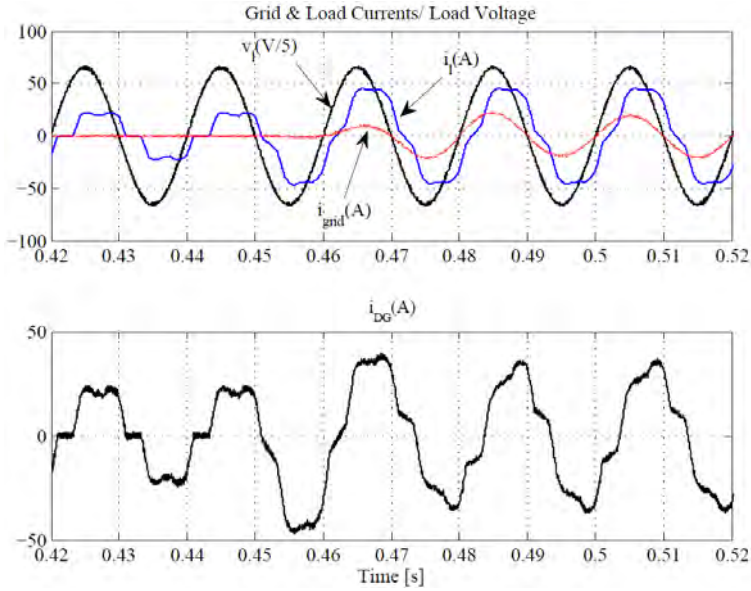


Figure 7.18: Grid current, load voltage and load current before and after connection of additional RL loads to the grid

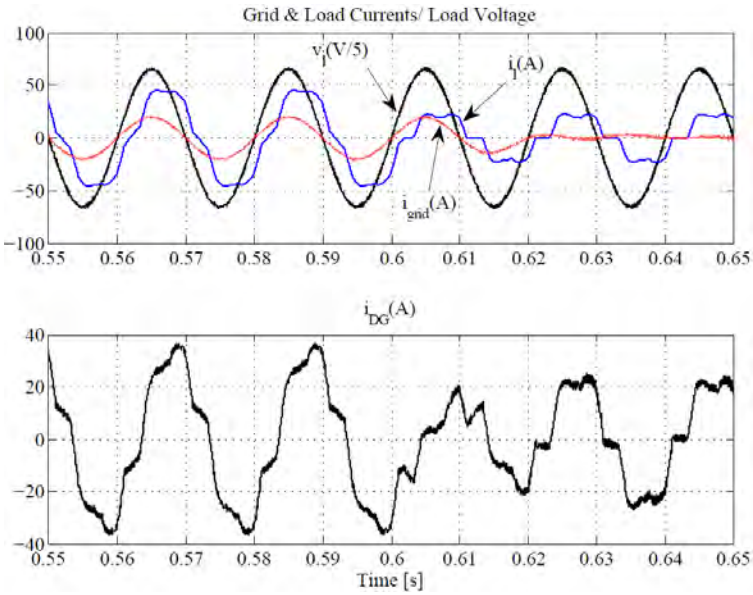


Figure 7.19: Grid current, load voltage and load current before and after disconnection of additional RL loads to the grid

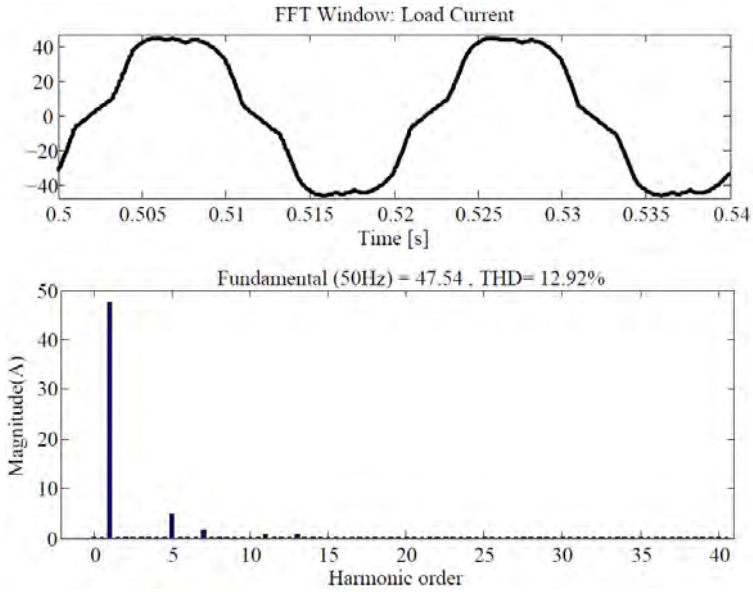


Figure 7.20: Load current spectra after connection of additional RL load to the grid

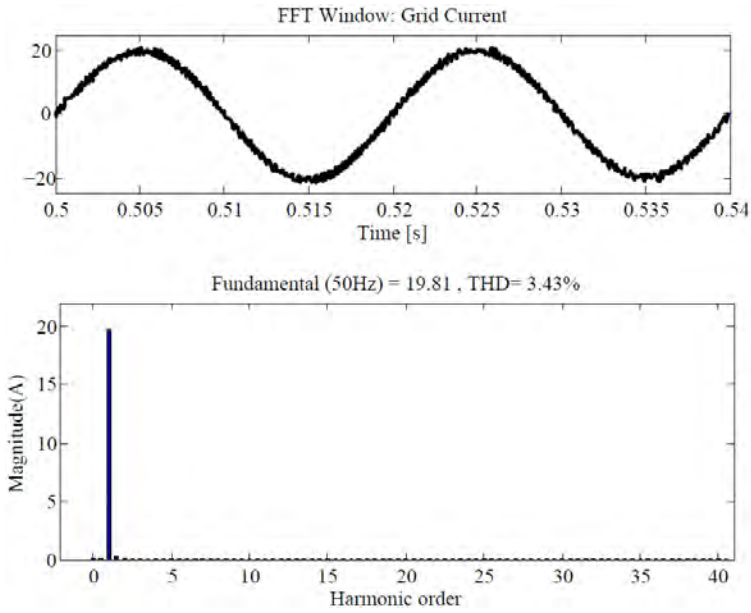


Figure 7.21: Grid current spectra after connection of additional RL load to the grid

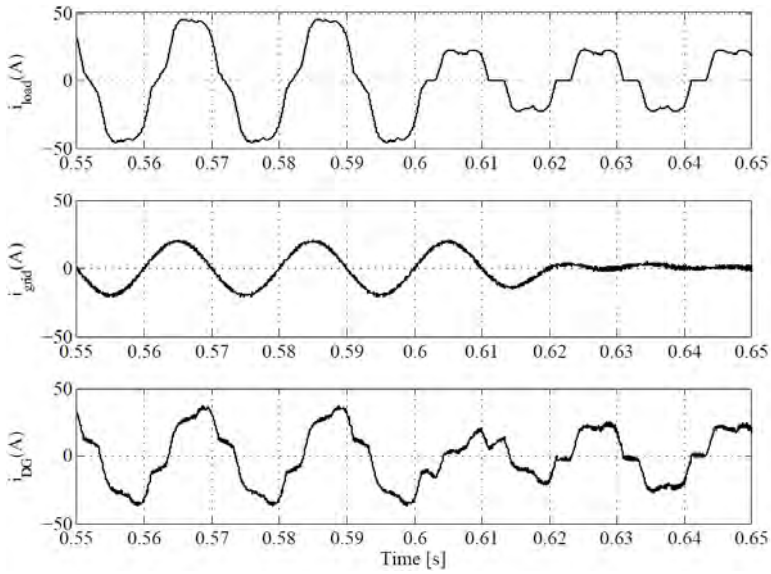


Figure 7.22: Load current, non-linear link current and grid current before and after disconnection of additional RL load

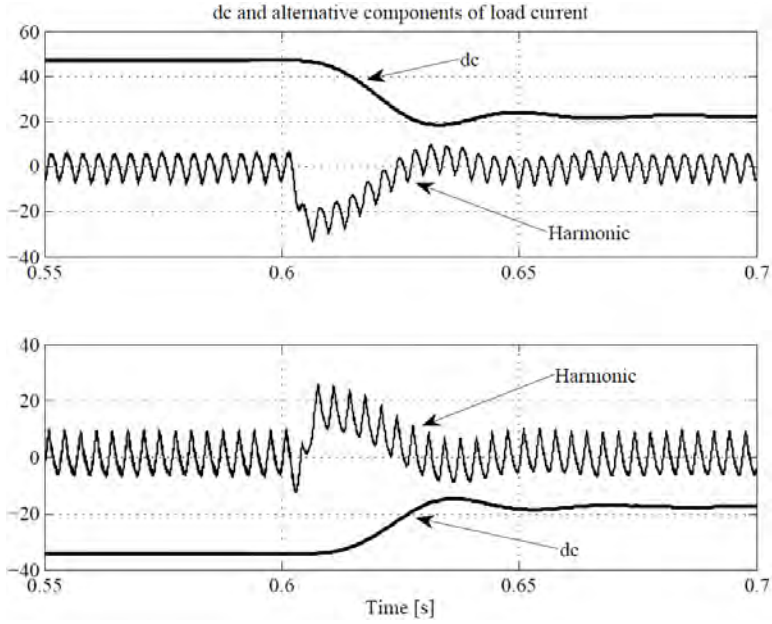


Figure 7.23: d and q-components of load currents before and after disconnection of additional RL load from the grid

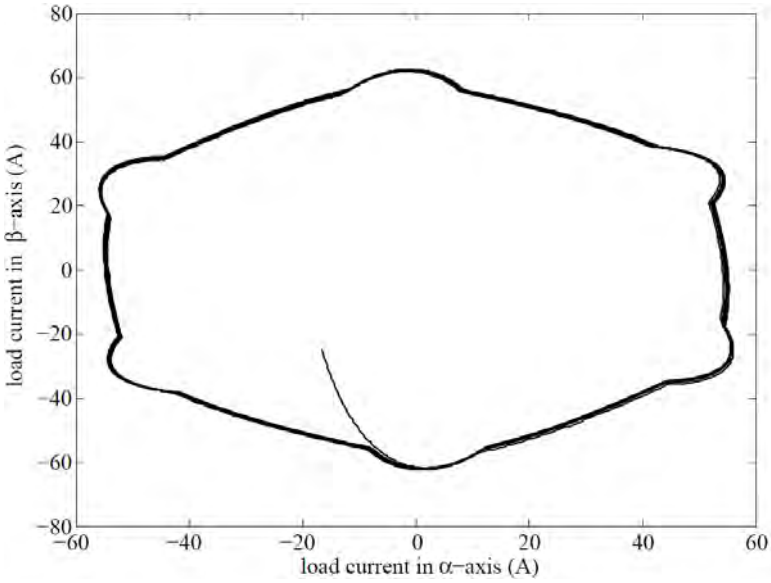


Figure 7.24: Trajectory of load current before and after connection of additional linear load to the grid in $\alpha\beta$ representation

representation of those currents is not circular and is hexagonal.

Figure 7.25 and Figure 7.26 shows the trajectory of the grid and DG currents in $\alpha\beta$ representation, after connection of DG link and during connection of additional load to the grid. Figure 7.25 shows that, after connection of additional load to the PCC, the grid current does not contain significant low-frequency distortion for feed forward modulation, since the $\alpha\beta$ representation of these currents are approximately circular in α *and* β-axis. Figure 7.26 shows that, after connection of additional load to the grid, DG link supplies the harmonic current components of loads and remains of active power and whole the reactive power of the grid-connected loads.

Figure 7.27 shows the load voltage, and load, grid, and DG currents in phase (a), during connection of DG to the grid, and connection of additional non-linear and linear loads to the PCC. It can be seen that, in all conditions, the injected current from main grid to the loads is high power quality current waveform, and DG link compensate the other components by injection of the maximum available power of the DG resources to the grid by considering the maximum capacity of interface system.

Finally, the active and reactive powers which pass through the network during connection of additional linear load to the grid, are shown in figures

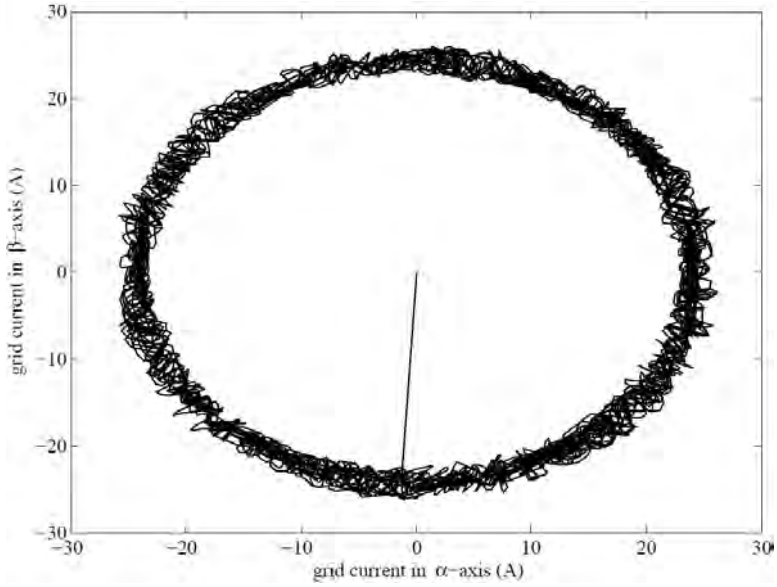


Figure 7.25: Trajectory of grid current before and during connection of additional linear load to the grid in $\alpha\beta$ representation

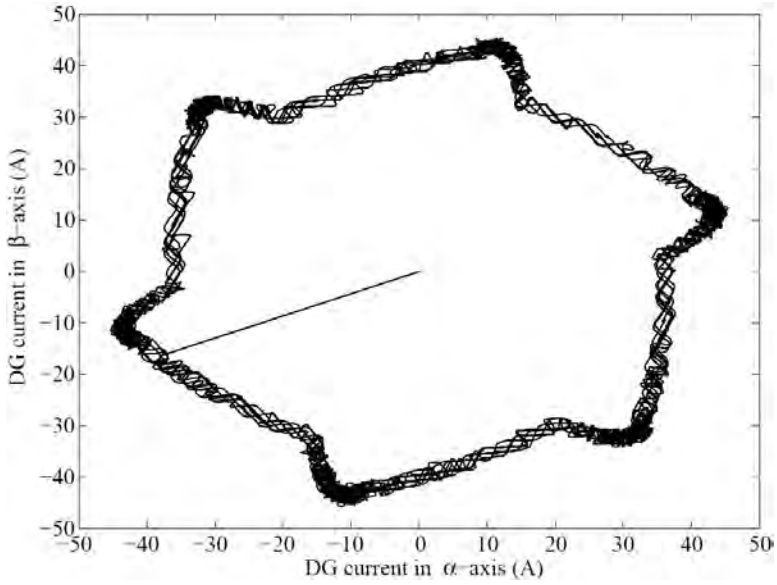


Figure 7.26: Trajectory of DG link current before and during connection of additional linear load to the grid in $\alpha\beta$ representation

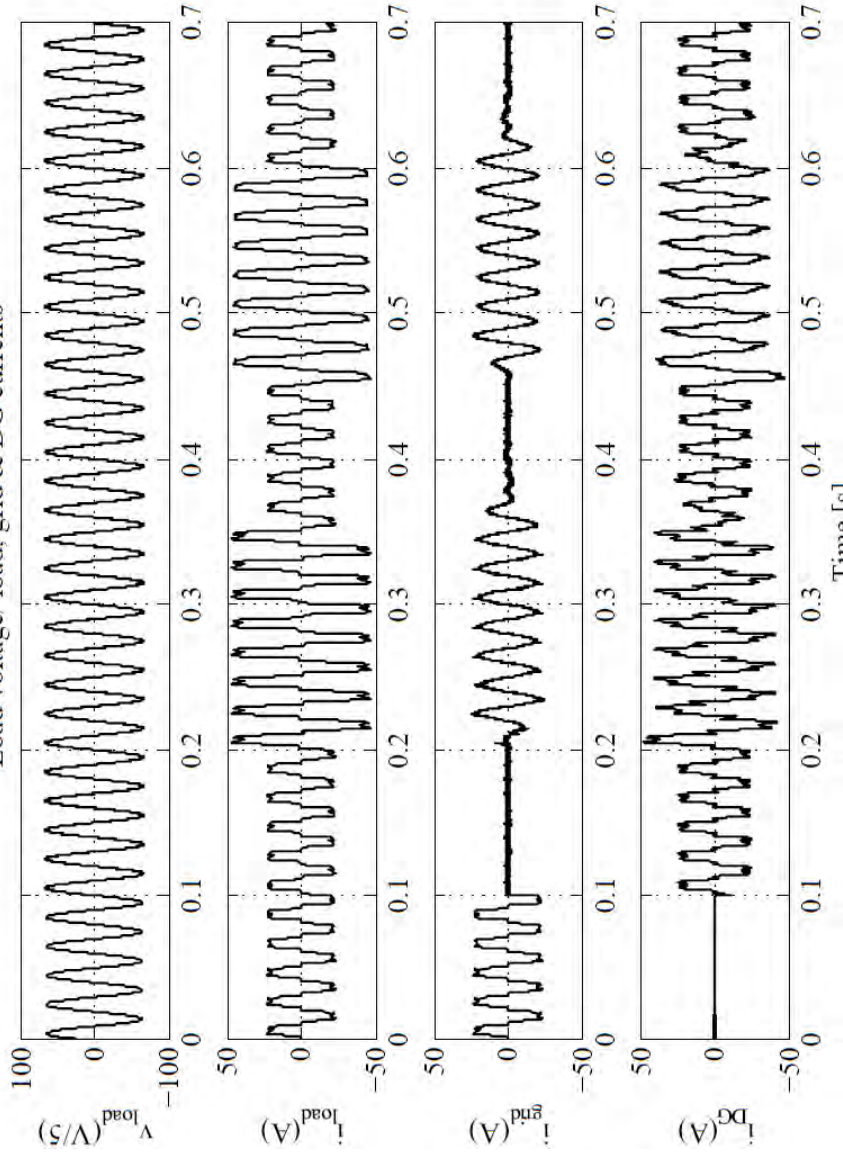


Figure 7.27: Load voltage, load, grid, and DG currents before and after connection of DG to the grid, and before and after connection of additional non-linear and linear loads to the grid

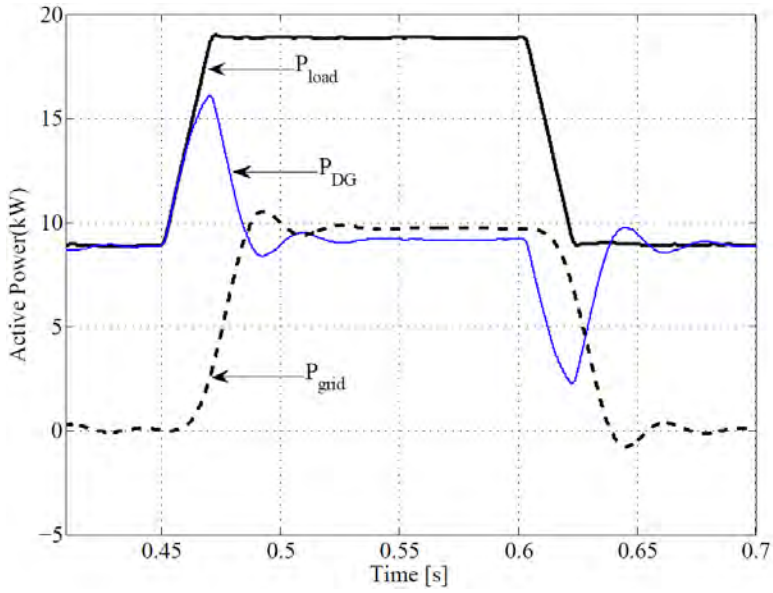


Figure 7.28: Grid, Load and DG link active power, during integration of DG resources to the grid, before and after connection and disconnection of additional non-linear and linear loads to the grid

7.28 and 7.29. Figure 7.28 shows grid, load and DG link active power during connection of DG link and connection and disconnection of additional linear load to the grid. As one can predict, the waveform of active power of DG link contains a step response which is related to MPHPF. Therefore, the delay and swings in this wave are due to the same reasons mentioned before. In addition, during connection of DG to the grid the active power which is delivered from grid is decreased to zero and DG link delivered active power, completely tracks load active power. But, during connection of additional linear load to the grid, some of active power is injected from utility grid, and others are compensated by DG. This is because the DG's reference power is less than load's total power. Due to delay settling time of MPHPF, after connection of additional linear load at t=0.45 sec, some swings appear in active power waveform. The transient time takes around one cycle (0.02 sec).

Figure 7.29 indicates grid, load and DG link reactive power which pass through the network during connection and disconnection of an additional linear load to the grid. As there is no filter in the control loop of q-component of DG link reference current, the waveform of DG reactive power has bet-

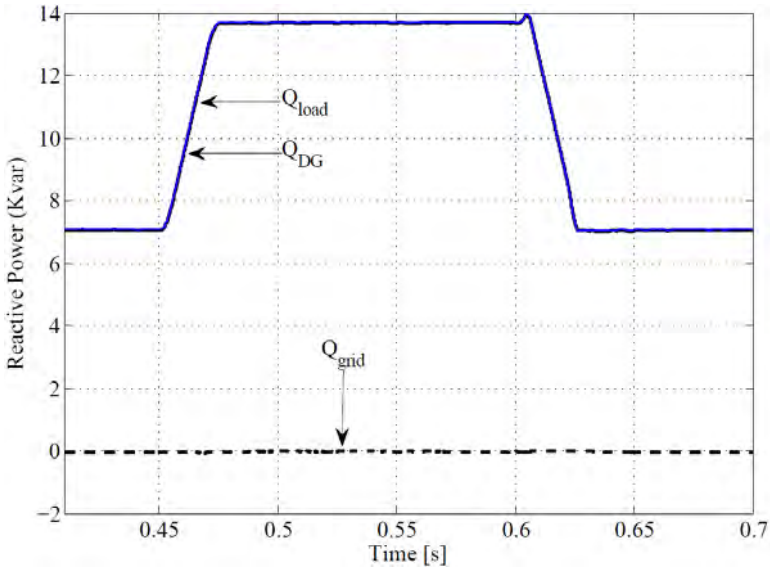


Figure 7.29: Grid, Load and DG link reactive power, during integration of DG resources to the grid, before and after connection and disconnection of additional non-linear and linear loads to the grid

ter response than DG's active power response. This figure also shows the capability of DG system to track and compensate load reactive power, completely. This can prevent load voltage fluctuations in case of sudden change in load reactive power.

7.1.3 The ability of proposed strategy to supply unbalanced load

With the adopted control technique, this part aims to evaluate the capability of the DG link to compensate for non-linear unbalanced load currents. To carry this out, the load consists of a three-phase full-wave thyristor converter supplies a load with resistance of 20 Ω and 10 mH inductors in each phase, and a single-phase thyristor converter supplies a load with resistance of 15 Ω and 10 mH inductors. The single-phase thyristor converter is connected between phases 1 and 2, as shown in figure 7.1.

Prior to the connection of DG to the grid, this unbalanced non-linear load draws unbalance current which is polluted by harmonic components from the ac grid continuously. The proposed DG link is connected to the ac grid at t=0.1 sec. The grid voltage, load, grid, and DG link currents are shown in figure 7.30. As shown in this figure, DG link injects the maximum power of

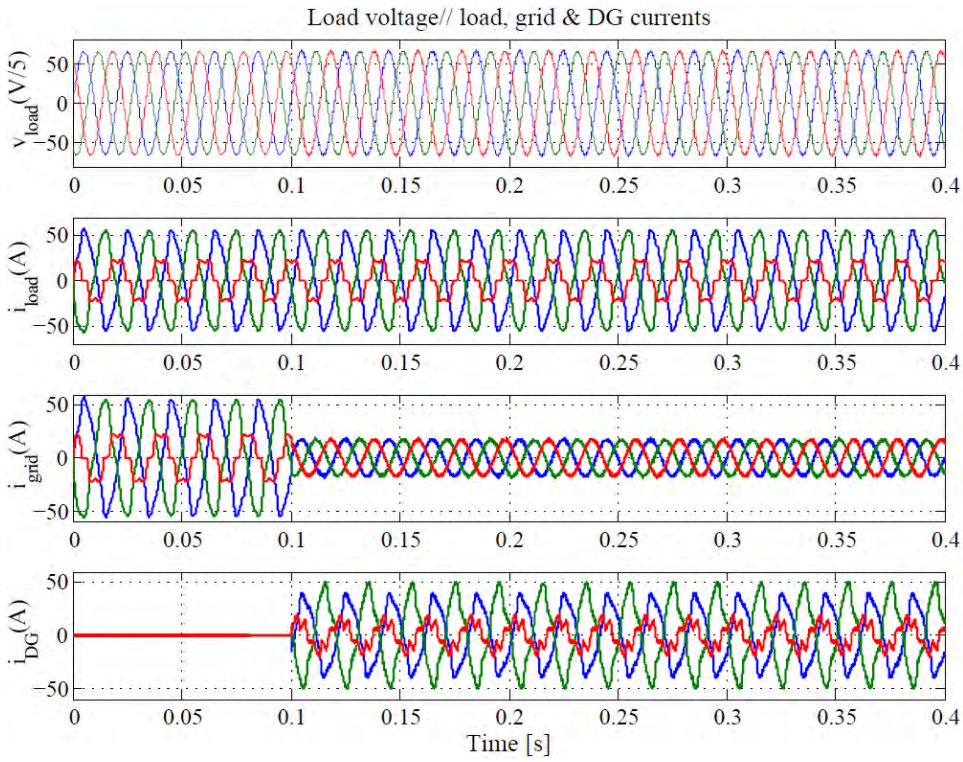


Figure 7.30: Load voltage, load, grid, and DG currents before and after connection of DG link into ac grid for compensation of non-linear unbalanced load

DG resources to the grid, which is consisted of harmonic current components of d and q-axis, reactive and some parts of active power of the unbalanced non-linear load. The other remained active power will be injected by the grid to the load. It can be seen that, the three-phase injected currents from grid to the load are balanced after connection of DG link to the ac grid.

Furthermore, the spectrum analysis results of load and grid currents depicted in table 7.2 indicates that the DG link can largely improve THD of the grid currents during feeding grid-connected unbalanced load. As mentioned in table 7.2, THD of the grid currents i_{g123} are reduced from 9.74%, 11.06%, and 21.76% before compensation to 3.84%, 3.8%, and 3.39% after compensation, respectively. These results confirm the capability of the proposed DG link to balance the grid currents while simultaneously compensating for active, reactive and harmonic unbalanced load current components.

Before Compensation	After Compensation					
Peak Current	$I_{g1}(A)$	$I_{g2}(A)$	$I_{g3}(A)$	$I_{g1}(A)$	$I_{g2}(A)$	$I_{g3}(A)$
Fundamental	48.78	49.7	22.1	14.53	14.44	14.35
THD%	9.74	11.06	21.76	3.84	3.8	3.39

Table 7.2: Fundamental and THD values of grid currents

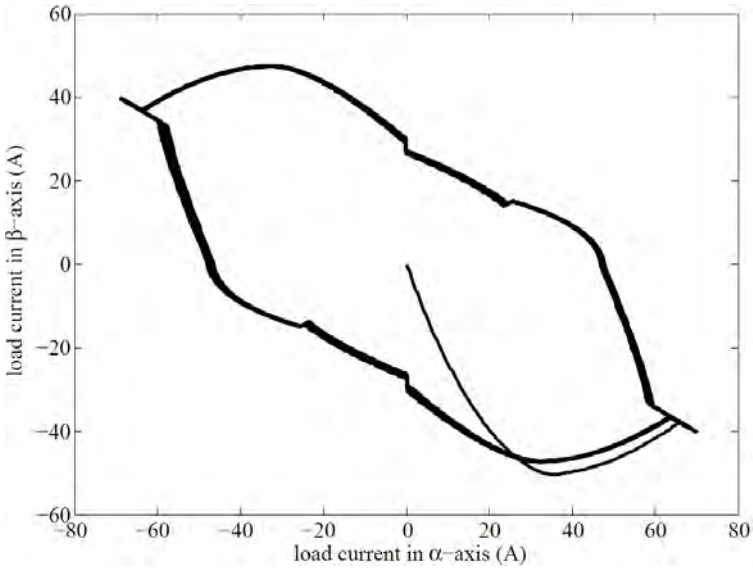


Figure 7.31: Trajectory of the unbalanced load current in $\alpha\beta$ representation

Figures 7.31-7.33 show the trajectory of the unbalanced load, grid and DG currents in $\alpha\beta$ representation after connection of DG link to the grid. Figure 7.31 shows, the ac currents are containing some harmonic currents distortion for feed forward modulation, and unbalanced current component, therefore; the $\alpha\beta$ representation of those currents is not circular and is consisted of asymmetrical shape. As shown in figure 7.32, after connection of DG to the grid at t=0.1 sec, the grid current does not contain significant low-frequency distortion for feed forward modulation, since the $\alpha\beta$ representation of those currents is approximately circular. Figure 7.33 shows, the DG link have these abilities to inject the maximum available active power of the DG source, supplies the harmonic current components of d and q-axis and whole the reactive power of the unbalance load.

Finally, the active and reactive powers which pass through the network are shown in figures 7.34 and figures 7.35. Figure 7.34 shows grid, load and

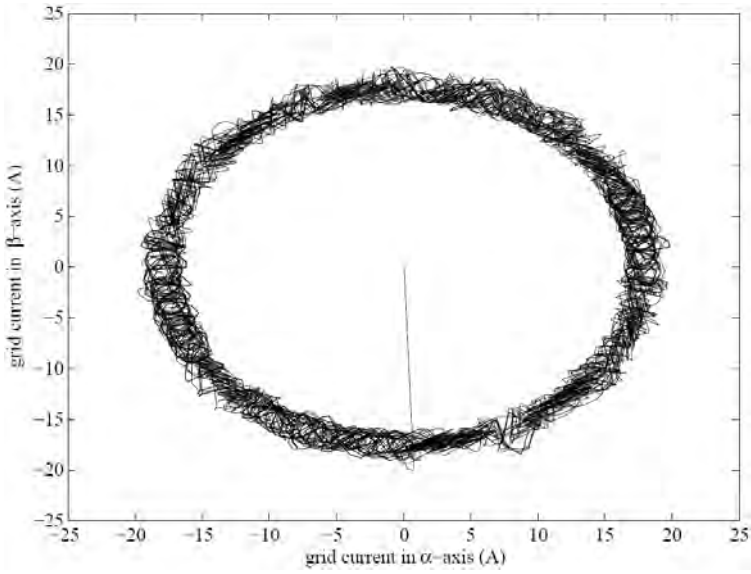


Figure 7.32: Trajectory of the grid current in $\alpha\beta$ representation

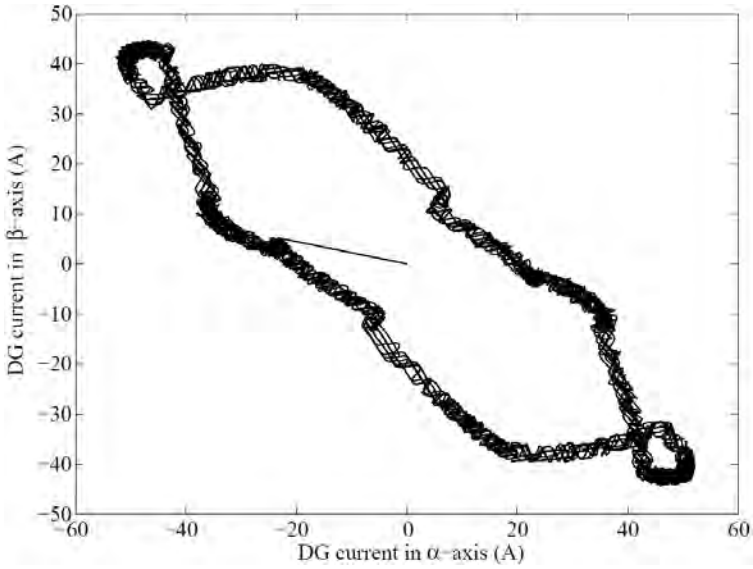


Figure 7.33: Trajectory of the DG current in $\alpha\beta$ representation

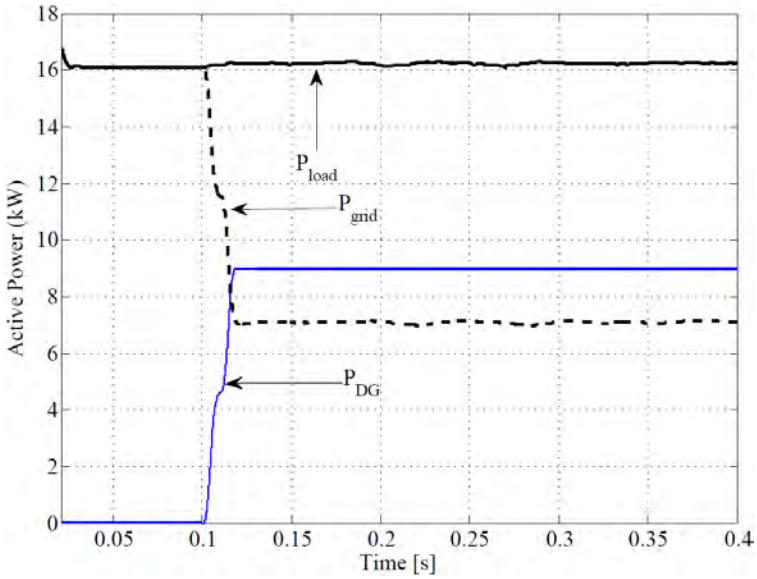


Figure 7.34: Grid, load and DG link active power, before and after integration of DG resources to the grid, and compensation of unbalanced load

DG link active power before and after connection of DG link to the grid. As shown in this figure, after connection of DG to the grid, DG link inject the maximum available active power to the grid, and the main grid supplies the others remained active power. Figure 7.35 indicates grid, load and DG link reactive power before and after connection of DG to the grid. This figure also shows the capability of DG system to track and compensate load reactive power, completely. This can prevent load voltage fluctuations in case of sudden change in load reactive power.

7.2 Conclusions of the Chapter

In this chapter, the simulation results of the proposed model have been presented. In this case, a three-level NPC converter employed as the heart of interfacing system between DG resources and ac grid. Flexibility of the DG model in both steady state and transient operation has been verified. The presented results clarified the ability of proposed control technique in compensation of active, reactive, unbalanced and harmonic load current components. According to the obtained results, in all conditions the load

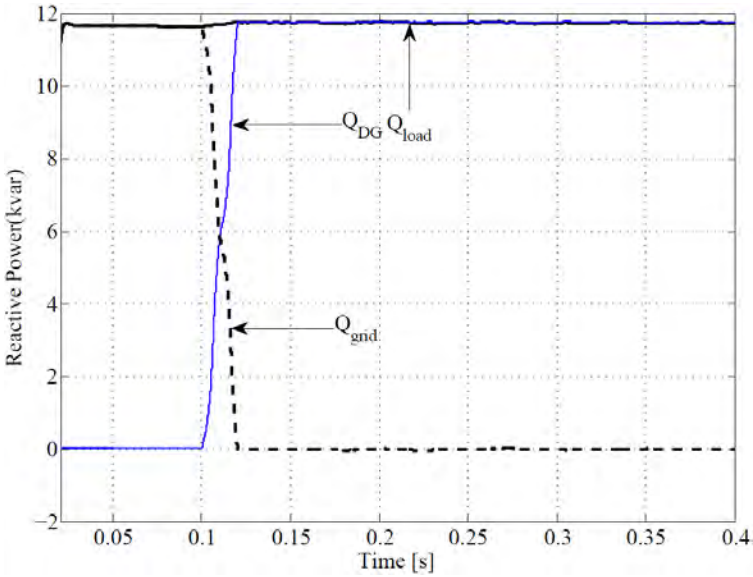


Figure 7.35: Grid, load and DG link reactive power, before and after integration of DG resources to the grid, and compensation of unbalanced load

voltage and grid current are in phase and, by improvement of power factor at PCC, DG systems can act as power factor corrector devices. One other important advantage of the control method is its fast dynamic response in tracking reactive power variations; the control loops of active and reactive power are considered independent. By the use of this control method, DG system is introduced as a new alternative for distributed static compensator in ac grid. The simulation results indicate that proposed DG model can provide required harmonic load currents in both balanced and unbalanced loads. Therefore, by reducing THD of grid current it can act as an active power filter. The proposed control method can be used for different types of DG resources and all types of multilevel converter topologies as power quality improvement devices in a medium and high power grid.

Chapter 8

Hardware Implementation and Experimental Test Results

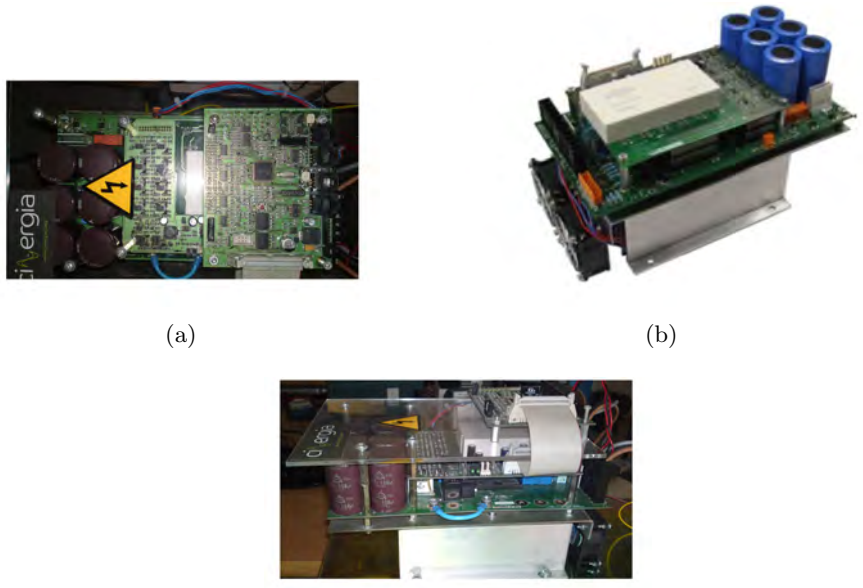
8.1 Prototype Description

The experimental tests results presented in this thesis have been achieved using the AC/DC three-phase rectifier and a DC/AC voltage source converter. In this system, the dc energy source has been emulated with three phase diode rectifier fed by a three-phase alternative voltage source. Figure 8.1 shows this prototype, which was designed in the Centre d'Innovació Tecnològica en Convertidors Estàtics i Accionaments (CITCEA-UPC) laboratory, in Universitat Politècnica de Catalunya(UPC), manufactured and commercialized by Cinergia, in Barcelona, Spain. Structure of the proposed model is consisted of power, driver and control.

The proposed Voltage Source Converter is a hardware module which integrates all the power elements, signal adaptation, transducers and protections of a three-phase converter. Its design enables its utilization on several applications such as: frequency converter and servo drive, rectifier and active filter, uninterruptible power supply, network emulator, voltage sags and disruptions generator, and renewable generation and micro-networks emulator.

Main features of the proposed VSC are:

1. Nominal power is 10kVA
2. Integrated over-voltage, over-current (AC and CC) and temperature hardware protections
3. Three-phase diode rectifier
4. IGBTs in three-phase converter configuration + brake chopper
5. Opto-isolated drivers with short-circuit and sub-voltage protection



(a) (b)

(c)

Figure 8.1: Experimental setup platform (a). Control, (b). Drive and power, (c). General structure

6. Pre-charge on both AC and DC sides
7. DC bus up to the 800V peak with discharge resistance
8. Hall Effect current transducers: 2xAC + 1xDC
9. Isolated voltage transducers: 2xAC + 1xDC

8.2 Digital Control Hardware

The complexities of control system in different converter topologies, together with the increase in power level in electrical networks, performance and availability of high-tech digital control hardware, result in almost exclusive application of digital control hardware for the majority of modern converter topologies and converter systems in electrical networks. Furthermore, the flexibility of new and high-tech microprocessors allows them to be used for the control of any type of converter topologies, and hardware implementation of any type of modulation techniques in electrical networks. Currently, the

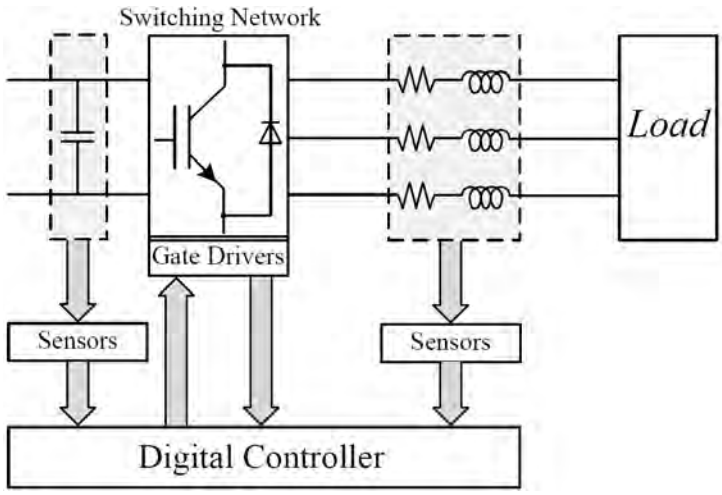


Figure 8.2: Power electronics system

ever-increasing processing power of microprocessors allows for much more user-friendly development tools that can accept input from higher programming languages such as C and (increasingly) Matlab software.

8.2.1 Structure of Digital Control Hardware

Regardless of the topological differences, the power flow direction, or its application in almost every power electronics system, has few main components, such as the switching network with filter components on both input and output, the sensors subsystem, the power terminals and a digital control subsystem as shown in figure 8.2. In similar case, the structure of modern digital controllers can be subdivided into several major functional blocks from figure 8.3. The central element is the processor usually accompanied by some kind of programmable logic devices to implement the PWM (if this capability is not already provided on the processor). Also, programmable logic devices provide the simplest way to implement some specific protection functions that require very fast response speed as well as any "glue" logic required to interface the processor with other components on the control board.

This traditional structure of the controller is being challenged as part of the development of the power electronic building block concept and the introduction of the digital communication subsystem.

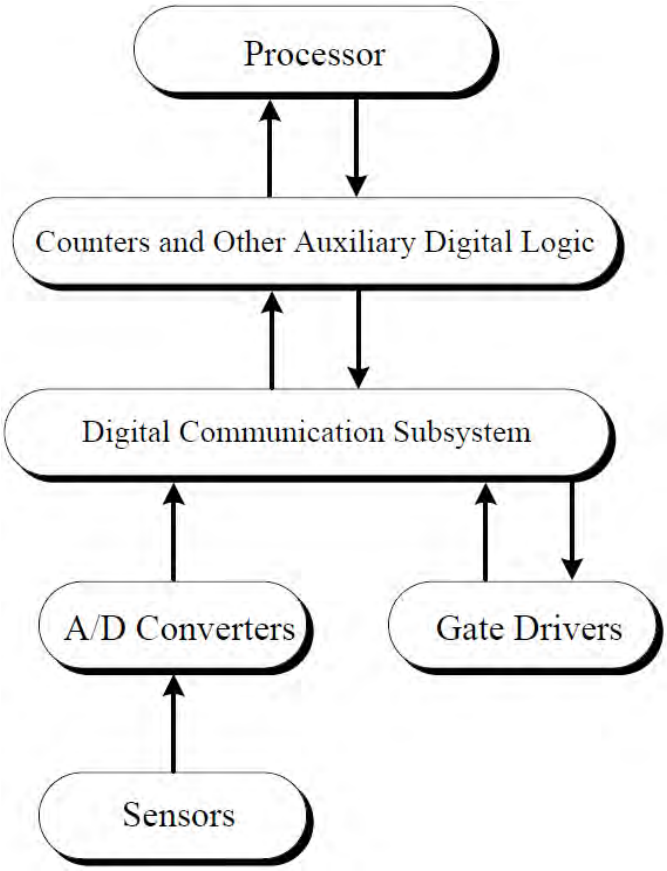


Figure 8.3: Structure of the digital controller for power electronics systems

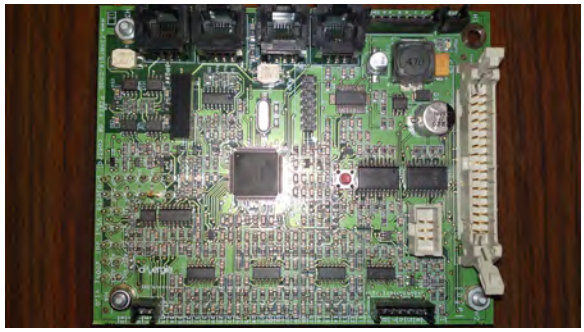


Figure 8.4: DSP based Power Electronics control board

8.2.2 DSP Control Board for Power Electronics Applications

Sussie Board is the DSP based Power Electronics control board shows in figure 8.4. It is Plug & Play with Cinergia's VSC 10 kVA flexible Power Electronics converter, and allows full power programming and debug of Power Electronics Algorithms and system state machines.

Block diagram of the proposed DSP-based controller is shown in figure 8.5. It can be divided into three functional subsystems, implemented on separate printed circuit boards:

1. DSP subsystem
2. Digital interface subsystem
3. Analog interface subsystem with A/D and D/A converter

8.2.3 Main Features of Sussie Board

Cinergia's Sussie Board is based on the Texas Instruments TMS320F2808 DSP. With Power Electronics applications in mind, it has been equipped with special onboard peripherals.

Main features of Sussie Board are:

1. Power Electronics Special Input/Outputs, including:
   a) PWM outputs
   b) Brake resistor signal
   c) Drivers reset signal
   d) IGBT error input

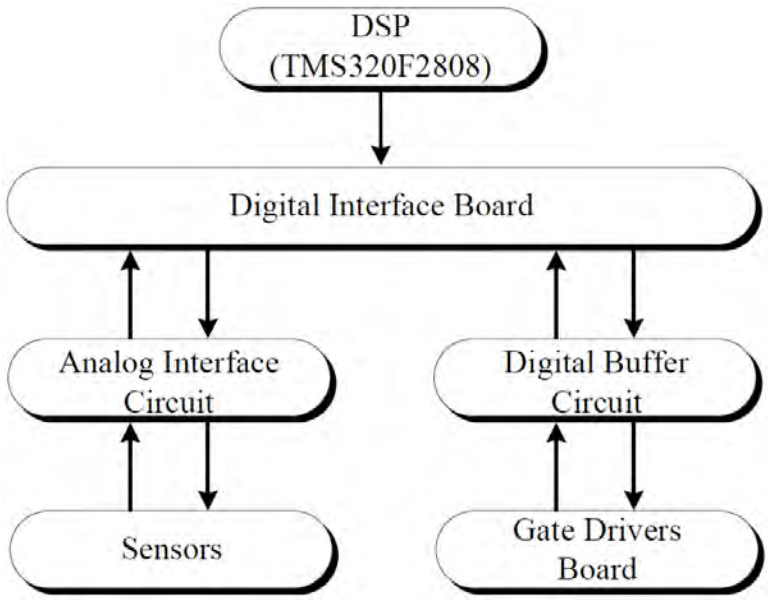


Figure 8.5: Architecture of the Sussie digital controller board

2. 7 ± 10V and 3 0-10V ADC inputs
3. Two isolated CAN channels
4. JTAG communications, supporting Real Time Debug
5. General purpose 5V input/outputs
6. Four channel on-board DAC, with one output
7. Encoder input, 2Ch+Z incremental encoder, with differential input signal
8. On-board temperature sensor
9. Outline dimensions: 100x125 mm [3.94x4.92 in]

The DSP Control Board is specially designed to fit Power Electronic converter needs.

Main industrial applications of this control board are:

- Active Front End

- Active Rectifier
- PFC- Renewable Energies
- Smart Grids
- Factory Motor Control
- Electric Vehicle
- Laboratory Applications
- Test Equipment

8.3 Control Algorithm

The first tasks of any system controller are regulation, and pulse width modulation. Figure 8.6 shows the schematic diagram of the control structure. The process in propose system model begins with the sensing of three-phase grid voltages and three-phase line currents. The measured currents and voltages are transformed from three-phase stationary reference frame (abc) to three-phase synchronous reference frame (dq0) and compared with reference values to generate error signals. The error signals are processed in a compensator and the result is transformed $0\alpha\beta$ coordinates. Then the modulator takes over and selects the switching states and duty cycles that implement the commanded reference vector from the compensators according to objectives of compensation. Up to this point the complete algorithm is implemented in software.

Finally the PWM generation is implemented in hardware requires many timers to keep track of the duty cycles and some combinatorial logic to change between the switching states.

8.4 Experimental Test Results

In this section, high performance of the proposed control technique is tested on a developed laboratory prototype of a DG system. The general schematic diagram of the experimental set-up is shown in figure 8.7, where the positive polarities for grid current (i_s), load current (i_l), and DG current (i_c) are emphasized, in agreement with figure 7.1. A general view of the experimental test bench is presented in figure8.8 and the system parameters are given in

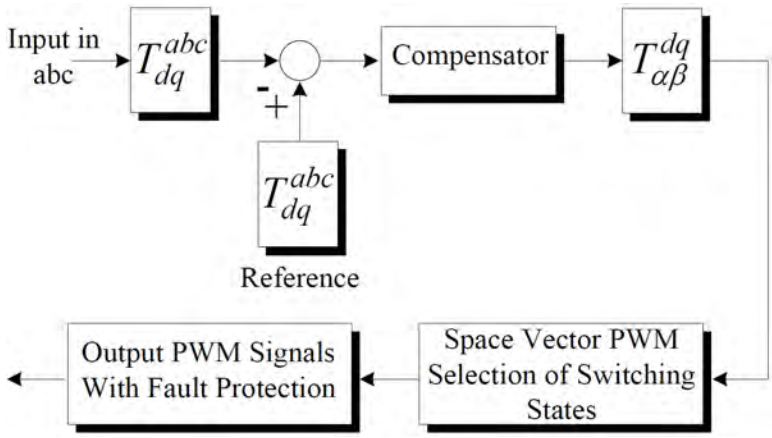


Figure 8.6: Control overview

Parameter	Value
Grid voltage (v_s)	80 V
Interfacing inductance (L_c)	4.6 mH
dc-link capacitance	1020 μF
dc-link voltage set-point (v_{dc})	610 V
Fundamental frequency	50 Hz
Switching/Sampling frequency	10 kHz
Linear load resistance	40 Ω
Linear load inductance	100 mH
Non-linear load resistance	30 Ω

Table 8.1: Experimental setup parameters

table 8.1. A 10-kVA three-phase full-bridge converter prototype using a switching frequency of 10 kHz has been used for the experimental tests.

The hardware platform used to implement the converter control algorithm is digitally controlled by TMS320F2808 fixed-point DSP for implementation of the power and current control algorithm. The quantities measured from the proposed system are the converter current (i_c), the PCC voltage (v_{pcc}), and the grid-connected load current (i_l), as shown in figure8.7. As the focus of this dissertation is on the grid-connected converter, the dc energy source has been emulated with a three phase diode rectifier fed by a three-phase alternative voltage source.

The test model contains a power converter with power rating of 2 kVA.

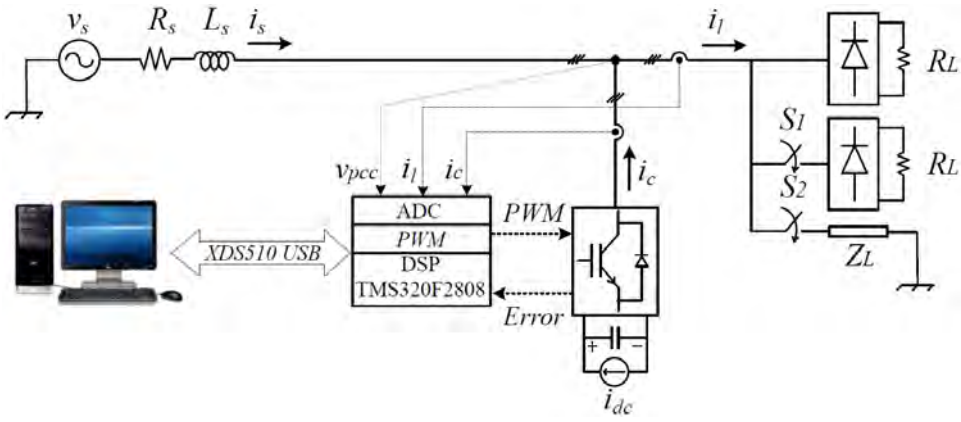


Figure 8.7: Experimental set-up of the proposed DG system

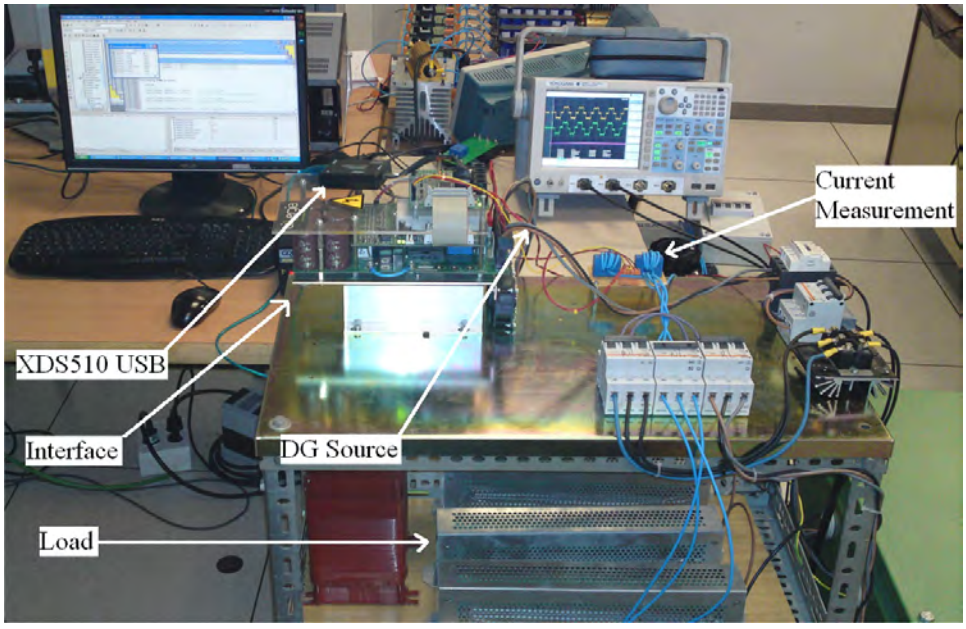


Figure 8.8: General view of the experimental test bench

The available DG source active power is 320 W, which is also the active power reference included in the real time tests. The main purposes of the experimental tests are to study different performance aspects of the control technique in different conditions. At first, capabilities of the DG resources and flexibility of the control strategy for control of VSC in providing active, reactive, and harmonic current components of different loads are shown, and the capabilities of proposed control method on reactive power tracking with constant output active power are considered. In addition, the active power which is delivered from the DG resources to the ac grid is considered to be constant. This assumption makes it possible to evaluate the capability of the proposed control strategy to track the fast change in the active and reactive power, independent of each other. For this purpose, when one of them is changed, another one must be constant. To consider a real ac grid, the load is connected and disconnected to power grid randomly and grid current waveform will be compared with each other under various loads and conditions.

8.4.1 Connection of DG link to the power grid to supply harmonic currents components and non-linear load increment

This test has been performed with the converter having only non-linear local load which is connected to the utility grid. Prior to the connection of DG link to the ac grid, a three-phase full-wave diode rectifier supplies a resistive load with resistance of 30 Ω in each phase. This non-linear load draws harmonic current from the grid continuously, and makes harmonic pollutants in utility grid. Figure 8.9 shows, three-phase load and grid currents before connection of DG link to the utility grid.

This process is continued until the DG link connects to the main grid. Figure 8.10 shows, after connection of DG link to the grid, the grid current becomes almost zero and all the active and reactive current component including fundamental and harmonics frequency are provided by DG link ($i_{grid} = i_{load} - i_{DG}$). The injected current from VSC is completely equal to measured current from the grid, but because of isolation transformer between the VSC and the grid, some injected current from VSC to the grid consume for compensation of magnetizing current of isolation transformer. Therefore, the grid injects the remained current which is equal to transformer magnetizing current, and because of this current, injected current from grid cannot be completely zero. It can be seen that, the problems due to synchronization between DG and power grid do not exist and DG link can be connected to the power grid without any high current overshoot.

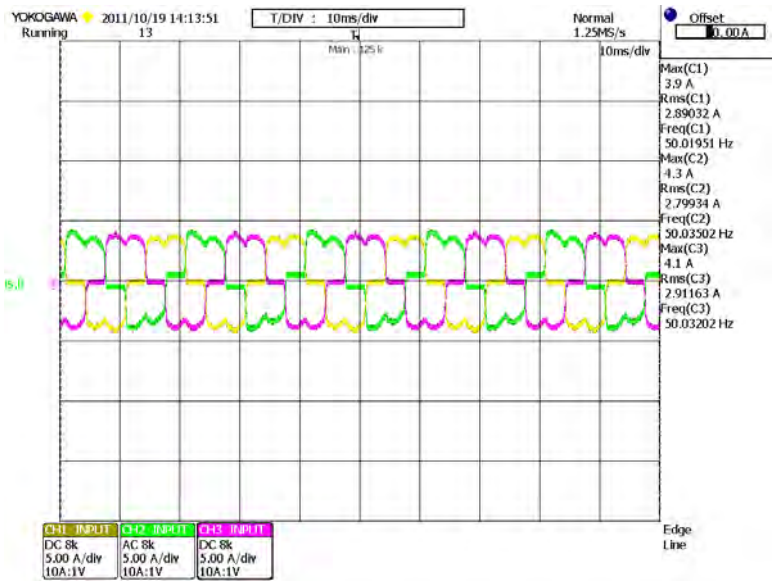


Figure 8.9: Load and grid current before connection of DG to the grid

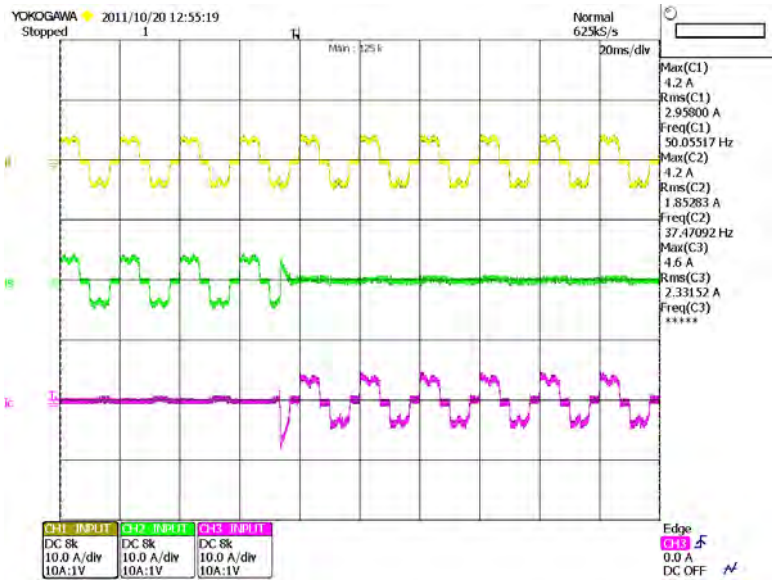


Figure 8.10: Load, grid, and DG currents before and after connection of DG link to the power grid

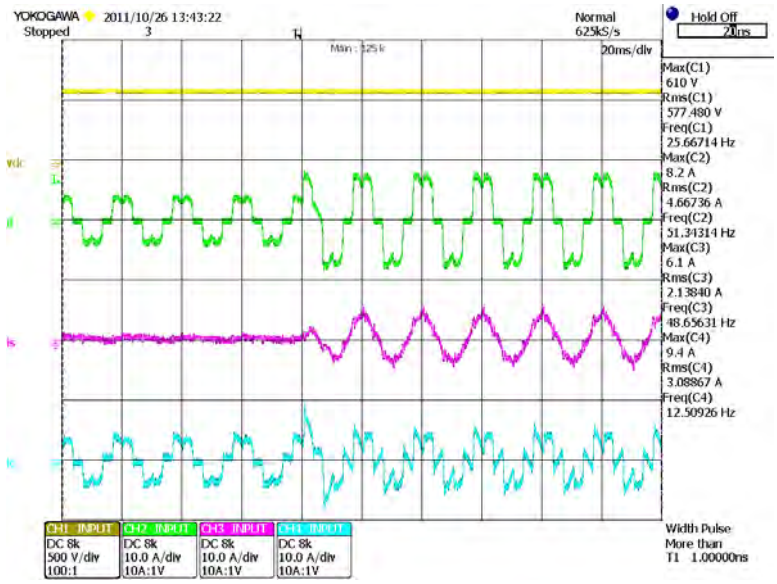


Figure 8.11: dc-bus voltage, load, grid, and DG currents before and after connection of additional load to the grid

The load's current is fed from non-linear DG link continuously and this process is continued until another full-wave diode rectifier similar to the prior load is connected to the grid. Figure 8.11 shows the transient waveforms of the dc-bus voltage, load, grid, and DG currents before and after sudden variation in the current-source type of non-linear load. It can be seen that, after connection of additional load to the grid, production in control circuit of DG system is delayed for less than half a cycle. This is due to settling time of MPHPF filter in control loop of DG system. In addition, load harmonic currents are provided by DG and grid current is sinusoidal, but there are sharp edges on grid current waveforms which are related to high order harmonic frequencies and created during switching of thyristor converters. In addition, figure 8.11 shows the dc-bus voltage of the VSC is well regulated, and no overvoltage appears in the transient state. Therefore, proposed integration strategy is insensitive to grid overload during connection of DG resources to the power grid.

Figure 8.12 shows, after connection of additional load to the power grid, the load voltage and grid current are in phase, therefore; the grid does not need to provide reactive and harmonic currents for the grid-connected loads. In this case, the local loads still draw active power from the main grid. This

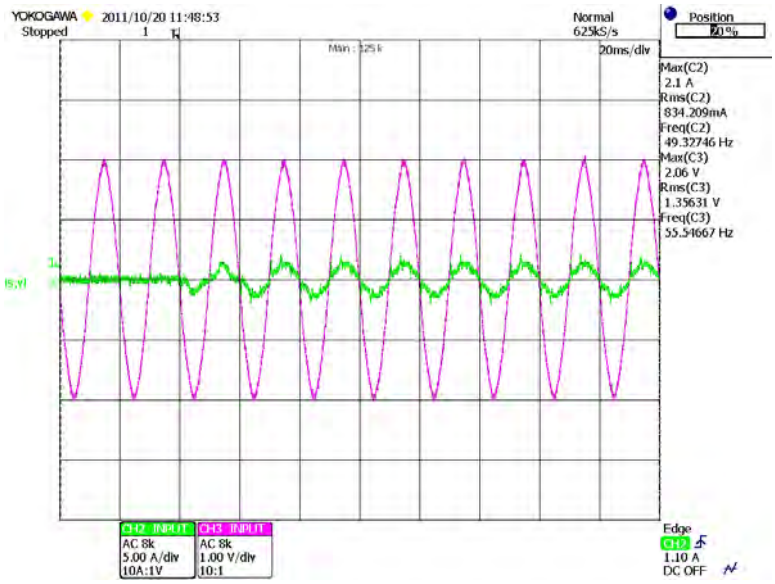


Figure 8.12: Phase-to-Phase voltage and grid current for phases (ab)

happens because the maximum reference active power of interfaced converter is less than the active power requested by the local loads.

Figure 8.13 shows, with the same delay as before, additional load is removed and, after the pass of the transient times the grid current becomes zero, therefore; all the active and reactive current component of non-linear load including fundamental and harmonics frequency are provided by DG link .

The ability of control loop to track the references current of d and q-axis, for the duration of connection of DG link and for the period of connection of additional load to the grid, is shown in figure 8.14 and figure 8.15. As shown in figure 8.14, before connection of additional load to the main grid, DG link fallows both active and reactive reference currents completely. But, according to figure 8.15, after connection of additional load to the main grid, DG fallows half of the reference active current in fundamental frequency, whole the reference reactive current and whole the active and reactive currents in fundamental frequencies. The remain active current in fundamental frequency is injected by grid.

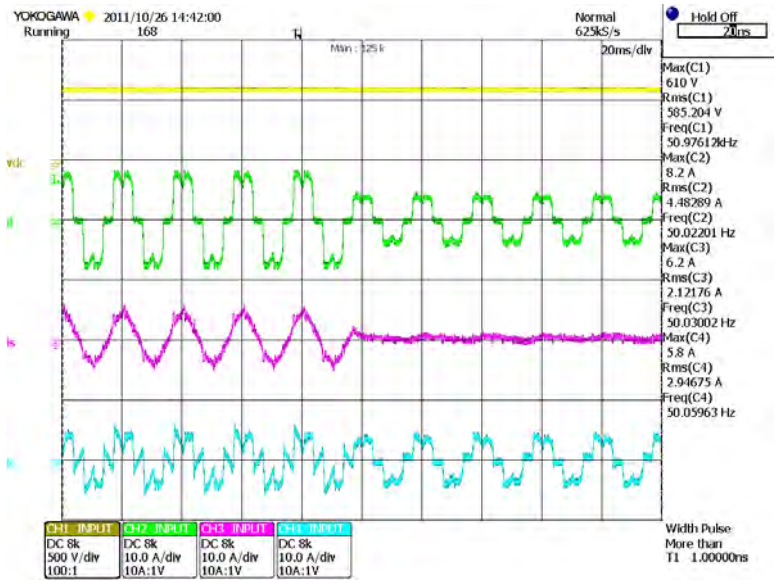


Figure 8.13: dc-bus voltage, load, grid, and DG currents before and after remove of additional load from the grid

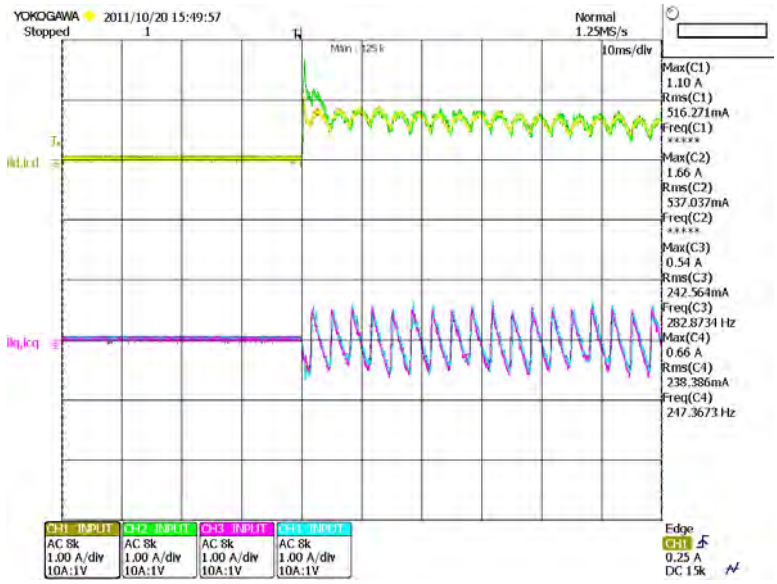


Figure 8.14: Reference currents track the load current after integration of DG to the grid

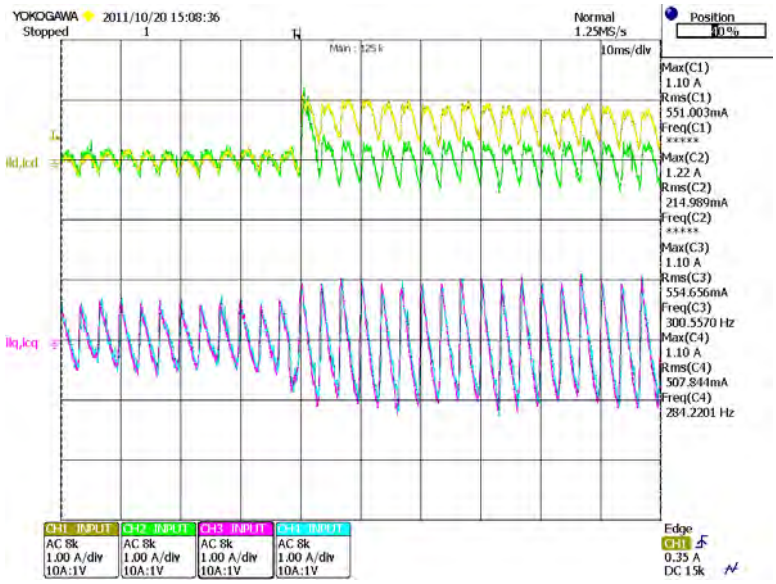


Figure 8.15: Reference currents track the load current after connection of additional load to the grid

8.4.2 Linear load increment

In this section, to evaluate the DG link to track both harmonic and sinusoidal currents, an additional linear (RL) load is connected to the PCC, during connection of a non-linear load to the power grid. This non-linear load draws harmonic current from the grid continuously, and makes harmonic pollutants in utility grid.

The related experimental results are shown in figures 8.16-8.18. Additional linear load is a 40 Ω resistance and a 100 mH inductance load in each phase. Maximum delivered power from DG system is considered constant (P_{ref}=320 W). Considering that all required reactive power of additional load is provided by DG system, additional required load active power must be provided by the main grid. Figure 8.16 shows dc-bus voltage, load current, grid current and non-linear link current during linear load increment. An additional load is connected to the power grid and due to delay settling time of MPHPF filter, production in DG link circuit is started less than half a cycle after load connection. According to figure 8.16, load harmonic current is provided by DG link and grid current is sinusoidal. Figure 8.17 shows, with the same delay as before, additional load is removed and, after the pass of the transient times the grid current becomes zero. Therefore,

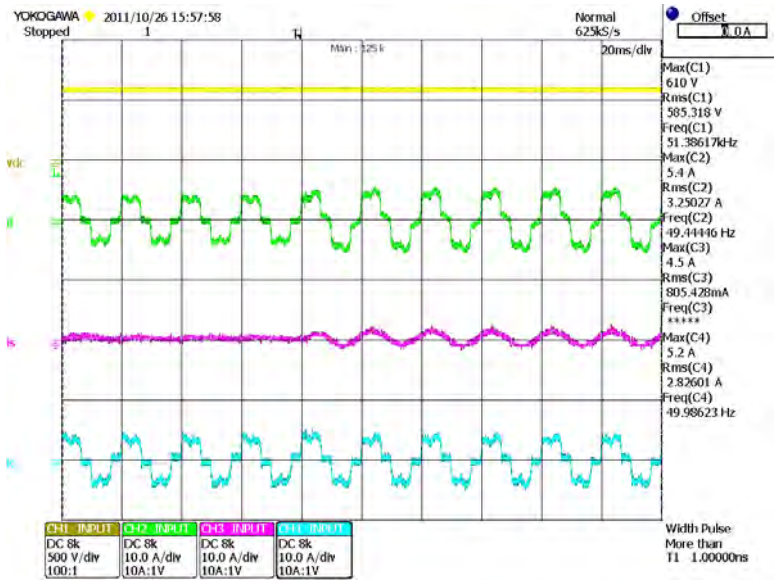


Figure 8.16: dc-bus voltage, load, grid, and DG currents before and after linear load increment

all the active and reactive current components of non-linear load including fundamental and harmonics frequency are provided by DG link. Similar to connection of non-linear loads to the power grid, the dc-bus voltage of the VSC is well regulated, and no over-voltage appears in the transient state.

The ability of control loop of DG link to track the references current of d and q-axis, for the duration of connection of additional linear load to the grid, is shown in figure 8.18. It can be seen that, before connection of additional linear load to the grid, DG link fallows both active and reactive reference currents completely ($i_{load} = i_{DG}$). But, after connection of additional linear load to the grid, DG cannot fallows whole of the reference active current in fundamental frequency, but whole the reference reactive current in fundamental and harmonic frequencies, plus some part of active power in fundamental frequency which is equal to reference active power of converter, and whole the harmonic currents in d-axis are fallowed. The remained active power in fundamental frequency is injected by grid.

Figure 8.19 shows the steady-state operations of the DG link for injection of maximum available power from DG source to the power grid during the grid-connected loads are disconnected. As shown in this figure, the grid current is out of phase with respect to the converter current by 180 electrical

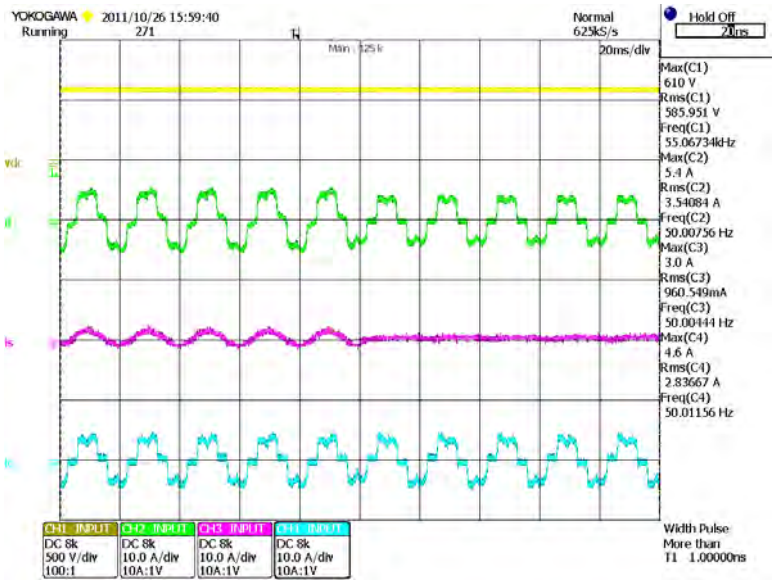


Figure 8.17: dc-bus voltage, load, grid, and DG currents before and after linear load increment

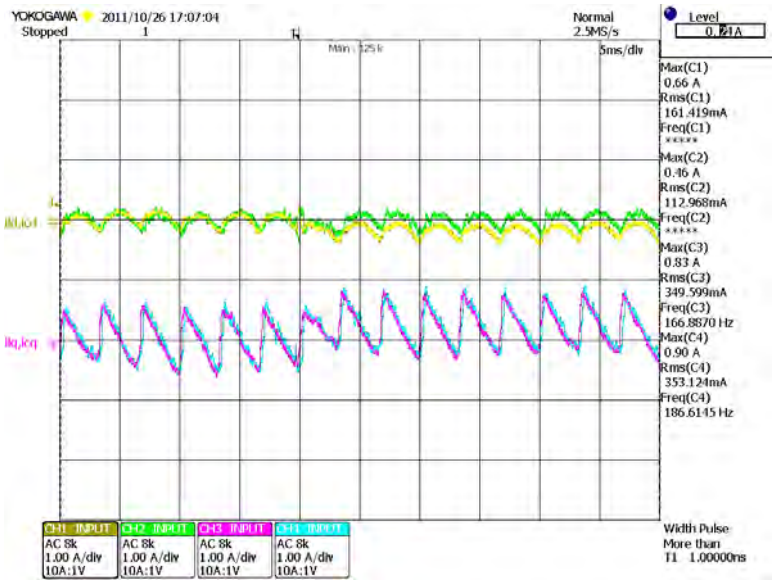


Figure 8.18: Reference currents track the load current before and after additional linear load increment

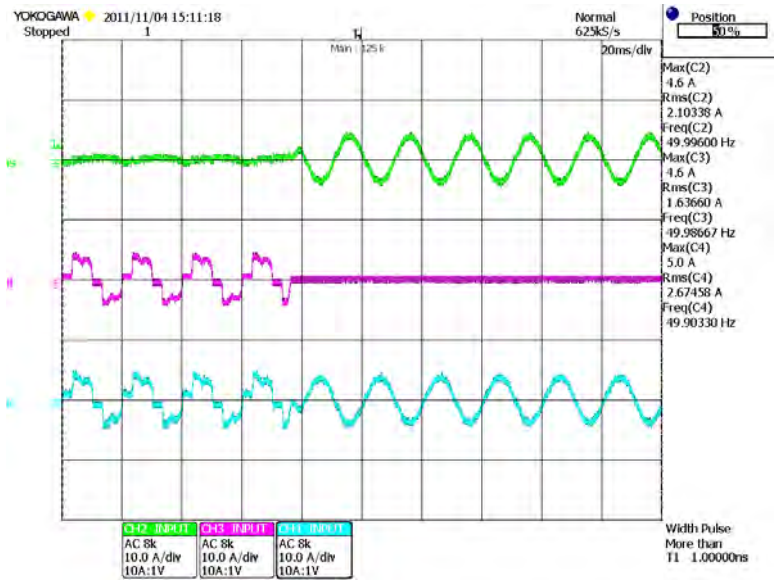


Figure 8.19: Steady-state operation of the DG link for injection of maximum available active power from DG source to the power grid, continuously

degrees, which means maximum active power injected from DG to the grid continuously.

8.5 Conclusions of the Chapter

Experimental test results of a robust control technique for DG system that broadly addresses a number of key integration issues have been presented in this chapter. Flexibility of the proposed technique in both steady state and transient operation has been verified. The presented experimental test results clarified the proposed interface system provides a powerful infrastructure for DG units to meet the stricter demands for different grid-connected loads. Real time analysis and test results have revealed the effectiveness of the proposed control scheme during connection of DG resources to the power grid.

Chapter 9

Conclusions

9.1 Summary and Conclusions

A multi-purpose control algorithm for the multilevel converter-based DG interface system, for integration of DG resources to the power grid, have been proposed and presented in this thesis. The proposed control algorithms are designed to realize a robust DG interface that guarantees a stable grid and high power quality injection from utility grid, under the challenging uncertain nature of electrical networks.

In Chapter 3, the state of the art of multilevel power converter technologies have been introduced. The basic principles of different multilevel converters topologies discussed in this chapter, and for each multilevel topology, different structures presented. In addition, different advantages and disadvantages of different topologies have been described and main applications of them in electrical networks and industrial projects briefly presented.

In Chapter 4, three-phase schematic diagram of the proposed system model has been introduced and presented. At first step, a brief explanation about the synchronous reference and the stationary reference frames control have been presented, and voltage and current components vectors shown in $\alpha\beta$ and dq reference frames. In the next step, reference currents of DG control loop have been defined for compensation, and injection to the power grid according to objectives of DG integration. In addition, the dynamic model of the proposed system has been elaborated in the stationary reference frame and then transformed into the synchronous orthogonal reference frame. The transformed variables are used in control of the multilevel voltage source converter as the heart of the interfacing system between DG resources and utility grid. Finally, the large-signal and small-signal mathematical model of the proposed system have been analyzed, and an averaged small-signal model of the three-level converter described for the design of control loop circuit.

In Chapter 5, SVPWM switching algorithm for three-phase multilevel

converter topologies has been presented, and a three-level diode-clamped converter has been considered as a case study. Different stages of this algorithm have been presented step by step for proposed converter, in different sections. The proposed algorithm is general and applicable to different topologies of converters with any number of levels.

In Chapter 6, a current control algorithms for converter-based DG interface, and a voltage regulator for dc bus voltage regulation of converter have been presented. In addition, a technique for balancing the voltage of dc bus cascaded capacitors presented in this chapter. The proposed voltage and current control scheme targets the problem of fast and large-signal-based current disturbances, which is common in typical power networks.

In Chapter 7, the schematic diagram and principle of the proposed control technique in a power grid has been presented. In order to demonstrate the high performance of the proposed control technique of the DG interface, the complete system model was simulated and evaluated using the "Power System Blockset" simulator operating under the Matlab/Simulink environment. Flexibility of the proposed system in both steady state and transient operation has been verified during the connection of different type of loads to the power grid.

In Chapter 8, the main features of the proposed system introduced for a real system and experimental setup of the proposed DG model. The flexibility of the proposed technique in both steady state and transient operation for compensation of different grid components has been verified.

9.2 Contributions

The main contributions of this thesis can be highlighted as follows:

1. The development of a multi-purpose control algorithm for the multilevel converter-based DG interface for integration of DG resources to the power grid. The proposed control algorithms yield a stable and high-power quality current control performance under the challenging uncertain nature of electrical networks and practical system constraints. In this proposed system, both cases of the converter-output current control and grid-side current control are considered. Hence, a wide applicability scope is yielded. The salient features of the proposed current controllers are:

    a) Injection the maximum active power of DG resources to the power grid continuously.

b) Supply load harmonic current components, therefore; high power quality current injection from grid under connection of non-linear loads to the grid.

c) Compensates load reactive power and increase the power factor of power grid.

d) Guarantees balanced overall grid currents of unbalanced load.

e) High robustness against un-certainties in the interfacing parameters.

f) No additional hardware is needed for delay compensation.

g) Contribute to compensate load voltage drops.

2. The development of a current control algorithm and dc voltage regulator which have been applied to the interfaced converter output current control, and dc bus voltage regulation, during connection to the power grid. The controller shows adequate tracking performance and fast dynamic response in tracking reference components according to the grid characteristics and conditions during connection to the grid.

3. The development of control technique for the multilevel converter topologies with any types and levels. By application of the proposed control technique in multilevel converter topologies, connection of DG resources to the medium and high voltage ac grid will be possible.

4. The development a high performance synchronization technique between DG resources and power grid. By application of this method, the problems due to synchronization between DG and network do not exist and DG link can be connected to the power grid without any current overshoot.

5. The development of a robust DG interface that utilizes the developed control algorithms in a way to preserve the generation stability and power quality under the challenging uncertain and dynamic nature of typical electrical networks. The overall DG interface facilitates a stable and reliable operation along with a safe plug-and-play integration of DG units in power grid; hence increasing the system penetration of DG. The direct result of this development is high financial saving for utilities by capturing the salient features of deploying DG into existing utility grids. Further, these developments are significant to the industry as they provide the blue print for reliable control algorithms

in future DG units, which are expected to operate under challenging system conditions.

9.3 Directions for Future Work

In continuation of this work, the following subjects are suggested for future studies:

1. The adaptation and application of the proposed control technique to different custom power devices, such as active filters, distribution static synchronous compensators, and unified power conditioners.

2. Application of the proposed control schemes for multilevel VSC to High Voltage Direct Current (HVDC) converters.

3. The utilization of the proposed control technique in different multilevel converter topologies, and different types of DG resources specially based on renewable energy resources.

4. The extension of the proposed technique for islanded and micro grid operations.

Bibliography

[1] W. Ouyang, H. Cheng, X. Zhang, and F. Li, "Evaluation of distributed generation connecting to distribution network based on long-run incremental cost," *IET Generation, Transmission & Distribution*, vol. 5, no. 5, pp. 561–568, 2011. 1

[2] H. H. Zeineldin, T. H. M. El-Fouly, E. F. El-Saadany, and M. M. A. Salama, "Impact of wind farm integration on electricity market prices," *IET Renewable Power Generation*, vol. 3, no. 1, pp. 84–95, 2009. 1

[3] M. F. Akorede, H. Hizam, and E. Pouresmaeil, "Distributed energy resources and benefits to the environment," *Renewable and Sustainable Energy Reviews*, vol. 14, no. 2, pp. 724 – 734, 2010. 1

[4] M. N. M. A. Keyhani and M. Dai, *Integration of Green and Renewable Energy in Electric Power Systems.* A John Wiley & Sons, Inc., Hoboken, New Jersey, 2010. 1

[5] F. A. Farret and M. Simoes, *Integration of Alternative Sources of Energy.* IEEE Press, A John Wiley & Sons, Inc., Hoboken, New Jersey, 2006. 1, 2, 13, 15, 16, 46

[6] G. Pepermans, J. Driesen, D. Haeseldonckx, R. Belmans, and W. D'haeseleer, "Distributed generation: definition, benefits and issues," *Energy Policy*, vol. 33, no. 6, pp. 787 – 798, 2005. 1

[7] E. J. Coster, J. M. A. Myrzik, B. Kruimer, and W. L. Kling, "Integration issues of distributed generation in distribution grids," *Proc. IEEE*, vol. 99, no. 1, pp. 28–39, 2011. 1

[8] H. Willis and W. G. Scott, "Distributed power generation: Planning and evaluation," New York, 2000. 1

[9] C. Chen, S. Duan, T. Cai, B. Liu, and G. Hu, "Smart energy management system for optimal microgrid economic operation," *IET Renewable Power Generation*, vol. 5, no. 3, pp. 258–267, 2011. 1

[10] S. Naderi, E. Pouresmaeil, and W. D. Gao, "The frequency-independent control method for distributed generation systems," *Applied Energy*, no. 0, pp. –, 2011. 2, 58

[11] Z. Chen, F. Blaabjerg, and J. K. Pedersen, "A multi-functional power electronic converter in distributed generation power systems," in *Proc. IEEE 36th Power Electronics Specialists Conf. PESC '05*, 2005, pp. 1738–1744. 2

[12] K. Kirubakaran, S. Jain, and R. K. Nema, "Dsp-controlled power electronic interface for fuel-cell-based distributed generation," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3853–3864, 2011. 2

[13] H. Akagi, "Large static converters for industry and utility applications," *Proc. IEEE*, vol. 89, no. 6, pp. 976–983, 2001. 2

[14] Y. A.-R. I. Mohamed, "New control algorithms for the distributed generation interface in grid-connected and micro-grid systems," Ph.D. dissertation, University of Waterloo, 2008. 3, 6, 15, 16, 17, 18

[15] Y. A.-R. I. Mohamed and E. F. El-Saadany, "A robust natural-frame-based interfacing scheme for grid-connected distributed generation inverters," *IEEE Trans. Energy Conversion*, vol. 26, no. 3, pp. 728–736, 2011. 6

[16] F. Wang, J. L. Duarte, M. A. M. Hendrix, and P. F. Ribeiro, "Modeling and analysis of grid harmonic distortion impact of aggregated dg inverters," *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 786–797, 2011. 6

[17] R. Piwko, R. DeMello, R. Gramlich, W. Lasher, D. Osborn, C. Dombek, and K. Porter, "What comes first?" *IEEE Power Energy Mag.*, vol. 5, no. 6, pp. 68–77, 2007. 14

[18] T. Ackermann, Ed., *Wind Power in Power Systems.* John Willy & sons Press, 2005. 14

[19] Y.-K. Wu, C.-Y. Lee, and G.-H. Shu, "Taiwan's first large-scale offshore wind farm connection—a real project case study with a comparison of wind turbine," *IEEE Trans. Ind. Applicat.*, vol. 47, no. 3, pp. 1461–1469, 2011. 15

[20] E. Denny and M. O'Malley, "Wind generation, power system operation, and emissions reduction," *IEEE Trans. Power Syst.*, vol. 21, no. 1, pp. 341–347, 2006. 15

[21] D. Gautam, V. Vittal, and T. Harbour, "Impact of increased penetration of dfig-based wind turbine generators on transient and small signal stability of power systems," *IEEE Trans. Power Syst.*, vol. 24, no. 3, pp. 1426–1434, 2009. 15

[22] M. Castro, D. Pudjianto, P. Djapic, and G. Strbac, "Reliability-driven transmission investment in systems with wind generation," *IET Generation, Transmission & Distribution*, vol. 5, no. 8, pp. 850–859, 2011. 15

[23] S. Zhang, K. J. Tseng, and S. S. Choi, "Statistical voltage quality assessment method for grids with wind power generation," *IET Renewable Power Generation*, vol. 4, no. 1, pp. 43–54, 2010. 15

[24] T. H. M. El-Fouly, H. H. Zeineldin, E. F. El-Saadany, and M. M. A. Salama, "Impact of wind generation control strategies, penetration level and installation location on electricity market prices," *IET Renewable Power Generation*, vol. 2, no. 3, pp. 162–169, 2008. 15

[25] M. H. Bollen and F. Hassan, *Integration of Distributed Generation in Power System.* Wiley-IEEE Press Series on Power Engineering, 2011. 15

[26] N. J. Guilar, T. J. Kleeburg, A. Chen, D. R. Yankelevich, and R. Amirtharajah, "Integrated solar energy harvesting and storage," *IEEE Trans. VLSI Syst.*, vol. 17, no. 5, pp. 627–637, 2009. 15

[27] C. S. Tao, J. Jiang, and M. Tao, "Natural resource limitations to terawatt-scale solar cells," *Solar Energy Materials and Solar Cells*, vol. 95, no. 12, pp. 3176 – 3180, 2011. 15

[28] L. Hassaine, E. Olias, J. Quintero, and M. Haddadi, "Digital power factor control and reactive power regulation for grid-connected photovoltaic inverter," *Renewable Energy*, vol. 34, no. 1, pp. 315 – 321, 2009. 16

[29] G. Tsengenes and G. Adamidis, "A multi-function grid connected pv system with three level npc inverter and voltage oriented control," *Solar Energy*, vol. 85, no. 11, pp. 2595 – 2610, 2011. 16

[30] H. E. Fadil and F. Giri, "Climatic sensorless maximum power point tracking in pv generation systems," *Control Engineering Practice*, vol. 19, no. 5, pp. 513 – 521, 2011. 16

[31] M. L. Remus Teodorescu and P. Rodrigues, *Grid Converters for Photovoltaic and Wind Power Systems.* John Wiley & sons, Ltd, 2011. 16

[32] J. Peirs, D. Reynaerts, and F. Verplaetsen, "A microturbine for electric power generation," *Sensors and Actuators A: Physical*, vol. 113, no. 1, pp. 86 – 93, 2004. 16

[33] J. Kaikko and J. Backman, "Technical and economic performance analysis for a microturbine in combined heat and power generation," *Energy*, vol. 32, no. 4, pp. 378 – 387, 2007. 17

[34] D. Stolten, *Hydrogen and Fuel Cells.* John Wiley & sons, Ltd, 2010. 17

[35] K. A. F. L. Carrette and U. Stimming, *Fuel Cells Fundamentals and Applications.* John Wiley & sons, Ltd, 2001. 17

[36] B. F. T. M. E. Karden, S. Ploumen and K. Snyder, "Energy storage devices for future hybrid electric vehicles," *Journal of Power Sources*, vol. 168, no. 1, pp. 2 – 11, 2007. 18

[37] B. Mao, B. Zhang, J. Wang, Y. Chen, X. Zheng, Y. Gao, B. Wu, and Y. Liu, "Dynamic modelling for distribution networks containing dispersed generations and energy storage devices," in *Proc. Int Power System Technology (POWERCON) Conf*, 2010, pp. 1–6. 18

[38] M.-C. Alvarez-Herault, D. Picault, R. Caire, B. Raison, N. HadjSaid, and W. Bienia, "A novel hybrid network architecture to increase dg insertion in electrical distribution systems," *IEEE Trans. Power Syst.*, vol. 26, no. 2, pp. 905–914, 2011. 18

[39] E. Twining and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an lcl input filter," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 888–895, 2003. 21, 22

[40] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Multiple harmonics control for three-phase grid converter systems with the use of pi-res current controller in a rotating frame," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 836–841, 2006. 21, 22

[41] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source pwm converters: a survey," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 691–703, 1998. 21

[42] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of pwm inverters with zero steady-state error," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 814–822, 2003. 21

[43] S. Fukuda and R. Imamura, "Application of a sinusoidal internal model to current control of three-phase utility-interface converters," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 420–426, 2005. 22

[44] C. T. Rim, N. S. Choi, G. C. Cho, and G. H. Cho, "A complete dc and ac analysis of three-phase controlled-current pwm rectifier using circuit d-q transformation," *IEEE Trans. Power Electron.*, vol. 9, no. 4, pp. 390–396, 1994. 22

[45] T. M. Rowan and R. J. Kerkman, "A new synchronous current regulator and an analysis of current-regulated pwm inverters," *IEEE Trans. Ind. Applicat.*, no. 4, pp. 678–690, 1986. 22

[46] J. Mossoba and P. W. Lehn, "A controller architecture for high bandwidth active power filters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 317–325, 2003. 23

[47] H. Abu-Rub, J. Guzinski, Z. Krzeminski, and H. A. Toliyat, "Predictive current control of voltage-source inverters," *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 585–593, 2004. 23

[48] O. Kukrer, "Discrete-time current control of voltage-fed three-phase pwm inverters," *IEEE Trans. Power Electron.*, vol. 11, no. 2, pp. 260–269, 1996. 23, 24

[49] D. G. Holmes and D. A. Martin, "Implementation of a direct digital predictive current controller for single and three phase voltage source inverters," in *Proc. Conf Industry Applications Conf. Thirty-First IAS Annual Meeting, IAS '96. Record of the 1996 IEEE*, vol. 2, 1996, pp. 906–913. 23, 24

[50] H.-T. Moon, H.-S. Kim, and M.-J. Youn, "A discrete-time predictive current control for pmsm," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 464–472, 2003. 23, 24

[51] G. H. Bode, P. C. Loh, M. J. Newman, and D. G. Holmes, "An improved robust predictive current regulation algorithm," *IEEE Trans. Ind. Applicat.*, vol. 41, no. 6, pp. 1720–1733, 2005. 23, 24

[52] L. Malesani, P. Mattavelli, and S. Buso, "Robust dead-beat current control for pwm rectifiers and active filters," *IEEE Trans. Ind. Applicat.*, vol. 35, no. 3, pp. 613–620, 1999. 23, 24

[53] L. Springob and J. Holtz, "High-bandwidth current control for torque-ripple compensation in pm synchronous machines," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 713–721, 1998. 23, 24

[54] Y.-Y. Tzou and S.-Y. Lin, "Fuzzy-tuning current-vector control of a three-phase pwm inverter for high-performance ac drives," *IEEE Trans. Ind. Electron.*, vol. 45, no. 5, pp. 782–791, 1998. 23, 24

[55] K.-H. Kim, I.-C. Baik, G.-W. Moon, and M.-J. Youn, "A current control for a permanent magnet synchronous motor with a simple disturbance estimation scheme," *IEEE Trans. Contr. Syst. Technol.*, vol. 7, no. 5, pp. 630–633, 1999. 23, 24

[56] K.-H. Kim and M.-J. Youn, "A simple and robust digital current control technique of a pm synchronous motor using time delay control approach," *IEEE Trans. Power Electron.*, vol. 16, no. 1, pp. 72–82, 2001. 23, 24

[57] D.-C. Lee, S.-K. Sul, and M.-H. Park, "High performance current regulator for a field-oriented controlled induction motor drive," *IEEE Trans. Ind. Applicat.*, vol. 30, no. 5, pp. 1247–1257, 1994. 23

[58] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Stability of photovoltaic and wind turbine grid-connected inverters for a large set of grid impedance values," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 263–272, 2006. 25

[59] M. Malinowski, M. P. Kazmierkowski, S. Hansen, F. Blaabjerg, and G. D. Marques, "Virtual-flux-based direct power control of three-phase pwm rectifiers," *IEEE Trans. Ind. Applicat.*, vol. 37, no. 4, pp. 1019–1027, 2001. 26

[60] T. Noguchi, H. Tomiki, S. Kondo, and I. Takahashi, "Direct power control of pwm converter without power-source voltage sensors," *IEEE Trans. Ind. Applicat.*, vol. 34, no. 3, pp. 473–479, 1998. 26

[61] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," vol. 2, no. 2, pp. 28–39, 2008. 29

[62] P. C. Loh, S. W. Lim, F. Gao, and F. Blaabjerg, "Three-level z-source inverters using a single lc impedance network," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 706–711, 2007. 29

[63] L. Demas, T. A. Meynard, H. Foch, and G. Gateau, "Comparative study of multilevel topologies: Npc, multicell inverter and smc with igbt," in *Proc. IEEE 2002 28th Annual Conf IECON 02 [Industrial Electronics Society of the]*, vol. 1, 2002, pp. 828–833. 29

[64] V. T. Somasekhar and K. Gopakumar, "Three-level inverter configuration cascading two two-level inverters," *IEE Proceedings -Electric Power Applications*, vol. 150, no. 3, pp. 245–254, 2003. 29

[65] F. Wang, "Multilevel pwm vsis," *IEEE Ind. Appl. Mag.*, vol. 10, no. 4, pp. 51–58, 2004. 29

[66] M. Marchesoni and M. Mazzucchelli, "Multilevel converters for high power ac drives: a review," in *Proc. , ISIE'93 - Budapest. Symp. IEEE Int Industrial Electronics*, 1993, pp. 38–43. 29

[67] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, 2002. 29, 37

[68] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Applicat.*, vol. 32, no. 3, pp. 509–517, 1996. 29, 33, 36, 37, 38

[69] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," vol. 2, no. 2, pp. 28–39, 2008. 29

[70] M. H. Rahsid, Ed., *Power Electronics Handbook*. Academic Press, 2001. 29, 30

[71] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, 2010. 29

[72] W. Bin, Ed., *High-power converters and ac drives.* New Jersey: John Wiley & Sons, Inc, 2006. 29, 30

[73] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, 2007. 29

[74] P. W. Hammond, "A new approach to enhance power quality for medium voltage ac drives," *IEEE Trans. Ind. Applicat.*, vol. 33, no. 1, pp. 202–208, 1997. 29

[75] R. H. Baker and L. H. Bannister, "Electric power converter," U.S. 3 867 643, Feb. 1975. 30, 36

[76] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Trans. Ind. Applicat.*, no. 5, pp. 518–523, 1981. 30, 31

[77] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Trans. Ind. Applicat.*, vol. 41, no. 3, pp. 855–865, 2005. 30

[78] Multilevel Cascade Voltage-source Inverter with Separate DC source, U.S. Patent Patent 5 642 275, 1997. 30

[79] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "A multilevel converter-based universal power conditioner," *IEEE Trans. Ind. Applicat.*, vol. 36, no. 2, pp. 596–603, 2000. 33

[80] L. Tolbert, F. Z. Peng, and T. Habetler, "Multilevel inverters for electric vehicle applications," in *Proc. Power Electronics in Transportation*, 1998, pp. 79–84. 33, 43

[81] F. Z. Peng, J.-S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate dc sources for static var generation," *IEEE Trans. Ind. Applicat.*, vol. 32, no. 5, pp. 1130–1138, 1996. 33

[82] F. Z. Peng and J.-S. Lai, "Dynamic performance and control of a static var generator using cascade multilevel inverters," *IEEE Trans. Ind. Applicat.*, vol. 33, no. 3, pp. 748–755, 1997. 33

[83] F. Z. Peng, J. W. McKeever, and D. J. Adams, "A power line conditioner using cascade multilevel inverters for distribution systems," in *Proc. Conf Industry Applications Conf. Thirty-Second IAS Annual Meeting, IAS '97. Record of the 1997 IEEE*, vol. 2, 1997, pp. 1316–1321. 33

[84] F. Peng, J. McKeever, and D. Adams, "Cascade multilevel inverters for utility applications," in *Proc. 23rd Int. Conf. Industrial Electronics, Control and Instrumentation IECON 97*, vol. 2, 1997, pp. 437–442. 33

[85] G. Joos, X. Huang, and B. T. Ooi, "Direct-coupled multilevel cascaded series var compensators," in *Proc. Conf Industry Applications Conf. Thirty-Second IAS Annual Meeting, IAS '97. Record of the 1997 IEEE*, vol. 2, 1997, pp. 1608–1615. 33

[86] R. W. Menzies and Y. Zhuang, "Advanced static compensation using a multilevel gto thyristor inverter," *IEEE Trans. Power Delivery*, vol. 10, no. 2, pp. 732–738, 1995. 33, 36

[87] L. A. Tolbert, F. Z. Peng, T. Cunnyngham, and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1058–1064, 2002. 33, 43

[88] M. D. Manjrekar and T. A. Lipo, "A hybrid multilevel inverter topology for drive applications," in *Proc. 1998. Thirteenth Annual Applied Power Electronics Conf and Exposition APEC '98*, vol. 2, 1998, pp. 523–529. 33

[89] M. Manjrekar and T. Lipo, "A generalized structure of multilevel power converter," in *Proc. Int Power Electronic Drives and Energy Systems for Industrial Growth Conf*, vol. 1, 1998, pp. 62–67. 33

[90] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of multilevel inverters for static var compensation," in *Proc. Conf Industry Applications Society Annual Meeting Record of the 1994 IEEE*, 1994, pp. 921–928. 33, 36

[91] K. Corzine and Y. Familiant, "A new cascaded multilevel h-bridge drive," *IEEE Trans. Power Electron.*, vol. 17, no. 1, pp. 125–131, 2002. 33, 36

[92] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Applicat.*, vol. 35, no. 1, pp. 36–44, 1999. 36, 37, 38

[93] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Proc. rd Annual IEEE Power Electronics Specialists Conf. PESC '92 Record*, 1992, pp. 397–403. 38

[94] G. Sinha and T. A. Lipo, "A new modulation strategy for improved dc bus utilization in hard and soft switched multilevel inverters," in *Proc. 23rd Int. Conf. Industrial Electronics, Control and Instrumentation IECON 97*, vol. 2, 1997, pp. 670–675. 38

[95] S. Hiti, "Modeling and control of three-phase pwm converters," Ph.D. dissertation, Virginia Polytechnic Institute and State University (Virginia Tech), 1995. 45

[96] N. Celanovic, D.-H. Lee, D. Peng, D. Borojevic, and F. C. Lee, "Control design of three-level voltage source inverter for smes power conditioning system," in *Proc. 30th Annual IEEE Power Electronics Specialists Conf. PESC 99*, vol. 2, 1999, pp. 613–618. 45

[97] U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient modeling of modular multilevel hvdc converters (mmc) on electromagnetic transient simulation programs," *IEEE Trans. Power Delivery*, vol. 26, no. 1, pp. 316–324, 2011. 45

[98] E. W. H. Akagi and M. Aredes, *Instantaneous power theory and applications to power conditioning.* IEEE Press, New Jersey: John Wiley & Sons, Inc, 2007. 52, 54, 56

[99] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1398–1409, 2006. 53, 55

[100] E. Pouresmaeil, D. Montesinos-Miracle, and O. Gomis-Bellmunt, "Control scheme of three-level npc inverter for integration of renewable energy resources into ac grid," no. 99, 2011, early Access. 60, 130

[101] E. Pouresmaeil, O. Gomis-Bellmunt, D. Montesinos-Miracle, and J. Bergas-Jane, "Multilevel converters control for renewable energy integration to the power grid," *Energy*, vol. 36, no. 2, pp. 950 – 963, 2011. 61, 125

[102] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, 2009. 83, 87

[103] N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in *Proc. nd Annual IEEE Power Electronics Specialists Conf. PESC '91 Record*, 1991, pp. 96–103. 83

[104] J. P. i Felix, "Modulation and control of three-phase pwm multilevel converters," Ph.D. dissertation, Technical University of Catalonia, 2002. 85, 90, 99

[105] N. Celanovic, "Space vector modulation and control of multilevel converters," Ph.D. dissertation, Virginia Polytechnic Institute and State University (Virginia Tech), 2000. 85

[106] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Applicat.*, vol. 37, no. 2, pp. 637–641, 2001. 87

[107] J. Pou, D. Boroyevich, and R. Pindado, "New feedforward space-vector pwm method to obtain balanced ac output voltages in a three-level neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1026–1034, 2002. 94

[108] J. Pou, R. Pindado, D. Boroyevich, and P. Rodriguez, "Limits of the neutral-point balance in back-to-back-connected three-level converters," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 722–731, 2004. 101

[109] S. K. Mondal, B. K. Bose, V. Oleschuk, and J. O. P. Pinto, "Space vector pulse width modulation of three-level inverter extending operation into overmodulation region," *IEEE Trans. Power Electron.*, vol. 18, no. 2, pp. 604–611, 2003. 104

[110] S. K. Mondal, J. O. P. Pinto, and B. K. Bose, "A neural-network-based space-vector pwm controller for a three-level voltage-fed inverter

induction motor drive," *IEEE Trans. Ind. Applicat.*, vol. 38, no. 3, pp. 660–669, 2002. 104

[111] A. Kocalmis and S. Sunter, "Simulation of a space vector pwm controller for a three-level voltage-fed inverter motor drive," in *Proc. IECON 2006 - 32nd Annual Conf. IEEE Industrial Electronics*, 2006, pp. 1915–1920. 107

[112] O. G.-B. E. Pouresmaeil, D. Montesinos-Miracle and A. Sudria-Andreu, "Instantaneous active and reactive current control technique of shunt active power filter based on the three-level npc inverter," *European Transactions on Electrical Power*, vol. 21, pp. 2007–2022, 2011. 119

[113] S. Rahmani, N. Mendalek, and K. Al-Haddad, "Experimental design of a nonlinear control technique for three-phase shunt active power filter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 10, pp. 3364–3375, 2010. 121

[114] E. Pouresmaeil, D. Montesinos-Miracle, O. Gomis-Bellmunt, and J. Bergas-Jane, "A multi-objective control strategy for grid connection of dg (distributed generation) resources," *Energy*, vol. 35, no. 12, pp. 5022 – 5030, 2010. 121

[115] P. Verdelho and G. D. Marques, "An active power filter and unbalanced current compensator," *IEEE Trans. Ind. Electron.*, vol. 44, no. 3, pp. 321–328, 1997. 121

[116] [Online]. Available: http://www.powerdesigners.com/InfoWeb/designcenter/DesignTips/Electrolytics/Caps.htm. 125

Appendix A

Publications

This chapter presents the publications related to the specific topics of this thesis the author contributed to.

Journal Papers

Published

2012

1. S. Naderi, E. Pouresmaeil, and D.W. Gao, "The Frequency-Independent Control Method for Distributed Generation Systems", Applied Energy, Special Issue on Smart Grid. DOI:10.1016/j.apenergy.2011.09.034.

2011

2. E. Pouresmaeil, D. Montesinos-Miracle, and Oriol Gomis-Bellmunt, "Control Scheme of Three-level Inverter for Integration of Renewable Energy Resources into AC Grid," IEEE System Journal, DOI: 10.1109/JSYST.2011.2162922.

3. E. Pouresmaeil, O. Gomis-Bellmunt, D. Montesinos-Miracle, and J. Bergas-Jane, "Multilevel Converters Control for Renewable Energy Integration to the power Grid," Energy, vol. 36, no. 2, pp. 950-963, 2011.

4. E. Pouresmaeil, D. Montesinos-Miracle, O. Gomis-Bellmunt, and A. Sudria-Andreu, "Instantaneous Active and Reactive Current Control Technique of Shunt Active Power Filter Based on the Three-Level NPC Inverter," European Transactions on Electrical Power, vol. 21, no. 7, pp. 2007-2022, 2011.

2010

5. E. Pouresmaeil, D. Montesinos-Miracle, O. Gomis-Bellmunt, and Joan Bergas-Jane, "A Multi-objective Control Strategy for Grid Connection of DG (Distributed Generation) Resources," Energy, vol. 35, no. 12, pp. 5022-5030, 2010.

6. M.F. Akorede, H. Hizam, and E. Pouresmaeil, "Distributed energy resources and benefits to the environment," Renewable and Sustainable Energy Reviews, vol. 14, no. 2, pp. 724-734, 2010.

Other journal contributions

2011

7. E. Pouresmaeil, M.F. Akorede, and M. Hojabri, "A Hybrid Algorithm for Fast Detection and Classification of Voltage Disturbances in Electric Power Systems," European Transactions on Electrical Power, vol. 21, no. 1, pp. 555-564, 2011.

2010

8. M. Hojabri, H. Hizam, N. Mariun, S.M. Abdullah, and E. Pouresmaeil, "Available Transfer Capability for Power System Planning Using Krylov-Algebraic Method," International Review of Electrical Engineering, vol. 5, no. 5, pp. 2251-2262, 2010.

Submitted and under review

9. E. Pouresmaeil, D. Montesinos-Miracle, O. Gomis-Bellmunt, C. Miguel-Espinar, "Interfacing of Three-level H-bridge Converter for Connection of DG to the Grid and Compensation of Balanced and Unbalanced Loads," IEEE Transactions on Industrial Informatics.

10. E. Pouresmaeil, C. Miguel-Espinar, M. Massot-Campos, D. Montesinos-Miracle, O. Gomis-Bellmunt, "A PLL-less Control Technique for Integration of DG Units to the Electrical Networks,"IEEE Transactions on Industrial Electronics.

11. E. Pouresmaeil, D. Montesinos-Miracle, O. Gomis-Bellmunt, J. Bergas-Jane, "Frequency-Independent Control of Multilevel Converters for the Integration of Distributed Generation Power into AC Grid," Electrical Engineering.

12. E. Pouresmaeil, M.F. Akorede, D. Montesinos-Miracle, and O. Gomis-Bellmunt, "Hysteresis Current Control Technique of VSI for Compensation of Grid-connected Unbalanced Load," Expert Systems With Applications.

13. E. Pouresmaeil, D. Montesinos-Miracle, and O. Gomis-Bellmunt, "A Flexible Control Technique Based on SVPWM for DG Connection to the Grid," International Journal of Electrical Power and Energy Systems.

Book chapter

1. D. Montesinos-Miracle, J. Bergas-Jane and E. Pouresmaeil, "Electrical drives and power electronics", in "Electrical Energy Efficiency: Technologies and Applications", Edited by Andreas Sumper, Angelo Baggini, John Wiley & Sons, In Press.

Conference papers

1. E. Pouresmaeil, D. Montesinos-Miracle, and O. Gomis-Bellmunt, "Interfacing Renewable Energy Resources to the Utility Grid Using a Cascaded Multilevel Inverter," Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011).

2. M.F. Akorede, H. Hizam, I. Aris, M.Z.A. Ab. Kadir, and E. Pouresmaeil, "Economic Viability of Distributed Energy Resources Relative to Substation and Feeder Facilities Expansion," IEEE International Conference on Power and Energy, pp. 238-42, 2010.