TESI DOCTORAL

Títol

Electric-Device Characterization for Interference Prediction and Mitigation by an Optimal Filtering Design

Realitzada per Albert-Miquel Sánchez Delgado

en el Centre Enginyeria i Arquitectura La Salle, Universitat Ramon Llull

i en el Departament Comunicacions i Teoria del Senyal

Dirigida per Joan Ramon Regué Morreres

C. Claravall, 1-3
08022 Barcelona
Tel. 936 022 200
Fax 936 022 249
E-mail: urlsc@sec.url.es
www.url.es

Abstract

The common mode and differential mode interference propagated through the single-phase power-line cable is usually suppressed with power-line filters. This kind of filters is composed by common-mode chokes, X capacitors and Y capacitors to mitigate both the common mode and the differential mode. However, the present-day power-line filter design methodologies present some disadvantages: they are designed to be placed in an ideal 50-Ω system and the common mode and differential mode attenuations are analyzed independently, without considering the mode conversion that can be produced by asymmetries in the power-line filter, in the power-line network or in the electric device. These facts lead to inaccurate predictions of the power-line filter behavior and, consequently, the suitable filter is usually selected by trial and error in long and expensive measurement sessions. In order to improve this situation, this work presents:

- New measurement systems and characterization methodologies to completely model the behavior of power-line filters, power-line networks and electric devices. To this end, a new characterization methodology is presented: the modal characterization, that confines the common mode and the differential mode into a different port and provides the information about the propagation of the modal interference, information that can be useful to select the suitable filter for its mitigation.

- A new methodology to accurately predict the level of conducted emissions that an electric device supplies to the power-line network through its power-line filter, based on the measurement systems and characterization methodologies presented before. Accurate characterizations will allow predictions similar to the actual conducted emissions, avoiding long measurement sessions.

- New design methodologies of power-line filters to achieve optimal and low cost implementations. In a first proposal, the components of the power-line filters are modally characterized to find, by computation, the combination that gets the desired filtering response with the minimum number of components. This methodology is further improved by using asymmetric power-line filters, obtaining an optimal mitigation of the common and differential mode.

All measurement systems, as well as characterization, prediction and designing methodologies, have been successfully tested on actual devices.

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About the Author

Albert-Miquel Sánchez Delgado received the Bachelor and Master degrees in Telecommunication Engineering from Enginyeria i Arquitectura La Salle, Ramon Llull University (URL), Barcelona, in 2004 and 2006 respectively. In March 2006 he was awarded with a Ph.D. scholarship from the local catalan government (FI-G 2008FIC 00275, *Departament d'Universitats, Recerca i Societat de la Informació*) and, since then, he has been an active member of the Communications and Electromagnetics Research Group (GRECO) at Enginyeria i Arquitectura La Salle (URL).

The author has participated in the project *Analysis of the Common and Differential Mode Interference in Electronic Devices and Its Mitigation by Means of Multimodally Adapted Power-Line Filters*, supported by the *Ministerio de Educación y Ciencia* (TEC 2005-04238) and the project *FPGA System Boards to Digitalize and Process Radiofrequency Signals*, supported by the *Agència de Gestió d'Ajuts Universitaris i de Recerca* (2006PEIR-10010-3). He has exerted as assistant professor in *Electromagnetic Theory* since 2008 and *Digital Communications* for the period 2005-2009, at Enginyeria i Arquitectura La Salle (URL). Before, he had been working as an EMC engineer, performing pre-compliance tests, for the period 2003-2007 at the same institution.

During his Ph.D. research period, he was awarded with an international research mobility fund (2009 BE-100052, *Agència de Gestió d'Ajuts Universitaris i de Recerca*), which allowed him to perform a three-month stay in the *Dipartimento di Elettrotecnica*, EMC section, of *Politecnico di Milano*, Italy, working on the application of time-domain measurements for the characterization of electric devices.

Preface

Background

The Electromagnetic Compatibility (EMC) is the science that analyzes the attitude of an electric device to correctly work in its electromagnetic environment, and it is divided in two main branches:

- The Electromagnetic Interference (EMI) measures the interference level that a device generates and emits either via its power-line cable (conducted EMI), or by radiated waves (radiated EMI).

- The Electromagnetic Susceptibility (EMS) measures the interference level that a device is able to support, either in a radiated or conducted way, without altering its performance.

The Research Group in Electromagnetism and Communications (GRECO, `http://www.salle.url.edu/GRECO/`), which belongs to the Department of Electronics and Telecommunications from Engineering and Architecture La Salle, Ramon Llull University, has a long experience in the EMC field. Its activity started in 1989 as a laboratory for radioelectric measurements, an it was accredited as a Laboratory for Radioelectric Homologations in 1993. In 1992 the laboratory started to offer measurements for EMC precertifications and engineering, giving solutions to tens of companies in the electronic and telecommunications sector.

With regard to research, the group has focused on two main topics:

- Alternative EMC measurement systems (since 1998): the electromagnetic far field of an electric device can be predicted from near field measurements in order to get the same results obtained in a big anechoic chamber, having the advantage that such structure is not needed. This research can be found in the doctoral thesis of Joan Ramon Regué Morreres.

- Modal modeling (since 1998): any system that propagate more than one mode can be modeled as a new structure where each mode is confined to a different port. This model keeps the same behavior as the original one and can be used to study the propagation of a particular mode in the system. The modal modeling was originally applied on microwave coplanar circuits in the doctoral thesis of Miquel Ribó i Pal, and afterward was used to analyze the electromagnetic interference propagation in printed circuit boards in the doctoral thesis of Francisco Javier Pajares Vega and microstrip lines in the doctoral thesis of Pablo Rodríguez Cepeda.

From the experience obtained in the last research topic arose the idea of its application on power-line filters (PLFs) and electric and electronic devices for interference prediction. With this aim, the modal modeling technique was used to characterize the interference propagation in a single-phase power-line cable and extended to model the complete behavior of PLFs, electric devices and power-line networks (PLNs). The results of this research can be found in the doctoral thesis of Antonio Pérez Jiménez, finished in 2008, and in this thesis report. The early research about modal characterization of PLFs started in 2004, and has been supported, since then, by the Spanish Government Projects TEC 2004-02196 and TEC 2005-04238 (*Ministerio de Educación y Ciencia*).

Structure of the document

The work presented in this document is mainly centered on the characterization, prediction and elimination of the conducted EMI by designing a suitable filtering device known as PLF. The main lines of the research have been structured as follows:

- **Chapter 1: Introduction.** The most important concepts, the state of the art and its associated present-day problems are introduced in this chapter in order to justify the research, as well as the objectives expected to achieve. This work turns around the interference decomposition into its modal components, that is, the common mode (CM) and the differential mode (DM), and the development of different methodologies to characterize, predict and eliminate them.

- **Chapter 2: Power-Line Filter Characterization.** Two different PLF characterization methods are presented in this chapter: the first one can be used to characterize its circuital behavior, that is, the PLF effect on the circuital voltages and currents; the second one can be used to characterize its modal behavior, that is, the PLF effect on the modal voltages and currents. Both methods are based on the scattering parameters (S parameters) and the characterizations obtained allow the prediction of the PLF performance in front of any situation.

- **Chapter 3: Electric Devices and Power-Line Network Characterization.** The characterization of the PLF has no sense without the information of the impedance and

conducted emissions of the electric device and the PLN. In this chapter a complete characterization of PLNs and electric devices and their respective measurement systems, all in the frequency domain, are presented and validated. Again, the characterization can be performed from the circuital point of view with circuital impedances and emissions, or from the modal point of view with modal impedances and emissions.

- **Chapter 4: Characterization of Conducted Emissions in Time Domain.** When the measurements are performed in the frequency domain and according to the EMC standards, a long time process is required, making difficult, for instance, the measurement of non-stationary interference. In this chapter, time-domain techniques are studied and applied to characterize the conducted emissions of electric devices, and their advantages are shown when measuring an actual device with impulsive conducted emissions.

- **Chapter 5: Prediction of Conducted Emissions.** Using the characterizations of the different devices involved in a measurement of conducted emissions, a new methodology to predict the conducted emissions present at the line side of a PLF is presented. This methodology is validated by comparing the predicted emissions with the measured ones according to the EMC standards.

- **Chapter 6: Power-Line Filter Design from S-Parameter Measurements.** If the characterization of a PLF through its S parameters is useful to predict the conducted emissions of an electric device connected to it, the same characterization can be applied to the individual components that constitutes the PLF, that is, common-mode chokes (CMC) and X and Y capacitors. The PLF design methodology presented in this chapter finds the best combination of these components to filter the interference under the limit imposed by the EMC standards, and presents the results sorted according to the interests of the EMC designer.

- **Chapter 7: Power-Line Filter Design Using Mode Conversion.** Using asymmetric structures of PLFs, and therefore, provoking mode conversion, this chapter extends the design methodology to obtain optimal filters. The mode conversion phenomenon is analyzed in deep through two new modal models that characterize the modal behavior of CMCs and X and Y capacitors and allow the direct visualization of the effects produced by their asymmetrization.

- **Chapter 8: Conclusions and Future Work.** A summary of the work carried out on the objectives, and the means by which they have been achieved is presented. The future work is also examined.

- **Bibliography.** All the references of this document can be found in this section sorted by their order of appearing.

- **Appendix.** The derived equations to transform S parameters to T parameters and vice versa are shown.

Contents

Abstract **iii**

Acknowledgments **v**

About the Author **vii**

Preface **ix**

Acronym Glossary **xxiii**

Symbol Glossary **xxv**

1 Introduction **1**

1.1 Signals in the Power-Line Terminals 1
1.2 Circuit and modal conducted emissions of a device 4
1.3 Power-line filters 5
1.4 Electric device and power-line network characterization 8
1.5 Modal analysis 10
1.6 Research objectives 10

2 Power-Line Filter Characterization **15**

2.1 Introduction 15
2.2 Circuit and modal characterization of linear four-port devices 16
2.3 Measurement system 20
2.4 Extended measurement system 22

3 Electric Devices and Power-Line Network Characterization **29**

3.1 Introduction 30
3.2 Circuit and modal characterization of electric devices and power-line networks . 30
3.3 Measurement system for electric devices 34
3.4 Measurement system for power-line networks 41
3.5 Measurements on real devices and networks 48

4 Characterization of Conducted Emissions in Time Domain 53
4.1 Introduction . . . 53
4.2 Theory of signal processing . . . 55
4.3 Measurement system . . . 57
4.4 Characterization of electric devices with non-stationary emissions . . . 61

5 Prediction of Conducted Emissions 67
5.1 Introduction . . . 67
5.2 Methodology for the prediction of the conducted emissions . . . 68
5.3 Experimental validation . . . 68

6 Power-Line Filter Design from S-Parameter Measurements 77
6.1 Introduction . . . 77
6.2 Methodology for a PLF design . . . 78
6.3 Experimental validation . . . 81

7 Power-Line Filter Design Using Mode Conversion 91
7.1 Introduction . . . 92
7.2 Modal characterization of PLF capacitors . . . 93
7.3 Modal characterization of CMCs . . . 96
7.4 Parametric study of the mode conversion . . . 99
7.5 Design of the optimal components of a PLF . . . 102
7.6 Experimental Validation . . . 105

8 Conclusions and Future Work 113
8.1 Conclusions . . . 113
8.2 Future work . . . 116

Bibliography 121

Appendix 135
.1 S parameters to T parameters . . . 135
.2 T parameters to S parameters . . . 136

List of Figures

1.1 The single-phase PLN. 2
1.2 Decomposition of the circuit voltages and currents (a) propagated in a single-phase power-line cable as an addition of the CM (b) and the DM (c). 4
1.3 PLF connection. 5
1.4 PLF structure. 5
1.5 PLF, DUT and PLN traditional analysis: a) physical device; b) modal characterization. 11
1.6 PLF, DUT and PLN modal analysis: a) physical device; b) modal characterization. 11

2.1 Linear RF circuit characterizations: a) physical; b) circuit; c) modal. 16
2.2 Circuit port definition in a S-parameter measurement. 17
2.3 Modal port definition in a S-parameter measurement. 18
2.4 S-parameter measurement with a VNA. 20
2.5 CM and DM IL of a PLF (Prefilter FB-2Z 2A), obtained from the modal S-parameter characterization and from the measurements performed according to the standard ANSI C63.13. 21
2.6 CM and DM attenuation of a PLF (Belling Lee SF4110-1/01 1A), with different load impedances. 21
2.7 Energy transfer between the line and load sides for the PLF: Belling Lee SF4110-1/01 1A. 22
2.8 S-parameter measurement system for PLF under operating conditions. 23
2.9 The LISN can be considered as linear four-port device when it is seen from L_{monX} and N_{monX} or L_{devX} and N_{devX} ports (for $X = 1, 2$). 24
2.10 Comparison of the CM and DM attenuation for the PLF Belling Lee SF4110-1/01 1A measured with and without LISNs. 25
2.11 Comparison of the CM and DM attenuation for the PLF Belling Lee SF4110-1/01 1A and current rates between 0 A and 6 A. 25
2.12 Comparison of the mode conversion between the CM at the line side and the DM at the load side and between the DM at the line side and the CM at the load side for the PLF Belling Lee SF4110-1/01 1A and current rates between 0 A and 6 A. 26

2.13 Magnetic flux direction in the ferromagnetic core due to DM currents (a) and CM currents (b). 27
2.14 CM and DM attenuation comparison of a 2-mH CMC with different current levels. 27
2.15 Mode conversion comparison between the line side CM and the load side DM and between the line side DM and the load side CM produced in a 2-mH CMC with different current levels. 28

3.1 DUT and PLN characterization: a) physical; b) circuit; c) modal. 31
3.2 DUT and PLN circuit model. 31
3.3 DUT and PLN modal model. 33
3.4 Block diagram of the S-parameter measurement setup of a DUT. 35
3.5 Block diagram of the voltages and currents measurement setup at the DUT terminals. 35
3.6 Equivalent circuit of the measurement system. 36
3.7 Image and circuit of the test device. 37
3.8 Comparison between the physical impedances of the test device measured individually and the impedances of the circuit model obtained from the S-parameter measurement after applying (3.1). 38
3.9 Comparison of the interference sources obtained from the values of V'_{nL} and V'_{nN} after applying (3.10) and the ones obtained from the conducted emissions measurement after applying (3.3). 39
3.10 Comparison of the modal impedances obtained after applying (3.6) to the physical impedances measured individually and the impedances of the circuit model obtained from the S-parameter measurement. 40
3.11 Comparison of the modal interference sources obtained from the physical voltage sources mathematically converted with (3.10), and from the interference sources of the circuit model. 41
3.12 CNs used for the measurement of PLNs. 42
3.13 Block diagram of the S-parameter measurement setup of a PLN. 42
3.14 Block diagram of the voltages and currents measurement setup at the PLN terminals. 43
3.15 Equivalent circuit of the PLN measurement setup. 43
3.16 Test network. 44
3.17 Comparison between the impedance values Z_L, Z_N and Z_T of the test network of figure 3.16 computed and measured. 45
3.18 Comparison between the interference sources V_{nN} and V_{nL} of the circuit model of the test network and the ones obtained by applying (3.10) to its physical sources. 46
3.19 Comparison between the modal impedances Z_{CM}, Z_{DM} and Z_{TM} of the test network obtained from the impedances measured individually and from the impedances of the circuit model. 47

3.20 Comparison of the modal interference sources obtained from the physical voltage sources mathematically converted with (3.10), and from the interference sources of the circuit model. 48
3.21 100-W HF Transceiver with a switching power supply. 48
3.22 Circuit and modal impedances of the 100-W HF transceiver. 49
3.23 Circuit interference sources of the 100-W HF transceiver. 49
3.24 Modal interference sources of the 100-W HF transceiver. 50
3.25 Circuit and modal impedances of a PLN in an office environment. 50
3.26 Circuit interference sources of a PLN in an office environment. 51
3.27 Modal interference sources of a PLN in an office environment. 51

4.1 Different window functions. 56
4.2 Two possible setups for the conducted emissions measurements in time domain via (a) current measurements or (b) voltage measurements. 58
4.3 Switching power supply connected to several loads. 59
4.4 Spectrum of the I_L and I_N currents measured with both setups of figure 4.2. . 60
4.5 Simulation of the circuit conducted emissions of a DUT. 60
4.6 Comparison between simulated and measured conducted emissions of a switching power supply. 61
4.7 Conducted emissions of a switching power supply with the three EMI detectors: peak, quasi-peak and average detector. 62
4.8 Conducted emissions of a switching power supply at the frequency of 200 kHz and zero-span. 62
4.9 Conducted emissions of the switching power supply measured in time domain. . 63
4.10 Comparison between the simulated conducted emissions and the conducted emissions measured with the peak detector. 63
4.11 STFT of the conducted emissions at the L terminal (V_L). 64
4.12 Comparison between the simulated conducted emissions and the conducted emissions measured with the peak detector. 64
4.13 Simulation of the modal conducted emissions of a DUT. 65
4.14 Modal conducted emissions of the switching power supply. 65

5.1 Circuit simulation of a DUT with a PLF. 69
5.2 Modal simulation of a DUT with a PLF. 69
5.3 Block diagram for the measurement setup of the voltage in the line terminals of a DUT with a PLF. 70
5.4 Predicted and measured circuit voltages (V_L and V_N) for the configuration of figure 5.3. 71
5.5 Predicted and measured circuit voltages (V_{CM} and V_{DM}) for the configuration of figure 5.3. 72

5.6 Comparison between the conducted emissions predicted according to the common engineering practice and the measured ones. 74
5.7 Predicted and measured circuit voltages V_L and V_N for the 100-W HF transceiver. 74
5.8 Predicted and measured modal voltages V_{CM} and V_{DM} for the 100-W HF transceiver. 75
5.9 Comparison between the conducted emissions predicted according to the common engineering practice and the measured ones. 76

6.1 Block diagram of the implementation of CMC, X-capacitor and Y-capacitor networks. 79
6.2 CMCs and capacitors placed in individual boards. 79
6.3 Block diagram of the PLF implementation: (a) PLF of order 1; (b) PLF of order 2; (c) PLF of order n. 79
6.4 Block diagram for the simulation of the circuit conducted emissions of a DUT connected to a PLF of n^{th} order. 80
6.5 Block diagram for the simulation of the modal conducted emissions of a DUT connected to a PLF of n^{th} order. 80
6.6 Connection of three different components to build a complete PLF. 81
6.7 Circuit and modal S parameters of a network composed by a X capacitor of 100 nF. 82
6.8 Circuit and modal S parameters of a network composed by two Y capacitors of 3.3 nF. 82
6.9 Circuit and modal S parameters of a network composed by a CMC of 10 mH. . 83
6.10 Circuit and modal S parameters of a PLF composed by a X capacitor of 100 nF, two Y capacitors of 3.3 nF and a CMC of 10 mH. 83
6.11 Microcontroller with a 4 MHz clock used to validate the PLF design methodology. 84
6.12 Circuit conducted emissions V_L and V_N of the switching power supply without any PLF. 84
6.13 Modal conducted emissions V_{CM} and V_{DM} of the switching power supply without any PLF. 84
6.14 Circuit and modal S parameters of the LISN. 85
6.15 Circuit conducted emissions V_L and V_N of the switching power supply with a first-order PLF composed by a CMC of 10 mH. 85
6.16 Circuit conducted emissions V_L and V_N of the switching power supply with a third-order PLF composed by a X capacitor of 100 nF, two Y capacitors of 3.3 nF and a CMC of 10 mH. 86
6.17 Structure of the optimal PLF obtained with the design methodology. 86
6.18 Circuit conducted emissions V_L and V_N of the switching power supply with a PLF composed by a CMC of 20 mH and a X capacitor of 100 nF. 87
6.19 Modal conducted emissions V_{CM} and V_{DM} of the switching power supply with a PLF composed by a CMC of 20 mH and a X capacitor of 100 nF. 87

6.20 Structure of the swapped PLF. 88
6.21 Circuit conducted emissions V_L and V_N of the switching power supply with the original and the swapped PLF, both composed by a X capacitor of 100 nF and a CMC of 20 mH. 88
6.22 Circuit and modal conducted emissions of the switching power supply with non-stationary noise. 89
6.23 Structure of the PLF designed by the methodology. 89
6.24 Comparison between the predicted and measured circuit conducted emissions of the switching power supply connected to the PLF of figure 6.23. 90
6.25 Prediction of the modal conducted emissions of the switching power supply connected to the PLF of figure 6.23. 90

7.1 Impedance network connected to L, N and G terminals. 93
7.2 Modal model of a shunt-connected two-port network. 94
7.3 Models for X capacitor networks: (a) Circuit model. (b) Full modal model. (c) Simplified modal model. 95
7.4 Models for Y capacitor networks: (a) Circuit model. (b) Modal model. 96
7.5 Models for star capacitor networks: (a) Circuit model. (b) Modal model. 96
7.6 Two-port network series-connected to the L and N terminals. 97
7.7 Modal model of a series-connected two-port network. 98
7.8 Ideal CMC series-connected to the L and N terminals (a) and its modal model (b). 99
7.9 Propagation of the modal interference in the modal model of Y and X capacitors (b), placed between the modal model of a DUT (a) and the modal model of a PLN without interference (c). 100
7.10 V_{CMout} and V_{DMout} for different values of C_{Y1}. 100
7.11 Propagation of the modal interference in the modal model of CMCs (b), placed between the modal model of a DUT (a) and the modal model of a PLN without interference (c). 101
7.12 V_{CMout} and V_{DMout} for different values of L_2. 102
7.13 Block diagram of the GA performance. 103
7.14 Circuit conducted emissions of the DUT connected to the asymmetric PLF obtained with the GA (table 7.3) and the symmetric PLF (C_X = 87 nF and $L_1 = L_2 = 8.2$ mH). 104
7.15 Modal conducted emissions of the DUT connected to the asymmetric PLF obtained with the GA (table 7.3) and the symmetric PLF (C_X = 87 nF and $L_1 = L_2 = 8.2$ mH). 104
7.16 Equivalent circuit for a real capacitor. 105
7.17 Comparison between measured and computed modal S-parameters in X- and Y-capacitor networks. 106

7.18 Modal models of X and Y capacitors connected to the modal models of a DUT and a LISN, and to the measured modal S parameters of a CMC. 107
7.19 Measured and predicted modal interference levels. 107
7.20 CM and DM conducted emissions without PLF, with the balanced PLF (two Y capacitors), and with the unbalanced PLF (one Y capacitor). 108
7.21 CM and DM conducted emissions with the unbalanced PLF (one Y capacitor) and with the PLF without the Y-capacitor network. 108
7.22 Equivalent circuit for actual CMCs. 109
7.23 Comparison between measured and computed modal S parameters of a 1-mH CMC. 110
7.24 Modal model of an actual CMC connected to the modal models of a DUT and a LISN. 110
7.25 Measured and predicted modal interference levels. 111
7.26 Comparison between the modal S parameters of the asymmetric CMC with and without current. 111
7.27 CM and DM conducted emissions with the original CMC, and with the unbalanced CMC. 112

8.1 Definition of modal voltages and currents in a three-line-microstrip transmission line: (a) *ee* mode or CM; (b) *oo* mode or DM_1; (c) *oe* mode or DM_2. 117

List of Tables

5.1 Comparaison of the modal voltages (V_{CM}, V_{DM}) measured, predicted with $Z_{TM} = \infty$ and predicted with the Z_{TM} of figure 3.19, for the test device of figure 3.7 and the PLF Belling-Lee SF4110-1. 73

6.1 Measured X-capacitor networks for the PLF design methodology. 81
6.2 Measured Y-capacitor networks for the PLF design methodology. 81
6.3 Measured CMC networks for the PLF design methodology. 82

7.1 Modal model values of the DUT and the PLN. 99
7.2 Modal model values of the DUT and the PLN. 101
7.3 Component values of the PLF found by the GA. 103
7.4 Component values of the 100-nF X-capacitor equivalent circuit (Z_{CX}) and of the two 10-nF Y-capacitor equivalent circuits (Z_{CY1} and Z_{CY2}). 105
7.5 Component values of the equivalent circuit of a 1-mH toroidal CMC. 109

Acronym Glossary

ADC	Analog to Digital Converter
AMN	Artificial Mains Network
CM	Common Mode
CMC	Common Mode Choke
CN	Coupling Network
DC	Direct Current
DM	Differential Mode
DFT	Discrete Fourier Transform
DUT	Device Under Test
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EMS	Electromagnetic Susceptibility
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
G	Ground
GA	Genetic Algorithm
HF	High Frequency
HPF	High Pass Filter
IL	Insertion Loss
L	Line
LISN	Line Impedance Stabilization Network
MTL	Multiconductor Transmission Line

N	Neutral
PLC	Power-Line Communications
PLF	Power-Line Filter
PLN	Power-Line Network
PSD	Power Spectral Density
RBW	Resolution Bandwidth
RC	Resistor-Capacitor
RMS	Root Mean Square
RF	Radio Frequency
S	Scattering
SA	Spectrum Analyzer
STFT	Short-Time Fourier Transform
T	Transmission
TOSM	Through-Open-Short-Match
VNA	Vector Network Analyzer
VSA	Vector Spectrum Analyzer
Y	Admittance
Z	Impedance

Symbol Glossary

$[a]$	Input wave matrix
$[a_M]$	Modal input wave matrix
a_{CM}	Input wave for the common mode
a_{DM}	Input wave for the differential mode
a_L	Input wave present at the line terminal
a_N	Input wave present at the neutral terminal
$[b]$	Output wave matrix
$[b_M]$	Modal output wave matrix
b_{CM}	Output wave for the common mode
b_{DM}	Output wave for the differential mode
b_L	Output wave present at the line terminal
b_N	Output wave present at the neutral terminal
C_X	Capacitor between line and neutral terminals
C_{Y1}	Capacitor between line and ground terminals
C_{Y2}	Capacitor between neutral and ground terminals
f_s	Frequency sampling
G_C	Coherent gain
I_{CM}	Common-mode current
I_{DM}	Differential-mode current
I_L	Current at line terminal
I_N	Current at neutral terminal
L_1	Inductance at line terminal

L_2	Inductance at neutral terminal
$\mathbf{L}_{dev}$	DUT line-port of the LISN
$\mathbf{L}_{mon}$	Monitor line-port of the LISN
$\mathbf{L}_{PL}$	PLN line-port of the LISN
$\mathbf{N}_{dev}$	DUT neutral-port of the LISN
$\mathbf{N}_{mon}$	Monitor neutral-port of the LISN
$\mathbf{N}_{PL}$	PLN neutral-port of the LISN
M	Mutual inductance
V_{CM}	Common-mode voltage
$[S]$	S parameter matrix
$[S_M]$	Modal S parameter matrix
$[T]$	T parameter matrix
$[T_{ob}]$	Observation time
V_{DM}	Differential-mode voltage
V_{BL}	Voltage at the monitor line-port of the LISN or CN
V_{BN}	Voltage at the monitor neutral-port of the LISN or CN
V_L	Line voltage
V_N	Neutral voltage
V_{nCM}	Source of common-mode noise
V_{nDM}	Source of differential-mode noise
V_{nL}	Source of noise at line terminal
V_{nN}	Source of noise at neutral terminal
$w[n]$	Window function
$x[n]$	Discrete-time signal
$x_w[n]$	Discrete-time windowed signal
$x(t)$	Continuous-time signal
$X[k]$	Discrete-frequency spectral sequence
$X(k\Delta f)$	Continuous-frequency spectral sequence

$X_w[k]$	Discrete-frequency windowed signal
Z_0	Characteristic impedance
Z_{0CM}	Common-mode characteristic impedance
Z_{0DM}	Differential-mode characteristic impedance
Z_{CM}	Common-mode impedance
Z_{CX}	Impedance of the capacitor placed between line and neutral terminals
Z_{CY1}	Impedance of the capacitor placed between line and ground terminals
Z_{CY2}	Impedance of the capacitor placed between neutral and ground terminals
Z_{DM}	Differential-mode impedance
Z_L	Line impedance
Z_N	Neutral impedance
Z_T	Circuital transimpedance
Z_{TM}	Modal transimpedance
Δt	Sampling interval
Δf	Frequency interval

Chapter 1

Introduction

Contents of this chapter

1.1 Signals in the Power-Line Terminals 1
1.1.1 The power-line network 1
1.1.2 Classification of interference signals 2
1.1.3 Signal characterization 3
1.2 Circuit and modal conducted emissions of a device 4
1.3 Power-line filters 5
1.3.1 Power-line filter structure 5
1.3.2 Power-line filter characterization 6
1.3.3 Standards of Electromagnetic Compatibility 7
1.3.4 Power-line filter design 7
1.4 Electric device and power-line network characterization 8
1.4.1 Impedance measurements of an electric device 8
1.4.2 Impedance measurements of a PLN 9
1.4.3 Equivalent models 9
1.5 Modal analysis 10
1.6 Research objectives 10

1.1 Signals in the Power-Line Terminals

1.1.1 The power-line network

The early electric power distribution networks or, as they are commonly named, power-line networks (PLNs), appeared at the end of the XIX century and the beginning of the XX century.

These PLNs evolved in a different way according to the needs of each region and, consequently, present-day PLNs exhibit different characteristics [1]. For instance, European PLNs use a 50-Hz and 230-V mains signal in contrast to the 60-Hz and 110-V mains signal of the American ones. A remarkable example is Japan, which uses, in the same country, both mains signal types. Despite of these differences, all kinds of PLNs share a similar structure: either they are constituted of a four-conductor structure (three-phase PLN) or a three-conductor structure (single-phase PLN).

In a three-phase PLN three sinusoidal voltages are propagated with a phase-shift of 120 degrees while only one sinusoidal voltage lies in a single-phase PLN. In Europe, the high and medium voltage distribution networks use a three-phase PLN structure. These networks transport tenths of kilovolts and they are placed between the generation and the transform substation, which steps down the voltage to the suitable 230 V [2]. However, low voltage distribution networks, that is, the part of the PLN that reaches the final customer, typically residential and small commercial or industrial sites, mainly uses the single-phase PLN structure. Therefore, most of the electric and electronic devices are connected to this kind of PLN.

1.1.2 Classification of interference signals

The three conductors of the single-phase PLN are known as line (L) and neutral (N), among which there is the mains signal, and ground (G), used for the protection of a possible current leakage, as shown in figure 1.1.

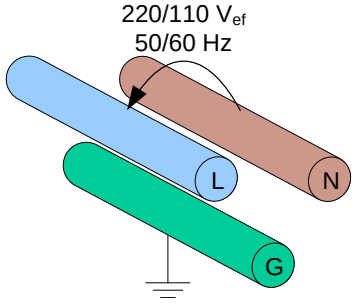

Figure 1.1: The single-phase PLN.

Apart from the power supply signal, the PLN is usually characterized by an additional noise that may disturb the performance of electric and electronic devices or interfere in power-line communications (PLC) [3]–[5]. The characteristics of this interference has been observed in several measurement campaigns, and they can be classified as [6], [7]:

- Colored background noise: wide-band interference caused by the addition of different noise sources with low power spectral density (PSD).

- Narrow-band noise: sinusoidal interference caused by the coupling of radiated signals coming from broadcast stations.

- Impulsive noise: short-time interference (usually with a duration less than 100 μs). According to its frequency repetition, they can be further classified in:

  a. Periodic impulsive noise synchronous to the mains frequency, with a repetition rate of 50 or 100 Hz and caused by the rectifier diodes stage of power supplies.

  b. Periodic impulsive noise asynchronous to the mains frequency, with a repetition rate between 50 and 200 kHz and mostly caused by switching power supplies.

  c. Asynchronous impulsive noise, of random nature and caused by the connection and disconnection of electric devices.

Alternatively, the signals mentioned above can be arranged according to their statistical behavior [8]:

- Stationary signal: narrow-band emissions and background noise.

- Quasi-stationary signal: Periodic impulsive noise synchronous and asynchronous to the mains frequency.

- Non-stationary signal: asynchronous impulsive noise.

The conducted emissions (interference at the L and N terminals) measured on the PLN or on the devices connected to it are usually a combination of signals of different nature, and the classifications presented above allow their identification. Once they have been recognized, it is necessary to completely characterize them in order to find a suitable device for their suppression.

1.1.3 Signal characterization

Any signal in the power-line terminals of a single-phase PLN can be characterized in two alternative ways:

1. Circuitally: the electrical signals are characterized considering the physical voltages between L and G (V_L) and between N and G (V_N), and the physical currents at the L (I_L) and N (I_N) terminals (figure 1.2(a)).

2. Modally: the electrical signals are characterized considering the modal decomposition in the common mode (CM) voltages and currents (V_{CM} and I_{CM}) (figure 1.2(b)) and the differential mode (DM) voltages and currents (V_{DM} and I_{DM}) (figure 1.2(c)).

The relationship between circuit and modal voltages and currents is [9]:

$$\begin{aligned} V_{CM} &= \frac{V_L + V_N}{2} \quad I_{CM} = I_L + I_N \\ V_{DM} &= V_L - V_N \quad I_{DM} = \frac{I_L - I_N}{2} \end{aligned} \tag{1.1}$$

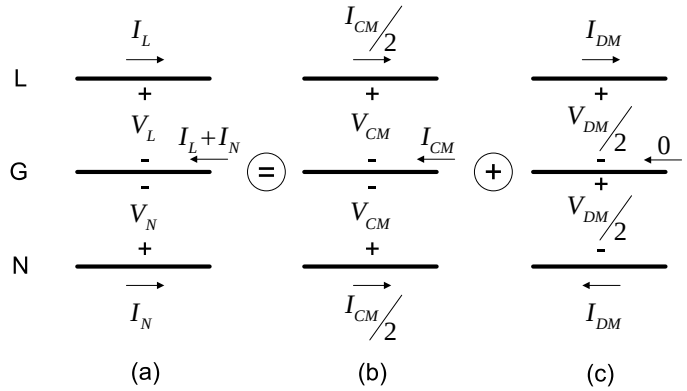

Figure 1.2: Decomposition of the circuit voltages and currents (a) propagated in a single-phase power-line cable as an addition of the CM (b) and the DM (c).

Both characterizations completely model any signal present in the PLN, and they can be easily measured, for instance, with an spectrum analyzer (SA). The different setups to measure the circuit and modal signals, and the importance of getting both signal characterizations, are shown in the following sections.

1.2 Circuit and modal conducted emissions of a device

New electric and electronic devices are appearing every day, and their massive use entails a considerable presence of electromagnetic pollution [10]. In order to control the interference level in the PLN, the conducted emissions of each device must be kept under a certain threshold. The international standard CISPR 22 [11] fixes the limit for circuit signals (V_L and V_N) between 150 kHz and 30 MHz, and establishes the setup configuration for the conducted emissions measurement: instead of using the actual PLN to supply the device under test (DUT), this is connected to an artificial mains network (AMN) in accordance with the standard CISPR 16 [12] named line impedance stabilization network (LISN). The function of the LISN is to filter the interference coming from the PLN, to present a constant impedance of 50 Ω in parallel with 50 μH to guarantee the repeatability of the measurements, and to lead the conducted emissions of the DUT toward the SA [9].

The measurement of the modal conducted emissions (V_{CM} and V_{DM}) can be obtained by inserting a signal combinator between the LISN and the SA. Thus, if the combinator adds the signals (0º combinator), the CM is obtained; if the combinator subtracts the signals (180º combinator), the DM is obtained. Different methodologies to implement such combinators can be found in the literature by using passive and low-cost components [13], transformers [14]–[17] or commercial RF combinators [18], [19]. However, the modal components of the interference can also be extracted without an external combinator if the relative phase between V_L and V_N is measured. Then, the modal conducted emissions are easily obtained using equation (1.1) [20].

1.3 Power-line filters

1.3.1 Power-line filter structure

Traditionally, the conducted emissions have been mitigated by using some kind of filters named power-line filters (PLFs). Such filters are connected to the power-line terminals of the DUT and are responsible to avoid the interference propagation from and to the DUT (electromagnetic interference (EMI) and electromagnetic susceptibility (EMS)), as seen in figure 1.3. Its simplest circuit is shown in figure 1.4, and consists of an X capacitor placed between L and N terminals to mitigate the DM (C_X); a common-mode choke (CMC) placed in L and N terminals (with an inductance L_1 and L_2 at L and N terminals respectively and a mutual inductance M) to mitigate the CM; and two Y capacitors, placed between L and G terminals (C_{Y1}), and between N and G terminals (C_{Y2}), to mitigate both CM and DM, [9], [21]. Some PLFs have, besides, a resistance between L and N terminals to discharge the X capacitors when the power supply is disconnected [21].

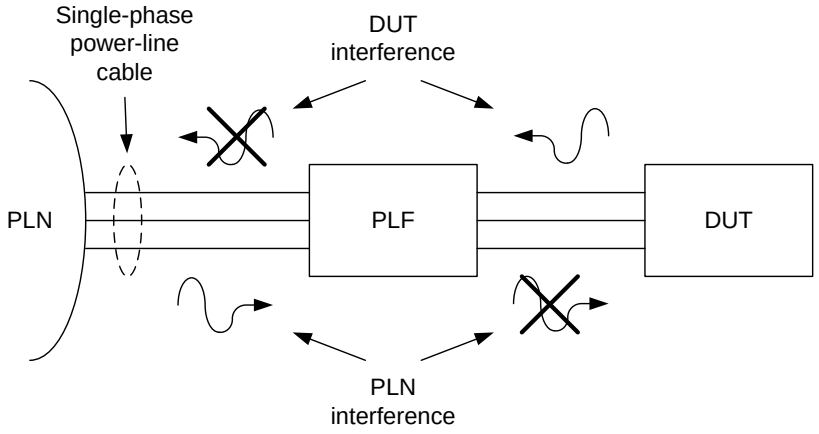

Figure 1.3: PLF connection.

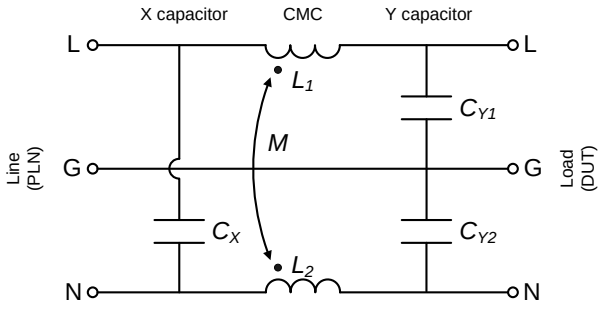

Figure 1.4: PLF structure.

Therefore, the measurement of both kinds of conducted emissions, that is, the circuit and modal emissions, is equally important: the circuit conducted emissions measurement allows

to know if the DUT fulfills the limit established by the standard, and the modal conducted emissions measurement allows the selection of the most suitable filtering component [22].

1.3.2 Power-line filter characterization

In front of a high conducted emissions level, it is essential to know which PLF can be used to solve the problem. The PLF manufacturers usually give the CM and DM insertion loss (IL) measurements performed in a 50-Ω measurement system, that is, the ratio of voltages appearing across the line immediately beyond the point of insertion, before and after insertion of the filter under test [23], [24]. However, this filter will unlikely be placed between actual DUTs and PLNs that present an ideal impedance of 50 Ω, and, without matching, its response can be severely degradated [10], [25].

This problem has been known for a long time, and different proposals to improve the characterization system have appeared in the literature [26]. For instance, in [27] the IL is measured connecting the PLF to a LISN instead of a 50-Ω impedance to simulate the inductive impedance of an actual PLN. And in [28] and [29] the IL is measured connecting the PLF directly to the DUT. However, the information obtained with these measurements can only be used when the PLF is connected to that particular line and load impedances, and it cannot be extrapolated to DUTs or PLNs with different input impedances. In this sense, the concept of worst-case IL gives a more general solution to the characterization problem. The worst-case IL is a useful parameter that gives the minimum attenuation that a PLF presents in any circumstance (with any line and load impedances), and it can be determined with the methods of [10], [30] and [31]. Other definitions based on the same idea have been used to describe the PLF behavior in unfavorable circumstances, such as the minimum voltage attenuation, the minimum current attenuation, the mismatch attenuation and the total attenuation in the worst case at the input or at the output, the minimum attenuation and the input impedance domain of the filter [30], [32]–[35]. But, if the designer of the PLF wants to ensure a minimum worst-case IL in the stop band, high frequency losses are needed, which means the addition of lossy components such as resistances or ferromagnetic materials [36]–[38]. Therefore, basing the PLF choice on the worst-case IL can lead to the use of over-dimensioned PLFs.

The S parameters can be used as an alternative characterization method for PLFs, as proposed in [39] and [40]. S parameters completely characterize the PLF and allow an accurate prediction of its behavior in front of any line and load impedances. Unfortunately, none direct information about the CM and DM mitigation is obtained. In order to obtain the information about the modal behavior, [41] decomposes the PLF in two networks, one to characterize the CM mitigation, and another to characterize the DM mitigation, and the behavior of each one is described through the Z-parameter matrix. The problem of the analysis of CM and DM mitigation in separate networks is that it can only be used with symmetric PLFs (symmetry with respect to the reference G) because mode conversion (any asymmetry in the PLF provokes a conversion from CM to DM, and vice versa) is not considered [42]. Besides, several asymmetric

structures are commonly used (such as inductive filters or pi-structures), and, hence, only some kinds of filters can be characterized this way [43].

1.3.3 Standards of Electromagnetic Compatibility

The standards of Electromagnetic Compatibility (EMC) that define the effectiveness of passive EMI filters describe test procedures to measure their behavior and obtain the characterizations presented above [44]:

- The military standard MIL-STD-220 [45] presents a measurement method for the IL of two-port filters in a 50-Ω measurement system.

- The international standard CISPR 17 [24] defines a method for the measurement of the IL for two-port filters in a 50-Ω or 75-Ω measurement system, and two variants for the worst-case measurement: a quasi analytic method in which the minimum voltage attenuation is obtained from the measurement of the Thevenin and the transfer impedance of the filter, and an approximate method in which the IL is measured in a system with line and load impedances of 0.1-Ω-100-Ω and 100-Ω-0.1-Ω respectively.

- The standard ANSI C63.13 [21] considers the PLF as a four-port network and extends the measurement methods to obtain the CM IL by short-circuiting the L and N terminals of the PLF, and the DM IL by connecting the L and N terminals of the PLF with a 180^{o} combinator.

- Finally, the IEEE standard 1560-2005 [46] provides a method to obtain the CM IL and DM IL of a PLF in a 50-Ω measurement system, three tests methods for the IL of a PLF with line and load impedances different from 50 Ω, a method for the S-parameter measurement and an annex on the worst-case behavior of PLFs, among other quality measurements.

In summary, there is not a general solution for the PLF characterization, but a collection of solutions more or less suitable depending on the problem to be analyzed. The circuit behavior of a PLF is completely characterized through its S parameters, but since the modal behavior is usually separated in independent CM and DM components (either by IL or worst-case measurements, or its CM and DM S-, Z- or Y-parameter matrix), there is not a complete and accurate PLF modal characterization method.

1.3.4 Power-line filter design

In order to optimize the cost of the electric or electronic device, it is usually better to design an specific PLF instead of using a commercial one. The most widespread methodology between EMC engineers is to identify the dominant mode in the conducted emissions of the DUT and modify the PLF components that directly affect that mode [47], [48]. In order to find the most

suitable component values, in [49]–[53] different methodologies based on the same principle are presented: firstly, the CM and DM equivalent circuits of a general PLF structure are found. Then, analyzing the desired attenuation level for the worst interference in each mode, and knowing the order of the filter (and, therefore, its attenuation slope), the necessary cut-off frequency is found. With this information, and setting the value of one of the components, the rest of the PLF components are finally obtained. However, these methodologies only consider ideal components, for what the real attenuation level at high frequencies is worse than the expected one. In [54] the repercussion of the parasitics in a CMC and a capacitor is emphasized, and presents some equivalent circuits to model them. These models are used in [55] when evaluating the PLF behavior at high frequencies, once the component values are found with the previous method.

Other authors use optimization techniques to design the PLF in order to improve its features as regards cost, weight and volume. For instance, from a fixed cut-off frequency, the optimal PLF topology is chosen in [56] by using graphs that link the PLF attenuation with the nominal current. An optimal PLF design technique based on global optimization and combinatorial methods is presented in [57]. And the tensorial analysis is used in [58] to obtain the mathematic formalism that computes the interactions between different circuit networks. With the help of a genetic algorithm (GA), the optimal PLF components are found. However, the last two methods share an inconvenience: both are based on a fixed PLF structure. If a more optimal structure exists, it is not considered.

As can be seen, there are several recommendations for the PLF design but not an standard methodology. Without an accurate PLF modal characterization, it is not possible to precisely predict its effect on the modal emissions and the design becomes a difficult task. Therefore, most EMC engineers usually design the PLF by trial and error [59].

1.4 Electric device and power-line network characterization

The IL of a PLF in an actual environment can only be predicted if the impedances of the DUT and the PLN, among which the PLF is connected, are known. In general, the values of these impedances will change in function of the frequency, and several methodologies for their measurement have appeared in the last 40 years. The most relevant ones are shown in the following sections.

1.4.1 Impedance measurements of an electric device

In order to measure the input impedance of a switching power supply, the resonance method was introduced [60]: considering the input impedance as capacitive, the CM and DM input impedances are estimated by connecting a resonating inductor between the device and the PLN. However, this first attempt was quite complicated and the results obtained were inaccurate due to the predominance of the parasitic effects at increasing frequencies. Later, the input

impedance of a power electronic device was analyzed in [61], which derived an equivalent model for the CM impedance. At the same time, the IL method was introduced in [62]. This method involves the placement of a known impedance either in parallel or in serial depending on the noise source impedance of the DUT. Measuring the decrement of the voltage on the known impedance, the magnitude of CM and DM input impedances of the DUT are determined. Nevertheless, the phase information can only be estimated using a complicated Hilbert transform process. Finally, the current-probe methodology was proposed in [63]–[65] to measure the CM and DM input impedances of switching power supplies. The measurement setup consists of an injecting probe, a sensing probe and some coupling capacitors. Again, this methodology only obtains the magnitude of CM and DM impedances. Besides, if the CM and DM impedances are dealt as independent impedances, the modal interaction is not considered.

1.4.2 Impedance measurements of a PLN

The PLN impedance characterization is more complex to deal with than the DUT one, not because of the measurement system, but for its variant nature in function of the place and the hour. This is the reason for what it is usually dealt with probability distributions [1], [66]–[68]. As in the DUT case, there are different techniques to measure the PLN impedance: the three voltages method was proposed in [69], where a reference impedance is connected between the PLN and a power source tuned to the desired frequency. The input impedance magnitude is found by comparing the measured voltages in both impedances (the reference and the PLN one), and the impedance phase is obtained with the construction of a vectorial diagram from the measured voltages in both impedances and the power source. The two-probe method was presented in [70], and used in [71] to measure the impedance of the PLN in the 20 kHz to 30 MHz frequency band, showing the results obtained in different places of the United States of America. These measurements were compared in [72]–[74] with similar measurements performed in Europe and extended in [75], [76] to 500 MHz. Recently, the measurement of the PLN impedance has been performed inserting a circuit characterized with its $ABCD$-parameter matrix between the PLN and a signal generator [77]. With this network, the voltage and the current present at the PLN terminals can be computed and, applying the Ohm law, the input impedance is obtained. Nevertheless, all these methodologies are only used to find the circuit impedances of the PLN and they need to be extended if the CM impedance, the DM impedance and the total amount of mode conversion produced in an unbalanced network are desired.

1.4.3 Equivalent models

If the DUT and PLN emissions and impedance are known (for instance, measured with the methodologies presented before), it can be useful to group all the information in a single model, that is, an equivalent circuit that behaves, from the EMC point of view, as its real homonym (with the same conducted emissions and impedance). Then the PLF characterization can be interconnected with the DUT and PLN models, and the interference propagation through the

different devices can be simulated or computed. In [78] the modeling methodologies are divided in two main groups, those that describe the DUT or PLN behavior with non-linear differential equations [79], [80], and those that are based on simple circuit models [81]–[84]. The models obtained with the methodologies of the first group are very exact, but the precise value of each variable for all the equations is difficult to get due to the practical complexity. In the second group either a current source, a voltage source or an ideal commutator are usually used to model the emissions, plus a passive circuit to model the impedance. The precision of these models directly depends on the precision of the measurements. However, there is a similar situation as the one presented in the PLF characterization: if the CM and DM impedances are analyzed separately, the interaction between both modes is not considered, and the models obtained do not completely reproduce the actual behavior of the DUT or PLN [85], [86]. Consequently, the prediction over the modal IL that introduces a PLF in a particular situation, even considering the real line and load impedances, will be inaccurate if mode conversion takes place.

1.5 Modal analysis

The situation presented in the previous sections can be summarized in two points:

- There is not a complete PLF modal characterization method because the CM and the DM are analyzed separately (figure 1.5). The fact that mode conversion is not considered involves less-than-optimal design techniques .

- There is not a complete DUT and PLN modal characterization either. Present-day methods analyze the CM and DM impedance separately (figure 1.5).

Therefore, the necessity of a method that completely analyzes the PLF, DUT and PLN behavior, detailing the mode conversion between CM and DM produced in their asymmetries, is justified. This analysis is the modal analysis, which deals simultaneously with both modes present in a single-phase power-line cable. In a modal model, each mode is confined to a different port, and the mode conversion between CM and DM appears explicitly in the model. Figure 1.6 shows the complete modal characterization of PLFs, DUTs and PLNs. The simulation of the interference propagation through the set DUT+PLF+PLN can be performed by connecting the ports of their equivalent models in an appropriate way (CM to CM and DM to DM). If all models are properly defined, the overall conducted emissions at the PLN terminals can be accurately predicted and used to design optimal PLFs.

1.6 Research objectives

The objectives expected to reach in this work are:

1. Development of new modal measurement techniques that allow a complete PLF, DUT and PLN characterization.

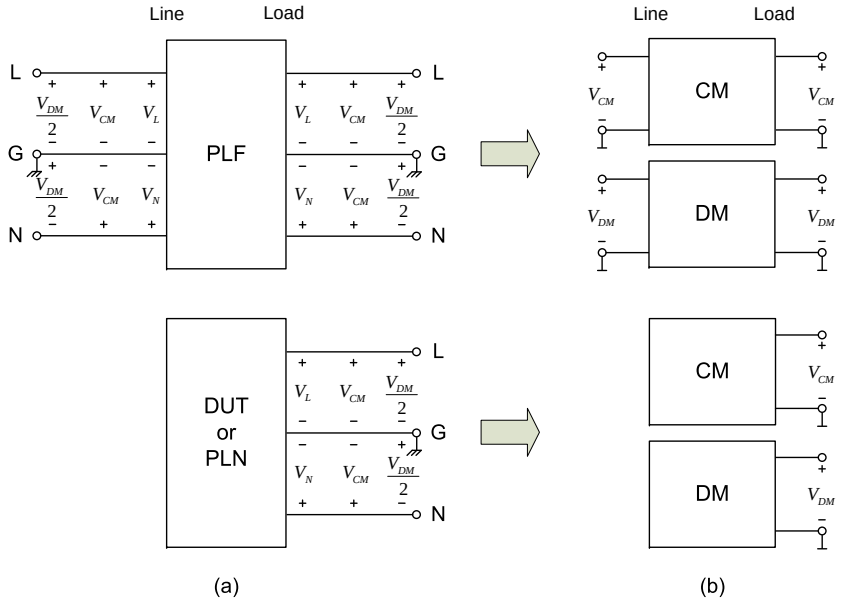

Figure 1.5: PLF, DUT and PLN traditional analysis: a) physical device; b) modal characterization.

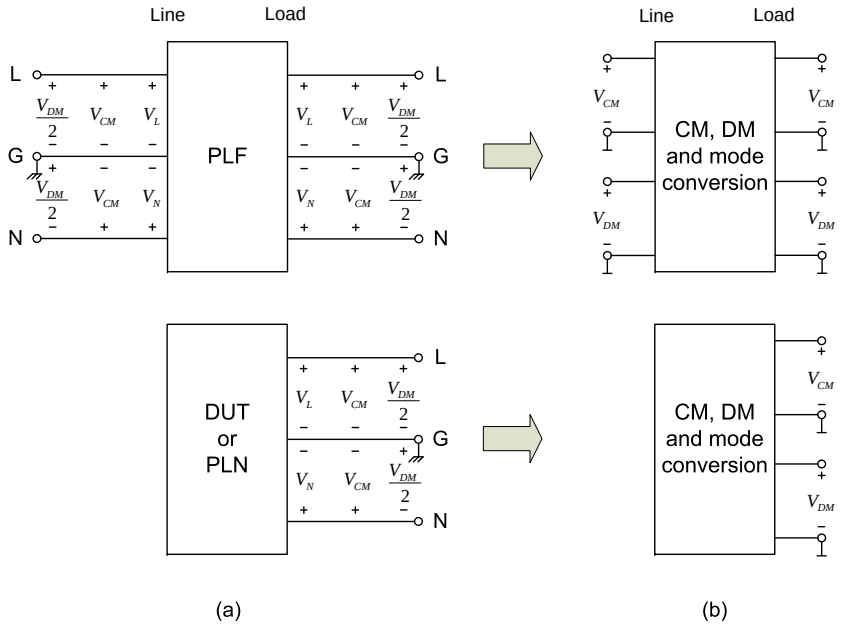

Figure 1.6: PLF, DUT and PLN modal analysis: a) physical device; b) modal characterization.

- To obtain a complete PLF characterization, as seen in figure 1.6, some new parameters named modal S parameters are proposed. These parameters are a mathematical extension of the traditional S parameters. The modal S parameters present a more general characterization that those ones based on independent CM and DM circuits, since they consider the possible spurious interference that flows from one mode to the other due to the asymmetries in the PLF design.
- To obtain a complete DUT and PLN characterization, as seen in figure 1.6, the measurement of their modal impedance is performed via S-parameter measurements, and the modal conducted emissions (either generated by the DUT, or present in the PLN) are obtained measuring the phase between the V_L and V_N voltages. The conducted emissions measurements can be obtained via frequency-domain or time-domain measurements. In this work both kind of measurements are studied and the advantages and disadvantages of each method are exposed through the characterizations of DUTs with different types of conducted emissions. In any case, once the S parameters and the conducted emissions are measured, all the information is finally grouped in a model composed by a three-impedance pi-network and two voltage sources, whose behavior, from the EMC point of view, is similar to the actual DUT or PLN.

2. Development of a new methodology to predict the conducted interference level that a DUT supplies to the PLN through a PLF. The current standards and methods do not allow the precise conducted interference prediction that a DUT connected to a PLF produces, mainly due to their incomplete characterization. From the different characterizations obtained in the first objective, the new methodology has to predict, with a high reliability, the interference level under two points of view: circuit (considering the physical signals at the L and N terminals) and modal (considering the CM and DM signals). While the circuit predictions allow the knowledge of the possible compliance according to the EMC standards, the modal point of view provides the comprehension of some events, such as the efficiency loss of the PLF or the modal power reflection due to the mismatched input impedances or asymmetries in the devices.

3. Development of new methodologies to design optimal PLFs. Two approaches have been developed for this purpose:

   - The first approach for an optimal methodology is performed via an iterative method that, using the prediction methodology and the S-parameter characterization, designs the best PLF by finding the most suitable components and its optimal structure.
   - The second approach is based on the mode conversion. The importance of a mode conversion characterization has been stressed several times in order to get accurate predictions of the conducted emissions. This mode conversion can be further ana-

lyzed to determine if it can be used to improve the filtering capabilities by being expressly generated in a PLF, for instance, unbalancing CMCs or Y-capacitor networks. To this end, two new modal models to characterize networks composed by CMCs, X and Y capacitors are presented. These models are useful to analyze the reflections and transmissions of both modes, to analyze the modal conversion and to find the best component values in order to optimize the mitigation of both CM and DM, obtaining, in some cases, asymmetric structures when $L_1 \neq L_2$ and/or $C_{Y1} \neq C_{Y2}$.

The main objective of all the methodologies presented in this work is to get optimal PLFs as regards size, volume, cost, efficiency or any other interesting parameter for a PLF or DUT manufacturer.

4. Spreading of all the research activities and results between the scientific community, through national and international, journal and symposium publications of the EMC sector.

Chapter 2

Power-Line Filter Characterization

Contents of this chapter

2.1 Introduction 15
2.2 Circuit and modal characterization of linear four-port devices . . 16
2.2.1 Circuit characterization 16
2.2.2 Modal characterization 18
2.3 Measurement system 20
2.3.1 Measurement methodology 20
2.3.2 Experimental validation 20
2.4 Extended measurement system 22
2.4.1 Measurement methodology 23
2.4.2 Experimental validation 24
Measurements on a PLF 24
Measurements on a CMC 26

2.1 Introduction

A physical power-line filter (PLF) (figure 2.1(a)) can be considered as a linear four-port device (the relationship between its currents and voltages is constant [87]) provided that the operating point is on the linear part of the response of its components. This linear four-port device can be circuitally characterized, with a model that presents circuit voltages and currents at its terminals, as shown in figure 2.1(b). From this model, it can be observed that:

- V_{IL}, I_{IL}, V_{IN}, I_{IN} are the voltages and currents present at the line (L) and neutral (N) terminals of the line side of the PLF.

- V_{OL}, I_{OL}, V_{ON}, I_{ON} are the voltages and currents present at the L and N terminals of the load side of the PLF.

The same linear four-port device can also be modally characterized, with a model that presents modal voltages and currents at its terminals, as shown in figure 2.1(c). From this model, it can be observed that:

- V_{ICM}, I_{ICM}, V_{IDM}, I_{IDM} are the voltages and currents for the CM and DM present at the line side of the PLF.

- V_{OCM}, I_{OCM}, V_{ODM}, I_{ODM} are the voltages and currents for the CM and DM present at the load side of the PLF.

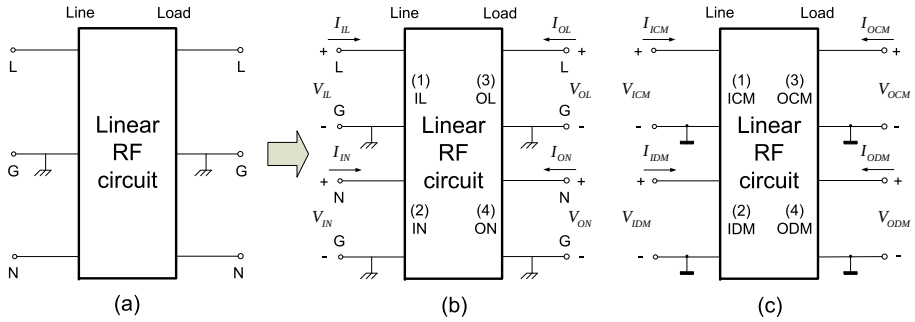

Figure 2.1: Linear RF circuit characterizations: a) physical; b) circuit; c) modal.

Since scattering (S) parameters completely characterize any linear four-port device [87], they can be used to characterize circuitally and modally the PLFs [40], [88]. This characterization methodology is presented in this chapter, which structure is as follows: in the second section the S parameters that characterize the circuit behavior of a PLF are defined, and, based on them, a new class of parameters are extracted, known as modal S parameters, that, analogously, characterize its modal behavior; in the third section the measurement setup is presented and used to validate both characterizations and to show its advantages in front of the traditional characterization techniques; finally, in the fourth section, the measurement setup is extended to characterize PLFs with high currents flowing through them and, therefore, presenting a non-linear behavior.

2.2 Circuit and modal characterization of linear four-port devices

2.2.1 Circuit characterization

In the circuit characterization the S parameters characterize the electric signals in function of its voltages and currents referred to ground (G), as seen in figure 2.2.

From the network of figure 2.2, it can be observed that:

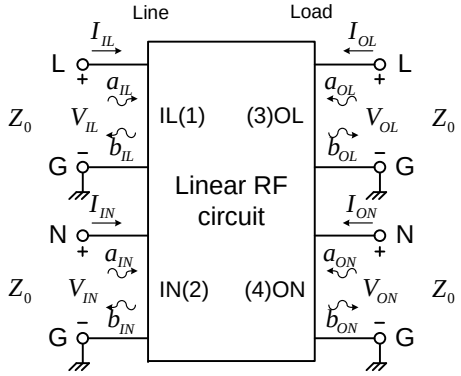

Figure 2.2: Circuit port definition in a S-parameter measurement.

- a_{IL}, b_{IL}, a_{IN}, b_{IN} are the input and output waves present at the L and N terminals of the line side of the PLF.

- a_{OL}, b_{OL}, a_{ON}, b_{ON} are the input and output waves present at the L and N terminals of the load side of the PLF.

The S parameters relate output waves (b) with input waves (a) in each PLF port [87]:

$$[b] = [S] \cdot [a] \tag{2.1}$$

with

$$[b] = \begin{bmatrix} b_{IN} \\ b_{IL} \\ b_{ON} \\ b_{OL} \end{bmatrix} \qquad [a] = \begin{bmatrix} a_{IN} \\ a_{IL} \\ a_{ON} \\ a_{OL} \end{bmatrix} \tag{2.2}$$

The relationship between a and b waves and the voltages and currents in each port is:

$$\begin{aligned} a_L &= \frac{1}{2\sqrt{Z_0}}(V_L + Z_0 I_L) \\ a_N &= \frac{1}{2\sqrt{Z_0}}(V_N + Z_0 I_N) \\ b_L &= \frac{1}{2\sqrt{Z_0}}(V_L - Z_0 I_L) \\ b_N &= \frac{1}{2\sqrt{Z_0}}(V_N - Z_0 I_N) \end{aligned} \tag{2.3}$$

where Z_0 is the reference impedance of the measurement system, normally 50 Ω. Therefore, measuring the S parameters of the PLF, the relationship between the voltages and currents at the line and load side of the PLF is obtained.

2.2.2 Modal characterization

Although the circuit characterization obtains a complete characterization, it does not provide any direct information about the common mode (CM) and differential mode (DM) attenuation and mode conversion between the CM and the DM. The modal S parameters are introduced in [89]–[93] and, instead of relating circuit waves, they relate modal waves. These new parameters model a conceptual network where on each port there is either the input or output CM, or the input or output DM (figure 2.3). In contrast to the circuit characterization, whose ports are referred to the physical G of the system, the ports of the modal model are referred to a conceptual reference point whose relation with G is irrelevant for the purposes of this work. The modal S parameters can be measured with a modified vector network analyzer (VNA) [90], [91], or can be extracted from a mathematical transformation of the circuit S parameters, as can be seen below [90]–[93].

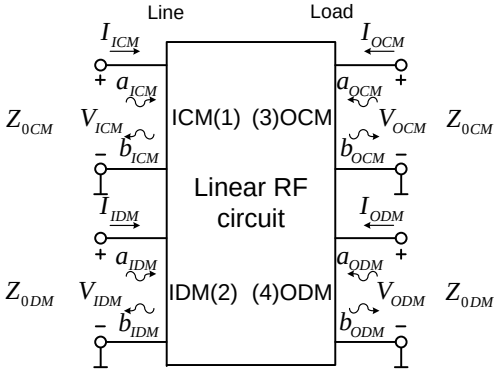

Figure 2.3: Modal port definition in a S-parameter measurement.

From the network of figure 2.3, it can be observed that:

- a_{ICM}, b_{ICM}, a_{IDM}, b_{IDM} are the input and output waves for the CM and DM present at the line side of the PLF.

- a_{OCM}, b_{OCM}, a_{ODM}, b_{ODM} are the input and output waves for the CM and DM present at the load side of the PLF.

Analogously to the circuit S parameters, the modal S parameters (S_M) relate output waves (b_M) with input waves (a_M):

$$[b_M] = [S_M] \cdot [a_M] \tag{2.4}$$

with

$$[b_M] = \begin{bmatrix} b_{ICM} \\ b_{IDM} \\ b_{OCM} \\ b_{ODM} \end{bmatrix} \qquad [a_M] = \begin{bmatrix} a_{ICM} \\ a_{IDM} \\ a_{OCM} \\ a_{ODM} \end{bmatrix} \tag{2.5}$$

The modal waves are related with the modal voltages and currents with:

$$\begin{aligned} a_{CM} &= \frac{1}{2\sqrt{Z_{0CM}}}(V_{CM} + Z_{0CM} I_{CM}) \\ a_{DM} &= \frac{1}{2\sqrt{Z_{0DM}}}(V_{DM} + Z_{0DM} I_{DM}) \\ b_{CM} &= \frac{1}{2\sqrt{Z_{0CM}}}(V_{CM} - Z_{0CM} I_{CM}) \\ b_{DM} &= \frac{1}{2\sqrt{Z_{0DM}}}(V_{DM} - Z_{0DM} I_{DM}) \end{aligned} \tag{2.6}$$

where Z_{0CM} and Z_{0DM} are the reference impedances for the CM and DM respectively.

By substituting equation (1.1) in (2.3) and (2.6), the relation between circuit waves (a_L, a_N, b_L, b_N) and modal waves (a_{CM}, a_{DM}, b_{CM}, b_{DM}) is obtained:

$$\begin{aligned} a_{CM} &= \frac{a_L + a_N}{\sqrt{2}} \\ b_{CM} &= \frac{b_L + b_N}{\sqrt{2}} \\ a_{DM} &= \frac{a_L - a_N}{\sqrt{2}} \\ b_{DM} &= \frac{b_L - b_N}{\sqrt{2}} \end{aligned} \tag{2.7}$$

And the circuit and modal reference impedances are related according to:

$$\begin{aligned} Z_{0CM} &= \frac{Z_0}{2} \\ Z_{0DM} &= 2Z_0 \end{aligned} \tag{2.8}$$

From the equation (2.7) two relations can be deduced between circuit and modal waves:

$$[a_M] = [A] \cdot [a] \tag{2.9}$$

$$[b_M] = [B] \cdot [b] \tag{2.10}$$

with

$$[A] = [B] = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & -1 \end{bmatrix} \tag{2.11}$$

By substituting the equations (2.9) and (2.10) in (2.1), and comparing the result with equation (2.4), the relationship between the modal S parameters and the circuit S parameters is obtained:

$$[S_M] = [B] \cdot [S] \cdot [A]^{-1} \tag{2.12}$$

This matrix completely describes the modal behavior of a linear circuit, and it can be extracted from the circuit S parameters measured with a classical VNA.

2.3 Measurement system

2.3.1 Measurement methodology

The S parameters of a PLF can be easily measured with a VNA, as seen in figure 2.4. N connectors have been soldered to the PLF terminals to connect the PLF to the VNA. In order to avoid external interference, the PLF can be confined in a Faraday cage (enclosure formed by conducting material).

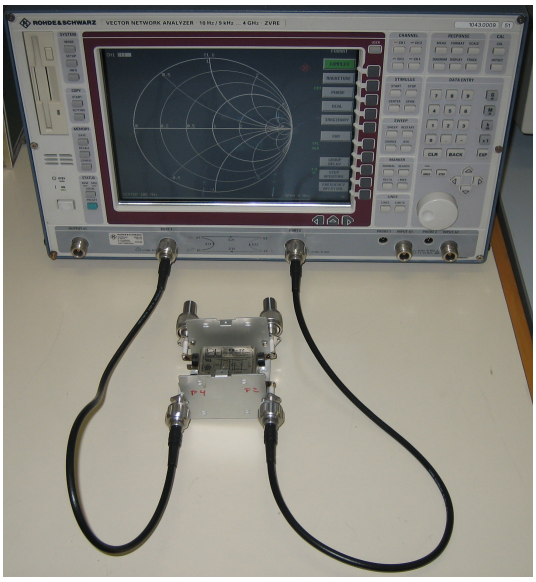

Figure 2.4: S-parameter measurement with a VNA.

2.3.2 Experimental validation

The modal S-parameter matrix, obtained with (2.12), is a complete characterization for linear PLFs, and the following information can be extracted:

- Information about the modal insertion loss (IL) in a 50-Ω measurement system (equivalent to the information provided by the standard ANSI C63.13 [21]). Figure 2.5 shows the

modulus of the CM IL and the DM IL of a PLF (Prefilter FB-2Z 2A) obtained from the modal S-parameter characterization and from the measurements performed according to the standard ANSI C63.13. Both methods present very close results.

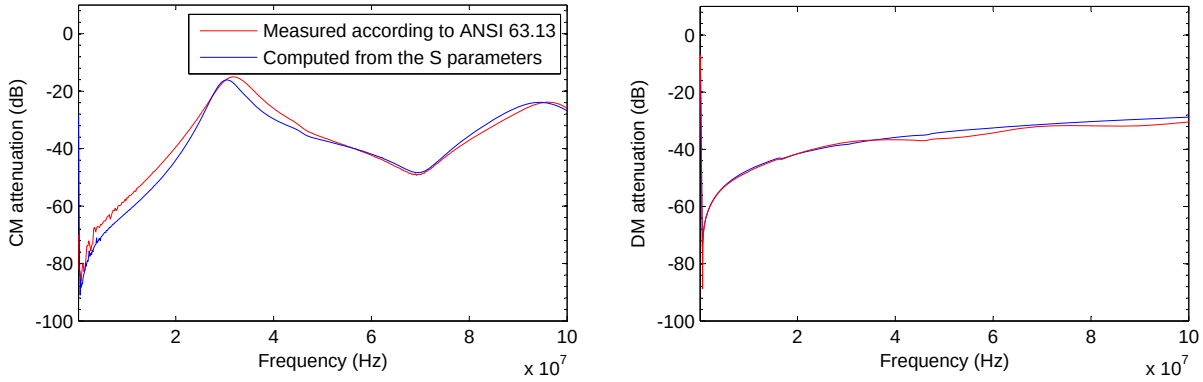

Figure 2.5: CM and DM IL of a PLF (Prefilter FB-2Z 2A), obtained from the modal S-parameter characterization and from the measurements performed according to the standard ANSI C63.13.

- Information about the modal IL for different line and load impedances. Using the S parameters to characterize the PLF allows the computation of the IL produced by any line and load impedances without having to perform any additional measurement, and the worst-case IL can be easily computed. The CM IL and the DM IL of a PLF (Belling Lee SF4110-1/01 1A) loaded with four different impedances at the load side, keeping a 50 Ω $\|$ 50 μH constant impedance at the line side (equivalent to the impedance presented by a line impedance stabilization network (LISN)) can be seen in figure 2.6. Some IL variations in function of the load impedance can be observed.

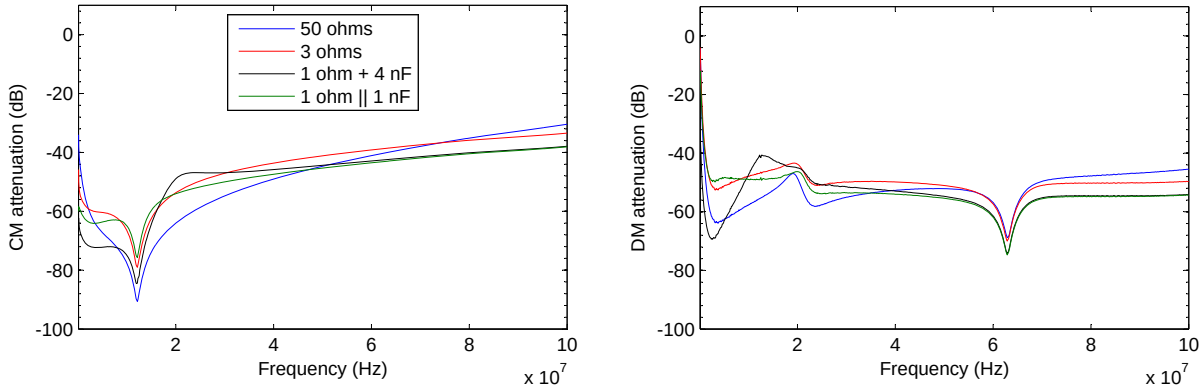

Figure 2.6: CM and DM attenuation of a PLF (Belling Lee SF4110-1/01 1A), with different load impedances.

- Information about the mode conversion between the CM and DM. The S parameters can predict the mode conversion produced between the line and load sides, and the mode

conversion produced by the reflected power in both PLF sides. Figure 2.7 shows, on the one hand, the energy transfer between the CM at the load side and CM and DM at the line side of a PLF (Belling Lee SF4110-1/01 1A). Most incident CM power at the load side is transferred to the DM power at the line side between 11 MHz and 13 MHz. On the other hand, figure 2.7 shows the energy transfer between the DM at the load side and CM and DM at the line side of the same PLF. Most incident DM power at the load side is transferred to the CM power at the line side between 3.4 MHz and 15.4 MHz, and over 20.5 MHz. This fact shows that the measurements of the CM IL and DM IL separately, as proposed by [21], are not enough to completely characterize a PLF.

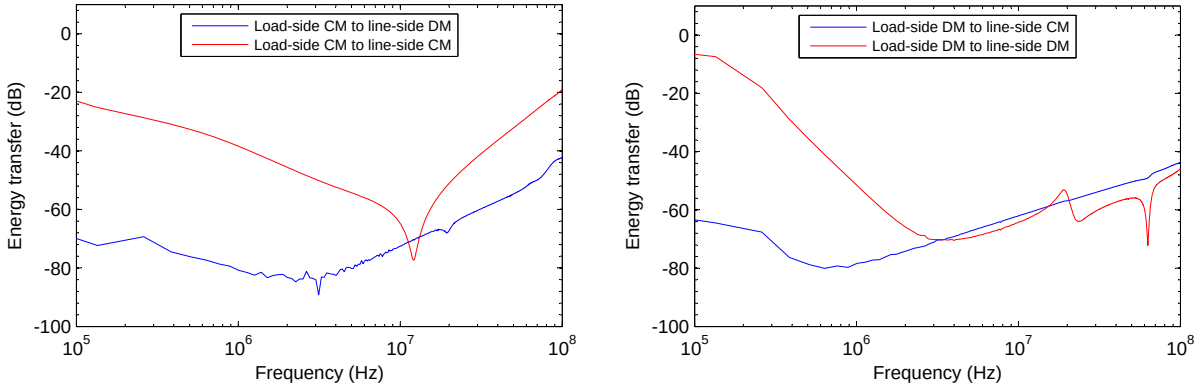

Figure 2.7: Energy transfer between the line and load sides for the PLF: Belling Lee SF4110-1/01 1A.

2.4 Extended measurement system

The linearity of a PLF, prerequisite for the S-parameter characterization, is lost when the flowing current reaches the saturation levels of the PLF. In such situation the S parameters obtained with the previous measurement system do not reflect the actual response of the PLF and, therefore, they cannot be used for an accurate characterization. In order to characterize PLFs under real performance conditions, a new characterization methodology is needed. Some efforts to find the saturation level, the IL or the impedance of the PLF at its operating point can be found in the literature: in [22] a method that distinguishes the state of a common-mode choke (CMC) connected to a device under test (DUT) by analyzing the interference in a 50-Hz signal period is presented. The CMC is saturated if the interference level oscillates with the 50-Hz signal. In [45] a current source is added in the measurement setup to inject current to the PLF through a coupling network while the IL measurement is performed. In [28] the use of two current probes to determine the IL of a PLF connected between the DUT and the PLN is suggested. And in [29] a similar technique to measure the CM impedance of a CMC is employed. However, these measurements do not provide a complete characterization of PLFs because they are only valid in the measurement system where they are obtained.

To continue using the S-parameter characterization, the S-parameter measurement system must be modified. The IEEE standard 1560-2005 [46] proposes an S-parameter measurement setup with two bias networks to inject direct current (DC) to the PLF. In this section, the measurement system of [46] is extended to characterize a PLF in a real operating conditions, that is, with the same 50-Hz current level as the one demanded by the DUT to be filtered. This characterization allows the prediction of the actual PLF effect on the conducted emissions of the DUT even when the filter is stressed by high current levels.

2.4.1 Measurement methodology

The new measurement setup proposed for the S-parameter measurement of a PLF under operating conditions is presented in figure 2.8. Instead of the bias networks proposed in [46] for DC power, two LISNs are used to couple and decouple the 50-Hz current. The PLF is placed between both LISNs ($LISN_1$ and $LISN_2$) and connected to their L_{devX} and N_{devX} respective ports (for $X = 1, 2$). A variable load connected at the L_{PL2} and N_{PL2} allows the injection of the desired current while the measurements are performed.

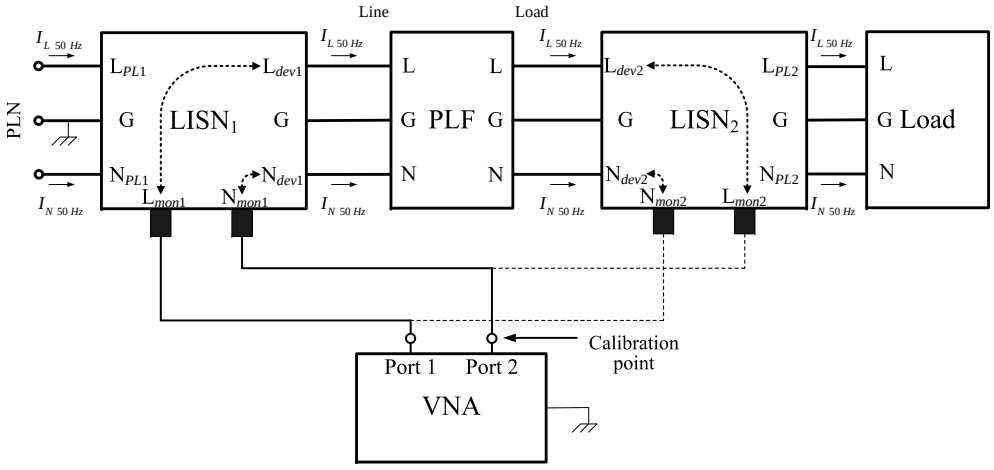

Figure 2.8: S-parameter measurement system for PLF under operating conditions.

Both LISNs can be considered as linear four-port devices because their power-line ports (L_{PLX} and N_{PLX}, for $X = 1, 2$) are largely isolated beyond the 150 kHz (the PLN impedance in $LISN_1$ and the load impedance in $LISN_2$ of figure 2.8 do not affect the measurements), as shown in figure 2.9. Therefore they can be characterized through their S parameters as it was done for a PLF.

Since the calibration point is placed between the VNA and the two LISNs, as seen in figure 2.8, the final S-parameter measurement will contain the effect of the PLF plus the two LISNs. In order to recover the S parameters of the PLF, the effect of the two LISNs can be deembedded by using the Transmission (T) parameters [94]. In a four-port device, T parameters link input and output waves (a and b respectively) between different ports as follows:

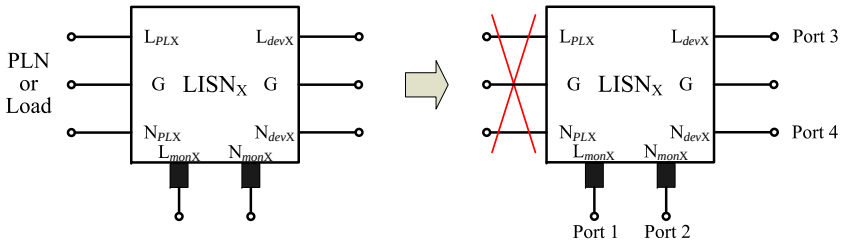

Figure 2.9: The LISN can be considered as linear four-port device when it is seen from L_{monX} and N_{monX} or L_{devX} and N_{devX} ports (for $X = 1, 2$).

$$\begin{bmatrix} b_1 \\ a_1 \\ b_2 \\ a_2 \end{bmatrix} = [T] \begin{bmatrix} a_3 \\ b_3 \\ a_4 \\ b_4 \end{bmatrix} \tag{2.13}$$

The main advantage of T parameters is that they allow the addition (or subtraction) effect of devices in cascade by multiplying (or dividing) their T parameters. S parameters can be easily converted to T parameters and vice versa with the appropriate transformation equations (see appendix). Therefore, if the S parameters of the $LISN_1$ and the $LISN_2$ and the S parameters of the system $LISN_1$+PLF+$LISN_2$ are converted to T parameters, the T parameters of the PLF can be recovered with the following equation:

$$[T_{PLF}] = [T_{LISN1}]^{-1} \times [T_{LISN1+PLF+LISN2}] \times [T_{LISN2}]^{-1} \tag{2.14}$$

Finally, the T parameters of the PLF can be converted again to S parameters, obtaining the S-parameter characterization of the PLF under operating conditions.

2.4.2 Experimental validation

Measurements on a PLF

Figure 2.10 shows the CM and DM attenuation of a PLF (Belling Lee SF4110-1/01 1A) measured: *a*) with the traditional S-parameter measurement setup (figure 2.4); and *b*) with the two-LISN measurement setup (figure 2.8) without current (in order to preserve the same biasing effect as in case *a*)). Both measurements present superposed results, which validates this new measurement setup.

In order to show an example of the efficiency loss in a PLF due to saturation, the same PLF (Belling Lee SF4110-1/01 1A) has been measured with the two-LISN measurement setup (figure 2.8) and different current levels. Figure 2.11 shows the CM and DM attenuation for current rates between 0 A and 6 A. As current increases, the effect of the PLF on both modes is progressively diminished. Beyond 5 A the PLF can be considered useless, specially due to a practically inexistent CM attenuation under 1 MHz.

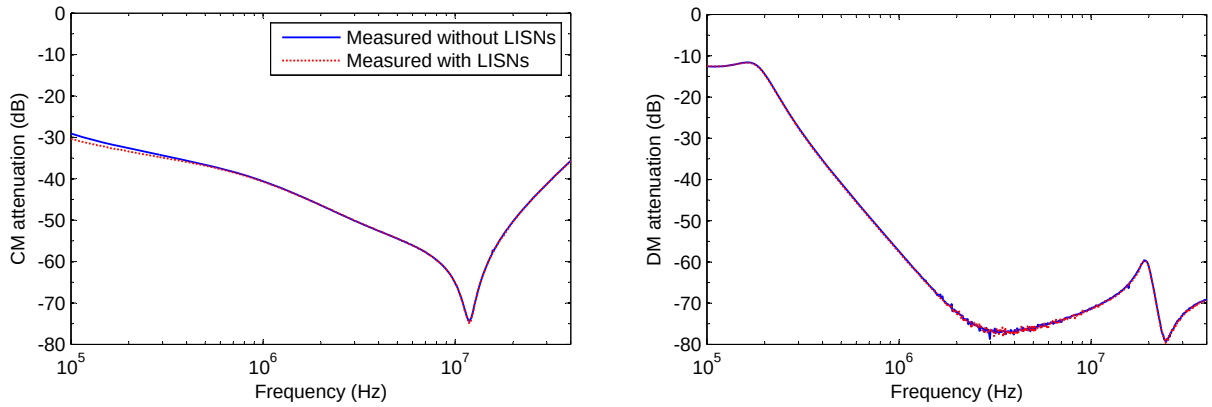

Figure 2.10: Comparison of the CM and DM attenuation for the PLF Belling Lee SF4110-1/01 1A measured with and without LISNs.

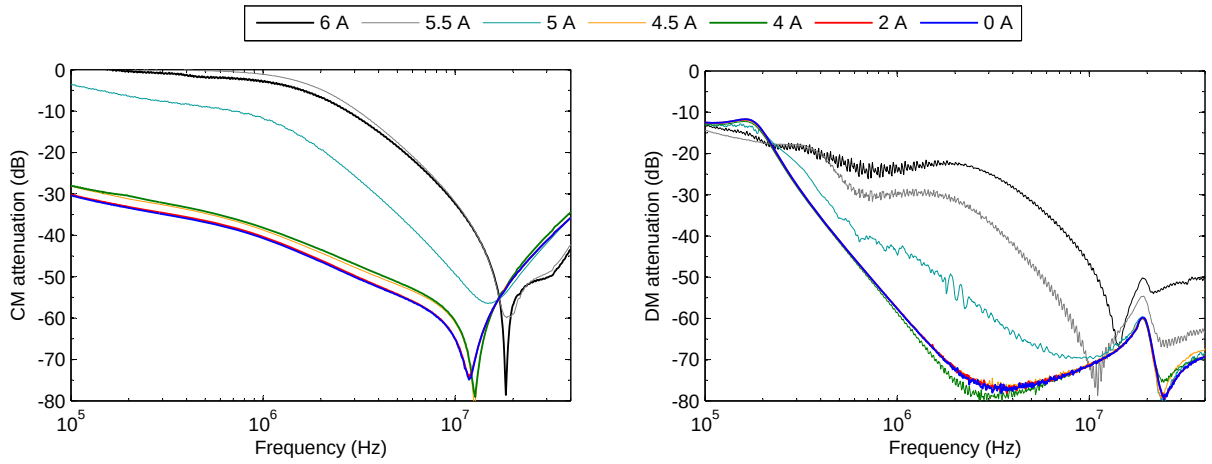

Figure 2.11: Comparison of the CM and DM attenuation for the PLF Belling Lee SF4110-1/01 1A and current rates between 0 A and 6 A.

Figure 2.12 shows the mode conversion produced between the CM at the line side and the DM at the load side, and between the DM at the line side and the CM at the load side of the PLF (Belling Lee SF4110-1/01 1A) for current rates between 0 A and 6 A. As current increases, the PLF asymmetries become more predominant. In both cases, the mode conversion increases from about -60 dB (0-4 A) to about -20 dB (5.5-6 A). Therefore, an increasing current level over the saturation point diminishes the PLF attenuation and increases the mode conversion, degrading its overall performance.

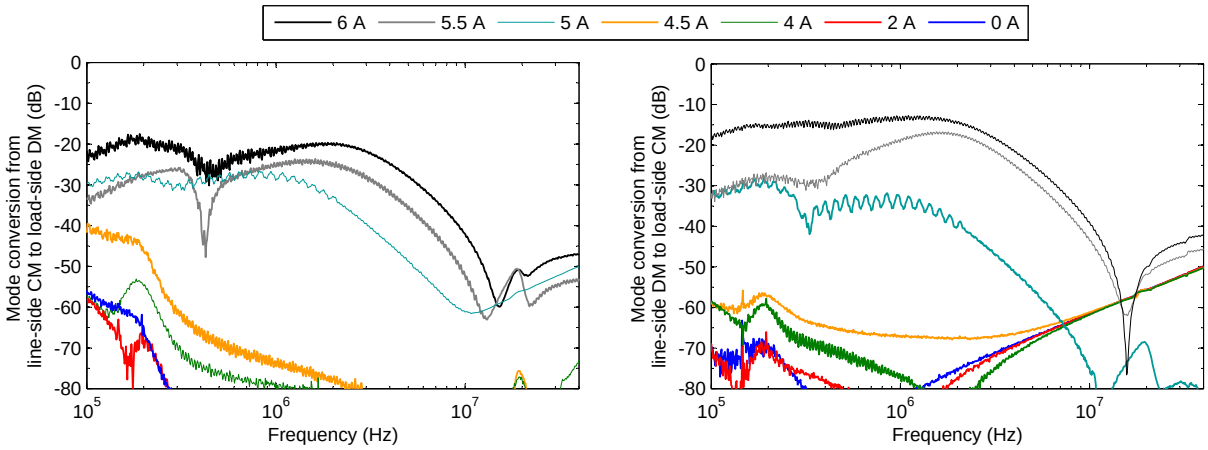

Figure 2.12: Comparison of the mode conversion between the CM at the line side and the DM at the load side and between the DM at the line side and the CM at the load side for the PLF Belling Lee SF4110-1/01 1A and current rates between 0 A and 6 A.

Measurements on a CMC

The lack of linearity in the PLF is mainly due to the CMC. This component is usually designed wounding two wires around a ferromagnetic core. In an ideal and perfectly symmetric CMC, the magnetic flux produced by the DM currents are canceled in the core and do not contribute to its saturation (figure 2.13(a)). Only high CM currents can saturate the ideal CMC (figure 2.13(b)). However, real CMCs are not perfectly symmetric (asymmetries appear during their manufacturing), and the DM flux is not totally canceled. For high current levels, the asymmetries become important and the non-canceled DM flux can saturate the CMC core. Saturating the core implies the reduction of its permeability, or, in other words, the reduction of the inductance and coupling inductance of the CMC [9], [21].

In order to show this effect, the S parameters of a 2-mH CMC with different current levels have been measured. The CM and DM attenuation can be seen in figure 2.14. An ideal CMC should not attenuate the DM, but low flux leakages (fluxes that do not go through the core and, consequently, are not coupled to the opposite inductance) cause a low DM filtering equivalent to the one produced by a small inductance. This effect can be noticed in the high frequencies of the DM attenuation shown in figure 2.14 [9], [22]. As in the PLF case, between 4 and 5

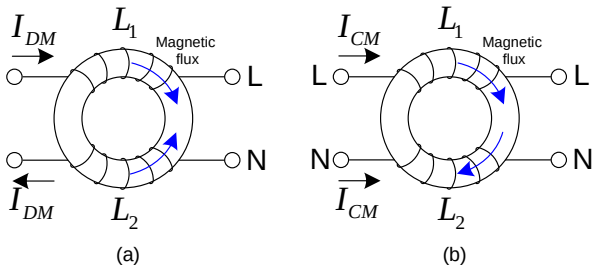

Figure 2.13: Magnetic flux direction in the ferromagnetic core due to DM currents (a) and CM currents (b).

A, the core is saturated, and the CM and DM attenuations are drastically reduced due to a decrement of the inductance value.

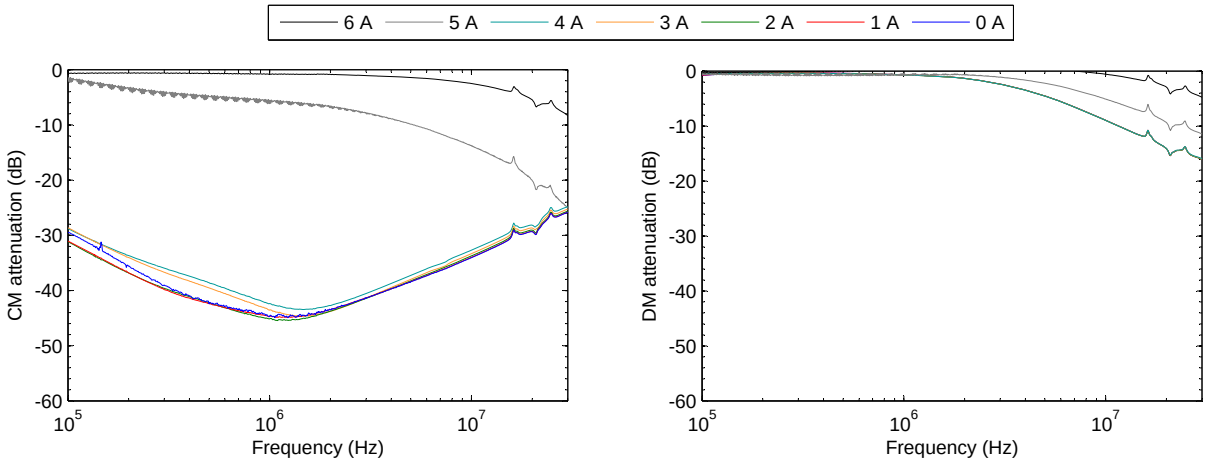

Figure 2.14: CM and DM attenuation comparison of a 2-mH CMC with different current levels.

The mode conversion between the CM at the line side and the DM at load side and between the DM at the line side and the CM at the load side produced in the CMC is presented in figure 2.15. As can be seen, the mode conversion is noticeably high when the CMC is strongly saturated (5-6 A). Since the asymmetry of the CMC is a parameter whose value depends on its physical structure, keeps constant for any current level. For high inductance values, small asymmetries can be neglected. However, as the core becomes saturated and the CMC inductance decreases, the network becomes progressively more unbalanced, and, consequently, the mode conversion increases [42].

To summarize, two examples of strongly saturated devices (the Belling Lee SF4110-1/01 1A PLF and the 2-mH CMC) have been shown. In general, PLFs and CMCs are not used in such stressed conditions, but in most applications they are designed to work near saturation (due to weight, size and economic scaling factors). Therefore, this measurement methodology can be useful to measure the modal S parameters of biased CMCs due to the current level in their coils, and to predict the actual effect of the PLF on the conducted emissions of a DUT.

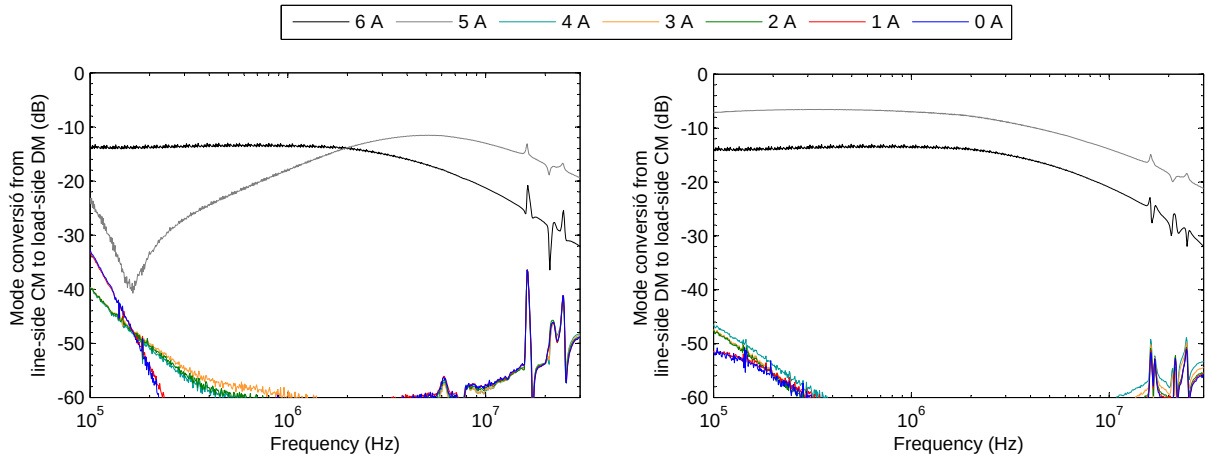

Figure 2.15: Mode conversion comparison between the line side CM and the load side DM and between the line side DM and the load side CM produced in a 2-mH CMC with different current levels.

Chapter 3

Electric Devices and Power-Line Network Characterization

Contents of this chapter

3.1 Introduction 30

3.2 Circuit and modal characterization of electric devices and power-line networks 30

3.2.1 Circuit characterization 31

3.2.2 Modal characterization 32

3.3 Measurement system for electric devices 34

3.3.1 Measurement methodology 34

3.3.2 Experimental validation 36

Test device 36

Circuit validation 37

Modal validation 40

3.4 Measurement system for power-line networks 41

3.4.1 Measurement methodology 41

3.4.2 Experimental validation 43

Test network 43

Circuit validation 44

Modal validation 44

3.5 Measurements on real devices and networks 48

3.5.1 Example of real electric device measurement 48

3.5.2 Example of a real power-line network measurement 49

3.1 Introduction

An electric device, or device under test (DUT), and a power-line network (PLN) behave in a similar way from the Electromagnetic Compatibility (EMC) point of view: from their power-line terminals both offer an impedance and conducted emissions, either due to its own interference generation, as in the DUT case, or due to the radiated coupling and conducted propagation, as in the PLN case. Therefore, both can be modeled using the same characterization methodology. However, the present measurement methods of DUTs [60]–[65] and PLNs [66]–[77] do not offer information either about the interaction between the common mode (CM) and the differential mode (DM), or about the conducted interference levels that they inject to an arbitrary load.

In this chapter, a complete characterization of DUTs and PLNs and their measurement systems are presented and tested. Their circuit behavior is modeled via a circuit model, which considers the circuit impedances between the PLN terminals and the circuit interference. Their modal behavior is modeled via a modal model, which considers the CM and DM impedances, the modal interference and the mode conversion between the CM and the DM, improving other separate CM and DM characterizations. Both models, along with the circuit and modal models of power-line filters (PLFs), can be used, for instance, to accurately predict the circuit and modal conducted emissions generated by a DUT with a PLF connected to the PLN or to a line impedance stabilization network (LISN).

In order to establish the foundations of the work presented in this chapter, the second section presents the circuit model and the modal model for the characterization of DUTs and PLNs. The measurement setup for DUTs is presented and validated in the third section, and the measurement setup for PLNs is presented and validated in the fourth one. Finally, measurements of real DUTs and PLNs are shown in the fifth section.

3.2 Circuit and modal characterization of electric devices and power-line networks

The three-terminal network of figure 3.1(a), that encloses a DUT or a PLN, can be seen as a two-port network if the current entering from one terminal of a port (line (L) or neutral (N)) is identical to the current leaving from the other terminal of the same port (ground (G)) [95]. Assuming this property, figure 3.1(b) shows the circuit two-port network that models the circuit behavior of a DUT or a PLN, with circuit voltages and currents in its terminals, and figure 3.1(c) shows the modal two-port network that models the modal behavior of a DUT or a PLN, with modal voltages and currents in its terminals.

Since the two-port networks of figure 3.1 contain inner noise sources, they can be represented by an equivalent circuit composed by a noise-free two-port network with two noise voltage serial-connected sources of inner zero impedance (Thévenin equivalent network) or two noise current shunt-connected sources of inner infinite impedance (Norton equivalent network) [81].

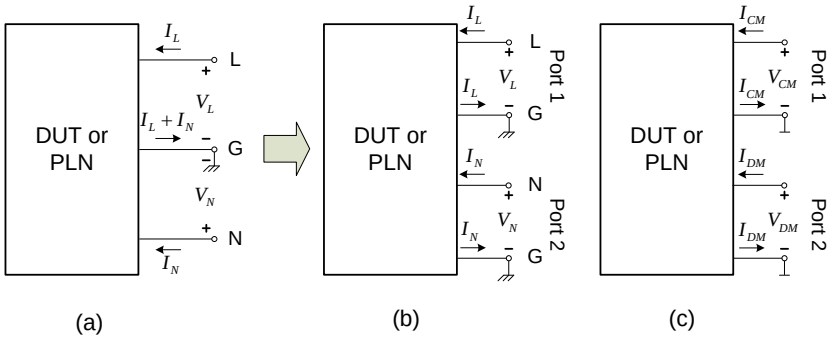

Figure 3.1: DUT and PLN characterization: a) physical; b) circuit; c) modal.

3.2.1 Circuit characterization

The two-port network with two noise voltage sources model has been selected to characterize the circuit behavior of DUTs and PLNs. Considering the DUTs and PLNs as reciprocal networks [95], their inner impedance can be modeled with a three-impedance pi-network, obtaining the model of figure 3.2. This circuit completely characterizes the DUT and PLN behavior, and it has been chosen for its simplicity of interpretation: Z_L is the L impedance, Z_N is the N impedance, Z_T is the transimpedance, and V_{nL} and V_{nN} generate the conducted interference present at the L and N terminals [96]–[100].

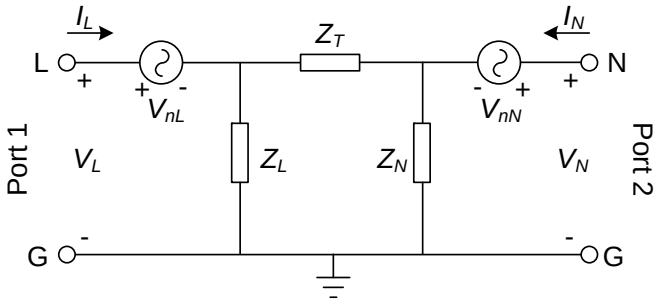

Figure 3.2: DUT and PLN circuit model.

The values of the impedances Z_L, Z_N and Z_T of figure 3.2 are computed from the measurement of the scattering (S) parameters (port 1 is the L-G port and port 2 is the N-G one):

$$\begin{aligned} Z_L &= \frac{Z_0(1+S_{11})(1+S_{22}) - Z_0 S_{12} S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21} - 2S_{21}} \\ Z_N &= \frac{Z_0(1+S_{11})(1+S_{22}) - Z_0 S_{12} S_{21}}{(1+S_{11})(1-S_{22}) + S_{12}S_{21} - 2S_{21}} \\ Z_T &= \frac{Z_0(1+S_{11})(1+S_{22}) - Z_0 S_{12} S_{21}}{2S_{21}} \end{aligned} \tag{3.1}$$

where Z_0 is the reference impedance of the measurement system.

To obtain the values of the two voltage sources V_{nL} and V_{nN}, the circuit model of figure 3.2 has to be analyzed. Applying the Kirchoff laws to this circuit the following relations are obtained:

$$\begin{aligned} I_L &= \frac{V_L - V_{nl}}{Z_L} + \frac{V_L - V_{nl} - V_N + V_{nN}}{Z_T} \\ I_N &= \frac{V_N - V_{nN}}{Z_N} + \frac{V_N - V_{nN} - V_L + V_{nl}}{Z_T} \end{aligned} \tag{3.2}$$

And the values of V_{nL} and V_{nN} are finally obtained with:

$$\begin{aligned} V_{nl} &= V_L - \frac{Z_L(Z_N + Z_T)I_L + Z_L Z_N I_N}{Z_L + Z_N + Z_T} \\ V_{nN} &= V_N - \frac{Z_N(Z_L + Z_T)I_N + Z_L Z_N I_L}{Z_L + Z_N + Z_T} \end{aligned} \tag{3.3}$$

3.2.2 Modal characterization

The circuit model allows the characterization of a DUT or a PLN, but it gives no clue as to its behavior as a CM and DM conducted interference generator. A model in terms of CM and DM impedances and sources of interference is more interesting in order to analyze its behavior, since the analysis from a modal point of view allows a better interpretation of the interference generation and propagation phenomena. This modal model can be seen in figure 3.3, and consists of a three-impedance pi-network (Z_{CM} is the CM impedance, Z_{DM} is the DM impedance and Z_{TM} is the modal transimpedance which accounts for interactions between the CM and DM) and two voltage sources (V_{nCM} and V_{nDM}) which model the generation of CM and DM conducted interference respectively [99], [100].

The parameters of the modal model of figure 3.3 can be derived from the existing relationship between the circuit voltages and currents (V_L, I_L, V_N, I_N) and the modal ones (V_{CM}, I_{CM}, V_{DM}, I_{DM}). By combining (1.1) and (3.3) the modal currents I_{CM} and I_{DM} are obtained:

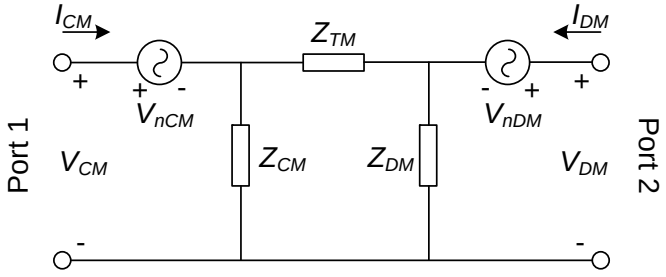

Figure 3.3: DUT and PLN modal model.

$$\begin{aligned} I_{CM} &= \left(\frac{1}{Z_L}+\frac{1}{Z_N}\right)V_{CM}+\left(\frac{1}{2Z_L}-\frac{1}{2Z_N}\right)V_{DM}-\frac{V_{nL}}{Z_L}-\frac{V_{nN}}{Z_N} \\ I_{DM} &= \left(\frac{1}{2Z_L}-\frac{1}{2Z_N}\right)V_{CM}+\left(\frac{1}{4Z_L}+\frac{1}{4Z_N}+\frac{1}{Z_T}\right)V_{DM}- \\ &\quad -\left(\frac{1}{2Z_L}+\frac{1}{Z_T}\right)V_{nL}+\left(\frac{1}{2Z_N}+\frac{1}{Z_T}\right)V_{nN} \end{aligned} \tag{3.4}$$

By analyzing the circuit of figure 3.3, the following equations are obtained:

$$\begin{aligned} I_{CM} &= \left(\frac{1}{Z_{CM}}+\frac{1}{Z_{TM}}\right)V_{CM}-\frac{1}{Z_{TM}}V_{DM}- \\ &\quad -\left(\frac{1}{Z_{CM}}+\frac{1}{Z_{TM}}\right)V_{nCM}+\frac{1}{Z_{TM}}V_{nDM} \\ I_{DM} &= -\frac{1}{Z_{TM}}V_{CM}+\left(\frac{1}{Z_{DM}}+\frac{1}{Z_{TM}}\right)V_{DM}+ \\ &\quad +\frac{1}{Z_{TM}}V_{nCM}-\left(\frac{1}{Z_{DM}}+\frac{1}{Z_{TM}}\right)V_{nDM} \end{aligned} \tag{3.5}$$

By comparing (3.4) and (3.5), the values of Z_{CM}, Z_{DM}, Z_{TM}, V_{nCM} and V_{nDM} are derived:

$$\begin{aligned} Z_{CM} &= \frac{2Z_LZ_N}{Z_L+3Z_N} \\ Z_{DM} &= \frac{4Z_LZ_NZ_T}{4Z_LZ_N+3Z_NZ_T-Z_LZ_T} \\ Z_{TM} &= \frac{2Z_LZ_N}{Z_L-Z_N} \end{aligned} \tag{3.6}$$

$$\begin{aligned} V_{nCM} &= \frac{V_{nL}+V_{nN}}{2} \\ V_{nDM} &= V_{nL}-V_{nN} \end{aligned} \tag{3.7}$$

As can be seen from (3.6), when the DUT or the PLN are unbalanced ($Z_L \neq Z_N$), the modal transimpedance Z_{TM} takes a finite value, causing an energy transfer between CM and DM. This fact shows that the CM and DM impedances (Z_{CM} and Z_{DM}) are not enough to model the behavior of a DUT or a PLN concerning CM and DM generation and behavior: it

cannot be modeled as two isolated generators (one for the CM with source impedance Z_{CM} and another one for the DM with source impedance Z_{DM}), but has to be considered as the more complex circuit of figure 3.3. Therefore, the characterization described earlier improves on previous ones that consider the CM and DM behavior of a DUT or a PLN as isolated phenomena [60]–[84]. Although it is not obvious from the circuit of figure 3.3, V_{nCM} and V_{nDM} have the same form as the definitions of voltages for the CM and DM of (1.1). This fact shows that the only source of energy exchange between CM and DM at any DUT or PLN is the modal transimpedance Z_{TM}.

3.3 Measurement system for electric devices

3.3.1 Measurement methodology

The methodology to find the circuit and modal models of a DUT (figures 3.2 and 3.3) consists of three steps:

1. Measurement of the S parameters of the DUT at its L and N ports. The measurement setup is mainly composed by a vector network analyzer (VNA) and a LISN (with its transient suppressors), as seen in figure 3.4. To compensate the effects of the LISN, the transient suppressors and the cables, the system is calibrated at the LISN-DUT interface using the standard calibration method through-open-short-match (TOSM) for VNAs, [101]. To obtain a correct S-parameter measurement, the power of the interference generated by the DUT has to be negligible in front of the power delivered by the VNA. The LISN presents a high isolation between the PLN ports (L_{PL} and N_{PL}) and the rest of the ports at the conducted emission range, so the effect of the PLN impedance is negligible in the measurement. In front of possible high interference levels and/or calibration problems, the S-parameter measurement setup can be optimized with the methodologies presented in [102]–[104]. Once the S parameters are measured, the impedances Z_L, Z_N and Z_T can be obtained with (3.1).

2. Measurement of the voltages and currents V_L, I_L, V_N and I_N of the DUT at its L and N ports. The measurement setup is mainly composed by a vector spectrum analyzer (VSA) and a LISN (with its transient suppressors), as seen in figure 3.5. The VSA allows the measurement of the conducted emissions at the two ports simultaneously and recover the relative phase of both voltages, so that the modal conducted emissions can be easily computed with (1.1) without the necessity of an external signal combinator [13]–[20].

   Since the conducted emissions are measured at the terminal ports of the VSA (V_{BL} and V_{BN} voltages), the effect introduced by the LISN, transient suppressors and cables has to be subtracted in order to recover the V_L and V_N voltages. The equivalent circuit of the measurement system is shown in figure 3.6, where high isolation on the PLN ports

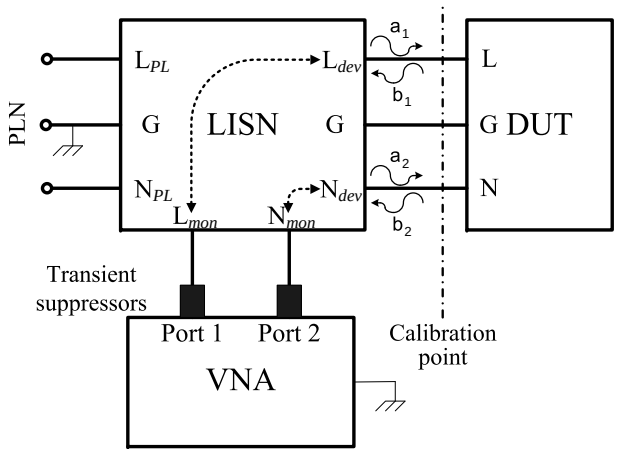

Figure 3.4: Block diagram of the S-parameter measurement setup of a DUT.

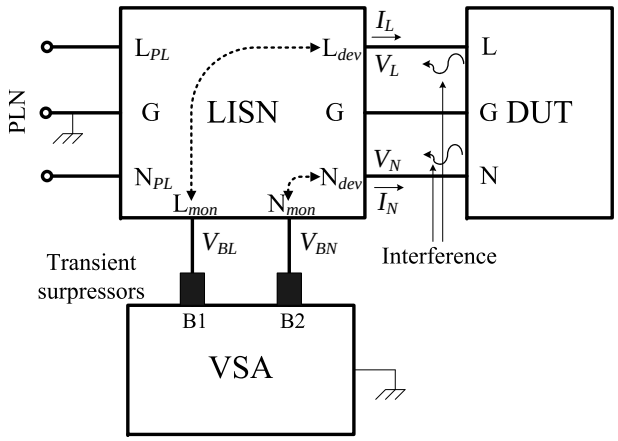

Figure 3.5: Block diagram of the voltages and currents measurement setup at the DUT terminals.

(L_{PL} and N_{PL}) has been considered and the effect of the LISN, transient suppressors and cables are represented through their S-parameter matrix $[S]$.

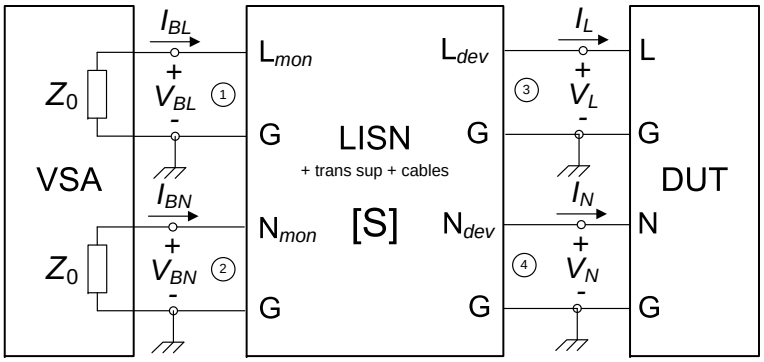

Figure 3.6: Equivalent circuit of the measurement system.

By analyzing the circuit of figure 3.6, the V_L and V_N voltages are obtained with:

$$\begin{aligned}
V_L &= V_{BL}\left(\frac{S_{24}(1+S_{33})-S_{23}S_{34}}{S_{13}S_{24}-S_{23}S_{14}}\right) - V_{BN}\left(\frac{S_{14}(1+S_{33})-S_{13}S_{34}}{S_{13}S_{24}-S_{23}S_{14}}\right) \\
V_N &= V_{BN}\left(\frac{S_{13}(1+S_{44})-S_{14}S_{43}}{S_{13}S_{24}-S_{23}S_{14}}\right) - V_{BL}\left(\frac{S_{23}(1+S_{44})-S_{24}S_{43}}{S_{13}S_{24}-S_{23}S_{14}}\right) \\
I_L &= -\frac{V_{BL}}{Z_0}\left(\frac{S_{24}(1-S_{33})+S_{23}S_{34}}{S_{13}S_{24}-S_{23}S_{14}}\right) + \frac{V_{BN}}{Z_0}\left(\frac{S_{14}(1-S_{33})+S_{13}S_{34}}{S_{13}S_{24}-S_{23}S_{14}}\right) \\
I_N &= -\frac{V_{BN}}{Z_0}\left(\frac{S_{13}(1-S_{44})+S_{14}S_{43}}{S_{13}S_{24}-S_{23}S_{14}}\right) + \frac{V_{BL}}{Z_0}\left(\frac{S_{23}(1-S_{44})+S_{24}S_{43}}{S_{13}S_{24}-S_{23}S_{14}}\right)
\end{aligned} \tag{3.8}$$

where Z_0 is the reference impedance for the measurement system (an the VSA input impedance). Once the V_L and V_N are computed, the interference voltage sources (V_{nL} and V_{nN}) can be obtained using (3.3).

3. Finally, having found all the component values of the circuit model (Z_L, Z_N, Z_T, V_{nL} and V_{nN}), the component values of the modal model (Z_{CM}, Z_{DM}, Z_{TM}, V_{nCM} and V_{nDM}) are computed using (3.6) and (3.7).

3.3.2 Experimental validation

Test device

In order to validate the measurement method proposed before, a test device that simulates a real DUT from the EMC point of view has been implemented. The test device consists of a three-impedance pi-network and two signal generators, as seen in figure 3.7. This circuit is similar to the circuit model of figure 3.2, but the voltage sources are placed in a different position due to instrumental limitations (a common reference is needed). However, the test

device components and the circuit model ones are related by applying the Kirchoff laws [97]:

$$\begin{aligned} Z_L &= Z'_L \\ Z_N &= Z'_N \\ Z_T &= Z'_T \end{aligned} \tag{3.9}$$

$$\begin{aligned} V_{nL} &= \frac{(Z_N + Z_T)V'_{nL} + Z_L V'_{nN}}{Z_L + Z_N + Z_T} \\ V_{nN} &= \frac{(Z_L + Z_T)V'_{nN} + Z_N V'_{nL}}{Z_L + Z_N + Z_T} \end{aligned} \tag{3.10}$$

Since the internal structure of the test device regarding to impedances and emissions is known, it can be compared with the component values obtained with the measurement method. For this measurement the voltage sources V'_{nL} and V'_{nN} have been implemented using a radio frequency (RF) generator with two outputs of equal amplitude (97 dBμV) and a phase shift of 53^o between them in all the frequency band from 50 kHz to 35 MHz. The 50-Ω inner impedances of the RF generator (Z'_{gL} and Z'_{gN}) have been included in the impedances Z'_L and Z'_N of the circuit.

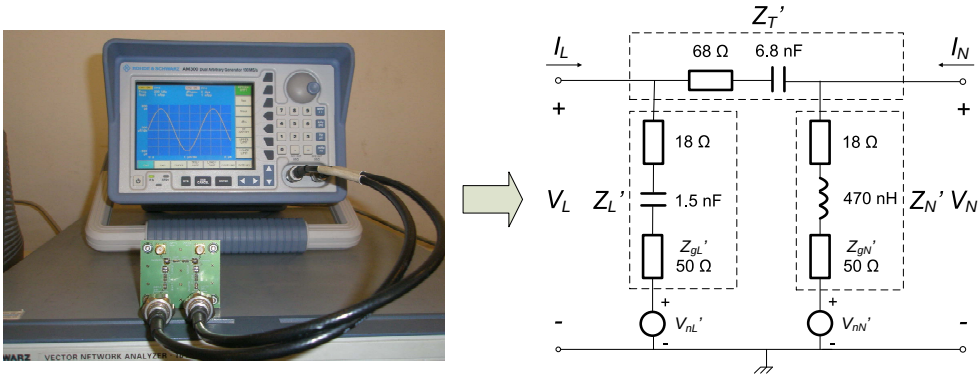

Figure 3.7: Image and circuit of the test device.

Circuit validation

Figure 3.8 shows the comparison between the physical impedances of the test device measured individually (that is, one by one), and the impedances of the circuit model Z_L, Z_N and Z_T obtained from the S-parameter measurement after applying (3.1), for the frequency band from 50 kHz to 35 MHz.

Figure 3.9 shows the comparison between the interference sources V_{nL} and V_{nN} obtained from the physical voltage sources (V'_{nL} and V'_{nN}) after applying (3.10) and the ones obtained from the conducted emissions measurement after applying (3.3), for the frequency band from 50 kHz to 35 MHz.

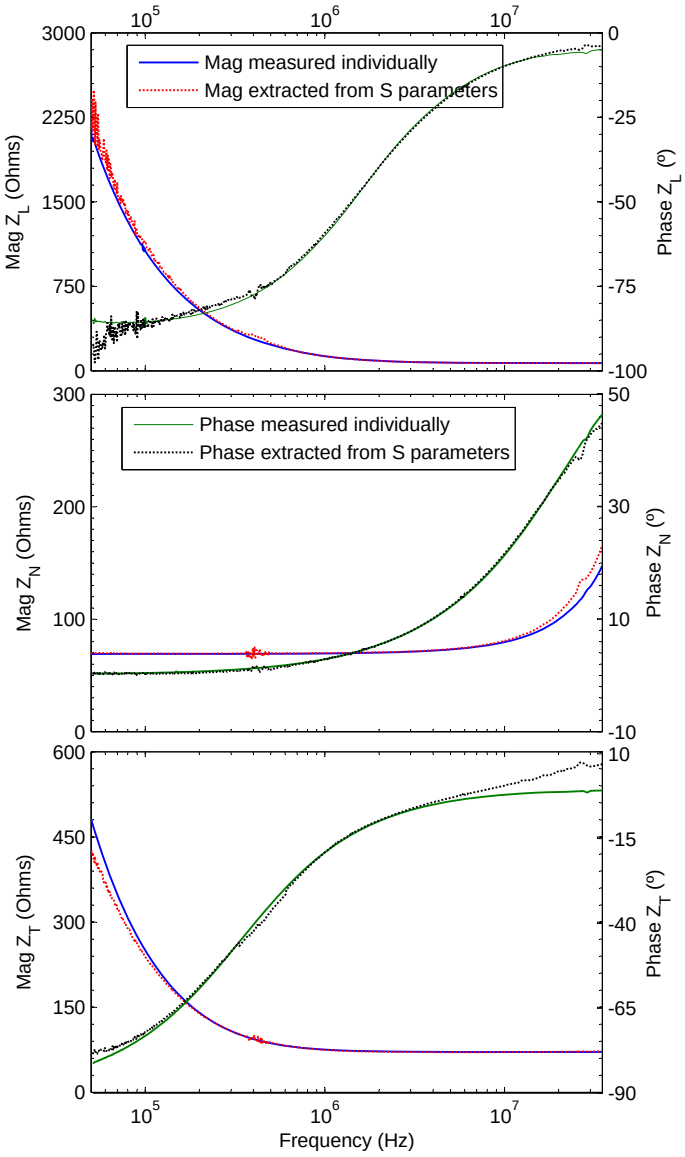

Figure 3.8: Comparison between the physical impedances of the test device measured individually and the impedances of the circuit model obtained from the S-parameter measurement after applying (3.1).

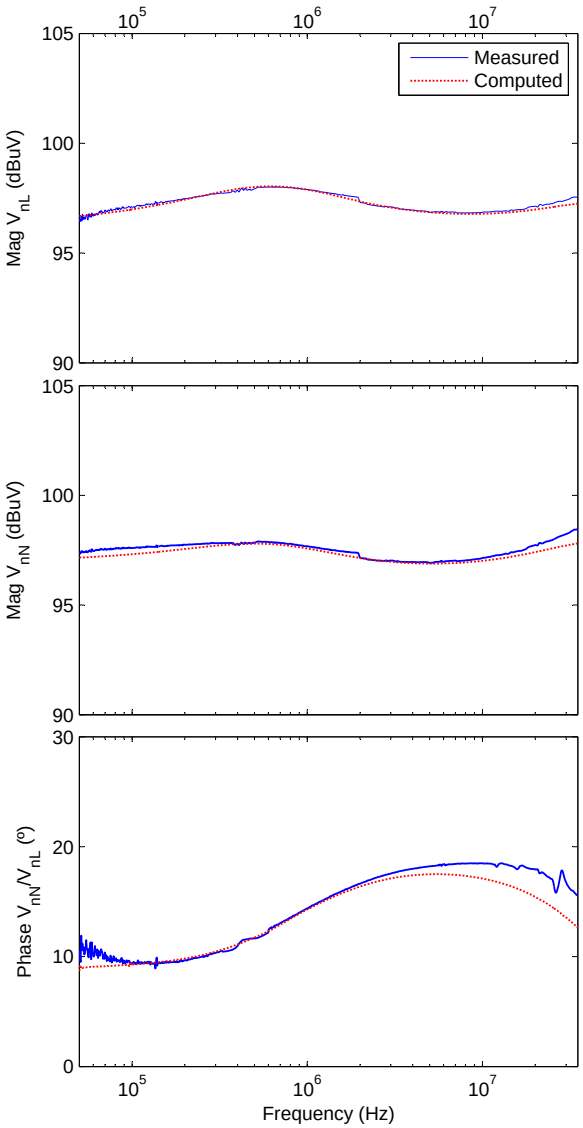

Figure 3.9: Comparison of the interference sources obtained from the values of V'_{nL} and V'_{nN} after applying (3.10) and the ones obtained from the conducted emissions measurement after applying (3.3).

Modal validation

To validate the modal model, the impedances and voltage sources of the test device, obtained from its physical components and from the measurement methodology presented before, are modally modeled with (3.6) and (3.7). Since both receive the same transformation equations, if the circuit characterization was correct, also should be the modal one.

Figure 3.10 shows the comparison between the modal impedances Z_{CM}, Z_{DM} and Z_{TM} acquired after applying (3.6) to the physical impedances measured individually and the impedances of the circuit model obtained from the S-parameter measurement.

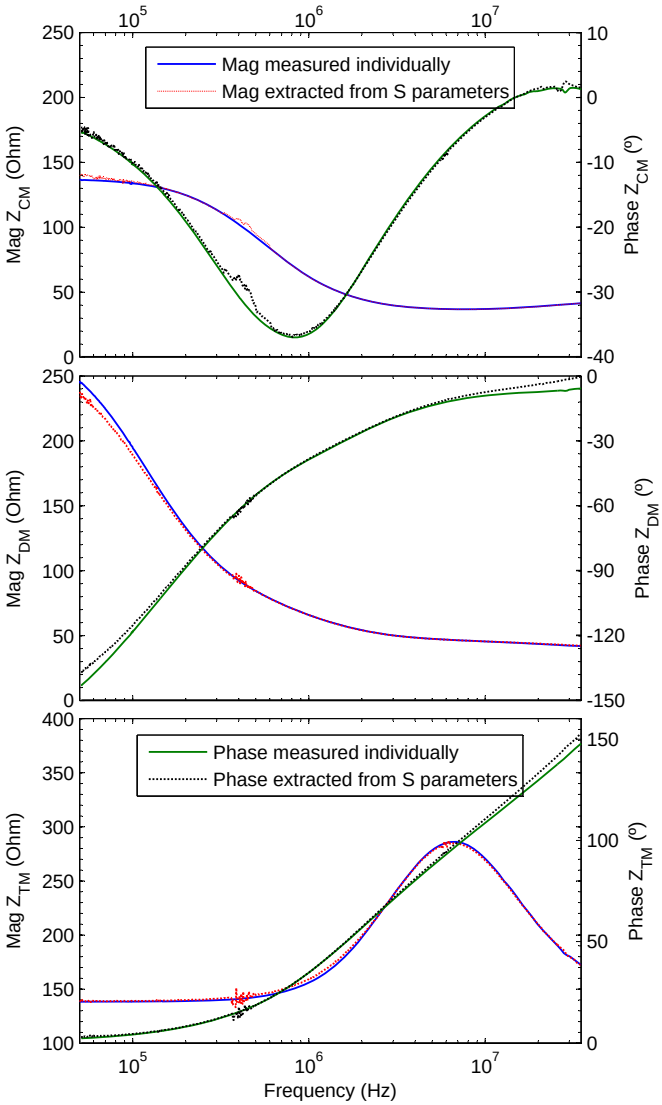

Figure 3.10: Comparison of the modal impedances obtained after applying (3.6) to the physical impedances measured individually and the impedances of the circuit model obtained from the S-parameter measurement.

Figure 3.11 shows the comparison between the modal interference sources (V_{nCM} and V_{nDM})

obtained after applying (3.7) to the physical voltage sources mathematically converted with (3.10), and to the interference sources of the circuit model, for the frequency band from 50 kHz to 35 MHz.

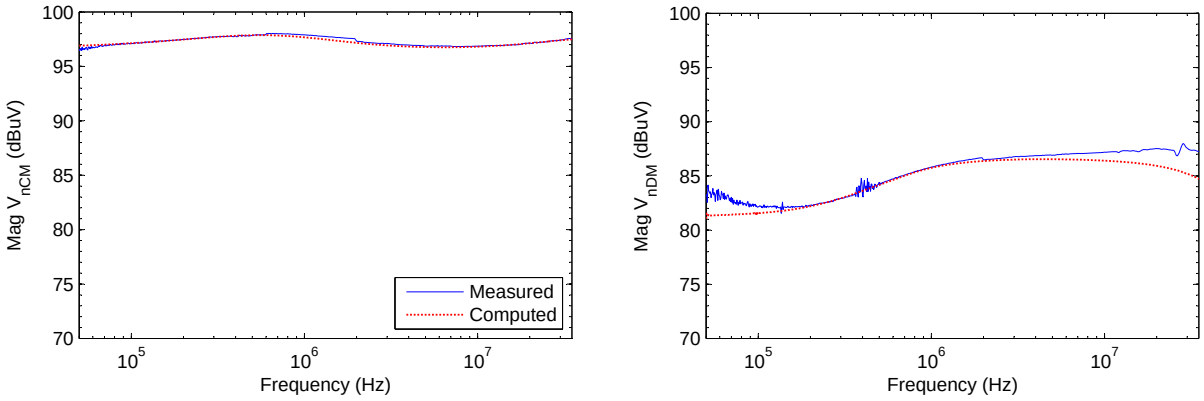

Figure 3.11: Comparison of the modal interference sources obtained from the physical voltage sources mathematically converted with (3.10), and from the interference sources of the circuit model.

The good agreement shown in both characterizations (circuit and modal) validates the models presented, and also validates the measurement system. However, the reader should be alerted that the characterization obtained is associated to the operating condition of the DUT when the measurement is performed. Some DUTs may vary their conducted emissions depending on its operation. As an example, power-electronic converters present different shapes of the conducted-emission spectrum in function of the loading conditions. This fact must be considered when such devices are characterized with this methodology.

3.4 Measurement system for power-line networks

3.4.1 Measurement methodology

The methodology to obtain the circuit and modal models of a PLN consists of the same three steps as the ones in the DUT measurement methodology case, but with a different measurement setup. Instead of using a LISN, two coupling networks (CN) are used to *a*) couple the RF signals between the analyzers (VNA/VSA) and the L and N ports of the PLN, and *b*) to protect the analyzers from the PLN mains voltage (50/60 Hz). The two CNs used are resistor-capacitor (RC) high-pass filters (HPF) implemented with a 1-kΩ resistor and a 100-nF capacitor (figure 3.12). The value of the components of the HPF have been chosen in order to find the best ratio between the band-pass attenuation ($\geq$ 50 kHz in this case) and the notch-pass attenuation (50/60 Hz). The value of the components is also restricted by the maximum G leakage current permitted by the earth leakage protection. The two CNs have been implemented in two independent shielded metallic boxes connected to G to minimize the possible coupling between both measurement channels.

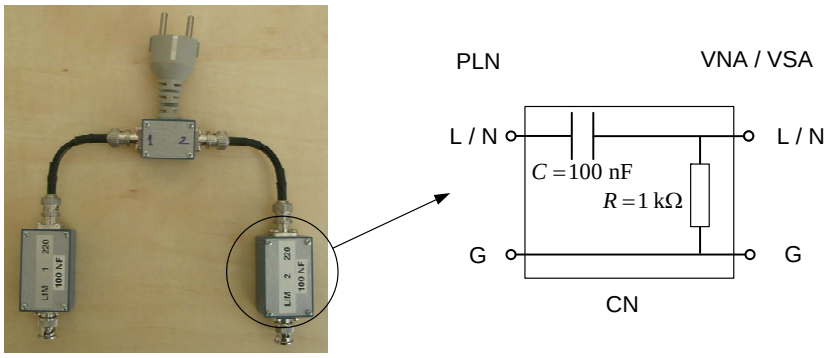

Figure 3.12: CNs used for the measurement of PLNs.

Therefore, the steps that must be followed are:

1. Measurement of the S parameters of the PLN. The setup can be seen in figure 3.13, and basically consists of a VNA and two CNs. In order to compensate the effects of the CNs, the transient suppressors and the cables, the system is calibrated at the CN-PLN interface using the calibration standard TOSM [101]. Once the S parameters are measured, the impedances Z_L, Z_N and Z_T are computed with (3.1).

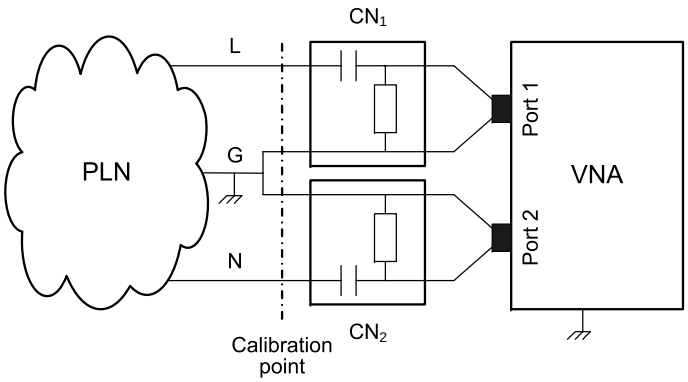

Figure 3.13: Block diagram of the S-parameter measurement setup of a PLN.

2. Measurement of the voltages and currents V_L, I_L, V_N and I_N at the PLN terminals. The measurement setup is mainly composed by a VSA and the two CNs, as seen in figure 3.14.

   Since both CNs are completely decoupled, the setup of figure 3.14 can be analyzed with its equivalent circuit, as seen in figure 3.15. The effect of CN_1 and CN_2, transient suppressors and cables are represented with their S parameters ($[S_L]$ and $[S_N]$ respectively).

   Analyzing the circuit of figure 3.15, the V_L and V_N voltages and the I_L and I_N currents are obtained from the measured voltages at the terminal ports of the VSA (V_{BL} and V_{BN}) and the measured S parameters of the CNs (plus transient limiters and cables):

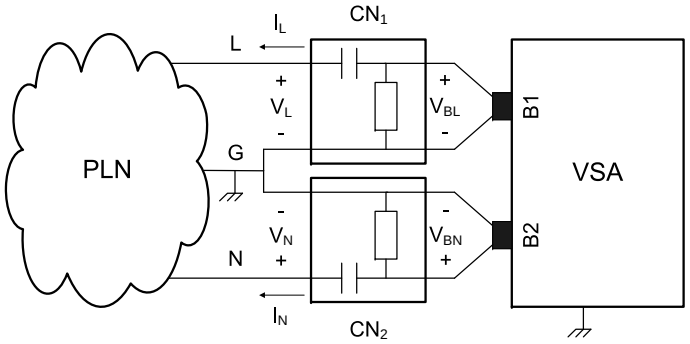

Figure 3.14: Block diagram of the voltages and currents measurement setup at the PLN terminals.

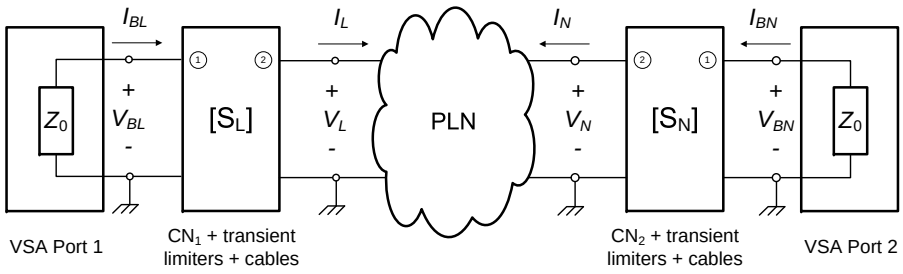

Figure 3.15: Equivalent circuit of the PLN measurement setup.

$$\begin{aligned} V_L &= V_{BL}\left(\frac{1+S_{L22}}{S_{L12}}\right) \\ V_N &= V_{BN}\left(\frac{1+S_{N22}}{S_{N12}}\right) \\ I_L &= -\frac{V_{BL}}{Z_0}\left(\frac{1-S_{L22}}{S_{L12}}\right) \\ I_N &= -\frac{V_{BN}}{Z_0}\left(\frac{1-S_{N22}}{S_{N12}}\right) \end{aligned} \tag{3.11}$$

where Z_0 is the reference impedance for the measurement system (and the input impedance of the VSA). The interference voltage sources V_{nL} and V_{nN} can be obtained using (3.3).

3. Finally, having found all the values of the components of the circuit model (Z_L, Z_N, Z_T, V_{nL} and V_{nN}), the values of the components of the modal model (Z_{CM}, Z_{DM}, Z_{TM}, V_{nCM} and V_{nDM}) are computed using (3.6) and (3.7).

3.4.2 Experimental validation

Test network

The measurement method for PLNs differs from the measurement method for DUTs because two CNs are used instead of the LISN. In order to validate the PLN measurement method, a test network that simulates a real PLN from the EMC point of view has been implemented.

The test network keeps the same structure as the test device used in the validation of the measurement method for DUTs (figure 3.7), but with different impedances, as seen in figure 3.16. The relations between the impedances and interference sources of the test network and its circuit model can be found using (3.9) and (3.10). The interference sources V'_{nL} and V'_{nN} have been implemented using an RF generator with two outputs of equal amplitude (97 dBμV) and a phase-shift between them of 65 degrees in all the frequency range between 50 kHz and 35 MHz.

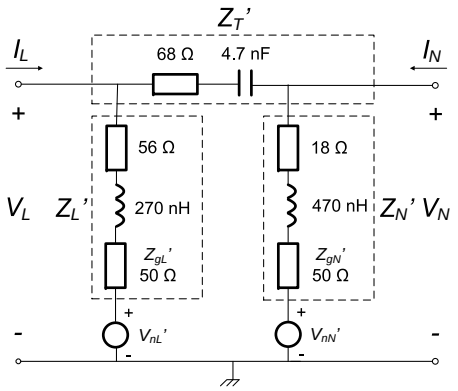

Figure 3.16: Test network.

Circuit validation

Figure 3.17 compares the computed and the measured values for the circuit impedances Z_L, Z_N and Z_T for the test network of figure 3.16 in the frequency range from 50 kHz to 35 MHz.

Figure 3.18 compares the interference sources V_{nN} and V_{nL} obtained by applying (3.10) to the physical source values and the ones of the circuit model obtained with the proposed methodology.

Modal validation

The modal model is found by applying (3.6) to the circuit values. Figure 3.19 shows the modal impedances (Z_{CM}, Z_{DM} and Z_{TM}) obtained from the impedances measured individually and from the impedances of the circuit model, and figure 3.20 shows the comparison of the modal interference sources (V_{nCM} and V_{nDM}).

The good agreement shown in both characterizations (circuit and modal) regarding to impedance and voltage sources, validates the models and the measurement system of a PLN.

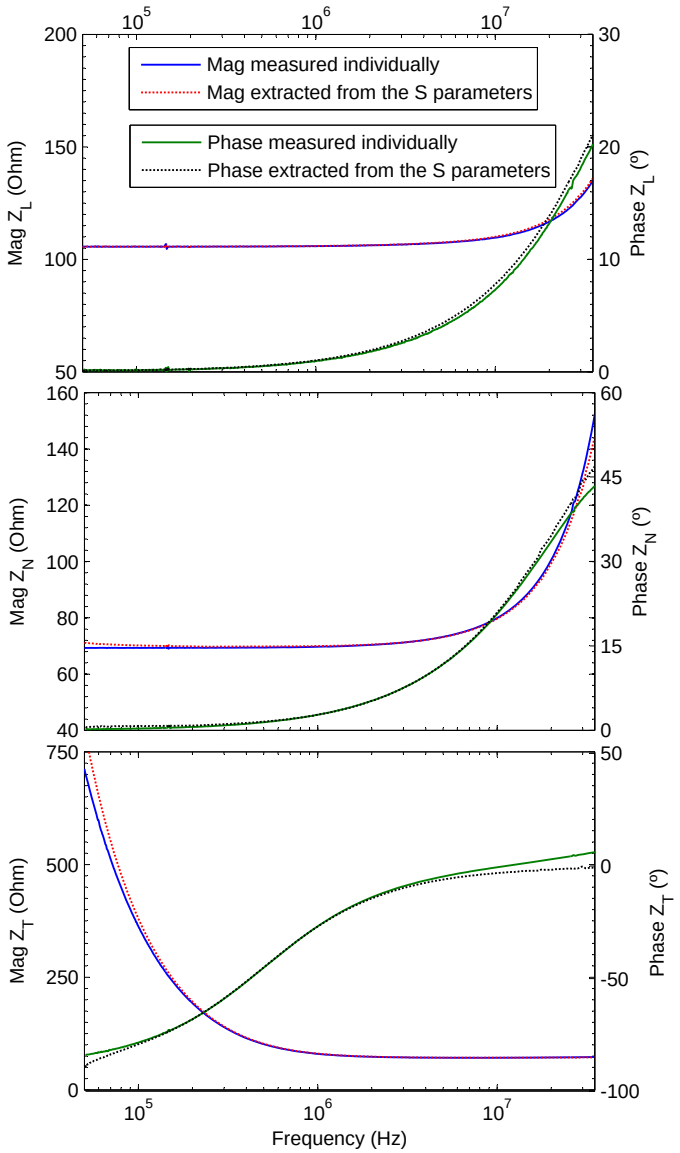

Figure 3.17: Comparison between the impedance values Z_L, Z_N and Z_T of the test network of figure 3.16 computed and measured.

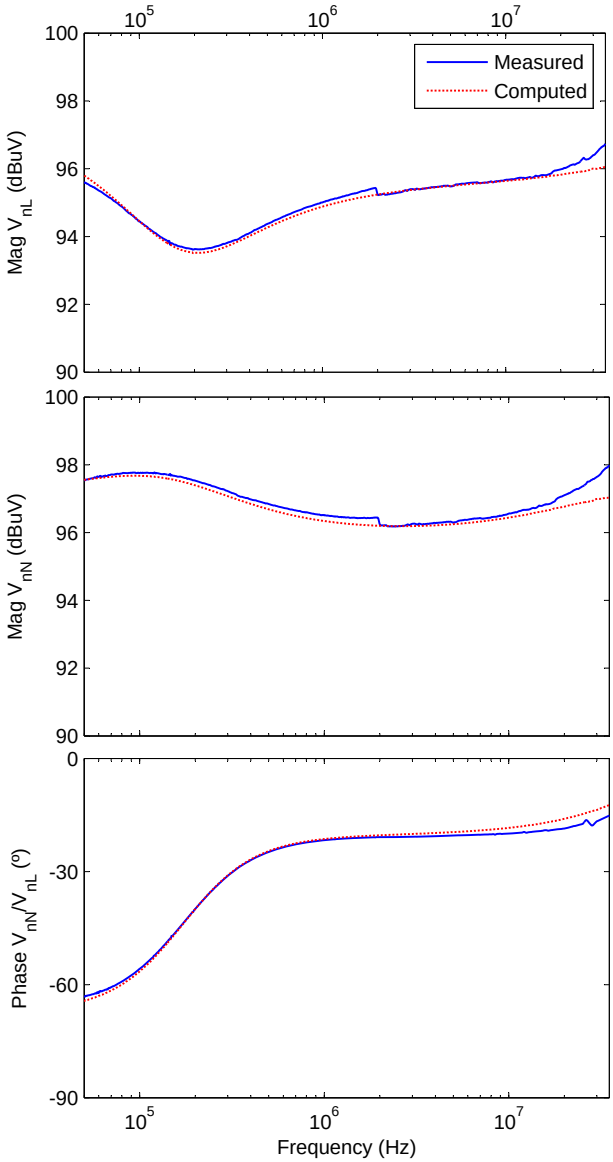

Figure 3.18: Comparison between the interference sources V_{nN} and V_{nL} of the circuit model of the test network and the ones obtained by applying (3.10) to its physical sources.

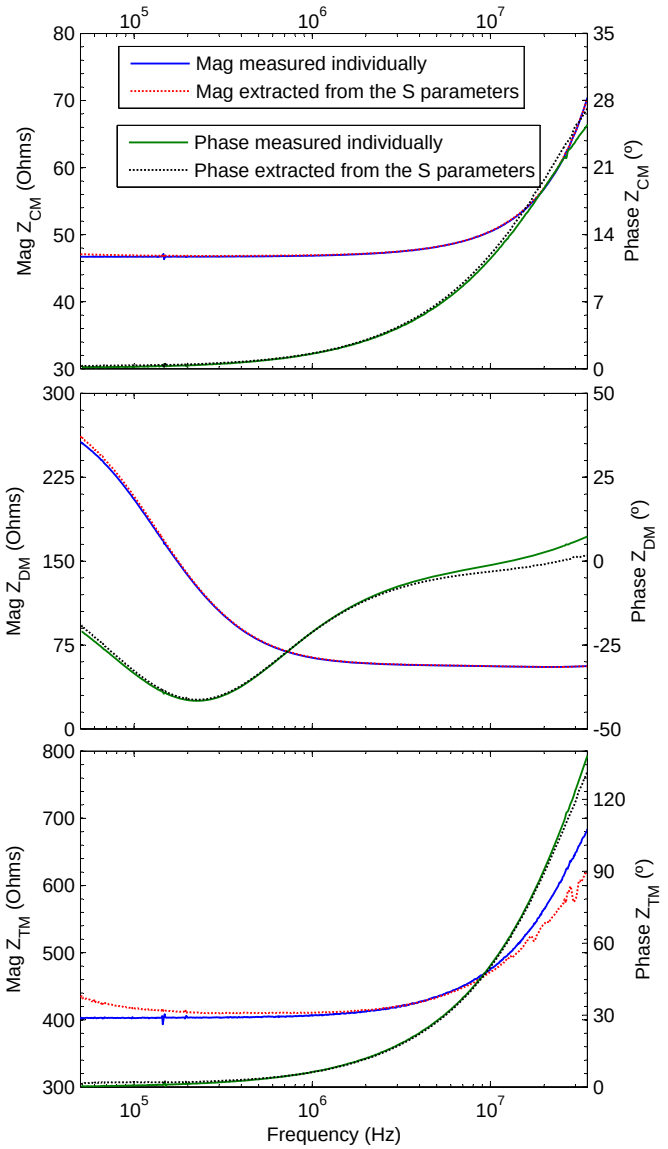

Figure 3.19: Comparison between the modal impedances Z_{CM}, Z_{DM} and Z_{TM} of the test network obtained from the impedances measured individually and from the impedances of the circuit model.

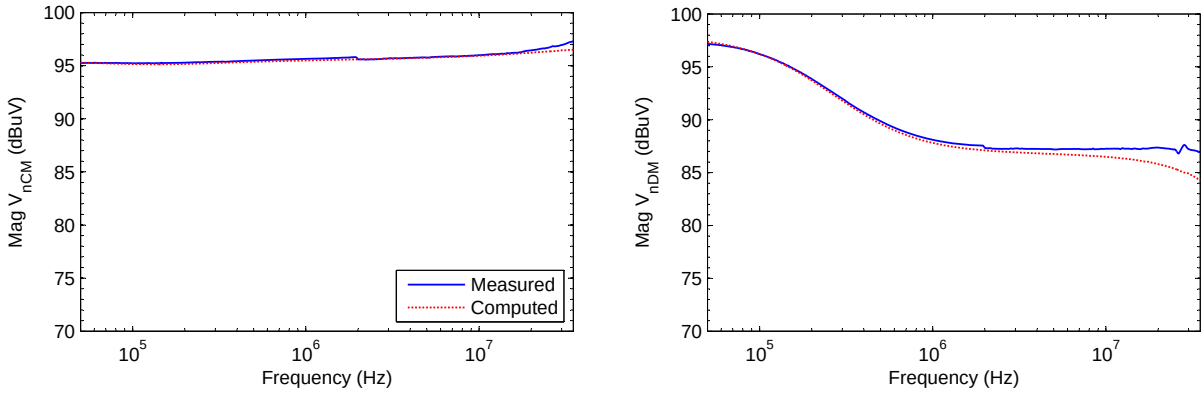

Figure 3.20: Comparison of the modal interference sources obtained from the physical voltage sources mathematically converted with (3.10), and from the interference sources of the circuit model.

3.5 Measurements on real devices and networks

The measurement and characterization methodologies proposed before have been used to find the parameters of the circuit and modal models of a commercial 100-W HF transceiver transmitting a 4-MHz carrier (figure 3.21) and an actual PLN in an office environment.

Figure 3.21: 100-W HF Transceiver with a switching power supply.

3.5.1 Example of real electric device measurement

Figure 3.22 shows the circuit and modal impedance values of the transceiver. In general, the modal impedance Z_{TM} is higher than Z_{CM} and Z_{DM}, except for the 150 kHz to 200 kHz frequency band, where Z_{TM} and Z_{CM} are similar. In those frequencies an important mode conversion level can exist.

Figures 3.23 and 3.24 show the circuit and modal interference source values. A set of interference in the band from 150 kHz to 2 MHz, generated by the switching power supply of

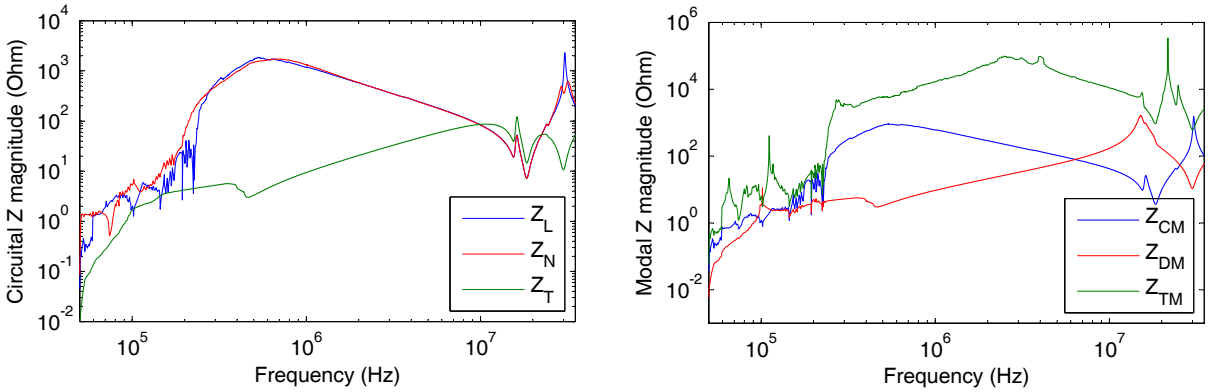

Figure 3.22: Circuit and modal impedances of the 100-W HF transceiver.

the transceiver, can be seen. Interference at multiple frequencies of 4 MHz are also noticeable. In this case, the CM is the predominant mode of the conducted emissions.

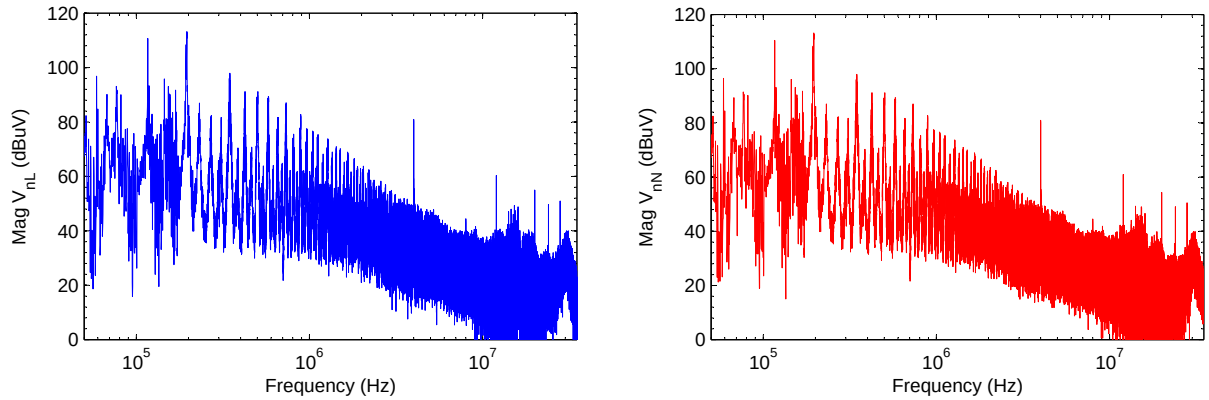

Figure 3.23: Circuit interference sources of the 100-W HF transceiver.

3.5.2 Example of a real power-line network measurement

Figure 3.25 shows the circuit and modal impedances of the PLN. As can be seen, the circuit impedances Z_L and Z_N are practically identical. On the other hand, the value of the DM impedance (Z_{DM}) is very low at low frequencies due to the equivalent impedance of all DUTs connected in parallel to the PLN and the low output impedance of the 50-Hz low voltage transformer. At the same frequencies, the CM impedance (Z_{CM}) is higher because the DUTs present a low coupling between both lines (L and N) and G. At higher frequencies the impedance parasitics of the PLN increase the DM impedance and its values are comparable to those of the CM impedance. The modal transimpedance (Z_{TM}) is usually higher than Z_{CM} and Z_{DM}, but at the frequencies at which their values are similar a strong modal conversion will take place.

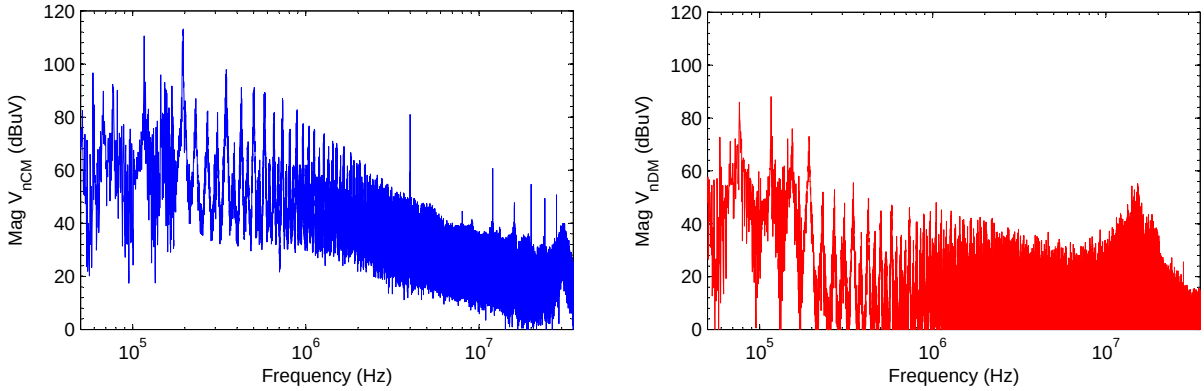

Figure 3.24: Modal interference sources of the 100-W HF transceiver.

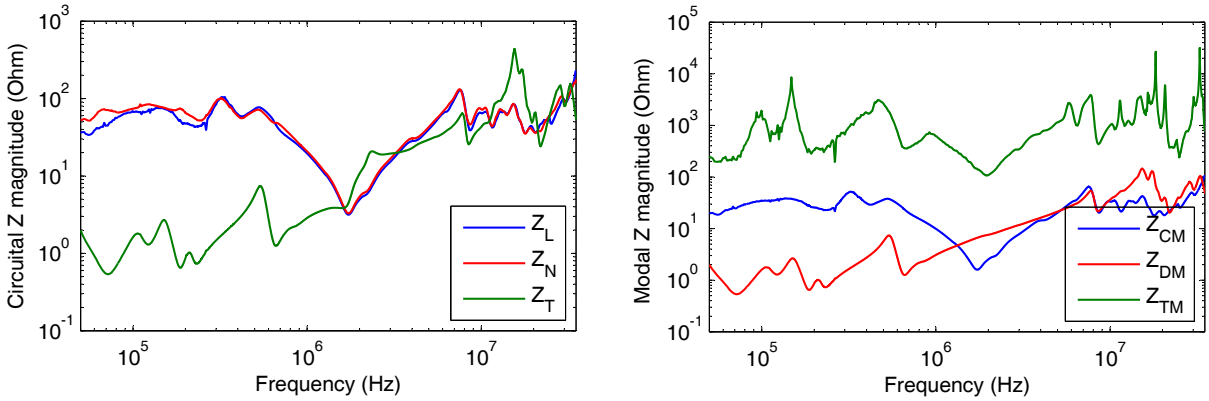

Figure 3.25: Circuit and modal impedances of a PLN in an office environment.

Figures 3.26 and 3.27 show the circuit and modal interference sources. The circuit sources (V_{nL} and V_{nN}) are very similar. Concerning the modal voltages, it can be observed that the CM noise (V_{nCM}) is usually higher than the DM noise (V_{nDM}), as expected from the similarity of the values of L and N impedances and voltages (figures 3.25 and 3.26). This fact results in high levels of CM radiation by the PLN.

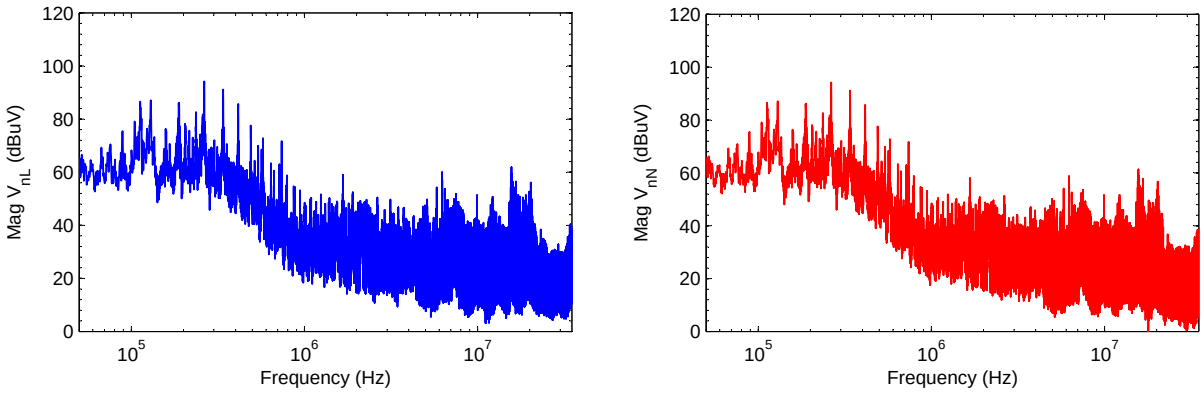

Figure 3.26: Circuit interference sources of a PLN in an office environment.

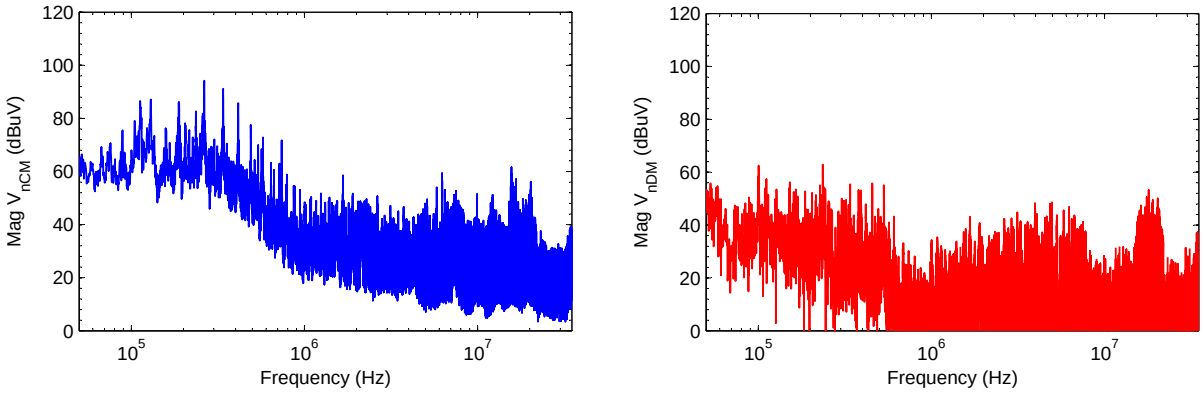

Figure 3.27: Modal interference sources of a PLN in an office environment.