Chapter 4

Characterization of Conducted Emissions in Time Domain

Contents of this chapter

4.1 Introduction

The measurements of the conducted emissions of devices under test (DUTs) and power-line networks (PLNs) presented in the previous chapter were performed using a vector spectrum analyzer (VSA), that is, in the frequency domain. Spectrum analyzers (SAs) are usually used in conducted emissions measurements since they present a high dynamic range and good accuracy of the frequency components of the signal [12]. However, such measurements require a long time when they are performed in accordance with the Electromagnetic Compatibility (EMC)

standards, what entails some disadvantages, as for instance, low precision with the measurement of non-stationary emissions. An alternative way of proceeding is to perform the conducted emissions measurement in the time domain, recovering the frequency components by further signal processing. The advantages of time-domain measurements in front of frequency-domain measurements are:

- Faster measurements: a VSA has to measure all the frequency range (150 kHz-30 MHz) using a narrow resolution bandwidth (RBW) (9 kHz, [12]), that involves slow measurements (specially if the quasi-peak and average detectors are used). Using a high-speed time sampling, it is possible to capture the signal in the time domain and compute its spectral components in a shorter time period [8], [105]–[109].

- Better precision with non-stationary emissions: since the measurement of the conducted emissions with a VSA is performed moving its 9-kHz RBW through the frequency range in several frequency steps, different frequencies are measured at different times. If the signal shows repeating events, the measurement time must be set long enough to ensure that at least one event of interest falls into the dwell time of each frequency step. In the case of a one-time transient, only a single frequency can be measured. This problem can be solved if the event is captured in the time domain, since all the frequencies are measured simultaneously [105], [106].

- The measurements performed by a VSA (peak, quasi-peak, average and phase) can also be obtained by simulating the different detectors via computation. Besides, further information not given by a VSA can be obtained, such as the statistical properties of the interference signal [8], [20], [109]–[114].

- Simpler measurement devices: it is easier to find a two-channel oscilloscope than a two-channel VSA, and the cost of an oscilloscope is usually cheaper than the VSA one [13], [20], [106], [107].

Therefore, time-domain analyzers seem to be the best choice for the conducted emissions measurements, especially for DUTs with non-stationary emissions. On the other hand, it must be considered that the time domain approach presents a limited dynamic range due to the quantization error [106]. For instance, an 8-bit oscilloscope has a theoretical dynamic range of about 48 dB while SAs usually present a dynamic range above the 80 dB. This is the main reason for what most of the EMC labs still measure the conducted emissions in the frequency-domain despite all the advantages of time-domain measurements presented above.

In this chapter, the feasibility of the circuit and modal characterization of DUTs via time-domain measurements is studied. To this end, the second section reviews the mathematical basis for the data transformation from time domain to frequency domain. In the third section, two different setups to measure the conducted emissions in time domain are presented and discussed, and the one with better performance is used to characterize a DUT with stationary

noise. The model obtained is finally validated by comparing its simulated conducted emissions with the ones measured with a SA. In the fourth section, the methodology is used to characterize a DUT with non-stationary noise, showing that time-domain measurements are very useful when frequency-domain measurements cannot be applied.

4.2 Theory of signal processing

4.2.1 Discrete Fourier transform

The digitization of a continuous-time signal $x(t)$ with a sampling frequency f_s (that corresponds to a sampling interval $\Delta t = 1/f_s$) leads to the discrete-time signal $x\,[n]$, where $x\,[n] = x(n\Delta t)$. Shannon's theorem requires f_s to be at least twice as high as the maximum signal frequency [105]. If $x\,[n]$ is a data block of N samples, its spectral estimation is obtained via the discrete Fourier transform (DFT) [115]:

$$X\,[k] = \sum_{n=0}^{N-1} x\,[n]\, e^{-\frac{j2\pi kn}{N}} \text{ with } 0 \leq k < N \tag{4.1}$$

The DFT transforms the discrete-time signal sequence $x\,[n]$ into the discrete-frequency spectral sequence $X\,[k]$, with k denoting the discrete frequency interval $X\,[k] = X(k\Delta f)$. Due to the basic properties of the DFT, the relation between Δt, N and Δf is:

$$\Delta f = \frac{1}{N\Delta t} \tag{4.2}$$

The DFT of a time-domain sampled waveform is a symmetric function which becomes redundant beyond the Nyquist frequency ($f_s/2$). Therefore, the spectral information can be evaluated from only one half of $X\,[k]$, but its magnitude has to be multiplied by two in order to balance the signal energy of the other half. Besides, the DFT has to be normalized by the number of time-domain samples N in order to obtain results analogous to the continuous Fourier transform, and divided by $\sqrt{2}$ (for $k > 1$) to compute the root mean square (RMS) values [105]. Joining all the scaling factors and obviating the direct-current (DC) component ($X[0]$), the following definition is obtained:

$$X\,[k] = \frac{\sqrt{2}}{N} \sum_{n=0}^{N-1} x\,[n]\, e^{-\frac{j2\pi kn}{N}} \text{ with } 1 \leq k < \begin{cases} \frac{N}{2} \text{ for N even} \\ \frac{N+1}{2} \text{for N odd} \end{cases} \tag{4.3}$$

4.2.2 Windowing

The DFT assumes that the finite data set $x\,[n]$ is one period of a periodic signal. If $x\,[n]$ do not contain an integer number of periods, the transition between two consecutive periods is discontinuous. This fact causes a leakage of the DFT coefficients, known as spectral leakage. In order to reduce this effect, a weighting function can be used [105]:

$$x_w[n] = x[n]\, w[n],\ 0 \leq n < N \tag{4.4}$$

The weighting function is chosen to smoothly roll off to zero the edge points of the signal in time domain. This is equivalent to convolute the signal $X[k]$ with a function whose side lobes have lower amplitude than the square window ones. Figure 4.1 shows some popular weighting functions in time and frequency domain. As can be seen, the improvement in the leakage comes as a trade-off against frequency resolution and energy. However, $w[n]$ can be scaled to make its integral over the observation interval ΔT_N equals the unity with a scaling factor called coherent gain (G_C) [116]:

$$G_C = \frac{1}{N} \sum_{n=0}^{N-1} w[n] \tag{4.5}$$

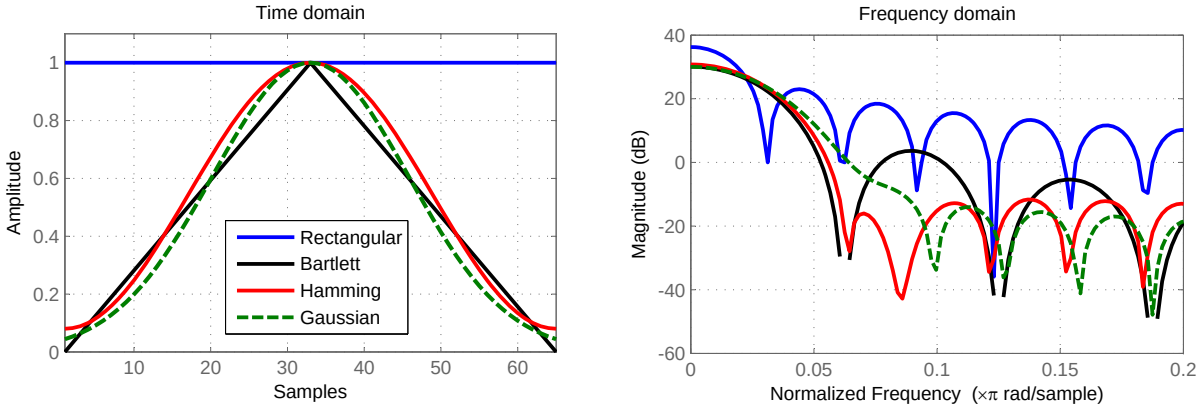

Figure 4.1: Different window functions.

Due to the linearity of the DFT, the scalar factor G_C can be applied after the transformation into the frequency domain:

$$X_w[k] = \frac{\sqrt{2}}{G_C N} \sum_{n=0}^{N-1} x_w[n]\, e^{-\frac{j2\pi kn}{N}} \text{ with } 1 \leq k < \begin{cases} \frac{N}{2} \text{ for N even} \\ \frac{N+1}{2} \text{for N odd} \end{cases} \tag{4.6}$$

Different choices of window functions present different compromises between leakage suppression and spectral resolution.

4.2.3 Time-frequency analysis

When a DUT is sensitive to emit non-stationary interference, the analysis of its spectra evolution through time can be more interesting than its one-dimensional spectrum. To perform such characterization, the short-time Fourier transform (STFT) can be used [117]–[119]. This method shifts a window $w[n]$ of length L over the signal $x[n]$ of length N in n' steps of s

samples, satisfying $N \geq L$ and $s \leq N$ (so that each block is overlapped by $N - s$ samples), and computes the DFT of each block to obtain $X\left[n', k\right]$, which depends of the time shift n' and the frequency k:

$$X_w\left[n', k\right] = \frac{\sqrt{2}}{G_C L} \sum_{m=0}^{L-1} x\left[sn' + m\right] w\left[m\right] e^{\frac{-j2\pi km}{N}}$$
$$\text{with } 1 \leq k < \begin{cases} \frac{N}{2} \text{ for N even} \\ \frac{N+1}{2} \text{for N odd} \end{cases} \text{ and } 0 \leq n' < \frac{N-L}{s} \tag{4.7}$$

The observation time T_{ob}, the time resolution Δt_{STFT} and the frequency resolution Δf are given by:

$$T_{ob} = \frac{N-L}{f_s} \quad \Delta t_{STFT} = \frac{s}{f_s} = s\Delta t \quad \Delta f = \frac{1}{L\Delta t} \tag{4.8}$$

The choice of the window length and the number of overlapping samples becomes a trade-off between frequency and time resolution.

4.3 Measurement system

4.3.1 Measurement methodology

The methodology to characterize a DUT consists of the following steps:

1. Measurement of the scattering (S) parameters of the DUT at its line (L) and neutral (N) ports as it was explained in chapter 3. The impedances Z_L, Z_N and Z_T are obtained with (3.1).

2. Measurement of the conducted emissions in time domain. Figure 4.2 shows two possible setups for the conducted emissions measurements in time domain: in figure 4.2(a) the conducted emissions are measured using two current probes on L and N terminals, a similar setup to the one used in [120] for the conducted emissions measurements of a DC-DC converter; in figure 4.2(b) the conducted emissions are measured after the line impedance stabilization network (LISN), as it was done in the previous chapter with the VSA.

   After measuring the conducted emissions in time domain, the spectral components are computed using (4.6). However, the information obtained in each scenario is different:

   - From the measurement setup of figure 4.2(a), the currents at the terminal ports I_L and I_N are obtained. Considering the equivalent circuit of the measurement system as seen in figure 3.6, the V_L and V_N voltages can be recovered using the following

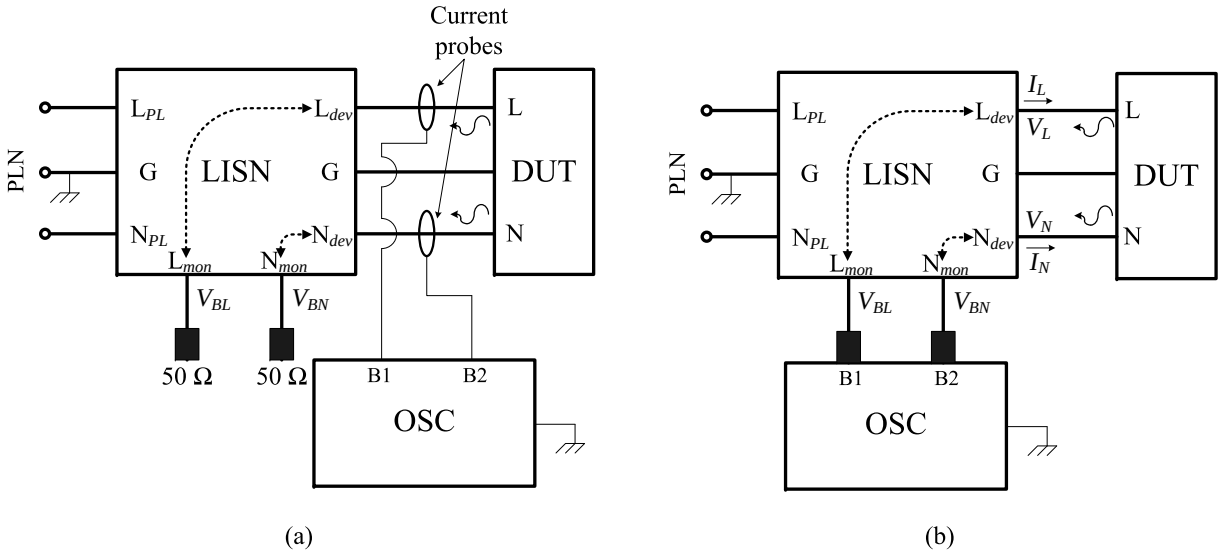

Figure 4.2: Two possible setups for the conducted emissions measurements in time domain via (a) current measurements or (b) voltage measurements.

expressions:

$$\begin{aligned} V_L &= I_L\left(Z_0\frac{S_{34}S_{43}-(S_{33}+1)(S_{44}-1)}{S_{34}S_{43}-(S_{33}-1)(S_{44}-1)}\right)+I_N\left(Z_0\frac{2S_{34}}{S_{34}S_{43}-(S_{33}-1)(S_{44}-1)}\right) \\ V_N &= I_N\left(Z_0\frac{S_{34}S_{43}-(S_{33}-1)(S_{44}+1)}{S_{34}S_{43}-(S_{33}-1)(S_{44}-1)}\right)+I_L\left(Z_0\frac{2S_{43}}{S_{34}S_{43}-(S_{33}-1)(S_{44}-1)}\right) \end{aligned} \tag{4.9}$$

where Z_0 is the reference impedance of the measurement system. Once the V_L and V_N voltages are found, the interference voltage sources V_{nL} and V_{nN} can be obtained using (3.3).

- From the measurement setup of figure 4.2(b), the voltages at the terminal ports of the oscilloscope V_{BL} and V_{BN} are obtained. The V_L and V_N voltages can be recovered by using (3.8), and the interference voltage sources V_{nL} and V_{nN} with (3.3). I_L and I_N can also be obtained with the following expressions:

$$\begin{aligned} I_L &= \frac{V_L}{Z_0}\left(\frac{S_{34}S_{43}-(S_{33}-1)(S_{44}+1)}{S_{34}S_{43}-(S_{33}+1)(S_{44}+1)}\right)+\frac{V_N}{Z_0}\left(\frac{-2S_{34}}{S_{34}S_{43}-(S_{33}+1)(S_{44}+1)}\right) \\ I_N &= \frac{V_N}{Z_0}\left(\frac{S_{34}S_{43}-(S_{33}+1)(S_{44}-1)}{S_{34}S_{43}-(S_{33}+1)(S_{44}+1)}\right)+\frac{V_L}{Z_0}\left(\frac{-2S_{43}}{S_{34}S_{43}-(S_{33}+1)(S_{44}+1)}\right) \end{aligned} \tag{4.10}$$

where Z_0 is the reference impedance of the measurement system.

3. Finally, having found all the values of the circuit-model components (Z_L, Z_N, Z_T, V_{nL} and V_{nN}), the values of the modal model components (Z_{CM}, Z_{DM}, Z_{TM}, V_{nCM} and V_{nDM}) are computed using (3.6) and (3.7).

4.3.2 Experimental validation

setup selection

In order to determine the most appropriate setup of figure 4.2, both scenarios have been used to perform the time-domain conducted emissions measurements on different switching power supplies as the one of figure 4.3. The measurement settings applied for an optimal capture are: $f_s = 500$ MSps, which corresponds to a $\Delta t = 2$ ns, and low-pass filtering with a cut-off frequency of 250 MHz; the storage length is of 1 MS, leading to a $\Delta f = 500$ Hz and a Nyquist frequency of 250 MHz. The frequency components are obtained computing (4.6) with the Fast Fourier Transform (FFT) algorithm [115].

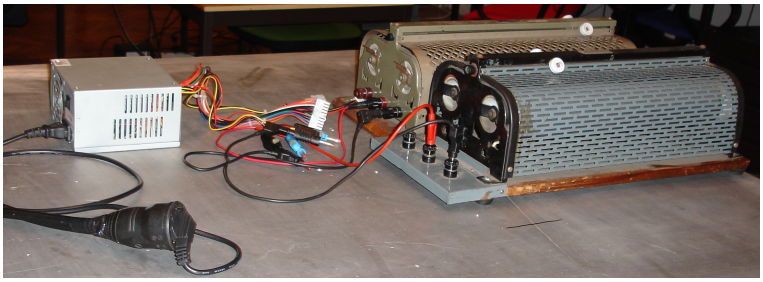

Figure 4.3: Switching power supply connected to several loads.

Figure 4.4 shows the currents at the L and N terminals of one of the switching power supplies, measured with the setup of figure 4.2(a) (using two Tektronix TCP0030 current probes with a current sensitivity of 1 mA) and the setup of figure 4.2(b). When the setup of figure 4.2(a) is used, the low frequency is not filtered and the spectral components of the 50-Hz windowed signal masks the conducted emissions of the switching power supply. To reduce this effect, the 50-Hz signal is filtered by applying detrending techniques [121]. As can be seen, both measurement setups present similar peak frequency results, but the setup of figure 4.2(b) presents a better sensitivity. Until now there is not any current probe available in the market with the same frequency span and better sensitivity, which means that it is not possible to get better results from current measurements without using further external devices. Therefore, the setup of figure 4.2(b) has been selected to validate the DUT characterization with time-domain measurements.

Validation of the characterization via time-domain measurements

To validate the characterization of a DUT with conducted emissions via time-domain measurements, the complete characterization of a switching power supply has been performed. The circuit model obtained has been simulated using the circuit of figure 4.5, where the LISN is represented through its S parameters.

The conducted emissions of the same switching power supply have also been measured with a SA according to CISPR 22 [11] (RBW of 9 kHz, dwell time of 100 ms and peak detector).

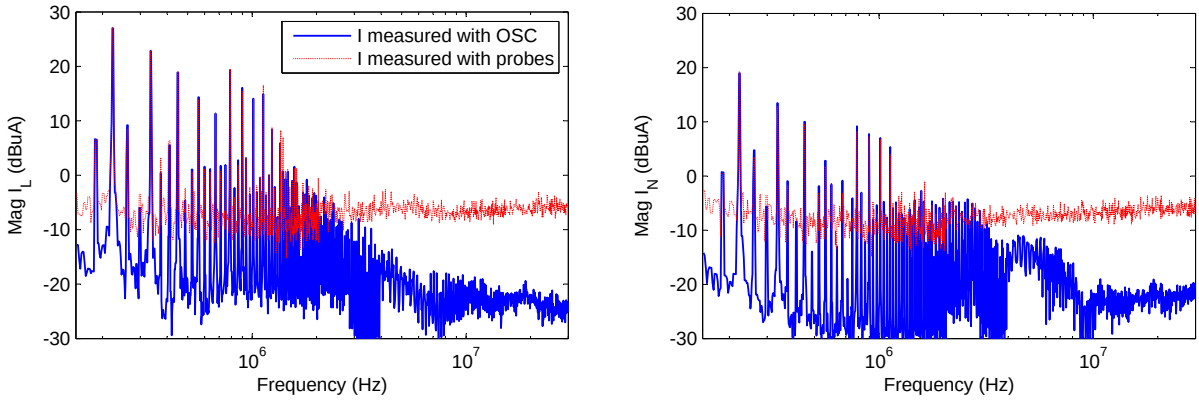

Figure 4.4: Spectrum of the I_L and I_N currents measured with both setups of figure 4.2.

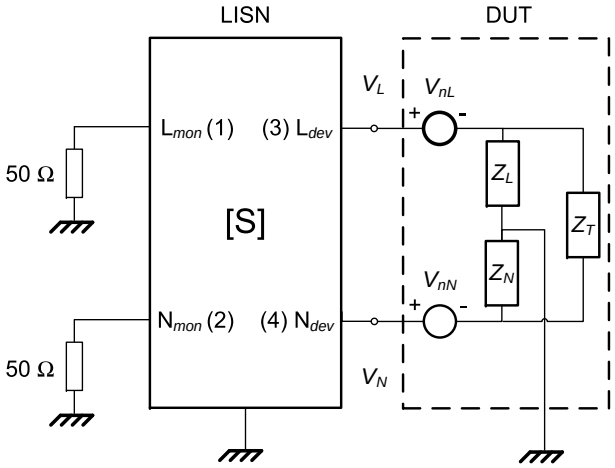

Figure 4.5: Simulation of the circuit conducted emissions of a DUT.

Figure 4.6 shows the simulated and measured conducted emissions of the switching power supply. The good agreement between them proves that time-domain measurements are useful to characterize this kind of DUT. Besides, while the conducted emissions measurement in the frequency domain lasts about ten minutes, the same measurement in time domain and post processing spends only twenty seconds, showing an advantageous reduction of time.

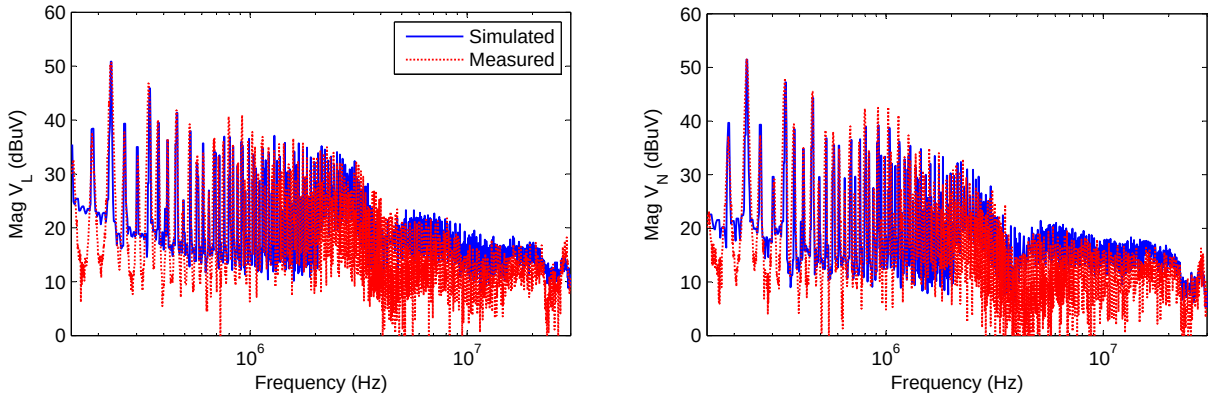

Figure 4.6: Comparison between simulated and measured conducted emissions of a switching power supply.

4.4 Characterization of electric devices with non-stationary emissions

Time-domain measurements have been proved to be useful in terms of time saving when they are applied on the characterization of DUTs with stationary interference. In this section, the same methodology is tested to study its performance when the DUT presents non-stationary interference. Figure 4.7 shows the conducted emissions at the L and N terminals of a switching power supply obtained with the three EMI detectors of a SA [12]: peak, quasi-peak and average detector. As can be seen, the peak and quasi-peak detectors show a wide-band interference which spans from 150 kHz to 30 MHz. However, this emission is not detected with the average detector. This is only explained due to the non-stationary nature of the wide-band interference, as can be seen in figure 4.8, which shows the conducted emissions measured with the SA at the frequency of 200 kHz and zero-span. The interference is only present a few times during the 50-Hz period.

The setup of figure 4.2(b) has been used to measure the same conducted emissions in time domain. The oscilloscope has been programmed to store 1 MS of data with a sample rate of 500 MSps and triggered to ensure the capture of the impulsive noise. Figure 4.9 shows the time-domain emissions measured at the terminals of the LISN. The impulsive noise can be seen in the center of the figure. The conversion of this signal to the frequency domain has been performed to obtain the characterization of the DUT. Once the circuit model, composed by the impedances

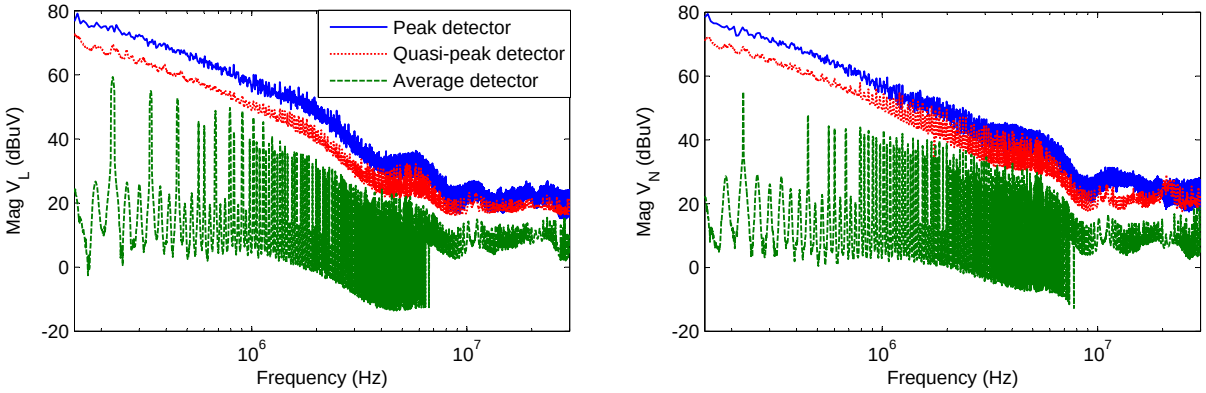

Figure 4.7: Conducted emissions of a switching power supply with the three EMI detectors: peak, quasi-peak and average detector.

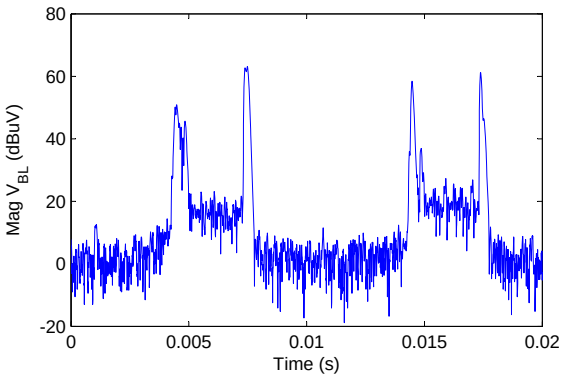

Figure 4.8: Conducted emissions of a switching power supply at the frequency of 200 kHz and zero-span.

Z_L, Z_N and Z_T and the two noise sources V_{nL} and V_{nN}, is obtained, it can be simulated using the circuit of figure 4.5. Figure 4.10 shows the comparison between the simulated conducted emissions of the equivalent model and the conducted emissions measured with the peak detector. As can be seen, both spectra are completely different, since the windowed time-domain signal is long enough to smooth the spectral components of the impulsive noise.

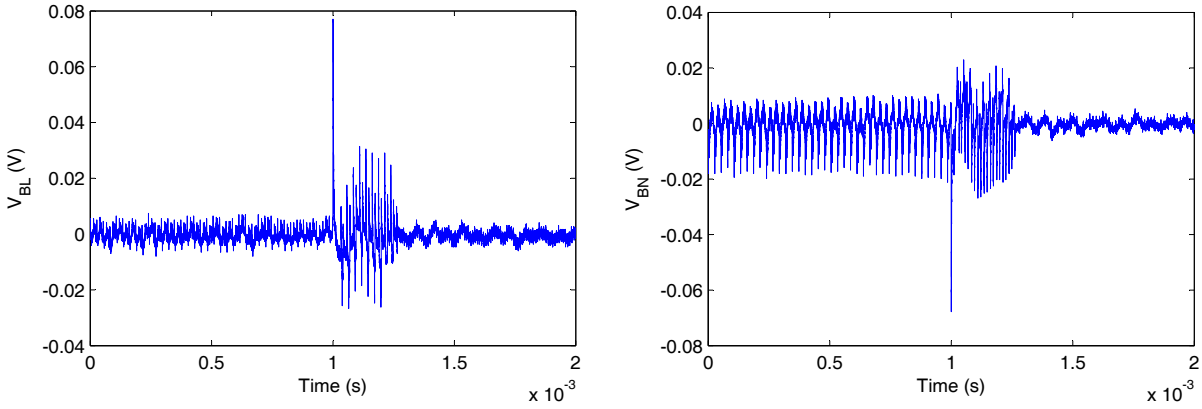

Figure 4.9: Conducted emissions of the switching power supply measured in time domain.

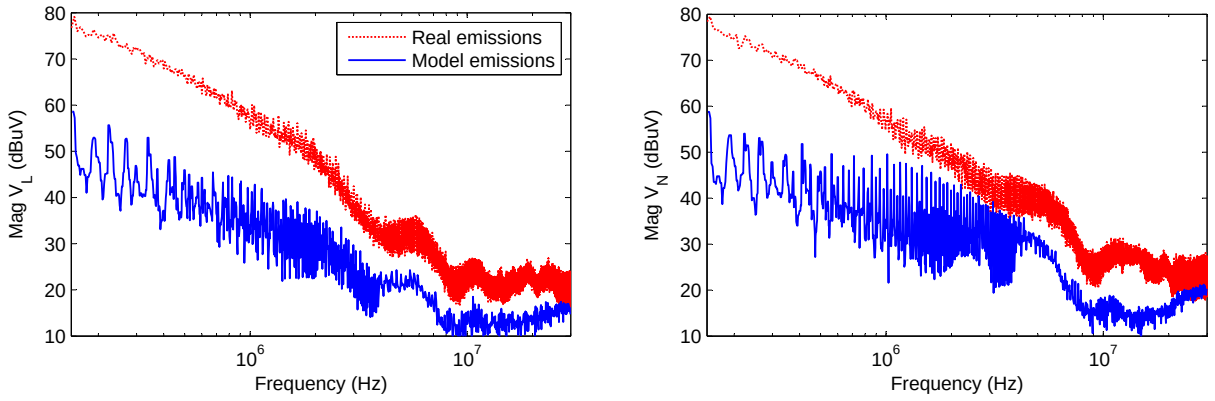

Figure 4.10: Comparison between the simulated conducted emissions and the conducted emissions measured with the peak detector.

In order to visualize the spectra disturbance when the transient appears, the STFT has been applied on the central 0.5 MS of the conducted emissions data at the L terminal (V_L), using a window length of 50000 samples and a step size of 7000 samples. The three-dimensional information is shown in figure 4.11, where the frequency resolution is of 10 kHz, time resolution of 14 μs and a total observation time of 0.9 ms. An increase of the spectral noise can be seen between the 0.4 and 0.6 ms, similar to the spectrum measured with the peak detector (figure 4.7).

The circuit characterization of the switching power supply has been performed again using

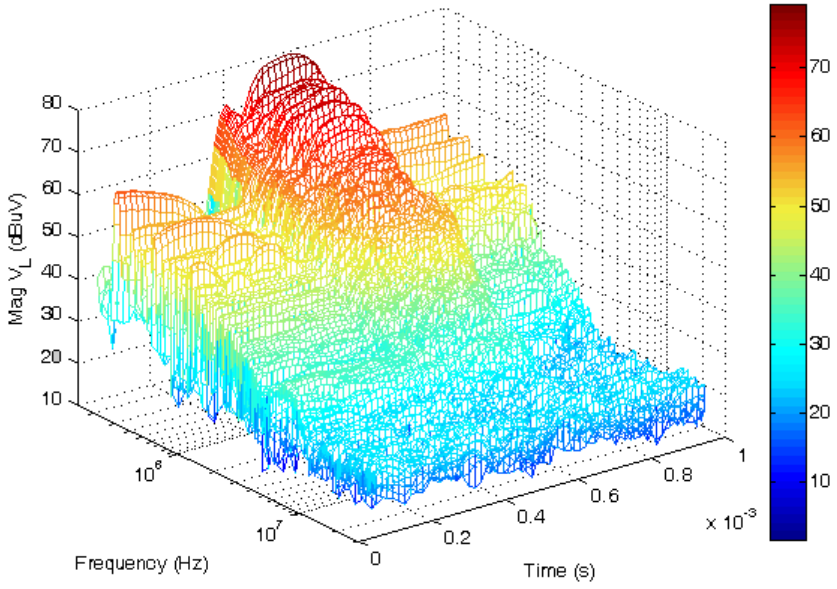

Figure 4.11: STFT of the conducted emissions at the L terminal (V_L).

only the samples that contain the impulsive interference, that is, those placed between the 0.4 and 0.6 ms. The simulation results are shown in figure 4.12, obtaining now a good agreement with the peak-detector measurements. The results obtained show that the impulsive noise of a DUT can be characterized using time-domain measurements.

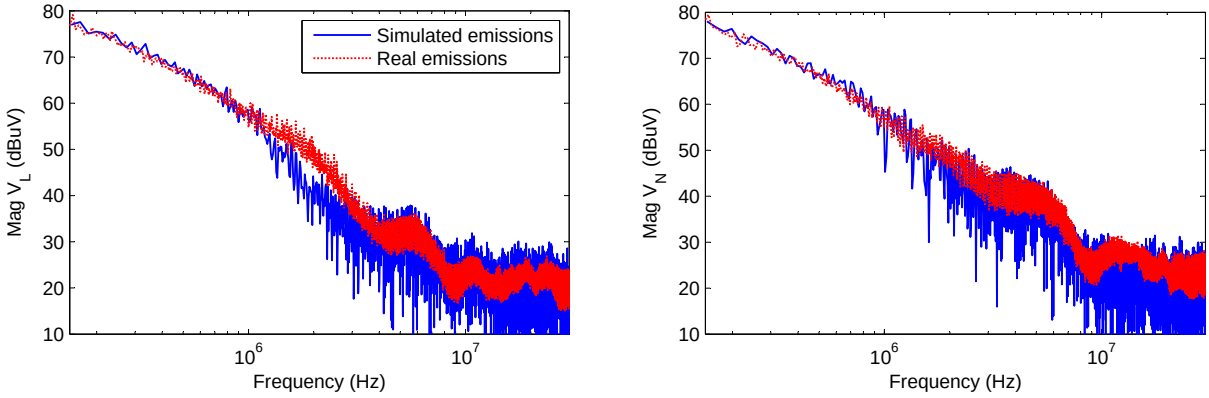

Figure 4.12: Comparison between the simulated conducted emissions and the conducted emissions measured with the peak detector.

The modal conducted emissions of the switching power supply can be simulated using the circuit of figure 4.13. The common-mode (CM) and differential-mode (DM) emissions are shown in figure 4.14. The quasi-peak limit for the circuit emissions of class B devices established in [11] has also been plotted to compare both magnitudes. As can be seen, the dominant mode

is the DM, which exceeds the circuit limit for 20 dB at low frequencies. Therefore, a suitable power-line filter (PLF) for this device has to be composed, at least, by an X capacitor, in order to mitigate the DM emissions. This fact shows that the modal simulation provides useful information for filtering design methodologies.

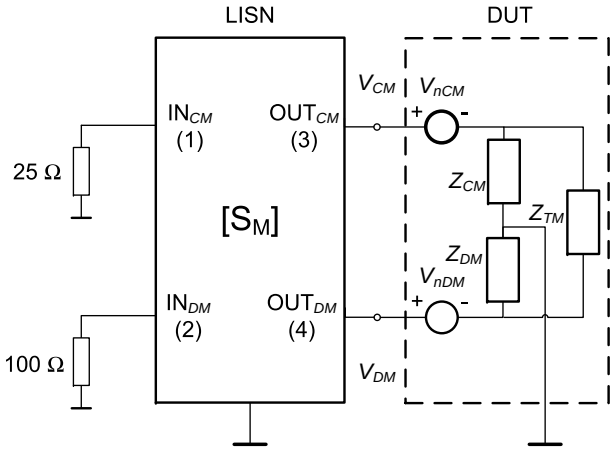

Figure 4.13: Simulation of the modal conducted emissions of a DUT.

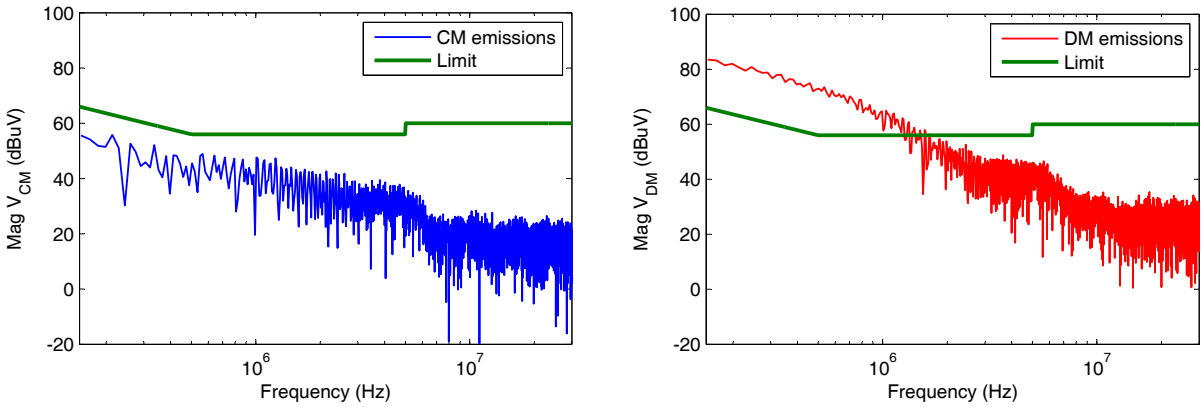

Figure 4.14: Modal conducted emissions of the switching power supply.

In conclusion, time-domain measurements are also useful to characterize DUTs with non-stationary emissions, especially when these emissions cannot be measured with a SA (for instance, when the disturbance is produced only once). In such case, the DFT has to be applied on the data that contains the peak of the impulsive noise. However, if the DUT presents an amplitude level about 38 dB over the limit of the circuit conducted emissions, the spectra under this limit will be difficult to analyze (the frequency range of an 8-bit oscilloscope is about 48 dB). In general, if an EMC designer wants to characterize a DUT with conducted emissions, the choice of the suitable methodology (time or frequency domain) will depend on the intrinsic characteristics of the interference.

Chapter 5

Prediction of Conducted Emissions

Contents of this chapter

5.1 Introduction

The main application of the different characterizations presented in the previous chapters is the prediction of the conducted emission levels that a device under test (DUT) supplies to the power-line network (PLN) through the power-line filter (PLF). Accurate characterizations will allow predictions similar to the real conducted emissions, avoiding long measurement sessions. This chapter presents a methodology to perform the predictions of conducted emissions, and it is structured as follows: the steps that must be followed to perform a prediction are exposed in the second section, either from the circuit point of view (obtaining the circuit voltages and currents at the PLF terminals), or from the modal point of view (obtaining the modal voltages

and currents at the PLF terminals). This methodology is validated in the third section with a test device, firstly, and a real DUT, later.

5.2 Methodology for the prediction of the conducted emissions

In order to predict the circuit or modal conducted interference levels of a DUT connected to a PLF (circuit or modal voltages at the line side of the PLF) that would be obtained in a conducted emissions measurement according to CISPR 22 [11], the steps that must be followed are:

1. Circuit (o modal) characterization of the PLF through its circuit (or modal) scattering (S) parameters, as it is described in chapter 2.
2. Circuit (or modal) characterization of the DUT, as it is described in chapter 3.
3. Circuit (or modal) characterization of the PLN. According to CISPR 22 [11], the conducted emissions must be performed with the DUT connected to an artificial mains network (AMN), that is, the line impedance stabilization network (LISN), which characteristics are defined in CISPR 16 [12]. The LISN can be characterized by its circuit (or modal) S parameters, measured as it is described in chapter 2. However, if the prediction of the emissions introduced in a real PLN is desired, the real PLN can be circuitally (or modally) characterized as it is described in chapter 3.
4. Combined computation or simulation of the previous models. Figure 5.1 shows the elements used in a circuit prediction: the model of the DUT, the PLF and the PLN. The prediction obtains the voltage values of V_L and V_N at the load-side ports of the PLF. Figure 5.2 shows the elements used in a modal prediction: the model of the DUT, the PLF and the PLN. The prediction obtains the values of V_{CM} and V_{DM} at the line-side ports of the PLF.

Since the whole system is modally modeled in figure 5.2, it is possible to identify both qualitatively and quantitatively how interference behave. For instance, if there is a mismatch between the output common mode (CM) generated by the DUT and the port OCM (3) of the PLF, this mode will be reflected (totally or partially) back to the DUT. If the DUT has a low modal transimpedance Z_{TM}, it will convert part of this reflected CM into the differential mode (DM), varying the amount of the DM conducted emissions. Therefore, this modal modeling can explain, for instance, how a mismatch in the filter for the CM can lead to an increase of the conducted emissions for the DM, and vice versa.

5.3 Experimental validation

In order to validate the conducted emissions prediction method, two different devices have been used: the first one is the test device of figure 3.7 connected to the PLF Belling Lee

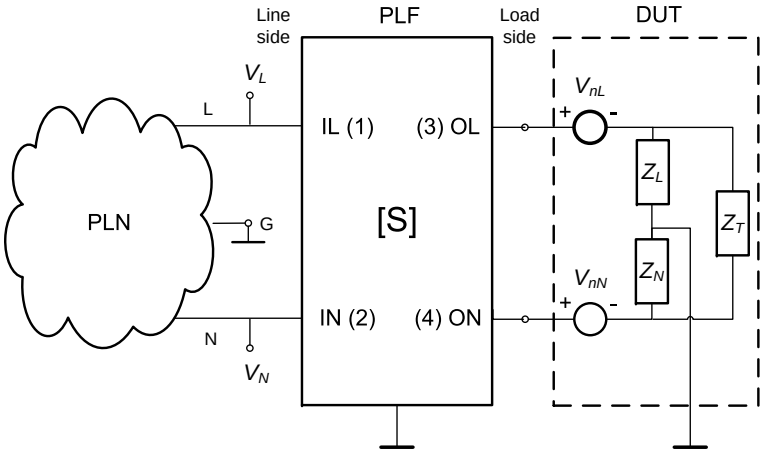

Figure 5.1: Circuit simulation of a DUT with a PLF.

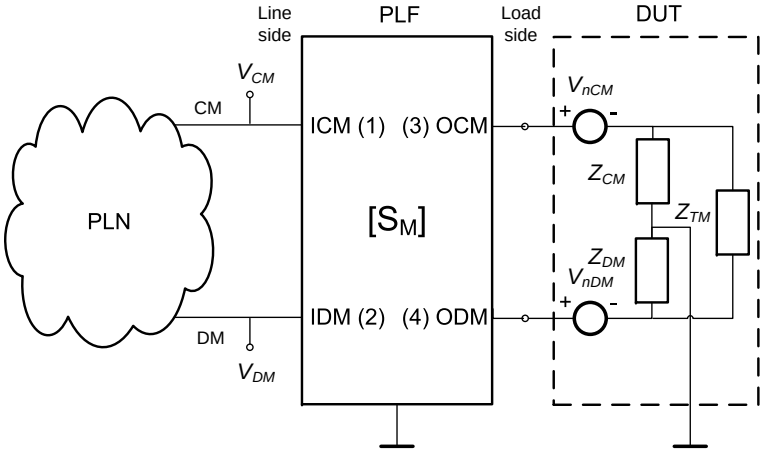

Figure 5.2: Modal simulation of a DUT with a PLF.

SF4110-1/01 1A (with the components $R = 10$ MΩ, $L_1 = L_2 = 1.8$ mH, $C_{Y1} = C_{Y2} = 3.5$ nF, $C_X = 100$ nF, figure 1.4), and the second one is the 100-W high-frequency (HF) transceiver of figure 3.21 connected to the PLF Konfektronic GMBH 2A (with the components $R = 1$ MΩ, $L_1 = L_2 = 4.6$ mH, $C_X = 33$ nF, $C_{Y1} = C_{Y2} = 0$ nF).

5.3.1 Prediction of the conducted emissions of the test device

Circuit prediction

To perform a prediction of the circuit conducted emissions of the test device of figure 3.7, its circuit characterization (Z_1, Z_2, Z_3, V_{nl} and V_{nn}, figure 3.2), the circuit characterization of the PLF (circuit S parameters) and the circuit characterization of the LISN (circuit S parameters) are used in figure 5.1 to simulate the interference propagation through the different devices. The simulated V_L and V_N voltage values have been compared with the conducted emissions measured according to CISPR 22 [11], as seen in figure 5.3, in order to validate the prediction methodology. Figure 5.4 shows the comparison between the predicted and the measured conducted emissions. As can be seen, the prediction is practically superimposed on the measured values.

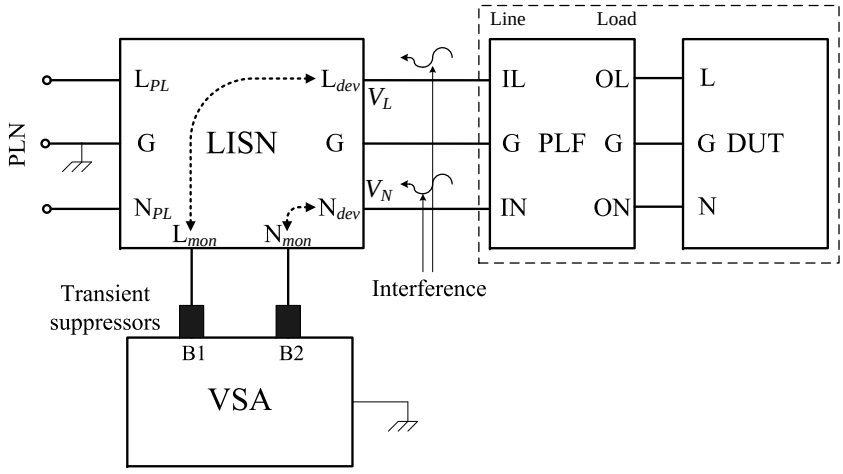

Figure 5.3: Block diagram for the measurement setup of the voltage in the line terminals of a DUT with a PLF.

Modal prediction

To perform a prediction of the modal conducted emissions of the test device, its modal characterization (Z_{CM}, Z_{DM}, Z_{TM}, V_{ncm} and V_{ndm}, figure 3.3), the modal characterization of the PLF (modal S parameters) and the modal characterization of the LISN (modal S parameters) are used in figure 5.2 to simulate the interference propagation through the different devices. The simulated V_{CM} and V_{DM} voltage values have been compared with the modal emissions measured according to the setup of figure 5.3 (V_{CM} and V_{DM} are recovered using

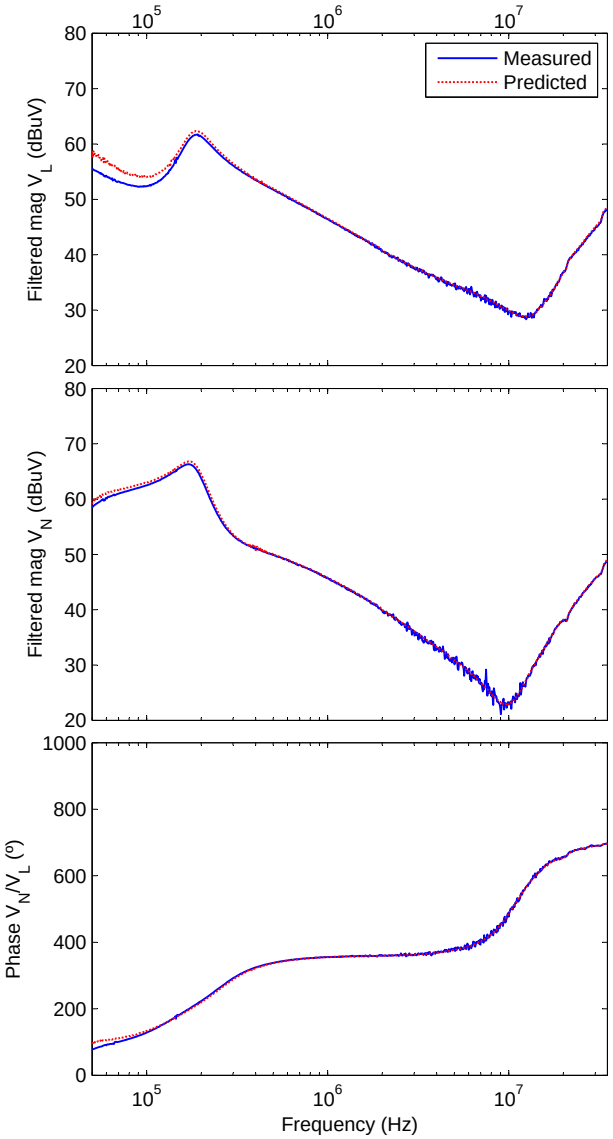

Figure 5.4: Predicted and measured circuit voltages (V_L and V_N) for the configuration of figure 5.3.

(1.1) on the measured V_L and V_N). Figure 5.5 shows the comparison between the predicted and the measured modal emissions. As can be seen, the prediction is again superimposed on the measured values. The good agreement between the prediction and measurement validates both the proposed circuit and modal prediction methodologies.

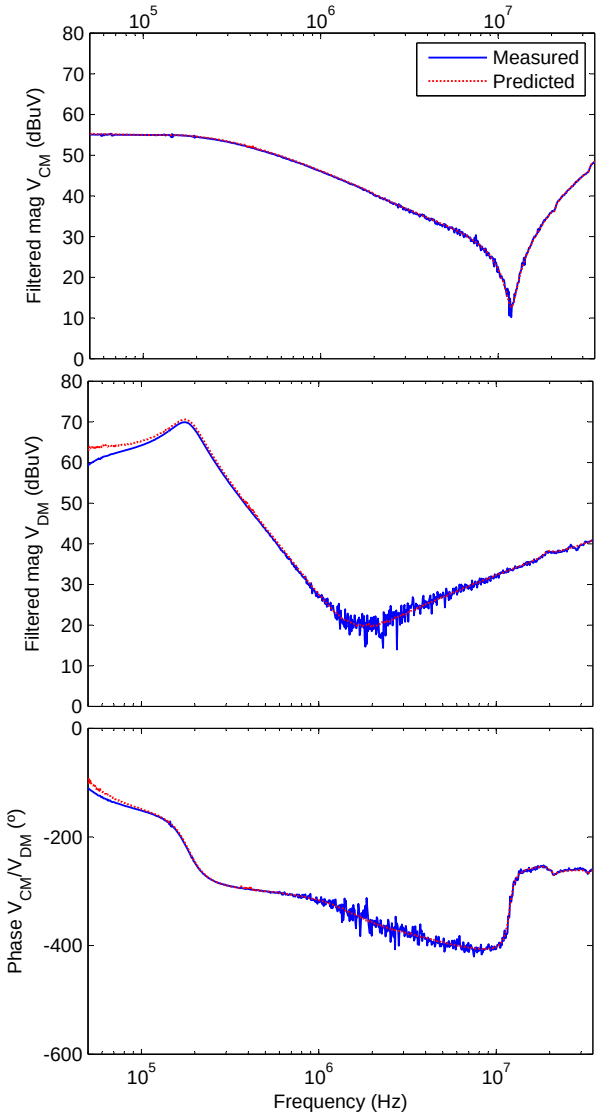

Figure 5.5: Predicted and measured circuit voltages (V_{CM} and V_{DM}) for the configuration of figure 5.3.

In order to state the importance of a complete modal characterization of the DUT, a prediction of the modal conducted emissions generated by the filtered DUT has been made, but this time with $Z_{TM} = \infty$ to emulate a characterization of the DUT considering only its CM and DM impedances. Since there is no connection between CM and DM at the DUT, the reflections of the conducted emissions at the load-side ports of the PLF (due to mismatches between the CM and DM input impedances of the PLF and those of the DUT) that return to

the DUT are not converted to the other mode by Z_{TM}, as occurs in the actual device. Table 5.1 compares, at two selected frequencies, the measured levels of CM and DM interference at the line side of the PLF with the simulated ones with a DUT with $Z_{TM} = \infty$. As can be seen, the predicted values do not match the measured ones. This fact shows that in the design of an optimum PLF for a given DUT, its whole modal model has to be considered in order to account for all the modal conversions that can degrade its behavior. As can be seen in this example, not only the inner mode conversion at the components of the PLF can degrade its performance, but also the interactions (originated by mismatches) of the PLF with mode conversion mechanisms at the components of the DUT.

Voltages (dBuV)	176740 Hz	301155 Hz
Measured V_{CM}	54.76	53.25
Predicted V_{CM} without Z_{TM}	52.36	50.11
Predicted V_{CM} with Z_{TM}	54.83	53.43
Measured V_{DM}	69.89	55.94
Predicted V_{DM} without Z_{TM}	63.02	49.38
Predicted V_{DM} with Z_{TM}	70.58	56.61

Table 5.1: Comparaison of the modal voltages (V_{CM}, V_{DM}) measured, predicted with $Z_{TM} = \infty$ and predicted with the Z_{TM} of figure 3.19, for the test device of figure 3.7 and the PLF Belling-Lee SF4110-1.

Comparison with predictions using 50-Ω insertion loss characterization

As stated in chapter 1, insertion loss (IL) measurements in a 50-Ω measurement system are of little use when the PLF is connected to actual DUTs and PLNs. Besides, they do not detect the modal conversion between modes in the PLF. These facts lead to an unexpected decrease in the performance of the filter. It is, however, a common practice among EMC engineers to compute the expected values of conducted emissions of a DUT with a PLF simply by subtracting from the conducted emissions generated by the DUT (without the PLF) the values of the CM and DM attenuations of the PLF as measured by the standards. Figure 5.6 compares the predicted CM and DM voltages according to this common practice with the actual measured values. As can be seen, the error can be significant, in contrast to the results obtained using the method described in this chapter (figure 5.5). This fact corroborates the adequacy of the approach adopted in this chapter to predict conducted emissions.

5.3.2 Prediction of the conducted emissions of a real DUT

Circuit prediction

The same procedure has been applied to predict the circuit conducted emissions of a 100-W HF transceiver transmitting a 4-MHz carrier (figure 3.21) in order to test their adequacy with actual devices. This device has been characterized and the circuit and modal conducted

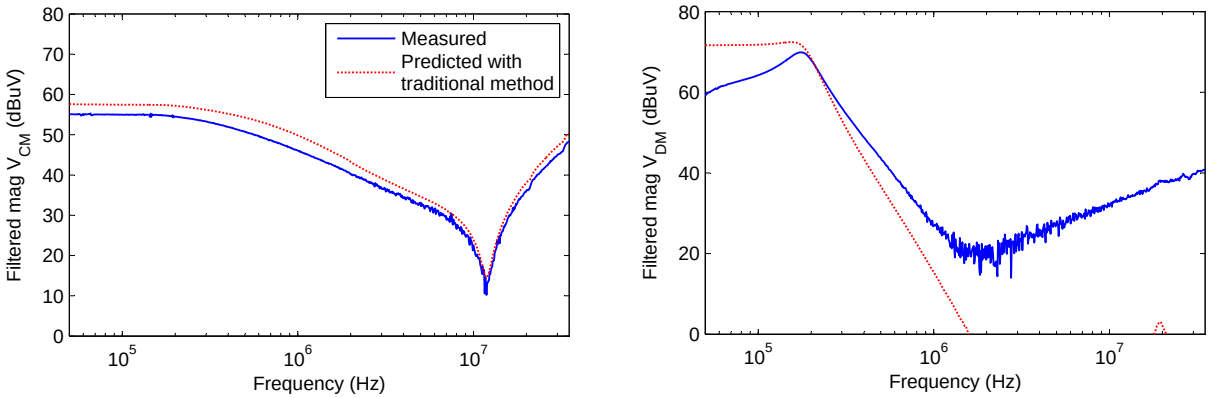

Figure 5.6: Comparison between the conducted emissions predicted according to the common engineering practice and the measured ones.

emissions have been computed using the circuits of figures 5.1 and 5.2 respectively. Both circuits contain the S parameters of the PLF Konfektronic GMBH 2A. The actual emissions have also been measured using the setup of figure 5.3. Figure 5.7 compares the measured and predicted values of the magnitudes of V_L and V_N at the line side of the PLF. A set of interference in the band from 150 kHz to 2 MHz, generated by the switching power supply of the transceiver, can be seen. Interference at multiple frequencies of 4 MHz are also noticeable. By simulating the effect of the PLF on the DUT, some frequencies have been attenuated to levels around -10 dBμV. However, interference levels below 10 dBμV cannot be compared due to the noise floor level of the measurement system (figure 5.3). Beyond 10 dBμV, a good agreement is obtained. The attenuation effect of the PLF is specially observed if the emissions are compared with the ones of figure 3.23.

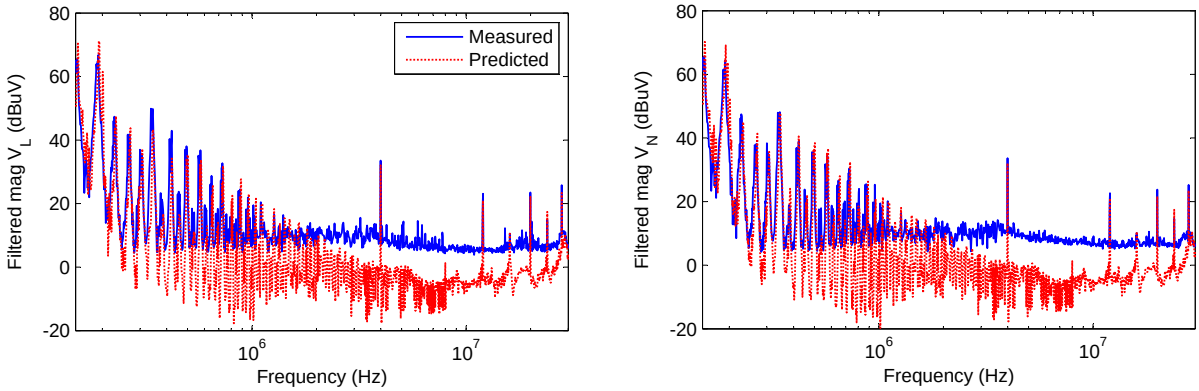

Figure 5.7: Predicted and measured circuit voltages V_L and V_N for the 100-W HF transceiver.

Modal Prediction

Figure 5.8 shows the comparison between the predicted and measured V_{CM} and V_{DM} voltages at the line side of the PLF. The very good agreement between the measurement and prediction validates the approach presented in this chapter, and shows that it is possible to predict the levels of conducted emissions that a generic DUT loaded with a PLF generates according to the desired standard (in this case, with the measurement setup of CISPR 16 [12]). This approach can be very useful in the design of an electronic device (or its PLF), since its levels of conducted emissions can be predicted easily when loaded with previously measured PLFs. This way, long and costly sessions of filter assembly and measurement can be avoided: the DUT has to be measured only once (in order to obtain its circuit and modal models), and its behavior when connected to a set of previously measured filters (as described in chapter 2) easily and rapidly predicted using the presented methodology.

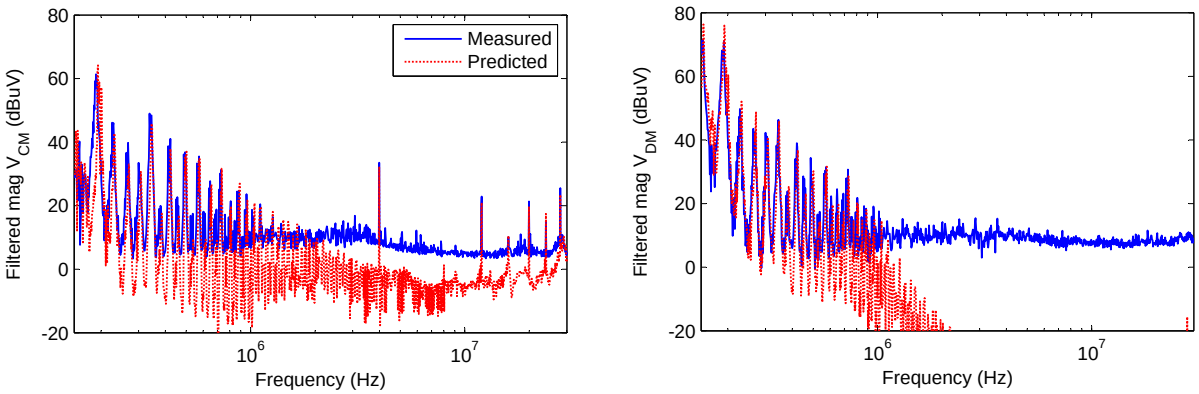

Figure 5.8: Predicted and measured modal voltages V_{CM} and V_{DM} for the 100-W HF transceiver.

Comparison with predictions using 50-Ω IL characterization

As in the previous example, the predictions made by the method described in this chapter have been compared to the predictions made using the PLF attenuations given by the IL in a 50-Ω measurement system. Figure 5.9 compares the modal voltages V_{CM} and V_{DM} according to this common practice with the actual measured values. For most of the CM interfering frequencies, errors of the order of 15 dB have been observed. This fact corroborates again the method adopted to predict the conducted emissions.

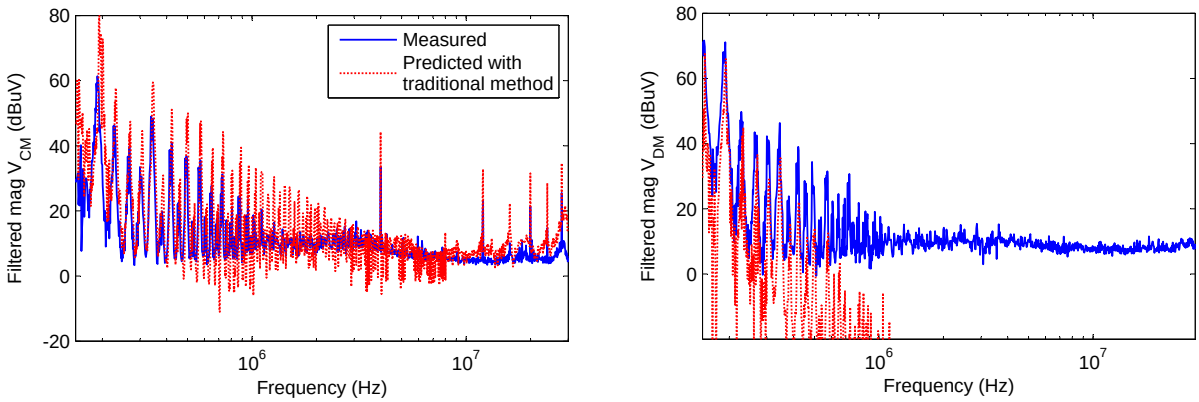

Figure 5.9: Comparison between the conducted emissions predicted according to the common engineering practice and the measured ones.

Chapter 6

Power-Line Filter Design from S-Parameter Measurements

Contents of this chapter

6.1 Introduction

The traditional power-line filter (PLF) design techniques reviewed in the introduction suffered from several disadvantages:

- Using the separated common-mode (CM) and differential-mode (DM) equivalent circuits of a general PLF, the methodologies presented in [49]–[53] find the suitable values of X capacitors, common-mode chokes (CMCs) and Y capacitors considering only their ideal behavior. This can lead to a wrong prediction of the PLF attenuation due to the non-ideal behavior at high frequencies and the mode conversion produced by asymmetric components.

- The optimization techniques of [57] and [58] to implement optimal PLFs are based on a fixed PLF structure. If a more optimal structure exists, it is not considered.

Therefore, the development of a new PLF design technique that improves all these points is needed to implement better PLFs. This methodology has to consider the parasitic impedances and the mode conversion in CMC, X- and Y-capacitor networks, and their best position in the PLF to obtain optimal results.

Different techniques to characterize the parasitic capacitances, the leakage inductance or the actual impedance under in-circuit conditions of CMCs are presented in [29], [122]–[126], and the equivalent circuit of a real capacitor can be found in [127]. These techniques are useful to analyze the characteristics of the PLF components, but they do not present a complete solution from the modal point of view: either they do not contribute with modal information, or they separate the CM and DM attenuation without considering the mode conversion. As can be observed, a similar problem was faced in chapter 2 with the PLF characterization, and the scattering (S) parameters were successfully used in that case. Considering the PLF as a four-port device, the actual CM and DM attenuation and mode conversion appear explicitly in the modal S parameters. Therefore, if the individual components that constitutes the PLF can be analyzed as four-port networks, the same characterization can be applied.

In this chapter, a new PLF design methodology based on the S-parameter characterization is presented. This methodology uses the measured S parameters of each component to compute their combined responses, and finds the best PLF to mitigate the conducted emissions of a particular device under test (DUT) according to the requirements of the designer. For instance, the best PLF can be the one that introduces the maximum attenuation, or the one that presents the lowest cost. The structure followed in this chapter is as follows: the design methodology is presented in detail in the second section, and it is validated in the third section with the results obtained from measurements on real devices with both stationary and non-stationary emissions.

6.2 Methodology for a PLF design

The proposed methodology to design a PLF consists of the following steps:

1. Characterization of CMCs and X and Y capacitors. To this end, four-port networks composed by individual CMCs, X and Y capacitors have been implemented. The block diagram of each network is shown in figure 6.1, and the appearance of some actual implementations can be seen in figure 6.2. For an accurate S-parameter measurement, each port has been connected to a SMA connector, and the information of all the components is stored in a database for a later treatment.

2. Generation of PLFs from first to n^{th} order by using the previous database. This generation is performed by computing the combined S parameters of the different component networks. In order to ensure that the optimal PLF is found, all possible combinations are considered. Therefore, the first-order PLFs are composed by only one of the component networks, which consists of either a CMC, a X capacitor or two Y capacitors (figure

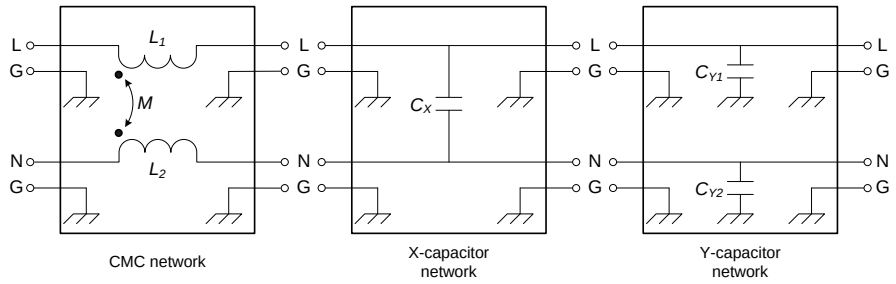

Figure 6.1: Block diagram of the implementation of CMC, X-capacitor and Y-capacitor networks.

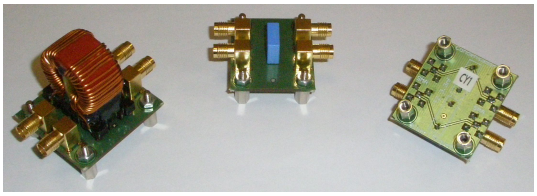

Figure 6.2: CMCs and capacitors placed in individual boards.

6.3(a)). The PLFs of second order are obtained joining the S parameters of two networks in cascade (figure 6.3(b)). The PLFs of n^{th} order are obtained joining the S parameters of n networks in cascade (figure 6.3(c)).

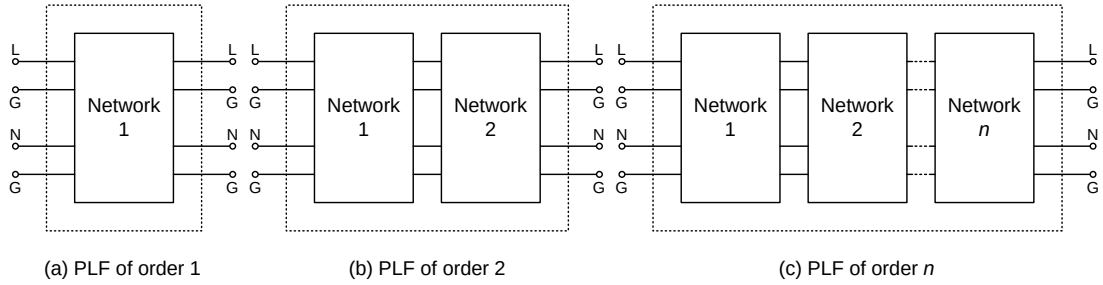

Figure 6.3: Block diagram of the PLF implementation: (a) PLF of order 1; (b) PLF of order 2; (c) PLF of order n.

3. Characterization of the DUT as it was explained in chapter 3.

4. Characterization of the line impedance stabilization network (LISN) as it was explained in chapter 2. If the predicted conducted emissions levels in a real power-line network (PLN) are desired, the PLN can be characterized as it was explained in chapter 3.

5. Prediction of the circuit and modal conducted emission levels of the DUT connected to each PLF, as seen in figure 6.4 and 6.5 respectively. The computation of the conducted emissions with the possible combinations generated before, allows the choice of the best PLF according to the designer restrictions.

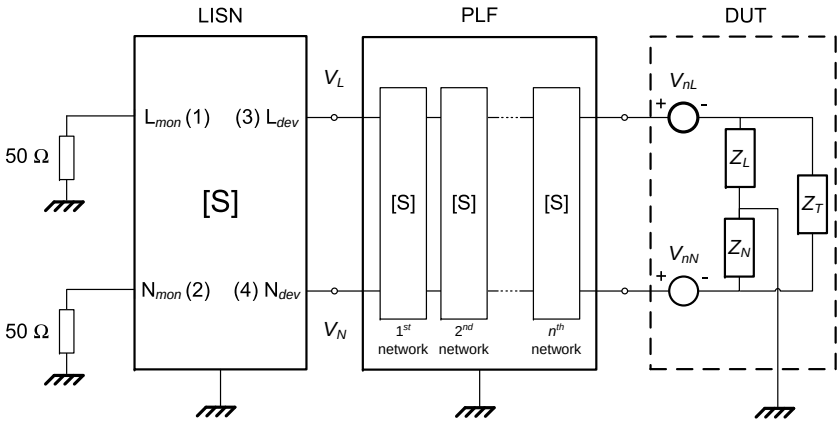

Figure 6.4: Block diagram for the simulation of the circuit conducted emissions of a DUT connected to a PLF of n^{th} order.

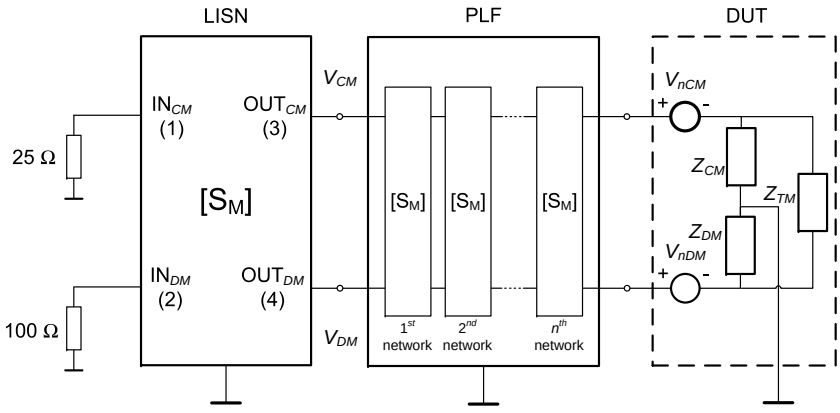

Figure 6.5: Block diagram for the simulation of the modal conducted emissions of a DUT connected to a PLF of n^{th} order.

X-capacitor values [nF]							
10	15	22	33	47	68	100	220

Table 6.1: Measured X-capacitor networks for the PLF design methodology.

Y-capacitor values [nF]					
1.5	2.2	3.3	4.7	6.8	10

Table 6.2: Measured Y-capacitor networks for the PLF design methodology.

6. Once the optimal PLF is obtained by computation, it can be implemented by joining its actual components. Figure 6.6 shows an example of a PLF composed by a X-capacitor, a CMC and a Y-capacitor network.

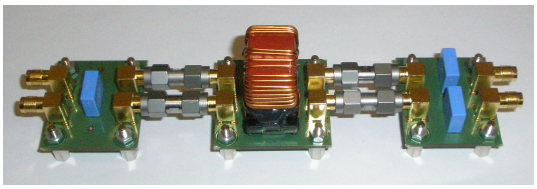

Figure 6.6: Connection of three different components to build a complete PLF.

6.3 Experimental validation

6.3.1 PLF design for a switching power supply with stationary noise

This section analyzes in detail each step of the PLF design methodology.

1. The S parameters of several networks composed by X capacitors (one capacitor per net, with the values shown in table 6.1), Y capacitors (two capacitors per net, with the values shown in table 6.2), and CMCs (one CMC per net, with the values shown in table 6.3) have been measured. Figures 6.7, 6.8 and 6.9 show the circuit and modal S parameters of three examples: a network composed by a X capacitor of 100 nF (which only affects the DM), a network composed by two Y capacitors of 3.3 nF (which affects both the CM and DM beyond 1 MHz) and a network composed by a CMC of 10 mH (which mainly affects the CM, but there is also an attenuation on the DM due to the leakage flux) respectively.

2. The component networks measured before have been used to generate all possible PLFs from first to third order by computing their combined S parameters. As an example, figure 6.10 shows the S parameters of a third-order PLF composed by the X-capacitor,

CMC values [mH]					
1	2.2	3.3	5	10	20

Table 6.3: Measured CMC networks for the PLF design methodology.

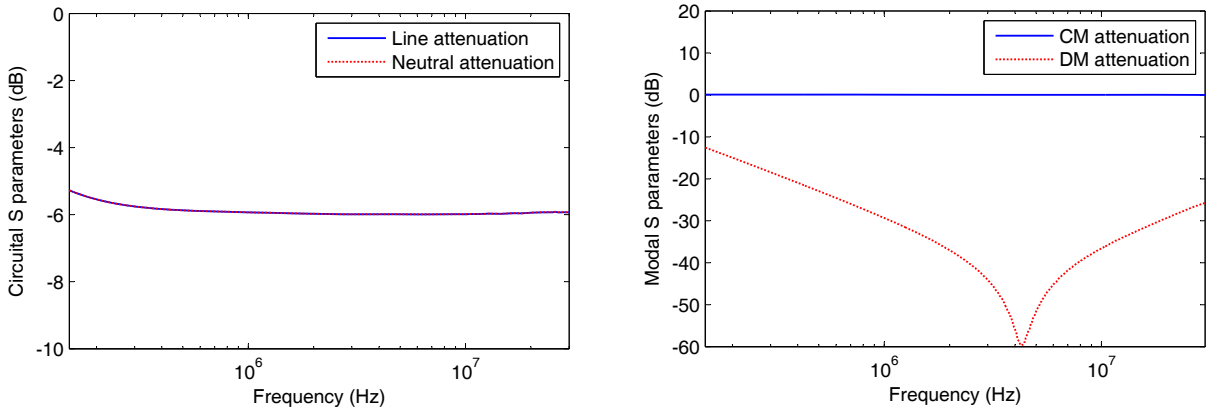

Figure 6.7: Circuit and modal S parameters of a network composed by a X capacitor of 100 nF.

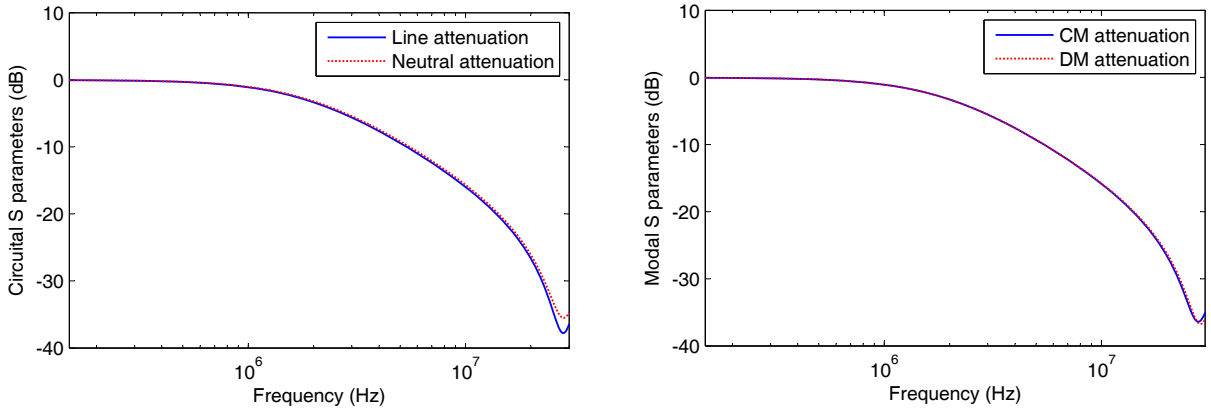

Figure 6.8: Circuit and modal S parameters of a network composed by two Y capacitors of 3.3 nF.

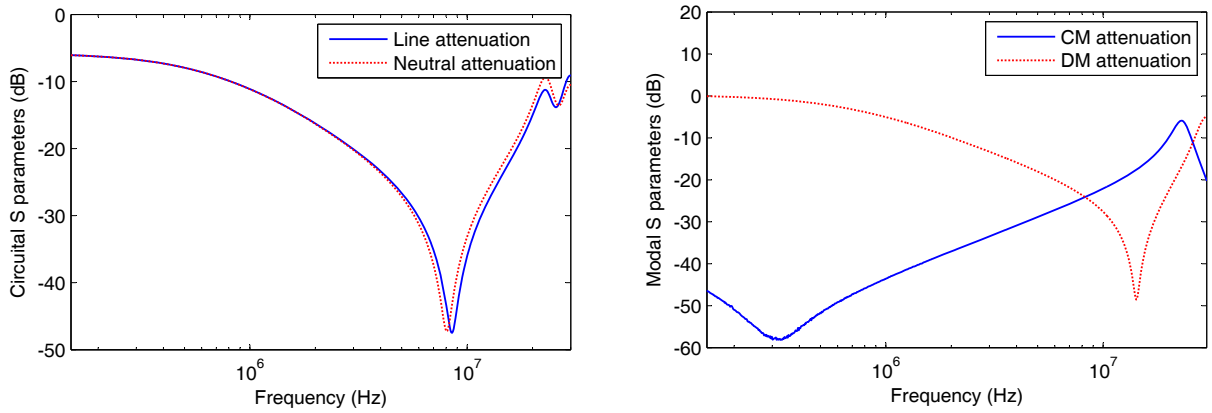

Figure 6.9: Circuit and modal S parameters of a network composed by a CMC of 10 mH.

Y-capacitor and CMC networks shown separately before. The combined effect of the three components present an strong attenuation on both CM and DM.

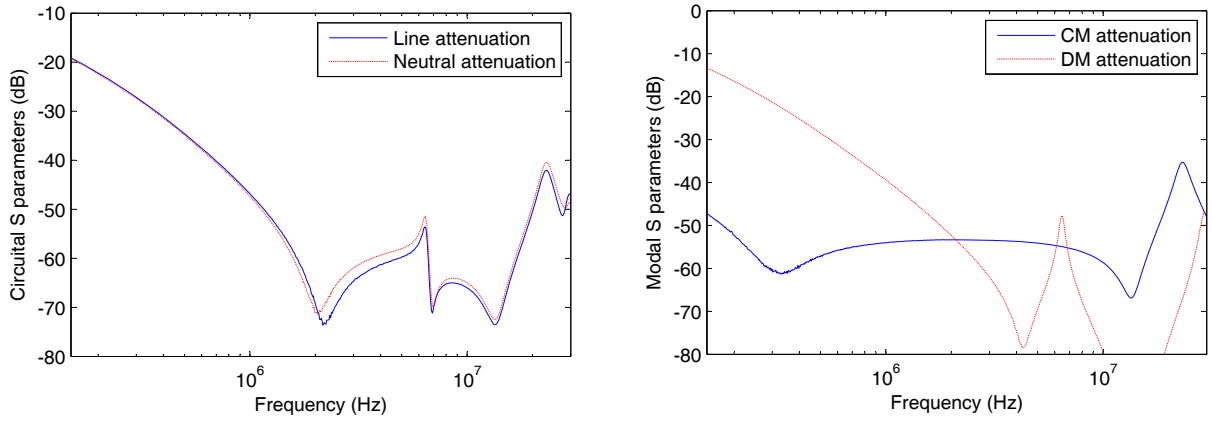

Figure 6.10: Circuit and modal S parameters of a PLF composed by a X capacitor of 100 nF, two Y capacitors of 3.3 nF and a CMC of 10 mH.

3. The DUT characterized and used for the validation is a switching power supply that feeds a microcontroller with a 4 MHz clock (figure 6.11). Figure 6.12 shows its circuit conducted emissions V_L and V_N measured according to [11]. As can be seen, the conducted emissions exceed the quasi-peak limit for class B devices established in [11].

   The modal conducted emissions V_{CM} and V_{DM} have been computed using (1.1) and compared with the circuit limit in figure 6.13 for guidance only (since there is no limit for the modal conducted emissions). Both modal components contain the 4-MHz clock and exceed the circuit limit in a wide frequency range.

4. Figure 6.14 shows the circuit and modal S parameters of the LISN. An attenuation of 10 dB due to the effect of the transient suppressors is shown.

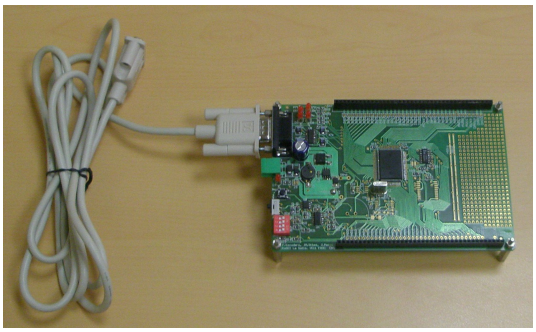

Figure 6.11: Microcontroller with a 4 MHz clock used to validate the PLF design methodology.

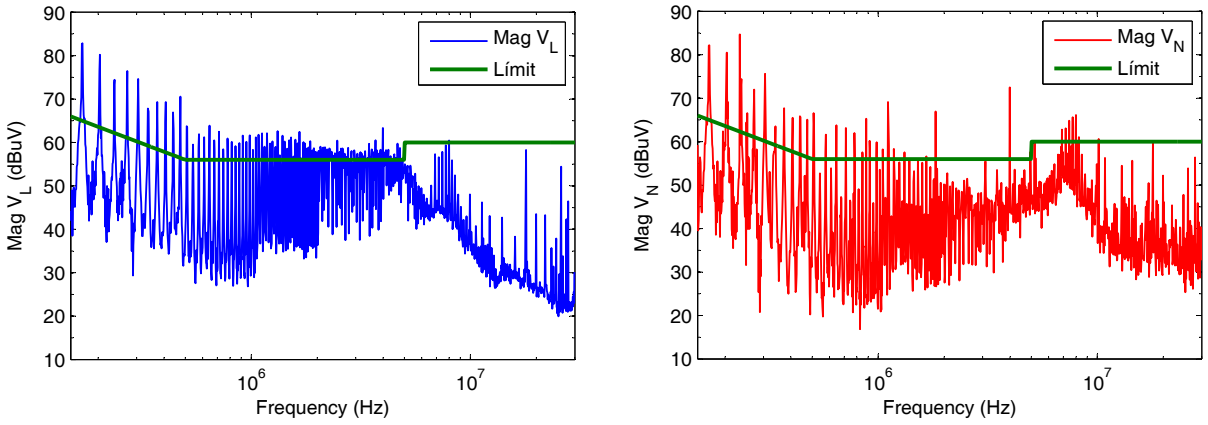

Figure 6.12: Circuit conducted emissions V_L and V_N of the switching power supply without any PLF.

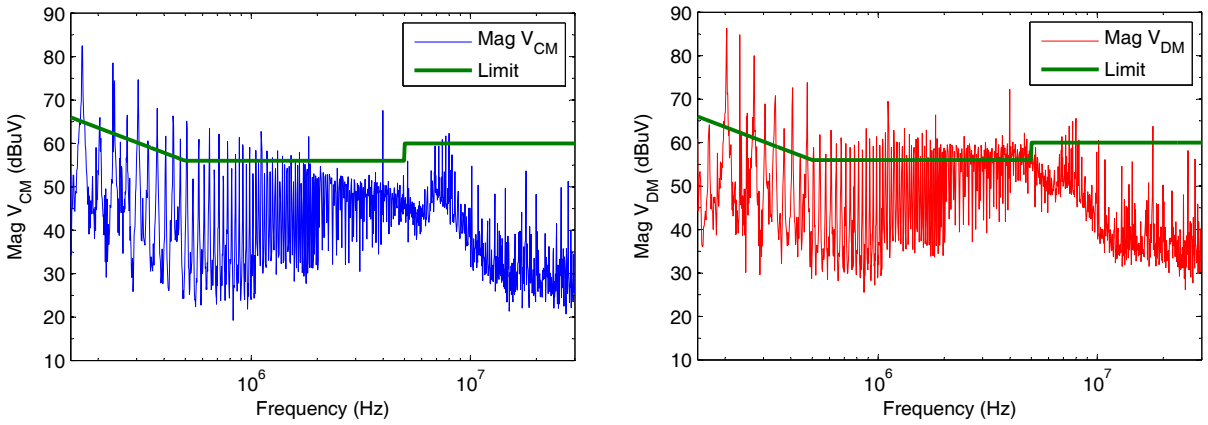

Figure 6.13: Modal conducted emissions V_{CM} and V_{DM} of the switching power supply without any PLF.

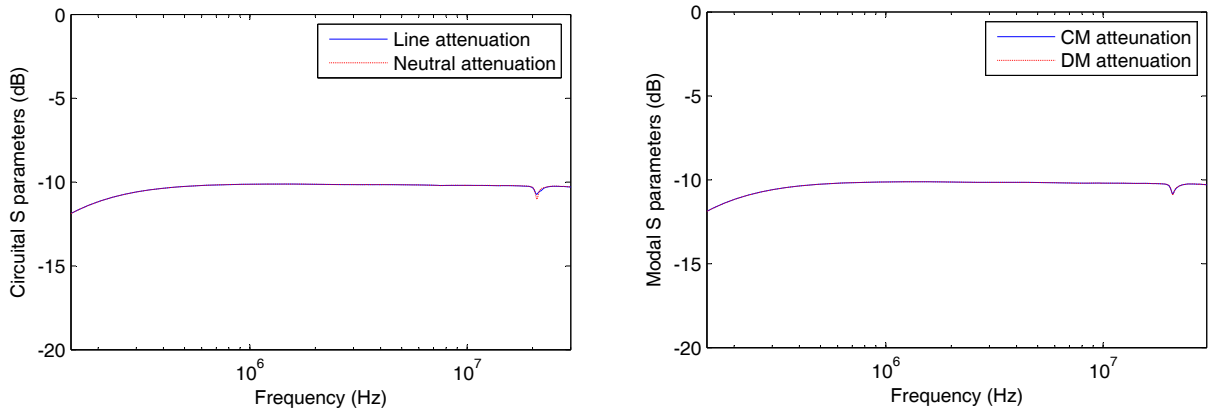

Figure 6.14: Circuit and modal S parameters of the LISN.

5. The predictions of the conducted emissions of the switching power supply with all the PLFs generated in step 2 are realized. Figure 6.15 shows the circuit conducted emissions of the DUT connected to a first-order PLF composed by a CMC of 10 mH. As can be seen, this PLF does not mitigate the conducted emissions under the circuit limit and it can be discarded as a possible PLF. On the other hand, figure 6.16 shows the circuit conducted emissions of the DUT connected to a third-order PLF composed by a X capacitor of 100 nF, two Y capacitors of 3.3 nF and a CMC of 10 mH. This is one of the possible PLFs since it attenuates the interference levels of the DUT under the limit.

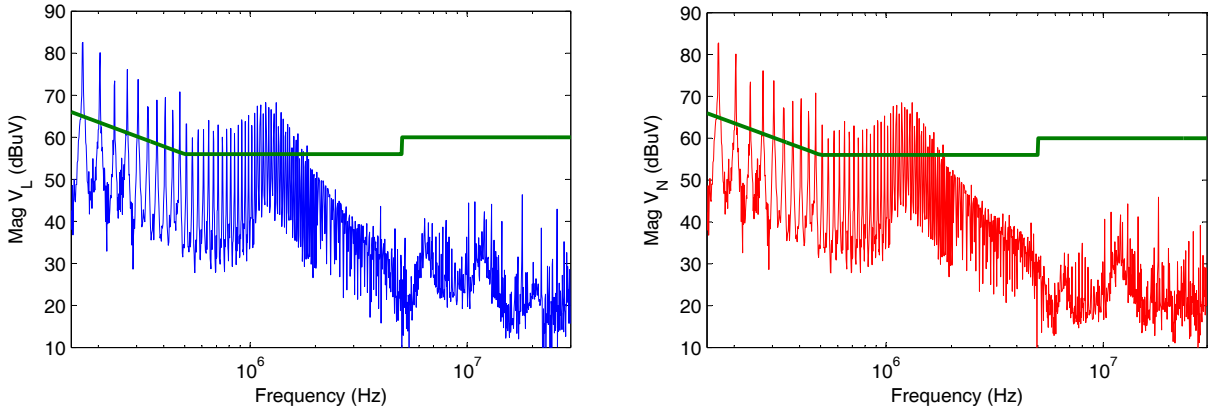

Figure 6.15: Circuit conducted emissions V_L and V_N of the switching power supply with a first-order PLF composed by a CMC of 10 mH.

After performing the predictions of the DUT with all possible combinations, the results obtained can be used to analyze which PLF is the most interesting for the designer purposes. In this case, the optimal PLF has been selected in accordance with its price, that is, the cheapest PLF that reduces the circuit conducted emissions under the limit. After considering this parameter, the optimal PLF obtained by the methodology is composed

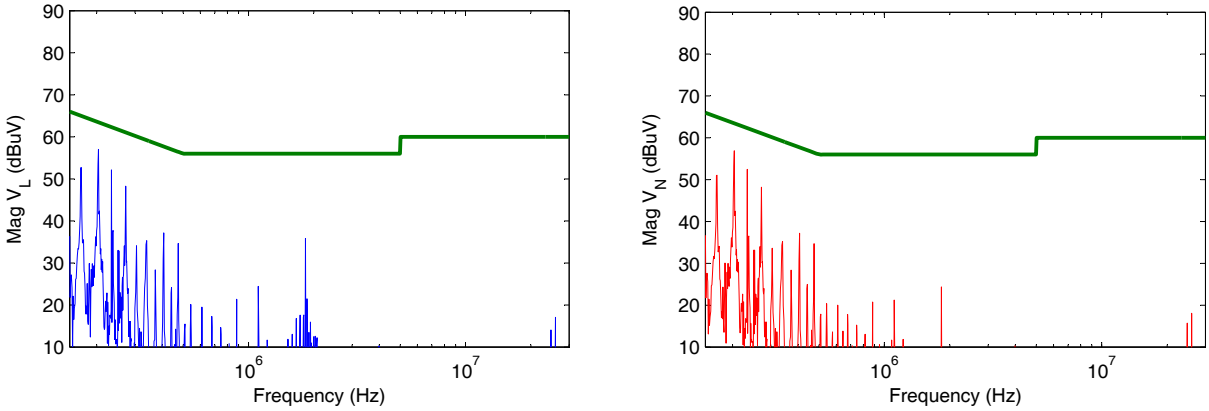

Figure 6.16: Circuit conducted emissions V_L and V_N of the switching power supply with a third-order PLF composed by a X capacitor of 100 nF, two Y capacitors of 3.3 nF and a CMC of 10 mH.

by a CMC of 20 mH and a X capacitor of 100 nF, as seen in figure 6.17. As the PLF of figure 6.16, this one attenuates the interference levels under the limit. However, it does not need the Y-capacitor network and, therefore, is cheaper.

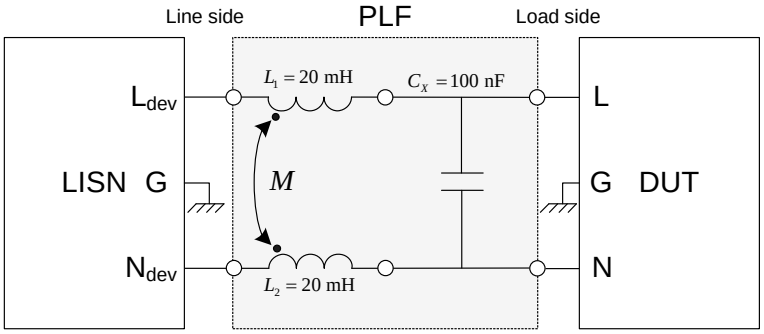

Figure 6.17: Structure of the optimal PLF obtained with the design methodology.

6. The optimal PLF obtained in step 5 has been implemented and connected to the DUT. Figure 6.18 shows the predicted and measured circuit conducted emissions of the set DUT plus PLF. The good agreement between them corroborates that it is possible to design the PLF from the S-parameter measurements of its individual components and reduce the conducted emissions under the limit with a PLF optimized in terms of cost.

   Figure 6.19 shows the predicted and measured modal conducted emissions of the set DUT plus PLF (the circuit limit has also been plotted for guidance). Between the 150 kHz and the 300 kHz, the DM presents more energy, since the attenuation on the DM introduced by the low impedance of the X capacitor is lower than the one on the CM introduced by the high impedance of the CMC, which is attenuated under the 40 dBμV. Over the 4 MHz the CM becomes predominant. At those frequencies, the parasitic capacities between the CMC coils degrades the effect of the CMC on the CM, while the X capacitor

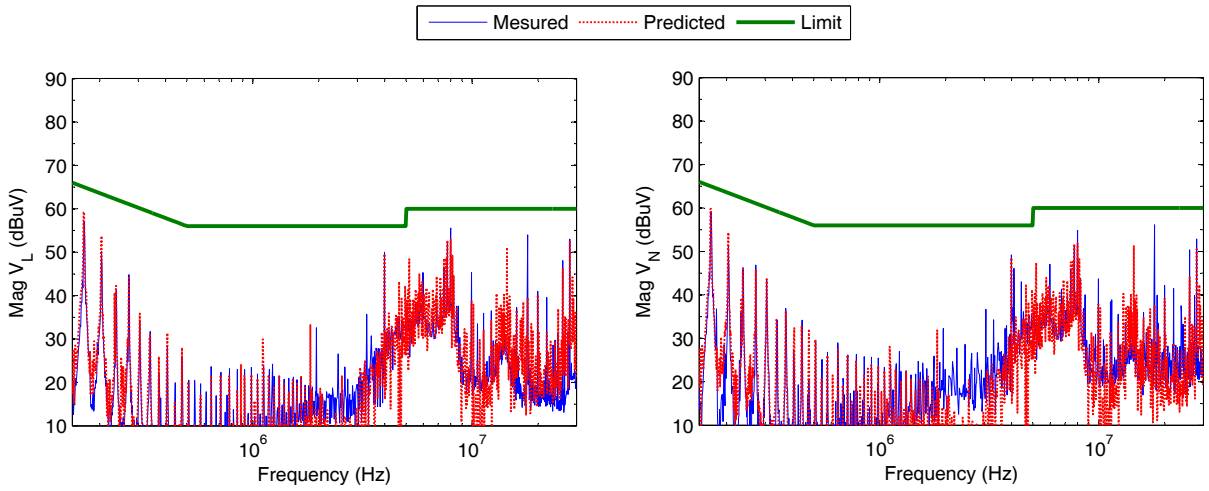

Figure 6.18: Circuit conducted emissions V_L and V_N of the switching power supply with a PLF composed by a CMC of 20 mH and a X capacitor of 100 nF.

is still decreasing its impedance inversely proportional to the frequency and increasing its attenuation on the DM.

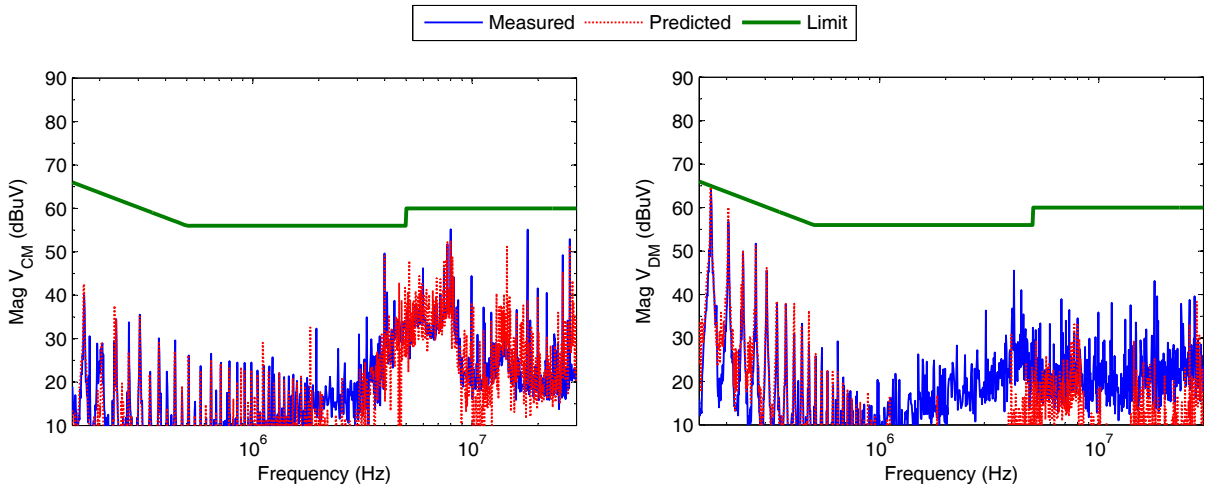

Figure 6.19: Modal conducted emissions V_{CM} and V_{DM} of the switching power supply with a PLF composed by a CMC of 20 mH and a X capacitor of 100 nF.

The PLF presented above has been designed to mitigate the conducted emissions just under the limit. However, the uncertainty in the conducted emission levels motivated by weaknesses of [11] can cause variations in these levels when the measurements are repeated in different laboratories (differences in the laboratory facilities, in the position of the device and in the length and folding of the power-line cable, [128]–[133]). In order guarantee that the conducted emissions of the DUT are under the limit wherever the measurements are performed, it is a usual practice to adjust the methodology with a security margin of some dB [55].

6.3.2 Filtering comparison with a different component position

The position of the different components in the PLF is not trivial, since different positions can lead to important variations of the conducted emission levels. To show this effect, the PLF of figure 6.17 has been modified by swapping the two components, as seen in figure 6.20. Figure 6.21 compares the circuit conducted emissions measured with the two PLF configurations. As can be seen, both PLF, that are composed by the same components but in a different position, present different attenuations on the conducted emissions of the switching power supply. With the swapped filter the emissions at the frequency of 170 kHz are over the limit, and at the frequency of 650 kHz there is a difference of about 30 dB with regard to the first PLF. Therefore, the methodology presented to design the PLF by computing all possible configurations improves those techniques based on fixed PLF structures [49]–[53], [57], [58].

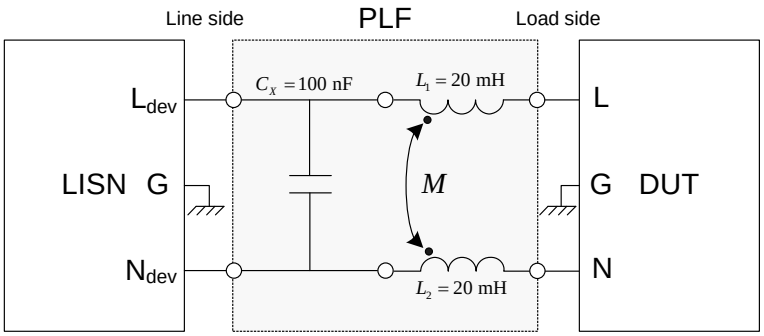

Figure 6.20: Structure of the swapped PLF.

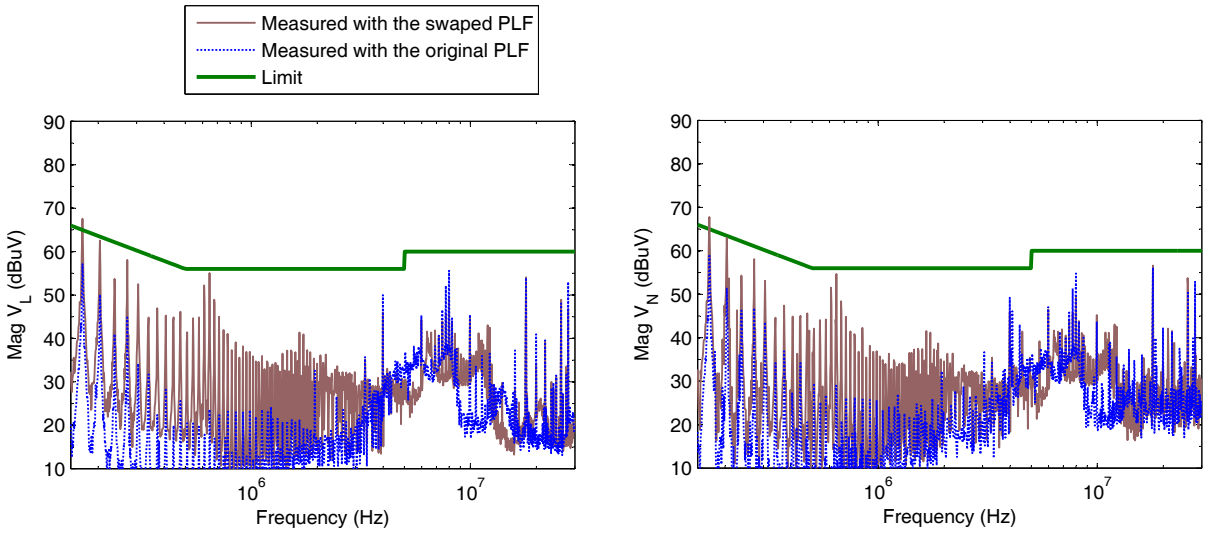

Figure 6.21: Circuit conducted emissions V_L and V_N of the switching power supply with the original and the swapped PLF, both composed by a X capacitor of 100 nF and a CMC of 20 mH.

6.3.3 PLF design for a switching power supply with non-stationary noise

The same methodology can be applied to the switching power supply of chapter 4, which conducted emissions, measured in time domain, were characterized by the presence of impulsive noise (figure 4.11). Figure 6.22 shows the circuit and modal conducted emissions of the switching power supply compared with the quasi-peak limit for class B devices established in [11]. As can be seen, the circuit conducted emissions are over the limit and they are mainly dominated by the DM, which means that the PLF has to be designed to mitigate this mode. The PLF obtained after applying the design methodology is shown in figure 6.23, and, as expected, it is exclusively composed by a X capacitor of 100 nF.

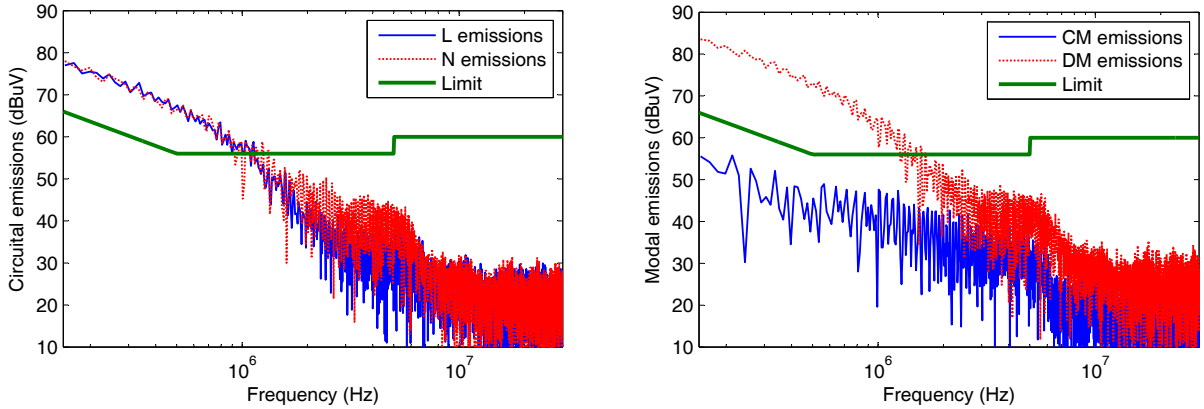

Figure 6.22: Circuit and modal conducted emissions of the switching power supply with non-stationary noise.

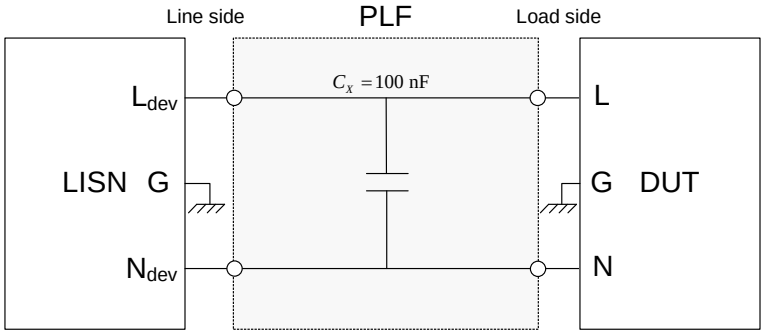

Figure 6.23: Structure of the PLF designed by the methodology.

Figure 6.24 shows the comparison between the predicted and measured circuit conducted emissions of the switching power supply connected to the PLF of figure 6.23. As can be seen, the predicted emissions are similar to the measured ones, which proves that it is possible to design a suitable PLF for a DUT with impulsive emissions using the methodology proposed in this chapter.

Figure 6.25 shows the prediction of the modal conducted emissions of the switching power

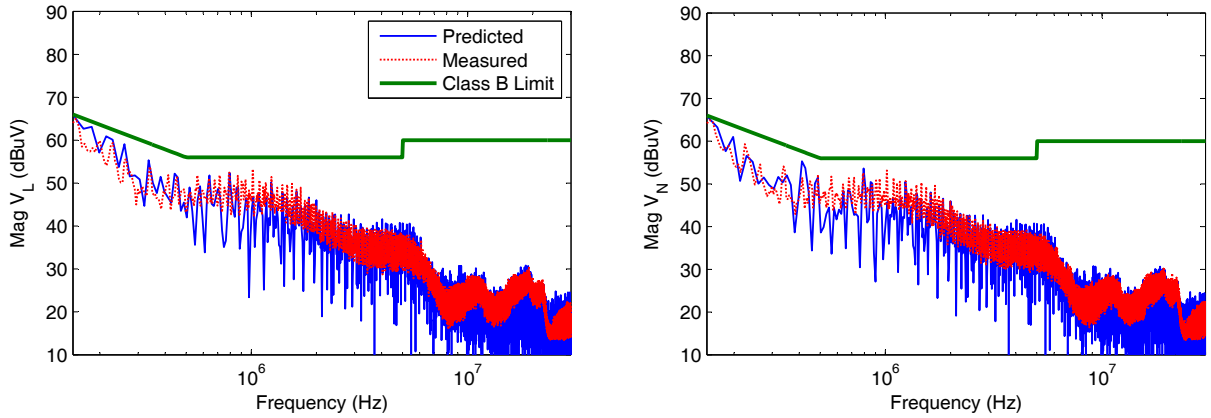

Figure 6.24: Comparison between the predicted and measured circuit conducted emissions of the switching power supply connected to the PLF of figure 6.23.

supply connected to the PLF of figure 6.23 (the circuit limit has also been plotted for guidance). The CM emissions are similar to the ones of figure 6.22, since a X capacitor placed between L and N terminals does not affect this mode, but the DM emissions are considerably reduced. Even though the DM is over the limit for class B devices under 200 kHz, the circuit values (V_L and V_N) which are composed by the combination of this mode with the CM, are under the limit.

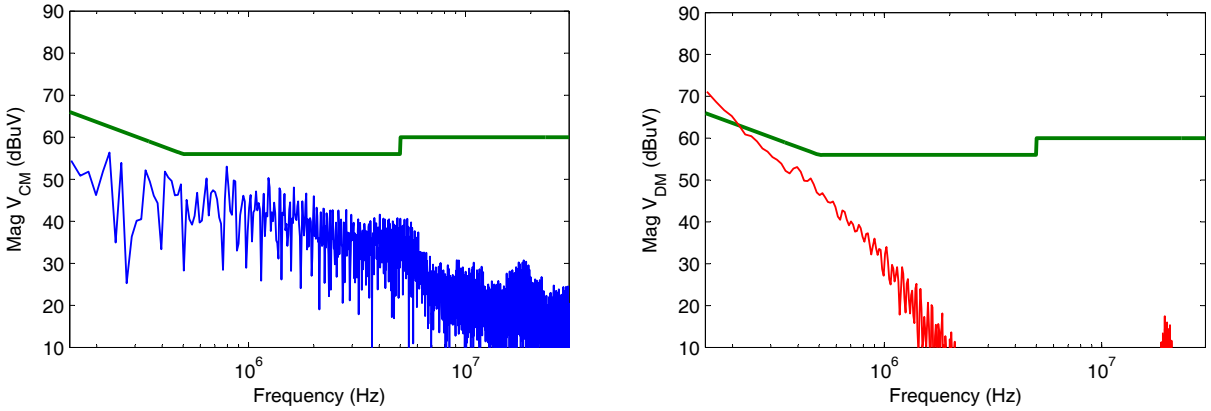

Figure 6.25: Prediction of the modal conducted emissions of the switching power supply connected to the PLF of figure 6.23.

Chapter 7

Power-Line Filter Design Using Mode Conversion

Contents of this chapter

7.1 Introduction

The methodology of the previous chapter was useful to design power-line filters (PLFs) using the classical symmetric structure, that is, an structure that avoids mode conversion. This structure has been proven to be efficient for the common-mode (CM) and differential-mode (DM) filtering, and the efforts to optimize the effect of a PLF are usually performed preserving this symmetry. For instance, the use of nanocrystalline material for the common-mode choke (CMC) core is proposed in [134] because of the good relationship between permeability and saturation. A model that predicts and optimizes the leakage flux in the core to increase the DM attenuation in a CMC by choosing the appropriate core material is presented in [122], and the use of a magnetically permeable bypass for the same purpose is suggested in [135].

However, a different point of view to optimize the PLF capabilities is arisen in this chapter: instead of using the classical symmetric structure, asymmetries are introduced in the circuit to produce mode conversion. Mode conversion is an energy exchange between CM and DM, and the objective is to determine whether this conversion can be used, for instance, to reduce the dominant mode of a conducted-emissions problem using fewer or smaller components than in a symmetric PLF. This point of view applied on the design of PLFs is completely novel since no previous references about this particular topic have been found in the literature.

Before focusing on the modal conversion effect, a new modeling methodology to characterize the modal behavior of the components of a PLF is needed, since even though the modal S parameters, presented in chapter 2, are useful to predict the overall effect of mode conversion, they do not reveal the causes of its generation. In order to achieve a deep understanding of the modal interference propagation in a PLF, two modal models to characterize two-port networks shunt- and series-connected to the power-line terminals are proposed in the second and third sections of this chapter. These models can be particularized to characterize, among others, networks composed by CMCs, X and Y capacitors placed in the power-line terminals. In the fourth section the models are used to determine how asymmetries can affect the interference propagation when they are placed between a synthetic device under test (DUT) and a power-line network (PLN). In the fifth section, the results of a genetic algorithm (GA) designed to find the optimal values of the components of a PLF are presented. Although the values obtained with this algorithm are the values of ideal components, they can be used to know if mode conversion is desirable or not in the actual implementation. Finally, in the sixth section, the modal models of capacitors and CMCs are experimentally validated with real measurements and they are used to predict the conducted emissions of an actual DUT and to optimize the

filtering of its PLF.

7.2 Modal characterization of PLF capacitors

7.2.1 Characterization of a shunt-connected two-port network

A generic two-port network shunt-connected to the line (L), neutral (N) and ground (G) terminals can be seen in figure 7.1 (G is the ground of the measurement system) [136]. The voltages and currents at the terminal ports of the network are $V_{IL} = V_{OL}$, $V_{IN} = V_{ON}$, $I_{IL} = -I_{OL}$ and $I_{IN} = -I_{ON}$. The two-port network can be mathematically characterized, for instance, by its Z parameters:

$$\begin{aligned} V_1 &= Z_{11}I_1 + Z_{12}I_2 \\ V_2 &= Z_{21}I_1 + Z_{22}I_2 \end{aligned} \tag{7.1}$$

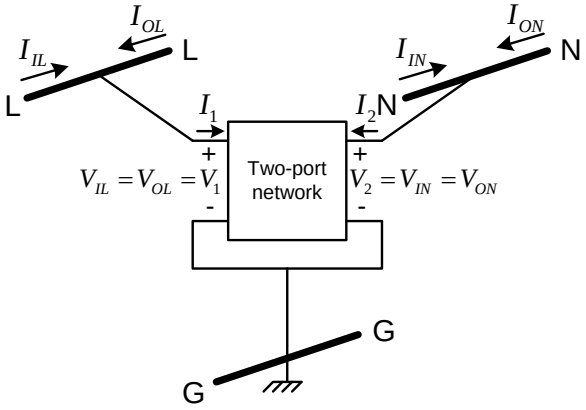

Figure 7.1: Impedance network connected to L, N and G terminals.

Using (7.1) and analyzing the circuit of figure 7.1, the equations that completely characterize its behavior are obtained:

$$\begin{aligned} V_{IL} = V_{OL} &= Z_{11}(I_{IL} + I_{OL}) + Z_{12}(I_{IN} + I_{ON}) \\ V_{IN} = V_{ON} &= Z_{21}(I_{IL} + I_{OL}) + Z_{22}(I_{IN} + I_{ON}) \end{aligned} \tag{7.2}$$

Combining (1.1) and (7.2), the equations that characterize the modal behavior of the impedance network of figure 7.1 can be obtained as:

$$\begin{aligned} \frac{V_{ID}}{\sqrt{2}} &= \left(\frac{I_{IC}}{\sqrt{2}} + \frac{I_{OC}}{\sqrt{2}}\right)\left(\frac{Z_{11} - Z_{22}}{2}\right) + \left(\sqrt{2}I_{ID} + \sqrt{2}I_{OD}\right)\left(\frac{Z_{11} + Z_{22} - 2Z_{12}}{2}\right) \\ \sqrt{2}V_{IC} &= \left(\frac{I_{IC}}{\sqrt{2}} + \frac{I_{OC}}{\sqrt{2}}\right)\left(\frac{Z_{11} + Z_{22} + 2Z_{12}}{2}\right) + \left(\sqrt{2}I_{ID} + \sqrt{2}I_{OD}\right)\left(\frac{Z_{11} - Z_{22}}{2}\right) \end{aligned} \tag{7.3}$$

A modal model for the generic circuit of figure 7.1 has to split each mode into a different port and its behavior has to be described by (7.3). This model can be obtained by a generalization of the modal model for asymmetric shunt impedances presented in [137], and it is shown in figure 7.2. It is composed by two equal impedance networks with their terminals connected between the CM and DM paths, and splits the contribution of each mode into a different port (namely, input CM into port 1, input DM into port 2, output CM into port 3 and output DM into port 4). Its structure allows a simple interpretation of the modal energy propagation: an interaction between CM and DM can exist, and this interaction is determined by the two impedance networks that connect the CM path to the DM path.

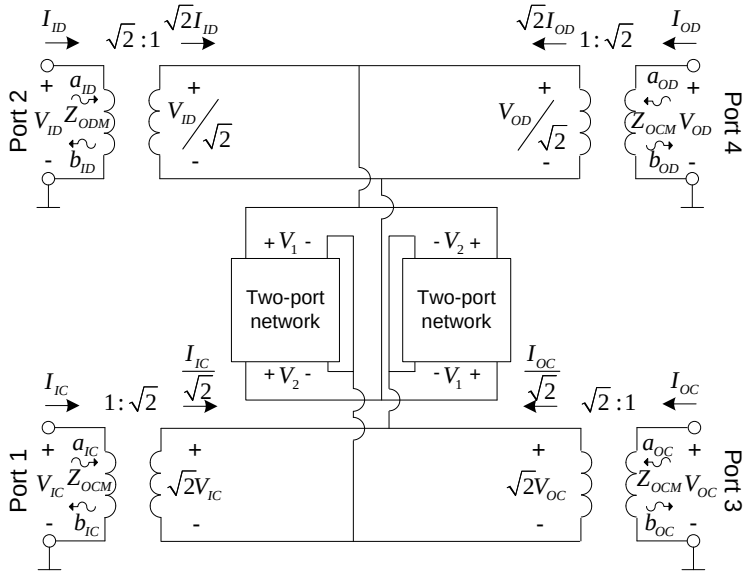

Figure 7.2: Modal model of a shunt-connected two-port network.

By analyzing the modal model of figure 7.2, its modal S-parameter matrix can be obtained as:

$$\begin{bmatrix} b_{IC} \\ b_{ID} \\ b_{OC} \\ b_{OD} \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} \alpha & \beta & \chi & \beta \\ \beta & \delta & \beta & \chi \\ \chi & \beta & \alpha & \beta \\ \beta & \chi & \beta & \delta \end{bmatrix} \begin{bmatrix} a_{IC} \\ a_{ID} \\ a_{OC} \\ a_{OD} \end{bmatrix} \tag{7.4}$$

where

$$\begin{aligned} \alpha &= -4Z_{0CM}\left(Z_{11}+Z_{22}-2Z_{12}\right)-2Z_{0CM}Z_{0DM} \\ \beta &= 2\sqrt{Z_{0CM}Z_{0DM}}\left(Z_{11}-Z_{22}\right) \\ \chi &= 8Z_{11}Z_{22}-8Z_{12}^2+Z_{0DM}\left(Z_{11}+Z_{22}+2Z_{12}\right) \\ \delta &= -Z_{0DM}\left(Z_{11}+Z_{22}+2Z_{12}\right)-2Z_{0CM}Z_{0DM} \\ \Delta &= 8Z_{11}Z_{22}-8Z_{12}^2+4Z_{0CM}\left(Z_{11}+Z_{22}-2Z_{12}\right)+ \\ &+Z_{0DM}\left(Z_{11}+Z_{22}+2Z_{12}\right)+2Z_{0CM}Z_{0DM} \end{aligned} \tag{7.5}$$

The reference impedance for the CM (port 1 and port 3) is Z_{0CM} and the reference impedance for the DM (port 2 and port 4) is Z_{0DM}. From the S-parameter matrix it can be concluded that mode conversion from CM to DM and vice versa is produced by the parameter β/Δ. If Z_{11} is different from Z_{22}, mode conversion will take place in the circuit.

The generic model of figure 7.1 can be adapted, among others, to the capacitor impedance networks commonly found in a PLF, such as X capacitor networks and Y capacitors networks, or to less used capacitor impedance network topologies such as an star capacitor network. Therefore, their respective modal models can be found with the modal model of figure 7.2.

7.2.2 X capacitor network

A X capacitor network is composed by a X capacitor placed between the L and N terminals with an impedance Z_{CX}, as can be seen in figure 7.3(a). The modal model of this network is shown in figure 7.3(b), and can be further simplified into the circuit of figure 7.3(c). As expected, a network composed by a X capacitor between L and N terminals has influence only on the DM. The CM remains unaffected by the X capacitor.

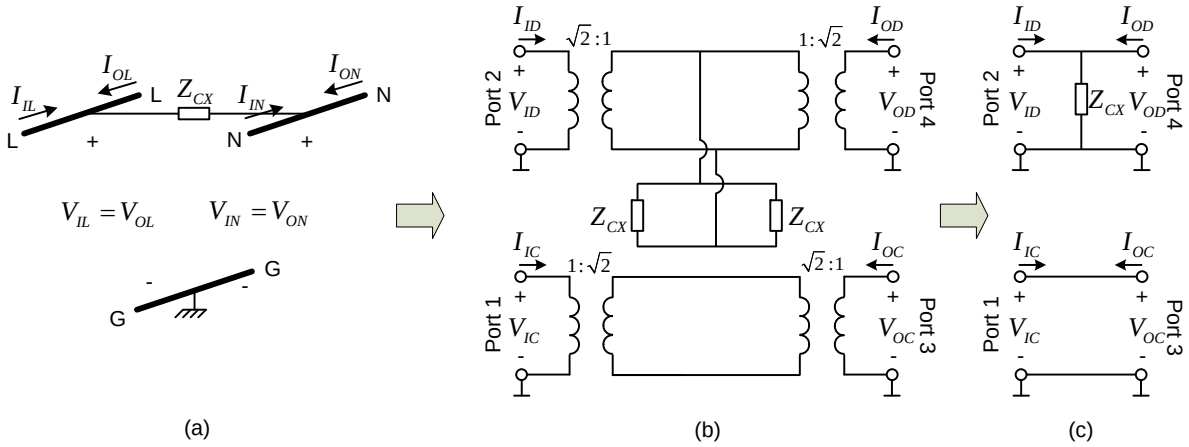

Figure 7.3: Models for X capacitor networks: (a) Circuit model. (b) Full modal model. (c) Simplified modal model.

7.2.3 Y capacitors network

A Y capacitor network is composed by two Y capacitors placed between L and G terminals, and between N and G terminals, with impedances Z_{CY1} and Z_{CY2}, as seen in figure 7.4(a). The Y capacitors have influence on both CM and DM, and their equivalent modal model is shown in figure 7.4(b). As can be seen, a connection between CM and DM is produced by the impedance bridge composed by the Z_{CY1} and Z_{CY2} capacitors. It is apparent from figure 7.4(b) that when $Z_{CY1} \neq Z_{CY2}$ the impedance bridge is unbalanced and mode conversion takes place.

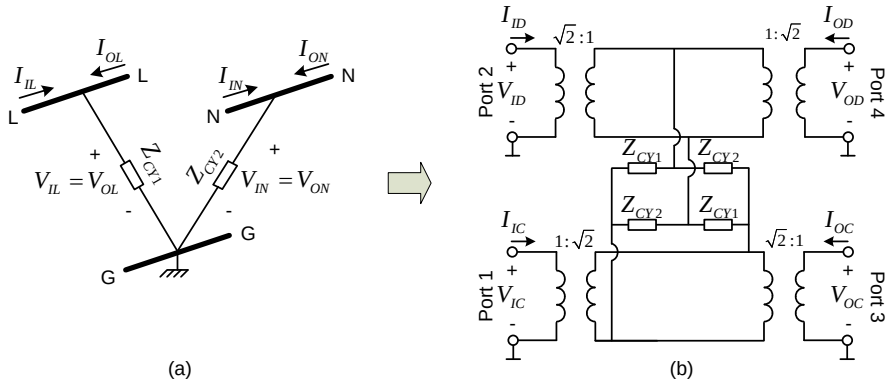

Figure 7.4: Models for Y capacitor networks: (a) Circuit model. (b) Modal model.

7.2.4 Star Capacitor Network

Although PLFs are usually composed by the X and Y capacitor topologies, the generic model of figure 7.2 can also be applied to less frequent topologies such as the star capacitor network, as seen in figure 7.5(a). Its equivalent modal model can be seen in figure 7.5(b). As can be expected, if $Z_{C3} \rightarrow 0$ the modal model for Y capacitors is recovered, whereas if $Z_{C3} \rightarrow \infty$ the modal model for X-class capacitors is obtained.

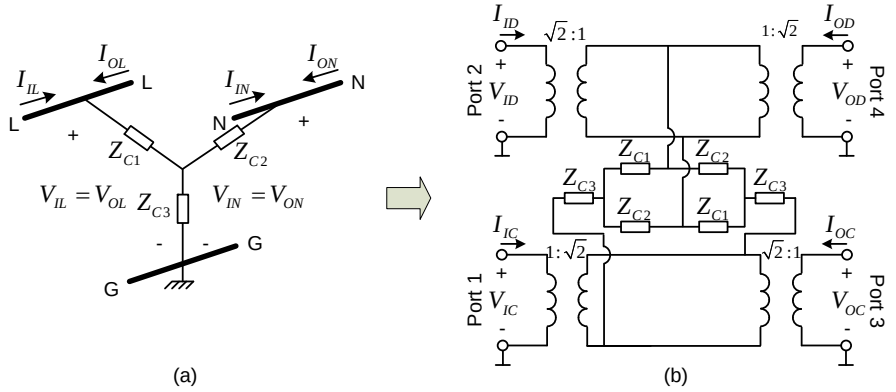

Figure 7.5: Models for star capacitor networks: (a) Circuit model. (b) Modal model.

7.3 Modal characterization of CMCs

7.3.1 Characterization of a series-connected two-port network

A similar procedure can be applied to a generic two-port network series-connected to the L and N terminals, as seen in figure 7.6 [138]. The voltages and currents in the terminals of this network are $V_{IL} = V_{OL}$, $V_{IN} = V_{ON}$, $I_{IL} = -I_{OL}$ and $I_{IN} = -I_{ON}$. This network can be mathematically characterized, for instance, by its Z parameters, as defined in equation (7.1).

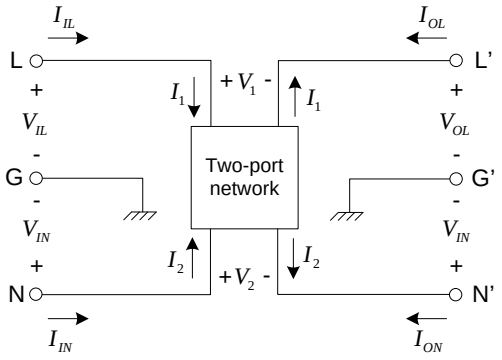

Figure 7.6: Two-port network series-connected to the L and N terminals.

Analyzing the circuit of figure 7.6 and using (7.1), the following equations are obtained:

$$\begin{aligned} V_{IL} - V_{OL} &= Z_{11} I_{IL} + Z_{12} I_{IN} \\ V_{IN} - V_{ON} &= Z_{21} I_{IL} + Z_{22} I_{IN} \end{aligned} \tag{7.6}$$

Combining (1.1) and (7.6), the equations that characterize the modal behavior of the circuit of figure 7.6 are found:

$$\begin{aligned} \frac{V_{ID}}{\sqrt{2}} - \frac{V_{OD}}{\sqrt{2}} &= \frac{I_{IC}}{\sqrt{2}} \left(\frac{Z_{11} - Z_{22}}{2} \right) + \sqrt{2} I_{ID} \left(\frac{Z_{11} + Z_{22} - 2Z_{12}}{2} \right) \\ \sqrt{2} V_{IC} - \sqrt{2} V_{OC} &= \frac{I_{IC}}{\sqrt{2}} \left(\frac{Z_{11} + Z_{22} + 2Z_{12}}{2} \right) + \sqrt{2} I_{ID} \left(\frac{Z_{11} - Z_{22}}{2} \right) \end{aligned} \tag{7.7}$$

A modal model for the generic circuit of figure 7.6, which splits each mode into a different port, has to be described by (7.7). This model can be obtained as a generalization of the modal model for asymmetric series-impedances presented in [139], and it is shown in figure 7.7. This structure allows a simple interpretation of the modal propagation: in particular, an interaction between CM and DM can exist through the two-port networks that connect the CM path to the DM path. As can be seen, this connection is different from the one present in the modal model of figure 7.2.

By analyzing the modal model of figure 7.7, its modal S-parameter matrix can be obtained:

$$\begin{bmatrix} b_{IC} \\ b_{ID} \\ b_{OC} \\ b_{OD} \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} \alpha & \beta & \chi & -\beta \\ \beta & \delta & -\beta & \varepsilon \\ \chi & -\beta & \alpha & \beta \\ -\beta & \varepsilon & \beta & \delta \end{bmatrix} \begin{bmatrix} a_{IC} \\ a_{ID} \\ a_{OC} \\ a_{OD} \end{bmatrix} \tag{7.8}$$

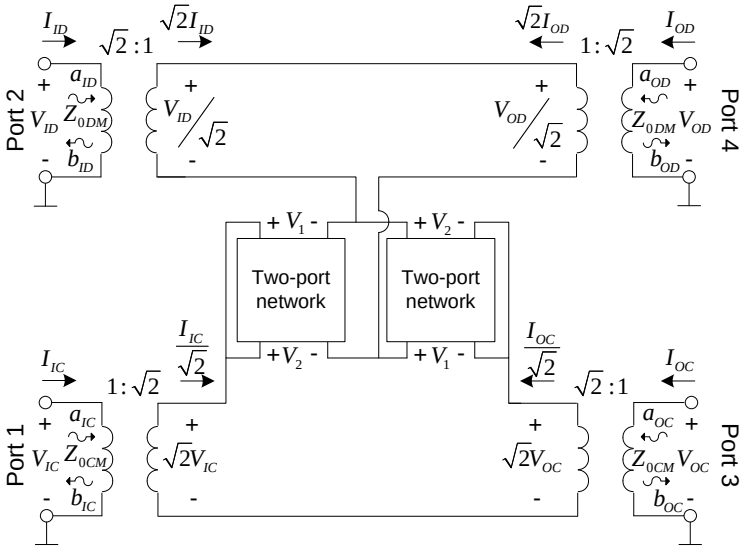

Figure 7.7: Modal model of a series-connected two-port network.

where

$$
\begin{aligned}
\alpha &= 2Z_{11}Z_{22} - 2Z_{12}^2 + Z_{0DM}\left(Z_{11} + Z_{22} + 2Z_{12}\right), \\
\beta &= 2\sqrt{Z_{0CM}Z_{0DM}}\left(Z_{11} - Z_{22}\right), \\
\chi &= 4Z_{0CM}\left(Z_{11} + Z_{22} - 2Z_{12}\right) + 8Z_{0CM}Z_{0DM}, \\
\delta &= 2Z_{11}Z_{22} - 2Z_{12}^2 + 4Z_{0CM}\left(Z_{11} + Z_{22} - 2Z_{12}\right), \\
\varepsilon &= Z_{0DM}\left(Z_{11} + Z_{22} + 2Z_{12}\right) + 8Z_{0CM}Z_{0DM}, \\
\Delta &= 2Z_{11}Z_{22} - 2Z_{12}^2 + 4Z_{0CM}\left(Z_{11} + Z_{22} - 2Z_{12}\right) + \\
&+ Z_{0DM}\left(Z_{11} + Z_{22} + 2Z_{12}\right) + 8Z_{0CM}Z_{0DM}
\end{aligned}
\tag{7.9}
$$

As before, Z_{0CM} is the reference impedance for the CM (ports 1 and 3), and Z_{0DM} is the reference impedance for the DM (ports 2 and 4). From the S-parameter matrix it can be concluded that the mode conversion from CM to DM and vice versa is controlled by β/Δ. Whenever Z_{11} and Z_{22} are different, mode conversion takes place.

7.3.2 CMC network

The circuit model of figure 7.6 can be particularized to model an ideal CMC series-connected to the L and N terminals, as seen in figure 7.8(a), and its modal model extracted from figure 7.7, as seen in figure 7.8(b). As can be seen, the connection between CM and DM is controlled by the impedance bridge formed by L_1 and L_2; whenever $L_1 \neq L_2$, it becomes unbalanced and modal conversion takes place.

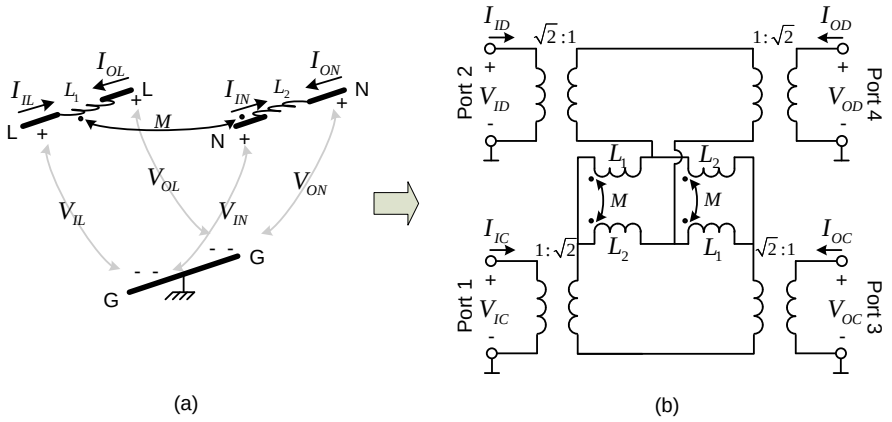

Figure 7.8: Ideal CMC series-connected to the L and N terminals (a) and its modal model (b).

7.4 Parametric study of the mode conversion

The mode conversion in a PLF can be expressly provoked by the addition of asymmetries in its Y capacitors ($C_{Y1} \neq C_{Y2}$) or in its CMC ($L_1 \neq L_2$), and used to improve its filtering capabilities. To show this effect, the conducted emissions of a test device connected to a PLF composed by capacitors first, and by a CMC later, have been simulated in order to compare their symmetrized and asymmetrized responses.

7.4.1 Simulations with ideal capacitors

To perform the study of the mode conversion in a PLF composed by ideal capacitor networks, the modal model of a generic DUT has been connected to the modal model of two ideal Y-class capacitors (figure 7.4(b)) and to the simplified modal model of an ideal X-class capacitor of $C_X = 22$ nF (figure 7.3(c)). Finally, the capacitors are connected to the modal model of a passive PLN (the interference in the PLN is not considered for simplicity). The particular values for the modal models of the DUT and the PLN used in the simulations are shown in Table 7.1.

Table 7.1: Modal model values of the DUT and the PLN.

Component	DUT	PLN
Z_{CM} [Ω]	25.3 + j5.6	20 + j0.6
Z_{DM} [Ω]	160.2 - j18.3	35 + j3.3
Z_{TM} [Ω]	50.7 + j32.1	130 + j62.1
V_{nCM} [dBμV]	95.58	-
V_{nDM} [dBμV]	87.31	-

In the simulations the value of C_{Y2} has been fixed to 10 nF, and the value of C_{Y1} has been swept from 10 nF to 1.8 nF. Figure 7.10 shows V_{CMout} and V_{DMout} for the different values

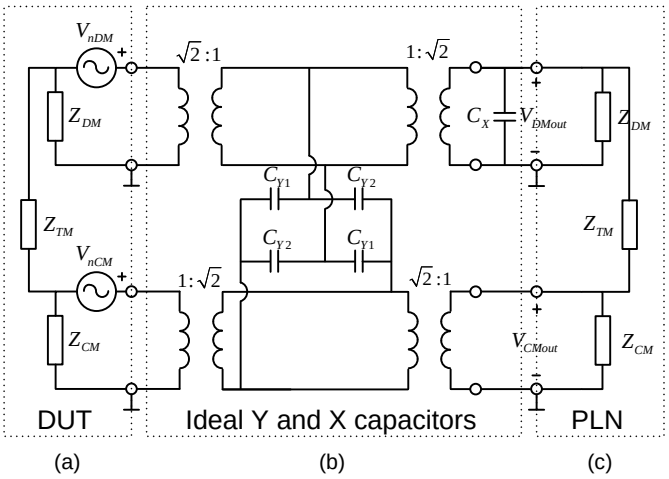

Figure 7.9: Propagation of the modal interference in the modal model of Y and X capacitors (b), placed between the modal model of a DUT (a) and the modal model of a PLN without interference (c).

of C_{Y1}. As can be seen, asymmetrizing the values of C_{Y1} from 10 nF to 1.8 nF produces a slight reduction of the attenuation of the CM, and a significant increase of the attenuation of the DM (up to 25 dB average at high frequencies). Therefore, non-standard configurations of Y capacitors can give interesting results, such as this significant reduction of V_{DMout} at the expense of a small increment of V_{CMout} (this increase can be tolerable or not depending on the rest of the filter components). In general, for balanced DUTs and PLNs, balanced values of Y-capacitor networks yield the best mitigation, but for unbalanced DUTs and PLNs, asymmetrized Y-capacitor networks improve the filter performance.

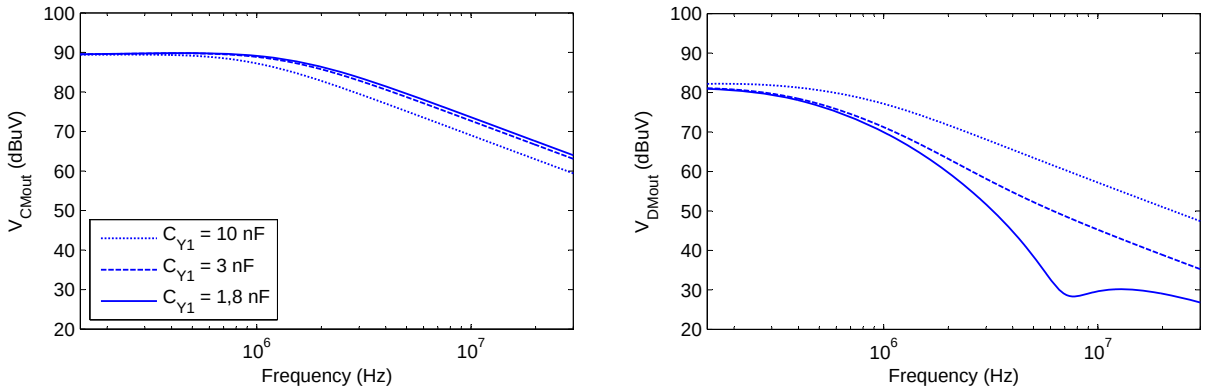

Figure 7.10: V_{CMout} and V_{DMout} for different values of C_{Y1}.

7.4.2 Simulations with ideal CMCs

The same experiment can be performed with CMCs. Figure 7.11 shows the circuit of this experiment, where the modal model of a CMC (figure 7.8(b)) has been connected between the

modal model of a DUT and the modal model of a passive PLN. The parametric investigation has been performed considering several DUTs, PLNs, and CMCs, modeled by their respective modal models. As an example consider the DUT and the PLN whose modal parameters are shown in Table 7.2.

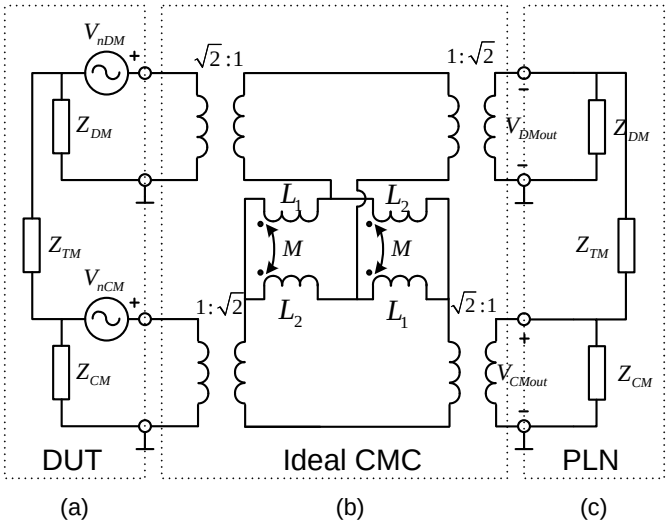

Figure 7.11: Propagation of the modal interference in the modal model of CMCs (b), placed between the modal model of a DUT (a) and the modal model of a PLN without interference (c).

Table 7.2: Modal model values of the DUT and the PLN.

Component	DUT	PLN
Z_{CM} [Ω]	3607 + j366	20 + j0.6
Z_{DM} [Ω]	3 - j4	35 + j3.3
Z_{TM} [Ω]	4502-j2151	130 + j62.1
V_{nCM} [dBμV]	95.58	-
V_{nDM} [dBμV]	87.31	-

Figure 7.12 shows V_{CMout} and V_{DMout} for different values of L_2 while keeping the value of L_1 to 20 mH. Unbalancing the values of L_2 from 20 mH to 13 mH produces a significant decrease of both CM and DM (an average of 25 dB for the CM and 15 dB for the DM).

Therefore, non-standard configurations of CMCs can also achieve, in some cases, significant reductions of V_{CMout} and V_{DMout}. From the performed parametric study, it can be concluded that, in general, for balanced DUTs and PLNs, balanced values of CMC inductances yield the best mitigation, but for unbalanced DUTs and PLNs, asymmetrized CMC inductances improve the filtering performance.

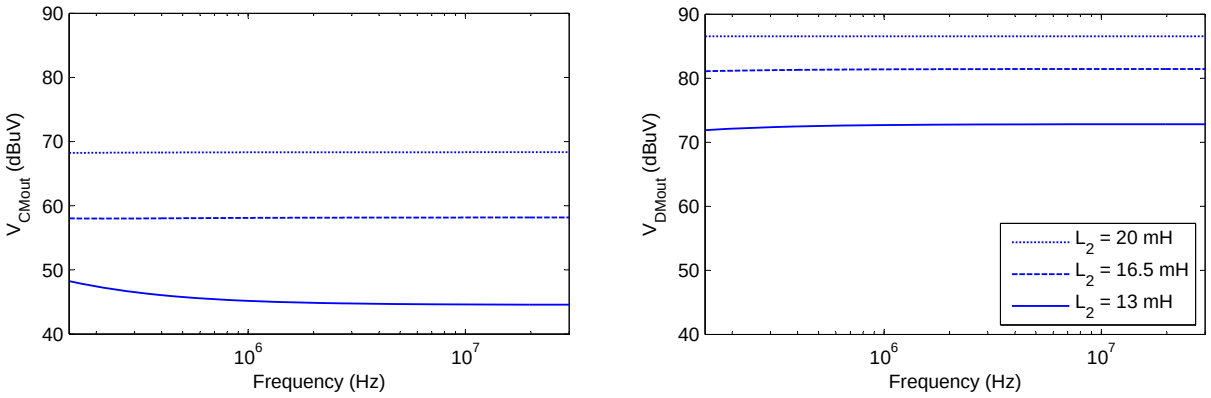

Figure 7.12: V_{CMout} and V_{DMout} for different values of L_2.

7.5 Design of the optimal components of a PLF

It has been shown that it is possible to improve the performance of a PLF generating mode conversion in networks composed by Y capacitors and CMCs. Therefore, a PLF design tool should consider simultaneously the DUT's conducted emissions, the DUT's and PLN's impedances, and all possible values of X capacitors, CMCs and Y capacitors that, with or without mode conversion, compose the optimal PLF, as for instance, regarding to cost. Because of the great amount of variables, the design becomes impossible without an optimization technique. In order to deal with this problem, a GA has been developed to work as a PLF design tool. A GA is a searching procedure based on the mechanics of natural selection and genetics, and its features allow its use as an optimization technique for the PLF design problem [140]–[142].

7.5.1 Performance of the genetic algorithm

Figure 7.13 shows the block diagram of the GA performance, and it can be explained as follows: first of all the algorithm generates a random group of solutions or chromosomes (each chromosome is a possible PLF made of a X capacitor, two Y capacitors and a CMC in an indifferent position), and their responses are evaluated by the fitness function. More specifically, the fitness function performs the prediction of the conducted emissions of the DUT connected to each solution. If the conducted emissions are under the circuit limit of [11], the solution receives a rated evaluation depending on its cost (which is related to the number of components and their value). Cheaper solutions have a better evaluation. If the conducted emissions are not under the circuit limit, the solution is penalized with a very bad evaluation in order to discard them in the next iteration. If no solutions fulfill the convergence condition, the best chromosomes are selected in the selection block. The crossover block combines two chromosomes to generate a new one for next iteration (or generation). And the mutation function make small random changes in the solutions, which provide genetic diversity and

enable the GA to search a broader space. The new generation of chromosomes is evaluated again in the fitness function. These steps are repeated until the convergence solution is achieved and the algorithm stops presenting its best results.

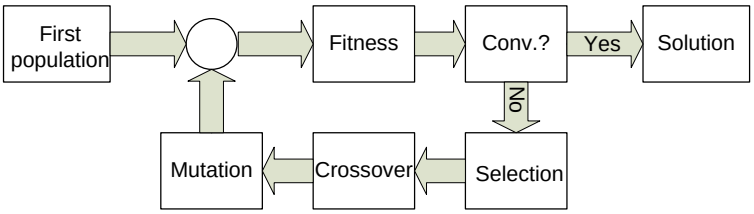

Figure 7.13: Block diagram of the GA performance.

7.5.2 Example with an actual DUT

In order to show the performance of this method, the switching power supply feeding the 4-MHz microcontroller of figure 6.11 has been used as a DUT. The different modal models of X and Y capacitors and CMCs presented in this chapter have been introduced in the GA, and there is not any restriction about the position of the components and neither about the amount of the possible mode conversion. After 1000 generations, with a population of 80 chromosomes in each generation, the PLF obtained is presented in table 7.3. The GA has omitted the components C_{Y1} and C_{Y2}, and the CMC is slightly unbalanced. The structure and the component values are similar to those obtained with the methodology of chapter 6 ($C_X = 100$ nF and $L_1 = L_2 = 20$ mH). However there is a small reduction of the component values due to the possibility of choosing continuous values and to the asymmetry introduced in the CMC, as seen in figures 7.14 and 7.15.

Table 7.3: Component values of the PLF found by the GA.

C_X [nF]	C_{Y1} [nF]	C_{Y2} [nF]	L_1 [mH]	L_2 [mH]
87	0	0	8.2	7.8

Figure 7.14 shows the circuit conducted emissions when the DUT is connected to the asymmetric PLF obtained with the GA (table 7.3) compared with the circuit conducted emissions when the DUT is connected to a similar but symmetric PLF ($C_X = 87$ nF and $L_1 = L_2 = 8.2$ mH). As can be seen, the asymmetric PLF gets a reduction of more than 14 dB at the frequency of 170 kHz in both V_L and V_N, making possible its use to keep the interference below the limit. In the symmetric case, higher values should be used in order to have the same effect. Frequencies beyond 2 MHz are less mitigated with the asymmetric PLF, but since they are far below the limit, in this particular case, this is not a problem.

Figure 7.15 shows the modal conducted emissions when the DUT is connected to the asymmetric PLF obtained with the GA (table 7.3) compared with the modal conducted emissions

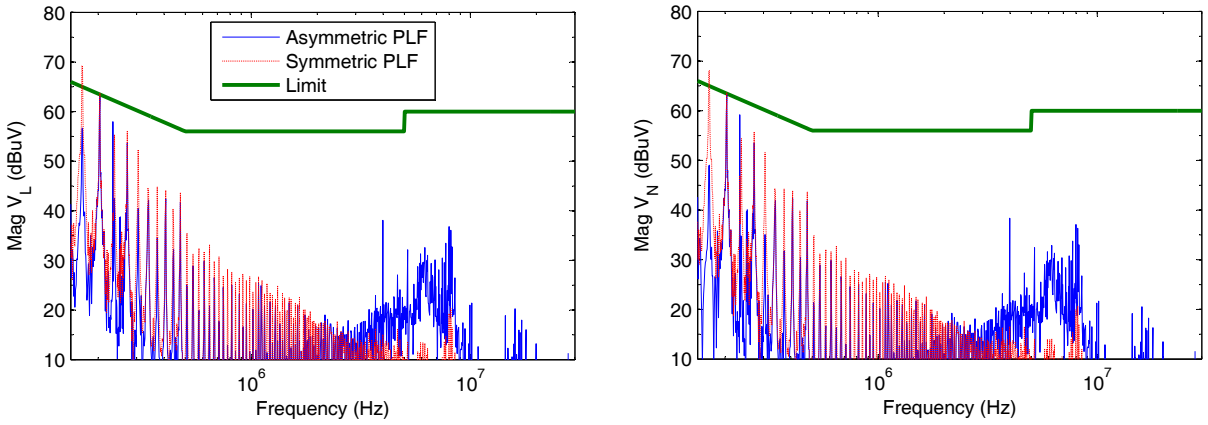

Figure 7.14: Circuit conducted emissions of the DUT connected to the asymmetric PLF obtained with the GA (table 7.3) and the symmetric PLF ($C_X = 87$ nF and $L_1 = L_2 = 8.2$ mH).

when the DUT is connected to a similar but symmetric PLF ($C_X = 87$ nF and $L_1 = L_2 = 8.2$ mH). The circuit limit [11] has also been plotted for guidance only. As can be seen, there is practically no difference on the CM attenuation between the asymmetric and symmetric PLFs, but a strong improvement can be seen on the DM attenuation at the frequency of 170 kHz when the asymmetric PLF is used. Therefore, asymmetric networks in a PLF can also be used to optimize the filtering performance of a PLF when it is connected to real devices. Even though the values obtained with the GA belong to ideal components, the results obtained can give an idea whether mode conversion is useful or not.

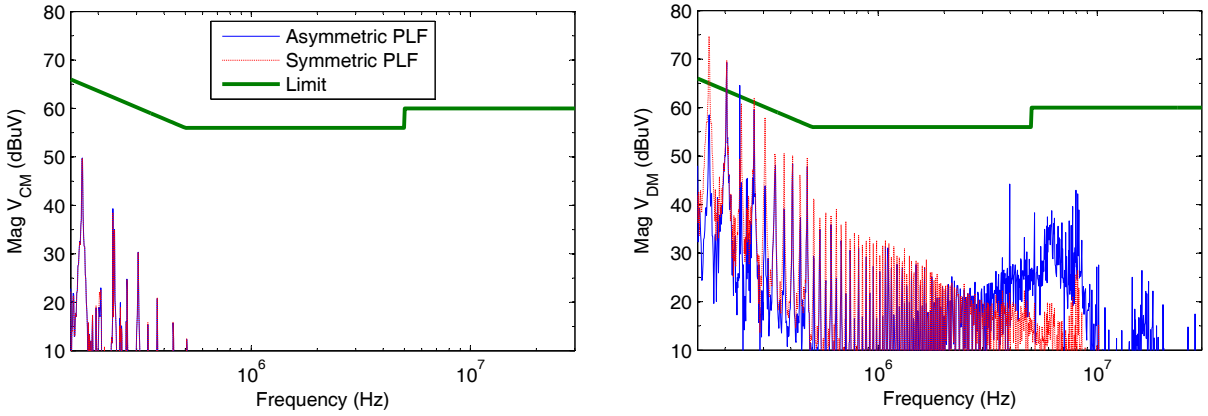

Figure 7.15: Modal conducted emissions of the DUT connected to the asymmetric PLF obtained with the GA (table 7.3) and the symmetric PLF ($C_X = 87$ nF and $L_1 = L_2 = 8.2$ mH).

7.6 Experimental Validation

In the previous sections, the mode conversion was used to optimize the filtering response of an ideal PLF. In this section the PLF design methodology using mode conversion is validated using actual networks of capacitors and CMCs. Firstly, the modal model of figure 7.2 is experimentally validated with actual capacitors and used to predict the conducted emissions and to optimize their mitigation in a PLF (mainly composed by capacitors) when it is connected to a real DUT. Secondly, the same procedure is applied on the modal model of figure 7.7 for its validation through real CMC measurements and the prediction and optimization (by using the optimization option of a circuit simulator) of the interference emissions of the same DUT.

7.6.1 Experimental validation of PLFs composed by actual capacitors

Actual X and Y capacitors present, apart from a capacitance, other parasitic elements that can be modeled, among others, with the equivalent circuit of figure 7.16, [54], [127]. The generic modal model of figure 7.2 allows the modal characterization of actual X and Y capacitors by substituting the two-port networks, either by the measured two-port Z- (or, in fact, S- or Y-) parameters of the capacitors, or by their equivalent circuit. In order to perform all the experimental tests, a 100 nF X capacitor and two 10 nF Y capacitors have been measured, and the values of their equivalent circuits are shown in table 7.5.

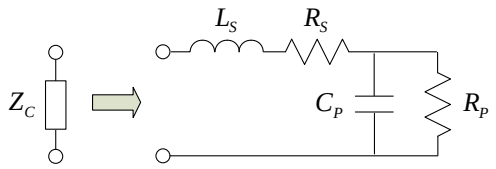

Figure 7.16: Equivalent circuit for a real capacitor.

Table 7.4: Component values of the 100-nF X-capacitor equivalent circuit (Z_{CX}) and of the two 10-nF Y-capacitor equivalent circuits (Z_{CY1} and Z_{CY2}).

Component	Z_{CX}	Z_{CY1}	Z_{CY2}
L_S [nH]	9.1	11.5	12.0
R_S [Ω]	0.11	0.14	0.15
C_P [nF]	101.8	10.6	10.4
R_P [kΩ]	37.2	4.4	6.4

Modal Model Validation

In order to validate the modal model of 7.2, X- and a Y-capacitor networks have been built with the 100-nF and 10-nF capacitors measured above. These networks have been measured and their modal S parameters extracted using the methodology described in chapter 2. These

networks have also been simulated using the modal models of figure 7.3(c) and figure 7.4(b). The comparison between the measured and simulated S_{M31} (input CM to output CM) and S_{M42} (input DM to output DM) parameters for the X-capacitor network, and the comparison between the measured and simulated S_{M41} (input CM to output DM) and S_{M42} (input DM to output DM) parameters of the Y-capacitor network, can be seen in figure 7.17. For the Y-class capacitor network, since both capacitors are similar, the modal conversion produced between port 1 and port 4 (S_{M41}) is very low (under -40 dB). Even in this case the modal conversion is perfectly predicted by the modal model. The excellent agreement between measurement and simulation validates the modal models proposed for shunt-connected two-port networks.

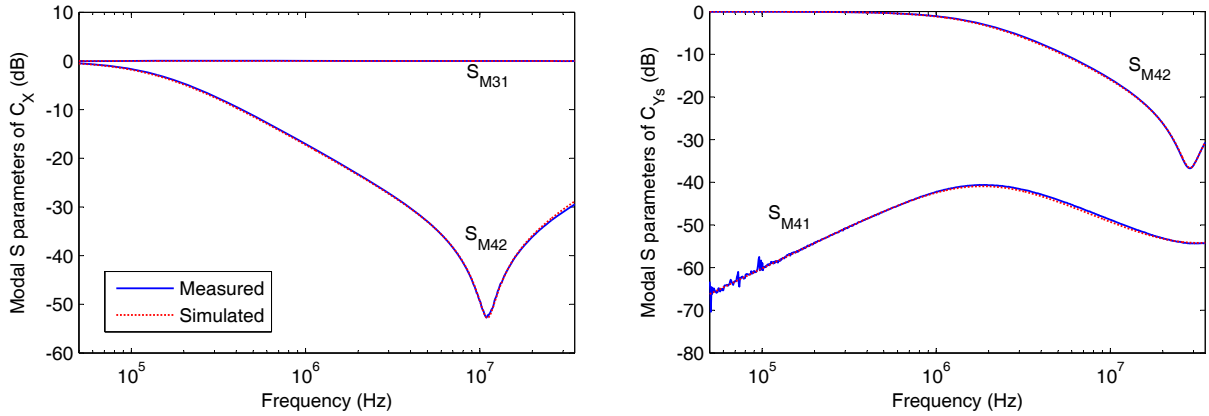

Figure 7.17: Comparison between measured and computed modal S-parameters in X- and Y-capacitor networks.

Prediction of the modal attenuation

The X- and Y-capacitor networks, along with a CMC of 1 mH, have been used to build the PLF of figure 7.18. This PLF has been connected to a switching power supply that feeds a microcontroller with a 4-MHz clock. The filtered CM and DM interference has been measured using a line impedance stabilization network (LISN) and a vector spectrum analyzer (VSA), as described in [11]. This same setup has been modally simulated using the modal models for X and Y capacitors as described in this chapter, the measured modal S parameters of the CMC and the LISN obtained as described in chapter 2, and the modal model of the DUT obtained as described in chapter 3, as seen in figure 7.18.

Figure 7.19 compares the measured and the predicted modal interference levels. A set of interference in the band from 150 kHz to 2 MHz, generated by the switching power supply of the transceiver, can be seen. A 4-MHz interference due to the clock is also noticeable. Measured interference levels below 15 dBμV are masked by the noise floor level of the measurement system. The good agreement between measurement and prediction validates again the capacitor modal models presented in this paper, and proves that they are useful tools to design PLFs

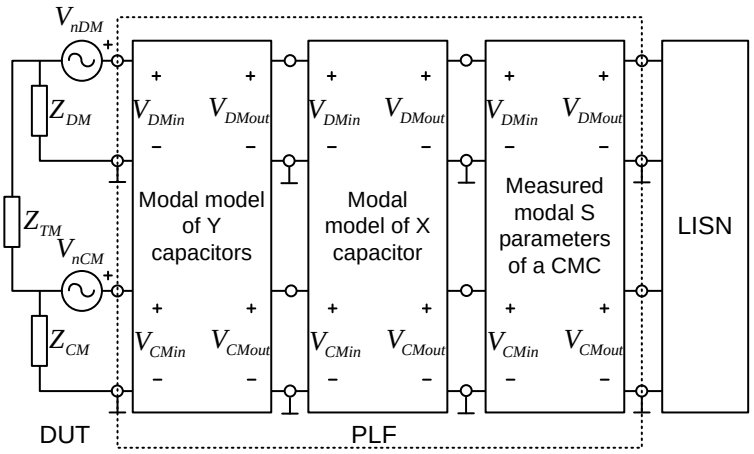

Figure 7.18: Modal models of X and Y capacitors connected to the modal models of a DUT and a LISN, and to the measured modal S parameters of a CMC.

since they allow the prediction of the actual modal interference levels that will be obtained once the filter is built.

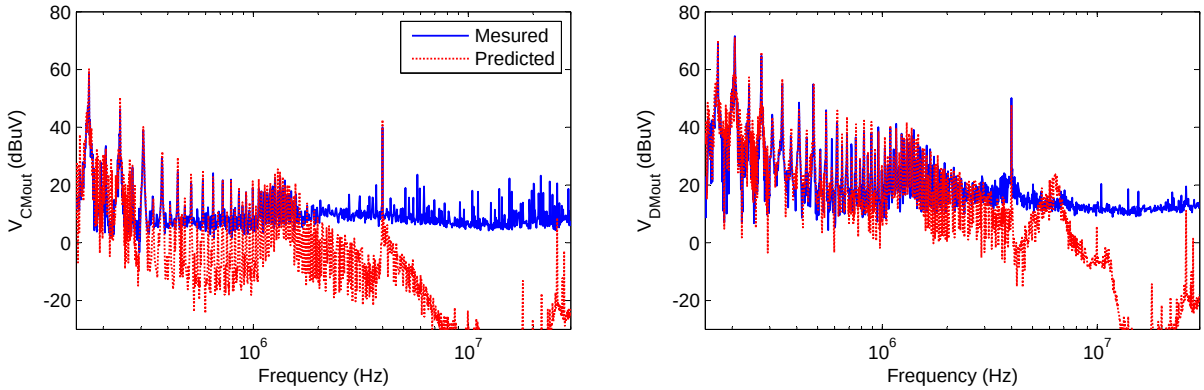

Figure 7.19: Measured and predicted modal interference levels.

PLF design using the mode conversion in a Y-capacitor network

The prediction of the conducted interference using the capacitor modal models can be used to optimize the PLF, as for instance, by unbalancing the Y-capacitor network. To this end, the interference levels of the same DUT have been simulated without a PLF; with a balanced PLF consisting of two Y capacitors, one X capacitor and a CMC (figure 7.18); and with the same PLF but unbalanced by eliminating one of the Y capacitors. Figure 7.20 shows the predicted interference levels in the three previous cases using the methodology presented in this chapter. When the device is filtered by the balanced PLF, an important decrease in the interference levels is achieved, but the interference levels obtained using the unbalanced PLF are very

similar to those obtained with the balanced PLF. Therefore the unbalanced PLF is preferable to filter the device since it is cheaper because it requires one less capacitor and obtains similar attenuation levels.

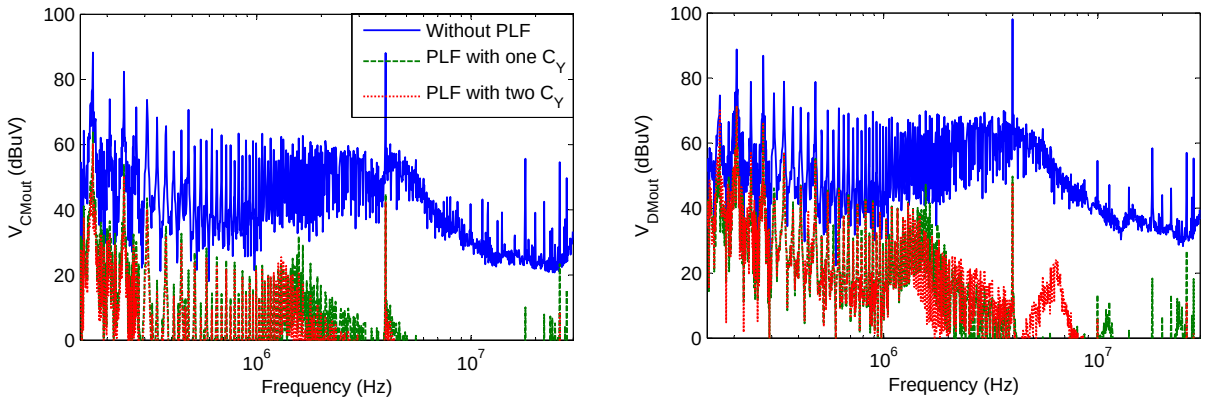

Figure 7.20: CM and DM conducted emissions without PLF, with the balanced PLF (two Y capacitors), and with the unbalanced PLF (one Y capacitor).

In order to corroborate the effect of the asymmetry, figure 7.21 shows the predicted interference levels of the DUT connected to the PLF of figure 7.18 but unbalanced by eliminating one of the Y capacitors and to the same PLF but eliminating both Y capacitors. The mode conversion effect is specially noticeable for the CM emissions at frequencies beyond 2 MHz. For instance, there is a difference of 20 dB for the 4-MHz interference between the unbalanced PLF and the PLF without the Y-capacitor network. This fact shows that the presented methodology is useful to optimize the PLFs. In this particular case it has been shown that one superfluous Y capacitor can be eliminated due to the modal study of the PLF.

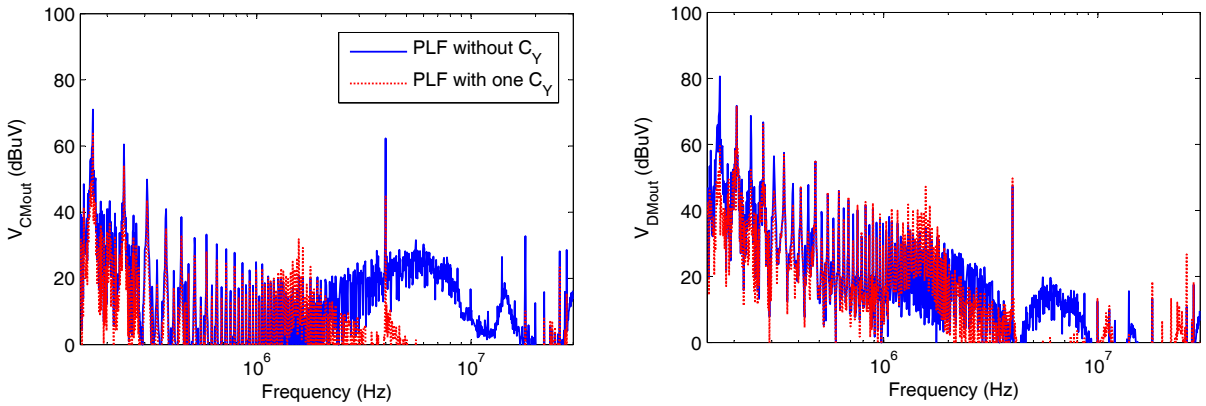

Figure 7.21: CM and DM conducted emissions with the unbalanced PLF (one Y capacitor) and with the PLF without the Y-capacitor network.

7.6.2 Experimental validation of PLFs composed by actual CMCs

Actual CMCs present, a part from the inductances L_1 and L_2, other parasitic elements that can be modeled, between others, with the equivalent circuit of figure 7.22, [54], [143]. The generic modal model of figure 7.7 allows the modal characterization of actual CMCs by substituting the two-port networks, either by the measured two-port Z- (or, in fact, S- or Y-) parameters of the capacitors, or by their equivalent circuit. In order to perform all the experimental tests, a 1-mH toroidal CMC has been measured, and the values of their equivalent circuits are shown in table 7.5.

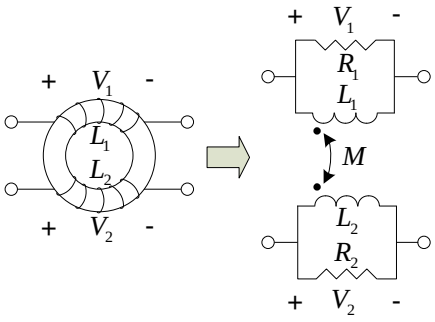

Figure 7.22: Equivalent circuit for actual CMCs.

Table 7.5: Component values of the equivalent circuit of a 1-mH toroidal CMC.

M [mH]	L_1 [mH]	R_1 [kΩ]	L_2 [mH]	R_2 [kΩ]
0.92	0.93	2.19	0.93	2.00

Modal Model Validation

In order to validate the modal model of figure 7.7, the 1-mH CMC has been measured as a four-port device, and its modal S parameters extracted using the methodology described in chapter 2. The CMC has also been simulated using, in this case, its equivalent circuit in the modal model of figure 7.7. The comparison between the measured and simulated S_{M11} (input CM to input CM), S_{M42} (input DM to output DM) and S_{M41} (input CM to output DM) parameters for the CMC network are shown in figure 7.23. Since L_1 and L_2 are similar, the mode conversion produced between port 1 and port 4 (S_{M41}) is very low (under -50 dB), but still accurately predicted by the modal model. The results obtained validate the modal model of figure 7.7.

Prediction of the modal attenuation

The CMC used previously has been used to filter the interference of an actual device, a switching power supply that feeds a microcontroller with a 4-MHz clock (figure 6.11). The

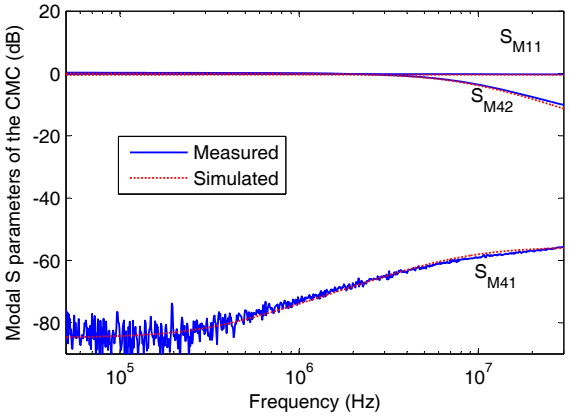

Figure 7.23: Comparison between measured and computed modal S parameters of a 1-mH CMC.

filtered CM and DM interference has been measured using a LISN and a VSA, as described in [11]. This same setup has been modally simulated using the modal model for CMCs described in this chapter and the modal model for the LISN and the DUT described in chapter 2 and chapter 3 respectively, as seen in figure 7.24.

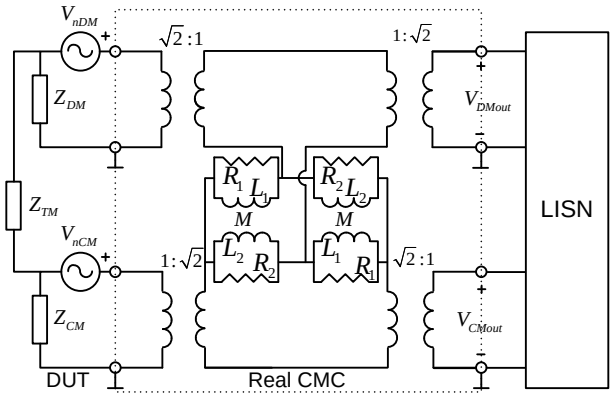

Figure 7.24: Modal model of an actual CMC connected to the modal models of a DUT and a LISN.

Figure 7.25 shows the measured and predicted modal interference levels. A set of interference from 150 kHz to 1 MHz, generated by the switching power supply, is apparent. The good agreement between measurement and prediction validates again the modal model of a CMC.

PLF design using the mode conversion in a CMC

The modal conversion, produced by an unbalanced CMC, can be used to improve the interference mitigation. By using the optimization option of a commercial circuit simulator (ADS), an improvement of the interference mitigation of the previous DUT is achieved by unbalancing the L_1 inductance to 1.3 mH. This value can be obtained by adding a coil to the actual L_1 inductance. When unbalancing CMCs, care attention must be taken to avoid core

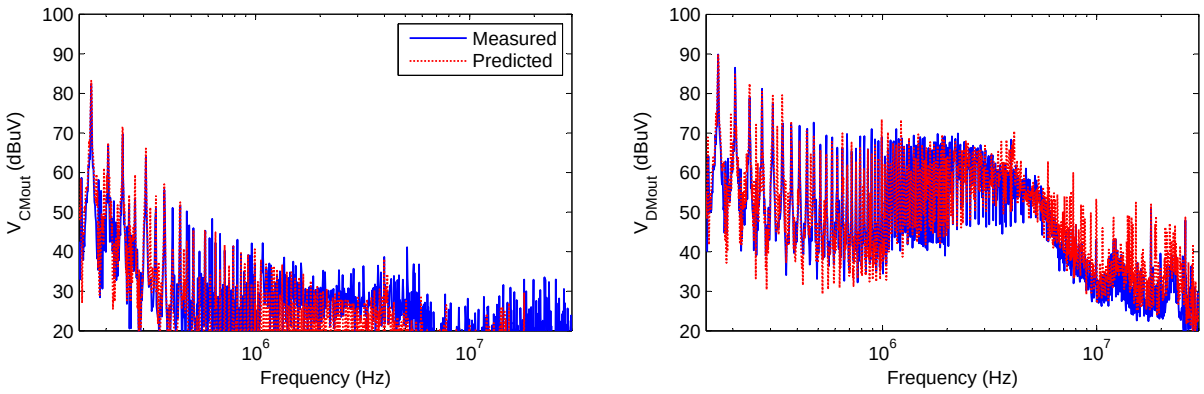

Figure 7.25: Measured and predicted modal interference levels.

saturation. In an unbalanced CMC, the flux due to the differential 50-Hz current flowing in its ferromagnetic core is not totally canceled. If this flux surpasses the saturation limit supported by the core, the inductance values will be considerably decreased [9], [21]. Then, before using an unbalanced CMC, it is important to know if it can supports such unbalancing. Figure 7.26 shows the measured S_{M31} (input CM to output CM), S_{M42} (input DM to output DM) and S_{M32} (input DM to output CM) parameters of the unbalanced CMC without any current through its coils, and with a 30-mA current. As can be seen, the flux due to the 30-mA current does not achieve important levels of saturation since both measurements present similar results. Therefore, this unbalanced CMC can be used to filter the DUT.

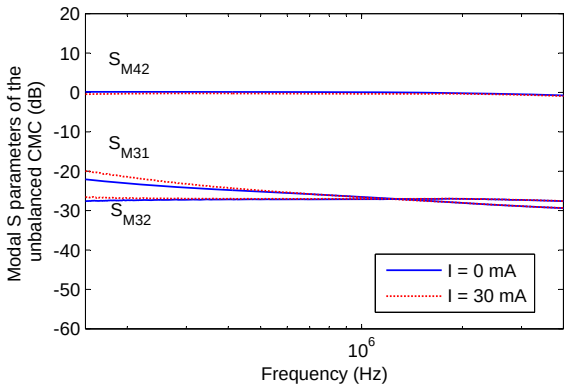

Figure 7.26: Comparison between the modal S parameters of the asymmetric CMC with and without current.

Figure 7.27 shows the predicted interference levels with the original and the unbalanced CMC (whose L_1 optimal value is of 1.3 mH). When the device is filtered by the unbalanced CMC, the CM presents a higher floor noise level, but a decrease of about 8 dB is achieved in the highest level of both CM and DM (170 kHz). This fact proves that the presented methodology is useful to design optimal CMCs.

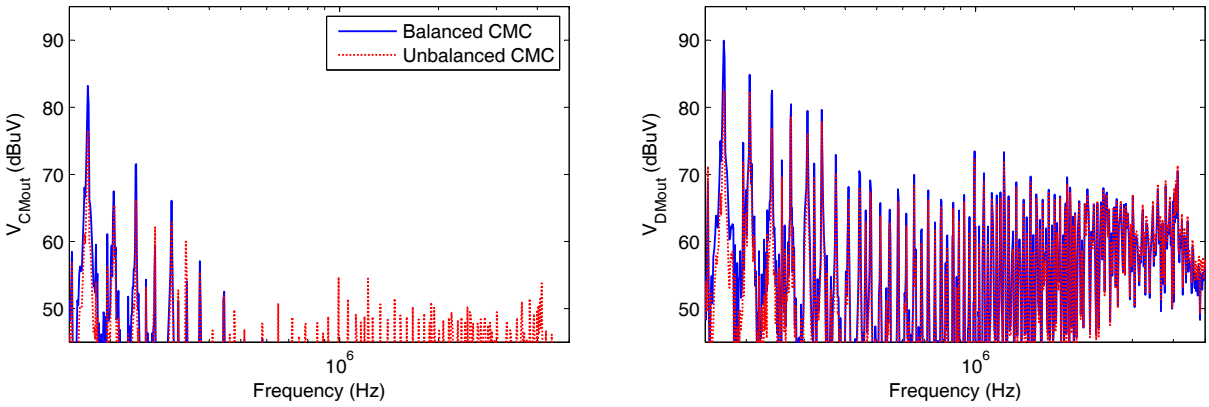

Figure 7.27: CM and DM conducted emissions with the original CMC, and with the unbalanced CMC.

Chapter 8

Conclusions and Future Work

Contents of this chapter

8.1 Conclusions

This section provides a summary of the work carried out on the objectives, and the means by which they have been achieved:

1. The first proposed objective was about the development of a new circuit and modal characterization technique for power-line filters (PLFs), electric devices (or devices under test (DUTs)) and power-line networks (PLNs). The circuit characterization is the natural characterization extracted from a physical structure, but the modal characterization is more useful to understand the generation and propagation of the common-mode (CM) and differential-mode (DM) interference, and to select the suitable components to its mitigation. To this end, all modal models separate the CM and the DM into a different port, so that the visualization of one of this terminals is enough to know the contribution of a modal component (CM or DM).

    - The circuit PLF characterization is performed through the circuit S parameters, and the modal characterization is done through the modal S parameters, which are a mathematical derivation of the circuit ones. The modal S parameters can be measured without or with a certain current level using the methodology presented in chapter 2, in order to consider the biasing effect of the PLF components in the characterization. Such characterization allows: 1) the prediction of the CM and DM insertion loss (IL) for line and load impedances of 50 Ω (equivalent information to the one given by the standard methods of measurement [21]); 2) the prediction of the CM and DM IL for line and load impedances of any value different from

50 Ω; and 3) the prediction of the energy transfer between the CM and the DM. Therefore, the methodology presented provides a complete solution for the PLF characterization, extracting all the necessary information to evaluate its behavior in front of any situation, and with a simple measurement system. This characterization also improves previous studies which present measurement methods and solutions for only one of the three previous points.

- DUTs and PLNs are included in the same characterization methodology, since they present a similar behavior from the electromagnetic compatibility (EMC) point of view. Both circuit and modal characterization consider the input impedance and the generation or presence of interference signals through a three-impedance pi-network and two voltage-sources model. The impedance values are extracted from the S-parameter measurements, and the voltage-source values are obtained from the conducted emission measurements, either in the frequency domain (when there is no restriction of time for a full measurement), as was seen in chapter 3, or in the time domain (which has some advantages when the DUT or the PLN contains non-stationary noise), as presented in chapter 4. The presented modal model is more accurate than those characterizations based on independent CM and DM paths, since the mode conversion is expressed through the modal transimpedance Z_{TM}.

2. The second objective was about the development of a new methodology to predict the conducted interference levels that an electric device supplies to the PLN through its PLF. Connecting all characterizations in a proper way (L terminals to L terminals and N terminals to N terminals or, alternatively, CM terminals to CM terminals, and DM terminals to DM terminals), it is possible to compute the reflection and transmission of the interference inside the different devices. Therefore, accurate characterizations will lead to accurate predictions. The most relevant characteristics of this methodology are:

   - It allows the prediction of the CM and DM attenuation in actual situations.
   - It allows the prediction of other effects, such as the mode conversion generated by asymmetries in the PLF, in the DUT or in the PLN.
   - It facilitates the election of the suitable PLF, avoiding long and expensive trial-and-error sessions.

   The methodology proposed in chapter 5 presents a complete solution to the conducted interference analysis produced by devices connected to the PLN through a PLF, and considerably improves the results obtained with the standard methods of characterization and measurement. In this document, the prediction has been based on the conducted emissions measurement setup of [11], but the same technique can be adapted to different setups following the same measurement procedure. Therefore, the presented methodology can be of interest for PLF manufacturers, for electric-device designers and for EMC laboratories.

3. The third objective of this work was about the development of a new methodology to design the optimal PLF. From the PLF, DUT and PLN characterization obtained in the first objective, and the prediction methodology of the second one, it is possible to find the most suitable PLF amongst a set of filters previously characterized. However, an specific design for a particular DUT would mainly improve the cost of production, avoiding the use of over-dimensioned PLFs. Chapter 6 presents a design methodology based on the S-parameter characterization. Using the measured S parameters of CMC, X-capacitor and Y-capacitor networks, this methodology generates all possible PLFs from first to n^{th} order by computing the combined S parameters of the individual networks. Each PLF is connected to the DUT and the conducted emissions are predicted to analyze their filtering behavior. Knowing the overall response of each PLF, the EMC designer can choose the best one according to his requirements, as for instance, the one that introduces the maximum attenuation, or the one that presents the lowest cost. This methodology has been used to design the PLF of switching power supplies with different kinds of conducted emissions, showing that it is possible to build efficient filters for devices with narrow-band and impulsive noise. This methodology improves previous design techniques based only on ideal components (so that it is difficult to predict the behavior of the PLF at high frequencies) or on fixed structures that do not consider different positions of their components.

4. The previous design methodology obtains optimal filters using the classical and symmetric structure of a PLF. Going beyond this structure, a new design methodology has been developed to obtain responses of filters that cannot be otherwise possible, thanks, mainly, to the mode conversion phenomenon. In chapter 7 this phenomenon is studied in detail through two modal models that characterize the modal behavior of networks with CMCs and capacitors placed in the PLN terminals. These models allow the direct visualization of the effects produced by their asymmetrization. Analyzing the results obtained from synthetic DUTs and PLNs, it is shown that, under certain conditions, specially for unbalanced DUTs and/or PLNs, the mode conversion improves the response of the PLF using the same or even less number of components than the symmetric one. This fact has also been corroborated with actual implementations of asymmetric filters connected to actual devices, allowing the elimination of superfluous components or the improvement of the filtering response at some particular frequencies.

5. Finally, the fourth objective was the spreading of the results obtained between the scientific community. This spreading has been done through the following publications in journals of the EMC field:

   - A.M. Sánchez, A. Pérez, J.R. Regué, M. Ribó, P. Rodríguez-Cepeda and F.J. Pajares, "Modal characterization of power-line filter capacitors", *IEEE Transactions on Power Delivery*, vol 25, no. 1, pp. 289-297, January 2010.

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8.2 Future work

The work presented in this document leaves some open topics of research:

1. The theory of modal decomposition presented in this report is based on a single-phase PLN structure, where three conductors (L, N and the reference G) leads to the existence

of two modes, the CM and the DM. However, the PLN structure used in high power applications is the three-phase PLN, which consists of four conductors instead of the three ones of a single-phase PLN. Therefore, a new modal signal characterization must be specified to consider the additional wires. A mode is defined as a solution of the multiconductor transmission lines (MTLs) equations, and a system composed by n transmission lines plus a reference (that is, $n+1$ conductors) has n solutions or modes [144]. The modes propagated in a three-line plus a reference system have been widely studied in the microwave field [145]–[147]. For instance, [145] proposes the mode definition shown in figure 8.1. Nevertheless, in the EMC community, it is more usual to talk about the CM and DM components. This is the reason for what [148] and [149] first, and [150] later, define the *ee* mode of figure 8.1(a) as the CM, and the *oo* and *oe* modes of figure 8.1(b) and 8.1(c) as the DM_1 and DM_2 respectively. Using this one or a similar definition, the modal theory and measurement systems presented in this report could be extended to cover the characterizations of three-phase electric devices and PLNs (without the N wire) and the design of three-phase PLFs.

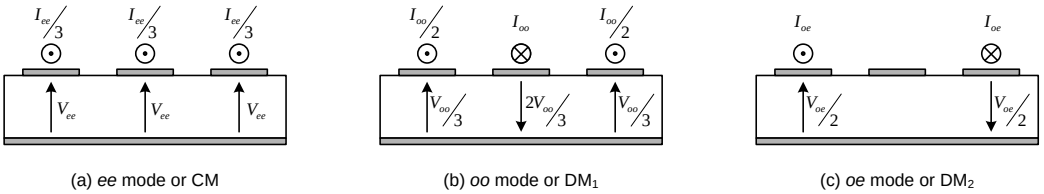

Figure 8.1: Definition of modal voltages and currents in a three-line-microstrip transmission line: (a) *ee* mode or CM; (b) *oo* mode or DM_1; (c) *oe* mode or DM_2.

2. The measuring device used to analyze the conducted emissions in the frequency domain was a vector network analyzer (VNA) with accessible receptors. A VNA is not a device built to perform such measurements, and some narrow-band tones appear in some figures due to the interference generated by the VNA itself. This fact degrades the measurements performed, being difficult to determine the real precision of the different methodologies presented in this report. If a vector spectrum analyzer (VSA) with two inputs was used instead of the VNA, that is, a device expressly built to measure the conducted emissions according to CISPR 22 [11], the precision of the measurements and the characterization methodologies could be rigorously studied.

3. Chapter 4 presented a methodology to obtain the root mean square (RMS) spectra of the conducted emissions from time-domain measurements, which main advantage in front of frequency-domain measurements was the time reduction. This methodology can be completed by including the digital quasi-peak [112], [113] and average [8], [114] detectors equivalent to the analog ones of a spectrum analyzer (SA). Therefore, the circuit and modal models of a DUT could be obtained from the quasi-peak and average values instead

of the RMS ones, and their simulated conducted emissions could be directly compared with the quasi-peak and average limits for circuit emissions established in CISPR 22 [11].

4. The main disadvantage of the time-domain conducted-emissions measurements performed with an 8-bit oscilloscope in front of the frequency-domain measurements is the dynamic range, which is approximately of 48 dB. However, there are other options to perform the time-domain measurements that can considerably improve this dynamic range, as for instance by using a field programmable gate array (FPGA) with a 16-bit analog to digital converter (ADC). Present-day 16-bit ADCs can achieve a sample rate of about 200 MSps, which is enough for conducted emission measurements, and the dynamic range, in this case, is of about 96 dB, similar to the one provided by a SA.

5. Chapter 7 presented a PLF design methodology based on the mode conversion. Although some experiments on actual CMCs and capacitors were shown, the GA used to design the PLF only gives the values of the ideal components of the PLF, without taking into account the effect introduced by their parasitics. Therefore, these values can only be considered as a guidance, since the response of the actual components differs from their ideal one, specially at high frequencies. In order to solve this problem, it is necessary to perform a deep study of the parasitic components of CMCs and capacitors, using, for instance, the equivalent circuits of [54]. If a direct connection between the ideal value and the parasitics of the actual component were found, the behavior of the PLF could be accurately predicted and the GA efficiency would be drastically improved.

6. Even though there is not any problem when asymmetrizing a Y-capacitor network, there are some drawbacks when asymmetrizing a CMC network, and they are due to the possible saturation of its ferromagnetic core. As it was seen in chapter 2, asymmetries of the CMC produce core saturation for a certain level of current. Therefore, the maximum asymmetry that a CMC can support is determined by the current level consumed by the DUT and the saturation point of the CMC core. Since the current level consumed by the DUT, in principle, is not configurable by the EMC engineer, the best option is to work with cores that, having a high relative permeability (and therefore, a high inductance), keep a high saturation level. The relation between permeability and saturation of three different cores is compared in [134]: a ferrite core, an amorphous core (quickly solidified metal) and a nanocrystalline core. The last one presents a good permeability/saturation relation. Studying these and other materials, the relation between the maximum asymmetry that can be achieved in function of the consumed current for each material can be obtained. In some sectors, as in the aerospace sector, the size of the filter is prioritized in front of its prize, so that more expensive materials can be used (as for instance nanocrystalline cores) with noticeable asymmetries. In other sectors, the prize is the main factor to be considered, and, therefore, the material used to build asymmetric filters should be a material with a worse permeability/saturation relation, limiting then the asymmetry that

the CMC can withstand.

7. The measurements presented in this work have been used to validate the different methodologies proposed in the frequency range between the 150 kHz and the 30 MHz. In [88] the circuit and modal characterization method based on the S parameters for PLFs is validated until 100 MHz, and in [143] these parameters are used to measure CMCs until 2 GHz. With the suitable equipment, the frequency range validated in this work could be extended to find the minimum and maximum frequencies where the characterization, prediction and design methodologies are still valid.

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Appendix

.1 S parameters to T parameters

The conversion from S parameters to T parameters of a two-port network is shown in [94]. For a four-port network, the parameter conversion can be performed as follows:

$$T_{11} = \frac{S_{11}(S_{33}S_{42} - S_{43}S_{32}) + S_{12}(S_{43}S_{31} - S_{33}S_{41}) + S_{13}(S_{41}S_{32} - S_{31}S_{42})}{S_{41}S_{32} - S_{31}S_{42}} \tag{1a}$$

$$T_{12} = \frac{S_{41}S_{12} - S_{11}S_{42}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1b}$$

$$T_{13} = \frac{S_{11}(S_{34}S_{42} - S_{44}S_{32}) + S_{12}(S_{44}S_{31} - S_{34}S_{41}) + S_{14}(S_{41}S_{14} - S_{31}S_{42})}{S_{41}S_{32} - S_{31}S_{42}} \tag{1c}$$

$$T_{14} = \frac{S_{32}S_{11} - S_{31}S_{12}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1d}$$

$$T_{21} = \frac{S_{33}S_{42} - S_{43}S_{32}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1e}$$

$$T_{22} = \frac{-S_{42}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1f}$$

$$T_{23} = \frac{S_{34}S_{42} - S_{44}S_{32}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1g}$$

$$T_{24} = \frac{S_{32}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1h}$$

$$T_{31} = \frac{S_{21}(S_{33}S_{42} - S_{43}S_{32}) + S_{22}(S_{43}S_{31} - S_{33}S_{41}) + S_{23}(S_{41}S_{32} - S_{31}S_{42})}{S_{41}S_{32} - S_{31}S_{42}} \tag{1i}$$

$$T_{32} = \frac{S_{41}S_{22} - S_{42}S_{21}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1j}$$

$$T_{33} = \frac{S_{21}(S_{34}S_{42} - S_{44}S_{32}) + S_{22}(S_{44}S_{31} - S_{34}S_{41}) + S_{24}(S_{41}S_{24} - S_{31}S_{42})}{S_{41}S_{32} - S_{31}S_{42}} \tag{1k}$$

$$T_{34} = \frac{S_{32}S_{21} - S_{31}S_{22}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1l}$$

$$T_{41} = \frac{S_{43}S_{31} - S_{33}S_{41}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1m}$$

$$T_{42} = \frac{S_{41}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1n}$$

$$T_{43} = \frac{S_{44}S_{31} - S_{34}S_{41}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1o}$$

$$T_{44} = \frac{-S_{31}}{S_{41}S_{32} - S_{31}S_{42}} \tag{1p}$$

.2 T parameters to S parameters

The conversion from T parameters to S parameters of a two-port network is shown in [94]. For a four-port network, the parameter conversion can be performed as follows:

$$S_{11} = \frac{T_{14}T_{42} - T_{44}T_{12}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2a}$$

$$S_{12} = \frac{T_{24}T_{12} - T_{14}T_{22}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2b}$$

$$S_{13} = \frac{T_{11}(T_{24}T_{42} - T_{44}T_{22}) + T_{12}(T_{44}T_{21} - T_{24}T_{41}) + T_{14}(T_{41}T_{22} - T_{21}T_{42})}{T_{24}T_{42} - T_{44}T_{22}} \tag{2c}$$

$$S_{14} = \frac{T_{12}(T_{23}T_{44} - T_{24}T_{43}) + T_{13}(T_{24}T_{42} - T_{22}T_{44}) + T_{14}(T_{22}T_{43} - T_{23}T_{42})}{T_{24}T_{42} - T_{44}T_{22}} \tag{2d}$$

$$S_{21} = \frac{T_{34}T_{42} - T_{44}T_{32}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2e}$$

$$S_{22} = \frac{T_{24}T_{32} - T_{34}T_{22}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2f}$$

$$S_{23} = \frac{T_{31}(T_{24}T_{42} - T_{44}T_{22}) + T_{32}(T_{44}T_{21} - T_{24}T_{41}) + T_{34}(T_{41}T_{22} - T_{21}T_{42})}{T_{24}T_{42} - T_{44}T_{22}} \tag{2g}$$

$$S_{24} = \frac{T_{32}(T_{23}T_{44} - T_{24}T_{43}) + T_{33}(T_{24}T_{42} - T_{22}T_{44}) + T_{34}(T_{22}T_{43} - T_{23}T_{42})}{T_{24}T_{42} - T_{44}T_{22}} \tag{2h}$$

$$S_{31} = \frac{-T_{44}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2i}$$

$$S_{32} = \frac{T_{24}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2j}$$

$$S_{33} = \frac{T_{21}T_{44} - T_{22}T_{41}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2k}$$

$$S_{34} = \frac{T_{23}T_{44} - T_{43}T_{24}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2l}$$

$$S_{41} = \frac{T_{42}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2m}$$

$$S_{42} = \frac{-T_{22}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2n}$$

$$S_{43} = \frac{T_{22}T_{41} - T_{21}T_{42}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2o}$$

$$S_{44} = \frac{T_{22}T_{43} - T_{23}T_{42}}{T_{24}T_{42} - T_{44}T_{22}} \tag{2p}$$

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