UNIVERSITAT ROVIRA I VIRGILI
DEVENLOPMENT OF COMPACT SMALL SIGNAL QUASI STATIC MODELS FOR MULTIPLE GATE MOSFETS
Oana Moldovan
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List of Publications

- **International Journals**

1. "Accurate Prediction of the Volume Inversion impact on Undoped DG MOSFETs' Capacitances",**Oana Moldovan**, Ferney A. Chaves, David Jiménez, Jean-Pierre Raskin and Benjamin Iñiguez- submitted

2. "A quasi two-dimensional compact drain current model for undoped symmetric double gate MOSFETs including short-channel effects", F. Lime, B.Iñiguez and **O. Moldovan –** accepted for publication in *IEEE Transaction on Electron Devices*

3." Compact Charge and Capacitance Modeling of Undoped Ultra-Thin-Body (UTB) SOI MOSETs", **Oana Moldovan**, Ferney A. Chaves, David Jiménez and Benjamin Iñiguez- accepted for publication in *Solid-State Electronics*

4. "Modeling of Potentials and Threshold Voltage for Symmetric Doped Double-Gate MOSFETs", Antonio Cerdeira, **Oana Moldovan**, Benjamín Iñiguez and Magali Estrada , *Solid-State Electronics*, Vol. 52, Issue 5, May 2008

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5. "Explicit Analytical Charge And Capacitance Models Of Undoped Double Gate MOSFETs", **Oana Moldovan**, David Jiménez, Jaume Roig, Ferney A. Chaves and Benjamin Iñiguez, *IEEE Transaction on Electron Devices*, Vol. 54, no. 7, July 2007

6. "Compact Model For Doped Double-Gate MOSFETs targeting baseband analog applications", **Oana Moldovan**, Antonio Cerdeira, David Jiménez, Jean-Pierre Raskin, Valeria Kilchytska, Denis Flandre, Nadine Collaert, and Benjamin Iñiguez , *Solid-State Electronics,* Vol.51, Issue 5, May 2007

7. "Analytical Charge And Capacitance Models Of Undoped Cylindrical Surrounding Gate MOSFETS", **Oana Moldovan**, Benjamin Iñiguez, David Jiménez and Jaume Roig, *IEEE Transaction on Electron Devices*, Vol. 53, no. 1, January 2007

8. "A Compact Quantum Model of Nanoscale Double-Gate MOSFET for High Frequency and Noise Simulations", A.Lázaro, B.Nae, **O. Moldovan**, B.Iñiguez, *Journal of Applied Physics*, *Vol.100, N.8,* Oct.2006

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- **International Conferences**

1. *"*Compact Charge and Capacitance Modeling of Undoped Ultra-Thin-Body (UTB) SOI MOSETs", Oana Moldovan, Ferney A. Chaves, David Jiménez and Benjamin Iñiguez, *EUROSOI* Fourth Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits,Tyndall National Institute, Cork, Ireland, Jan 23-25th, 2008

2."Finite Element Simulations of Parasitic Capacitances Related to Multiple-Gate Field-Effect Transistors Architectures", O. Moldovan, D. Lederer, B. Iñiguez, J.-P. Raskin, *8th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF 2008*), Orlando, Florida, USA, January 23-25, 2008

3."A New Explicit Compact Charge And Capacitance Model For Undoped Symmetric Double Gate MOSFETs", Oana Moldovan, Benjamin Iñiguez, David Jiménez and Jaume Roig, Walk-in Poster at the *Conference on Simulation of Semiconductor Devices and Processes (SISPAD), Vienna, Austria*, September 25-27, 2007

4."Charge-Based Compact Modeling of Multiple-Gate MOSFETs", B. Iñiguez, A. Lázaro, H. Abd-ElHamid, **O. Moldovan**, B. Nae, J. Roig, D. Jiménez, *IEEE Custom Integrated*

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Circuits Conference (CICC), *San José (California, USA)*,

September 16-19, 2007

5."Compact Model for Long-Channel Symmetric Doped DG MOSFETs", A. Cerdeira, **O. Moldovan**, B. Iñiguez and M. Estrada, Poster at *MOS-AK/ESSDERC/ESSCIRC Workshop, Munich, Germany*, September 14, 2007

6."Compact Model for Symmetric Doped Double-Gate MOSFETs including SCE", A. Cerdeira, **O. Moldovan**, J. Alvarado, B. Iñiguez and M. Estrada - *EUROSOI 2007,Third Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits, Leuven, Belgium*, January 24 - 26, 2007

7. "Compact Model of Double-Gate MOSFETs for Low Power Analog Applications", **Oana Moldovan**, Antonio Cerdeira, David Jiménez, Jean-Pierre Raskin, Denis Flandre, Nadine Collaert, Benjamin Iñiguez - *XXI Conference on Design of Circuits and Integrated Systems, Barcelona, Spain,* November 22-24, 2006

8. "Compact RF modeling of multiple gate MOSFETs", Benjamín Iñiguez, Antonio Lázaro and **Oana Moldovan,** *European Microwave Week, Manchester, UK*, September 10-15 2006

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9. “DC to RF Small-Signal Compact DG MOSFET model”, B. Iñíguez, A.Lázaro, **O. Moldovan**, A. Cerdeira and T.A. Fjeldly, *NSTI Nanotechnology Conference and Trade Show - Nanotech 2006 – Boston, Massachusetts*, *U.S.A.*, May 7-11, 2006

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List of Symbols

ρ charge density

ϕ potential

β thermal potential

ϕd potential difference at any voltage

ϕd_{BT} potential difference below threshold

ϕd_M potential difference at V_{GM}

ϕd_T potential difference at threshold

μ_{eff} effective mobility with series resistance

ϕ_F Fermi level

ϕ_{Fn} quasiFermi level for electrons

ϕ_{Fp} quasiFermi level for holes

ϕo potential at the center of the Si layer

ϕo_{BT} potential at the center of the Si layer below threshold

ϕo_T potential at the center of the Si layer at threshold

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ε_{ox} gate dielectric constant

ϕs surface potential

ϕs_{BT} surface potential below threshold

ε_{Si} Si dielectric constant

ϕs_{T} surface potential at threshold

ΔL length of the saturation region

μ electron mobility

μ_0 low field mobility

μ_{eff}^0 effective mobility without series resistance

A actual occupied planar silicon die area

C_{dg} drain-gate capacitance

C_{ds} drain-source capacitance

C_f fringing capacitance

C_{gd} gate-drain capacitance

C_{gg} total gate capacitance

C_{gs} gate-source capacitance

C_{ov} overlap capacitance

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C_{ox} gate capacitance per unit area

C_{sd} source-drain capacitance

C_{sg} source-gate capacitance

C_{Si} Si layer capacitance per unit area

E_{ld} longitudinal electric field at the drain

Es surface electric field

f_{max} maximum available gain cutoff frequency

f_T current gain cutoff frequency

h_{fin} fin height in FinFETs

I_{DS} drain current

k Boltzmann constant

L transistor channel length

LW Lambert function

N_A Si layer doped concentration

N_{Amax} Na at the maximum of the potential at the center

n_e electron concentration

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N_{fin} number of fins in FinFETs

n_i intrinsic carrier concentration

N_{poly} polysilicon layer doped concentration

N_{ss} surface state concentration

p hole concentration

Q induced charge carriers

q electron charge

Q_B total back gate charge

Q_d induced charge carriers at the drain

Q_D total drain charge

q_D normalized depletion charge

q_d normalized induced charge at the drain

Q_{Dep} modulus of the total depletion charge in the Si layer

Q_F total front gate charge

Q_G total inversion charge at gate

Q_m mobile charge in the saturated region

Q_S total source charge

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Q_s induced charge carriers at the source

q_s normalized induced charge at the source

Q_{Tot} total inversion charge

S_{fin} fins spacing in FinFETs

T temperature

t_{ox} gate dielectric thickness

t_{poly} polysilicon thickness

t_{Si} Si layer thickness

V potential along the channel

V_{bi} source and drain junction built-in voltage

V_{DS} drain voltage

V_E Early voltage

V_{FB} flat band voltage

V_{GB} back gate voltage

V_{GM} maximum analyzed gate voltage

V_{GS} gate voltage

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V_{sat} saturation potential

v_{sat} saturation velocity

V_t threshold voltage

W channel width

W_{fin} fin width in FinFETs

$\Delta\varphi$ work function difference between the gate electrode and the intrinsic silicon

λ_{DIBL} characteristic length for the DIBL

θ_1 mobility attenuation coefficients of the first order

θ_2 mobility attenuation coefficients of the second order

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Chapter 1

State of the Art and Current Trends for Multiple Gate MOS Devices

1A. Introduction

Since the invention of the integrated circuit (IC) in 1958, engineers and researchers around the world have worked on how to put more speed, performance and value onto smaller chips of silicon. The semiconductor industry has made considerable progress, especially regarding the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The fundamental driver has been the continued shrinking of its feature sizes, allowing the exponential growth in device count that tracks the well-known Moore's Law [1], first formulated by Intel co-founder Gordon Moore. Shrinking down feature sizes (at a rate of approximately 0.7 times every 18 months) allows more transistors to be packed onto a piece of silicon, with each one running at higher speeds. This combination translates into higher computing capabilities,

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ultimately delivering better value to the end user. However, this law is a rough prediction of the future of IC expansion. The need of a more accurate forecast defined the International Technology Roadmap for Semiconductors (ITRS) [2], which has been predicting and driving the pace of semiconductor technology at the same time. In the past century, together with the reduction of the MOSFET dimensions, also materials used for fabrication have changed: bulk silicon wafers changed to Silicon-on-Insulator (SOI) wafers. Also, the thickness of SOI varied, leading to MOS transistors in Partially-Depleted mode (thick SOI), and in Fully-Depleted mode (thin SOI). One of the main advantages of this wafer is the drastic reduction of all the parasitic effects coming from the silicon substrate. [3].A SOI wafer is actually a piece of a pure silicon wafer placed on an insulating device, such as silicon dioxide, called buried oxide. The transistors are then built on this thin silicon layer. If the silicon film is thin enough the depletion zone below the gate extends all the way through the buried oxide, and the device is said to be fully depleted (Fig.1A.1 A), if not it is called partially depleted (Fig.1A.1B). The remarkable feature of the fully depleted SOI MOSFET is that the current drive is higher than in bulk MOSFET and its subthreshold slope is sharper (better), due to a much smaller body factor [4].

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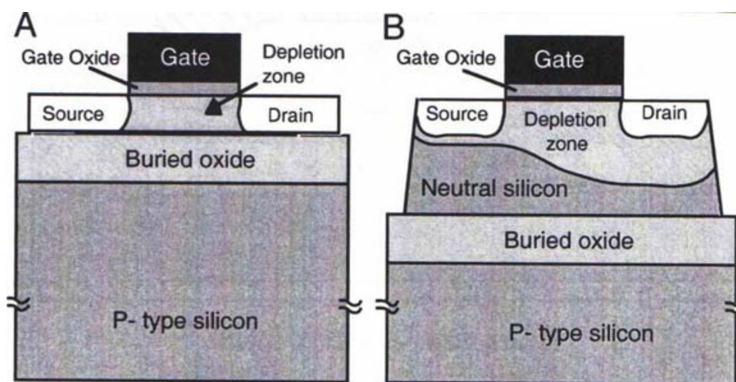

Fig.1A.1 *A Fully depleted SOI MOSFET, B-Partially depleted SOI MOSFET [5]*

However, even in ultrathin-film SOI technology, results have shown that the transconductance and AC characteristics of Single-Gate (SG) MOS structures, for gate lengths down to 40 nm are deteriorated due to Short Channel Effects (SCE) [6]. This means that the shrinking process will come to an end if no new technology can be found. The gate controls the channel of the transistor through capacitive coupling. The problem is that, when the MOSFET gate is shrunk, the drain is pulled closer to the middle of the channel, increasing the capacitive coupling between the drain and the channel. If the devices are too small, the drain has enough coupling to the channel that a leakage current will flow, only with a drain voltage applied, and no gate voltage. Being faced with this problem, ITRS proposes as one of the solutions, the implementation of novel devices like multiple-gate SOI MOSFETs, which will allow the gates to control the

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channel from several sides (solving the SCE problem) and so the gate length to be further reduced. The idea of the Double-Gate (DG) MOSFET was first introduced by J-P. Colinge [7]. Since then, other multiple-gate SOI MOSFETs have been introduced [8,9] such as Triple-Gate (TG), FinFET, Pi-Gate (PG), Quadruple-Gate (QG), Surrounding-Gate (SGT), also called Gate-All-Around (GAA), Omega-Gate (Ω-G), etc. (Fig.1A.2)

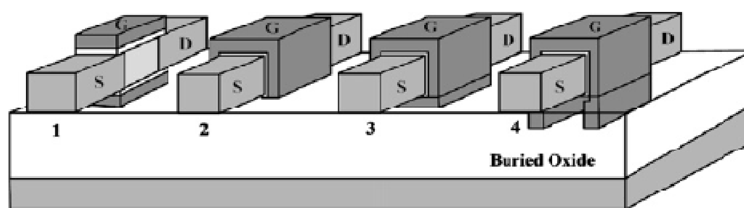

Fig.1A.2 The schematic device structures of MuGFETs[10]:1)double-gate,2)triple-gate,3)quadruple-gate, 4)PI-gate

Pi-gate MOSFETs are basically triple gate devices with an extension of the gate electrode below the active silicon island, which increases current drive and improves short-channel effects. The gate extension forms a virtual, field induced, gate electrode underneath the device that can block drain electric field lines from encroaching on the channel region at the bottom of the active silicon. Instead the lines terminate on the gate extensions. This gate structure is very effective at reducing short-channel effects. Such devices can be called 3+ (triple-

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plus)-gate devices because their characteristics lie between those of triple- and quadruple-gate devices [11].

The FinFET proves to be an interesting alternative to SG MOSFET [12-14] also, due to the fact that this structure has been used to set new world records for smallest gate length, in various research laboratories: the current record is 3nm gate length [15]. It is important to note that during the same process flow, conventional planar transistors can be also produced side by side on the same chip as the FinFETs. However, it is well known that the double-gate (top and bottom gate) silicon-on-insulator (SOI) MOSFET and the gate-all-around device are the most suitable device structures for suppressing short-channel effects such as DIBL (Drain Induced Barrier Lowering) and subthreshold slope degradation [7], [16-18]. Even though there is a lot of research around these different types of multiple-gate MOSFETs, until now, only the DG MOSFET is predicted to be introduced in 2011 due to its advantages [2]. So, the DG technology is presenting itself not as a possibility but as a certain long-term solution. The DG architecture can be defined as planar or non-planar. For example, a FinFET can be seen as a non-planar DG MOSFET if the width of the silicon fin is much smaller that its height. If the width of the silicon fin becomes comparable to its height, the structure changes to a triple-gate MOSFET.

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An interesting characteristic of the multiple-gate devices is the volume inversion concept, introduced by Balestra et al.[19]: if the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of this device is similar to the operation of two conventional MOSFETs connected in parallel. However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction appears between the two potential wells. In such conditions the inversion layer is formed not only near the two silicon–oxide interfaces, but throughout the entire silicon film thickness. It is then said that the device operates in ‘‘volume inversion,’’ i.e., carriers are no longer confined at one interface, but distributed throughout the entire silicon volume. Several authors have claimed that volume inversion presents a significant number of advantages, such as enhancement of the number of minority carriers; increase in carrier mobility [20] and velocity due to reduced influence of scattering associated with oxide and interface charges and surface roughness; as a consequence of the latter, an increase in drain current and transconductance [19,21]. This increase in the carrier mobility is due to the fact that when the film is fully inverted, a big fraction of the current flows around the center of the film, sufficiently far away from the interfaces, thus reducing the surface roughness scattering. This

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phenomenon usually takes place around the threshold voltage and it depends also on the doping concentration in the channel. For a thin film, a low or intrinsic doping is needed in order to assure the volume inversion. In fact, undoped films can be used, because the full depletion of the thin film prevents punch-through. Also, we can avoid the problems resulting from dopant-impurity location randomness and improve carrier transport by the consequent mobility enhancement.

DC analysis of DG devices has shown that the drain current (I_{DS}) and transconductance (g_m) of a DG MOSFET are higher than twice the drain current and transconductance, respectively, of a SG SOI MOSFET [9,19,22], due to volume inversion phenomena, thus suggesting to overcome the static and dynamic limitations of ultra deep submicron SG devices for high frequency analog applications.

Even if one of the disadvantages is the increase in the gate-source capacitance of DG devices, which is nearly twice that of SG devices, at high gate overdrive ($V_{GO}=V_{GS}-Vth$), at ultra short channel lengths ($L \leq 50$ nm) and lower gate overdrives ($V_{GO} \leq$ 400mV), DG devices show significantly higher values of the cut-off frequency, f_T ($= g_m/(2\pi(C_{GS}+C_{GD}))$) as compared to SG devices (due to the transconductance increase), thus presenting DG MOSFET as a serious candidate for microwave analog applications [23].

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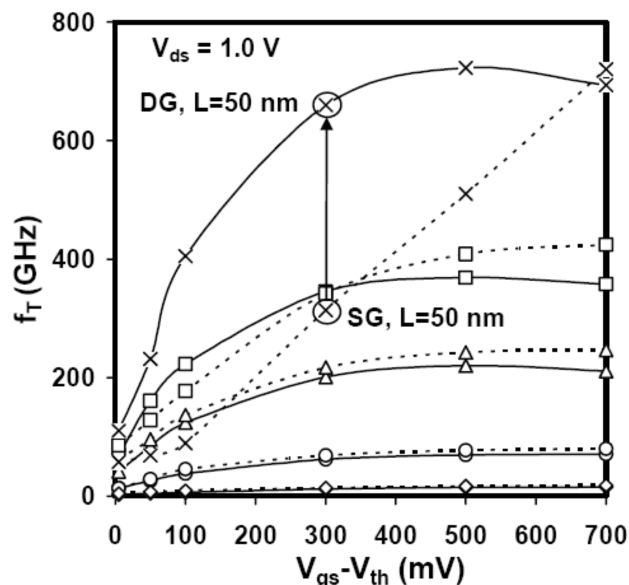

Fig.1A.3 *Dependence of cut-off frequency of DG and SG devices for various channel lengths at Vds =1.0V (DG—, SG ---, X 50 nm, □75 nm, Δ100 nm, o 200 nm, ◊ 500 nm). [23]*

Results have also shown that the DG architecture exhibits speed superiority compared to SG devices [24]. The increase in the parasitic capacitances for the DG MOSFETs compared to SG, will not deteriorate the overall speed. Another device that is of interest, but does not appear referred in [2] is the 4-terminal driven DG MOSFET (4T-DG) or Asymmetric DG MOSFET. This double-gate MOSFET can be driven in a genuine 4-

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terminal mode with two independent gates controlled separately. This means that the transistor operation speed can be controlled to an optimum, and the power loss caused by leak current during standby is substantially nullified, due to the Vth controllability. The 4T-DG MOSFET can also be regarded as a MOSFET equipped with an arithmetic operation feature based on independent two-input capability. A single device with such a circuit function indicates the possibility of extensively reduction of the number of devices in VLSIs.

Among the non-classic CMOS device concepts the ultra-thin-body silicon-on-insulator (UTB-SOI) is one of the most promising approaches for future CMOS scaling to feature sizes below 50 nm [25-29]. Ultra-thin body SOI has a very thin layer of single-crystal silicon, the ultra-thin silicon body (5-40 nm), on top of a silicon dioxide insulating layer (the buried oxide, or "BOX"), which itself is on top of the silicon substrate. The ultra-thin body forms the channel of the MOSFET. The advantages of ultra-thin body SOI for highly scaled MOSFETs include reduced junction capacitance, improved electrical isolation, the possibility of optimal operation with relatively light channel doping, and certain advantageous circuit characteristics. The ultra-thin body SOI may be either a single-gate (see structure in Figure 1A.4) or a DG MOSFET. One type of DG MOSFET is similar to the ultra-thin body SOI single-gate transistor, with the

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addition, in the BOX, of a bottom gate electrode fully self-aligned to the top gate electrode.

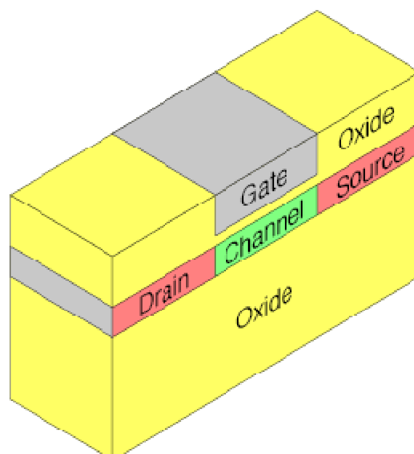

Fig.1A.4 *Schematic of a single-gate UTB SOI MOSFET*

It is clear that multiple-gate devices will respond to the future ITRS demands. These architectures have very good electrical characteristics even at nanoscale gate lengths, due to the excellent control of the charges in the channel. One of the main advantages of multiple-gate MOSFETs is the increase of the total current as compared to SG devices. The increase of the drain current per channel is related to the increased number of gates. Also, due to the short channel and thin film, the small dimensions of these devices allow a high packaging density. As shown above, they present a very good potential for RF and microwave analog applications. In digital applications, the small subthreshold swing of multiple gate devices keeps a high ratio

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between on current and off current even for devices with channel lengths of the order of nm [30].

1B. Compact modeling

Compact models of devices are used in circuit simulators, in order to predict the functionality of circuits. These multiple-gate devices will be preferred in nanoscale circuits, thus calling for accurate and reliable compact models, including new device specific effects. These compact models that accurately describe the novel devices, and are computationally efficient are an important prerequisite for successful circuit design. The currently available compact models are facing enormous challenges in modeling the observed physical phenomena in the sub-90-nm technologies [31]. The demands for advanced models, which can describe nanoscale silicon devices in analog and mixed-signal applications and can account for the physical effects on small geometry devices, have led to enormous R&D efforts in the development of advanced physics-based compact models.

The models should consist of high order continuity expressions, to prevent lack of convergence in circuit simulations. Smoothening functions are often used to assure continuity between the operating regimes. Also, a good model should be based on explicit expressions, as iterations require a higher computational time.

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For the multiple-gate MOSFETs, the principles of modeling will change as compared to the traditional SG MOSFET, first because they will have to introduce the volume inversion effect, then, contrary to bulk MOSFETs, depletion charges in multiple-gate devices are negligible because the silicon film is undoped (or lightly doped). Thus, only the mobile charge term needs to be included in Poisson's equation. Therefore, the exact analytic solutions to 1D Poisson's and current continuity equations based on GCA (gradual-channel-approximation, which assumes that the quasi Fermi potential stays constant along the direction perpendicular to the channel) can be derived, without the charge-sheet approximation. It is considered that the electrostatic control of the gates is good enough to neglect SCE associated to 2D effects. Most models presented so far are for undoped devices with a long enough channel to assume that the transport is due to the drift-diffusion transport mechanism [32-35].

Using the above principles, some models for undoped double-gate [33-36] and surrounding gate [32,37] have been published , showing good agreement with three dimensional numerical simulations.

In the case of a long-channel symmetrical undoped device, an analytical solution of 1D Poisson's equation is obtained [33],

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[34]. Making some approximations, a charge control model based on this solution can be derived [38].

If the film is strongly doped, an exact analytical solution of the 1-D Poisson's equation is not possible. Some approximations have been used to find an approximate analytical solution in the moderate inversion regime [39], in the weak inversion regime [40], or assuming a uniform mobile-charge sheet density along the thickness of the film [41] (which is valid from weak to moderate inversion).

For devices that are short enough, i.e., where the gate length is comparable to the body thickness, the electrostatic potential should be derived from a 2-D Poisson's equation. If the transport mechanism is drift-diffusion, a compact analytical solution seems difficult to obtain, since it has to be determined self-consistently with the current continuity equation, which includes the quasi-Fermi potential. An exception is the subthreshold regime where the quasi-Fermi potential is constant in most of the channel [42]. If the doping is high and the mobile charge can be neglected in the subthreshold regime, a simple solution for the potential can be obtained, which leads to an analytical expression of the threshold voltage that includes the scaling dependences (and therefore the threshold voltage rolloff and DIBL). In DG MOSFETs, this solution is written as a superposition $\Phi(x, y) = \Phi 1(y) + \Phi 2(x, y)$, where $\Phi 1(y)$ is the solution of the 1-D Poisson's equation, which includes the

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doping charge term, and Φ 2(x, y) is the solution of the remaining 2-D Laplace equation [43]. In GAA MOSFETs, the solution is written as: $\Phi(x, r) = \Phi 1(r) + \Phi 2(x, r)$. However, in these previous works, additional approximations were needed to solve the 2-D Laplace's equation [44–46]. Furthermore, their analyses were quasi-2-D rather than fully 2-D, which required the use of fitting parameters. In an undoped device, analytical solutions of the 2-D Poisson's equation were obtained at low V_{DS}, which accurately predicted the threshold voltage rolloff [42,47]; but at high V_{DS}, the problem becomes more complex. The solution also has two contributions, but the 2-D contribution is not the solution of a Laplacian, since the mobile charge is not ignored. At high V_{DS}, an expression for the quasi-Fermi potential along the channel length is necessary to solve the 2-D Poisson's equation. In [43], an approximate expression of the quasi-Fermi potential is used, although it was derived for long-channel bulk MOSFETs. An alternative assumption is to neglect the mobile-charge sheet density in the subthreshold even for an undoped device [48]. Again, the analysis used to solve the 2-D Poisson's equation was quasi-2-D. The threshold voltage is calculated from the value of the minimum of the surface potential [39,40,46]. The solution of the Poisson's equation in the subthreshold allows calculating the subthreshold swing [42,47,49].

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A very promising modeling approach presented recently is based on the solution of Laplace's equation for the extended body (including the gate insulators) of the short-channel nanoscale DG MOSFETs using conformal mapping techniques [50-52]. This technique was first explored for bulk longchannel MOSFETs [53] and later for sub-0.1-μm MOSFETs [54], and finally for DG MOSFETs.

However, for devices with channel lengths shorter than 50nm, the transport mechanism will probably not be drift-diffusion; ballistic or quasi-ballistic transport may appear. We cannot define a continuous quasi- Fermi potential that varies from the source to the drain and controls the mobile-charge distribution. What will happen is that carriers injected from the source will depend on the Fermi potential at the source, and carriers injected from the drain will depend on the Fermi potential at the drain.

For this, accurate models that will include the ballistic or quasi-ballistic regime are needed [55-66]. On the other hand, for films smaller than 10 nm, quantum confinement in the film may not be negligible.

Thus, accurate MOSFET models that include these new physical behaviours are crucial to design and optimize advanced VLSI circuits for nanoscale CMOS technology.

However, drain-current model is not enough for circuit simulation [67]. In order to calculate the dynamic behaviour of the device and so, to enable AC and transient circuit simulation,

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terminal charge and capacitance modelling of multiple-gate MOSFETs are needed. Unfortunately, less work has been dedicated to this modelling domain. The recently presented study in [68] which is consistent with the drain current model of the study in [33], for symmetric and asymmetric DG devices is not analytical, since it requires numerical integration or integral function tabulation, which is too time-consuming to be carried out. Thus, analytical charges and capacitances, associated with each terminal are preferred in circuit simulation. Regarding the surrounding-gate MOSFET, our group was the first to develop and publish a model of the charges and intrinsic capacitances [69], which is also analytic and explicit. Starting from an exact solution of the Poisson's equation, the model will be derived from Ward and Dutton charge partition scheme [70]. Every terminal charge or capacitance is described by an analytic function (See section 2D).

Another important area of study and modeling, due to its high influence in short-channel novel devices, is represented by the parasitic resistances and capacitances. One of the disadvantages of multiple-gate devices is the increase in the parasitic resistive and capacitive components (like fringing and overlap capacitances) that become comparable in magnitude or even larger than intrinsic ones [71]. Capacitive coupling with parasitic resistances even dominates device characteristics in

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analog/radio frequency (RF) ICs [72], a very important arena for the application of nanoscale devices.

1C. Numerical simulations

The advent and technological development of supercomputers in the last decade has dramatically improved the quality of scientific research, allowing the possibility for numerical simulations of unprecedented dynamical range and sophistication of physical modeling. In addition to the wealth of details necessary for an accurate treatment of complex processes, numerical simulations often also offer unparalleled insight into the understanding of a physics problem.

Numerical simulation is a powerful tool in the semiconductor industry because it can analyze and predict the behaviour of novel devices, without the high cost necessary to fabricate the real components. The TCAD (Technology Computed Aided Design) has the potential to reduce development costs by as much as 40% “if appropriately used” [2]. The simulation tool can include different materials, various fabrication processes, study of 1D, 2D and 3D structures, etc.

In order to remain useful for future technology nodes, process simulation has to follow shifts of state-of-the-art processes and new materials for future nanoelectronics devices. New requirements on TCAD can be found in the Modelling and Simulation Section of the ITRS.

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However, the simulation tools remain the easiest way to test the accuracy of compact models, in laboratories around the world, due to its low cost and also, to the limited number of measurements of optimized novel devices.

1D. Capacitance model

In real circuit operation, the device operates under time-varying terminal voltages. Depending on the magnitude of the time-varying voltages, the dynamic operation can be classified as large-signal operation or small-signal operation [73]. If the variation in voltages is sufficiently small, the device can be modeled with linear resistors, capacitors, current, sources, etc. Such a model is called a small-signal model. This type of dynamic operation is influenced by the device's capacitive effects. Thus, a capacitance model describing the intrinsic and extrinsic components of the device capacitance is another essential part of a compact MOSFET model for circuit simulation.

The capacitance model is almost always based on the quasi-static approximation, which assumes that the charges in a device can follow the varying terminal voltages immediately, without any delay. Generally MOSFET capacitances can be divided into two groups, the intrinsic and the extrinsic capacitances. The intrinsic capacitances are much more complex than the extrinsic

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components. The early intrinsic capacitances models, such as the Meyer model [74], simply treated the MOSFET capacitance as three separated lumped capacitances, gate-to-source capacitance (C_{GS}), gate-to-drain capacitance (C_{GD}) and gate-to-bulk capacitance (C_{GB}). It has the disadvantage of the charge non-conservation, unlike the charge-based capacitance model, which we also used for multiple-gate MOSFETs.

However, the Meyer model has been widely used in simulators and continues to be used occasionally as an optional model for its simplicity and efficiency.

1D.1 Intrinsic charge-based capacitance model for DG MOSFET

In a charge-based approach, the emphasis is put on the charge, rather than the capacitances. The idea is to determine the charges in the drain, source and gate, and the capacitances are then computed through mathematical differentiation of the charge with respect to the voltage. The charge-based capacitance model will ensure the charge conservation, as long as the following equation is satisfied: $Q_G + Q_D + Q_S = 0$.

Q_G can be obtained directly by integrating the corresponding charge density over the channel [75]. $Q_{INV} = -Q_G$, so, it is easy to calculate the total inversion charge in the channel. However, it is difficult to model the charges on the source and drain terminals, because only the total mobile channel charge $Q_{INV} = Q_D + Q_S$ is

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known and a partition of Q_{INV} into Q_D and Q_S is needed. As discussed by Ward and Dutton [70], the partitioning proposed leads to a set of charge-conserving and nonreciprocal capacitances between the different intrinsic terminals (nonreciprocity means that *Cij* is not equal to *Cji*, where *i* and *j* denote source, drain or gate).

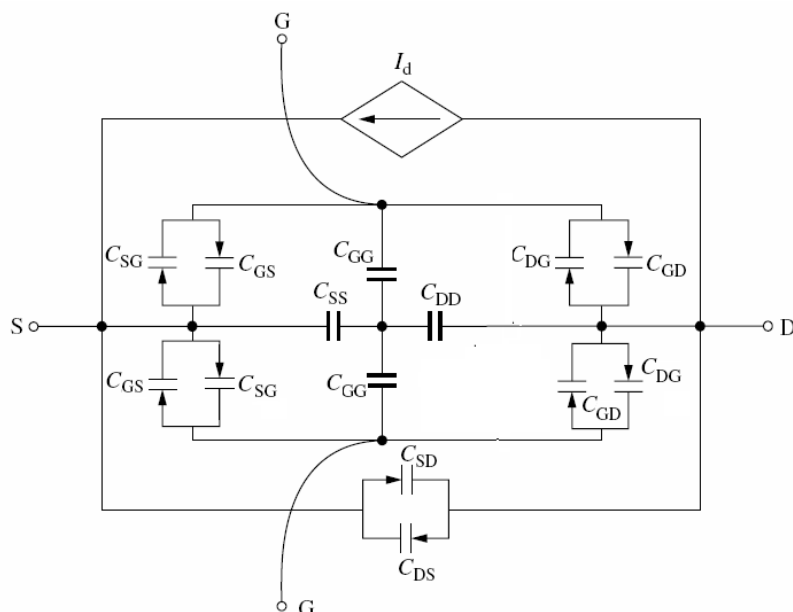

Fig.1D.1.1 *Intrinsic large-signal DG MOSFET equivalent circuit including a complete set of nonreciprocal and charge-conserving transcapacitances. The transcapacitances Cij are defined in the text. Based on Fjeldly T. A., Ytterdal T., and Shur M. (1998) Introduction to Device Modeling and Circuit Simulation, John Wiley & Sons, New York*

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The partitioning scheme is the following: the mobile charge Q_{INV} of a MOSFET is divided into a source charge $Q_S = FpQ_{INV}$ and a drain charge $Q_D = (1 - Fp)Q_{INV}$, where Fp is a partitioning factor.

$$Cij = k\frac{\partial Qi}{\partial Vj} \quad where\ k = \begin{cases} -1 & for \quad i \neq j \\ 1 & for \quad i = j \end{cases}$$

The elements *Cii* are called self-capacitances. *Cij* contain information on how much the charge *Qi* assigned to terminal *i* changes by a small variation in the voltage *Vj* at terminal *j* . To illustrate why *Cij* may be different from *Cji*, assume a MOSFET in saturation. Then the gate charge changes very little when the drain voltage is perturbed since the inversion charge is very little affected, making C_{GD} small. However, if V_{GS} is perturbed, the inversion charge changes significantly and so does Q_D, making C_{DG} high.

Based on the formula of the charges and the charge partition for drain and source charges, an admittance matrix for the device can be created. All of the capacitance terms in the matrix are non-zero and non-reciprocal. The elements in each column and each row must sum to zero owing to the constraints imposed by charge conservation (which is equivalent to obeying Kirchhoff's current law) [76]. Some capacitances, such as C_{SD} and C_{DS} are negative as they should be [77] and out of the 9 DG MOSFET elements, only 4 are independent.

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$$C = \begin{bmatrix} C_{GG} & C_{GS} & C_{GD} \\ C_{SG} & C_{SS} & C_{SD} \\ C_{DG} & C_{DS} & C_{DD} \end{bmatrix} \qquad (1D.1.1)$$

Similarly, these intrinsic capacitances can be obtained for an asymmetric (different front and back gate voltages) DG MOSFET, where $Q_G \neq Q_B$. Q_B represents the charge in the back-gate, so $Q_{INV}=-(Q_G+Q_B)$.

In this thesis we will develop explicit compact charge and capacitance models adapted for doped and undoped long-channel devices (doped DG MOSFETs, undoped DG MOSFETs, undoped UTB MOSFETs and undoped SGT) from a unified charge control model derived from Poisson's equation. We also show the impact of important geometrical parameters such as source and drain thickness, fin spacing, spacer width, etc. on the parasitic fringing capacitance component of multiple-gate field-effect transistors (MuGFET). Our results have been verified with numerical simulation results from different numerical simulators and when allowable, with experimental results that were obtained at the Microelectronics Laboratory, Université Catholique de Louvain, Belgium. The thesis is organized as follows: Chapter (1) presents the state of the art,

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Chapter (2) the compact modeling of the four devices: doped DG MOSFETs, undoped DG MOSFETs, undoped UTB MOSFETs and undoped SGT; in Chapter (3) we study the fringing capacitances in MuGFETs. Finally Chapter (4) summarizes the work done and the future points that need to be studied.

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Chapter 2

Current, Charge and Capacitance Model for Multiple Gate MOSFETs

2A. Compact model for highly-doped symmetrical Double-Gate SOI MOSFETs

In this section

an analytical and continuous compact model is developed, for a highly-doped double gate SOI MOSFET, in which the channel current, charge and capacitances are expressed as continuous, explicit functions of the applied voltages. The model is based on a unified charge control model derived from Poisson's equation.

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The results are compared with DG MOSFET simulations and FinFET experimental measurements [78]. Also, an extension to this model has been done, making it functional for a wide range of doping concentrations, between 10^{14} and $3x10^{18}cm^{-3}$ [79].

2A.1. Introduction

As explained before, among SOI devices, double-gate (DG) transistors are considered to be a very attractive option to improve the performance of CMOS devices and overcome some of the difficulties encountered in further downscaling of MOS field-effect transistors into the sub-50 nanometer gate length regime [2]. One of the limiting factors in MOSFET downscaling is the static power consumption, due to short channel effects (SCEs), such as threshold voltage roll-off, drain-induced barrier-height lowering (DIBL) and subthreshold slope degradation [80]. These effects increase the off state leakage current. In the DG MOSFETs, the control of the channel by the gate is stronger than in single gate MOSFETs. This leads to a significant reduction of DIBL, threshold voltage roll-off, off-state leakage and channel-length modulation [81,82].

Thanks to such advantages, DG devices will be one of the preferred devices in nanoscale circuits, thus calling for an accurate and CAD compatible DG SOI MOSFET model. Some

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compact models have been introduced before, but they are valid only for undoped DG MOSFETs, like in [33,34,37,38,83], whereas actual devices are doped, due to the fact that there is a small unintentional doping during real process. Moreover, doping can be used to adjust the threshold voltage without the need of changing the gate material, targeting multi-V_T processes which are very attractive [13]. In this section we present a model for the doped double gate MOSFET, which is analytical, explicit and continuous through all regimes of operation (from weak to strong inversion, as well as linear to saturation). It is based on a previous work done in [40], which presented a current model valid for low V_{DS}. The current expression is based on a unified charge control model, written in terms of charge densities at the source and drain ends [84] and derived for a doped DG MOSFET. We use an accurate explicit expression of the inversion charge densities in terms of the applied bias. No fitting parameters are used in the charge control model. The model is valid up to well above threshold. This model includes expressions of current, charge and capacitances, thus resulting also in a complete small-signal model. Although the model has been developed from the 1D Poisson's equation in the direction perpendicular to the channel (which leads to neglecting short-channel effects), it is in fact the first compact model developed for doped DG MOSFETs. Besides, short-channel effects are less stronger than in single gate devices with the same channel

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length. The explicit model of the channel current shows a good agreement with the 2D numerical device simulations and also with the experimental I-V measurements performed on comparable FinFETs. A good agreement is observed also for all the capacitances expressions compared to the 2D device numerical simulations. Therefore, this complete small signal model is suitable to be used in circuit simulators, a direct application targeting baseband analog designs in which very short transistors are not used, but moderate inversion is standard [85]. As mentioned above, an extension of this model has been done. A compact analytical model for long channel symmetric double-gate MOSFETs is presented in section 2A.3, which considers a doped silicon layer in a wide range of concentrations, between 10^{14} and $3x10^{18}$ cm^{-3}. Analytical expressions are presented to model the behavior of the potential at the surface and the difference between potentials at the surface and at the center of the doped silicon layer. No fitting parameters are required. All the equations obtained for the potentials were validated using rigorous numerical calculation, for different doping concentrations as well as for several double-gate structure dimensions and applied voltages.

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Using the expression for the potential and difference of potentials, analytical expressions for the current-voltage and capacitance-voltage characteristics are further derived. Comparison of modeled and simulated (using the ATLAS device simulator) transfer characteristics in linear and saturation regions, of output characteristics and of gate-drain and gate-source capacitance-voltage characteristics shows an excellent agreement within the practical range of gate and drain voltages, gate dielectric and silicon layer thicknesses.

2A.2. Model

In doped double gate MOS transistors, in the normal operating regimes, the majority carrier concentration (holes) is negligible in comparison with electron carrier concentration so that by using the gradual channel approach [33,40] (therefore, neglecting the derivative of the lateral field in the direction of the channel length) Poisson's equation reads as:

$$\frac{d^2\phi(x,y)}{dy^2}=\frac{q}{\varepsilon_{Si}}\left[N_A+n_e(x,y)\right]=\frac{q}{\varepsilon_{Si}}\left[N_A+\frac{n_i^2}{N_A}e^{\frac{q}{kT}\left[\phi(x,y)-V(x)\right]}\right] \qquad (2A.1)$$

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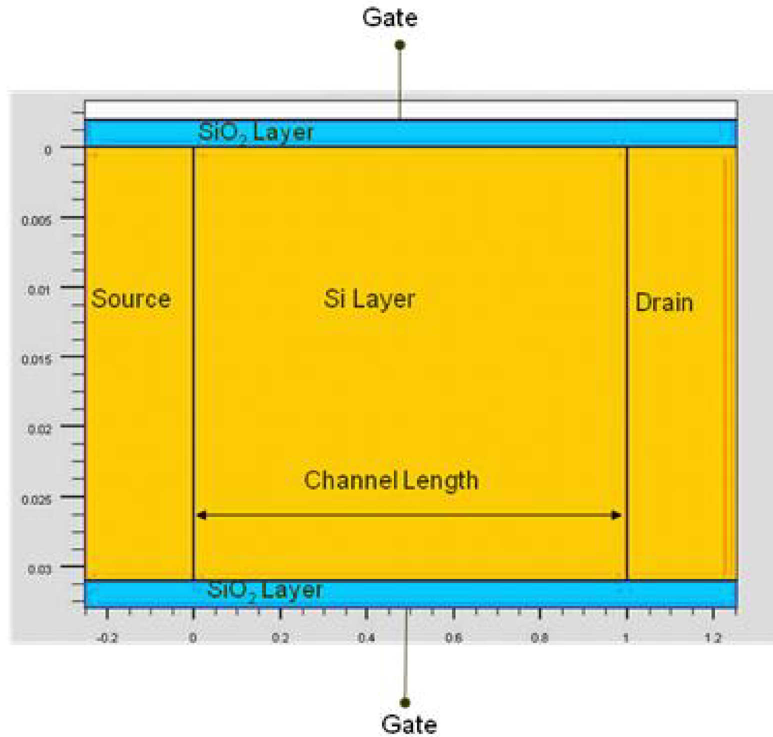

Fig.2A.1 *ATLAS simulation of the DG MOSFET considered*

The y-axis is perpendicular to the surface and the x-axis starts in source (x=0) and ends in drain (x=L) region. Fig.2A.1 represents the ATLAS simulation of the DG MOSFET considered in this section. N_A represents the doping density. The potential $\phi(x,y)$ is referred to the neutral region of one equivalent bulk MOS transistor. V(x) is the electron quasi-Fermi potential depending on the voltage applied to the channel between source and drain

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and is assumed to be independent of y [40]. The surface electric field can be written in terms of the mobile charge density (in absolute value) per unit area at each interface, Q, and the depletion charge density per unit area (in absolute value) $Q_{Dep}=qN_At_{Si}$ (t_{Si} being the Si film thickness) whatever x:

$$E_S\left(x\right)=\frac{Q(x)+\frac{Q_{Dep}}{2}}{\varepsilon_{Si}} \tag{2A.2}$$

In order to obtain the $I_{DS}(V_{GS})$ characteristic, we have to evaluate the surface electric field as a function of the gate voltage. Therefore we multiply both sides of Poisson's equation by $2\left[d\phi(x)/dy\right]$. Then, by integrating (2A.1) between the centre (y=0) and the top surface of the film (y=-t_{si}/2) we obtain [40]:

$$E_S\left(x\right)=\sqrt{\frac{2qN_A}{\varepsilon_{Si}}}\sqrt{\left(\phi_s-\phi_0\right)+\frac{kT}{q}\frac{n_i^2}{N_A^{\ 2}}e^{\frac{q}{kT}\left[\phi_S-V(x)\right]}\left(1-e^{-\frac{q}{kT}\left(\phi_s-\phi_0\right)}\right)} \tag{2A.3}$$

where $\phi_S=\phi(x,-t_{Si}/2)$ is the surface potential and $\phi_o=\phi(x,0)$ is the potential in the middle of the film. Contrary to the bulk case where the potential at the end of the depletion region is known to be zero, in fully-depleted SOI unfortunately ϕ_0 is unknown and (2A.3) cannot be analytically integrated for the potential, but it is observed, from numerical simulations, that the difference $\phi_S-\phi_0$ keeps a constant value from the subthreshold region to well above threshold [40]. In subthreshold, Poisson's

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equation can be reduced to its depletion form:

$$\frac{d^2\phi(x)}{dy^2} = \frac{qN_A}{\varepsilon_{Si}} \quad (2A.4)$$

therefore, the following expression is obtained for the difference $\phi_S - \phi_0$.

$$\phi_S - \phi_0 = \frac{qN_A t_{Si}^2}{8\varepsilon_{Si}} = \frac{Q_{Dep}}{8C_{Si}} \quad (2A.5)$$

where $C_{Si} = \varepsilon_{Si} / t_{Si}$ represents the silicon film capacitance. This approximation is valid from subthreshold to well above threshold, which is demonstrated by the correct agreement with simulations and measurements, for low and moderate V_{GS}(~2V) and for all V_{DS} values [40]. For high V_{GS}, the surface potential increases much more rapidly than the mid-film potential, making the approximation less correct. However, the numerical simulations have shown that (2A.5) is not a bad approximation for highly-doped devices ($N_A \geq 10^{17}$ cm^{-3}), even well above threshold. The term $e^{-\frac{q}{kT}\cdot\frac{Q_{Dep}}{8C_{Si}}}$, coming from (2A.3) and (2A.5), has been neglected, but this is also a valid approximation for highly doped devices. In Fig.2A.2 we can see that the increase of the difference between the surface and mid-film potentials is certainly small (less than 0.1V), up to well above threshold. The validity of the above approximation from subthreshold to well

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above threshold will also be proved/supported by the good agreement between model and numerical simulations.

Equating (2A.2) and (2A.3), applying the Kirchoff voltage law applied on the gate oxide, and using the two approximations discussed above, we obtain the following charge control model:

$$V_{GS} - V_{FB} - V - \left(\frac{Q_{Dep}}{2C_{ox}} + \frac{kT}{q} \log \left[\frac{q^2}{kT} \frac{N_A{}^3}{n_i^2} \frac{t_{Si}{}^2}{2\varepsilon_{Si}} \right] \right) = \\ = \frac{Q}{C_{ox}} + \frac{kT}{q} \log \left[\frac{Q}{Q_{Dep}} \right] + \frac{kT}{q} \log \left[\frac{Q + Q_{Dep}}{Q_{Dep}} \right] \quad (2A.6)$$

Note that V varies from source to drain, being V=0 at the source and $V=V_{DS}$ at the drain [84]. V_{FB} is the flat-band voltage, C_{ox} the oxide capacitance per unit area.

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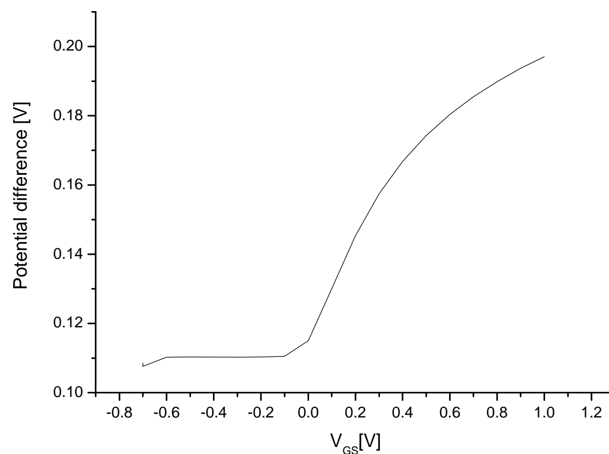

Fig.2A.2 *Difference between the surface and mid-film potentials* $\phi_S - \phi_0$ *of the DGMOSFET, as a function of the gate voltage. Simulation conditions: doping level* $N_A=6\cdot10^{17}$ cm^{-3}*; silicon film thickness* t_{Si}*=31nm; effective oxide thickness* t_{ox}*=2nm; channel length L=1µm and width W=1µm*

2A.2.1 Drain Current Model

The drain current is calculated, as usually, from:

$$I_{DS} = \frac{2W\mu}{L}\int_0^{V_{DS}} Q(V)\,dV \qquad (2A.7)$$

where W represents the width of the device, µ the effective mobility of the electrons and L the channel length. The term 2 appears because of the 2 gates.

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From (2A.6) we get:

$$dV = -\frac{dQ}{C_{ox}} - \frac{kT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q+Q_{Dep}}\right) \tag{2A.8}$$

Therefore the expression of I_{DS} can be written in terms of carrier charge densities. Integrating (2A.7) using (2A.8), between Q_s and Q_d ($Q=Q_s$ at source end and $Q=Q_d$ at the drain end), we have:

$$I_{DS} = \frac{2W\mu}{L}\left[2\frac{kT}{q}\left(Q_s - Q_d\right) + \frac{Q_s^2 - Q_d^2}{2C_{ox}} + \frac{kT}{q}Q_{Dep}\log\left[\frac{Q_d + Q_{Dep}}{Q_s + Q_{Dep}}\right]\right] \tag{2A.9}$$

In order to compute the charge densities from an explicit expression of the applied bias, since (2A.6) does not yield a closed form for Q, we find an approximate explicit expression of Q in the asymptotic limits of subthreshold and above threshold.[84].We can see that in (2A.6), well above threshold the two logarithmic terms in RHS (Right-Hand-Side) are smaller than the first term in RHS, and (2A.6) can be approximated as:

$$V_{GS} - V_{FB} - V - \left(\frac{Q_{Dep}}{2C_{ox}} + \frac{kT}{q}\log\left[\frac{q^2}{kT}\frac{N_A{}^3}{n_i{}^2}\frac{t_{Si}{}^2}{2\varepsilon_{Si}}\right]\right) = \frac{Q}{C_{ox}} \tag{2A.10}$$

and therefore

$$Q = C_{ox}\left(V_{GS} - V_0 - V\right) \tag{2A.11}$$

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where $V_0 = V_{FB} + \left(\frac{Q_{Dep}}{2C_{ox}} + \frac{kT}{q} \log\left[\frac{q^2}{kT} \frac{N_A^{\ 3}}{n_i^{\ 2}} \frac{t_{Si}^{\ 2}}{2\varepsilon_{Si}} \right] \right)$.

On the other hand, we can see that in (2A.6), well below threshold, since $Q \ll Q_{Dep}$

$$Q = Q_{Dep} \exp\left(\frac{V_{GS} - V_0 - V}{\beta} \right) \tag{2A.12}$$

where $\beta = \frac{kT}{q}$

An approximate explicit solution of the standard UCCM equation is (2A.13).

$$Q = C_{ox} \left(-\frac{2C_{ox}\beta^2}{Q_{Dep}} + \sqrt{\left(\frac{2C_{ox}\beta^2}{Q_{Dep}} \right)^2 + 4\beta^2 \log^2\left[1 + \exp\left[\frac{V_{GS} - V_0 - V}{2\beta} \right] \right]} \right) \tag{2A.13}$$

This expression tends to (2A.10) and (2A.12) above and below threshold, respectively. However, we observed that this explicit expression of Q does not work very well above threshold. The modeled Q using (2A.13) is significantly lower than the calculated Q from the numerical solution of (2A.6). The reason for this difference is that the two logarithmic terms in the RHS of (2A.6) increase, although slowly, with V_{GS} above threshold and they are not negligible. Nevertheless, this effect can be

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modeled as a correction of V_0. By considering this effect, from (2A.6), we can write the above threshold charge density as:

$$Q = C_{ox}\left(V_{GS} - V_0 - \beta \log\left(\frac{Q'}{Q_{Dep}}\right) - \beta \log\left(1 + \frac{Q'}{Q_{Dep}}\right)\right) \qquad (2A.14)$$

where $Q' = C_{ox}\left(V_{GS} - V_0 - V\right)$.

Equation (2A.14) is a much more accurate expression for above threshold than (2A.10). In order to keep a unified expression for Q, we need a unified expression of the threshold voltage. From (2A.12), the threshold voltage is V_T=V_0 below threshold, but from (2A.14), above threshold, it is:

$$V_T = V_0 + \beta \log\left(\frac{Q}{Q_{Dep}}\right) + \beta \log\left(1 + \frac{Q'}{Q_{Dep}}\right) \qquad (2A.15)$$

As we can see, V_T is defined in terms of technological parameters not as an extracted parameter.

We cannot use (2A.15) as a unified threshold voltage expression, because the second term in the RHS of (2A.15) would tend to -∞ as we decrease V_{GS} below threshold (since, then $\frac{Q'}{Q_{Dep}}$ tends to 0). However, for the same reason, the third term of the RHS tends to 0 as we decrease V_{GS} below threshold,

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as it should. Note, on the other hand, that well above threshold, $Q^{'} \gg Q_{Dep}$ and $V_T \approx V_0 + 2\beta \log\left(1 + \frac{Q^{'}}{Q_{Dep}}\right)$

A suitable unified expression of the threshold voltage is:

$$V_T = V_0 + 2\beta \log\left(1 + \frac{Q'}{Q_{Dep}}\right) \qquad (2A.16)$$

Below threshold $Q^{'} \ll Q_{Dep}$ and $V_T = V_0$ as it should. Well above threshold, $Q^{'} \gg Q_{Dep}$ and $V_T \approx V_0 + 2\beta \log\left(1 + \frac{Q^{'}}{Q_{Dep}}\right)$ as it should.

The final explicit expression of Q is written as (2A.17):

$$Q = C_{ox}\left(-\frac{2C_{ox}\beta^2}{Q_{Dep}} + \sqrt{\left(\frac{2C_{ox}\beta^2}{Q_{Dep}}\right)^2 + 4\beta^2 \log^2\left[1 + \exp\left[\frac{V_{GS} - V_T + \Delta V_T - V}{2\beta}\right]\right]}\right) \qquad (2A.17)$$

where $Q^{'}$ (2A.18) is calculated from the unified expression of (2A.13), that ignores the logarithmic corrections of the threshold voltage.

$$Q' = C_{ox}\left(-\frac{2C_{ox}\beta^2}{Q_{Dep}} + \sqrt{\left(\frac{2C_{ox}\beta^2}{Q_{Dep}}\right)^2 + 4\beta^2 \log^2\left[1 + \exp\left[\frac{V_{GS} - V_0 - V}{2\beta}\right]\right]}\right) \qquad (2A.18)$$

In (2A.17), the term ΔV_T ensures the correct behaviour of Q above threshold [84],

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$$\Delta V_T = \frac{\left(\dfrac{2C_{ox}\beta^2}{Q_{Dep}}\right)Q'}{Q_{Dep}+Q'} \tag{2A.19}$$

since $\Delta V_T \approx {}^{2C_{ox}\beta^2}\!\big/_{Q_{Dep}}$ above threshold and therefore

$Q \approx C_{ox}\left(-2C_{ox}\beta^2/Q_{Dep} + V_{GS} - V_T + \Delta V_T - V\right) \approx C_{ox}\left(V_{GS} - V_T - V\right)$
as it should. Below threshold, ΔV_T has no influence since
$\Delta V_T \approx \left(2C_{ox}\beta^2/Q_{Dep}{}^2\right)Q' \ll V_T$.

Therefore, Q_s and Q_d in the I_{DS} expression (2A.9) can be analytically computed by applying V=0 and $V=V_{DS}$ respectively, in (2A.10)-(2A.19).

In order to obtain a very good agreement of the channel current expression with simulations and measurements, the mobility has been computed using the Shirahata's model [86], also used in the ATLAS 2D simulator to compare the results of the model. This model takes into account the dependence of the transverse electric field.

The effective mobility μ is:

$$\mu = \frac{mu0\left(\dfrac{T}{300}\right)^{-thetan}}{\left(\dfrac{1+E_S}{e1n}\right)^{p1n} + \left(\dfrac{E_S}{e2n}\right)^{p2n}} \tag{2A.20}$$

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The method to compute the constants *mu0*, *e1n*, *e2n*, *p1n*, *p2n* was to take 5 points from the (I_{DS}, V_{GS}) and (E_S, V_{GS}) curves in ATLAS. Replacing these values and equation (2A.20) in the current expression (2A.9) we have a system of 5 equations with 5 unknowns to solve. Parameter *thetan* can be determined from extracted values of the mobility at different temperatures. In this work we have considered measurements and simulations at room temperature; therefore *thetan* did not need to be fitted. The flatband voltage value required in (2A.11) is obtained from the extraction of an empirical threshold voltage, V_t (from the measured or the numerically simulated characteristics) as follows. We use the maximum transconductance change (TC) method [39,40], where V_t is defined as the gate voltage at which $\partial g_m / \partial V_{GS}$ (Fig.2A.3) is maximum or

$$\frac{d^3 I_{DS}}{dV^3{}_{GS}} = 0 = \frac{d^3 E_S}{dV^3{}_{GS}} \tag{2A.21}$$

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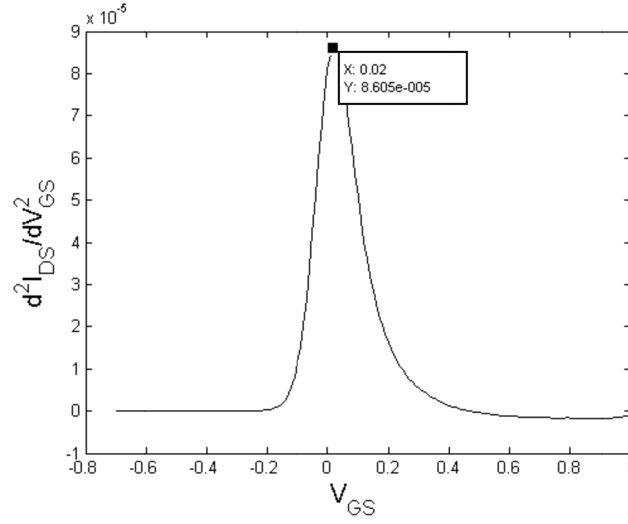

Fig.2A.3 *Maximum transconductance change (TC) method, applied to our numerically simulated model*

As we can see in Fig.2A.3 the empirical V_t=0.02V. Using some approximations [39] an expression of V_t is obtained, in terms of explicit expressions of the surface electric field and surface potential at threshold, E_S^* and $\phi^*{}_S$, respectively:

$$E_S{}^* = \frac{\frac{Q_{Dep}}{2}}{\varepsilon_{Si}} + \frac{1}{2}\frac{kT}{q}\frac{C_{ox}}{\varepsilon_{Si}} \tag{2A.22}$$

$$\phi_s^* = 2\phi_F + \frac{kT}{q}\ln\left[\frac{C_{ox}}{4C_{Si}}\left(1+\frac{kT}{q}\frac{C_{ox}}{Q_{Dep}}\right)\right] \tag{2A.23}$$

$$V_t = \phi_s{}^* + V_{FB} + \frac{\varepsilon_{Si}E_S^*}{C_{ox}} \tag{2A.24}$$

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The first term of the expression of E_S^* (2A.22) comes from the depletion charge controlled by each of the gates. The second term in (2A.22) is actually a correcting factor which depends only on the gate oxide thickness. As will be seen from the results, using the extracted value of V_{FB} obtained from (2A.22-2A.24) and the empirical V_t, a good agreement is obtained with both measurements and numerical simulations. We have indeed observed that the extracted value of V_{FB} corresponds to the calculated value (i.e. the difference between the work functions of the gate material and the semiconductor) in the case of the device simulated with ATLAS (where no interface states nor trapped charge in the oxide has been introduced).

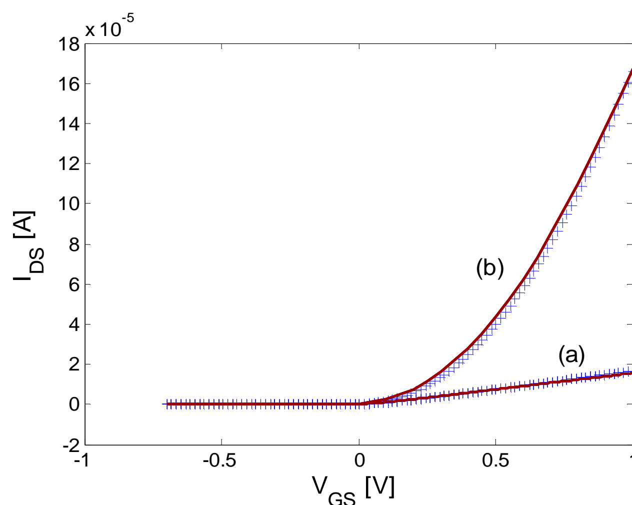

Fig.2A.4 *Transfer characteristics, for V_{DS}=0.05V (a) and for V_{DS}=1V (b) in linear scale. Solid line: ATLAS simulation; Symbol line: our model using (2A.9).Same simulation conditions as Fig.2A.2*

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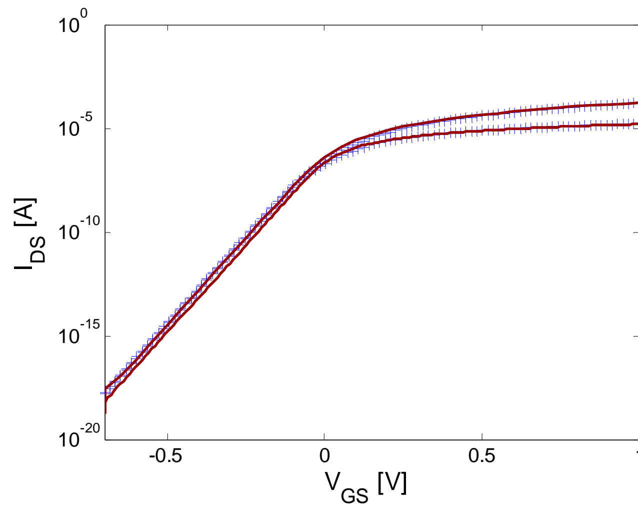

Fig.2A.5 *Transfer characteristics, for V_{DS}=0.05V (b) and for V_{DS}=1V (a) in logarithmic scale. Solid line: ATLAS simulation; Symbol line: our model using (2A.9). Same simulation conditions as Fig.2A.2*

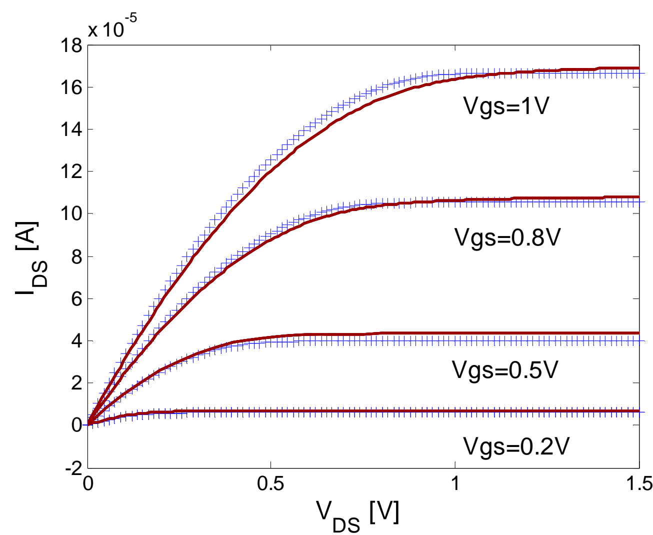

Fig.2A.6 *Output characteristics. Solid line: ATLAS simulation; Symbol line: our model using (2A.9). Same simulation conditions as Fig.2A.2*

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2A.2.2 Charge and Capacitance Model

The total inversion charge is calculated as [87]:

$$Q_{Tot} = -2W\int_0^L Q dx = -(2W)^2 \frac{\mu}{I_{DS}} \int_0^{V_{DS}} Q^2 dV \qquad (2A.25)$$

Using (2A.8) we get:

$$Q_{Tot} = (2W)^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left(\frac{Q^2}{C_{ox}} + \frac{kT}{q} Q + \frac{kT}{q} \frac{Q^2}{Q + Q_{Dep}} \right) dQ \qquad (2A.26)$$

From the total gate charge Q_G=-Q_{Tot}-Q_{ox}+WLQ_{Dep}, where Q_{ox} is the total oxide fixed charge at both front and back interfaces.

The intrinsic capacitances, C_{gd} and C_{gs}, are obtained as [87]:

$$C_{gi} = -\frac{dQ_G}{dVi} \qquad (2A.27)$$

where *i=d,s.*

We obtain these capacitances, by differentiating Q_{Tot} according to (2A.8) and using (2A.17) for the charge densities at source and drain.

Following the Ward's channel charge partitioning scheme [87] we obtain analytical expressions for the total drain (Q_D) and source (Q_S) charges:

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$$Q_D = -2W\int_0^L \frac{x}{L} Q dx = \frac{(2W)^3 \mu^2}{L I^2_{DS}} \int_{Q_s}^{Q_d} Q^2 \left(\begin{array}{l} \left(\frac{Q^2 - Q_s^2}{2C_{ox}} \right) + \\ + \frac{kT}{q}\left(2(Q - Q_s) - Q_{Dep} \log\left[\frac{Q + Q_{Dep}}{Q_s + Q_{Dep}} \right] \right) \end{array} \right) \cdot \left(\frac{1}{C_{ox}} + \frac{kT}{q}\left(\frac{1}{Q} + \frac{1}{Q + Q_{Dep}} \right) \right) dQ \quad (2A.28)$$

$$Q_S = Q_{Tot} - Q_D \quad (2A.29)$$

(The solutions for Eq.(2A.26) and Eq.(2A.28) are given in Appendix)

The non-reciprocal capacitances C_{dg} and C_{sg} are obtained as [87]:

$$C_{ig} = -\frac{dQ_i}{dV_G} \quad (2A.30)$$

The great advantage of this capacitance model is that it is charged-based and all the expressions are analytical, explicit and continuous through all operating regimes.

2A.2.3 Simulation Results

In order to compare this model with ATLAS 2D numerical simulations, we have considered a DG MOSFET with the following parameters: doping level $N_A = 6 \cdot 10^{17}$ cm^{-3}; silicon thickness t_{Si}=31nm; oxide thickness t_{ox}=2nm; channel length

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L=1μm and width W=1μm. We have compared the modelled and simulated I_{DS}-V_{GS} characteristics for two values of V_{DS} (0.05V and 1V). These characteristics are plotted in the linear and logarithmic scales (Fig**.** 2A.4, 2A.5). Agreement is good for V_{GS} up to 1V. Actually these devices are not operated at V_{GS} values much higher than 1 V, and therefore the model is valid for the regimes of practical interest. In the subthreshold regime there is a perfect match between this model and the simulations (Fig.2A.5). The I_{DS}-V_{DS} characteristics, for different values of V_{GS}, show a good agreement with the numerical simulations (Fig.2A.6). We have also compared this model with measurements on a FinFET with the following technological parameters: doping level $N_A=10^{18}$ cm^{-3}; fin width=35nm, which corresponds to the thickness of the silicon film in this model t_{Si}; effective oxide thickness t_{ox}=2nm; channel length L=1μm. The experimental FinFET was fabricated at IMEC [13] and has 66 fins (N_{fins}=66) with a height of hfin=75nm. We have modelled the FinFET as a DG MOSFET: this is valid when the width of the fin is very small compared to the height of the fin. In this case the width of the channel (to be used in (2A.9)) can be approximated by: $W=2h_{fin}N_{fins}$. We can see that the agreement between model and FinFET measurements is good in all operating regimes, up to high values of V_{GS}, where our approximation (2A.5) is less valid and, especially for low values

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of V_{DS}, the effect of the series resistance can be significant. (Fig.2A.7-2A.9). On the other hand, at negative values of V_{GS} we observe that the gate-induced drain leakage current, due to band-to-band tunnelling, dominates and masks the subthreshold diffusion current; this current contribution has not been included in the model so far.

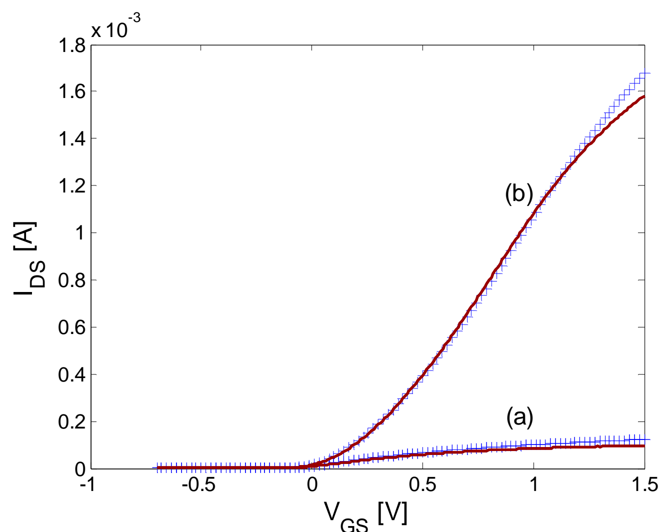

Fig.2A.7 *Transfer characteristics, for V_{DS}=0.05V (a) and for V_{DS}=1V (b) in linear scale. Solid line: FinFET measurements; Symbol line: our model using (2A.9) with FinFET extracted parameter values*

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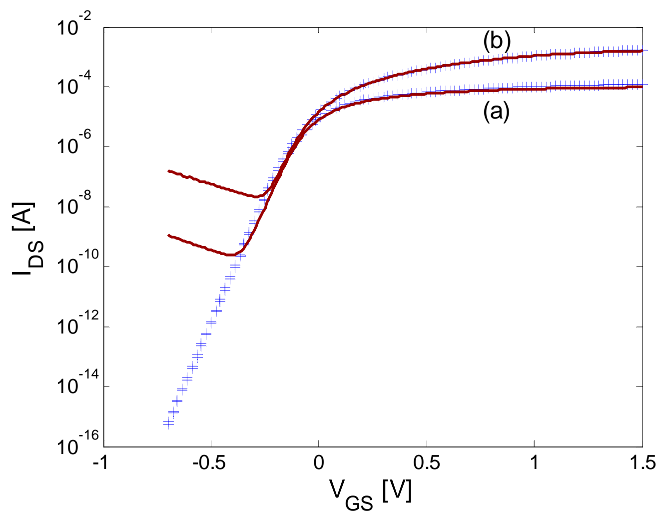

Fig.2A.8 *Transfer characteristics, for V_{DS}=0.05V (a) and for V_{DS}=1V (b), in logarithmic scale. Solid line: FinFET measurements; Symbol line: our model using (2A.9) with FinFET extracted parameter values*

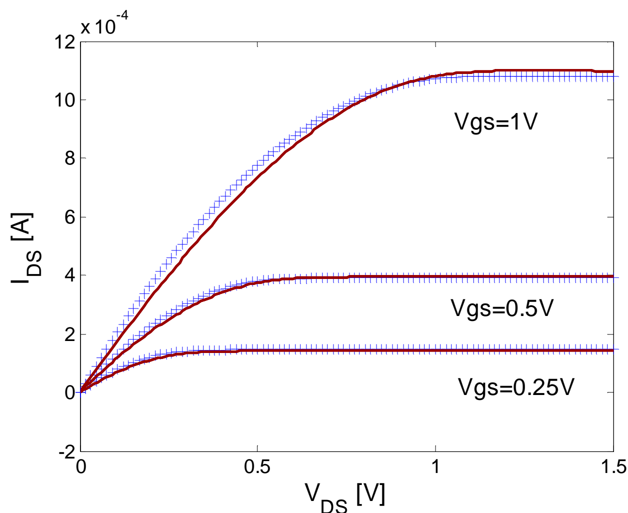

Fig.2A.9 *Output characteristics. Solid line: FinFET measurements; Symbol line: our model using (2A.9) with FinFET extracted parameter values*

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In order to have a complete model for the drain and source capacitances, we have to account for the parasitic overlap and fringing capacitances, which we add to the previously modelled intrinsic capacitances.

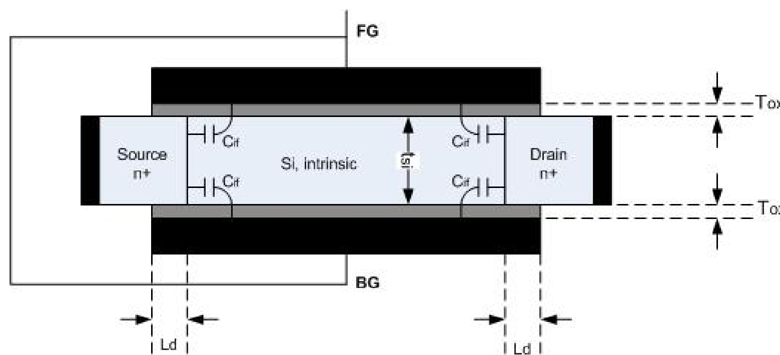

Fig.2A.10 *Intrinsic fringing capacitances in a DG MOSFET*

A model that introduces the bias dependence of the overlap and fringing capacitances was used [88] and adapted to DG MOSFETs. The inner fringing capacitance between gate and source is defined as:

$$C_f = C_{f,\max} \exp\left[-\left(\frac{V_{GS} - V_{FB} - \frac{\phi_F}{2}}{\frac{3\phi_F}{2}}\right)^2\right] \qquad (2A.31)$$

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where $C_{f,max}$ is an adjustable parameter [88]. By increasing V_{GS} the fringing capacitance tends to zero because of the formation of the inversion channel.

The gate-source overlap capacitance has the following expression [88]:

$$C_{ov} = WC_{ox}\frac{L_d}{1-\lambda V_{GS}^*} \tag{2A.32}$$

where L_d is the gate overlap region. Following [88], a smoothing function is used to make the bias dependent overlap capacitance converging to its maximum value:

$$V_{GS}^* = V_{GS} - \frac{1}{2}V_{GS} - 0.5\sqrt{V_{GS}{}^2 + 0.05} \tag{2A.33}$$

In (2A.32) λ is an adjustable parameter depending on the channel doping [88]. In our case λ=0.4 and the 0.05 value from (2A.33) represents a transition term from deep subthreshold to strong inversion. From (2A.32) and (2A.33), well above threshold we get $V_{GS}^* \approx 0$ and $C_{ov} \approx W C_{ox} L_d$, as it should. As V_{GS} decreases C_{ov} decreases and from (2A.32),(2A.33) $V_{GS}^* \approx V_{GS}$ and C_{ov} tends to 0 in deep subthreshold , as it should (since, as explained in [88], the overlap region becomes fully depleted and the lateral effective length vanishes).

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Therefore, the complete model for the parasitic gate-source capacitance which will be added to our intrinsic capacitance model is given by:

$$C_{gs,par} = 2W\left(C_{ox}\frac{L_d}{1-\lambda V_{GS}^{*}} + C_f\right) \tag{2A.34}$$

Following the same reasoning, the parasitic gate-drain capacitance, $C_{gd,par}$ can be calculated by replacing V_{GS} with V_{GD} in equations (2A.31) to (2A.34). These expressions of $C_{gs,par}$ and $C_{gd,par}$ should be added to the expressions of the intrinsic capacitances C_{sg}, C_{gs} and C_{dg}, C_{gd}. Using ATLAS we simulated the device capacitances for two values of V_{DS}: 0.05V and 1V. We have compared these simulations with this model. The capacitances have been normalized to the oxide capacitance (Figs 2A.11 and 2A.12). A good agreement is observed in all operating regimes.

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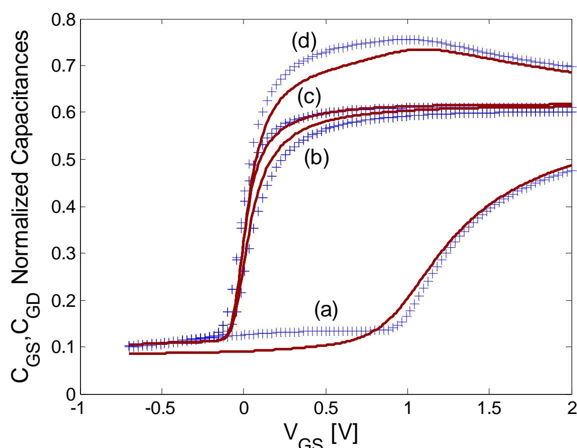

Fig.2A.11 *Normalized gate to drain capacitance (a, b) and gate to source capacitance (c, d) with respect to the gate voltage, for V_{DS}=1V (a,d) and V_{DS}=0.05V (b,c). Solid line: ATLAS simulations; Symbol line: our model using (2A.27) Same simulation conditions as Fig.2A.2*

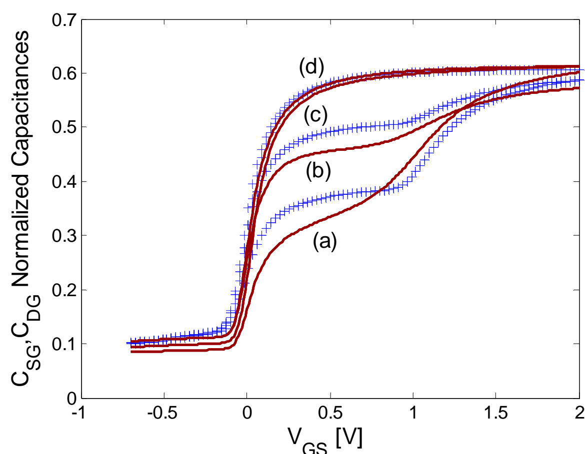

Fig.2A.12 *Normalized drain to gate capacitance (a, c) and source to gate capacitance (b, d) with respect to the gate voltage, for V_{DS}=1V(a,b) and V_{DS}=0.05V (c, d). Solid line: ATLAS simulations; Symbol line: our model using (2A.29) Same simulation conditions as Fig.2A.2*

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2A.3 Continuous modeling of symmetrical DG MOSFETs from low to high doping values

2A.3.1 Introduction

The main problem for modeling doped DG devices is that the potential at the surface and the potential at the middle of the silicon layer are related. The electric field at the interface is written as a function of these potentials, expressed by transcendental equations that have no analytical solution. The first approach to obtain an analytical expression was done considering the difference of potentials to be equal to its value in the below threshold condition and assuming a high doping [39,40] as in section 2A.2. These approximations lead to compact analytical expressions but the resulting model is only valid for highly doped devices and up to moderate inversion. Most DG MOSFET models reported up to now have been developed under the condition of undoped silicon layer, when an analytical solution can be easily achieved [33,34,38,83,84,90]. However, we will show that even for concentrations as low as 10^{14} cm^{-3} the effects of having a doped Si layer cannot be neglected in the solution of the surface potential equations. A new attempt to solve this situation was done recently using the so called regional approach [91], but with the same approximation of Francis in [40]. However, figures in [91] clearly show the disagreement obtained between calculated and

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simulated values of potential differences above threshold voltage.

In this section we present an analytical continuous compact model for long channel symmetric DG MOSFETs, which considers a doped silicon layer with any value of doping concentration, gate dielectric and silicon layer thickness and applied voltages in the typically used ranges. The charge density at source and drain is calculated using the analytical expressions previously derived to model the potential at the surface and the difference of the potential at the surface and at the center of the silicon doped layer. The current is then calculated using the charge control model from section 2A.2, derived for DG MOSFETs. Although, more complicated than the model in section 2A.2, this model is valid from low to high doping. In order to validate the expressions to model the potential and difference of potentials, an accurate numerical calculation was done implementing the procedure in [92] for symmetric double-gate structures. In order to validate the model, a typical DG structure was simulated using 2D ATLAS to obtain the transfer characteristics in the linear and saturation regions and the output characteristics for the different silicon layer concentrations, varying from 10^{14} cm^{-3} to 10^{18} cm^{-3}, and two polysilicon concentrations, of 10^{20} cm^{-3} and 10^{21} cm^{-3}. Gate-source and

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gate-drain capacitance were also simulated for comparison with the results from this model.

2A.3.2 Formulation of the Poisson's equation

The double-gate transistor structure under analysis is shown in Fig. 2A.13, where N_A is the uniform acceptor concentration in the silicon layer with thickness equal to t_{si}; t_{ox} is the gate dielectric thickness; t_{poly} is the polysilicon thickness with a donor concentration N_{poly} and L is the channel length. The transistor is symmetrical, with both gates connected together at V_{GS}.

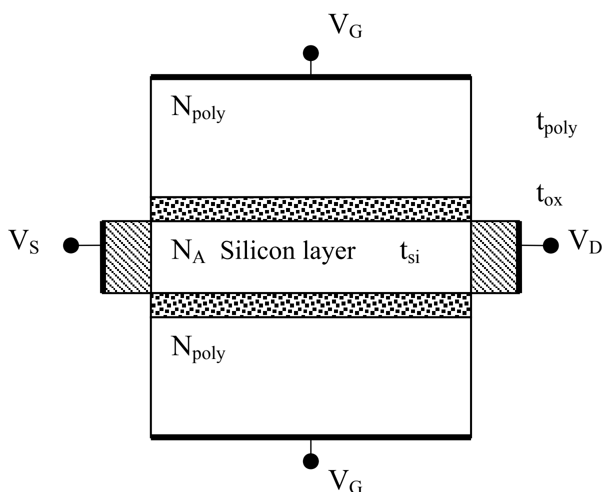

Fig.2A.13 *Diagram of the double-gate MOSFET structure analyzed.*

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The charge density as function of the potential ϕ is equal:

$$\rho = q\left(p - n_e - N_A\right) = q\left(n_i e^{\frac{\phi_{Fp}-\phi}{\beta}} - n_i e^{\frac{\phi-\phi_{Fn}}{\beta}} - n_i e^{\frac{\phi_{Fp}}{\beta}}\right) \tag{2A.35}$$

where β=kT/q is the thermal potential, k is the Boltzmann constant; q is the electron charge and T is the temperature in K; n_i is the intrinsic carrier concentration; ϕ_{Fp} is the quasiFermi level for holes in the P-type silicon layer and ϕ_{Fn} is the quasiFermi level for electrons.

The potential along the channel is $V=\phi_{Fn}-\phi_{Fp}$, and from now on, ϕ_{Fp} will be renamed as ϕ_F.

Equation (2A.35) can be rewritten as:

$$\rho = -qN_A\left(1 + e^{\frac{\phi-2\phi_F-V}{\beta}} - e^{-\frac{\phi}{\beta}}\right). \tag{2A.36}$$

The electric field at the surface of the silicon layer is calculated using Poisson equation (Section 2A.2.2, Eq.(2A.3)).

As can be seen the electric field depends not only on ϕs but also on the difference between potentials at the surface and at the center of the Si layer, ϕs-ϕo. If the Si layer is considered to be undoped, the electric field obtained appears to depend only on

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ϕs [39]. As was already mentioned, under this later approximation, analytical expressions have been obtained to calculate the current. However, as will be shown below, this approximation is very rough and even for layers with doping as low as 10^{14} cm^{-3}, the doping effect must be taken into account.

Equation (2A.3) can be rewritten as:

$$Es = \frac{\sqrt{2Q_{Dep}C_{Si}\beta}}{\varepsilon_{si}}\sqrt{\alpha}\sqrt{1+\frac{1-e^{-\alpha}}{\alpha}\cdot e^{\frac{\phi s-2\phi_F-V}{\beta}}}\,. \qquad (2A.37)$$

where $\alpha = (\phi s - \phi o)/\beta$ is the normalized difference of potentials, ε_{si} is the silicon dielectric constant and $C_{si} = \varepsilon_{si}/t_{si}$ is the silicon layer capacitance per unit area.

Substituting (2A.37) in the expression for the gate voltage V_{GS}, the surface potential ϕs is implicitly defined by the equation

$$V_{GS} = V_{FB} + \phi s + \frac{\sqrt{2Q_{Dep}C_{si}\beta}}{C_{ox}}\sqrt{\alpha}\sqrt{1+\frac{1-e^{-\alpha}}{\alpha}\cdot e^{\frac{\phi s-2\phi_F-V}{\beta}}}\,, \qquad (2A.38)$$

where $C_{ox} = \varepsilon_{ox}/t_{ox}$ the gate capacitance per unit area and ε_{ox} is the gate dielectric constant.

These potentials were calculated for a basic device structure with t_{ox}= 2 nm; t_{si}= 34 nm; t_{poly}= 100 nm; N_{poly}= 10^{20} cm^{-3}; N_{ss}=5x10^{10} cm^{-2} and N_A varying from 10^{14} to 3x10^{18} cm^{-3}. For

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this value of N_{poly}, polysilicon depletion has to be considered, obtaining an effective dielectric thickness of 2.24 nm. In some cases t_{ox} and t_{si} were also varied. A long channel device with L= 5 μm was considered to avoid short channel effects without affecting generalization of the calculations.

2A.3.3 Calculation of the potentials

2A.3.3.1 Below threshold regime

In the below threshold regime, the difference between the surface potential and the potential at the center of the layer is calculated using the depletion approximation which is valid in this regime. The expression obtained is:

$$\phi d_{BT} = \phi s_{BT} - \phi o_{BT} = \frac{q N_A t_{si}^2}{8 \varepsilon_{si}} = \frac{Q_{Dep}}{8 C_{si}}, \qquad (2A.39)$$

where ϕs_{BT} and ϕo_{BT} are the values of the surface potential and potential at the center of the Si layer corresponding to the below threshold condition. As can be seen, ϕd_{BT} depends only on the doping concentration N_A and on the silicon layer thickness t_{si}.

ϕs_{BT} can be calculated solving the transcendental equation (2A.38). For the below threshold regime, the term

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$(1-e^{-\alpha_{BT}})/\alpha_{BT} < 1$ and (2A.38) can be simplified expanding the square root. After some rearrangements it can be rewritten as:

$$V_{GS} - V_{FB} = \phi s_{BT} + \frac{Q_{Dep}}{2C_{ox}}\left(1 + \frac{1}{2}e^{\frac{\phi s_{BT} - 2\phi_F}{\beta}}\right). \qquad \text{(2A.40)}$$

Using the principal branch of the Lambert function LW (defined as: $W(x)\cdot e^{W(x)} = x$, which can be computed analytically through some approximations as in [89]), ϕs_{BT} can be calculated from (2A.40) as:

$$\phi s_{BT} = V_{GS} - V_{FB} - \frac{Q_{Dep}}{2C_{ox}} - \beta \cdot LW\left[\frac{Q_{Dep}}{4C_{ox}\beta} e^{\frac{V_{GS} - V_{FB} - 2\phi_F - \frac{Q_{Dep}}{2C_{ox}}}{\beta}}\right] \qquad \text{(2A.41)}$$

ϕo_{BT} is calculated substituting (2A.41) in (2A.39) as:

$$\phi o_{BT} = \phi s_{BT} - \phi d_{BT} \ . \qquad \text{(2A.42)}$$

2A.3.3.2 Threshold condition

When the gate voltage is equal to the threshold voltage, $\phi d_T = \phi s_T - \phi o_T$ is higher than the value calculated from (2A.39). From numerical calculations and simulations it was found that ϕd varies with V_{GS} and at $V_{GS}=V_t$ it can be expressed as:

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$$\phi d_T = \phi d_{BT} + \Delta\phi d_T = \frac{Q_{Dep}}{8C_{si}} + \frac{5}{8}\beta . \tag{2A.43}$$

If the threshold voltage is determined at the maximum of the derivative of the transconductance using the double-derivative method, the surface potential at threshold, ϕs_T, can be numerically calculated applying the condition $(d^3\phi s / dV_G{}^3) = 0$ to Eq (2A.38) [39,40]. However, according to calculations of these authors, ϕs_T remains constant for N_A lower than $3x10^{16}$ cm^{-3}, which is not correct because ϕs_T and ϕo_T as function of N_A calculated using Mallikarjun's method [92], vary with N_A in all the range from 10^{14} to $3x10^{18}$ cm^{-3}. Simulations also confirmed this behavior. The erroneous values of ϕs_T obtained in [39,40] for low N_A may be related to the approximation they made considering $\phi d_T = \phi d_{BT}$, which is only valid for N_A greater than $3x10^{17}$ cm^{-3}.

In [39] authors also found an approximate analytical expression which they adjusted to provide good agreement with the numerically calculated values, for concentrations greater than $3x10^{17}$ cm^{-3}.

$$\phi s_T = 2\phi_F + \beta \ln\left[\frac{C_{ox}}{4C_{si}}\left(1 + \frac{\beta C_{ox}}{Q_{Dep}}\right)\right], \tag{2A.44}$$

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while $\phi o_T = \phi s_T - \phi d_T$. (2A.45)

First, the potential at the center of the layer ϕo_T, as function of the layer concentration N_A, has a maximum for a concentration equal to:

$$N_{A\max} = \frac{\varepsilon_{si}\beta}{qt_{si}^2}\left[11.68 + \frac{C_{ox}}{2C_{si}} + \frac{1}{16}\left(\frac{C_{ox}}{2C_{si}}\right)^2\right]. \quad (2A.46)$$

As can be seen, for typical double-gate dimensions, below this concentration the center of the layer can be considered to be in strong inversion ($\phi o_T > 2\phi_F$) and above $N_{A\max}$ in weak inversion ($\phi_F < \phi o_T < 2\phi_F$). Another important feature is that the value of the surface potential at threshold can be greater or lower than $2\phi_F$, while in [39,40] it was considered that ϕs_T is always lower than $2\phi_F$. This apparent contradiction can be explained analyzing results in Fig.2A.14, where these potentials are shown for Si layer thickness of 10, 30 and 50 nm. As can be seen the surface potential is lower than $2\phi_F$ only for a specific combination of gate dielectric and Si layer thicknesses conditions and high doping concentration.

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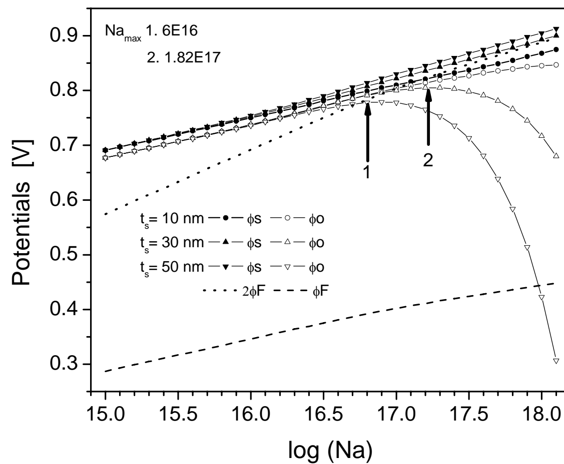

Fig.2A.14 *Modeled and numerically calculated potentials at the surface and at the center of the Si layer as function of N_A in threshold condition for silicon layer thickness of 10, 30 and 50 nm. t_{ox}= 2.24 nm. Curves $\phi_F(N_A)$ and $2\phi_F(N_A)$ are also shown. Arrows indicate the doping concentration at which the maximum value of the potential at the center of the layer occurs for t_{si}=30 nm and 50 nm respectively.*

The cases analyzed in [40], in fact, correspond to these conditions, so these results corroborate the statement of [40] for their specific conditions, but not as a general case. The shift of $N_{A\ max}$ with t_{si} varying from 10 to 50 nm is also indicated in Fig. 2A.14. Arrows 1 and 2 indicate the maximum observed for t_{si}=30 nm and 50 nm respectively. It is seen that transition from weak inversion to depletion at the center of the silicon layer can be achieved for thicker Si layer and higher doping

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concentration. The threshold voltage is calculated substituting (2A.44) in (2A.38):

$$V_t = V_{FB} + 2\phi_F + \beta \ln\left[\frac{C_{ox}}{4C_{si}}\left(1+\frac{\beta C_{ox}}{Q_{Dep}}\right)\right] + \\ + \frac{\sqrt{2Q_{Dep} C_{si} \beta}}{C_{ox}}\sqrt{\alpha_T}\sqrt{1+\frac{1-e^{-\alpha_T}}{\alpha_T}\frac{C_{ox}}{4C_{si}}\left(1+\frac{\beta C_{ox}}{Q_{Dep}}\right)}. \qquad (2A.47)$$

where $\alpha_T = \left(\phi s_T - \phi o_T\right)/\beta$.

Fig. 2A.15 shows V_t as function of N_A for t_{ox}= 2 ± 1 nm. It is observed that around N_A=2.6x10^{17} cm^{-3} the variation of V_t with t_{ox} is minimized: for lower doping concentrations V_t increases as t_{ox} decreases, while for higher doping V_t decreases with t_{ox}. This behavior can be useful for circuit designers. A similar behavior was reported in [93] from simulated data under the condition of workfunction difference equal to zero. However, the values of V_t and the doping concentration where the change of behavior occurred were different.

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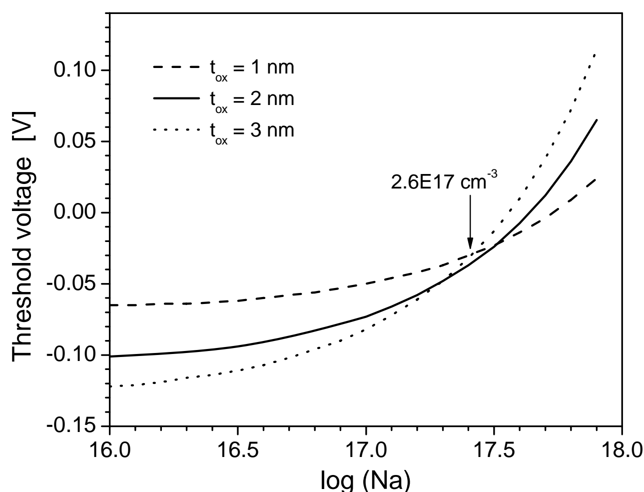

Fig.2A.15 *Modeled and extracted from 2D simulation threshold voltage as function of N_A for three gate oxide thickness: t_{ox}= 1, 2 and 3 nm and t_{si}= 34 nm.*

2A.3.3.3 Modeling of potentials and difference of potentials in all regions

The next step for modeling potentials was the definition of an empirical expression for the difference of potentials, ϕd, between the potential at the surface and at the center of the silicon layer as a function of applied gate and drain voltages.

Using the detailed numerical calculation it was found that this magnitude can be expressed by empirical analytical expressions in the following three conditions:

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1) below threshold

$$\phi d_1 = \phi d_{BT} + \frac{19}{16}\beta\left[\frac{e^{\frac{V_{GS}-V_t-V}{1.1\beta}}}{1+e^{\frac{V_{GS}-V_t-V}{1.1\beta}}}\right], \tag{2A.48}$$

2) above threshold for $N_A < N_{Amax}$

$$\begin{aligned}\phi d_{2a} &= \left(\frac{\phi d_{BT}}{3} + \phi d_M - 0.042\,V\right) - \\ &- \left(\frac{\phi d_{BT}}{3} + \phi d_M - 0.042\,V - \phi d_T\right)\left(\frac{1-\frac{V_{GS}-V_t-V}{V_{GM}-V_t-V}}{1+1.35\left(V_{GS}-V_t-V\right)}\right)\end{aligned} \tag{2A.49}$$

3) above threshold for $N_A > N_{A\,max}$

$$\begin{aligned}\phi d_{2b} &= \left(\frac{\phi d_{BT}}{2} + \phi d_M - 0.042\,V\right) - \\ &- \left(\frac{\phi d_{BT}}{2} + \phi d_M - 0.042\,V - \phi d_T\right)\left(\frac{1-\frac{V_{GS}-V_t-V}{V_{GM}-V_t-V}}{1+0.5\left(V_{GS}-V_t-V\right)}\right)\end{aligned} \tag{2A.50}$$

Combining (2A.49) and (2A.50) using the tanh function the following expression was obtained:

$$\begin{aligned}\phi d_2 &= \phi d_{2a}\frac{1-\tanh\left[10\left(\log(N_A)-\log\left(N_{A\max}\right)-0.5\right)\right]}{2} + \\ &+ \phi d_{2b}\frac{1+\tanh\left[10\left(\log(N_A)-\log\left(N_{A\max}\right)-0.5\right)\right]}{2}\end{aligned} \tag{2A.51}$$

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Combining (2A.48) with (2A.51) the complete expression to describe ϕd for the three above mentioned conditions was obtained:

$$\phi d = \phi d_1 \frac{1-\tanh\left[50(V_{GS}-V_t-V)\right]}{2} + \phi d_2 \frac{1+\tanh\left[50(V_{GS}-V_t-V)\right]}{2}. \quad (2A.52)$$

The value of ϕd_M is defined at maximum gate voltage considered for these structures V_{GM}= 2 V and V=0 V, as a function of the gate dielectric and silicon layer thicknesses, both in nm, and is expressed as:

$$\phi d_M = 0.197 - 0.047 t_{ox} + 0.0045 t_{ox}^2 + 0.00418 t_{si} - 3\cdot 10^{-5} t_{si}^2. \quad (2A.53)$$

Finally the surface potential as function of N_A, t_{si}, t_{ox}, V_{GS} and V can be calculated numerically from (2A.38) after substituting (2A.52) in α. In the above threshold regime Eq (2A.38) can be simplified neglecting the 1 in the square root and using the Lambert function, after which it can be rewritten as:

$$\phi s_{AT} = V_{GS} - V_{FB} - 2\beta \cdot LW\left[\frac{\sqrt{2Q_{Dep}C_{si}\beta}}{2C_{ox}\beta}\sqrt{1-e^{-\alpha}}\, e^{\frac{V_{GS}-V_{FB}-2\phi_F-V}{2\beta}}\right]. \quad (2A.54)$$

Combining the solutions for the surface potential in the below (2A.41) and above threshold (2A.54) regimes, the complete expression for the surface potential is obtained:

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$$\phi s = \phi s_{BT} \frac{1-\tanh\left[10(V_{GS}-V_t-V\right]}{2} + \phi s_{AT} \frac{1+\tanh\left[10(V_{GS}-V_t-V\right]}{2} \quad (2A.55)$$

The potential at the center of the Si layer is calculated as:

$$\phi o = \phi s - \phi d \ . \quad (2A.56)$$

2A.3.4. Derivation of the drain current and charge models

To calculate the current, we need to know the charge carrier concentration along the channel Q, which can be determined through the relation with the surface electric field at each interface Eq. (2A.2).

We consider that the total semiconductor charge at each surface of the DG transistor is equal to Q+Q_{Dep}/2, where Q_{Dep} is shared by the two surfaces.

Expressions derived up to now are required to calculate analytically the surface carrier concentration per unit area at each surface Q, which can be calculated substituting (2A.37) in Eq. (2A.2):

$$Q = \sqrt{2Q_{Dep}C_{si}\phi t}\sqrt{\alpha}\sqrt{1+\frac{1-e^{-\alpha}}{\alpha}\cdot e^{\frac{\phi s-2\phi_F-V}{\beta}}} - \frac{Q_{Dep}}{2} \quad , \quad (2A.57)$$

where α is determined using (2A.52) and ϕs using (2A.55).

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Using Eq. (2A.2), the gate voltage V_{GS} can be written as:

$$V_{GS} = V_{FB} + \phi s + \frac{1}{C_{ox}} \cdot \left(Q + \frac{Q_{Dep}}{2} \right) \quad . \tag{2A.58}$$

Substituting ϕs from (2A.58) in (2A.57) and solving for V_{GS}, considering also that

$$\alpha_{BT} = \frac{\phi d_{BT}}{\beta} = \frac{Q_{Dep}}{8 C_{si} \beta} \ , \tag{2A.59}$$

the following general relation is obtained:

$$\begin{aligned} & V_{GS} - V_{FB} - 2\phi_F - V - \frac{Q_{Dep}}{2C_{ox}} + \beta \ln\left(\frac{1 - e^{-\alpha}}{\alpha} \right) = \\ & = \frac{Q}{C_{ox}} + \beta \ln\left[\frac{\alpha_{BT}}{\alpha} \left(\frac{4Q}{Q_{Dep}} \cdot \left(1 + \frac{Q}{Q_{Dep}} \right) + 1 \right) - 1 \right] \end{aligned} \tag{2A.60}$$

Equation (2A.60) introduces a Unified Charge Control Model extended to symmetric DG MOSFETs.

For the typical voltages range in this type of transistors, (up to 2 V), and for Si layer concentration in the range from 10^{14}cm^{-3} to 3x10^{18} cm^{-3}, $\frac{\alpha_{BT}}{\alpha} \left(\frac{4Q}{Q_{Dep}} \cdot \left(1 + \frac{Q}{Q_{Dep}} \right) + 1 \right) >> 1$ and (2A.60) can be approximated to:

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$$V_{GS}-V_{FB}-2\phi_F-V-\frac{Q_{Dep}}{2C_{ox}}+\beta\ln\left(\frac{1-e^{-\alpha}}{\alpha}\right)= \\ =\frac{Q}{C_{ox}}+\beta\ln\left[\frac{\alpha_{BT}}{\alpha}\cdot\frac{4Q}{Q_{Dep}}\cdot\left(1+\frac{Q}{Q_{Dep}}\right)\right] \tag{2A.61}$$

The derivative of (2A.61) with respect to V gives:

$$-1+\frac{d}{dV}\left[\beta\ln\left(\frac{1-e^{-\alpha}}{\alpha}\right)\right]= \\ =\left[\frac{1}{C_{ox}}+\beta\left(\frac{1}{Q}+\frac{1}{Q+Q_{Dep}}\right)\right]\frac{dQ}{dV}+\beta\frac{d}{dV}\left[\ln\left(4\frac{\alpha_{BT}}{\alpha}\right)\right]. \tag{2A.62}$$

Again, on both sides of the equation, the terms involved with logarithm can be neglected considering their relative weight, resulting in the following expression to represent the variation of V through Q:

$$-1=\left[\frac{1}{C_{ox}}+\frac{kT}{q}\left(\frac{1}{Q}+\frac{1}{Q+Q_{Dep}}\right)\right]\frac{dQ}{dV}. \tag{2A.63}$$

Due to the fact that the derivative in (2A.63) equals the one in the previous model in (2A.8), the transistor current and gate-drain and gate-source capacitances are calculated as explained in section 2A.2.1 and section 2A.2.2, taking into consideration the new developed Q in Eq. (2A.57), for different N_A.

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2A.3.5 Simulation Results

The structure shown in Fig. 2A.13 was simulated in ATLAS using the following typical parameters for nanometric devices: t_{ox}= 2 nm, t_{si}= 34 nm, t_{poly}= 100 nm, W= 1 µm, L= 5µm, constant mobility equal 400 cm^2/Vs and without impact ionization. The silicon layer doping concentration was varied from 10^{14} cm^{-3} to $3x10^{18}$ cm^{-3} and two values of polysilicon doping concentration of 10^{20} cm^{-3} and 10^{21} cm^{-3} were considered. The selection of those parameters was done to avoid the short channel effects and mobility dependence, which will be considered for future work to complete this core model. The transfer characteristics were obtained for gate voltage varying from -0.5 V to 2 V and the drain voltage was fixed at 0.05V and 1 V. The output characteristics were obtained for V_{GS} equal to 0.5V, 1V and 2 V. The C-V characteristics were calculated using the small signal simulation in ATLAS at 1 MHz. The transfer characteristic in the linear region at V_{DS}= 0.05 V is shown in Fig. 2A.16. For doping concentrations from N_A= 10^{14} to 10^{16} cm^{-3} the curves are practically the same so in the figure we only show the curves for 10^{16} and 10^{18} cm^{-3}. The polysilicon doping concentration was 10^{20} cm^{-3}.

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Since polydepletion effect increases the effective gate oxide thickness, in the current calculation an effective value of the dielectric layer equal to 2.24 nm was used instead of 2 nm. As can be seen the agreement between the current simulated and the current modeled, in all operation regimes, is very good for both doping concentrations.

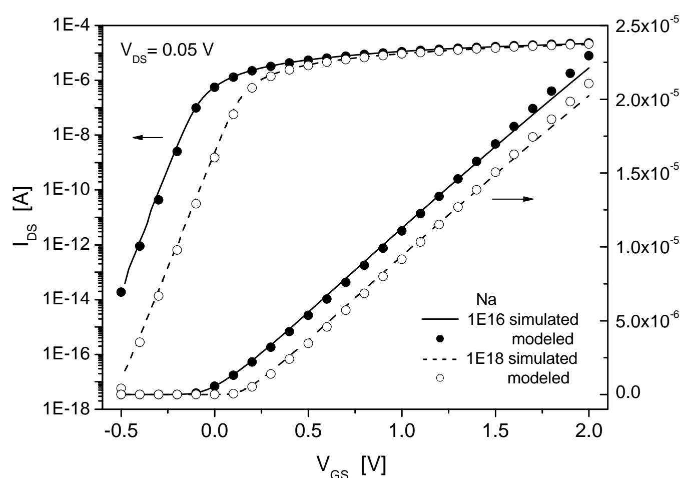

Fig.2A.16 *Comparison between simulated and modeled linear transfer characteristics for V_{DS}= 0.05 V and two Si layer doping concentrations: 10^{16} cm^{-3} and 10^{18} cm^{-3}; polysilicon doping is $N_{poly}=10^{20}$ cm^{-3} and t_{ox} = 2.24 nm.*

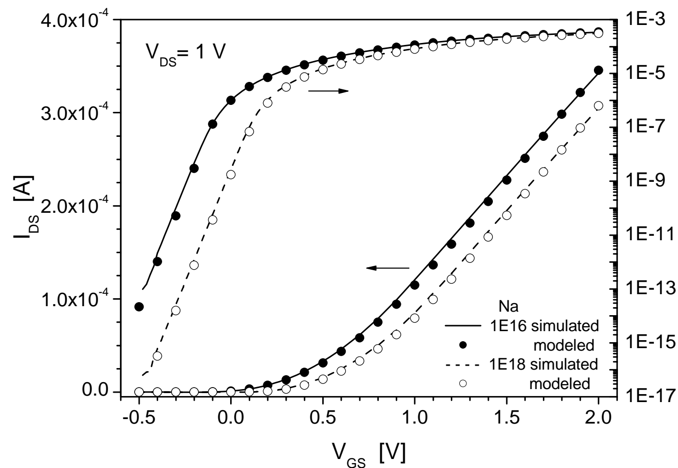

Fig.2A.17 *Comparison between simulated and modeled transfer characteristics in saturation for V_{DS}= 1 V and two Si layer doping concentrations: 10^{16} cm^{-3} and 10^{18} cm^{-3}; polysilicon doping is $N_{poly}=10^{20}$ cm^{-3} and t_{ox}= 2.24 nm.*

The same good agreement was obtained for the transfer characteristic in saturation at V_{DS}= 1 V, Fig. 2A.17.

Three output I-V characteristics are shown, one in Fig. 2A.18 for N_A= 10^{14} cm^{-3} and two in Fig. 2A.19 for N_A= 10^{16} and 10^{18} cm^{-3} where again, the agreement is excellent in all regions. If the polysilicon impurity concentration is 10^{21} cm^{-3}, the polydepletion can be neglected and the output characteristics shown in Fig. 2A.20 have an excellent agreement using t_{ox}= 2 nm.

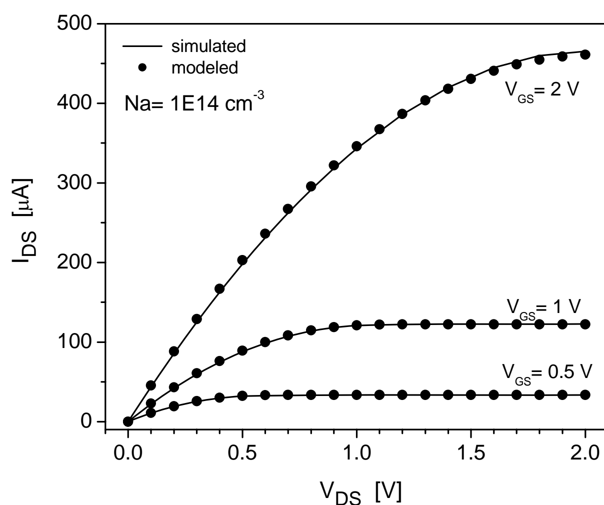

Fig.2A.18 *Simulated and modeled output characteristics for V_{GS}= 0.5, 1 and 2 V for a Si layer doping concentration of 10^{14}; polysilicon doping is N_{poly}=10^{20} cm^{-3} and t_{ox}= 2.24 nm.*

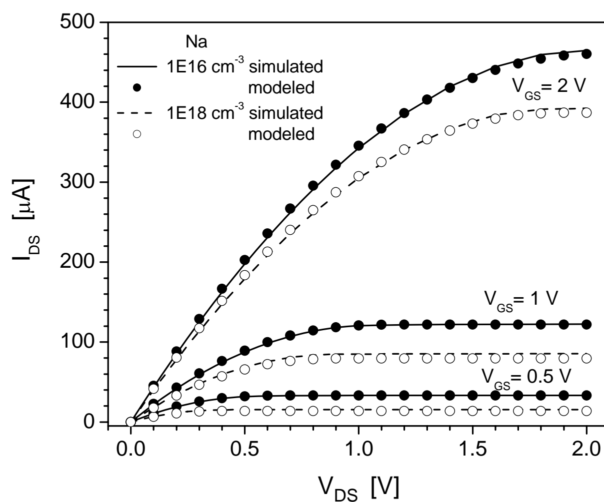

Fig.2A.19 *Simulated and modeled output characteristics for V_{GS}= 0.5, 1 and 2 V and two Si layer doping concentrations: 10^{16} cm^{-3} and 10^{18} cm^{-3}; polysilicon doping is N_{poly}=10^{20} cm^{-3} and t_{ox}= 2.24 nm.*

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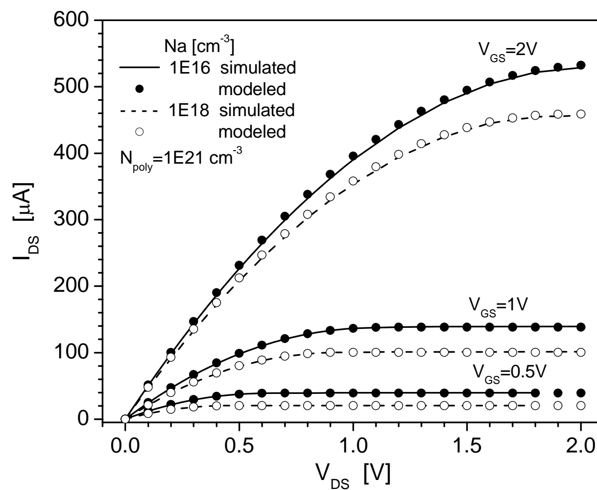

Fig.2A.20 *Simulated and modeled output characteristics for V_{GS}= 0.5, 1 and 2 V and two silicon layer doping concentrations: 10^{16} cm^{-3} and 10^{18} cm^{-3}; polysilicon doping is $N_{poly}=10^{21}$ cm^{-3}. No polysilicon depletion effect is observed.*

Simulated and calculated capacitance-voltage characteristics (C_{gs} and C_{gd}) are shown in Fig. 2A.21. As can be seen, this model provides a very good agreement at drain bias of 0.05V, 0.5V and 1V. It is worth to remark that the explicit, continuous an analytical character of the model for the capacitance provides significant advantages for circuit design.

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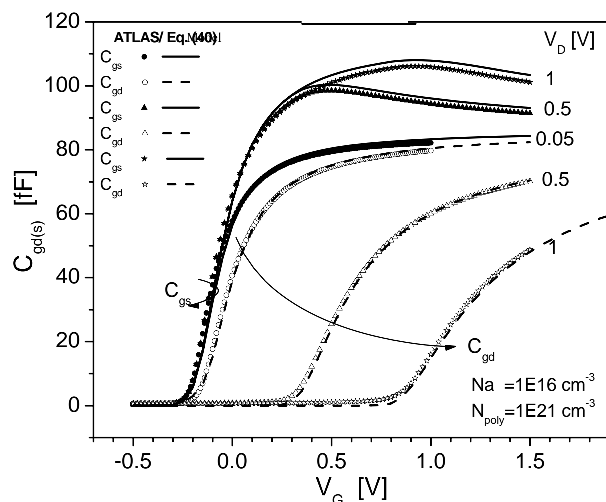

Fig.2A.21 *Gate-source and gate-drain capacitances at drain voltages equal 0.05V, 0.5V and 1 V: from simulation (symbols) and calculated (lines). Si layer doping concentrations equal 10^{16} cm^{-3} and a polysilicon doping equal to10^{21} cm^{-3}.*

Modeled and simulated transfer characteristics in the linear and saturation regions, output characteristics and gate-drain and gate-source capacitance-voltage characteristics show an excellent agreement between them in the practical range analyzed of gate and drain voltages and silicon layer doping concentrations, confirming the validity of the proposed model. In the following chapters, the capacitance model will be adapted to different device geometries with very good results proving again its accuracy.

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2B. Compact model for undoped symmetrical Double-Gate SOI MOSFETs, including Volume Inversion regime characterization

In this section

an analytical, explicit and continuous charge model for undoped symmetrical double gate (DG) MOSFETs is developed [94]. This charge model allows obtaining analytical expressions of all total capacitances. The model is based on a unified charge control model derived from Poisson's equation and is valid from below to well above threshold, showing a smooth transition between the different regimes. The drain current, charge and capacitances are written as continuous explicit functions of the applied bias. The model shows an accurate dependence on the silicon layer thickness, consistent with two dimensional numerical simulations, for both thin and thick silicon films. It demonstrates that the transition from volume inversion regime to dual gate behaviour is well simulated. Whereas the current drive and transconductance are enhanced in volume inversion

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regime, intrinsic capacitances present higher values as well, thus leading to an unclear improvement of the high speed (delay time) behaviour of DG MOSFETs under volume inversion regime [95]. Finally, SCE (Short Channel Effects) like: velocity saturation, channel length modulation and DIBL effects are added to this model [96].These are calculated using an approximate solution of the 2D Poisson's equation.

2B.1. Introduction

Even if actual devices are doped, the use of undoped Si films for DG MOSFET avoids the problems resulting from dopant impurity location randomness and improves carrier transport by the resulting mobility enhancement. The idea of an undoped body is expected to become widespread in the coming years as miniaturization advances [97]. Even though quantum corrections were ignored, this approach is an interesting formulation that is suited for silicon film thicknesses down to 10 nm. For thinner films, quantum effects start to play a role [98-100].

A few analytical channel current models for undoped DG MOSFETs have been presented [33,34,38]. Most of these models require iterations to calculate the drain current. The need of iterations is a drawback compared to explicit models, since it leads to a higher computation time. Even far less work has been done on charge and capacitance modeling of these devices. The capacitance model recently presented in [68], consistent with the

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drain current model of [33], is not analytical, since it requires numerical integration or integral function tabulation. However, analytical charge and capacitance models are much more suitable for circuit simulation.

In this section, based on a previous work, by Sallese et al. [38], where a channel current model, written in terms of the charge densities at the source and drain ends, was developed, we present analytical and explicit charge and capacitance models obtained from the unified charge control model derived by [38] from the 1D Poisson's equation in the direction vertical to the channel. Unlike the model of [101], no approximations are used to derive the charge and capacitance expressions (in terms of the mobile charge densities at source and drain ends) from the charge control model obtained in [38]. The only approximation considered, which is the explicit expression for the mobile charge sheet density (Q), is applied after charge and capacitance expressions are found [84]. We obtain a complete charge-based small-signal model (which includes analytical expressions of the transconductance, output conductance and capacitances). The charge and capacitance expressions are written in terms of explicit and infinitely continuous expressions of the applied bias, which are valid and continuous through all operating regimes. A very good agreement is observed for all the capacitance expressions compared to the 2D device numerical

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simulations. Another very important advantage of this model is the absence of empirical parameters. Therefore, this complete small signal model has the potential to be very successfully used in circuit simulators for the design of integrated circuits using DG MOSFET models. Also, to demonstrate the accuracy of this model, we present results for two different silicon film thicknesses.

We have also tested the impact of Volume Inversion regime on undoped DG MOSFETs' capacitances.

2B.2. Compact Model of a symmetrical undoped DG MOSFET

As in [38] we consider a DG undoped *n*-channel MOSFET ignoring quantum effects and gate poly-Si depletion. We also consider a channel long enough in order that the device electrostatics is described by the 1D Poisson's equation in the direction vertical to the channel.

Neglecting the hole density, Poisson's equation in the silicon is given by:

$$\frac{d^2\phi(x)}{dx^2} = \frac{d^2\left(\phi(x)-V\right)}{dx^2} = \frac{q}{\varepsilon_{Si}} \cdot n_i \cdot e^{\frac{q\left(\phi(x)-V\right)}{kT}} \qquad (2B.1)$$

q being the electronic charge, n_i the intrinsic carrier concentration, ε_{Si} the permittivity of silicon, $\phi(x)$ is the

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electrostatic potential and V the electron quasi-Fermi potential. By solving (2B.1) with the appropriate boundary conditions and a few approximations which were shown to not significantly affect the accuracy of the model, the following implicit unified charge control model is obtained [38] (Q represents the mobile charge sheet density per unit area):

$$(V_{GS}-\Delta\varphi\text{-V})+\frac{kT}{q}\log\left(\frac{qn_i t_{Si}}{8C_{ox}\frac{kT}{q}}\right)-\frac{kT}{q}\log\left(\frac{C_{ox}}{C_{Si}}\right)= \\ =\frac{Q}{2C_{ox}}+\frac{kT}{q}\left(\log\left(\frac{Q}{8C_{ox}\frac{kT}{q}}\right)+\log\left(\frac{C_{Si}}{C_{ox}}+\frac{Q}{8C_{ox}\frac{kT}{q}}\right)\right) \tag{2B.2}$$

where Δφ is the work function difference between the gate electrode and the intrinsic silicon, C_{Si} is the silicon capacitance and C_{ox} is the oxide capacitance.

2B.2.1 Drain Current Model

The drain current in a DG MOSFET is calculated as [38]:

$$I_{DS}=\frac{W\mu}{L}\int_{0}^{V_{DS}}Q(V)\,dV \tag{2B.3}$$

where μ is the effective mobility of the electrons, W the width of the device and L the channel length.

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From (2B.2) we obtain:

$$dV = -\frac{dQ}{2C_{ox}} - \frac{kT}{q}\left(\frac{dQ}{Q} + \frac{dQ}{Q+2Q_0}\right) \quad \text{(2B.4)}$$

where $Q_0 = 4\frac{kT}{q}C_{Si}$.

Integrating (2B.3) using (2B.4), between Q_s and Q_d ($Q=Q_s$ at source end and $Q=Q_d$ at the drain end), we obtain an expression of I_{DS} in terms of carrier charge densities [38]:

$$I_{DS} = \frac{W\mu}{L}\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{4C_{ox}} + 8\left(\frac{kT}{q}\right)^2 C_{Si}\log\left[\frac{Q_d + 2Q_0}{Q_s + 2Q_0}\right]\right] \quad \text{(2B.5)}$$

Equation (2B.2) does not yield a closed form expression for Q; therefore, in [38] Q had to be found iteratively from (2B.2). However, in this section we propose an approximate explicit expression, which was demonstrated to be a very good solution for an equation of the type of (2B.2). In [84] an explicit continuous expression for the mobile charge sheet density was used. Since for undoped DG MOSFETs the charge control model (2B.2) has a similar form as for Surrounding-Gate MOSFETs [84] we can use an explicit expression for Q of the same type, adapted to DG MOSFETs, that has also been explained in section 2A.

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The explicit expression for Q we use is:

$$Q = 2C_{ox}\left(-\frac{2C_{ox}\beta^2}{Q_0}+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_0}\right)^2+4\beta^2\log^2\left[1+\exp\left[\frac{V_{GS}-V_T+\Delta V_T-V}{2\beta}\right]\right]}\right) \quad (2B.6)$$

where $\beta = \frac{kT}{q}$. V_T is defined as:

$$V_T = V_0 + 2\beta\log\left(1+\frac{Q'}{2Q_0}\right) \quad (2B.7)$$

where Q' is actually the first iteration result when solving (2B.2) for Q:

$$Q' = C_{ox}\left(-\frac{2C_{ox}\beta^2}{Q_0}+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_0}\right)^2+4\beta^2\log^2\left[1+\exp\left[\frac{V_{GS}-V_0-V}{2\beta}\right]\right]}\right) \quad (2B.8)$$

and $$V_0 = \Delta\varphi - \beta\cdot\log\left(\frac{qn_i t_{Si}}{2Q_0}\right) \quad (2B.9)$$

In (2B.6), the term ΔV_{th} ensures the correct behaviour of Q above threshold [84]:

$$\Delta V_T = \frac{\left(\frac{C_{ox}\beta^2}{Q_0}\right)Q'}{Q_0+\frac{Q'}{2}} \quad (2B.10)$$

Therefore Q_s and Q_d in the I_{DS} expression (2B.5) are analytically computed by applying V=0 and V=V_{DS} respectively, in (2B.6)-

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(2B.10). Using this expression of the I_{DS} current, (2B.5) and the charge control model (2B.2), we can compute the transconductance (g_m) and drain conductance (g_d) parameters.

After some manipulations, we obtain:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{W\mu}{L}\left(Q_s - Q_d\right) \tag{2B.11}$$

$$g_d = \frac{\partial I_{DS}}{\partial V_{DS}} = \frac{W\mu}{L} Q_d \tag{2B.12}$$

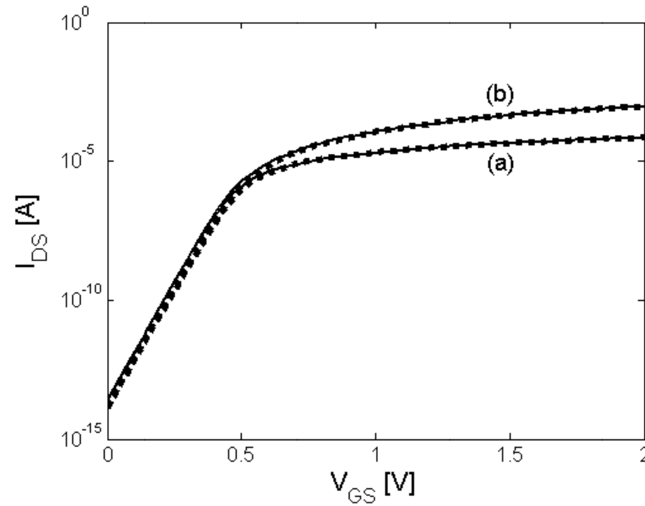

Fig.2B.1 *Transfer characteristics, for V_{DS}=0.05V (a) and for V_{DS}=1V (b), for t_{Si}=20nm in logarithmic scale. Solid line: DESSIS-ISE simulation; Symbol line: analytical model using (2B.5)*

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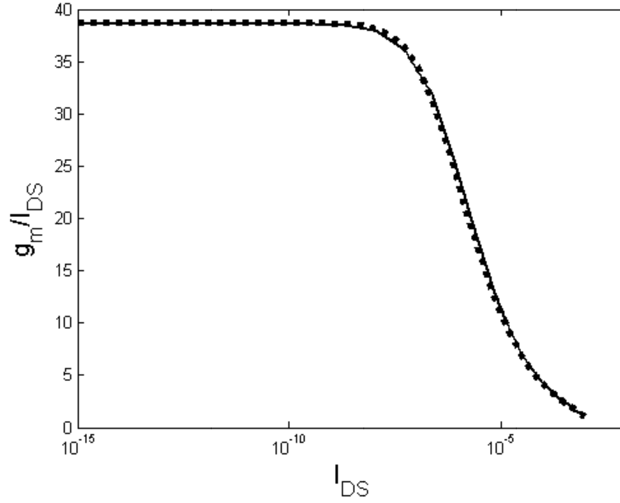

Fig.2B.2 *The transconductance g_m normalized to the drain-source current, for t_{Si}=20nm and V_{DS}=1V. Solid line: DESSIS-ISE simulation; Symbol line: analytical model*

2B.2.2. Charge and Capacitance Model

The total channel charge is obtained by integrating the mobile charge sheet density over the channel length:

$$Q_{Tot} = -W\int_0^L Q dx = -W^2 \frac{\mu}{I_{DS}} \int_0^{V_{DS}} Q^2 dV \qquad (2B.13)$$

Using (2B.4) in (2B.13) we get:

$$Q_{Tot} = -W^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left(\frac{Q^2}{2C_{ox}} + \frac{kT}{q} Q + \frac{kT}{q} \frac{Q^2}{Q+2Q_0} \right) dQ \qquad (2B.14)$$

The resulting expression of Q_{Tot} is given in the Appendix.

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The total gate charge is obtained as Q_G=-Q_{Tot}-Q_{ox}, where Q_{ox} is the total oxide fixed charge at the oxide/silicon interface. The intrinsic capacitances, C_{gd} and C_{gs}, are obtained as [102]:

$$C_{gi} = -\frac{dQ_G}{dVi} \tag{2B.15}$$

where *i=d,s*

We obtain these capacitances by differentiating Q_{Tot} according to (2B.4).

Both Q_{Tot}, C_{gd} and C_{gs} are written in terms of the mobile charge sheet densities at the source and drain ends. Using the charge explicit formula in [84] for the mobile charge sheet densities at source and drain, the expressions of Q_{Tot}, C_{gd} and C_{gs} become explicit.

Following the Ward's channel charge partitioning scheme [70], and using (2B.4) we obtain analytical expressions for the total drain (Q_D) and source (Q_S) charges:

$$Q_D = -W\int_0^L \frac{x}{L} Q dx = -\frac{W^3\mu^2}{L(I_{DS})^2}\int_{Q_s}^{Q_d} Q^2 \left(\begin{array}{l} \left(\dfrac{Q^2 - Q_s^{\,2}}{4C_{ox}}\right) + \\ + \dfrac{kT}{q}\left(2(Q-Q_s) - 2Q_0 \log\left[\dfrac{Q+2Q_0}{Q_s+2Q_0}\right]\right) \end{array} \right) \cdot \left(\frac{1}{2C_{ox}} + \frac{kT}{q}\left(\frac{1}{Q} + \frac{1}{Q+2Q_0}\right)\right) dQ \tag{2B.16}$$

$$Q_S = Q_{Tot} - Q_D \tag{2B.17}$$

(The solution for Eq. (2B.16) is given in Appendix)

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The non-reciprocal capacitances C_{dg} and C_{sg} are obtained as [102]:

$$C_{ig} = -\frac{dQ_i}{dV_G} \tag{2B.18}$$

where $i=d,s$

The capacitances C_{sd} and C_{ds} are computed as follows [102]:

$$C_{ds} = -\frac{dQ_D}{dV_S} \tag{2B.19}$$

$$C_{sd} = -\frac{dQ_S}{dV_D} \tag{2B.20}$$

By differentiating Q_D and Q_S as in [84], analytical expressions of all these capacitances are obtained in terms of the mobile charge sheet densities at the source and drain ends. These expressions become explicit by using the charge formula in (2B.6)-(2B.10) to calculate the mobile charge sheet densities at source and drain. Therefore, analytical and explicit expressions of all the capacitances have been obtained.

It has to be remarked that, due to charge conservation, only four out of the nine possible capacitances are independent. The other five capacitances can be calculated from the four independent capacitances using equations derived from the charge conservation equation.

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At V_{DS}=0, the capacitance expressions go to 0/0; to avoid numerical instability when the drain voltage is close to 0, we could use the asymptotic value of the capacitances [68].

In order to compute the limits of the capacitances when V_{DS}=0, we use the fact that at V_{DS}=0, the gate-channel capacitance per unit area is constant along the channel. Since the quasi-Fermi potential at any point of the channel is equal to its value at the source end, and the gate charge sheet density is equal to the channel charge sheet density, the gate-channel capacitance per unit area is given by $\frac{\partial Q_s}{\partial V_s}$.

Therefore, at V_{DS}=0, using (2B.4), the total gate capacitance will be equal to:

$$C_{gg} = WL\frac{\partial Q_s}{\partial V_s} = -\frac{WL}{\frac{1}{2C_{ox}} + \frac{kT}{q}\left(\frac{1}{Q_s} + \frac{1}{Q_s + 2Q_0}\right)} \tag{2B.21}$$

The rest of transcapacitance expressions, as V_{DS} tends to 0, can be computed from C_{gg} as in undoped cylindrical Surrounding Gate MOSFETs [103] (since the charge control model has the same form [69,84]):

$$C_{gg} = 2C_{gd} = 2C_{dg} = 2C_{gs} = 2C_{sg} = -6C_{ds} = -6C_{sd} \tag{2B.22}$$

The very good agreement proves the correct behaviour of this model, for V_{DS} =0.

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Therefore, when V_{DS}=0 we use the above way for computing the capacitances. Near V_{DS}=0, the charge and capacitance equations may still create numerical instability problems, for $0<V_{DS}<\varepsilon_C$ (where ε_C is a very low V_{DS} value which depends on the software used). However, we can observe that for very low values of V_{DS} the capacitance characteristics depend approximately linearly on the drain voltage (Fig.2B.5b, 2B.5c). Therefore, to avoid numerical instability, the following linear approximation can be used:

$$C_{ij} = C_{ij}\left(V_{DS} = 0\right) + V_{DS}\frac{C_{ij}\left(V_{DS} = \varepsilon_C\right) - C_{ij}\left(V_{DS} = 0\right)}{\varepsilon_C} \quad (2B.23)$$

For the case when $V_{DS}>\varepsilon_C$, the capacitances are computed using the equations (2B.13)–(2B.20). This modeling ensures the continuity of the capacitances at $V_{DS}=\varepsilon_C$. The continuity of the charge expressions Q_i near V_{DS}=0 is achieved by using a linear approximation for the interval $0<V_{DS}<\varepsilon_Q$, where ε_Q is a very low V_{DS} value which depends on the software used and does not need to be the same as ε_C.

$$Q_i = Q_i\left(V_{DS} = 0\right) + V_{DS}\frac{Q_i\left(V_{DS} = \varepsilon_Q\right) - Q_i\left(V_{DS} = 0\right)}{\varepsilon_Q} \quad (2B.24)$$

For the case when $V_{DS}>\varepsilon_Q$, the charge expressions are computed using the equations (2b.25)–(2b.26), given in Appendix .

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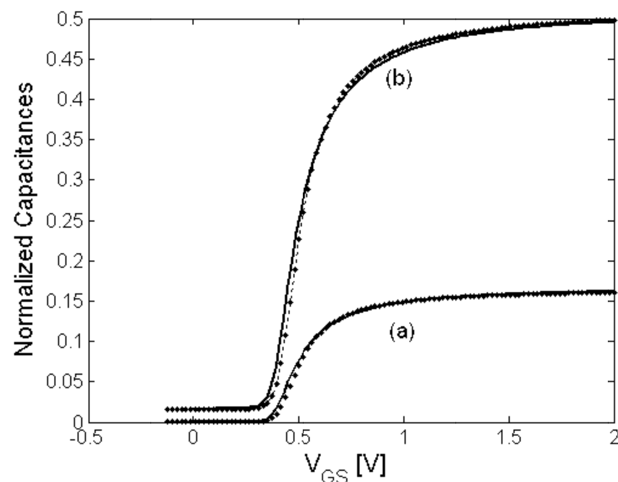

Fig.2B.3 *Normalized source-to-drain capacitance in (a), gate-to-drain capacitance, gate-to-source capacitance and drain-to-gate capacitance in (b) with respect to the gate voltage, for $V_{DS} = 0$ V, for t_{Si}=20nm. Solid line: DESSIS-ISE simulations. Symbols: our model*

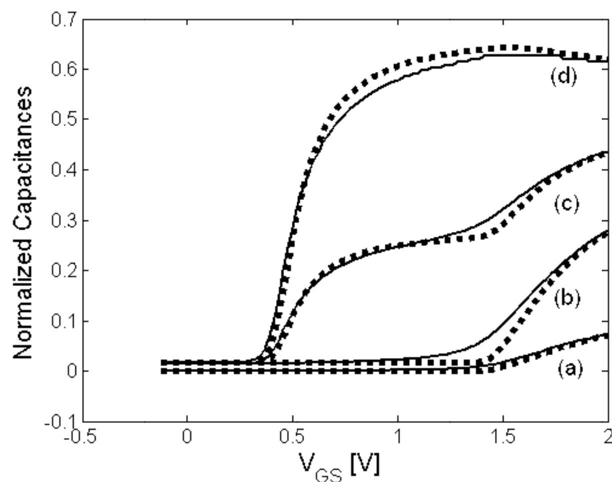

Fig.2B.4 *Normalized source-to-drain capacitance in (a), gate-to-drain capacitance in (b), drain-to-gate capacitance in (c) and gate-to-source capacitance in (d) with respect to the gate voltage, for V_{DS} = 1V, for t_{Si}=20nm. Solid line: DESSIS-ISE simulations. Symbol line: analytical model.*

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2B.2.3 Simulation Results

To validate this model, we have compared our modeled capacitance characteristics with 2D numerical simulations using DESSIS-ISE [104]. We have assumed a device with channel length L=1μm, a device width of W=1 μm, a silicon oxide thickness t_{ox}=2 nm and two silicon film thickness t_{Si}=20 nm and t_{Si}=10 nm . We have considered Q_{ox}=0. We have used a constant mobility equal to 300 cm^2/Vs. Figures 2B.1-2B.5 present the results for the case when the silicon film thickness equals 20nm and Figures 2B.6-2B.7, for the case when the silicon film thickness equals 10nm.

Fig.2B.1 shows the comparison between the modeled (using our explicit expressions) and numerically simulated transfer characteristics. As expected, the agreement between them is very good. Also the model presents a smooth transition between all the operation regimes (linear, saturation and subthreshold) without fitting parameters. In Fig.2B.2 we present the comparison between the simulated and modeled g_m / I_{DS} (a main parameter in analog design), which also proves to be very good. Excellent agreement is also observed between the modeled and numerically simulated values of C_{gd}, C_{gs} , C_{dg} and C_{sd} (Fig 2B.3, 2B.4), as functions of the gate voltage, for different values of the drain-source voltage (0V and 1V, respectively). In these figures all the capacitances are presented

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in the normalized form, as $C/2WC_{ox}L$, where C represents the capacitances C_{gd}, C_{gs}, C_{dg} and C_{sd}. In order to have a complete model for the drain and source capacitances, we have to account for the parasitic capacitance, which in the case of the 2D simulations (with DESSIS-ISE) of C_{gd}, C_{gs}, C_{dg} appears to be a constant ($5.6{\cdot}10^{-16}$ F) and is added to the expressions of the intrinsic capacitances as a constant, showing an almost perfect agreement (Fig 2B.3-2B.5). Fig.2B.5a presents the source-to-drain capacitance, gate-to-drain capacitance, drain-to-gate capacitance and gate-to-source capacitance with respect to the drain voltage, for the strong inversion regime (V_{GS} = 1.5 V).

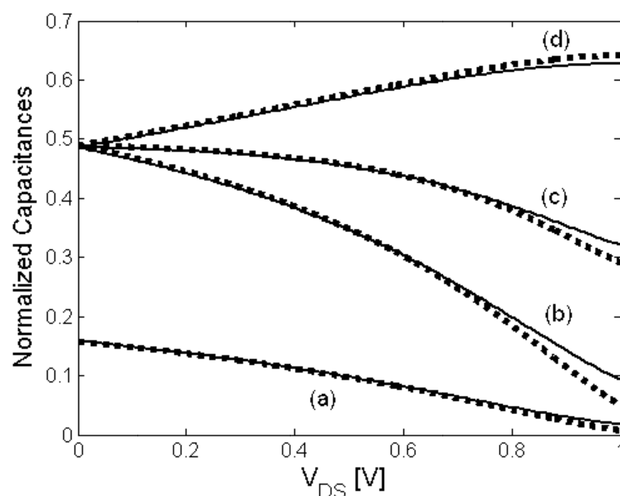

Fig.2B.5a *Normalized source-to-drain capacitance in (a), gate-to-drain capacitance (b), drain-to-gate capacitance (c) and gate-to-source capacitance (d) with respect to the drain voltage, for* V_{GS} *= 1.5 V, for* t_{Si}*=20nm. Solid line: DESSIS-ISE simulations. Symbol line: analytical model.*

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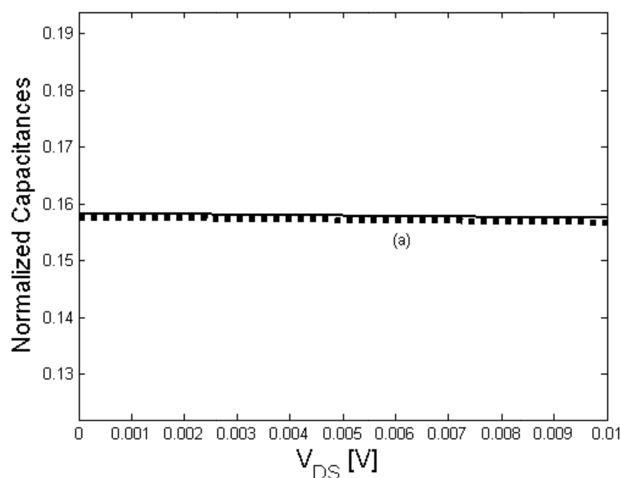

Fig.2B.5b *Zoom-in on Fig.2B.5a showing V_{DS} from 0 V to 0.01V, where (a) is the source-to-drain capacitance. Solid line: DESSIS-ISE simulations. Symbol line: analytical model.*

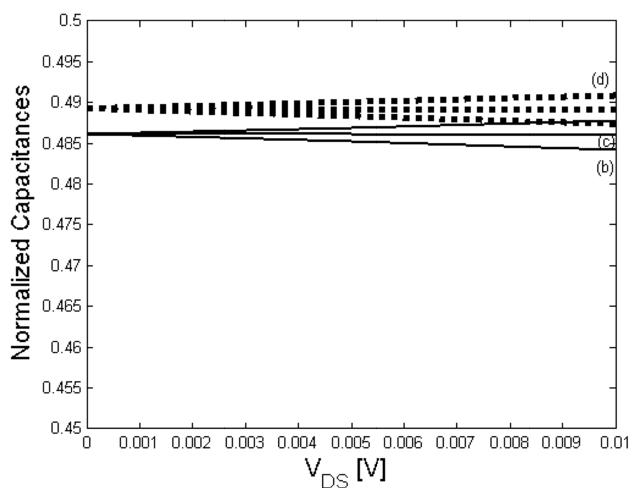

Fig.2B.5c *Zoom-in on Fig.2B.5a showing V_{DS} from 0 V to 0.01V, where (b) is the gate-to-drain capacitance, (c) is the drain-to-gate capacitance and (d) is the gate-to-source capacitance Solid line: DESSIS-ISE simulations. Symbol line: analytical model.*

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We show a zoom-in on Fig.2B.5a around the region where V_{DS}=0V (Fig.2B.5b, Fig.2B.5c) and the result proves to be very good. Also, an excellent agreement is observed for all the capacitances, for all V_{DS} biases, when taking into consideration t_{Si}=10nm. (Fig.2B.6-7). The constant parasitic capacitance added to the expressions of the intrinsic capacitances C_{gd}, C_{gs}, C_{dg} is, in this case, $5 \cdot 10^{-16}$ F.

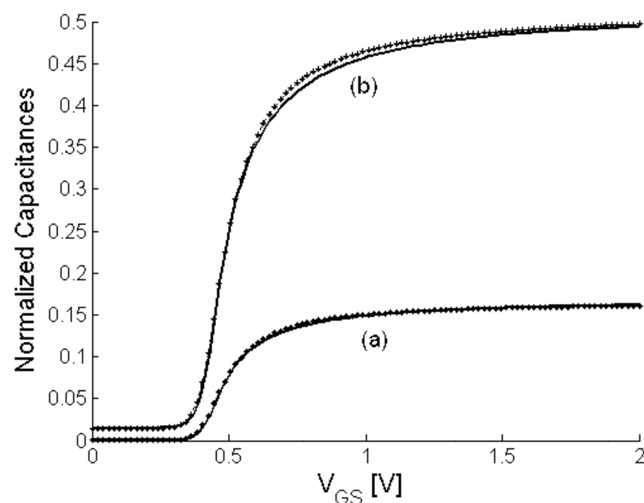

Fig.2B.6 *Normalized source-to-drain capacitance in (a), gate-to-drain capacitance, gate-to-source capacitance and drain-to-gate capacitance in (b) with respect to the gate voltage, for V_{DS} = 0 V, for t_{Si}=10nm. Solid line: DESSIS-ISE simulations. Symbol line: analytical model.*

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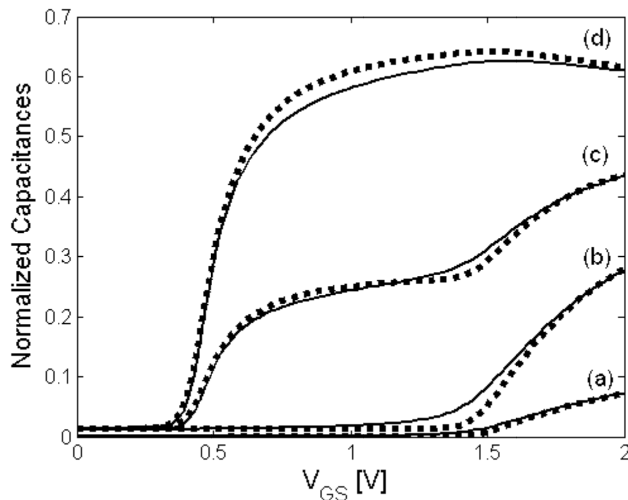

Fig.2B.7 *Normalized source-to-drain capacitance in (a), gate-to-drain capacitance in (b), drain-to-gate capacitance in (c) and gate-to-source capacitance in (d) with respect to the gate voltage, for* V_{DS} = *1V, for* t_{Si}*=10nm. Solid line: DESSIS-ISE simulations. Symbol line: analytical model.*

The modeled capacitances in this section show excellent agreement with the 2D numerical simulations, in all operating regimes, for all V_{DS} biases and for different silicon film thicknesses, proving the accuracy of this model.

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2B.3 Volume Inversion impact on symmetrical undoped DG MOSFETs' capacitances

2B.3.1 Volume-Inversion Effect

Thanks to the volume inversion (VI) phenomena, one of the main features in DG MOSFETs, a 25% electron mobility improvement is observed for a range of silicon layers between 5 and 20 nm [21]. Under VI regime the potential increases at the middle of the silicon layer. However, charge-sheet-based models (developed for bulk MOSFETs and single-gate SOI MOSFETs) cannot properly describe volume inversion, a unique characteristic of double-gate (DG) MOSFETs, in the subthreshold region [105]. Contrary to bulk MOSFETs, depletion charges in DG MOSFETs are often negligible since the silicon film is usually undoped (or lightly doped). Thus, in this case only the mobile charge term needs to be included in Poisson's equation, and it should be considered along the whole Si thickness. Therefore, the exact solutions to Poisson's and current continuity equations based on Gradual Channel Approximation (GCA) should be derived without the charge-sheet approximation [68], thus correctly describing the VI phenomena. As explained in section 2B.2, we developed a compact DG MOSFET model by considering the carrier charge density in the Poisson's equation, without assuming the charge

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sheet approximation. Therefore, our model can be a very promising tool to study the volume inversion effect.

Several authors have claimed that volume inversion presents a significant number of advantages, such as: enhancement of the number of minority carriers; increase in carrier mobility and velocity due to reduced influence of scattering associated with oxide and interface charges and surface roughness. As a consequence of the latter, an increase in drain current and transconductance, a decrease of low frequency noise, and a great reduction in hot-carrier effects have been presented [19]. The increase of current and transconductance thanks to the volume inversion seems to lead to better high-speed (lower delay time) and high-frequency (higher cutoff frequency) characteristics. However, a complete evaluation of the high-speed and high-frequency performance of these devices needs to properly consider the effect of the volume inversion on the transcapacitances, which so far have not been appropriately addressed.

In this section, we demonstrate the ability of our previously presented DG-MOSFET analytical model (see section 2B.2) to correctly predict volume-inversion and film thickness effects in the transcapacitance characteristics, without the need of iterative computations as in [106]. As before, in the previous section, the

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model is validated by DESSIS two-dimensional (2-D) simulations.

At lower gate bias (below the threshold voltage) the carriers spread out across the silicon film thus indicating the presence of volume inversion, so the potential and electron concentration at the centre and surface of the film are not very different. But, at higher gate voltage (V_{GS}), the carriers at the surface screen those at the centre, therefore the potential at the centre will not increase with any increase in V_{GS} [23]. Therefore, in weak inversion the dominant current flows will be at the centre of the silicon film and in strong inversion it will shift to the gate oxide interface (top and bottom Si channel surfaces). This means that the drain current dependence on the Si film thickness (t_{Si}) will be stronger in the subthreshold region (as a manifestation of the VI) than above threshold where the drain current depends much less on t_{Si}.

An accurate reproduction of the mobility dependence on the film thickness (in conditions of volume inversion) is still not very clear, and it also depends very much on the process. Although certainly the mobility is, in a moderately thin DG MOSFET, higher when compared with a single-gate transistor in which the conduction only takes place at the gate-interface, a strong decrease of the Si film thickness may lead to a further decrease of the mobility. As a consequence, researchers are interested in

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determining an optimum value of the film thickness in terms of mobility behavior. According to Shoji *et al.* [107]-[108] the optimum thickness of the silicon layer in DG MOSFETs is around 10 nm, from the phonon-limited mobility viewpoint. They have shown that in DG MOSFETs, as silicon thickness is reduced, phonon-limited mobility increases gradually to a maximum around t_{Si} = 10 nm, decreases in the 5-10 nm range to values below the value for the case of conventional bulk MOSFETs, rises rapidly to another maximum in the vicinity of t_{Si} = 3 nm, and finally falls. However, phonon scattering is not the only scattering mechanism present in these devices. Very thin t_{Si} will result in degraded electron mobility due also to severe surface-roughness scattering [109]**,** so the minimum value for t_{Si} should be around 5 nm.

Anyway, we must not forget that in order to achieve volume inversion regime, both channels must interact strongly, and this only happens in the medium-high transverse electric field range when the silicon thickness between the two oxides is thin enough (below 20 nm as pointed out by [107] and [110]). However, we show in this section that even at a silicon thickness of 40 nm we see evidence of VI. For this we make comparisons between intrinsic capacitances values in a device with a very thick silicon film of 100 nm (where we do not expect VI) and for t_{Si} equal to 10 and 40 nm. We do not consider quantum

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effects, since they can be assumed to be negligible for t_{Si} larger than 10 nm.

2B.3.2 Simulation results

An undoped device is considered, with channel length L = 1 μm, a width of W = 1 μm, a silicon oxide thickness t_{ox} = 2 nm.

We show the continuity of our model in the capacitance characteristics from subthreshold to strong inversion and from linear to saturation (Figs. 2B.8-2B.9), for different values of t_{Si}.

In Figs. 2B.8 and 2B.9 we demonstrate that our model captures the Si film thickness dependence in the gate-to-source capacitance (C_{gs}) characteristics, which proves its capability to accurately model the VI phenomena. The capacitance C_{gs} presents a higher value (thus a higher I_{DS} value) for t_{Si} equal to 10 and 40 nm than for the case of t_{Si} = 100 nm, in weak inversion, for different V_{DS} values. This capacitance increase is directly related to an increase of the free carriers controlled by both gates under VI regime. It is worth noting that for t_{Si} = 40 nm there is an increase in the value of normalized C_{gs} compared to the one for t_{Si} = 100 nm, which indicates that efficient VI appears even for a thickness of 40 nm. C_{gs} is presented in a normalized form as:

$$C_{gs} = \text{gate-to-source capacitance} / (2\, C_{ox}\, W\, L) \qquad (2B.25)$$

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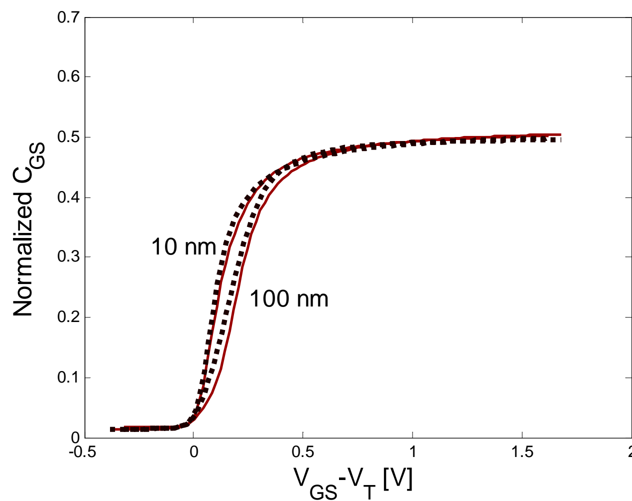
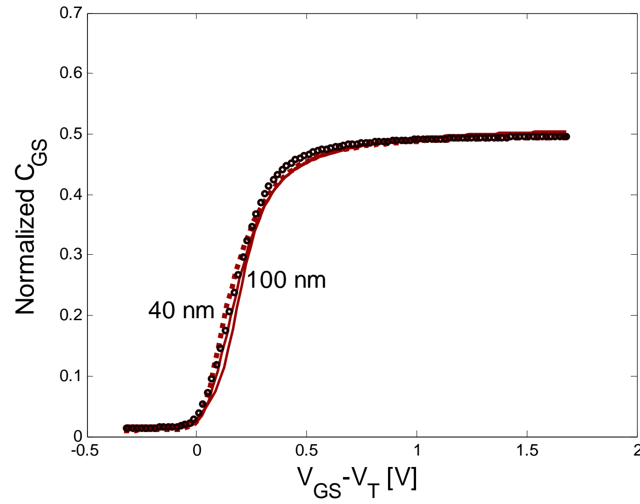
$$\text{with } C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2B.26}$$

where ε_{ox} is the absolute permittivity of silicon dioxide and t_{ox} the gate oxide thickness.

In (2B.25), the factor 2 is to take into account the contribution of both gates. For the extraction of the capacitance threshold voltages (V_t) the well known extrapolation method was used.

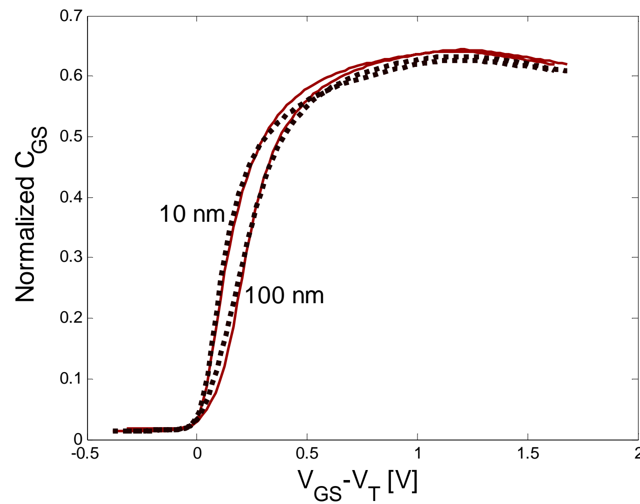


(a)



(b)

Fig.2B.8 *Normalized gate-to-source capacitance, with respect to the gate overdrive, for V_{DS} = 0.05 V, (a) for t_{Si} = 10 and 100 nm, and (b) for t_{Si} = 40 and 100 nm (symbol 'o'). Dashed line: DESSIS-ISE simulations, Solid line: our analytical model.*



(a)

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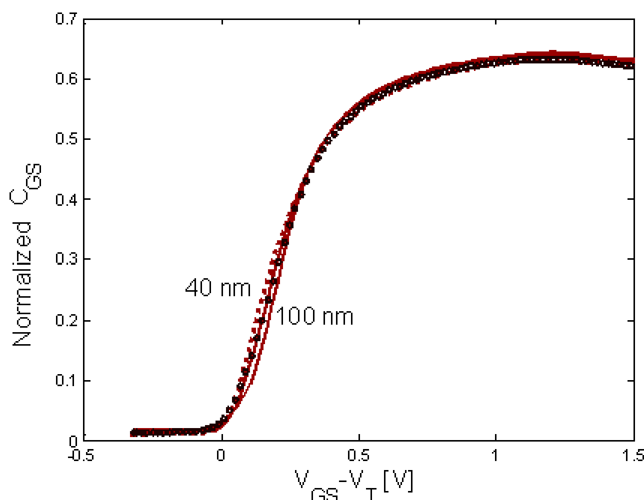

(b)

Fig.2B.9 *Normalized gate-to-source capacitance, with respect to the gate overdrive, for V_{DS} = 1 V, (a) for t_{Si} = 10 and 100 nm, and (b) for t_{Si} = 40 and 100 nm (symbol 'o'). Dashed line: DESSIS-ISE simulations, Solid line: our analytical model.*

We have not considered the dependence of the mobility with the Si film thickness. For simplicity, a constant mobility value has been used in the DESSIS-ISE simulations and in our analytical model. A constant mobility model certainly does not take into account the fact that the mobility should be higher at the centre of the film than at the interfaces (which is the main advantage of the volume inversion in the transconductance characteristics), but actually in DESSIS-ISE, as in many simulators, it is not very clear how to determine the mobility model that has the most correct dependence of the film thickness, and even adjustable

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parameters are used in the available mobility model. This is not so important, since we focus on capacitance modelling, and the mobility has a very minor effect. Therefore, for this study, a proper electrostatic model of the VI effect, with the correct film thickness dependence, is sufficient.

It has to be mentioned that in order to extend the model from section 2B.2 to high values of t_{Si} we had to change the ΔV_T function from Eq. (2B.10):

$$\Delta V_T = \frac{\left(\frac{C_{ox}\beta^2}{Q_0}\right)Q'}{A\sqrt{T_{Si}} + \frac{Q'}{2}} \tag{2B.27}$$

This factor is only used to adjust the transition between subthreshold and strong inversion so it does not affect the model performance in the other regimes. The constant A is equal to 10 C/m. The same ΔV_T function is considered for all t_{Si} values. As in [94], we find a constant parasitic fringing capacitance that has to be added to the expression of the intrinsic capacitance C_{gs}, for t_{Si} equals 10, 40 and 100 nm, of $5\cdot10^{-16}$ F, $5\cdot10^{-16}$ F and $6\cdot10^{-16}$ F, respectively. In Figs. 2B.10 and 2B.11, we present, for a clearer view, the normalized difference $\Delta C_{gs} = C_{gs}$ (t_{Si} = 100 nm) - C_{gs} (t_{Si} = 10 nm) and $\Delta C_{gs} = C_{gs}$ (t_{Si} = 100 nm) - C_{gs} (t_{Si} = 40 nm).

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Those graphs demonstrate the continuity of the model between the volume inversion and dual-gate regime. In weak inversion close to the threshold voltage, we can see an important value for ΔC_{gs} due to a strong increase of C_{gs} for t_{Si} = 10 nm compared to the capacitance value in the case of t_{Si} = 40 nm. It is directly related to the enhancement of the minority carriers' number under volume inversion regime. However, in strong inversion the two capacitances will have almost the same value since the volume inversion is not efficient anymore. In strong inversion, we observe an important difference between the model and the simulations but because the capacitances in that regime are high, the relative error will be small.

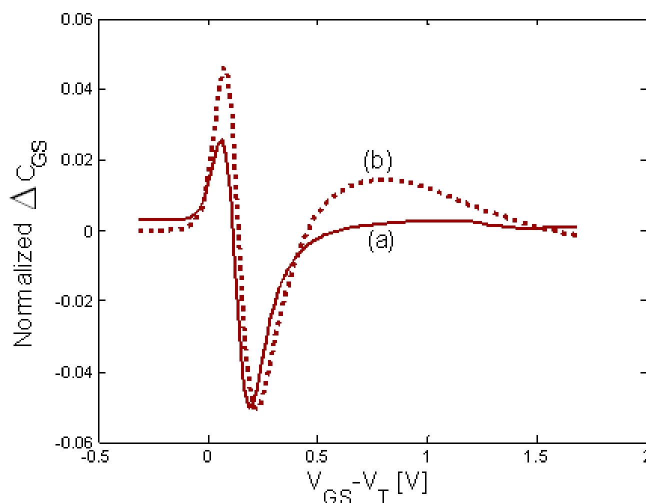

Fig.2B.10 *Normalized Δ C_{gs} with respect to the gate overdrive, for V_{DS} = 1 V, Δ C_{gs} = C_{gs} (t_{Si} = 100 nm) - C_{gs} (t_{Si} = 10 nm). (a) Solid line: our analytical model and (b) Dashed line: DESSIS-ISE simulations.*

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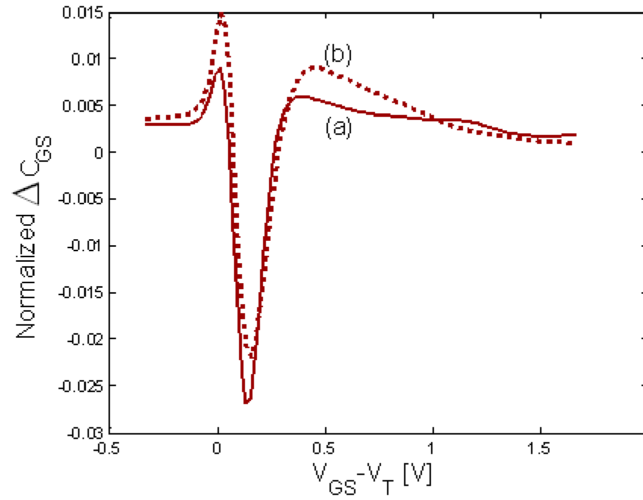

Fig.2B.11 *Normalized Δ C_{gs} with respect to the gate overdrive, for V_{DS} = 1 V, Δ C_{gs} = C_{gs} (t_{Si} = 100 nm) - C_{gs} (t_{Si} = 40 nm). (a) Solid line: our analytical model and (b) Dashed line: DESSIS-ISE simulations.*

One of the important factor of merits in the digital field is the delay time equal to [24]:

$$C_{GG}.V_{DD}/I_{DS} \qquad (2B.28)$$

Where C_{GG} is the total gate capacitance, V_{DD} the supply-voltage (V_{DD} = V_{GS} for the on-state). In weak inversion for t_{Si} = 10 and 40 nm C_{GG} is higher than for t_{Si} = 100 nm as illustrated in Fig. 2B.10 and 2B.11. Thus, in VI regime, besides the drain current (I_{DS}) related to the higher carrier mobility at the centre of the channel, we also see a gate capacitance increase. Therefore, the delay time for t_{Si} = 10 or 40 nm may not be better than the one

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for t_{Si} = 100 nm. Furthermore, if we dramatically decrease the silicon film thickness the mobility (and therefore the drain current) may decrease due to higher surface roughness scattering, and this would lead to a further increase of the delay time.

In conclusion, because of the increase of the intrinsic capacitance, the volume inversion regime in thin film DG MOSFETs may not bring any improvement for the delay time with respect to a transistor with a thicker silicon film in which volume inversion does not take place, and a further reduction of the Si film thickness seems to clearly increase the delay time. Therefore, the advantages of reducing the Si film thickness for high-speed and high-frequency operation are not clear.

However, the reduction of the Si film thickness in conditions of volume inversion reduces short channel effects permitting the downscaling of the device's channel length. The developed model simulates the volume inversion and Si film dependence thickness effects in the DG-MOSFET down to a silicon layer of 10 nm-thick.

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2B.4. Short Channel Effects in symmetrical undoped DG MOSFETs

2B.4.1. Model

In this subsection we extend our long-channel DG undoped model to short-channel devices. As in [38] and [94] we consider a DG undoped MOSFET ignoring quantum effects and polydepletion. As a starting point we consider the explicit long channel drain current model, which is described in section 2B.2 (based on the charge control model presented in 2A.2). It will be the backbone of this model, to which we will add various short channel effects. This short-channel DG MOSFET model could be later extended by including quantum effects.

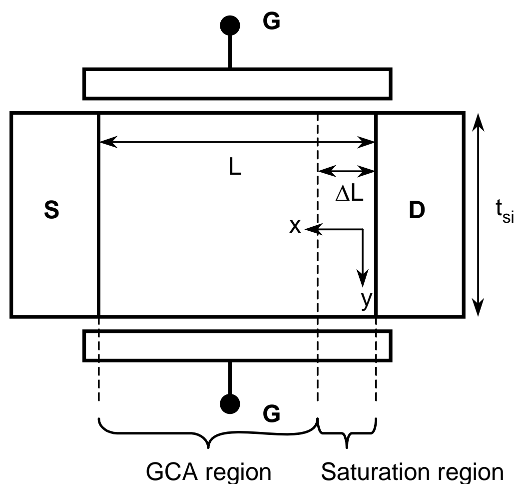

Fig.2B.12 *Schematic representation of the DGMOSFET considered in this section*

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2B.4.1.1. Velocity saturation

One of the most used expressions for the saturation potential for electron is [111]

$$V_{sat} = \left(V_{GS} - V_t\right) \frac{v_{sat}}{\frac{\mu_{eff}}{2L}\left(V_{GS} - V_t\right) + v_{sat}} \tag{2B.29}$$

μ_{eff} being the effective mobility, v_{sat} the saturation velocity, and V_t the threshold voltage. To extend the validity of this relation to weak inversion, we replaced V_{GS}-V_t by $Q_s/(2C_{ox})$ [111], which is a term that tends to V_{GS}-V_t in strong inversion and to 0 in low inversion, Q_s being the charge at the source end of the channel. Thus,

$$V_{sat} = \left(-Q_s / 2C_{ox}\right) \frac{v_{sat}}{-Q_s \frac{\mu_{eff}}{4LC_{ox}} + v_{sat}} \tag{2B.30}$$

However, with this equation, V_{sat} tends to 0 in weak inversion, whereas the theoretical value is 2kT/q. To correct this, we propose to replace Q_s in (2B.30) with Q_s' so that we have:

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$$V_{sat} = \left(-Q_s'/2C_{ox}\right)\frac{v_{sat}}{-Q_s'\frac{\mu_{eff}}{4LC_{ox}} + v_{sat}} \qquad (2B.31)$$

with $Q_s' = Q_s + 4\frac{kT}{q}C_{ox}\frac{v_{sat}}{v_{sat} - \frac{kT}{q}\frac{\mu_{eff}}{L}}$

This way, Q_s' tends to Q_s in strong inversion, and to a value that gives the correct V_{sat} in weak inversion.

The usual approximated relation for the mobility dependence with the longitudinal electric field is:

$$\mu = \frac{\mu_{eff}}{1 + \frac{\mu_{eff}}{v_{sat}}\frac{V_{sat}}{L - \Delta L}} \qquad (2B.32)$$

where ΔL is the length of the saturation region. However, the results have been found to be far better with the more precise relation:

$$\mu = \frac{\mu_{eff}}{\left(1 + \left(\frac{\mu_{eff}}{v_{sat}}\frac{V_{sat}}{L - \Delta L}\right)^{n_m}\right)^{1/n_m}} \qquad (2B.33)$$

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with n_m=2. In fact, Eq. (2B.32) is a usual approximation of Eq. (2B.33).

If we replace the above expression in the equation of the drain current (2B.5), we obtain:

$$I_{DS} = \frac{W\mu_{eff}}{L_e}\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{4C_{ox}} + 8\left(\frac{kT}{q}\right)^2 C_{Si}\log\left[\frac{Q_d + 2Q_0}{Q_s + 2Q_0}\right]\right] \qquad (2B.34)$$

In this way, I_{DS} is expressed in terms of μ_{eff}. Velocity saturation is taken into account in L_e, which can be considered as an effective gate length due to the effect of velocity saturation [112]:

$$L_e = (L - \Delta L)\left[1 + \left(\frac{\mu_{eff} V_{sat}}{v_{sat}(L - \Delta L)}\right)^{n_m}\right]^{\frac{1}{n_m}} \qquad (2B.35)$$

We found necessary to use the exact relation for longitudinal field dependence of the mobility, as the approximated relation was fairly inaccurate in reproducing the ATLAS drain current simulations.

For the model to be continuous during the transition to saturation regime, we need to introduce an effective drain voltage, that is equal to V_{DS} in the linear regime and that

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becomes continuously and progressively equal to V_{sat} in the saturation regime. A possible expression is [113]:

$$V_{deff} = V_{sat} - V_{sat}\frac{\ln\left[1+\exp\left(1-\frac{V_{DS}}{V_{sat}}\right)\right]}{\ln\left[1+\exp\left(A\right)\right]} \qquad (2B.36)$$

where A is a fitting parameter which defines the abruptness of the transition V_{DS} to V_{sat}. A value of A=6 worked well in this case.

2B.4.1.2. Series resistances

For a not too high series resistance, R_s, its effect can be modeled to the first order, as a corrective term in the mobility expression:

$$\mu_{eff} = \left(\left(\mu_{eff}{}^{0}\right)^{-1} + \left(\mu_{Rs}\right)^{-1}\right)^{-1} \qquad (2B.37)$$

Where μ_{eff} and μ_{eff}^{0} are respectively the effective mobility with and without series resistance, and

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$$\mu_{Rs} = \frac{1}{2C_{ox}R_S\, W/(L-\Delta L)\left(Q_d/(2C_{ox}) + 0.5V_{deff}\right)}$$

A possible well known expression for μ_{eff} is:

$$\mu_{eff}{}^{0} = \frac{\mu_0}{1+\theta_1 \frac{Q_s}{2C_{ox}} + \theta_2 \left(\frac{Q_s}{2C_{ox}}\right)^2} \tag{2B.38}$$

where μ_0, θ_1 and θ_2 are respectively the low field mobility, and mobility attenuation coefficients of the first and second order, which can be viewed as fitting parameter [114]. The physical interpretation of this mobility attenuation is still under debate [115, 116 and 117] and could find its origin in an enhanced remote coulomb scattering due to charge in the poly-gate [115] or in a significant role of remote interface plasmon–phonon scattering mechanism [117].

2B.4.1.3. Channel length modulation

In order to model the channel length modulation, we need to solve the Poisson equation in the saturation region. It can be written, considering a symmetric undoped double gate nMOS, as:

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial y^2} = -\frac{-q\, n_e(x,y)}{\varepsilon_{si}} \tag{2B.39}$$

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where n_e is the mobile electron charge concentration. We use the following boundary conditions:

The electric field cancels at the middle of the Si film, $y=t_{si}/2$.

$$\left.\frac{d\phi}{dy}\right|_{y=tsi/2} = 0$$

The displacement vector is continuous at the interface, y=0.

$$\varepsilon_{si}\left.\frac{d\phi}{dy}\right|_{y=0} = \varepsilon_{ox}\frac{\phi_S - V_{GS} + \Delta\varphi}{t_{ox}}$$

$\phi_s=\phi(y=0)$ is the potential in Si at the interface and $\Delta\varphi$ is the work function difference between the gate electrode and the intrinsic silicon.

Like in other works, we chose a power law as an approximation for the potential profile along axis y [118-120]. This gives simpler solutions to Poisson equation. However, unlike those works, we are not in threshold conditions here so we chose not to use a parabolic profile, but to consider the exponent as a parameter n whose value will be discussed in the next section.

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$$\phi(x,y) = a + b(x)y + c(x)y^n \qquad (2B.40)$$

The parameters a, b and c are evaluated by applying the boundary conditions, which yields the following potential profile:

$$\phi(x,y) = \phi_S + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_S - V_{GS} + V_{FB}}{t_{ox}}y - \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_S - V_{GS} + V_{FB}}{n \cdot t_{ox}}\left(\frac{2}{t_{si}}\right)^{n-1} y^n \qquad (2B.41)$$

for $y \le t_{si}/2$

$$\phi(x,y) = \phi_S + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_S - V_{GS} + \Delta\varphi}{t_{ox}}(t_{si} - y) - \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_S - V_{GS} + \Delta\varphi}{n \cdot t_{ox}}\left(\frac{2}{t_{si}}\right)^{n-1}(t_{si} - y)^n$$

for $y > t_{si}/2$

One should note that in (2B.40), if n=1 we have a flat profile, while n=2 gives a parabolic profile.

Then integrating (2B.39) over y using (2B.41) gives:

$$\int_0^{tsi} \frac{\partial^2 \phi}{\partial x^2} dy = -\frac{Q_m}{\varepsilon_{si}} + 2\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_S - V_{GS} + V_{FB}}{t_{ox}} \qquad (2B.42)$$

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where Q_m is the mobile charge in the saturated region integrated over the silicon thickness, which is negative for a nMOS.

Evaluating the left-hand side of (2B.42) using (2B.41) gives:

$$\frac{\partial^2 \phi_S}{\partial x^2} = -\frac{Q_m}{\lambda^2 \, 2\varepsilon_{ox}/t_{ox}} + \frac{\phi_S - V_{GS} + \Delta\varphi}{\lambda^2} \qquad (2B.43)$$

where

$$\lambda = \sqrt{\frac{\varepsilon_{si} t_{ox} t_{si}}{2\varepsilon_{ox}} + \frac{t_{si}^{\;2}}{8}\left(1 - \frac{2}{n(n+1)}\right)} = \frac{t_{si}}{2}\sqrt{\frac{1}{2} + \frac{1}{2r} - \frac{1}{n(n+1)}} \qquad (2B.44)$$

λ is a characteristic length that depends only on the device structure and the chosen potential profile. λ can be rewritten in terms of $r=C_{ox}/4C_{si}$, which is a structural parameter more relevant of the physical behavior of the device, C_{ox} and C_{si} being respectively the gate dielectric and the silicon film capacitance.

If we consider that Q_m is constant along the channel, then we can easily solve (2B.43). Indeed (2B.43) becomes

$$\frac{\partial^2 \varphi}{\partial x^2} - \frac{\varphi}{\lambda^2} = 0 \qquad (2B.45)$$

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with $\varphi = \phi_S - V_{GS} + \Delta\varphi - \frac{Q_m}{2C_{ox}}$.

(2B.45) is solved with the following boundary conditions, considering the origin of the x axis at the drain (see Fig. 2B.12):

$$\varphi(x = -\Delta L) = \varphi(\phi_S = V_{deff} + \phi_b) = \varphi_{sat}$$

$$\left.\frac{d\varphi}{dx}\right|_{x=-\Delta L} = \frac{f\, v_{sat}}{\mu}$$

ΔL, v_{sat}, V_{sat} and μ being respectively the length of the saturation region, the saturation velocity, the saturation voltage and the effective mobility. ϕ_b is the surface potential at the source and at threshold condition, such that $\Delta\varphi+\phi_b=V_t$.

Here, f=2 as we are considering nMOSFETs. f=1 for a pMOS. This gives the following solution for φ:

$$\varphi(x) = \varphi_{sat} \cosh\left(\frac{\Delta L + x}{\lambda}\right) + \frac{f\, v_{sat}}{\mu} \lambda \sinh\left(\frac{\Delta L + x}{\lambda}\right) \qquad (2B.46)$$

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ΔL is then obtained from $\varphi_d = \varphi(x=0) = \varphi(\phi_S = V_{DS} + \phi_b)$:

$$\Delta L = \lambda \ln\left(\frac{\varphi_d + \sqrt{\varphi_d^{\,2} - \varphi_{sat}^{\,2} + \left(\frac{f\, v_{sat}}{\mu} \lambda \right)^2}}{\varphi_{sat} + \frac{f\, v_{sat}}{\mu} \lambda} \right) \qquad (2B.47)$$

With

$$\varphi_{sat} = V_{deff} - V_{GS} + V_t - \frac{Q_m}{2C_{ox}} \approx V_{deff} + \frac{Q_s + Q_m}{4C_{ox}} - \frac{Q_m}{2C_{ox}}$$

$$\varphi_d = V_{DS} - V_{GS} + V_t - \frac{Q_m}{2C_{ox}} \approx V_{DS} + \frac{Q_s + Q_m}{4C_{ox}} - \frac{Q_m}{2C_{ox}}$$

These expressions are equivalent to what has been obtained for bulk MOSFETs, differing only by the expressions for the parameters φ_d, φ_{sat} and λ [121]. Here Q_m = -Q(V_{GS}, V_{deff}), as given by equations (2B.6) and (2B.36), and Q_s = -Q(V_{GS},0).It is possible to obtain an expression similar to (2B.47) for the potential in the middle of the Si film. However with this approach, it is necessary to know an expression of the saturation potential in the middle of the film, which is less convenient since the well-known equation (2B.30) that we used here is for the surface potential.

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2B.4.1.4. Early Voltage

The Early voltage is an important parameter as it is related to the gain of the device. We can easily obtain an analytic expression for the Early Voltage with this model. We use the formalism as in [112]:

$$V_E = \frac{I_{DS}}{g_d} = -E_{ld} \cdot \left(L - \Delta L + \frac{\mu}{f v_{sat}} V_{sat} \right) \qquad (2B.48)$$

E_{ld} being the longitudinal electric field at the drain, that we can derive from (2B.46):

$$E_{ld} = -\frac{\varphi_{sat}}{\lambda} \sinh\left(\frac{\Delta L}{\lambda}\right) - \frac{f v_{sat}}{\mu} \cosh\left(\frac{\Delta L}{\lambda}\right) \qquad (2B.49)$$

This relation for V_E has been obtained using the usual approximated relation for the mobility dependence with the longitudinal electric field, that is to say, eq (2B.32).

However, the results have been found to be far better with the non-approximated relation eq (2B.33).

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In that case, a more general expression for V_E can be found:

$$V_E = -\frac{L_e}{\frac{dL_e}{dV_{DS}}} \tag{2B.50}$$

where L_e is given by (2B.35),

$$\frac{dL_e}{dV_{DS}} = -\frac{d\Delta L}{dV_{DS}}\frac{L-\Delta L}{L_e} \text{ and } \frac{d\Delta L}{dV_{DS}} = \frac{\lambda}{\sqrt{\varphi_d^{\,2} - \varphi_{sat}^{\,2} + \left(\frac{f\,v_{sat}}{\mu}\lambda\right)^2}}$$

L_e is an effective gate length due to the effect of velocity saturation [112]. We checked that these relations for V_E are equivalent to the evaluation of the quantity I_{DS}/g_d from the I_{DS}-V_{DS} curves simulated with the same assumptions.

2B.4.1.5. DIBL effect

The DIBL effect can be modeled by solving the Poisson equation in the same way as for the channel length modulation. As the DIBL takes place in weak inversion, and therefore concerns mainly a conduction in the depth of the silicon film, it is more rigorous here to consider the potential at the center ϕ_c, located at $y=t_{si}/2$, similarly to what has been done in [120].

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However, we have to say that we observed nearly no differences by calculating the DIBL from the surface potential. ϕ_c is obtained from (2B.41), as a function of ϕ_s. We then have to replace ϕ_s in (2B.43). We finally obtained the same equation as (2B.45) but the boundaries conditions and the variable φ are different:

$$\varphi(x=0)=\varphi(\phi_c=V_{deff}+V_{bi})=\varphi_d$$

and

$$\varphi(x=-L)=\varphi(\phi_c=0+V_{bi})=\varphi_s \text{ at the source.}$$

V_{bi} being the source and drain junction built-in voltage. As we will see below, we assume here that V_{sat} at the center of the silicon film is approximately the same as the one at the surface.

The variable φ is this time equal to

$$\varphi=\phi_c-V_{GS}+\Delta\varphi-\left(1+\frac{C_{ox}}{2C_{si}}\left(1-\frac{1}{n}\right)\right)\left((Q_s+Q_d)/2\right)\frac{1}{2C_{ox}}$$

Q_s and Q_d being the mobile charge at the source and drain, respectively. We chose here to approximate the mobile charge to the average charge in the channel, because we need a constant

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charge for the integration of (2B.45) along the channel. Then we find the following expression for φ [119]:

$$\varphi(x) = \frac{\varphi_s \sinh\left(\dfrac{L-x}{\lambda_{DIBL}}\right) + \varphi_d \sinh\left(\dfrac{x}{\lambda_{DIBL}}\right)}{\sinh\left(\dfrac{L}{\lambda_{DIBL}}\right)} \tag{2B.51}$$

where λ_{DIBL} is the characteristic length for the DIBL, that is to say (2B.44) with n=2, which correspond to the potential profile usually taken in weak inversion.

The minimal potential for φ is [119]:

$$\varphi_{\min} = 2\sqrt{\varphi_s \varphi_d}\exp\left(\frac{-L}{2\lambda}\right) \tag{2B.52}$$

This quantity, equal to 0 for long channel devices [119], can be considered as the barrier potential drop due to the DIBL effect and must not be confounded with the surface potential which is taken into account in the V_t parameter in the CLM section. It is then introduced into the calculation of the charge Q in (2B.6)-(2B.10) by replacing V_{GS} with $V_{GS}+\phi_{min}$, for example.

However, the previous analysis fails in strong inversion, where ϕ_{min} appeared to be too large. To ensure that ϕ_{min} tends to zero

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well in strong inversion [122] and to have the correct behaviour for the reduction of DIBL above threshold, we multiplied the barrier lowering ϕ_{min} by a fitting parameter F_{DIBL} whose value change progressively from 1 to 0 when going from weak to strong inversion. We propose the following expression:

$$F_{DIBL} = \exp\left(-\left(\frac{Q_{ch}}{2\sigma_{DIBL} C_{ox} \beta} \right)^{n_{DIBL}} \right) \tag{2B.53}$$

The transition begins when $Q_{ch} = (Q_s+Q_d)/2$ is superior to $2C_{ox}\beta$, which corresponds approximately to the threshold voltage, and can be adjusted with the parameters n_{DIBL} and σ_{DIBL}. nDIBL defines the abruptness, while σ_{DIBL} defines the threshold of the transition.

2B.4.2.Simulation Results

Usually, around the threshold voltage, the value of the n parameter is taken as 2 in the gradual channel approximation (GCA) region, i.e. a parabolic potential profile. However this is not true in this case in the saturation region. In fact, ATLAS simulations give a somewhat parabolic profile in the GCA region that becomes flat near the boundary between the

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saturated region and the GCA region. This flat potential profile corresponds to n=1. In the saturated region, ATLAS gives a potential profile that presents a very small curvature that can be fitted with an n value slightly inferior to 1, that depends on the device geometry.

Therefore, it is important to note that in this model, we consider two different constant values of n for the GCA and saturated region, respectively. For the evaluation of the channel length modulation, we assume that n=1 in the saturated region is a good approximation for the devices considered here. Furthermore, we observed that the value of n has little influence on the channel length modulation. However, for the DIBL calculation, i.e in the expressions of ϕ_s, ϕ_d and λ_{DIBL}, the value of n is taken as 2, because DIBL mainly occurs in weak inversion. Anyway, a model for an undoped transistor can be applied to a lightly doped one by adjusting the value of the flat band voltage [123].

Parameter F_{DIBL} acts as a fitting parameter for moderate inversion and cancels the DIBL in strong inversion. The dependence on V_{GS} and V_{DS} is included in the channel mobile charge Q_{ch}. The dependence on L, however is not taken into account, but it can be neglected if short channel effects are not too strong. The optimal values for σ_{DIBL} and n_{DIBL} were found to be between 1 and 10, and 1, respectively.

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The model is for undoped devices, but a channel doping of $10^{15}cm^{-3}$ was used for the simulations. The simulated device is represented in Fig 2B.12. The doping of the source and drain region is $6x10^{20}cm^{-3}$. The gate and source workfunctions are 4.73 and 4.1eV, respectively.

Fig. 2B.13 and Fig. 2B.14 represent the length of the saturation region, as given by the model. The effective mobility dependence on V_{GS} and on dopant concentration has been extracted from ATLAS simulations with the same parameters. The overall qualitative behavior of the model seems to be good as the length of the saturated region ΔL increases with V_{DS} and decreases with V_{GS}, as we can see in Fig. 2B.13, but we noticed that the V_{GS} dependence of ΔL is mainly driven by the V_{GS} dependence of the mobility. In Fig. 2B.13, we can also note that ΔL was found to be approximately half of the channel length at an operated voltage of 1V for L=50nm, t_{si}=30nm and t_{ox}=2nm. This indicates that the length of the saturated region will become an even more important parameter for deeply scaled MOSFETs. In Fig. 2B.13 we can note that ΔL can be reduced using a thinner silicon film, by approximately the same amount on both gate lengths. ΔL is also found reduced for thinner gate oxides (see Fig. 2B.14). Finally, the dependence on the channel length was found to be weak.

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Concerning the calculation of the DIBL, the exact value of V_{bi} is difficult to determine in a double gate MOSFET because the silicon film is floating. Therefore, V_{bi} was taken as a fitting parameter for the DIBL, and was found close to 0V. In Fig. 2B.15, we present a fitting of the I_{DS}-V_{DS} and I_{DS}-V_{GS} curves given by ATLAS simulations. In order to reduce the number of fitting parameters and facilitate the comparison with ATLAS, we chose a constant mobility with V_{GS} in the simulations of Fig. 2B.15, but we used in the model the mobility extracted from ATLAS curves. We can see that the overall agreement for the current is very good, especially for the DIBL, which gave the correct qualitative and quantitative behavior below the threshold, without the use of any fitting parameters. The correct quantitative behavior was obtained with the right V_{bi}.= 0.57V. Concerning the dynamic conductance g_d, the agreement between ATLAS and the model is reasonably good below 1.5V in Fig. 2B.15c. Beyond 1.5V, the model overestimates the slope of g_d, but nanoscale DG MOSFETs are not supposed to work in the high V_{GS} regime. This is due to the fact that the model seems to underestimate slightly the channel length modulation when short channel effects are very strong. The short channel model is further verified in Fig 2B.16, which shows excellent agreement with ATLAS when the channel length is varied, illustrating the accuracy of the DIBL modeling.

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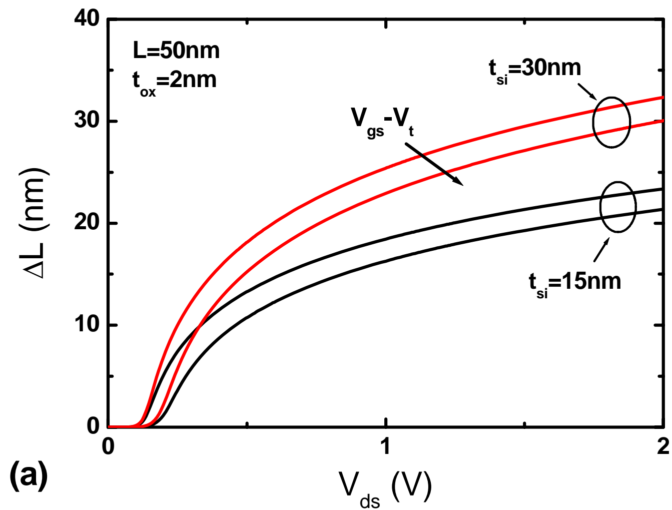

Fig.2B.13a *Plots of $\Delta L(V_{DS})$ for two different values of the silicon thickness t_{si}, with V_{GS}-V_t=0.25 and 0.5V. a) for L = 50nm, b) for L = 120nm.*

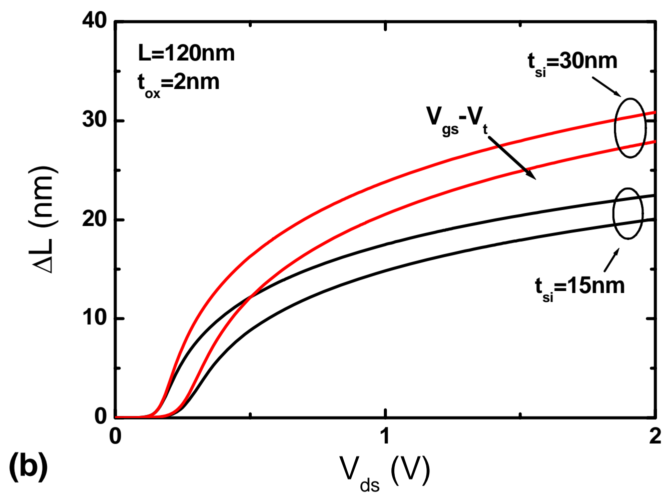

Fig. 2B.13b: *Plots of $\Delta L(V_{DS})$ for two different values of the silicon thickness t_{si}, with V_{GS}-V_t=0.25 and 0.5V. a) for L = 50nm, b) for L = 120nm.*

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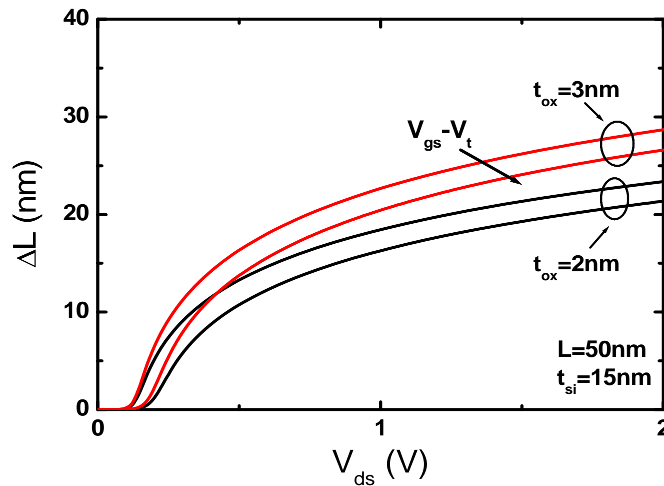

Fig.2B.14 *Plots of $\Delta L(V_{DS})$ for two different values of the gate oxide thickness t_{ox}, with V_{GS}-V_t=0.25 and 0.5V*

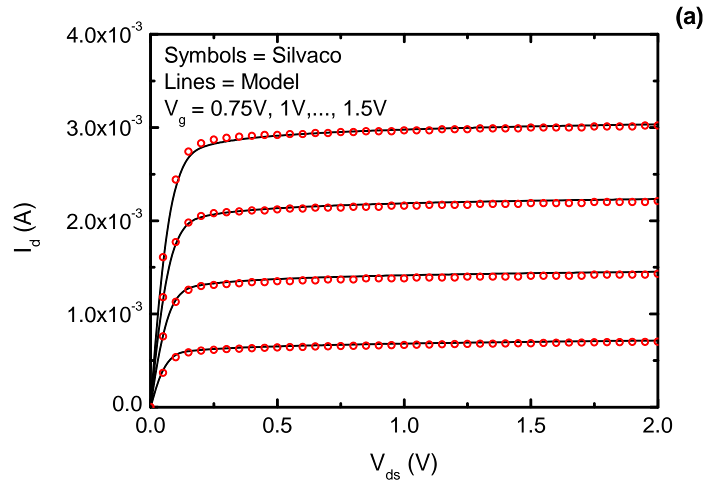

Fig.2B.15a *Comparison of the model with Silvaco simulations, for a DGMOS with t_{ox}=2nm, t_{si}=15nm and L=50nm.*

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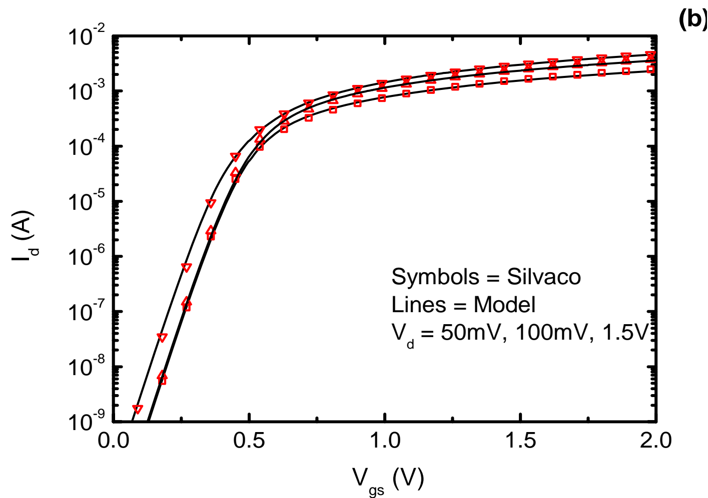

Fig. 2B.15b: *Comparison of the model with Silvaco simulations, for a DGMOS with t_{ox}=2nm, t_{si}=15nm and L=50nm.*

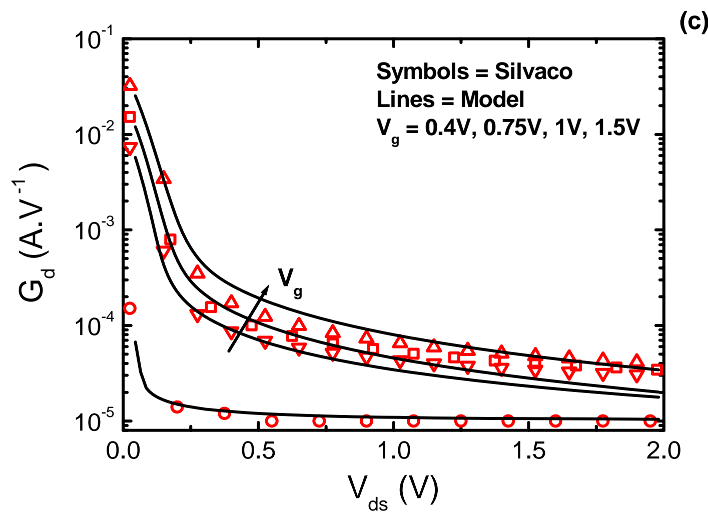

Fig. 2B.15c: *Comparison of the model with Silvaco simulations, for a DG-MOSFET with t_{ox}=2nm, t_{si}=15nm and L=50nm.*

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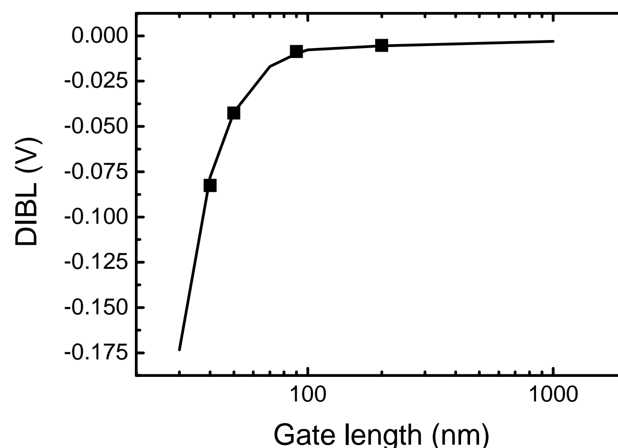

Fig.2B.16 *DIBL defined in weak inversion as the V_{GS} offset between I_{DS}@V_{DS}=1V and I_{DS}@V_{DS}=50mV, as given by the model (lines) and ATLAS simulations (symbols). t_{si}=15nm, t_{ox}=2nm.*

One of the main advantages of this model is that the short channel effects have been added in a "piecewise" manner to the long channel model, thus allowing easy future improvement and customization of each of its parts. As a result, it could, as well, be used as an improvement to other long channel models of other multiple-gate MOS structures.

This DC model can also be the basis to incorporate short-channel effects to the charge and capacitance model developed for DG MOSFETs.

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2C. Compact model for undoped Ultra-Thin-Body (UTB) SOI MOSETs

In this section

an analytic, explicit and continuous charge model for a long-channel UTB (Ultra-Thin-Body) SOI (Silicon-on-Insulator) MOSFET is presented. From this charge model analytical expressions of the total capacitances are obtained. Our model is valid from below to well above threshold, without suffering from discontinuities between the regimes. It is based on a unified-charge-control-model derived from Poisson's equation. The drain current, charge and capacitances expressions result in continuous explicit functions of the applied bias. The calculated capacitance characteristics are validated by 2-D numerical simulations showing a very good agreement for different silicon film thicknesse. [124.]

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2C.1. Introduction

As the traditional CMOS is fast approaching the limit of the bulk technology scaling, non-classical CMOS devices such as ultra-thin body silicon-on-insulator (UTB SOI), double-gate devices and surrounding-gate (SRG) structure provide a path to scale CMOS to the end of the Roadmap using new transistor structural designs and new materials [25]. The advantage of UTB design is that in contrast to other emerging device concepts, UTB SOI technology combines a planar transistor configuration with a superior sub-threshold slope resulting from a thin Si film thickness of 5–40 nm [125]. However, quantum-mechanical effects become remarkable below the critical thickness of the Si film (which is equal to 10nm [99]) and raise the threshold voltage with decreasing the Si thickness. So, when using a Si film thinner than 10 nm the quantum effects should be taken into consideration in modeling the behavior of the device. In order to benchmark the circuit performance and optimize the layout of UTB SOI devices, there is a strong demand for a physics-based compact model that can be implemented into the existing circuit simulators. In this section, based on a previous work done by A.S. Roy et.al [126] where a channel current model, written in terms of the charge densities at the source and drain ends, was developed for an asymmetric undoped DG MOSFET, we present an analytical charge and capacitance

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model obtained from a unified charge control model derived in [126] from the 1-D Poisson equation in the direction perpendicular to the channel, for the case when one interface is in weak inversion, which actually corresponds to the practical regime of operation of UTB SOI MOSFET. This case will be simulated by a DG MOSFET, having a grounded back-gate voltage (V_{GB}) and a variable front-gate voltage. This functioning is identical with the one of an UTB SOI MOSFET.

In this section, we have assumed, as in [126] that both oxides have the same thickness, although an extension to the case for two different oxide thicknesses can be done by solving iteratively the charge control model obtained in this case.

Also, we use a Si film thicker than 10 nm, so it is safe to assume that quantum mechanical effects are not important for our device.

The charge and capacitance expressions are written in terms of explicit and infinitely continuous expressions of the applied bias. It is shown that this analytic model covers very well all regimes of MOSFET operations: from linear to saturation and from sub-threshold to strong inversion without the need of empirical parameters. The capacitance characteristics have been validated by 2-D numerical simulations (with DESSIS-ISE). In addition, to demonstrate the accuracy of this model, results for

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two different silicon film thicknesses are presented. Due to all these advantages, this model has the potential to be very successfully used in circuit simulators for the design of integrated circuits using long-channel UTB SOI models.

2C.2 Model

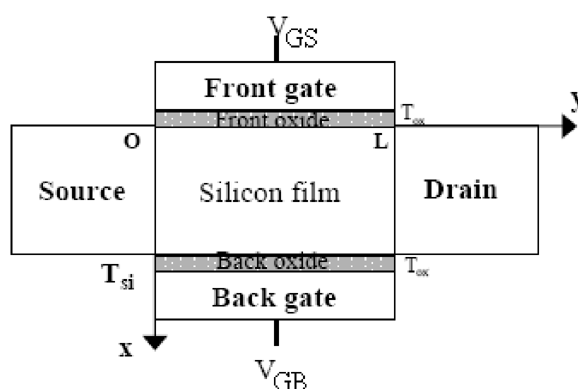

Fig.2C.1 *Schematic of the asymmetric DG MOSFET used in this section*

As in the study of [126], we consider the case of an undoped channel, with N-type source and drain contacts and ignoring holes in the charge neutrality equation, the electrostatics can be described by Poisson equation, in the direction vertical to the channel, the x-direction from Fig. 2C.1.

$$\frac{d^2\phi}{dx^2} = \frac{qn_i}{\varepsilon_{Si}} e^{\frac{q\phi}{kT}} \tag{2C.1}$$

q being the electronic charge, n_i the intrinsic carrier concentration, ε_{Si} the permittivity of silicon and Φ the potential.

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Assuming the front and back oxide thicknesses are the same, by solving (2C.1) with the appropriate boundary conditions, for the case when one interface is in weak inversion the following implicit unified charge control model is obtained [126] (Q represents the mobile charge sheet density per unit area):

$$\begin{aligned}
&\frac{1}{1+\alpha_1}V_{GS}+\frac{\alpha_1}{1+\alpha_1}V_{GB}-V-\frac{1}{1+\alpha_1}V_{FB1}-\frac{\alpha_1}{1+\alpha_1}V_{FB2}-\\
&-\frac{kT}{q}\log\left[\frac{1}{2}\cdot\left(\frac{4C_{Si}\left(V_{GS}-V_{GB}+V_{FB2}-V_{FB1}\right)}{C_{ox}\frac{kT}{q}}\right)^2\right]-\\
&-\frac{kT}{q}\log\left(\frac{1-\alpha_1}{1+\alpha_1}\right)+\frac{kT}{q}\log(2a^2)=\frac{Q}{C_{ox}\left(1+\alpha_1\right)}+\frac{kT}{q}\log\left(\frac{Q}{Q_0}\right)+\frac{kT}{q}\log\left(\frac{2Q}{Q_0}+1\right)
\end{aligned} \quad (2C.2)$$

where $\alpha_1=\frac{C_{Si}}{C_{Si}+C_{ox}}$, $C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}$ and $C_{Si}=\frac{\varepsilon_{Si}}{t_{Si}}$ V_{FB1} is the work function difference between the front gate electrode and the intrinsic silicon, V_{FB2} is the work function difference between the back gate electrode and the intrinsic silicon. (we consider $V_{FB1}= V_{FB2}$), V is the electron quasi-Fermi potential ; $Q_0=4C_{Si}\left(V_{GS}+V_{FB2}-V_{FB1}\right)$ and $a=\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\frac{t_{ox}}{L_{D2}}$; $L_{D2}=\sqrt{\frac{kT\varepsilon_{Si}}{q^2 n_i}}$ [126]. L_{D2} is in fact equal to $\frac{L_{Di}}{\sqrt{2}}$ and L_{Di} represents the intrinsic Debye length.

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2C.2.1. Explicit Drain-Current Model

The drain-current is calculated as [126]:

$$I_{DS} = \frac{W\mu}{L}\int_{0}^{V_{DS}} Q(V)dV \qquad (2C.3)$$

where μ is the effective mobility of the electrons, W is the width of the device and L is the channel length.

From (2C.2) we obtain:

$$dV = -\frac{dQ}{C_{ox}\left(1+\alpha_1\right)} - \frac{kT}{q}\left(\frac{dQ}{Q} + 2\frac{dQ}{2Q+Q_0}\right) \qquad (2C.4)$$

Integrating (2C.3) using (2C.4) between Q_s and Q_d ($Q=Q_s$ at source end and $Q= Q_d$), we obtain an expression of I_{DS} in terms of carrier charge densities:

$$I_{DS} = \frac{W\mu}{L}\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2C_{ox}(1+\alpha_1)} - \frac{1}{2}\frac{kT}{q}Q_0 \log\left[\frac{2Q_s + Q_0}{2Q_d + Q_0}\right]\right] \qquad (2C.5)$$

In order to compute the charge densities from an explicit expression of the applied bias, since equation (2C.2) does not yield a closed form expression for Q, we propose an approximate explicit expression, which was demonstrated to be

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a very good solution for an equation of the type of (2C.2). [94], [84]. This expression, (2C.6), is similar to the expression used for the double-gate MOSFETs in [94] and for surrounding gate MOSFETs in [84] and where the charge control model results to have a similar form as for undoped UTB SOI MOSFET from equation (2C.2). This expression tends to the desired limits below and above threshold (see [84] for details). So, we can use an explicit expression for Q of the same type, adapted to our device:

$$Q = C_{ox}(1+\alpha_1)\left(-\frac{2C_{ox}\beta^2}{Q_0}+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_0}\right)^2+4\beta^2\log^2\left[1+\exp\left[\frac{V_{GS}-V_T+\Delta V_T-V}{2\beta}\right]\right]}\right) \quad (2C.6)$$

where $\beta=\frac{kT}{q}$. V_T is defined as:

$$V_T = V_0+\beta\log\left(1+\frac{2Q'}{Q_0}\right)+\beta\log\left(1+\frac{Q'}{Q_0}\right) \quad (2C.7)$$

where Q’ is calculated as:

$$Q' = C_{ox}(1+\alpha_1)\left(-\frac{2C_{ox}\beta^2}{Q_0}+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_0}\right)^2+4\beta^2\log^2\left[1+\exp\left[\frac{V_{GS}-V_0-V}{2\beta}\right]\right]}\right) \quad (2C.8)$$

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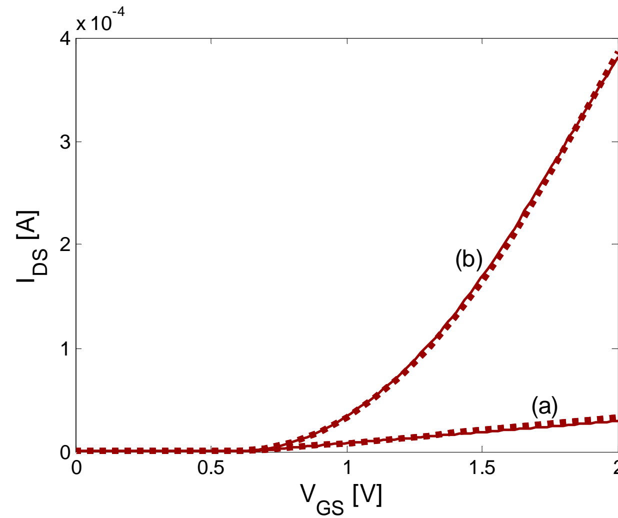
$$V_0 = \frac{V_{FB1}+V_{FB2}}{2} + \frac{kT}{q}\log\left[\frac{1}{2}\cdot\left(\frac{4C_{Si}\left(V_{GS}+V_{FB2}-V_{FB1}\right)}{C_{ox}\frac{kT}{q}}\right)^2\right] + \frac{kT}{q}\log\left(\frac{1-\alpha_1}{1+\alpha_1}\right) - \frac{kT}{q}\log(2a^2) \quad (2C.9)$$

In (2C.6), the term ΔV_T ensures the correct behaviour of Q above threshold [94]:

$$\Delta V_T = \frac{\left(\frac{2C_{ox}\beta^2}{Q_0}\right)Q'}{Q_0 + Q'} \quad (2C.10)$$

Therefore Q_s and Q_d in the I_{DS} expression (2C.5) are analytically computed by applying V=0 and V=V_{DS} respectively, in (2C.6)-(2C.10).



(a)

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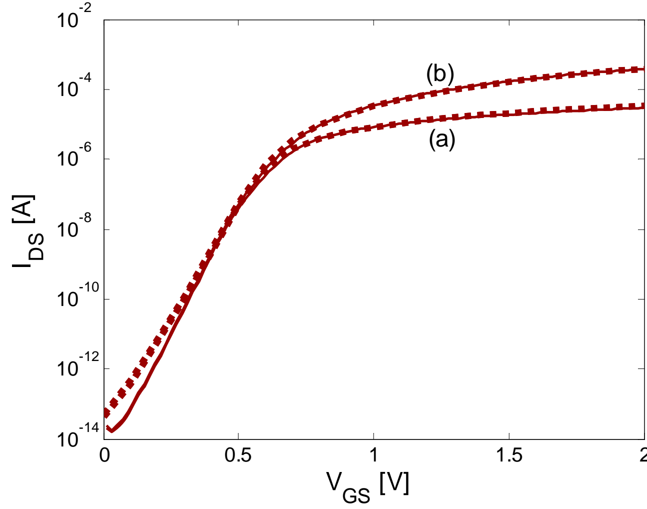

(b)

Fig.2C.2 *Transfer characteristics, for V_{DS}=0.05V (a) and for V_{DS}=1V (b) in linear scale for t_{Si}=31nm (Fig.2C.2.a). Transfer characteristics, for V_{DS}=0.05V (a) and for V_{DS}=1V (b) in logarithmic scale for t_{Si}=31nm (Fig.2C.2.b). Solid line: analytical model; Symbol line: DESSI-ISE simulation*

2C.2.2. Charge and Capacitance Model

The total channel charge is obtained by integrating the mobile charge sheet density over the channel length:

$$Q_{Tot} = W\int_0^L Q dx = -W^2 \frac{\mu}{I_{DS}} \int_0^{V_{DS}} Q^2 dV \qquad (2C.11)$$

Using (2C.4) in (2C.11) we get:

$$Q_{Tot} = -W^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left(\frac{Q^2}{C_{ox}(1+\alpha_1)} + \frac{kT}{q}\left(Q + \frac{2Q^2}{2Q+Q_0} \right) \right) dQ \qquad (2C.12)$$

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The resulting expression of Q_{Tot} is given in the Appendix.

The total gate charge is obtained as $Q_G=-Q_{Tot}-Q_{ox}$, where Q_{ox} is the total oxide fixed charge at the oxide/silicon interface. The total front gate charge is from [126]:

$$Q_F = \frac{Q_G}{1+\alpha_1} + \frac{W}{1+\alpha_1} 2\alpha_1 \cdot V_{GS} L \qquad (2C.13)$$

The total back gate charge is calculated as:

$$Q_B = Q_G - Q_F \qquad (2C.14)$$

Following the Ward's channel charge partitioning scheme [70], and using (2C.4) we obtain analytical expressions for the total drain (Q_D) and source (Q_S) charges:

$$Q_D = W\int_0^L \frac{x}{L} Q dx = -\frac{W^3\mu^2}{L(I_{DS})^2}\int_{Q_s}^{Q_d} Q^2 \left(\begin{aligned} &\left(\frac{Q^2-Q_s^2}{2C_{ox}(1+\alpha_1)}\right)+ \\ &+\frac{kT}{q}\left(2(Q-Q_s)-\frac{1}{2}Q_0 \log\left[\frac{2Q+Q_0}{2Q_s+Q_0}\right]\right) \end{aligned} \right) \cdot \qquad (2C.15)$$

$$\cdot \left(\frac{1}{C_{ox}(1+\alpha_1)} + \frac{kT}{q}\left(\frac{1}{Q}+\frac{2}{2Q+Q_0}\right)\right) dQ$$

$$Q_S = Q_{Tot} - Q_D \qquad (2C.16)$$

(The solution for Eq.(2C.16) is given in Appendix)

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The non-reciprocal intrinsic capacitances are obtained by differentiating the total charge expressions with respect to the applied voltages as:

$$C_{ij} = \chi_{ij} \frac{dQ_i}{dV_j} \tag{2C.17}$$

where *i*,*j*=*g* (front gate),*b* (back gate),*d*,*s* and $\chi_{ij} = 1$ if $i = j$ and $\chi_{ij} = -1$ if $i \neq j$.

By differentiating the total charge expressions as in [94], analytical expressions of all these capacitances are obtained in terms of the mobile charge sheet densities at the source and drain ends. These expressions become explicit by using the charge formula in (2C.6)-(2C.10) to calculate the mobile charge sheet densities at source and drain. Therefore, analytical and explicit expressions of all front gate capacitances have been obtained.

It has to be remarked that, due to charge conservation, only nine out of the sixteen possible capacitances are independent. The other seven capacitances can be calculated from the nine independent capacitances using equations derived from the charge conservation equation.

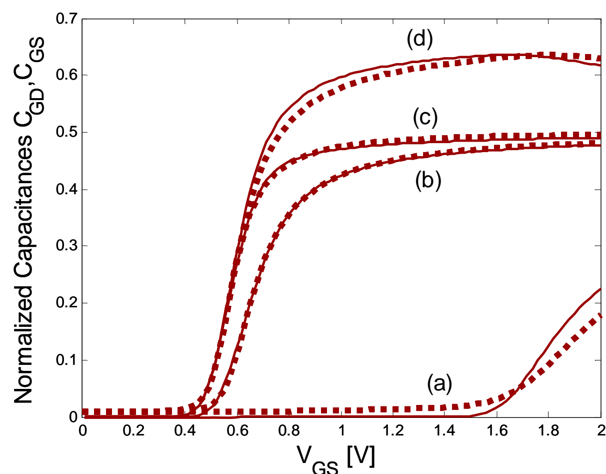

Fig.2C.3 *Normalized gate-to-drain capacitance (a, b) and gate-to-source capacitance (c, d) with respect to the gate voltage, for* V_{DS}*=0.05V (b,c) and* V_{DS}*=1V (a,d);* t_{si}*=31nm. Solid line: analytical model; Symbol line: DESSIS-ISE simulation*

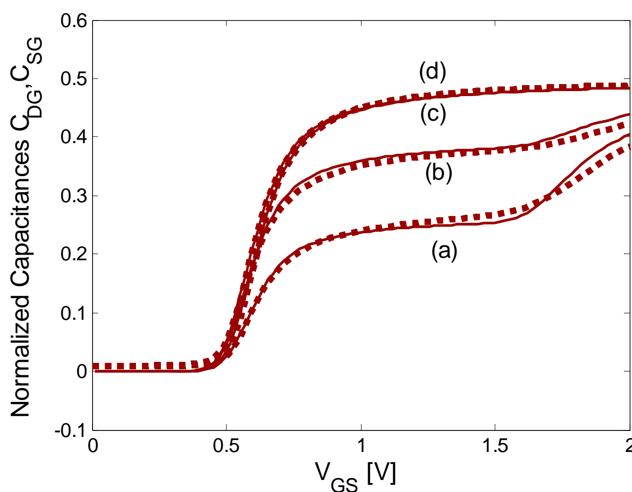

Fig.2C.4 *Normalized drain-to-gate capacitance (a, c) and source-to-gate capacitance (b, d) with respect to the gate voltage, for* V_{DS}*=1V (a, b) and* V_{DS}*=0.05V (c, d);* t_{si}*=31nm Solid line: analytical model; Symbol line: DESSIS-ISE simulation*

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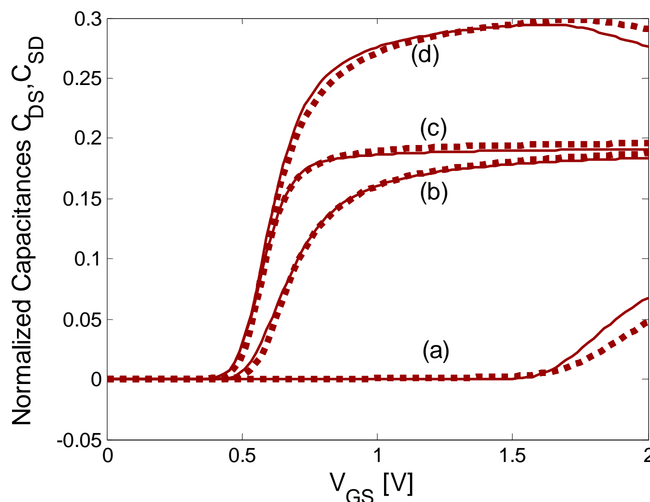

Fig.2C.5 *Normalized source-to-drain capacitance (a, b) and drain-to-source capacitance (c, d) with respect to the gate voltage, for V_{DS}=1V (a, d) and V_{DS}=0.05V (b, c); t_{si}=31nm. Solid line: analytical model; Symbol line: DESSIS-ISE simulations*

2C.3. Simulation Results

To validate this model, we have compared the modeled capacitance characteristics with 2D numerical simulations using DESSIS-ISE [104]. We have simulated a DG MOSFET, having a grounded back-gate voltage (V_{GB}) and a variable front-gate voltage (V_{GS}). We have assumed a device with channel length L=1µm, a device width of W=1 µm, a silicon oxide thickness t_{ox}=2 nm (the same for top and back gate) and two silicon film thickness t_{Si}=31 nm and t_{Si}=20nm.

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Figures 2C.2-2C.5 present the results for the case when the silicon film thickness equals 31nm and Figures 2C.6-2C.8, for the case when the silicon film thickness equals 20nm. Fig. 2C.2 shows the comparison between the modeled (using the explicit expressions) and numerically simulated transfer characteristics. As expected, the agreement between them is very good. Also the model shows a smooth transition between all the operation regimes (linear, saturation and subthreshold) without fitting parameters. An excellent agreement is also observed between the modeled and numerically simulated values of C_{gd}, C_{gs} ,$C_{dg,}$ C_{sg}, C_{ds} and C_{sd} (Fig 2C.3-2C.5), as functions of the gate voltage, for different values of the drain-source voltage (0.05V and 1V). In these figures all the capacitances are presented in the normalized form, as $C/WC_{ox}L$, where C represents the capacitances C_{gd}, C_{gs} ,$C_{dg,}$ C_{sg}, C_{ds} and $C_{sd.}$

Also, an excellent agreement is observed for the capacitances C_{gd}, C_{gs} ,$C_{dg,}$ $C_{sg,}$$C_{ds}$ and C_{sd}, for all V_{DS} biases, when taking into consideration t_{Si}=20nm. (Fig. 2C.6-2C.8).

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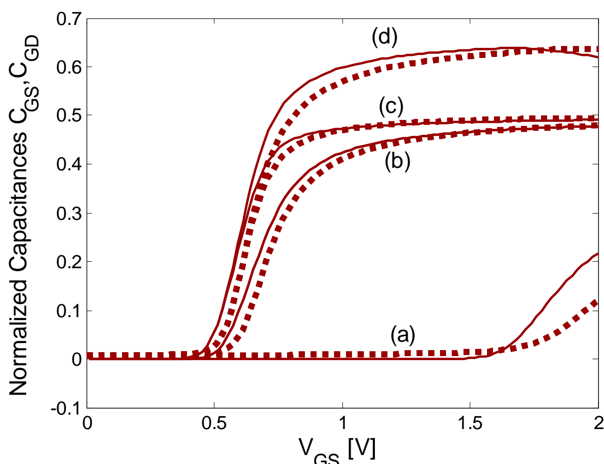

Fig.2C.6 *Normalized gate-to-drain capacitance (a, b) and gate-to-source capacitance (c, d) with respect to the gate voltage, for* V_{DS}*=0.05V (b,c) and* V_{DS}*=1V (a,d);* t_{si}*=20nm. Solid line: analytical model; Symbol line: DESSIS-ISE simulation*

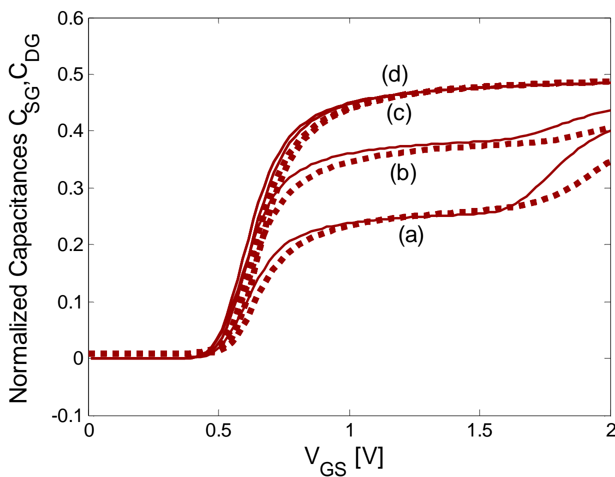

Fig.2C.7 *Normalized drain-to-gate capacitance (a, c) and source-to-gate capacitance (b, d) with respect to the gate voltage, for* V_{DS}*=1V(a, b) and* V_{DS}*=0.05V (c, d);* t_{si}*=20nm. Solid line: analytical model; Symbol line: DESSIS-ISE simulation*

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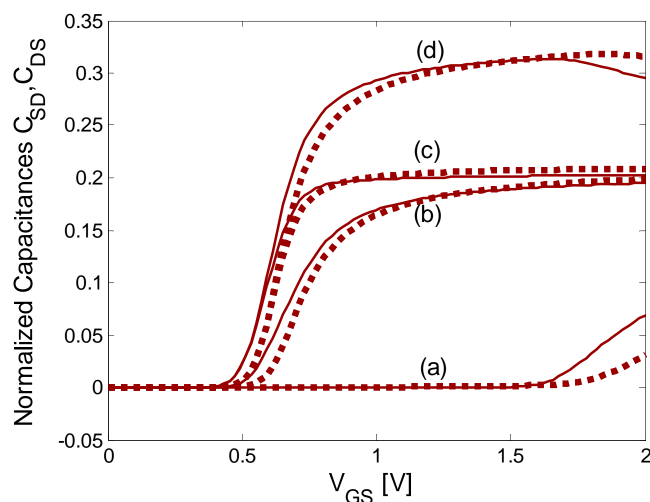

Fig.2C.8 *Normalized source-to-drain capacitance (a, b) and drain-to-source capacitance (c, d) with respect to the gate voltage, for V_{DS}=1V (a, d) and V_{DS}=0.05V (b, c); t_{si}=20nm. Solid line: analytical model; Symbol line: DESSIS-ISE simulations*

In conclusion the modeled capacitances show excellent agreement with the 2D numerical simulations, in all operating regimes, for all V_{DS} biases and for different silicon film thicknesses, proving the accuracy of this model. Therefore, the model is very promising for being used in circuit simulators.

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2D. Compact model for undoped cylindrical Surrounding-Gate MOSFETs

In this section

an analytical and continuous charge model for cylindrical undoped surrounding gate (SGT) MOSFETs is developed, from which analytical expressions of all total capacitances are obtained [69]. The model is based on a unified charge control model derived from Poisson's equation. The drain current, charge and capacitances are written as continuous explicit functions of the applied voltages. To validate the model, we have compared the capacitance modeled characteristics with 3D numerical simulations using the DESSIS-ISE simulator. Also, the drain current model has been introduced in AGILENT ADS (Advanced Design System) circuit simulator with very good results.

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2D.1. Introduction

The surrounding gate (SGT) MOSFET is one of the most promising candidates for the downscaling of CMOS technology toward the nanometre channel length range, since the surrounding gate architecture allows an excellent control of the channel charge in the silicon film, reducing short channel effects [35,127-130]. Due to the better electrostatic control, short-channel effects are even smaller in SGT MOSFETs than in DG MOSFET [129,130].

Compact models for SGT MOSFETs, adequate for circuit simulators, are necessary for the future use of these devices in integrated circuits. Circuit design requires a complete small-signal model, which consists of analytical expressions of the transconductance and conductance (derived from a drain current expression) and also of the total capacitances.

In a previous work [84], a channel current model, written in terms of the charge densities at the source and drain ends, was developed from a unified charge control model derived from the solution of the 1D Poisson's equation. In this section, we present the development of analytical charge and capacitance models obtained from the unified charge control model. This results in a

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complete charge-based small-signal model. The charge and capacitance expressions are written in terms of explicit and infinitely continuous expressions of the applied bias, which are valid and continuous through all operating regimes. A very good agreement is observed for all the capacitance expressions compared to the 3D device numerical simulations. Another very important advantage of this model is the absence of empirical parameters. Therefore, this model has the potential to be very successfully used in circuit simulators for the design of integrated circuits using SGT MOSFET models.

2D.2. Model

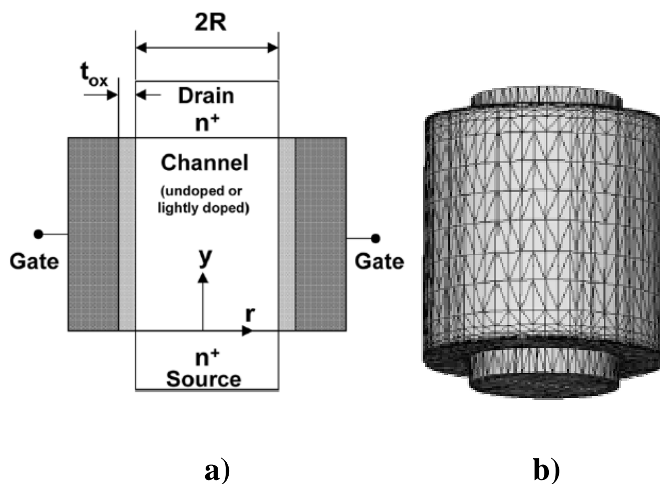

Fig.2D.1 *a) Cross section of the surrounding gate MOSFET b) Simulated surrounding gate MOSFET structure*

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As in [35,84] we consider a SGT MOSFET in which the electrostatic control by the surrounding gate is good enough to neglect the short-channel effects associated to 2D effects (gradual channel approximation). Therefore, the electrostatic behaviour of the device is described by the 1D Poisson's equation in the radial direction.

In an undoped (lightly doped) cylindrical n-type SGT-MOSFET (Fig.2D.1) Poisson's equation takes the following form:

$$\frac{d^2\phi}{dr^2}+\frac{1}{r}\frac{d\phi}{dr}=\frac{kT}{q}\delta\cdot e^{\frac{q(\phi-V)}{kT}} \qquad \text{(2D.1)}$$

where $\delta = q^2 n_i / kT\varepsilon_{Si}$, q being the electronic charge, n_i the intrinsic carrier concentration, ε_{Si} the permittivity of silicon, $\phi(r)$ the electrostatic potential and V the electron quasi-Fermi potential. It has been assumed that the hole density is negligible compared with the electron density [35, 84].

By solving (2D.1) with the appropriate boundary conditions, the following unified charge control model is obtained [84] (Q represents the mobile charge sheet density per unit area):

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$$(V_{GS}-\Delta\varphi-V)-\frac{kT}{q}\log\left(\frac{8}{\delta\cdot R^2}\right)=\frac{Q}{C_{ox}}+\frac{kT}{q}\log\left(\frac{Q}{Q_0}\right)+\frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right) \quad (2D.2)$$

where Δφ is the work function difference between the gate electrode and the intrinsic silicon, R is the radius of the surrounding gate, C_{ox} is the oxide capacitance and $Q_0=\left(\frac{4\varepsilon_{Si}}{R}\right)\cdot\left(\frac{kT}{q}\right)$.

2D.2.1 Drain Current Model

The drain current in a SGT MOSFET is calculated as [84]:

$$I_{DS}=\frac{2\pi R\mu}{L}\int_0^{V_{DS}}Q(V)\,dV \quad (2D.3)$$

μ is the effective mobility of the electrons and L the channel length.

From (2D.2) we obtain:

$$dV=-\frac{dQ}{C_{ox}}-\frac{kT}{q}\left(\frac{dQ}{Q}+\frac{dQ}{Q+Q_0}\right) \quad (2D.4)$$

Integrating (2D.3) using (2D.4), between Q_s and Q_d ($Q=Q_s$ at source end and $Q=Q_d$ at the drain end), we obtain an expression

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of I_{DS} in terms of carrier charge densities [84]:

$$I_{DS} = \frac{2\pi R\mu}{L}\left[2\frac{kT}{q}\left(Q_s - Q_d\right) + \frac{Q_s^2 - Q_d^2}{2C_{ox}} + \frac{kT}{q}Q_0 \log\left[\frac{Q_d + Q_0}{Q_s + Q_0}\right]\right] \quad (2D.5)$$

In order to compute the charge densities from an explicit expression of the applied bias, since (2D.2) does not yield a closed form for Q, we use the explicit analytical equation for the charge sheet density as in [84]. Therefore Q_s and Q_d in the I_{DS} expression (2D.5) are analytically computed.

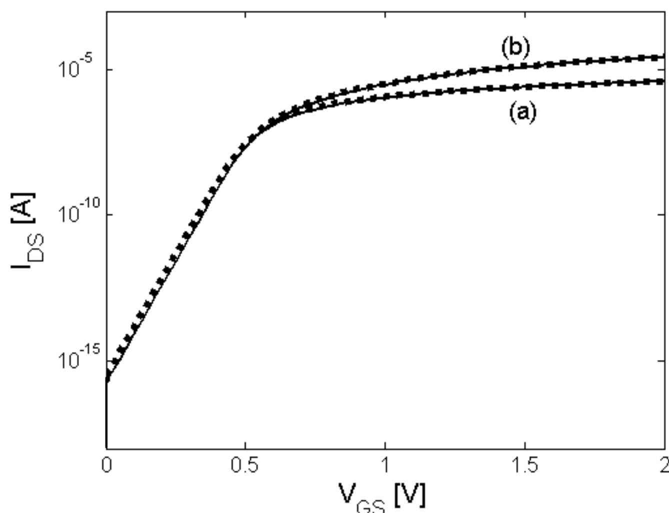

Fig.2D.2 *Transfer characteristics, for V_{DS}=0.1V (a) and for V_{DS}=1V (b) in logarithmic scale. Solid line: DESSIS-ISE simulation; Symbol line: analytical model using (2D.5)*

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2D.2.2 Charge and Capacitance Model

The total inversion charge is obtained by integrating the mobile charge sheet density over the channel length:

$$Q_{Tot} = -2\pi R \int_0^L Q dx = -(2\pi R)^2 \frac{\mu}{I_{DS}} \int_0^{V_{DS}} Q^2 dV \qquad (2D.6)$$

Using (2D.4) in (2D.11) we get:

$$Q_{Tot} = (2\pi R)^2 \frac{\mu}{I_{DS}} \int_{Q_s}^{Q_d} \left(\frac{Q^2}{C_{ox}} + \frac{kT}{q} Q + \frac{kT}{q} \frac{Q^2}{Q+Q_0} \right) dQ \qquad (2D.7)$$

The resulting expression of Q_{Tot} is given in the Appendix .

The total gate charge is given by Q_G=-Q_{Tot}-Q_{ox}, where Q_{ox} is the total oxide fixed charge at the oxide/silicon interface. The intrinsic capacitances, C_{gd} and C_{gs}, are obtained as [87]:

$$C_{gi} = -\frac{dQ_G}{dVi} \qquad (2D.8)$$

where *i=d,s*

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We obtain these capacitances, by differentiating Q_{Tot} according to (2D.4). Both Q_{Tot}, C_{gd} and C_{gs} are written in terms of the mobile charge sheet densities at the source and drain ends. Using the explicit formula in [84] for the mobile charge sheet densities at source and drain, the expressions of Q_{Tot}, C_{gd} and C_{gs} become explicit.

Following the Ward's channel charge partitioning scheme [70], and using (2D.4) we obtain analytical expressions for the total drain (Q_D) and source (Q_S) charges:

$$Q_D = -2\pi R\int_0^L \frac{x}{L} Q dx = \frac{(2\pi R)^3 \mu^2}{L(I_{DS})^2} \int_{Q_s}^{Q_d} Q^2 \left(\begin{array}{l} \left(\dfrac{Q^2 - Q_s{}^2}{2C_{ox}} \right) + \\ + \dfrac{kT}{q}\left(2(Q - Q_s) - Q_0 \log\left[\dfrac{Q + Q_0}{Q_s + Q_0} \right] \right) \end{array} \right) \cdot \left(\frac{1}{C_{ox}} + \frac{kT}{q}\left(\frac{1}{Q} + \frac{1}{Q + Q_0} \right) \right) dQ \quad (2D.9)$$

$$Q_S = Q_{Tot} - Q_D \quad (2D.10)$$

(The solutions for Eq.(2D.9) and Eq.(2D.10) are given in Appendix). The non-reciprocal capacitances C_{dg} and C_{sg} are obtained as [87]:

$$C_{ig} = -\frac{dQ_i}{dV_G} \quad (2D.11)$$

where $i=d,s$

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The capacitances C_{sd} and C_{ds} are computed as follows [87]:

$$C_{ds} = -\frac{dQ_D}{dV_S} \tag{2D.12}$$

$$C_{sd} = -\frac{dQ_S}{dV_D} \tag{2D.13}$$

By differentiating Q_D and Q_S using (2D.2), analytical expressions of all these capacitances are obtained in terms of the mobile charge sheet densities at the source and drain ends. These expressions become explicit by using the charge sheet expressions in [84] to calculate the mobile charge sheet densities at source and drain.

Therefore, analytical expressions of all the capacitances have been obtained.

It has to be remarked that, due to charge conservation, only four out of the nine possible capacitances are independent. The other five capacitances can be calculated from the four independent capacitances using equations derived from the charge conservation equation.

2D.3 Simulation Results

To validate this model, we have compared the capacitance modeled characteristics with 3D numerical simulations using DESSIS-ISE [104]. We have assumed a device with channel

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length L=1 μm, a silicon film radius R=6.25 nm, a silicon oxide thickness t_{ox}=1.5 nm, and a mid-gap gate electrode (gate working function of 4.61 eV). Since the Si body diameter is higher than 10 nm, quantum effects are neglected [99]. We have considered Q_{ox}=0. The value of mobility used is 290 cm^2/Vs. Fig.2D.2 shows the comparison between the modeled and numerically simulated transfer characteristics. As expected, the agreement between them is very good. Also the model provides a smooth transition between all the operation regimes (linear, saturation and subthreshold) without fitting parameters.

An excellent agreement is also observed between the modeled and numerically simulated values of C_{gd}, C_{gs}(Fig.2D.3), C_{dg}, C_{sg} (Fig.2D.4) and C_{sd}, C_{ds} (Fig.2D.5) as functions of the gate voltage, for different values of the drain-source voltage. Again, the modeled capacitance characteristics show smooth transition between the different operating regimes. For demonstrating the accuracy of the capacitance model, we introduced Fig.2D.6, where the model is derived for V_{DS}=0. It can be seen that $C_{gd}=C_{gs}$, $C_{dg}=C_{sg}$ and $C_{ds}=C_{sd}$, as it should. In these figures all the capacitances are presented in their normalized form, as $C/2\pi RC_{ox}L$, where C stands for any of the capacitances: C_{gd}, C_{gs}, C_{dg}, C_{sg}, C_{sd} and C_{ds}. In order to have a complete model for the drain and source capacitances, we have to account for the parasitic capacitance, which in the case of the DESSIS-ISE 3D

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simulations of the C_{gs}, C_{gd}, C_{dg} and C_{sg} capacitances appears to be a constant ($1.1*10^{-17}$ F) and is added to the previously modelled intrinsic C_{gs}, C_{gd}, C_{dg} and C_{sg} capacitances as a constant, showing an almost perfect agreement (Figs. 2D.3, 2D.4, 2D.6).

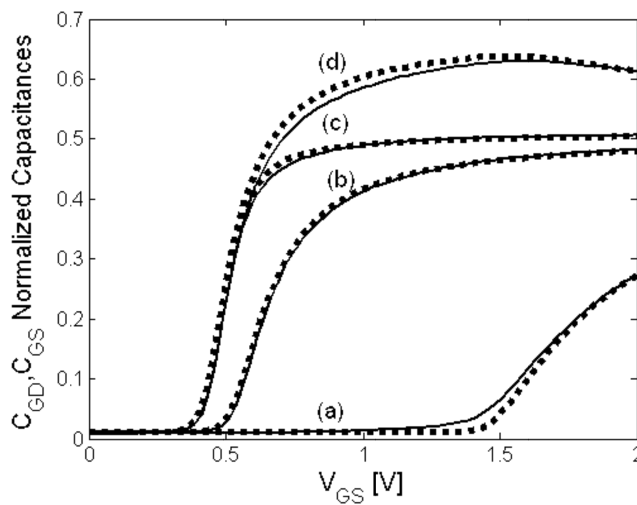

Fig.2D.3 *Normalized gate to drain capacitance (a, b) and gate to source capacitance (c, d) with respect to the gate voltage, for* V_{DS}*=0.1V (b,c) and* V_{DS}*=1V (a,d). Solid line: DESSIS-ISE simulations; Symbol line: analytical model*

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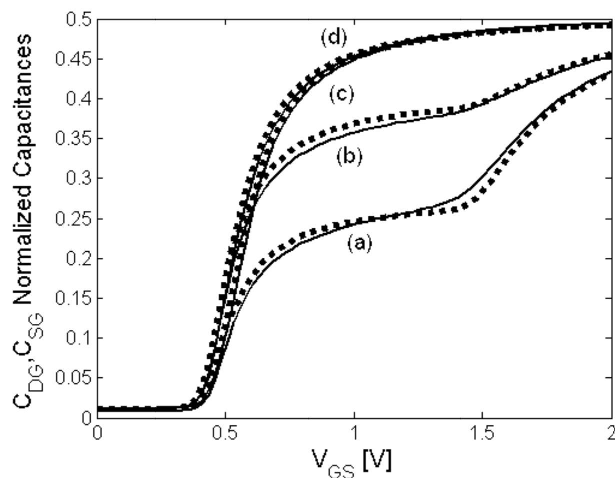

Fig.2D.4 *Normalized drain to gate capacitance (a, c) and source to gate capacitance (b, d) with respect to the gate voltage, for V_{DS}=1V (a, b) and V_{DS}=0.1V (c, d). Solid line: DESSIS-ISE simulations; Symbol line: analytical model*

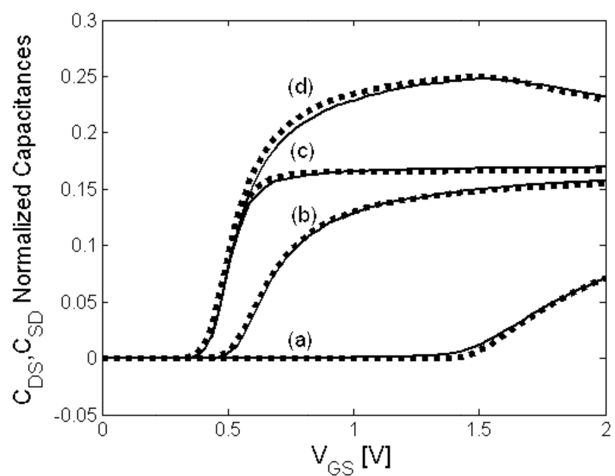

Fig.2D.5 *Normalized drain to source capacitance (c,d) and source to drain capacitance (a, b) with respect to the gate voltage, for V_{DS}=1V (a, d) and V_{DS}=0.1V (b, c). Solid line: DESSIS-ISE simulations; Symbol line: analytical model*

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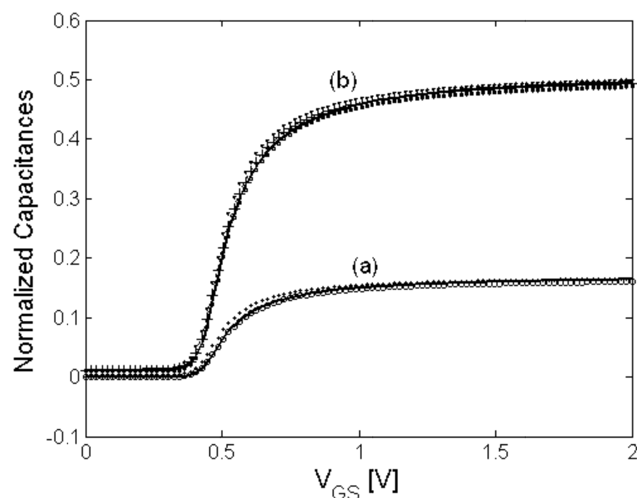
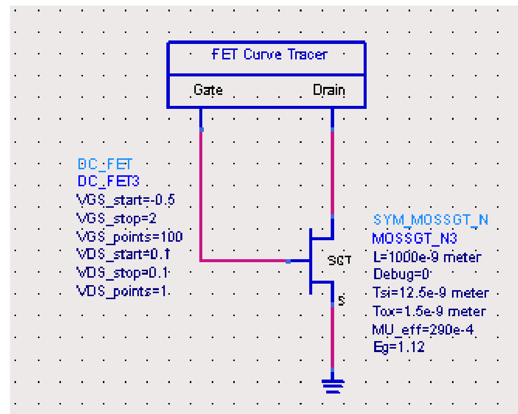


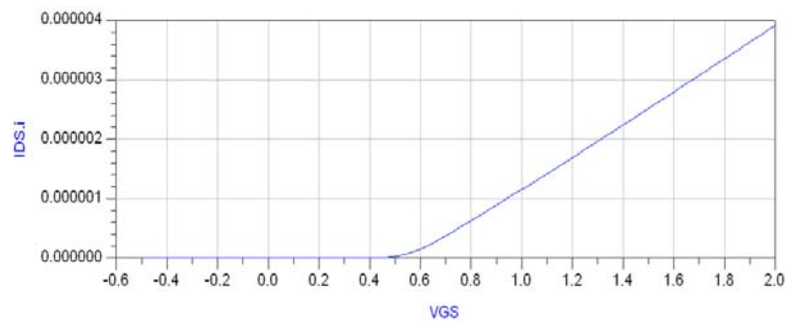
Fig.2D.6 *Normalized drain to source capacitance (*), source to drain capacitance (o) in (a), gate to drain capacitance (△), gate to source capacitance (□), drain to gate capacitance (+) and source to gate capacitance (:) in (b) with respect to the gate voltage, for V_{DS}=0V. Solid line: DESSIS-ISE simulations; Symbol line: analytical model*

The modelled capacitances in this section show excellent agreement with the 3D numerical simulations, in all operating regimes. Therefore, the model is very promising for being used in circuit simulators. The group of Professor Roldán Aranda, from the University of Granada has implemented and tested the SGT current model in the circuit simulator AGILENT ADS (Advanced Design System) and good results were obtained (Fig.2D.7). The next step is the introduction of our SGT capacitance model.

Surrounding – Gate MOSFET



a)



b)

Fig.2D.7 *a) Simulation of the SGT structure in AGILENT ADS (Advanced Design System). b) Result for the transfer characteristics, for V_{DS}=0.1V, in AGILENT ADS (Advanced Design System)*

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Chapter 3

Parasitic Capacitances Related to Multiple-Gate Field-Effect Transistor Architectures

In this section

the impact of important geometrical parameters such as source and drain thickness, fin spacing, spacer width, etc. on the parasitic fringing capacitance component of multiple-gate field-effect transistors (MuGFET) is deeply analyzed using finite element simulations [131]. Several architectures such as single gate, FinFETs (double gate), triple-gate represented by Pi-gate MOSFETs are simulated and compared in terms of channel and fringing capacitances for the same occupied die area. The

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impact of these technological solutions on the transistor cut-off frequencies is also discussed. Also a decomposition of the fringing capacitance into several portions is made, in order to see which part has the highest influence on the total fringing capacitance.

3.1. Introduction

In order to pursue the scaling of MOS devices into the 45-nm technology node, nonplanar double-gate (DG) and triple-gate MOSFETs (such as FinFETs, Pi-gate FETs) have become attractive for their good control of short channel effects and high current drive [12]. Currently, the technological trend points towards the FinFET device as a likely-to-emerge structure also thanks to its excellent compatibility with the quasi-planar Si technology [13]. However, large series resistances, which are induced by the narrow-fin nature of nonplanar MOSFETs, result in a significant degradation of current drive in direct current operation regions. Another effect of the increase in the source/drain and gate resistances is the decrease of the maximum cutoff frequency and so, the decrease of the transistor's gain in RF. Also an augmentation of source and gate resistances means a noise increment. So, in order to retain the advantages of a narrow fin width techniques like Selective

Epitaxial Growth (SEG) are employed [132]. The SEG technology is effective in decreasing the parasitic S/D resistance, which also translates into improved drive current. The impact of SEG dimensions on the parasitic MuGFET capacitances will be discussed in this section. A recent FinFET geometrical approach has been proposed in [71], observing the capacitance parasitics, but without considering SEG technology impact. One of the primary requirements for MuGFETs to be a technology enabler is that they must have at least the same current drive as the planar technology, for identical layout area [133]. So, in order to find out which are the dimensions for an optimum MuGFET, we compare the parasitic and channel capacitances between the different analyzed MOSFETs, based on equal die area occupation. In this way, we develop new design guidelines for the best performance. Furthermore, in order to thoroughly investigate the influence of geometrical parameters on the RF performance, the simulated cutoff frequencies of MuGFETs with respect to the fins spacing and to the introduction of SEG, are shown.

3.2. Capacitance Analysis

COMSOL software uses the proven finite-element analysis (FEA) method to efficiently model any physical phenomena which can be described by partial differential equations. Due to its tight coupling into MATLAB, the simulations can be done

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very fast and easy compared to other commercially available simulation tools. Fig. 3.1 shows the simulated structure of one half of a FinFET fin. For the simulation of a single gate transistor (SG) we consider a very wide fin, with thick gate oxide on both sides of that fin; and for the Pi-gate transistor simulation we consider an extension of the gate into the buried oxide (BOX) and a thin top gate oxide (triple gate). In order to consider the most up to date geometrical parameters for MuGFETs, we intensively reviewed the recent publications (see Table 3.1) on that topic. Table 3.2 summarizes the main geometrical parameters considered in this work for the nominal SG and MuGFETs, considering the same occupied area. The capacitance values have been normalized to the actual occupied planar silicon die area:

$$A = W \cdot L \tag{3.1}$$

where W is the total occupied silicon width of the transistor and L, the gate length (Table 3.2). The total occupied silicon width for MuGFETs is:

$$W = \left(N_{fin} - 1\right)\left(S_{fin} + W_{fin} + 2 \cdot t_{ox}\right) + (W_{fin} + 2 \cdot t_{ox}) = 4280\ nm \tag{3.2}$$

where N_{fin}, S_{fin}, W_{fin} and t_{ox} are, respectively, the number of fins, the fins spacing, the fin width and the gate oxide thickness.For the nominal SG transistor, the transistor width to occupy the

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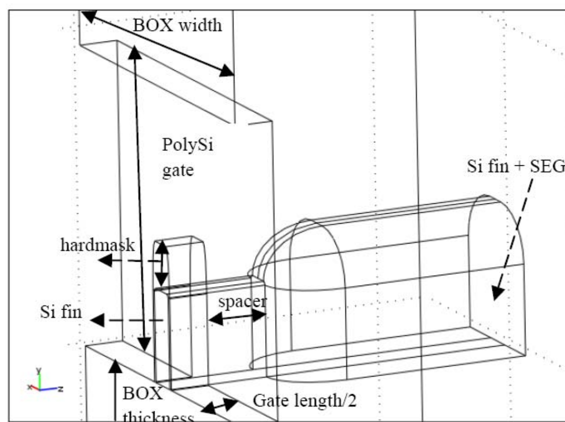
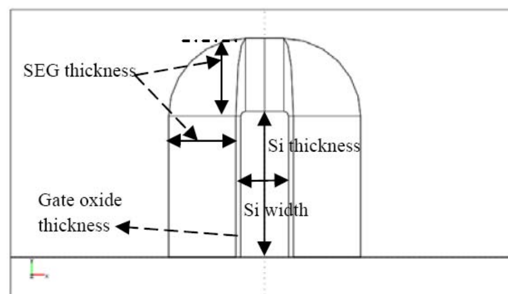
same area is the total occupied silicon width of MuGFET reduced by twice the side oxide (Table 3.2): $4280 - 2 \cdot 30 = 4220\ nm$



(a)



(b)

Fig.3.1 *(a) 3-D structure for half of a FinFET fin simulated with COMSOL, (b) front 2-D view of the same structure.*

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As it will be explained later on, the optimization of the $C_{channel}/C_{fringing}$ ratio is of first importance to improve the analog/RF performance of MOSFETs. For the nominal dimensions summarized in Table 3.2, we obtain a very good agreement between the simulated values of this ratio and the measurements presented in [134]. In the following sections, we simulate the impact of the main geometrical parameters (spacer width, S_{fin}, SEG, gate extension depth for Pi-gate) on the fringing and channel capacitances, in strong inversion. These capacitances are calculated by integration of the surface charge in the fin region, for the channel capacitance (theoretical intrinsic capacitance), and outside the channel for the fringing capacitance - mainly between the vertical poly-Si gate and the fin, but also through the BOX.

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MuGFET		**SG**	
Fin Width (W_{fin})	20	Transistor Width	4220
Fin Height	60	Silicon Thickness	60
PolySi gate	100	PolySi gate	100
Gate oxide (t_{ox})	2	Gate oxide (t_{ox})	2
No. of fins (N_{fin})	20	-	-
SEG thickness	30	SEG thickness	30
Gate length (L)	50	Gate length	50
Hardmask	30	Side Oxide	30
Spacer Width	40	Spacer Width	40
BOX thickness	150	BOX thickness	150
S_{fin}	200	-	-
$C_{channel}$ (F/m^2)	0.009	$C_{channel}$ (F/m^2)	0.017
$C_{fringing}$ (F/m^2)	0.005	$C_{fringing}$ (F/m^2)	0.005
$C_{channel}/C_{fringing}$	1.8	$C_{channel}/C_{fringing}$	3.4

Table 3.2. *Nominal values for the studied devices. All geometrical dimensions are given in nm.*

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3.2.1. Integration level

From Table 3.2, we notice that the normalized channel capacitance is higher in the case of the SG, due to a higher effective width for the same occupied Si area, which translates into a higher drive current (when we assume that both devices have the same mobility and the same source-drain resistances), whereas the relative importance of the fringing capacitance is higher for FinFET. Our goal is to have at least the same drive current in a FinFET as in a SG for the same occupied area, so we should increase the fin height or decrease the spacing between fins (pitch). Indeed, multiple-fin devices can exceed the area efficiency of traditional planar devices if the fin height is greater than half the pitch (for FinFETs) or half the spacing (for triple gate MOSFETs). However, the fin height is somehow technologically limited due to aspect ratio (fin width/fin height) and topography considerations [135]. In fact, increasing the ratio between fin width and fin height causes degradation of the gate control over the active channel for a fixed gate length [11]. Nowadays, the ratio does not exceed 1/6 [71], so the fin height is limited to typically 50 to 100 nm [136]. Also, the increased topography impacts the gate lithography and etching [137] as well as the silicidation process of the contacts. Thus, due to these technological limitations regarding the fin height, as

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presented in Section C, we analyzed the impact of the fin spacing of MuGFET on the drive current density and also on the parasitic capacitances.

3.2.2 Impact of SEG technology

One of the major disadvantages of MuGFETs with narrow fin width is the associated high parasitic S/D resistances, which degrade the drive current and the transconductance. For its minimization it is desirable to widen the S/D extension regions alone without widening the body region [132], i.e. without compromising short channel control. This is achieved using SEG technology. As presented in [138], a SEG thickness of 50 nm reduces the series resistances by a factor of 4. However, as we see in Fig. 3.2, the drawback of the SEG process is an increase in the parasitic capacitance. Hence, there exists a trade-off between series S/D resistance minimization and parasitic capacitance augmentation.

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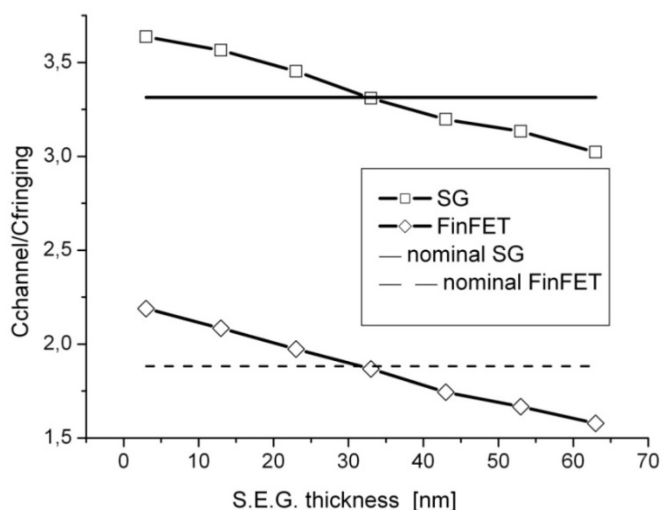

Fig.3.2 $C_{channel}/C_{fringing}$ *ratio versus SEG thickness.*

The simulations are in agreement with the measurements in [132], where they experimentally observed a 10% increase of the parasitic capacitance with the introduction of SEG process. It can be noted that the ratio is lower in the case of the FinFET for the nominal value of the fin spacing found in the literature. It means that the parasitic fringing capacitances are relatively more important in the case of FinFETs compared to SG. As presented in the next Section, an increase of this ratio, in the case of MuGFETs can be achieved by reducing the spacing between fins.

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3.2.3 Impact of fin spacing

First of all, by minimizing the fin spacing we assure a higher drive current for MuGFETs for the same occupied Si area. Fig. 3.3 shows the channel and fringing capacitances for a SG and various FinFETs characterized by different fin spacings and different numbers of fins (the occupied area being fixed). We can see that for a fin spacing below 100 nm, the normalized drive current of FinFETs is higher than the one of a SG. The absolute value of the fringing capacitance for FinFETs also increases with the decrease of fin spacing, i.e. with the increasing number of fins, but as shown in Fig. 3.4 the relative importance of these fringing capacitances is greatly decreased (higher $C_{channel}/C_{fringing}$ ratio) with the reduction of S_{fin}. Indeed, for a fin spacing of 60 nm the $C_{channel}/C_{fringing}$ ratio for FinFETs reaches a similar value as for the SG devices. As explained in [139] a fin pitch of 50 nm can be obtained, using a fin doubling and quadrupling technique based on spacer lithography.

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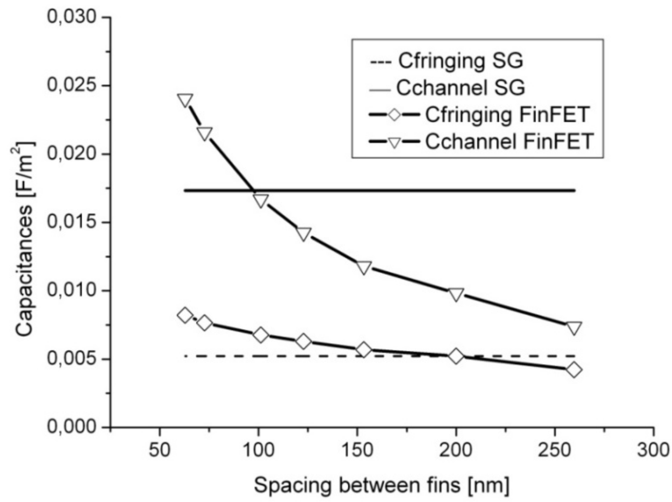

Fig.3.3 *Fringing and channel capacitances versus fin spacing*.

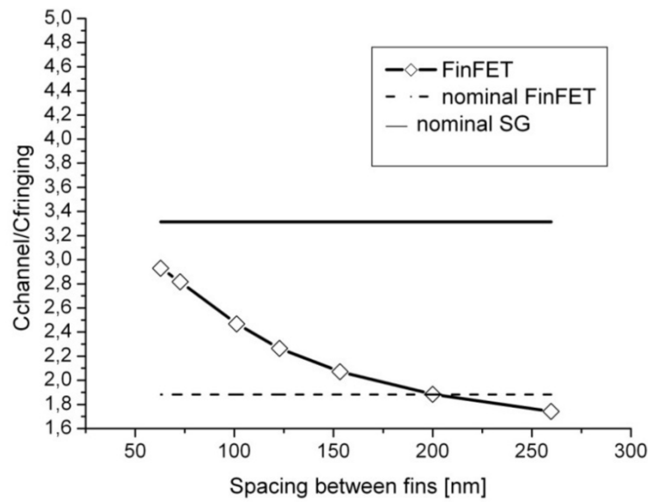

Fig.3. 4 $C_{channel}/C_{fringing}$ *ratio versus fin spacing.*

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3.2.4 Impact of gate extension depth into the BOX

In [11], J.-P. Colinge showed that Pi-gate structure – extension of gate material into the BOX - could be of great interest for controlling short channel effects in MuGFETs. In Fig. 3.5, we indeed see a nice increase of the channel capacitance for Pi-gate devices compared to the FinFET architecture. But our simulations also show that the fringing capacitance increases with the extension depth for values higher than 10 nm. The optimum $C_{channel}/C_{fringing}$ ratio (higher channel capacitance and lower fringing capacitance) for Pi-gate is obtained for a gate extension of 10 nm - $C_{channel}/C_{fringing}$ = 2.2 (compared to 1.8 for FinFET).

3.2.5 Impact of spacer width

For minimizing the source and drain resistances, the spacer width can be optimized, without modifying the channel control, to values lower than 20 nm [138]. Unfortunately, as presented in Fig. 3.6, a decrease of the spacer width will lead to an increase of the fringing capacitances, therefore, we face again a trade-off.

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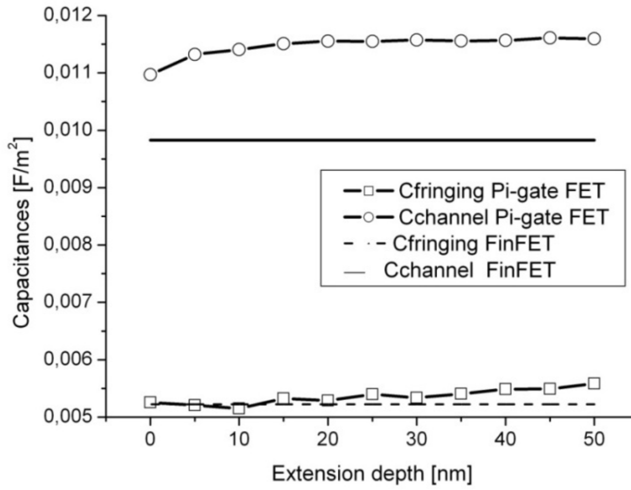

Fig.3.5 *Fringing and channel capacitances vs. gate extension depth.*

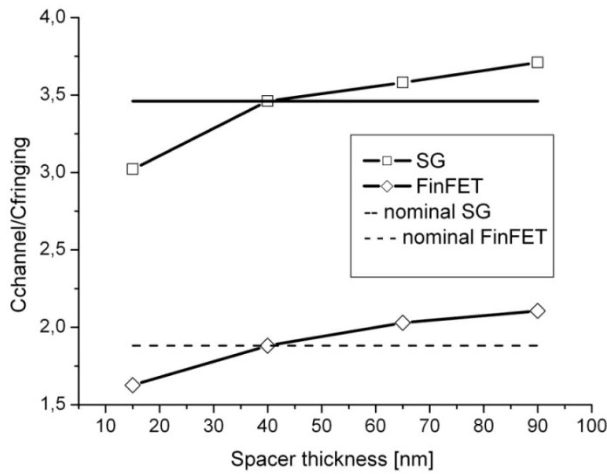

Fig.3.6 $C_{channel}/C_{fringing}$ *ratio versus spacer thickness.*

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3.3. Cutoff Frequencies

In previous section, we have shown the impact of SEG and fin spacing on the fringing capacitances. As we mentioned, using SEG technology there is a tradeoff between the reduction of series resistances and the increase of fringing capacitances.

Based on the expressions (3.3) and (3.4) the current gain and maximum available gain cutoff frequencies, respectively, have been calculated using the equivalent lumped elements extracted from measurements in [134] and the $C_{channel}/C_{fringing}$ (C_{gs}/C_{gd}) ratio simulated in this work.

$$f_T = \frac{f_c}{\left(1+\frac{C_{gd}}{C_{gs}}\right)+\left(R_s+R_d\right)\left(\frac{C_{gd}}{C_{gs}}\left(g_m+g_d\right)+g_d\right)} \quad (3.3)$$

with $f_c = \frac{g_m}{2\pi C_{gs}}$

$$f_{max} = \frac{f_c}{\left(1+\frac{C_{gd}}{C_{gs}}\right)}\frac{1}{2\cdot\sqrt{g_d\left(R_g+R_s+R_i\right)+\frac{1}{2}\frac{C_{gd}}{C_{gs}}\left(\left(R_s+R_i\right)g_m+\frac{C_{gd}}{C_{gs}}\right)}} \quad (3.4)$$

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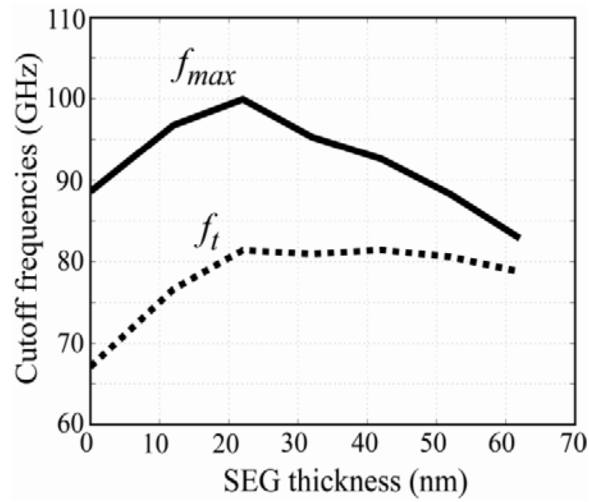
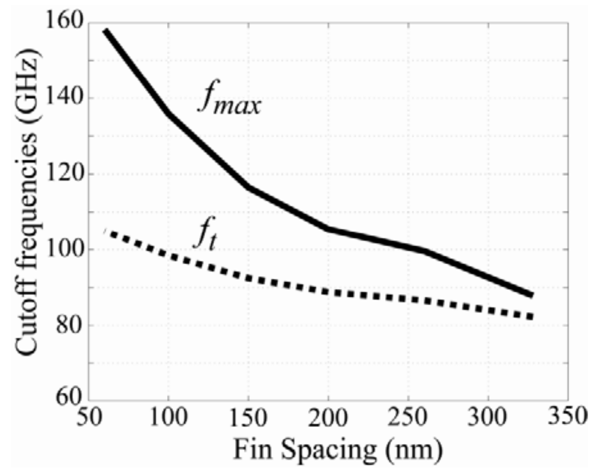


(a)



(b)

Fig.3.7 *Cutoff frequencies vs. (a) SEG thickness and (b) fin spacing for L=50nm*

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Fig. 3.7a clearly shows the existence of an optimum SEG thickness layer, which achieves the best trade-off between the series resistances (R_s and R_d) and the C_{gd}/C_{gs} ratio, corresponding to the peak values of f_t and f_{max}. Fig. 3.7b presents the cutoff frequencies of MuGFET versus fin spacing. We observe an improvement of both cutoff frequencies with the reduction of S_{fin}, thanks to the decrease of C_{gd}/C_{gs} ratio (increase of $C_{channel}/C_{fringing}$ ratio), the increase of the fin numbers and thus the reduced values of the access resistances. In order to further make our study more detailed, we decompose the fringing capacitance for one fin in the nominal FinFET, into several portions. In this way we can see which portion has the highest influence on the total fringing capacitance.

As before we vary some of the technological parameters like: polysilicon thickness (Fig. 3.9,3.10), SEG thickness (Fig.3.11, 3.12), spacing between fins (Fig. 3.13, 3.14) and spacer thickness(Fig.3.15, 3.16).

In Fig. 3.8 we present the schematics of the structure, showing the capacitances considered.

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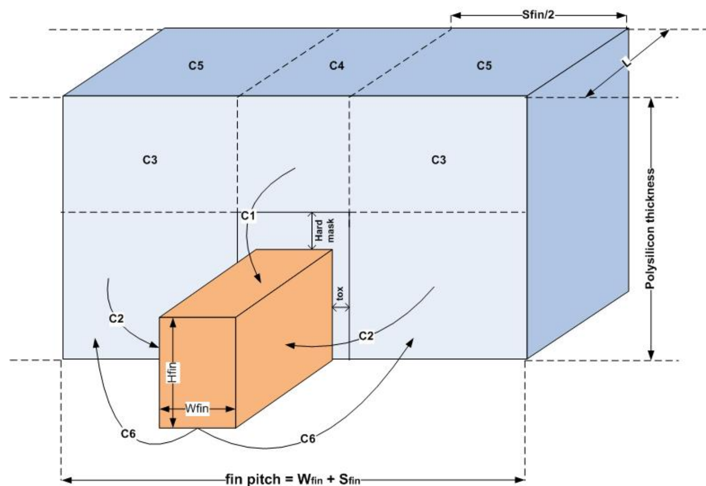

Fig.3.8 *Fringing capacitances considered for one fin in the nominal FinFET. See Table 3.2*

C_1 can be regarded as the contributions of the electric flux from the gate sidewalls to the top surfaces of the silicon fins.

C_2 is induced by the coupling between a side surface of the silicon fins and the polysilicon gate.

C_4 is associated with the electric flux starting from the top surface of the polysilicon gate and ending on the top surface of the silicon fins.

C_6 represents the capacitance associated with the electric flux from the bottom of the polysilicon gate to the bottom of the silicon fins in S/D extensions only.

C_3, C_5 represent the influence of the polysilicon surfaces 3 and 5 on the silicon fins.

$$C_{fringing/fin} = C_1 + C_2 + C_3 + C_4 + C_5 + C_6 \quad (3.5)$$

C_2 in (3.5) represents the sum of all C_2 capacitances from Fig. 3.8. The same goes for C_3, C_5 and C_6. These capacitances are calculated as before, by integrating the surface charge on the different polysilicon regions: C_1 in region 1, C_2 in region 2, etc.

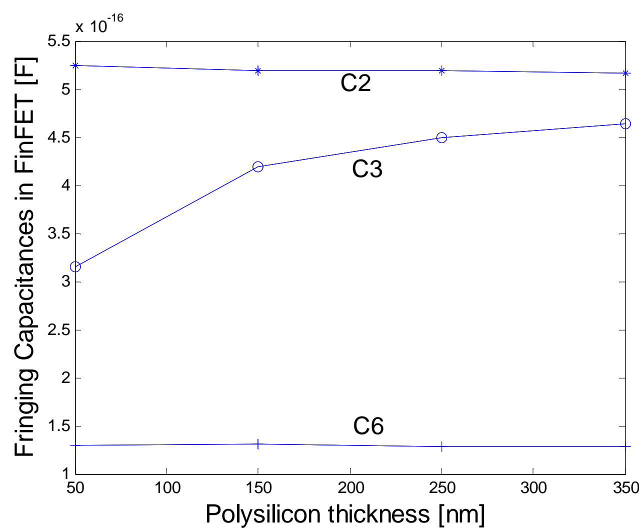

Fig.3.9 *C_2, C_3, C_6 versus polysilicon thickness*

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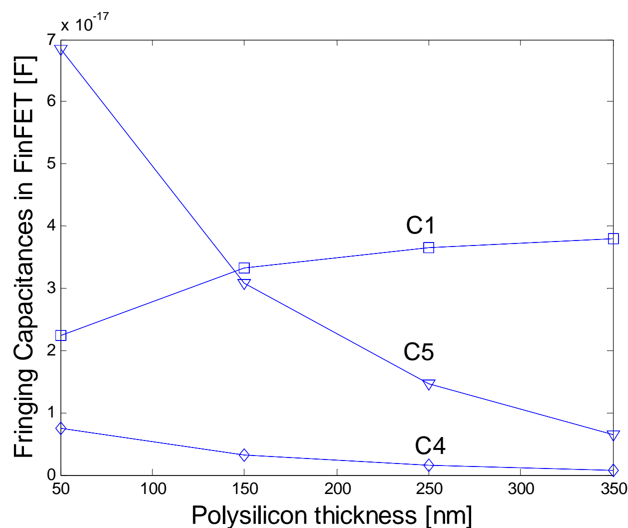

Fig.3.10 *C_1, C_4, C_5 versus polysilicon thickness*

As expected, see [71], C_1 and C_3 will increase with the increase of the polysilicon thickness, while C_4 and C_5 will decrease. Even if C_2 and C_6 remain constant with the increase of the polysilicon thickness, they present an important part of the total fringing capacitance, C_2 being the heighest one from all 6 capacitances.

One conclusion that we can draw from here is that the spacing between fins is of most importance due to the fact that the portions of polysilicon between fins give the highest fringing capacitances: C_2, C_3 and C_6.

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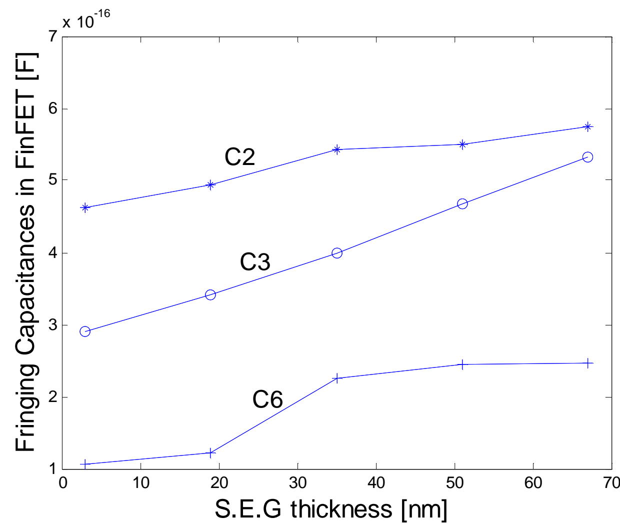

Fig.3.11 *C_2, C_3, C_6 versus S.E.G. thickness*

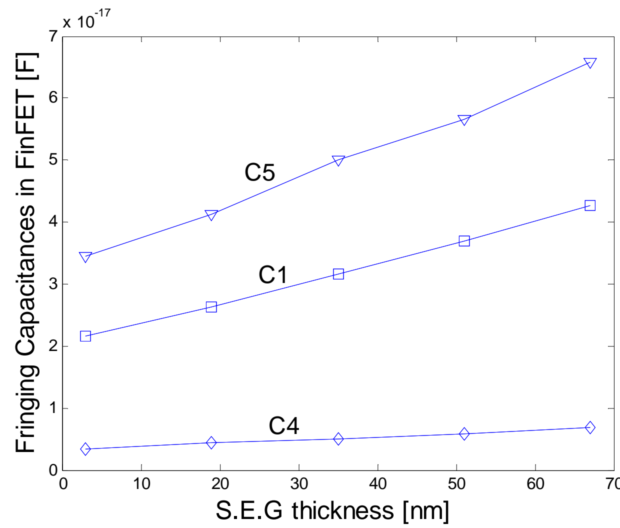

Fig.3.12 *C_1, C_4, C_5 versus S.E.G. thickness*

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All fringing capacitances increase with the increase of SEG thickness. So SEG process is one of the most important factors in the increase of the fringing capacitance, even if it helps reducing the series resistance.

The order of importance is maintained as before: C_2, C_3, C_6, C_1, C_4 and C_5.

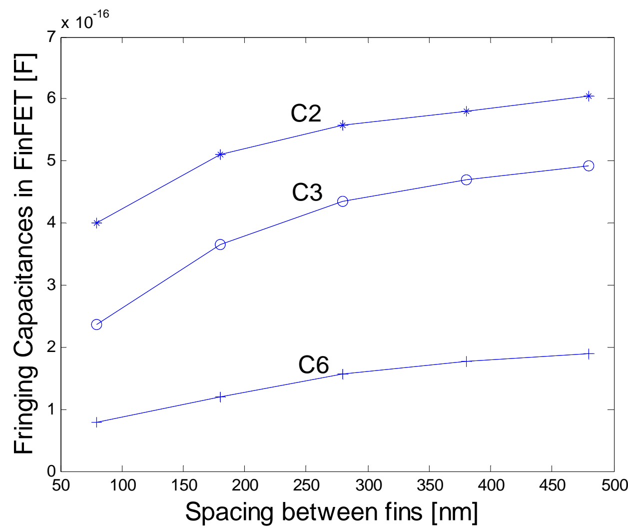

Fig.3.13 *C_2, C_3, C_6 versus spacing between fins*

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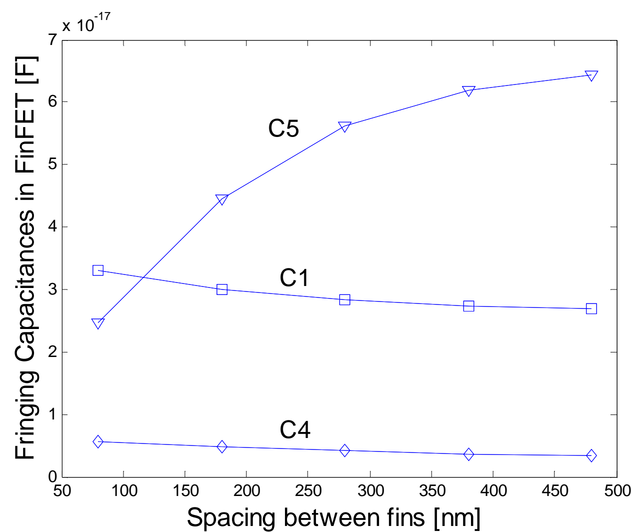

Fig.3.14 *C_1, C_4, C_5 versus spacing between fins*

All the fringing components that depend on the electric flux from the polysilicon between fins to the silicon fins increase if the spacing between fins increases. As presented before a small spacing will provide less parasitic capacitances.

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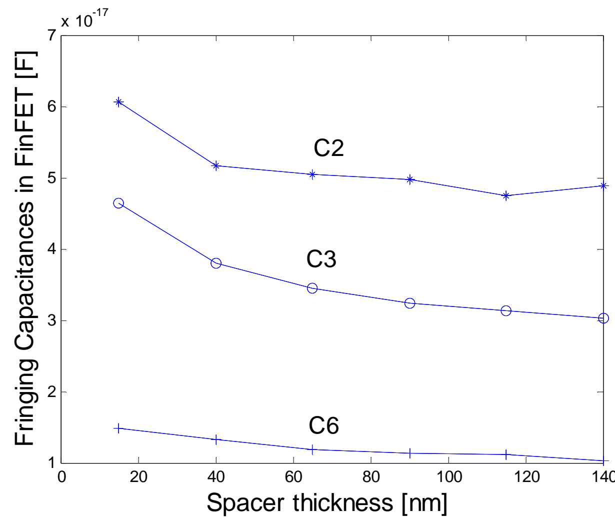

Fig.3.15 *C_2, C_3, C_6 versus spacer thickness*

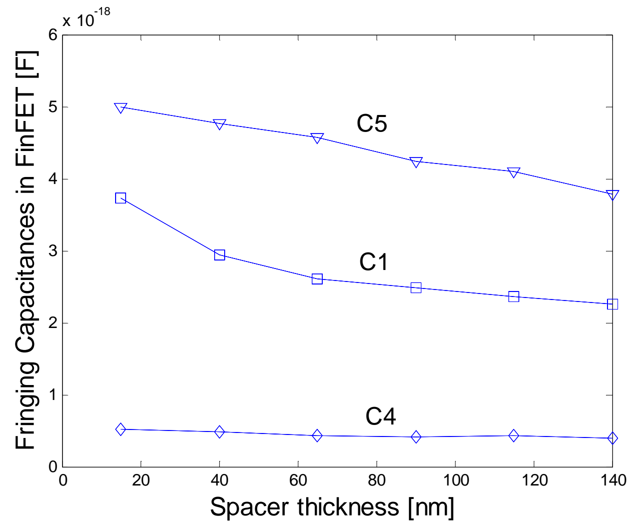

Fig.3.16 *C_1, C_4, C_5 versus spacer thickness*

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All components of the fringing capacitance will decrease with the increase of the spacer thickness.

From Fig. 3.12-3.16 we can see that C_2 is the most dominant among the fringing capacitive components in multifin FinFETs and it is independent of the polysilicon thickness.

Based on these simulation results, the reduction of the fin spacing appears to be a major technological issue for the next MuGFET generations for achieving high integration density level as well as high analog/RF performance.

In conclusion simulations highlight the great impact of diminishing the spacing between fins for MuGFETs and the trade-off between the reduction of parasitic source and drain resistances and the increase of fringing capacitances when Selective Epitaxial Growth (SEG) technology is introduced.

In order to optimize the RF performance of MuGFETs, their geometry has to fulfill the following design rules:

- fin spacing should be reduced down to 50 nm;
- SEG thickness should be kept between 30-50 nm for a good trade-off between low S/D resistances and parasitic capacitance;
- spacer thickness should be kept between 15-30 nm for a good trade-off as well;

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- Pi-gate devices (referred gate extension depth of 10 nm) have a better $C_{channel}/C_{fringing}$ ratio than FinFETs and are, then, of interest for analog/RF applications.

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Chapter 4

Conclusions and recommendations for future work

4.1 Conclusions

In this thesis we have developed explicit compact charge and capacitance models adapted for doped and undoped long-channel devices (doped DG MOSFETs, undoped DG MOSFETs, undoped UTB MOSFETs and undoped SGT) from a unified charge control model derived from Poisson's equation. The modelling scheme is similar in all these devices and is adapted to each geometry. The dc and charge models are fully compatible. The capacitance expressions are derived from the charge model. The current, total charges and capacitances are written in terms of the mobile charge sheet densities at the source and drain ends of the channel. Explicit and infinitely

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continuous expressions are used for the mobile charge sheet densities at source and drain. As a result, all small signal parameters will have an infinite order of continuity. The modeled capacitances show excellent agreement with the 2D and 3D (SGT) numerical simulations, in all operating regimes. Therefore, the model is very promising for being used in circuit simulators.

Due to the limitation of available optimized devices for analysis, numerical simulation was used as the main analysis tool. However, when available, measurements were used to validate our results. The experimental part was realised at the Microelectronics Laboratory, Université Catholique de Louvain, Louvain-la Neuve, Belgium.
For example, in section 2A, in the case of highly-doped DG MOSFETs we could compare our results with experimental data from FinFETs modeled as DG MOSFETs. The drain current expression shows a good agreement compared to experimental data as well 2D numerical simulations from subthreshold to well above threshold, for long-channel MOSFET. The modeled capacitances show good agreement with the 2D numerical simulations, for all operating regimes. To have a complete model, we take into account the extrinsic capacitances like fringing and overlap capacitances. Considering this, the model can be included in circuit simulators, in particular for baseband

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analog circuits.

Also, this model has been extended and made functional for a variety of doping concentrations, between 10^{14} and $3x10^{18}$ cm^{-3}, by computing the difference between the potential at the surface and the potential at the middle of the silicon layer. In this case the capacitance model proves to be working very good, as well.

The main advantage of this work is the analytical and explicit character of the charge and capacitance model that makes it easy to implement in circuit simulators. The model presents almost perfect results for different cases of doping (doped/undoped devices) and for different non classical MOSFET structures (DG MOSFET, UTB MOSFETs and SGT). The variety of the MOSFET structures in which our modeling scheme has been included and the obtained results, demonstrate its absolute validity.

In the case of the undoped DG MOSFET model in section 2B, the volume inversion phenomena is also explained. This model correctly predicts the volume-inversion effect, shown by intrinsic capacitances graphs for devices with different silicon thicknesses. The model predicts well the dependence of capacitances with the reduction of the silicon layer thickness. The developed model simulates the volume inversion and Si film dependence thickness effects in the DG-MOSFET down to

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a silicon layer of 10 nm-thick. The reduction of the Si film thickness in conditions of volume inversion, may not improve the delay time, although of course, it reduces short channel effects permitting the downscaling of the device's channel length. Therefore, the advantages of reducing the Si film thickness for high-speed and high-frequency operation are not clear.

SCE (Short Channel Effects) like: velocity saturation, channel length modulation and DIBL effects are added to the DC model for the undoped DG MOSFET. These are calculated using an approximate solution of the 2D Poisson's equation. By studying these effects we get a good idea about how the device will perform when scaling down its dimensions.

We demonstrate that ΔL was found to be approximately half of the channel length at an operated voltage of 1V for L=50nm. This indicates that the length of the saturated region will become an even more important parameter for deeply scaled MOSFETs. Also, ΔL can be reduced using a thinner silicon film, by approximately the same amount on both gate lengths: L = 50nm and L = 120nm. ΔL is also found reduced for thinner gate oxides.

In chapter 3, we investigate the influence of geometrical parameters on the RF performance in MuGFETs.

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It is expected that due to 3-D interconnections, multiple gate MOSFETs to have high parasitic capacitances, which can affect the analog/RF performance.

We show the impact of important geometrical parameters such as source and drain thickness, fin spacing, spacer width, etc. on the parasitic fringing capacitance component of multiple-gate field-effect transistors (MuGFET). Several architectures such as single gate, FinFETs (double gate), triple-gate represented by Pi-gate MOSFETs are simulated and compared in terms of channel and fringing capacitances for the same occupied silicon area. Results highlight the advantage of diminishing the spacing between fins for MuGFETs and the trade-off between the reduction of parasitic source and drain resistances and the increase of fringing capacitances when Selective Epitaxial Growth (SEG) technology is introduced, in order for MuGFETs to be a technology enabler and have at least the same current drive as the planar technology, for identical layout area.

We also present the simulated cutoff frequencies of MuGFETs with respect to the fins spacing and to the introduction of SEG, to further prove the impact of geometrical parameters on RF performance of these devices.

Also a decomposition of the fringing capacitance into several portions is made, in order to see which part has the heighest

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influence on the total fringing capacitance. All the fringing components that depend on the electric flux from the polysilicon between fins to the silicon fins increase if the spacing between fins increases. We show that the capacitance which is induced by the coupling between a side surface of the silicon fins and the polysilicon gate is the most dominant among the fringing capacitive components in multifin FinFETs. These results also corroborate the fact that the reduction of the fin spacing appears to be a major technological issue for the next MuGFET generations for achieving high integration density level as well as high analog/RF performance. The goal of our study and work is the usage of our models in circuit simulators. This part, of implementing and testing our models of these multi gate MOSFET devices in circuit simulators has already begun. The group of Professor Roldán Aranda, from the University of Granada has implemented the SGT current model in the circuit simulator Agilent ADS (Advanced Design System) and good results were obtained. The next step is the introduction of our SGT capacitance model.

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4.2 Recommendations for future work

We have only studied devices for channel thicknesses larger than 10nm which allows us to exclude quantum effects from the model. A natural continuation of this work is to study devices where quantum effects should be included.

The future work will take into consideration the application and adaptation of our charge and capacitance model in asymmetric doped/undoped DG MOSFETs (an extension of our UTB MOSFET model) and doped SGT for short-channel devices. This extended charge model will be based on the DC model adapted to short channel effects. Also, we will consider the development of these models in high frequency. A first step towards this development has been made in [100], where an analytical model for high frequency and microwave noise model of our nanoscale doped DG MOSFET is presented. The model is based on the one detailed in section 2A.2 and it includes overshoot velocity effects. Also, its RF and noise performances are calculated.

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So, in the end, we will have complete small signal models for all types of channel lengths, in all the frequencies, for both doped and undoped multi gate MOSFET structures.
A further extension of this work is the adaptation of the model to devices below the 22nm node where the transport is quasi-ballistic or ballistic.

Finally, the new modeling scheme can be applied to other novel FET structures, such as Schottky Barrier SOI MOSFETs, strained Si/SiGe SOI MOSFETs and carbon based nanotubes and nanoribbons.

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Appendix

The solution of Eq. (2A.26) is:

$$Q_{Tot} = (2w)^2 \frac{\mu}{I_{DS}} \left(\frac{Q^3}{3C_{ox}} + \frac{kT}{q}\frac{Q^2}{2} + \frac{kT}{q}\left(-Q_{Dep}Q + \frac{Q^2}{2} + Q_{Dep}^2 \log\left[Q_{Dep} + Q\right] \right) \right) \Big|_{Q_s}^{Q_d} \quad (2a.35)$$

and the solution for Eq. (2A.28) is :

$$Q_D = -\frac{(2w)^3 \mu^2}{LI^2{}_{DS}} \left(\frac{1}{2C_{ox}{}^2 q^2} \left(\begin{array}{l} -\frac{1}{3} C_{ox} Q_{Dep} kT \left(Q_{Dep}^2 q - 3qQ_s^2 - 12C_{ox} kQ_s T\right) Q + \\ +\frac{1}{6} C_{ox} kT \left(Q_{Dep}^2 q - 6qQ_s^2 - 6C_{ox} Q_{Dep} kT - 24 C_{ox} kQ_s T\right) Q^2 + \\ +\frac{1}{9}\left(-3q^2 Q_s^2 - C_{ox} Q_{Dep} kqT - 12 C_{ox} kqQ_s T + 24 C_{ox}^2 k^2 T^2\right) Q^3 + \\ +\frac{3}{2} C_{ox} kqTQ^4 + \frac{q^2 Q^5}{5} + \frac{1}{3} C_{ox} Q_{Dep}^2 kT \left(Q_{Dep}^2 q - 3qQ_s^2 - 12 C_{ox} kQ_s T\right) \\ \cdot \log\left[Q_{Dep} + Q\right] - \frac{2}{3} C_{ox} Q_{Dep} kTQ \left(-3C_{ox} Q_{Dep} kT + 3C_{ox} kTQ + qQ^2\right) \\ \cdot \log\left[\frac{Q_{Dep} + Q}{Q_{Dep} + Q_s}\right] - C_{ox}^2 Q_{Dep}^3 k^2 T^2 \log\left[\frac{Q_{Dep} + Q}{Q_{Dep} + Q_s}\right]^2 \end{array} \right) \right) \Bigg|_{Q_s}^{Q_d} \quad (2a.36)$$

The solution of Eq. (2B.14) is:

$$Q_{Tot} = -W^2 \frac{\mu}{I_{DS}} \left(\begin{array}{l} \frac{Q^3}{6C_{ox}} + \frac{kT}{q}\frac{Q^2}{2} + \\ +2\frac{kT}{q}\left(-Q_0 Q + \frac{Q^2}{4} + 2Q_0^2 \log\left[2Q_0 + Q\right] \right) \end{array} \right) \Bigg|_{Q_s}^{Q_d} \quad (2b.25)$$

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and the solution for Eq. (2B.16) is :

$$Q_D = -\frac{W^3\mu^2}{L(I_{DS})^2}\left(\frac{1}{8C_{ox}^2}\left(\begin{array}{l}\frac{1}{5}Q^5 + 3\beta C_{ox}Q^4 + \frac{1}{9}\left(96\beta^2 C_{ox}^2 - 4\beta Q_0 C_{ox} - 24\beta Q_s C_{ox} - 3Q_s^2\right)Q^3 + \\ + \frac{2}{3}\beta C_{ox}\left(2Q_0^2 - 12\beta C_{ox}Q_0 - 3Q_s^2 - 24\beta Q_s C_{ox}\right)Q^2 - \\ - \frac{4}{3}\beta C_{ox}Q_0\left(4Q_0^2 - 3Q_s^2 - 24\beta Q_s C_{ox}\right)Q - \\ - \frac{8}{3}\beta C_{ox}Q_0\left(Q^2 + 6\beta C_{ox}Q - 12\beta Q_0 C_{ox}\right)\log\left[\frac{2Q_0 + Q}{2Q_0 + Q_s}\right]Q - \\ - 32\beta^2 C_{ox}^2 Q_0^3 \cdot \log^2\left[\frac{2Q_0 + Q}{2Q_0 + Q_s}\right] + \\ + \frac{8}{3}\beta C_{ox}Q_0^2\left(4Q_0^2 - 3Q_s^2 - 24\beta Q_s C_{ox}\right)\log\left[2Q_0 + Q\right]\end{array}\right)\right)\Bigg|_{Q_s}^{Q_d} \quad (2b.26)$$

The solution of Eq. (2C.12) is:

$$Q_{Tot} = -W^2\frac{\mu}{I_{DS}}\left(\frac{Q^3}{3C_{ox}(1+\alpha_1)} + \frac{kT}{q}\frac{Q^2}{2} + \frac{kT}{q}\frac{1}{4}\left(\log\left(2Q+Q_0\right)\cdot Q_0^2 + 2Q\left(Q-Q_0\right)\right)\right)\Bigg|_{Q_s}^{Q_d} \quad (2c.18)$$

$$a = C_{ox}(1+\alpha_1)$$

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and the solution for Eq. (2C.16) is :

$$Q_D = -\frac{W^3\mu^2}{L(I_{DS})^2}\frac{1}{2a^2}\left.\left(\begin{array}{l} \frac{Q^5}{5}+\frac{3}{2}a\beta Q^4+\frac{1}{18}\left(-6Q_s^2-24a\beta Q_s+48a^2\beta^2-aQ_0\beta\right)Q^3+ \\ +\frac{1}{24}a\beta\left(Q_0^2-12a\beta Q_0-24Q_s^2-96aQ_s\beta\right)Q^2- \\ -\frac{1}{24}aQ_0\beta\left(Q_0^2-12Q_s^2-48aQ_s\beta\right)Q- \\ -\frac{1}{6}aQ_0\beta\left(2Q^2+6a\beta Q-3aQ_0\beta\right)\log\left(\frac{Q_0+2Q}{Q_0+2Q_s}\right)Q- \\ -\frac{1}{8}a^2Q_0^3\beta^2\log^2\left(\frac{Q_0+2Q}{Q_0+2Q_s}\right)+ \\ +\frac{1}{48}aQ_0^2\beta\left(Q_0^2-12Q_s^2-48aQ_s\beta\right)\log\left(Q_0+2Q\right) \end{array}\right)\right|_{Q_s}^{Q_d} \quad (2c.19)$$

The solution of Eq. (2D.9) is:

$$Q_{Tot} = (2\pi R)^2\frac{\mu}{I_{DS}}\left(\frac{Q^3}{3C_{ox}}+\frac{kT}{q}\frac{Q^2}{2}+\frac{kT}{q}\left(-Q_0Q+\frac{Q^2}{2}+Q_0^2\log\left[Q_0+Q\right]\right)\right)\Big|_{Q_s}^{Q_d} \quad (2d.14)$$

and the solution for Eq. (2D.10) is :

$$Q_D = -\frac{(2\pi R)^3\mu^2}{L(I_{DS})^2}\left(\frac{1}{2C_{ox}{}^2q^2}\left(\begin{array}{l} -\frac{1}{3}C_{ox}Q_0kT\left(Q_0^2q-3qQ_s^2-12C_{ox}kQ_sT\right)Q+ \\ +\frac{1}{6}C_{ox}kT\left(Q_0^2q-6qQ_s^2-6C_{ox}Q_0kT-24C_{ox}kQ_sT\right)Q^2+ \\ +\frac{1}{9}\left(-3q^2Q_s^2-C_{ox}Q_0kqT-12C_{ox}kqQ_sT+24C_{ox}^2k^2T^2\right)Q^3+ \\ +\frac{3}{2}C_{ox}kqTQ^4+\frac{q^2Q^5}{5}+\frac{1}{3}C_{ox}Q_0^2kT\left(Q_0^2q-3qQ_s^2-12C_{ox}kQ_sT\right)\cdot \\ \cdot\log\left[Q_0+Q\right]-\frac{2}{3}C_{ox}Q_0kTQ\left(-3C_{ox}Q_0kT+3C_{ox}kTQ+qQ^2\right)\cdot \\ \cdot\log\left[\frac{Q_0+Q}{Q_0+Q_s}\right]-C_{ox}^2Q_0^3k^2T^2\log\left[\frac{Q_0+Q}{Q_0+Q_s}\right]^2 \end{array}\right)\right)\Bigg|_{Q_s}^{Q_d} \quad (2d.15)$$

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Sim/Experim	Fin Width	Fin Height	PolySi gate	Gate oxide	No. of fins	S.E.G. thickness	Gate length	Hardmask	Spacer	BOX thickness	Sfin	Reference
S	20	48-120	50-400	1.3	2--5		45	10--80	14		50-100	[71]
S	24	50-180			2		45					[133]
	12				8		25					
					100							
E	6.5	50		2.5	6		60					[140]
	36											
	40											
E	15	60		2	2	28				150	30	[139]
	20				4	40					95	
											330	
E	20	75			2	25	30	25			100	[141]
					5	50						
					7							
E	40	50		2.1	6		60	50				[142]
	10						20					
E	25			1.6			100					[143]
E	15	63	100	2.4	30	5,6 - 37	90	60				[144]
S	20	60		1.4	1	40	30	30	40	150		[145]
S	20	60		1.2			30		40			[146]
	10			1			20		80			
S	15	90					20					[14]
S	20-40			2.4			30-100					[147]
S	9			1.1			28	1.1	15			[148]
E	32	60			3		60			145	328	[134]
					6							
					9							
S	10	50	50	1.3	29		25	50	3*Lgate			[149]
	20	120					37					
							90					
E	20	65	150	1.6	1	55	30					[150]

Table 3.1 *Some simulated and experimental geometrical dimensions (nm) for MuGFETs, from published papers*

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