Universitat Autònoma de Barcelona

Escola d'Enginyeria

Departament d'Enginyeria Electrònica

Variability and reliability at the nanoscale of gate dielectrics of MOS devices and graphene based structures

A dissertation submitted by Albin Bayerl
in fulfillment of the requirements
for the degree of Doctor
in Electronic Engineering

Supervised by Dr. Marc Porti i Pujal
Bellaterra, September 2013

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Dr. Marc Porti i Pujal, associate professor at the Electronic Engineering Department of the Autonomous University of Barcelona,

herewith certifies, that the dissertation entitled

Variability and reliability at the nanoscale of gate dielectrics of MOS devices and graphene based structures

submitted by Albin Bayerl to the School of Engineering in fulfillment of the requirements for the Degree of Doctor in the Electronic Engineering Program, has been performed under his supervision.

Dr. Marc Porti

Bellaterra, November 22, 2013

To my wife Helen
and my family

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After 3 years of intense studies the moment has come to finalize this chapter of life. Moreover, it is the time to recognize the support from many colleagues I have received. Without their contribution this thesis would not have been possible.

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Index

Publications related to this thesis

Compendium of publications included in this thesis

1) A. Bayerl, M. Lanza, M. Porti, M. Nafría, Senior Member, IEEE, X. Aymerich, F. Campabadal and G. Benstetter, „Nanoscale and Device Level Gate Conduction Variability of High-k Dielectrics-Based Metal-Oxide-Semiconductor Structures“, IEEE Transactions on Device and Materials Reliability, vol. 11, no. 3, pp. 495-501, 2011.

2) A. Bayerl, M. Lanza, M. Porti, F. Campabadal, M. Nafría, X. Aymerich and G. Benstetter, „Reliability and gate conduction variability of HfO_2-based MOS devices: a combined nanoscale and device level study“, Microelectronic Engineering, vol. 88, no. 7, pp. 1334-1337, 2011.

3) M. Lanza, A. Bayerl, T. Gao, M. Porti, M. Nafria, G. Y. Jing, Y. F. Zhang, Z. F. Liu, and H. L. Duan, „Graphene-coated Atomic Force Microscope tips for nanoscale electrical characterization“, Advanced Materials, vol. 25, pp. 1440-1444, 2013.

4) A. Bayerl, M. Lanza, L. Aguilera, M. Porti, M. Nafría, X. Aymerich, „Nanoscale and device level electrical behavior of annealed ALD Hf-based gate oxide stacks grown with different precursors”, Microelectronics Reliability, vol. 53, no. 6, pp. 867–871, 2013.

Other publications included this thesis

5) A. Bayerl, M. Porti, J. Martin-Martínez, M. B. Gonzalez, R. Rodriguez, V. Velayudhan, E.Amat, M. Nafria, X. Aymerich, E. Simoen, „A Conductive AFM nanoscale study of channel hot-carriers degradation in MOSFETs”, IEEE International Reliability Physics Symposium, pp. 5D.4.1-5D.4.6, 2013.

6) M. Lanza, Y. Wang, A. Bayerl, T. Gao, M. Porti, M. Nafria, H. Liang, G. Jing, Z. Liu, Y. Zhang, H. Duan, „Tuning graphene morphology by substrate towards wrinkle-free devices: experiment and simulation”, Journal of Applied Physics, vol. 113, no. 10, art. no. 104301, 2013.

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8) V. Iglesias, M. Lanza, K. Zhang, A. Bayerl, M. Porti, M. Nafría, X. Aymerich, G. Benstetter, Z. Y. Shen, and G. Bersuker, „Degradation of polycrystalline HfO_2-based gate dielectrics under nanoscale electrical stress“, Applied Physics Letters, vol. 99, no. 10, art. no. 103510, 2011.

9) A. Fontserè, A. Pérez-Tomás, M. Placidi, J. Llobet, N. Baron, S. Chenot, Y. Cordier, J.C. Moreno, P. M. Gammon, M. R. Jennings, M. Porti, A. Bayerl, M. Lanza, and M. Nafría, "Micro and nano analysis of 0.2 Ω mm Ti/Al/Ni/Au ohmic contact to AlGaN/GaN", Applied Physics Letters, vol. 99, no. 21, art. no. 213504, 2011.

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Contributions to conferences

1) A. Bayerl, V. Iglesias, M. Lanza, M. Porti, M. Nafría and X. Aymerich, „High-k dielectric polycrystallization effects on the nanoscale electrical properties of MOS structures", Proceedings of the 8th Spanish Conference on Electron Devices, February 8-11th of 2011, Palma de Mallorca (Spain).

2) V. Iglesias, A. Bayerl, M. Lanza, M.Porti, M.Nafria, X.Aymerich, „Impact of the polycrystallization of high-k dielectrics on the nanoscale and device level electrical properties of MOS capacitors", Proceedings of the ImageNano Conference, April 11-14th of 2011, Bilbao (Spain).

3) M. Lanza, A. Bayerl, V. Iglesias, M. Porti, J. Martin-Martinez, R. Rodriguez, M. Nafria, X. Aymerich, "Nanoscale electrical properties and variability of amorphous and polycrystalline thin high-k gate stacks in MOS devices", 6th International Conference on Technological Advances of Thin Films & Surface Coatings (ThinFilms2012), Invited Oral, 2012.

4) M. Lanza, A. Bayerl, V. Iglesias, H. Duan, G. Bersuker, M. Porti, M. Nafria, X. Aymerich, „Nanoscale characterization of high-k insulators for future memory devices“, 2nd Annual world congress of Nanoscience and Nanotechnology 2012 (Nano S&T2012). Qingdao (China), 24-26 October 2012.

5) M. Lanza, A. Bayerl, M. Porti, M. Nafria, X. Aymerich, Y. Wang, T. Gao, H. Liang, G. Jing, Z. Liu, Y. Zhang, H. Duan, „Nanoscale morphology of graphene on different substrates”, Proceedings of the 8th Spanish Conference on Electron Devices, February 12-14th of 2013, Valladolid (Spain).

6) M. Lanza, A. Bayerl, M. Porti, M. Nafria, X. Aymerich, „Improved Nanoscale Electrical Characterization with Graphene-Coated Atomic Force Microscope Tips“, ImagineNano 2013, 23. - 26. April, Bilbao (Spain).

Patents

1) M. Lanza, A. Bayerl, M. Porti, M. Nafria, H. Duan, „Conductive Atomic Force Microscope tips coated with Graphene”, European patent, reference numbers: GB1222559.5 (14/12/2012), EP12382504.4 (14/12/2012).

Presentation

During the last decades, electronics has paved its way in virtually every corner of human life. The electronic revolution became such an integral part of our daily life that everything is related in some way to electronics. Milestones such as the discovery of charge carriers in the early 80s of the 19^{th} century initiated an invention chain never seen before. When talking about the technological progress, it is often associated with the computer. Invented in 1938 by the german engineer Conrad Zuse, it was defined by himself as a "mechanical brain" as it consisted exclusively of mechanical parts. In a subsequent approach, in 1942, he replaced central parts by mechanic relays, which are electrically controlled mechanical switches. Of course, this invention was later redesigned including different electronic devices, such as the electron tubes. As a result, the first electronic computer was the ENIAC, in 1947, which was able to perform calculations a lot faster. However, a great disadvantage of such computer in this era was the space and the energy needed to operate, since they were very huge machines, which occupied entire rooms and halls. But the missing link between the computer of the late 1940s and the computer we nowadays are accustomed to use for our needs implies one more revolutionary concept – the integrated circuit.

An integrated circuit is a circuit on one single substrate. The first entirely integrated circuit, fabricated in 1958 by Jack Kilby, consisted of two bipolar transistors on a germanium substrate. Inspired by this invention, Gordon Moore, founder of the Intel corporation, in 1975 predicted a doubling of the number of elements (basically the MOSFET – Metal Oxide Semiconductor Field Effect Transistor) integrated on one single chip every two years. A very tempting aspect of device shrinking is that it provides a higher operation speed due to lower transition times and the MOSFET enabled to follow this dictum easily. But, nowadays, miniaturization is reaching the limits set by physics itself, leading to new reliability and variability issues affecting, for example the gate oxide of the MOSFET. To solve such problems, a substantial change in the device material composition or configuration seems unavoidable. The introduction of high-k dielectrics as replacement of SiO_2 as the gate dielectric is considered to be a highly interesting approach. This would allow using thicker gate stacks and, therefore, reducing leakage currents. However, the introduction of these dielectrics leads to new challenges. Among them, the most important are a) high density of intrinsic defects, b) poor interaction with the gate electrode, c) unavoidable formation of a SiO_2 layer at the interface with the Silicon substrate, d) poor carrier's mobility at the conductive cannel due to scattering phonons, and e) changes in the morphology depending on the manufacturing process (such as crystallization) which can alter their electrical properties, among others.

One completely new material is graphene, a mono-atomic layer of carbon arranged in a honeycomb lattice. In 2004, when Novoselov and Keim managed to fabricate graphene flakes by a very ingenious and, at the same time, simple method, a great rush on this material was about to begin. Since then, much investigation has been done. Graphene shows some very astonishing properties, such as an extremely high mobility of charge carriers. However, the absence of a bandgap makes difficult its applications for digital circuits. In particular, when integrated into device technology as electrodes, it offers a very low contact resistance and high surface area. As a conductive channel in transistors it can make them operated at higher frequencies, owing to the higher mobility of the

charge carriers. However, before incorporating it in present technologies, much work has to be done, especially that related to the growth of large area flakes free of defects, which can impoverish its electronic properties. Many of the problems associated with high-k dielectrics, such as polycrystallization and the failure mechanisms that affect the gate oxide reliability, and with graphene, such as defects present in graphene layers which can impoverish their electronic properties, are phenomena that have been found to originate from effects occurring at the nanoscale. In order to understand these effects they have to be studied with instrumentation that provides a nanometric resolution. Techniques that recently have been used to perform such analyses are the Scanning Probe based microscopes. Among them, especially when studying the electrical properties and reliability of gate dielectrics, the Conductive Atomic Force Microscope (CAFM) has been the most used until now. This technique is capable to obtain simultaneously and independently topographical and electrical information at the nanoscale. So, in this thesis, CAFM will be used to study the variability and reliability of gate stacks and the properties of graphene layers for nanoelectronic applications.

In the first chapter of this thesis, the MOSFET transistor and an overview of the implications of ongoing device shrinking will be given. Possible alternatives to allow the scaling down such as the introduction of high-k dielectrics and the potential of graphene for nanoelectronic applications are also explained.

The second chapter will be devoted to describe in more detail the AFM (Atomic Force Microscope), which has been used to investigate the electrical properties of different materials at the nanoscale.

In the third chapter, different fabrication conditions of HfO_2 layers based devices, such as the annealing temperature (and polycrystallization), the thickness and the precursor with which it was grown will be investigated at the nanoscale. The influence of an electrical stress at the device level is also studied.

In chapter 4, the impact of different electrical stresses on the nanoscale electrical properties of ultra-thin SiON based MOSFETs is investigated. Using a CAFM, the gate oxide has been analyzed after a BTI (Bias Temperature Instability) and CHC (Channel Hot Carriers) stress. Since with the CAFM tip very small areas can be studied, the degradation induced at different regions of the gate oxide along the channel was analyzed.

Chapter 5 describes the invention of a completely new approach to significantly improve the intrinsic mechanical and electrical properties of commercially available CAFM tips by coating them with graphene.

Finally, in chapter 6, the usability of graphene for nanoelectronic applications will be investigated at the nanoscale. One aspect that will be analyzed is the presence of corrugations, wrinkles and grain boundaries, which are shown to increase the device-to-device variability. The impact of the substrate on which graphene is transferred to will be also studied. Since graphene has been recently started to be used as top electrode in memory devices, in the second part of this chapter, the variability and reliability of Graphene-Insulating-Semiconductor (GIS) structures based on HfO_2 will be preliminarily investigated.

Chapter 1: Introduction

One of the main, more common and important device in the silicon-based integrated circuits is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). It is present in almost every electronic set having, therefore, a vital position in the microelectronics field. In this chapter, first, the basic concepts of a MOSFET are introduced as well as the consequences of the continuous shrinking of its dimensions and the possible alternatives to avoid them, such as the introduction of new materials as high-k dielectrics. The variability and failure mechanisms associated to gate dielectrics, such as dielectric breakdown (BD), Bias Temperature Instability (BTI) and Channel Hot Carrier (CHC) are also presented. Graphene and its applications to nanoelectronics are briefly described in this chapter as well. Finally, the attention will be centered to the different characterization techniques normally used to electrically characterize MOS devices: those that can reach a nanometer resolution, such as the Conductive Atomic Force Microscope (CAFM), and those traditionally used to obtain the global electrical properties of MOSFETs, the so-called “Standard Characterization Techniques”.

1.1 The MOSFET

The MOSFET is one of the fundamental devices in modern circuit technology. It is based on a traditional Metal Oxide Semiconductor (MOS) structure (Fig. 1.1a), with two electrodes, gate (G) and bulk (B), and an insulator (gate oxide) between them. The metal serves as gate contact although it has also been implemented during many years by polysilicon. In fact, the introduction of polysilicon as contact material brought the advantage that it does not react with the dielectric (SiO_2). The insulating layer between gate and substrate traditionally was SiO_2 which, due to continuous device scaling, has been replaced by nitrided Silicon oxides (SiON) and high-k dielectrics [Degraeve 08] (see section 1.3). The substrate can be a silicon substrate with P or N doping, leading to an n- or p-MOSFET, respectively. Regarding the substrate, modifications such as the introduction of Germanium or the use of III/V semiconductors as promising materials are being investigated in order to increase its mobility [Swaminanthan 10, Kim 10].

When a potential difference is applied between gate and bulk electrodes (V_{GB}) of a MOS structure (Fig. 1.1a), the distribution of charge carriers in the substrate can be modified. Depending on V_{GB}, three operation modes can be distinguished [Barbottin 86]. Fig. 1.2 describes the three operation modes for a p-type Silicon substrate MOS capacitor:

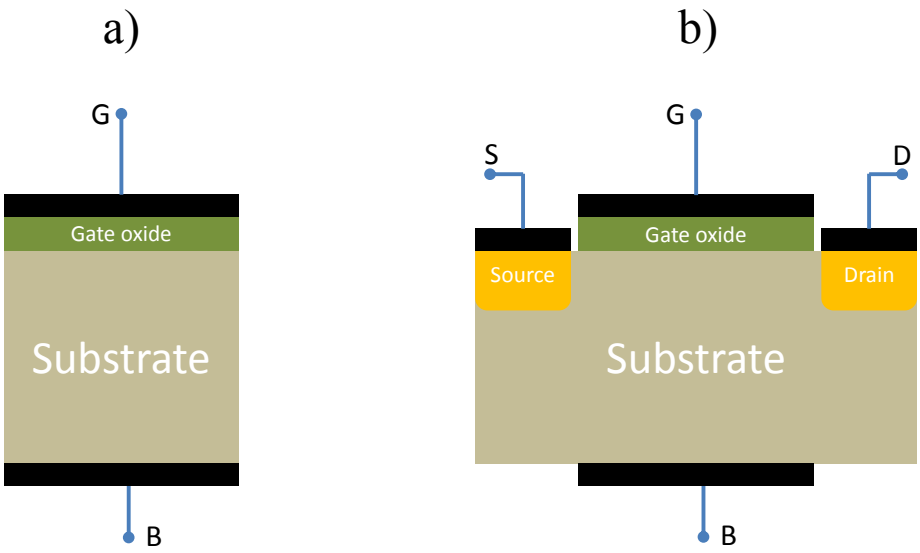

Figure 1.1. Schematic of a (a) MOS structure and (b), MOSFET.

a) When applying a negative gate voltage, e. g. $V_{GB} < 0V$, positive charge carriers are attracted to the substrate/gate dielectric interface region (Fig. 1.2a). Therefore, the hole concentration in this region (majority carriers) is higher than in the rest of the substrate. This working regime is called *accumulation*.

b) Applying a positive voltage between gate and bulk, e. g. $V_{GB} > 0V$, positive charge carriers are repelled from the substrate/dielectric interface region into the substrate. A space charge region of fixed and ionized ions is formed leading to what is called *depletion* regime (Fig. 1.2b).

c) If V_{GB} is high enough (V_{GB} >> 0V), free electrons are attracted to the insulator/semiconductor interface. Therefore, the density of negative charge close to the interface exceeds the density of holes and turns the semiconductor into n-type. In this mode, called *inversion* (Fig. 1.2c), a conductive channel of electrons is formed at the substrate/insulator interface. The minimum voltage for V_{GB} to enter in this working mode is called threshold voltage, V_{TH}.

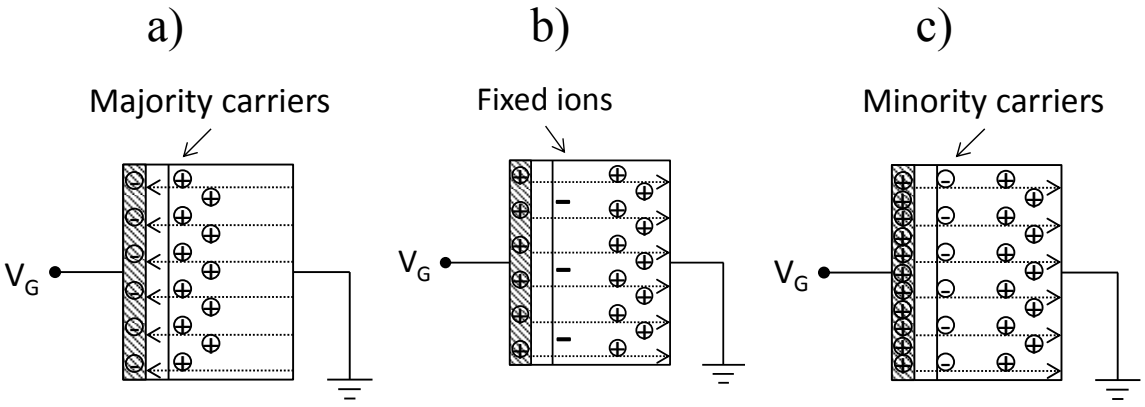

Figure 1.2. Schematic of the charge movement in a MOS structure (p-type substrate) for each of the different operating modes: (a) accumulation, (b) depletion and (c) inversion.

An analogue behavior can be described for a MOS structure with an n-type substrate, where electrons are the majority charge carriers. The operation modes described above are, therefore, reached by changing polarities of the bias. The behavior of the MOS structure described above corresponds to the ideal situation, where no charge trapping is considered in the oxide and a gate-semiconductor work function difference of value zero is supposed. The work function of a material is defined as the energy needed by a charge carrier to move from the Fermi to vacuum level. In order to obtain flat band conditions in a non-ideal MOS capacitor, a voltage has to be added for compensating the workfunction difference across the MOS structure and the presence of charge in the oxide.

To explain the work principle of a MOSFET, a transistor with a p-type substrate will be considered. A MOSFET is a 4-terminal device that consists of a MOS structure (Fig. 1.1a) and two additional terminals (Fig. 1.1b) called source (S) and drain (D), being S and B normally connected. When $V_{GS} < V_{TH}$, a channel has not been formed. Therefore, there is no conduction between source (S) and drain (D) even when $V_{DS} \neq 0V$. This mode is called *subthreshold* regime. The inversion channel is formed when the applied gate voltage exceeds the threshold voltage, $V_{GS} > V_{TH}$. In that case, for small V_{DS} voltages, that is, when $V_{GS} > V_{TH}$ and $V_{DS} < (V_{GS} - V_{TH})$, the current flowing between source and drain, I_{DS}, can be approximated by the following expression, which is the so-called linear regime (Fig. 1.3):

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right) \qquad \text{(Eq. 1.1)}$$

Being μ_n the mobility, C_{ox} the MOS structure capacitance and W and L the width and length of the channel. Further incrementing V_{DS} ($V_{DS} > V_{GS}-V_{TH}$) leads to the saturation mode, in which I_{DS} does not depend on V_{DS} but only on V_{GS} (Fig. 1.3). The onset of this mode is called "pinch-off".

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} \qquad \text{(Eq. 1.2)}$$

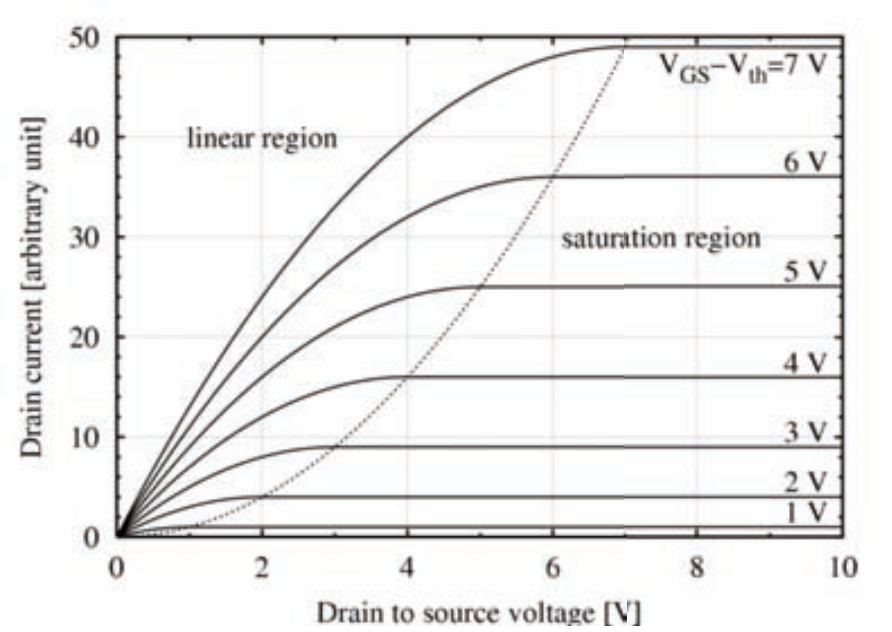

Figure 1.3. I_{DS}-V_{DS} characteristics of a MOSFET for different gate voltages (V_{DS}) [Wiki].

1.2 Scaling of the device dimensions

Moore's law

The success of the semiconductor industry is based on the continuous improvement of integrated circuit technology in terms of performance. As the MOSFET is the key component of contemporary circuitry, desired improvements are achieved by reducing its dimensions. Generally, the reduction of device dimensions makes possible the integration of more transistors on a single chip leading to a higher speed and lower production costs. "Moore's law" suggests an exponential increase in the number of transistors integrated on a chip [Moore 65] (Fig. 1.4). In order to compare, the 4004 processor (1971) was made up of 2250 integrated transistors from the 10 µm technology node and was operated at a clock frequency of ~100kHz. The Intel Pentium4 processor, introduced in 2002, already integrated about 50 million transistors from the 0.13 µm technology, and ran at frequencies of up to 2GHz.

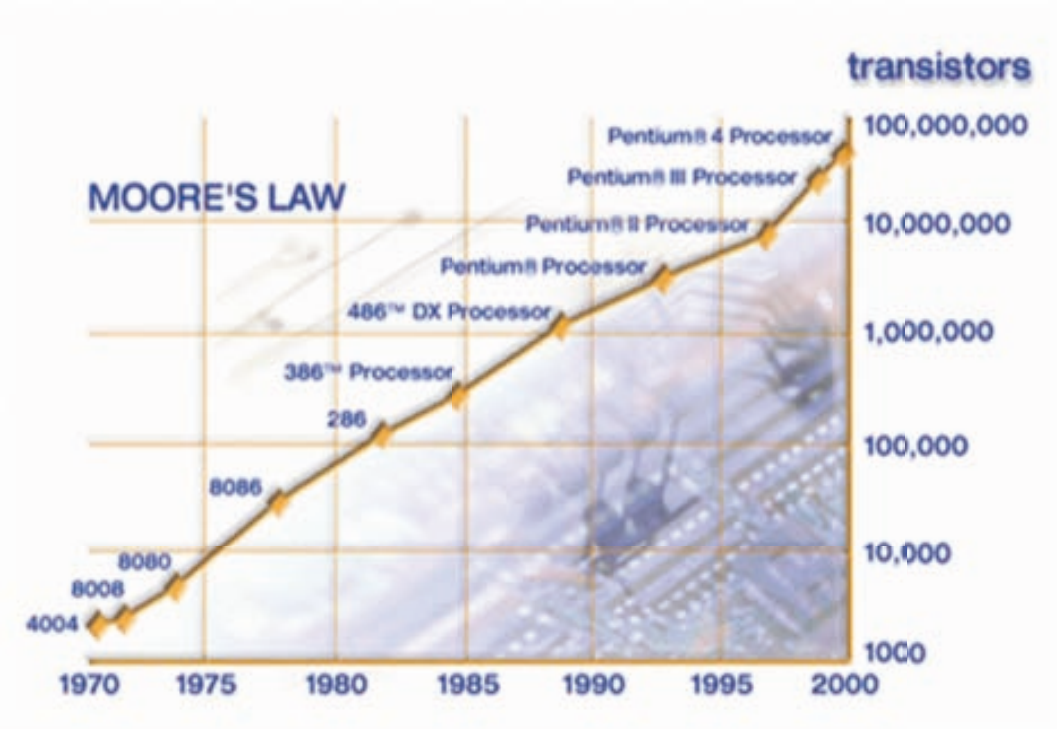

Figure 1.4. Number of transistors integrated in Intel's microprocessors as a function of the production year [Intel]. The exponential increase of such number is in agreement with the Moore's law prediction.

The reduction of the transistor size doesn't only affect the lateral but also the vertical dimensions and, in particular, the gate oxide thickness. One of the basic elements that allowed the successful MOSFET scaling is the excellent properties of the SiO_2. On one hand, because it can be grown thermally on a silicon substrate with good control of thickness and uniformity, and forms a very stable oxide/substrate interface with low density of defects and high breakdown fields. On the other hand, it presents great thermal and chemical stability, which is necessary for the transistor fabrication processes that include annealing treatment at elevated temperatures. Furthermore, its band gap of about 9eV gives outstanding electrical isolation properties. These properties gave rise to the production of MOSFETs with dielectric layers down to thicknesses of 1.5nm [Timp 99, Chau 00]. However, further shrinking of the SiO_2 layer thickness leads to undesired effects.

Limits of SiO_2 scaling

It has to be pointed out that the band gap of an insulator is not formed completely below a thickness of ~7Å – which actually establishes the physical limit for the thickness scaling of SiO_2 layers [Muller 99]. Moreover, even for oxide thicknesses below 1.5nm other problems raise, such as an excess of tunneling leakage current flowing through the MOS structure. In thin SiO_2 layers, although the bandgap is very large, charge carriers can flow through the gate dielectric by quantum tunneling effects [Depas 95, Lo 97]. For oxides typically below 3nm, this mechanism involves the tunneling of charge carriers through a trapezoidal energy barrier (Fig. 1.5a), which is called Direct Tunneling (DT). For thicker oxides, charge carriers are injected from the conduction

band of the gate to the conduction band of the oxide, leading to the Fowler-Nordheim Tunneling (FNT). The tunneling probability increases exponentially with decreasing the thickness of the SiO_2 layer [Depas 95]. This leads to a significant increase of the leakage current flowing through the gate (Fig. 1.5b) and, therefore, of the power consumption. The leakage current specifications from the International Technology Roadmap for Semiconductors (ITRS) are represented in Fig. 1.5b by shaded areas, both for high performance logic and low operating power applications [ITRS 01]. This figure clearly shows that the SiO_2 layer thickness scaling is limited by the leakage current specifications, typically to ~2.3nm for low operating power circuits and 1.5nm for high performance circuits. However, as illustrated in table 1.1 (extracted from the specifications of the latest ITRS) [ITRS 01], the following generations of MOSFETs would require equivalent oxide thicknesses (EOT) below 1.5 nm, for the high performance logic applications (microprocessors) and low operating power applications (wireless communication).

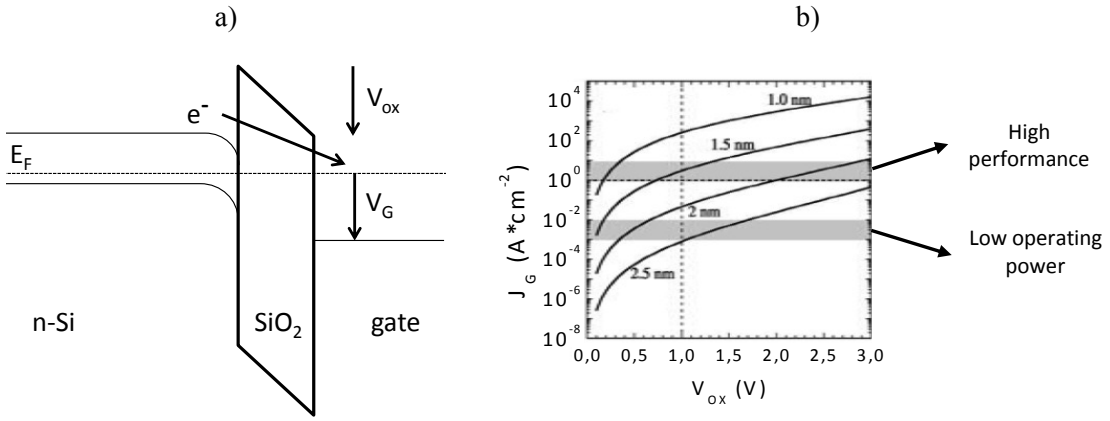

Figure 1.5. (a) Schematic energy band diagram of a biased n-Si/SiO_2/metal gate structure, showing direct tunneling of charge carriers from the Si substrate to the gate. E_F is the Fermi level of the semiconductor, V_{ox} the potential drop in the SiO_2 layer and V_G the applied gate voltage. (b) Simulated tunneling current through a metal–oxide–semiconductor structure as a function of the potential drop in the gate oxide, V_{ox}, for different SiO_2 gate layer thicknesses [Wong 06]. Shaded areas represent the maximum leakage current specified by the ITRS for high performance and low operating power applications, respectively.

Therefore, SiO_2 cannot be used as gate dielectric for the 80nm (and below) technologies. Actually, nitrided silicon dioxide was already used as gate dielectric in some high performance technologies. Despite high power consumption, another issue related to gate dielectric thickness scaling concerns reliability aspects. During the operation of MOSFETs in integrated circuits, the presence of high leakage currents through the gate stack results in the generation of defects in the dielectric layer and at the Si/gate dielectric interface [Harari 78, DiMaria 93, DiMaria 95], leading to different failure modes that can make the MOSFET inoperative.

Table 1.1. EOT for the future generations of Si-based MOSFET technologies, including high performance logic applications and low operating power applications.

Technology (nm)	Year	EOT (nm)	
		High performance logic	Low operating power logic
130	2002	1.2–1.5	1.8–2.2
107	2003	1.1–1.4	1.6–2.0
90	2004	0.9–1.4	1.4–1.8
80	2005	0.8–1.3	1.2–1.6
70	2006	0.7–1.2	1.1–1.5
65	2007	0.6–1.1	1.0–1.4
50	2010	0.5–0.8	0.8–1.2
25	2016	0.4-0.5	0.6-1.0

1.3 Alternative gate dielectrics

One alternative to partially solve the excessive leakage current through gate oxides consists in the use of high-k dielectrics [Ribes 05]. From an electrical point of view, the MOS structure behaves like a parallel plate capacitor. The capacitance C_{ox} of this parallel plate capacitor is given by

$$C_{ox} = \frac{A\varepsilon_r \varepsilon_0}{t_{ox}} \qquad \text{(Eq. 1.3)}$$

where A is the area of the capacitor, ε_r the relative dielectric constant of the material (3.9 for SiO_2), ε_0 the permittivity of vacuum and t_{ox} the gate oxide thickness. From the equation 1.3, decreasing t_{ox} lets raise the capacitance of the structure, leading to an increment in the number of charges in the channel for a fixed value of V_G and increasing the current drive capacity of a MOSFET (see Eq. 1.1 and 1.2). However, that also increases the leakage current and, therefore, the power consumption, and impoverishes the device reliability. A different way of increasing the capacitance is using an insulator with a higher dielectric constant than SiO_2. This permits to fabricate structures with a thicker gate dielectric layer, reducing the leakage current.

The equivalent oxide thickness (EOT) of a material is given by the thickness of the SiO_2 layer that would be needed to obtain the same capacitance than that using a high-k material with a thickness $t_{high\text{-}k}$

$$EOT_{high-k} = \frac{K_{SiO_2}\, t_{high-k}}{K_{high-k}} \qquad \text{(Eq. 1.4)}$$

where t_{high-k} and K_{high-k} are the thickness and relative dielectric constant of the high-k material, respectively. As an example, using ZrO_2 as gate dielectric would allow us to use a 5.1nm thick layer of that material in order to achieve a capacitance equivalent to a 1 nm thick SiO_2 layer. However, when a high-k metal oxide like ZrO_2 or HfO_2 is deposited on a Si substrate, an ultrathin low-k interfacial layer is formed at the silicon interface, as illustrated in Fig. 1.6 [Choi 05]. This interfacial layer either grows during the deposition of the high-k dielectric or during post-deposition thermal treatment. Furthermore, another low-k layer can be formed at the high-k dielectric/metal gate interface. Since an additional low-k interfacial layer increases the EOT of the gate stack that should thus be as thin as possible.

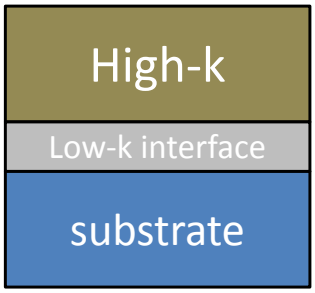

Figure 1.6. Schematic illustration of a MOS structure with a high-k gate stack, formed by a low-k interfacial layer (normally SiO_2) and a high-k dielectric layer.

Despite the higher K value of the high-k dielectrics, the material that could potentially replace SiO_2 as gate dielectric in advanced CMOS technologies should also satisfy a long list of other requirements [Wilk 01], e.g.:

- good thermal stability in contact with Si, preventing the formation of a thick SiO_x interfacial layer and the formation of silicide layers;
- low density of intrinsic defects at the Si/dielectric interface and in the bulk of the material, providing high mobility of charge carriers in the channel and sufficient gate dielectric lifetime;
- a sufficiently large energy band gap, providing high energy barriers at the Si/dielectric and metal gate/dielectric interfaces, in order to reduce the leakage current flowing through the structure;
- material's compatibility with CMOS processing, as, for example, high thermal budgets, which can lead to the polycrystallization of the high-k dielectric.

From all these considerations, the selection of a material as a gate dielectric is a compromise considering various factors. As an example, permittivities of the different studied materials (Table 1.2) can range from values only slightly larger than that of SiO_2 ($\varepsilon_r < 10$) over a moderate permittivity ($\varepsilon_r = 15$-30) for some binary and ternary oxides to oxides and ferroelectric materials with very high permittivity (TiO_2: $\varepsilon_r = 80$). However, none of the materials listed in table 1.2 meets all the requirements describe above. Moreover, for the most high-k dielectrics, the size of the band gap E_g behaves inversely proportional to its permittivity, so that the reduction of leakage current in thicker dielectrics is nullified by the lower barrier [Robertson 00]. Despite that, at present HfO_2 has turned out to be the most auspicious candidate for replacing SiO_2. Its capability of being integrated into existing device production was demonstrated about 6 years ago. Since 2007, a Hf-based Dielectric was integrated in products of the 45 nm technology

generation by chipmaker Intel [Mistry 07]. Other companies such as AMD / Global Foundries and Samsung followed in 2010 with the introduction of Hf-based dielectrics in products of the 32-nm technology generation [Jotwani 11].

Table 1.2. Examples of high-k materials studied in the literature for the potential replacement of SiO_2 as advanced gate dielectrics [Gupta 12].

Dielectric material	Dielectric constant
Al_2O_3	~9
Yb_2O_3	~11
La_2O_3	~30
HfO_2	~25
TiO_2	~60

However, despite that, there are still several issues that must be further investigated as the impact of polycrystallization and reliability of high-k based gate dielectrics. Regarding polycrystallization, it is worth mentioning that high-k materials are existent in three different phases: poly-crystalline, amorphous and epitaxial-crystalline. Although deposition of materials via epitaxial processes yields better quality in terms of interface properties, the cost of fabrication is prohibitively large for being integrated into mass production lines due to its complexity. Therefore, the trend in selecting materials heads onto the amorphous phase, which is advantageous from different points of view, such as the compatibility with already existing device fabrication technology, a low amount of interfacial defects compared with the polycrystalline phase, and the possibility of tuning its properties via changing its composition [Lanza 07]. However, in amorphous high-k dielectrics, polycrystallization can be induced due to high deposition temperatures in combination with a low thermal budget or due to a post-deposition thermal annealing. Such polycrystallization can change the gate oxide electrical properties, which can depend on the material analyzed. As an example, in [Iglesias 11], a significant contribution of grain boundaries to the measured current is observed on an HfO_2 based oxide, whereas other works [Kim 04] come to a different conclusion. Therefore, due to the fact that polycrystallization is an undesired effect that affects the electrical properties of the gate stack, a more detailed analysis of this topic is needed, which will be performed in this thesis. How the polycrystallization also affects the gate stack reliability will also be studied.

1.4 Failure mechanisms of gate oxides

Despite the requirements that as-grown high-k dielectrics must fulfill to substitute SiO_2 (see previous section), the reliability of these materials is also critical, since aging mechanisms provoke an impoverishment of the device performance. When a gate oxide is subjected to electrical stress, in general, its insulating properties can gravely be affected, which leads to changes in the desired device behavior. Moreover, the introduction of new materials as high-k dielectrics generally implies greater challenges in terms of reliability, which at the state of its infancy have to be investigated as detailed

as possible. Nevertheless, high-k materials have demonstrated to suffer similar degradation mechanisms to those already known for SiO_2 based technologies, although some of them with different impact on the device performance [Degraeve 08]. Therefore, the knowledge gained on device behavior based on SiO_2 can be partially adopted and maintained. This section is dedicated to briefly introduce some of the most common failure mechanisms in high-k based MOSFETs, as they form a basic part of this thesis. The most important degradation mechanisms in MOSFETs, which will be described in more detail in next sections, are:

- Dielectric breakdown (BD): BD consists in the loss of the dielectric properties of the gate oxide when being exposed to high vertical electric fields.

- The Bias Temperature Instability (BTI): BTI is defined as a shift of the threshold voltage of transistors. This aging mechanism is more pronounced at elevated temperatures and is related to the generation of defects and charge trapping in the gate stack when a gate voltage is applied to the MOS structure. This phenomenon has been observed to be more important in high-k dielectrics than in SiO_2 layers [Degraeve 08, Krishnan 06, Chang 06].

- Channel Hot Carriers (CHC): Charge carriers gain energy when travelling from Source to Drain across the MOSFET channel due to the source-drain electrical field, E_{DS}. The high energy acquired by the carriers due to such a large E_{DS} create e^--h^+ pairs, which can be injected into the gate dielectric, leading to the degradation of the oxide at the Drain region.

In the last decades, BTI became more detrimental than the CHC degradation [Degraeve 08]. Nevertheless, for the recent technology nodes, CHC degradation has acquired a renewed relevance because supply voltage reduction is slowing down, increasing in this way the lateral electric fields in the device. BTI and CHC aging involve the generation of defects at the gate oxide/Si interface and/or oxide bulk, so that several device parameters (threshold voltage and carrier mobility in the channel) shift during the device operation, and that could affect circuit performance [Bravaix 09].

1.4.1 Dielectric Breakdown

Although BD has been studied since more than two decades [Ricco 83, Wolters 86, DiMaria 89, McPherson 98, Bersuker 08, Stathis 10], there is not yet general consensus about how exactly originates from a physical point of view. However, the scientific community widely accepts the so called “percolation model” [Degraeve 98, Raghavan 12], according to which dielectric breakdown is the consequence of a degradation stage of the oxide microstructure [Lombardo 05, DiMaria 93], related to the generation of defects. The oxide degradation induced during an electrical stress can be understood as a random and continuous creation of traps (Fig. 1.7a and 1.7b), leading to energy states in the band gap of the oxide. Such defects facilitate trapping of charges and tunneling of carriers. When the density of defects in the oxide reaches a critical value, a connection of the electrodes through a defect related conduction path is created (Fig. 1.7c), which leads to the oxide breakdown. When BD is triggered, the oxide loses its dielectric properties and a sudden increase of the tunneling current [Suñé 90, Degraeve 96,

Degraeve 99] through the MOS structure is observed. The percolation model also predicts that BD (which is a random phenomenon according to the also random generation of defects) takes place in areas of about $100nm^2$ and is, therefore, highly localized.

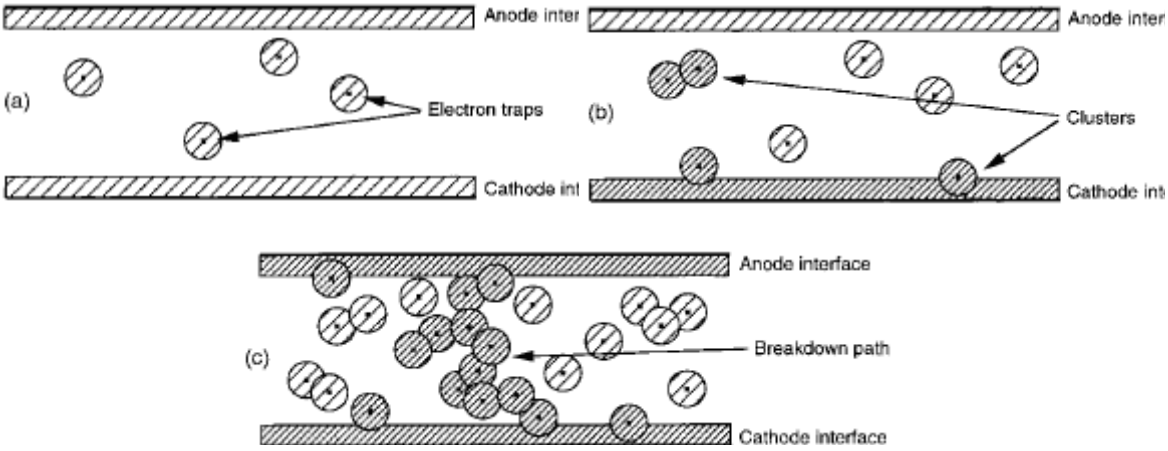

Figure 1.7. Schematics showing the creation of a percolation path [Degraeve 99], where traps are randomly created in the dielectric, (a) and (b), until electrically connects both the anode with the cathode (c).

In oxides of thickness t_{ox}>10nm, the dielectric breakdown was observed as a complete loss of the dielectric insulation properties (hard breakdown, HBD). However, as with the ongoing development of microelectronic technologies, thinner oxides were required leading to new failure mechanisms. For oxide layers in the thickness range between 3 and 7nm, the progressive generation of defects during a high electrical stress (prior to the BD) was detected as an increase of the leakage current at low voltages (stress induced leakage current, SILC) [Jahan 99]. In thicker oxides, trapping charge at the generated defects becomes dominant while in thinner oxides, SILC is masked by Direct Tunneling. Even in oxides of this range (between 3 and 7nm), SILC can be generally only measured at low fields, since at high electric fields it is masked by Fowler-Nordheim Tunneling (FNT) [DiMaria 95].

In the sub-5nm oxide thickness range, less severe failure modes appear, such as soft breakdown (SBD) and progressive breakdown (PBD) [Monsieur 02]. The analysis of these new failure modes is especially important since they lead to different breakdown hardness. Soft Breakdown (SBD) [Okada 94, Lee 94] and Hard breakdown (HBD) differ in their post breakdown current level, which can be some orders of magnitude smaller for SBD. Moreover, Miranda et al. [Miranda 98] observed that the variations in the tunneling current observed during SBD are related to instabilities in ON/OFF states of the different conduction paths created during degradation, which is the reason why SBD can occur more than once during a single stress.

Finally, dielectrics with a t_{ox} < 2.5nm can show an accelerated raise of the tunneling current through the oxide before HBD is reached, named Progressive Breakdown (PBD) [Suñé 06, Monsieur 02, Linder 02]. This failure mode corresponds to the same phenomenon than SBD and HBD, but at different time scales, where a reduced stack

thickness leads to a smaller dissipation rate of energy when a percolation path is formed [Monsieur 01]. Fig. 1.8 shows the different current levels measured on MOS structures after SILC, SBD and HBD events, compared to those registered on a fresh SiO_2 based MOS device (FN current).

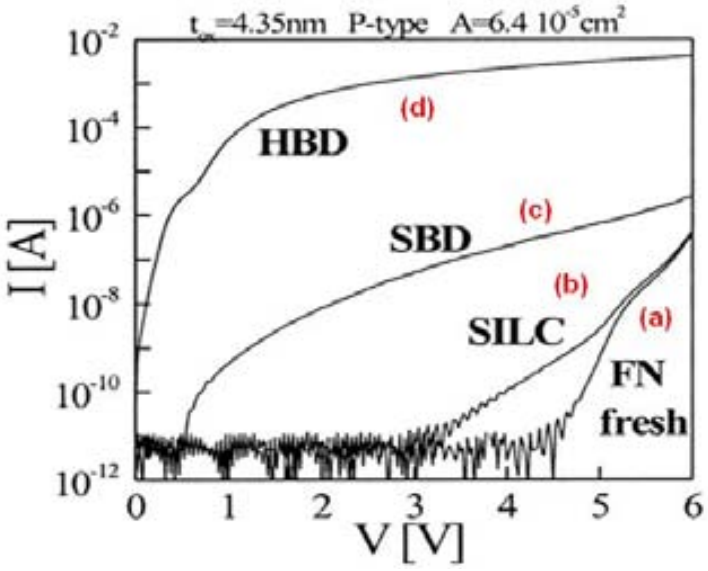

Figure 1.8. Typical I-V curves measured on a MOS structure after applying ramped voltage stresses in a thin SiO_2 stack, showing (a) Fowler-Nordheim behavior of a fresh oxide, (b), Stress Induced Leakage Currents (SILC), (c) Soft-Breakdown (SBD) and (d), Hard-Breakdown (HBD) [Miranda 98].

Due to its random nature, BD must be described from a statistical point of view. In this sense, gate oxide breakdown is recognized as a statistical process which is normally characterized by a Weibull distribution:

$$F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \qquad \text{(Eq. 1.5)}$$

Where $F(t)$ is the cumulative failure, t is the random variable, β is the shape parameter (called Weibull slope) that indicates the data dispersion, and η is the scale factor (time for a 63% probability of BD occurrence). Such distributions are normally written as:

$$ln(-\ln(1 - F(t))) = \beta * \ln(t) - \beta * \ln(\eta) \qquad \text{(Eq. 1.6)}$$

Note that when plotting ln[-ln(1-F(t))] as function of ln(t), the plot follows a linear behavior from which β and η can be easily extracted. In Fig. 1.9, typical Weibull plots of the time-to-breakdown (t_{BD}) distributions for SiO_2 layers with different thickness are shown [Wu 05].

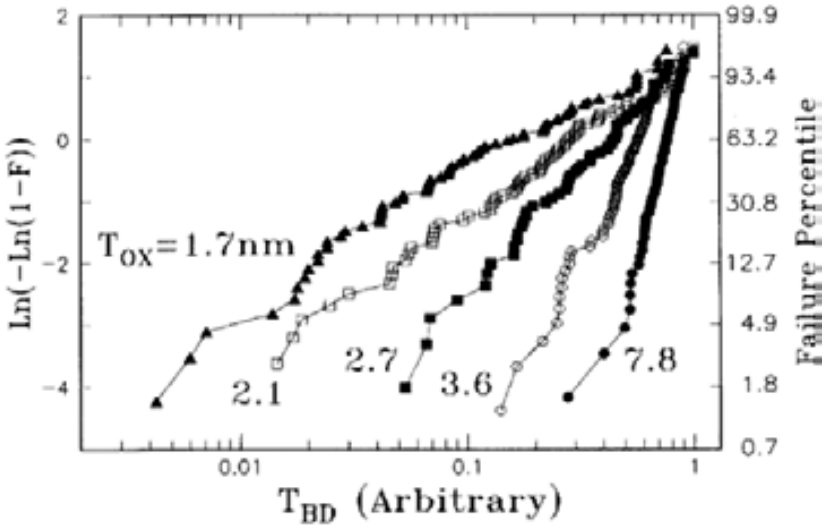

Figure 1.9: Typical normalized t_{BD} distributions for different oxide thicknesses [Wu 05]

1.4.2 Bias Temperature Instability

The Bias Temperature Instability (BTI) [Seo 10] is the increase in the absolute value of the threshold voltage of a transistor when a given voltage is applied to the gate and all other terminals are connected to ground. This phenomenon is even more pronounced at elevated temperatures. Depending on the polarity of the voltage applied to the gate one can distinguish between PBTI (Positive Bias Temperature Instability) with $V_G > 0V$ and NBTI (Negative Bias Temperature Instability) when $V_G < 0V$.

In the past, the effects of the NBTI stress have been widely studied in pMOS transistors with gate dielectrics based on both SiO_2 and SiON [La Rosa 97], since they have been considered as one of the most important phenomenon limiting the lifetime of CMOS technology [Kimizuka 00, Fernandez 06]. It is widely accepted that the threshold voltage shift originates from charge trapping at the dielectric/Silicon interface [Aoulaiche 06], which makes the interfacial SiO_2 layer a key factor in controlling the NBTI degradation in high-k based dielectric stacks.

PBTI degradation has not been investigated to such an extent as NBTI, since its effects on devices based on SiO_2 and SiON are much smaller. However, it has been found that on devices based on high-k gate dielectrics, the effects of PBTI and NBTI are comparable [Degraeve 08]. The degradation induced by PBTI stress is mainly due to the generation of charge trapping in the bulk of the high-k layer [Onishi 03]. Hence, in order to minimize the impact of PBTI, metal gates were introduced [Degraeve 08].

As an example of the effects of BTI on the threshold voltage, the time evolution of the variation in threshold voltage (ΔV_{th}) due to NBTI in pMOS transistors is depicted in Figure 1.10 when a constant voltage stress (CVS) at different voltages was applied. An increasing shift of the threshold voltage ΔV_{th} with time and the applied voltage can be observed. For a given voltage, it has been shown that

$$\Delta V_{th} = a * t_{stress}^{b} \qquad \text{(Eq. 1.7)}$$

where 'a' and 'b' are parameters that depend on the design technology, applied electric field and temperature to which the device is exposed.

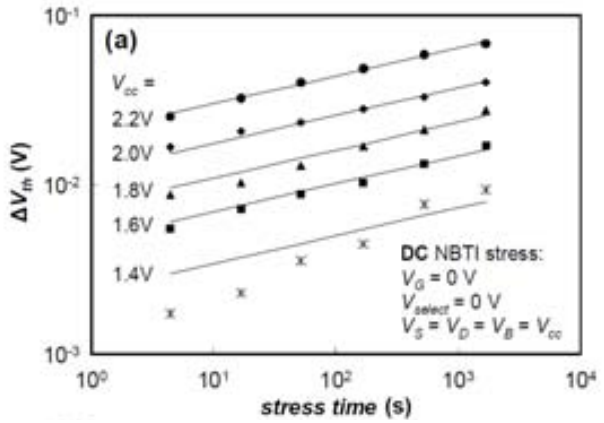

Figure 1.10. Time evolution of the threshold voltage in pMOSFETs for different gate voltages [Fernandez 06].

Another important characteristic of ΔV_{th} is that it depends on the time between the completion of stress and when V_{th} was obtained [Kaczer 07]. In particular, ΔV_{th} decreases as the time of measuring of V_{th} after the end of the stress increases. This indicates that a part of the NBTI damage of the device is recovered, leading to a permanent and a recoverable component of the NBTI effects. As an example, Fig. 1.11 [Degraeve 08] shows that once the NBTI stress has stopped, the variation of the threshold voltage is reduced progressively as the relaxation time increases, tending to a permanent value.

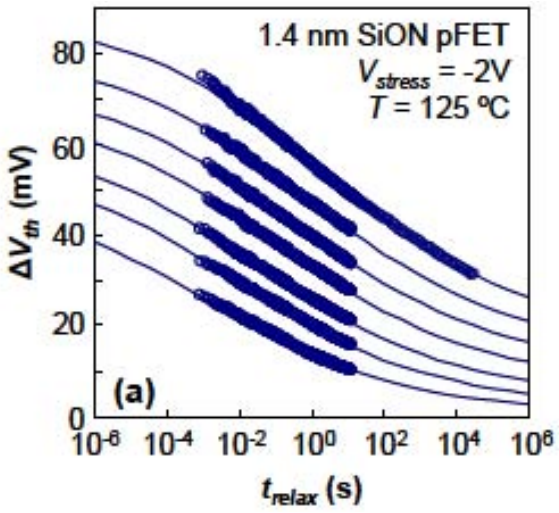

Figure 1.11. ΔV_{th} as a function of relaxation time after application of NBTI stress [Degraeve 08].

The relaxation of the degradation has important implications in the study of BTI as it is difficult to estimate the real damage generated in the device during the stress. For example, when a device is working in dynamic conditions, it is subjected to a process of relaxation when the stress signal is in its low state. Moreover, the process of characterizing the degradation also involves relaxation because it is inevitable that passes a short time interval between the termination of stress and its characterization. To

overcome this issue, several characterization techniques have been developed, such as measurements "On-the-Fly" [Denais 04], where the drain current is measured simultaneously to stress application, or "Ultra-Fast" measurement methods [Reisinger 06], which characterize the BTI degradation from the measurement of one single point in the entire IV curve, minimizing the time relaxation.

1.4.3 Channel-Hot-Carrier degradation

Hot carriers is a phenomenon in solid state electronics that happens when charge carriers (e^- or h^+) gain sufficient energy (by being exposed to an electric field) to create e^--h^+ pairs when impacting with atoms. In a MOSFET, hot carrier degradation occurs when the gate voltage V_{GS} is higher than the threshold voltage V_{th} ($V_{GS} > V_{th}$) and when simultaneously a bias to the drain above its saturation voltage is applied ($V_{DS} > V_{Dsat}$), while the other terminals are connected to ground [Amat 09]. With this configuration, in the region called "pinch-off" of the channel (close to drain), the electric field is very high. Therefore, in an nMOS transistor, for example, when electrons move from the source terminal to the drain (generating the drain current) and reach the pinch-off area, they experience strong accelerations due to the high electric field. Then, a certain percentage of these electrons collide with atoms and due to impact ionization e^--h^+ pairs are generated (Fig. 1.12). Whereas the electrons generated by impact ionization can flow to the drain, gate or source, the holes usually flow towards the substrate, such as shown in Fig. 1.12. Therefore, the measurement of the substrate current (I_{sub}) can be used to estimate the amount of generated e^--h^+, and, consequently, as parameter to monitor the CHC degradation [Acovic 96].

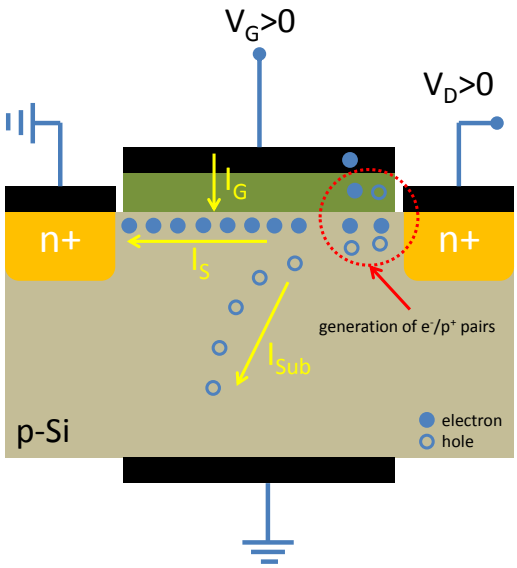

Figure 1.12. Impact ionization in an nMOS transistor.

On the other hand, electrons created by impact ionization gain great energy under the influence of a high electric field in the drain, and some of them are injected into the dielectric, degrading the electrical characteristics of the gate oxide and, therefore, of the device [Martin-Martinez 09]. The effects of this degradation are observed through changes in V_{th}, I_{Dsat} or by generating interfacial states. It has to be noted that the impact ionization mainly occurs in the pinch-off area of the channel and hence the degradation essentially is localized near the drain, which makes the hot carrier degradation a non-

uniform degradation mechanism. In this thesis, the non-homogeneity of CHC degradation of the gate dielectric along the channel will be studied with CAFM in chapter 4.

1.5 Variability

Besides reliability, ultra-scaled technologies suffer from variability issues, which are intrinsically related to device scaling [Asenov 8]. Electrical characteristics of highly scaled MOSFETs may exhibit significant device-to-device variability, which is ultimately associated with the discrete nature of matter and charge and/or to variations in the fabrication process [Borkar 05, Alam 08]. These effects are becoming increasingly important and can have a strong impact on the global electrical device characteristics. As integrated circuits (ICs) usually consist at least of thousands of such devices, it may also affect gravely the overall functionality of entire ICs [Cui 07, Kulkarni 08, Kulkarni 12]. Several variability sources, such as random dopant distribution, line edge roughness, gate oxide roughness and granularity of the poly-Si gate (either during deposition or fabrication), etc., have been identified and investigated [Asenov 08]. However, most of them have been studied from modelling. As modelling results have shown, these variability sources might lead to variations in threshold voltage [Asenov 08]. Some details about these variability sources are the following:

a) *Random dopant distribution* (RDD). This variability source is a consequence of random local variations in the distribution of impurities, introduced by, for example, ionic implantation. RDD can alter the parameters of MOSFETs as its threshold voltage, which can significantly vary from device to device.

b) *Line Edge Roughness* (LER), which correspond to the roughness in the gate of the transistor. These variations are introduced due to intrinsic imperfections of the photolithographic process.

c) Oxide thickness fluctuation and its polycrystallization (see section 1.3) is also another variability source, which can lead to variations in the tunneling current through the gate and threshold voltages. This variability source strongly depends on the fabrication process such as thermal treatment.

However, few reports have addressed these topics since standard electrical characterization techniques can only provide information that is averaged over the entire device gate area of fully processed MOS capacitors or transistors [Degraeve 08, Kittl 09, Pagano 08, Ribes 10]. This confirms the need for advanced characterization methods with high lateral resolution, which can study highly localized electrical processes. The main results obtained until now regarding this point are introduced in section 1.8. In this thesis, scanning probe microscopes and, in particular, Conductive Atomic Force Microscope, (CAFM), have been used to study the homogeneity of the gate oxide electrical properties (see chapter 3) and its impact at device level.

1.6 Graphene for nanoelectronics

The continuous scaling of device dimensions has allowed entering into the 32nm technology node thanks to, for example, the introduction of strain engineering (since the 90nm node) and high-k dielectrics (since the 45nm node). However, to sustain this trend, other technological breakthroughs are expected below the 22nm generation. Some innovative solutions consist in the use of high-mobility materials (as Ge or III/V compounds) as replacement of Si for the device channel [Claeys-Simoen]. Other solutions propose innovations by changing the geometry of the transistor, as FinFETs [Chin 11]. However, there are other options that are being explored, although they are nowadays still far away of being implemented, as graphene based devices [Kim 11]. The discovery of the excellent properties of graphene and the recent possibility to fabricate it has turned this material into a very hot-topic in many fields and, especially, in nanoelectronics. In this section, different methods used to fabricate graphene, as well as the most important properties regarding electronic applications are presented.

1.6.1 Graphene fabrication methods

One of the most surprising and simplest ways to fabricate single-layer graphene flakes was discovered in 2004 by Andre Geim and Kostya Novoselov at Manchester University. They managed to extract single-atom-thick crystallites from bulk graphite [Novoselov 04]. The Manchester researchers transferred graphene onto an isolating substrate (SiO_2) by a method called micromechanical cleavage. With this method, graphene is exfoliated by using a commercially available adhesive tape to repeatedly divide graphite crystals into small pieces. Consecutively, the tape is dissolved in acetone and the one-atomic-layered flakes are sedimented onto a silicon-based substrate. Due to optical interference, the flakes could be identified with an optical microscope. Figure 1.13 shows examples of the prepared films, including single-layer graphene. The main drawback of this method is that only small graphene flakes (~50µm) can be obtained.

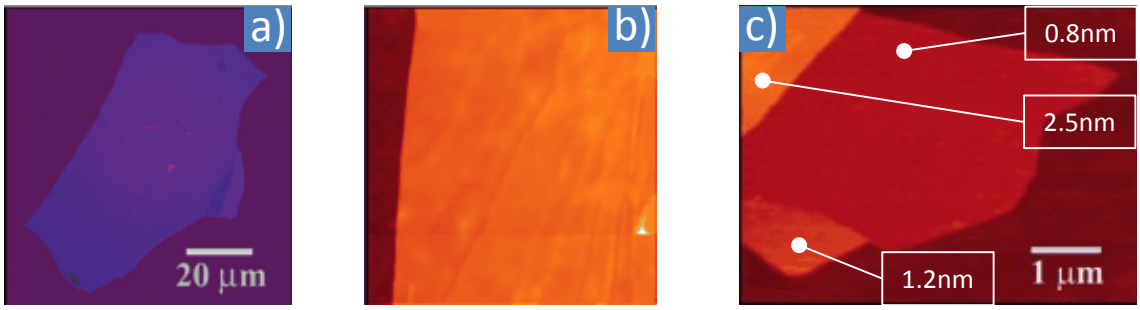

Figure 1.13. Examples of graphene films. a) Photograph of a large multilayer graphene flake with thickness ~3 nm on top of a SiO_2/Si substrate. b) Atomic force microscope (AFM) image of 2x2µm^2 area of the flake shown in a) near its edge, c) AFM image of single-layer graphene. Colors: dark brown, SiO_2 surface; brown-red (central area), 0.8nm height; yellow-brown (bottom left), 1.2nm; orange (top left), 2.5nm [Novoselov 04].

However, large area graphene sheets with low defects and controllable thickness are highly demanded by semiconductor industry. At present, one of the methods used to fabricate high quality graphene layers is epitaxial growth of graphene on the faces of a SiC wafer by atomic sublimation at well controlled temperatures [Gyan 11, Alaboson 11, Huang 11a, Yue 11, Vecchio 11]. However, using this method, even if the carriers' mobility, which is a good indicator of the graphene quality, is acceptable, the elevated cost of the substrate and the difficulty of growing monolayer graphene flakes make this process still not recommendable for mass production of graphene devices [Gyan 11, Vecchio 11]. Alternatively, chemical vapor deposition (CVD) methodology has recently been used to produce graphene on both nickel and copper substrates [Chae 09, Bae 10]. In particular, the process to grow graphene flakes on copper is based on the decomposition of methane at high temperatures, which can lead to the deposition of graphene monolayers [Han 11]. One of the characteristics of CVD-grown graphene flakes is that they can be transferred onto other substrates using an ingenious method [Suk 11], which is not possible for epitaxial SiC graphene. This transfer capability facilitates the study of the interaction of graphene with different materials, which is essential for the fabrication of graphene field effect transistors and graphene-oxide-semiconductor capacitors that use SiO_2 and High-k dielectrics as a substrate [Yang 12, Stützel 10, Liu 10, Park 11]. However, the graphene flakes fabricated by this method can contain many kinds of defects that impoverish their properties. Among them, topographic imperfections are especially important because they can difficult perfect adhesion of graphene on the substrate [Zhang 11], being very harmful in large area devices. Such topographic imperfections can be classified into two groups depending on their origin: strain-related wrinkles and substrate-induced corrugations. The origin of wrinkles, which have been observed in both as-grown and transferred samples [Mattevi 11], is related to the high compressive strain induced by the high temperatures and the different thermal expansion coefficients between graphene and copper [Gyan 11, Zhang 11]. On the other hand, substrate-induced corrugations are related to the morphology of the substrate on which the graphene layer was grown [Liu 11a, Pan 11]. These corrugations can be kept after the transfer process [Liu 11a, Pan 11], and normally appear as folds, buckling and cracks. Both, substrate-induced corrugations and strain-related wrinkles have been observed to be the most harmful defects in large areas. More specifically, they can degrade the electronic structure, transport, and mobility of graphene [Myer 07, Barnarda 12] and they may also increase the device-to-device variability. Therefore, the mechanism of corrugation and wrinkle formation should be clearly investigated and, in particular, finding a way to fabricate graphene sheets free of topographical defects is essential for applications based on graphene. The presence of grain boundaries in graphene layers can also affect their electrical properties. Grain boundaries can be formed, firstly, due to the elevated temperature during the CVD deposition process, which can make that the copper substrate develops large copper grains observable by optical microscopy. And secondly, when islands of graphene begin to coalesce during the initial growth stage [Yu 11]. The copper steps and the grain boundaries are the preferable nucleation sites for the graphene islands to start growing [Liu 11b]. As they are randomly distributed over the surface, the graphene grains increase in size having different crystal orientation [Huang 11a], which are observed at the zones where they coalesce, leading to the grain boundaries (Fig. 1.14). The resulting graphene films therefore are polycrystalline, as they nucleate from random locations.

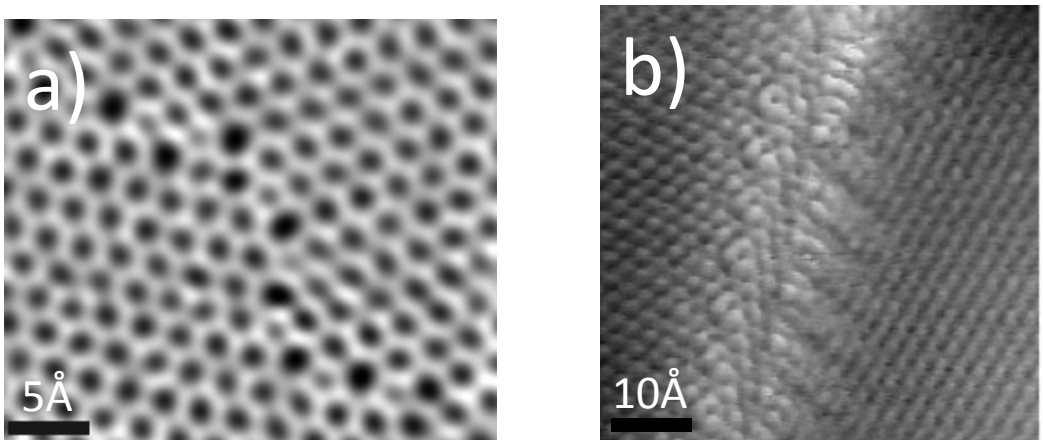

Figure 1.14. (a) TEM image of two graphene grains (bottom left, top right) intersect with a 27° relative rotation. An aperiodic line of defects stitches the two grains together [Huang 11b]. (b) Topographic image of a graphene layer showing the atomic scale appearance of grain boundary in the topmost layer of highly ordered pyrolytic graphite (HOPG) [Biro 13].

High-resolution transmission electron microscopy (TEM) and STM methods have been used to investigate graphene grain boundaries (Fig. 1.15). Even it is characterized as defect in its crystalline structure, the grain boundaries are identified to be entirely made up of carbon atoms, which means that it keeps being a continuous graphene membrane. However, from an electrical point of view, graphene grains can also be observed based on their different electrical conductivity. In [Ahmad 11] graphene domains are identified via their ability to drive current horizontally. A considerable non-uniformity in its electrical conduction is considered to be the consequence of two aspects. On one hand, differences in the graphene-layer thickness could suggest a different number of layers, whereas a thicker layer involves a higher conductivity. On the other hand, the complete isolation of graphene domains could be attributed to large resistance of grain boundaries. It's important to remark that this polycrystallization can affect to the transport properties of the device and the electrical properties of the layers underneath the graphene single layer (GSL), especially at grain boundaries. As an example, GSL-coated Cu and Ni substrates have shown resistance to oxidation in hydrogen peroxide (H_2O_2) [Chen 11], heating up to 200ºC [Kang 12, Nilsson 12] in air, under ultraviolet irradiation in moisture-rich ambient conditions [Duong 12], and when exposed to electrochemical tests [Nemes-Incze 11, Raman 12, Won 12, David 13, Prasai 12] demonstrating that can be useful as coating material to prevent oxidation of different substrates. However, at the same time, it has been suggested that the defects present at the domain boundaries of polycrystalline GSL [Huang 11b, Li 09a] might be a source of local oxidation [Chen 11] of the underneath substrate altering its properties. Actually, this property has been even used to analyze the domain size of polycrystalline graphene grown by different methods [Nilsson 12, Nemes-Incze 11]. Since, the experiments performed in this thesis are carried out with graphene grown by CVD on Cu, which is then transferred to other substrates, the quality of the graphene layer will be analyzed in detail in chapter 6. Moreover, the effect of domain boundary imperfections on the morphological and electrical properties of polycrystalline GSL and the substrate underneath will be investigated. The effect of the local oxidation on the electrical properties of GFETs will be also studied.

1.6.2 Graphene electronic properties

Some of the most relevant properties of graphene regarding electronic applications are mobility and the absence of a bandgap. Large-area graphene is a semimetal with zero bandgap. Because of that, devices with large-area graphene-based channels cannot be switched off and, therefore, are not suitable for logic applications. However, the band structure of graphene can be modified, and it is possible to open a bandgap in three ways: by constraining large-area graphene in one dimension to form graphene nanoribbons, by biasing bilayer graphene and by applying strain to graphene. It has been predicted [Prasai 12] that armchair and zigzag nanoribbons (the two ideal types of nanoribbon) have a bandgap that is, to a good approximation, inversely proportional to the width of the nanoribbon. The opening of a bandgap in nanoribbons has been verified experimentally for widths down to about 1 nm [Nemes-Incze 11, Raman 12, Won 12, David 13], and theory and experiments both reveal bandgaps in excess of 200meV for widths below 20nm. However, it should be noted that real nanoribbons have rough edges and widths that change along their lengths leading to an important device-to-device variability. To open a bandgap useful for conventional field-effect devices, very narrow nanoribbons with well-defined edges are needed [Li 09b]. This represents a serious challenge given the semiconductor processing equipment available at the moment. Recently, nanoribbons that were uniform in width and had reduced edge roughness were produced by 'unzipping' carbon nanotubes [Jiao 10]. However, even a perfect nanoribbon is not perfect for electronics applications: in general, the larger the bandgap that is opened in a nanoribbon, the more the valence and conduction bands become parabolic and that increases the effective mass of the charge carriers [Raza 08], which is likely to decrease the mobility [Balog 10].

The most frequently stated advantage of graphene for electronic applications is its high carrier mobility at room temperature. Mobilities of 10,000–15,000$cm^2V^{-1}s^{-1}$ are routinely measured for exfoliated graphene on SiO_2-covered silicon wafers [Chen 08], and upper limits of between 40,000 and 70,000 $cm^2V^{-1}s^{-1}$ have been suggested [Chen 08, Chen 09]. Moreover, in the absence of charged impurities and ripples, mobilities of 200,000 $cm^2V^{-1}s^{-1}$ have been predicted [Morozov 08], and a mobility of 1,000,000$cm^2V^{-1}s^{-1}$ was recently reported for suspended graphene [Geim 10]. For large-area graphene grown on nickel and transferred to a substrate, mobilities greater than 3,700$cm^2V^{-1}s^{-1}$ have been measured [Kim 09]. Finally, for epitaxial graphene on silicon carbide, the mobility depends on whether the graphene is grown on the silicon face or the carbon face of SiC. In early graphene based MOS structures, the mobility was affected by the use of a top-gate dielectric [Lemme 07, Lin 09]. However, the recent demonstration of mobilities of around 23,000 $cm^2V^{-1}s^{-1}$ in top-gated graphene MOS channels [Liao 10] and the observation of similar mobilities before and after top-gate formation [Farmer 09] show that high-mobility graphene channels can be made with a proper choice of the gate dielectric and optimization of the deposition process. Although, these values of mobilities are very high, they are related to large-area graphene flakes, which is gapless. However, a general trend for conventional semiconductors is that the electron mobility decreases as the bandgap increases, which was also predicted for carbon nanotubes (CNTs) [Zhou 05, Obradovic 06] and graphene nanoribbons [Obradovic 06, Fang 08, Bresciani 09, Betti 09]. This means that the mobility in nanoribbons with a bandgap similar to that of silicon (1.1 eV) is expected to be lower than in bulk silicon and no higher than the mobility in the silicon channel of a conventional MOS device [Obradovic 06]. The mobilities measured in experiments—

less than 200 $cm^2V^{-1}s^{-1}$ for nanoribbons 1–10 nm wide [Won 12, Wang 08] and 1,500 $cm^2V^{-1}s^{-1}$ for a nanoribbon 14 nm wide [Jiao 10] (which is the highest mobility so far measured for a nanoribbon)—support the theoretical results. Therefore, although the high mobilities offered by graphene can increase the speed of devices, they come at the expense of making it difficult to switch devices off, being one of the main drawbacks for logic applications. At this point, it should be mentioned that opening a band gap in Graphene sheets without degrading its mobility is one of the main challenges of the semiconductor industry, as it has been reported in the last version of the International Technology Roadmap for Semiconductors (ITRS). Despite that, at present there is still a high interest in using graphene as a channel replacement material (GFETs) for analog and radio frequency applications.

1.6.3 Graphene-based Field Effect Transistors (GFETs)

The progress in the fabrication of graphene based transistors (GFETs) has advanced very fast since the fabrication of the first top-gate GFET was reported in 2007 [Lemme 07]. Although research into graphene is still in its infancy, GFETs can compete with devices that have benefited from decades of research and investment. Top-gated GFETs have been made with exfoliated graphene [Lemme 07, Lin 09, Liao 10, Farmer 09, Meric 08, Meric 08b], graphene grown on metals such as nickel and copper [Kedzierski 09, Li 09a], and epitaxial graphene [Liu 11, Kedzierski 09, Moon 09]. SiO_2, Al_2O_3, and HfO_2 have been used for the top-gate dielectric.

The carrier density and the type of carriers (electrons or holes) in the channel are governed by the potential differences between the channel and the gates. Fig. 1.15 shows a schematic of a GFET with a back gate. Large positive gate voltages promote an electron accumulation in the channel (n-type channel), and large negative gate voltages lead to a p-type channel. This behavior gives rise to the two branches of the transfer characteristics separated by the Dirac point of a GFET. The position of the Dirac point depends on several factors: the difference between the work functions of the gate and the graphene, the type and density of the charges at the interfaces at the top and bottom of the channel, and any doping of the graphene.

The output characteristics of many GFETs either show a linear shape without any saturation [Lin 09] or only weak saturation [Lin 10, Moon 09], each of which is a disadvantage with respect to device speed. However, some GFETs have an unusual form of saturation-like behavior that includes a second linear region [Meric 08b, Kedzierski 09, Israelachvili 92]. This peculiar behavior is a consequence of these devices having gapless channels and does not occur in FETs with semiconducting channels. Recently, GFETs with gigahertz capabilities have been reported. These transistors possess large-area channels of exfoliated [Emtsev 09, Farmer 09, Meric 08, Thiele 10] and epitaxial [Rutherglen 09, Yoon 07] graphene. A weak point of all radiofrequency GFETs reported so far is the unsatisfying saturation behavior (only weak saturation or the second linear regime), which has an adverse impact on the cut-off frequency, the intrinsic gain and other figures of merit for radiofrequency devices.

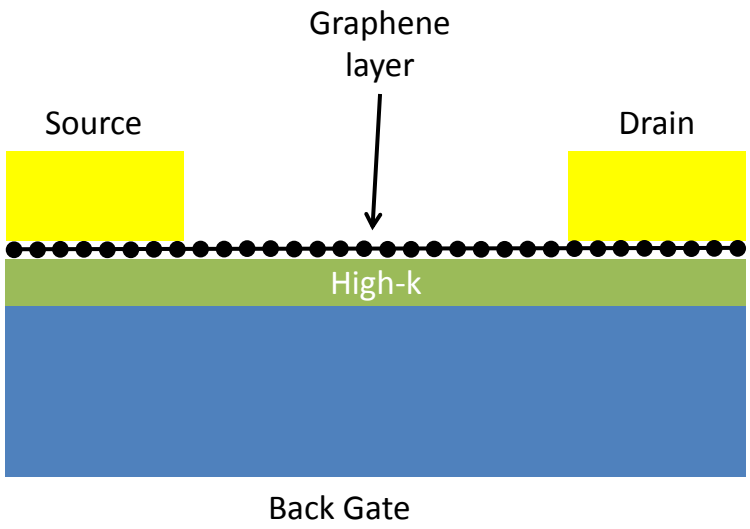

Figure 1.15. Schemactic of a back gated GFET.

1.7 Standard characterization techniques

In order to study the electrical properties and failure mechanisms of gate dielectrics, different techniques and/or electrical tests are applied to test structures (capacitors or transistors). This section is devoted to introduce the most common characterization tests used to perform these analyses. In order to study the degradation process of gate oxides, test structures are subjected to electrical stresses by applying voltages or forcing currents through them, whose aim is to provoke its deterioration. Since, under normal operational conditions, the lifetime of devices would be too large, to perform reliability studies in reasonable time scales, so-called accelerated electrical tests are applied. These tests basically consist in applying larger voltages and drive larger currents than under normal conditions and measuring the evolution of the electrical properties. In the following the most common tests used in reliability assessment are briefly described.

Constant Voltage (CVS) and current (CCS) stress

Two of the most common tests are the so-called Constant Voltage Stress (CVS) and constant current stress (CCS). They have in common that a stress parameter is kept constant over time. In the first case a constant voltage is applied between gate and bulk of the sample, whereas in the second case a constant current is injected and the complementary magnitude is measured with time (current in the CVS and voltage in the CCS). These tests provide information about the time elapsed between the beginning of the stress and the moment when the dielectric BD is triggered (time-to-breakdown, t_{BD}), which is detected as a brusque increase in leakage current for the CVS (Fig. 1.16a) and an abrupt decrease in voltage (Fig. 1.16b) over the gate oxide for the CCS. The evolution of the measured electrical properties during the stress can also be used to get information about the degradation process of the gate stack.

a) b)

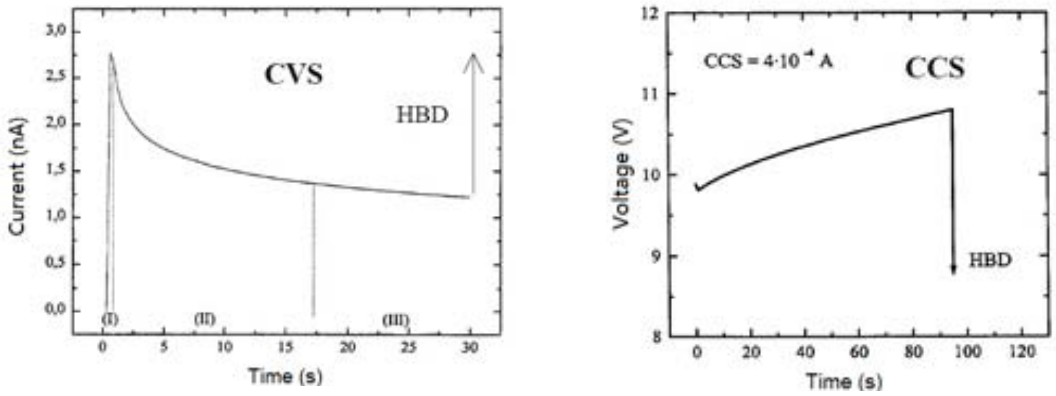

Figure 1.16. (a) I-t and (b) V-t curves measured on thick SiO_2 layers after applying a CVS and CCS, respectively [Rodriguez 00].

Ramped Voltage Stresses (RVS)

A linearly increased ramped voltage (RVS) is applied to the sample and the current at each applied voltage is measured until dielectric breakdown occurs, providing current voltage (I-V) characteristics. Fig. 1.17 shows an example where 2 RVS are applied at a SiO_2-based MOS structure. In this test, BD is identified as a sudden increase in the tunneling current through the oxide at ~6.5V during the first voltage ramp. Note, that the second I-V curve is completely different as it shows high level conduction even at low voltages, demonstrating that during the previous stress the dielectric has lost its insulating properties.

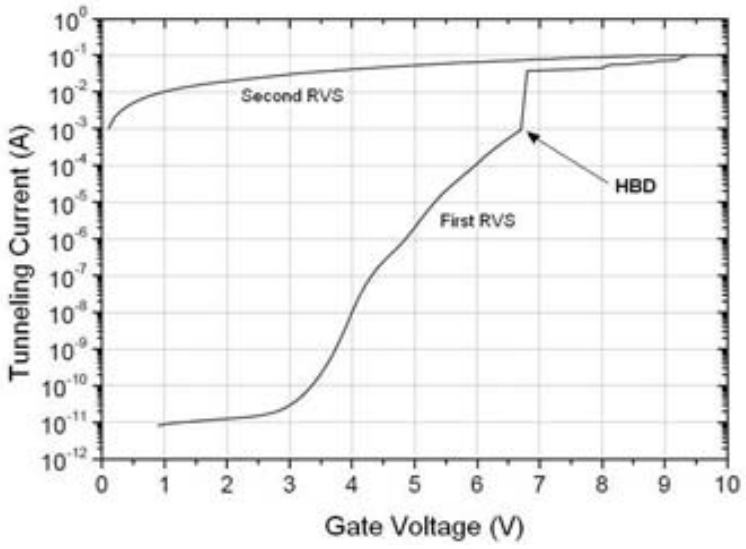

Figure 1.17. Typical I-V curves obtained after applying two RVS at a SiO_2 based capacitor. The first curve shows a characteristic increase of the current at ~6.5V due to a HBD event. The second curve shows a complete loss of its dielectric insulation properties.

The accelerated electrical tests mentioned above are usually applied to gated devices, that is, to test structures as capacitors or transistors with a gate electrode, and are usually called "standard characterization techniques". They allow measuring the global electrical properties through the gate, such as the average tunneling current, the time-to-breakdown (t_{BD}) and the injected charge-to-BD (Q_{BD}). However, nanoscale information cannot be obtained. Note that all variability sources (such as polycrystallization of gate dielectrics or graphene layers, see section 1.5 and 1.6.1, respectively) are phenomena that take at the nanoscale. Moreover, in section 1.4 it was introduced that the failure mechanisms of gate oxides were associated to the creation of defects, which are also related to mechanisms that also occur at the nanoscale. Taking into account that all these phenomena (variability sources and aging mechanisms) occur at the sub-micron scale, device level characterization techniques are not suitable, because local variations of the electrical properties cannot be measured. In order to have more detailed insight into variability and degradation processes, tools with a high lateral resolution are essential. Such tools will be introduced in the next section.

1.8 Nanoscale characterization techniques

Among the different nanoscale resolution techniques, Scanning Probe Microscopes (SPM) are currently some of the most successful. SPM is a general term describing different microscopes which are based on an extremely sharp tip that scans the surface under study to measure its topography. SPM provides a sub-nanometric resolution in three dimensions, e. g. lateral and vertical. This information can be used to create a 3D representation of the investigated surface. The two main representatives of SPM technology are Scanning Tunneling Microscope (STM) and Atomic Force Microscope (AFM).

STM

The first prototype of a Scanning Tunneling Microscope (STM) was fabricated in 1981 by Gerd Binnig and Heinrich Rohrer from IBM in Zürich/Switzerland. Due to the development of this microscopy technique, they were awarded with the Nobel Prize for Physics in 1986. With this microscope, for the first time, it was possible to image single atoms and their crystalline arrangement [Binnig 83]. The principle of operation of an STM consists in a conductive tip which is approximated to a sample until reaching atomic distances. Applying a voltage bias will establish a flow of electrons (tunneling current), from which a topographical map with sub-nanometer resolution can be obtained since tunneling current depends on the tip-sample distance. However, an STM implies some restrictions, which have to be kept in mind. For example, as the tunneling current strongly depends not only on the tip-sample distance but also on the electronic characteristics of the sample, changes in a topographic image cannot exclusively be attributed to morphology, but may also be originated from changes in its electrical properties. Moreover, as the tunneling current is highly sensitive to ambient influences, STM experiments are carried out in ultra-high vacuum conditions. Finally, with a STM, only conductive samples (or ultrathin dielectrics on conductive substrates) can be measured.

AFM based techniques

With ongoing technological development, a new measurement method was invented in 1986 – the Atomic Force Microscope (AFM). In that case, since topography is obtained from the force that appears between the tip and the sample when they are very close to each other (see chapter 2), topographical information is not affected by the electrical properties of the sample. Moreover, many different kinds of surfaces can be investigated, including insulating materials. Finally, experiments can be performed in many environments, such as liquids, ambient air and vacuum, although the last one improves significantly the instruments resolution [Lanza 10].

Since 1986, different variations of AFMs have been invented in order to detect, simultaneously to the topography, other properties of the sample under study. The most representatives for nanoelectronics applications [Oliver 08, De Wolf 01, Kalinin 07] are the Conductive Atomic Force Microscope (CAFM) [Murrell 93], Scanning Spreading Resistance Microscope (SSRM) [De Wolf 98, De Wolf 99], Kelvin Probe Force Microscope (KPFM) [Nonnemacher 91] and Scanning Capacitance Microscopy (SCM) [Martin 88, Dreyer 95]. In the CAFM and SSRM, a bias voltage between the tip and the sample is applied and the current through the sharp AFM probe is measured. CAFM in general is used to measure the tunneling current flowing through a dielectric layer. SSRM was primarily used to detect the local distribution of dopants by measuring the spreading resistance. Note that in the case of the CAFM, when working on a bare gate oxide, the tip of the SPM plays the role of a MOS capacitor with an area that is the contact area between the tip and the sample. Since this area is in the range ~10-100nm², a nanometer resolution can be achieved (Fig. 1.18).

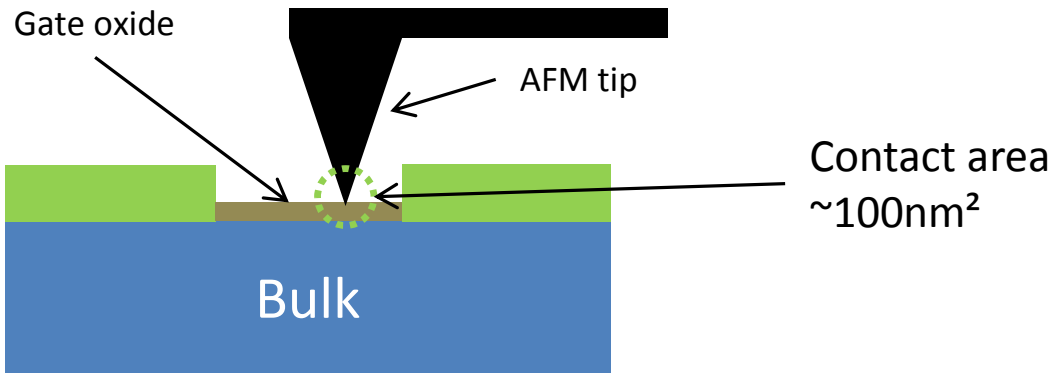

Figure 1.18. Experimental configuration when characterizing MOS structures without top electrode at the nanoscale with AFM (area ~10-100nm^2)

Actually, since its inception, CAFM has been extensively used to study the electrical properties of as-grown (before an electrical stress) and stressed gate dielectrics. In the case of SiO_2 films, for example, [Porti 01, Pakes 04, Polspoel 07], it has been used to evaluate the dielectric strength of SiO_2 gate oxides [Porti 01], local variations of the gate oxide thickness with high resolution [Olbrich 99], the influence of electrical stress [Blasco 05, Porti 03, Frammelsberger 06] and irradiation [Wu 07] on the degradation. Porti et al. [Porti 01] presented a work demonstrating experimentally the local character of a BD event (~100 nm^2) based on CAFM measurements. However, lateral BD

propagation (depending on the BD level) has been observed by Porti [Porti 04] and Blasco [Blasco 05]. These authors observed that a current limited stress provokes a smaller propagation area compared to a non-limited current flow through the tip. Here, one has to take into account that in this case, the nature of the breakdown is much more violent and may provoke the melt of the conductive layer of the tip (due to Joule heating). Works based on statistical analyses of different gate dielectrics, taking into account different types and different thicknesses, come to the conclusion that the time-to-breakdown (t_{BD}) measured at the nanoscale follows a Weibull distribution [Sire 07, Fiorenza 07].

With the introduction of high-k materials, the CAFM began to be used for investigation of their electrical properties [Rumler 12]. The electrical homogeneity of as-grown hafnium-based dielectric stacks, such as HfO_2 or $HfAlO_x$, were studied [Shubharar 13, Petry 04]. Subsequently, its came into use for the investigation of different material, for example ZrO_2 [Paskaleva 08], $HfSi_xO_y$ [Yanev 09], Al_2O_3 [Lanza 11a] and $SrTiO_3$ [Kraya 12]. It was used to assess the conduction by trap assisted tunneling (TAT) [Nasyrov 09, Fiorenza 06] provoked by the higher density of native defects in high-k materials [McKenna 11, Lanza 11b] or due to the effect of a thermal treatment leading to polycrystallization and, therefore, to morphological and electrical changes of the gate oxide [Pawlak 10]. At this respect, CAFM has been used to study the impact of its polycrystallization on the nanoscale electrical properties of polycrystalline HfO_2 based MIS structures. In [Iglesias 10] (Fig. 1.19) it has been demonstrated that GBs are more conductive, probably due to an excess of O-vacancies [Iglesias 11], impoverishing its reliability. This technique has also been helpful to show the contribution of dominant TAT and FN current transport mechanism to the oxide leakage [Frammelsberger 06, Iglesias 11, Uppal 09] and to study the effect of gate dopant diffusion on the leakage current of poly-Si/HfO_2 stacks [Yu 07]. The impact of the interfacial layer on the electrical properties of a high-k/SiO_2/Si structure [Aguilera 07] has also been studied by growing an ultra-thin SiO_2 layer between the high-k material and the Si substrate.

Studies performed with CAFM about the degradation of the gate stack can be also found in the literature. Some of these works suggest that this degradation is due to the existing charge traps in polycrystalline high-k gate stacks, being the precursors of stress-induced defects [Paskaleva 08]. Recently, nanoscale electrical characterization has been performed to determine the cumulative failure distribution of TDDB [Wu 08I, Erlbacher 11], which shows a bimodal shape for bilayer stacks [Delcroix 11, Iglesias 13]. This effect has also been observed by [Masuduzzaman 12], where the electric breakdown in polycrystalline dielectric layers was primarily localized in the grain boundaries, and that was associated to an elevated number of pre-existing defects in such positions. Actually, in [Iglesias 13] it was demonstrated that the bimodal BD distributions measured in polycrystalline high-k dielectrics can be attributed to the different electrical properties of grains and grain boundaries. In [Ganesan 11] the SILC in ALD grown ultrathin Al_2O_3 films has been investigated using C-AFM, showing great difference of SILC and degradation of thick films, with respect to thin films.

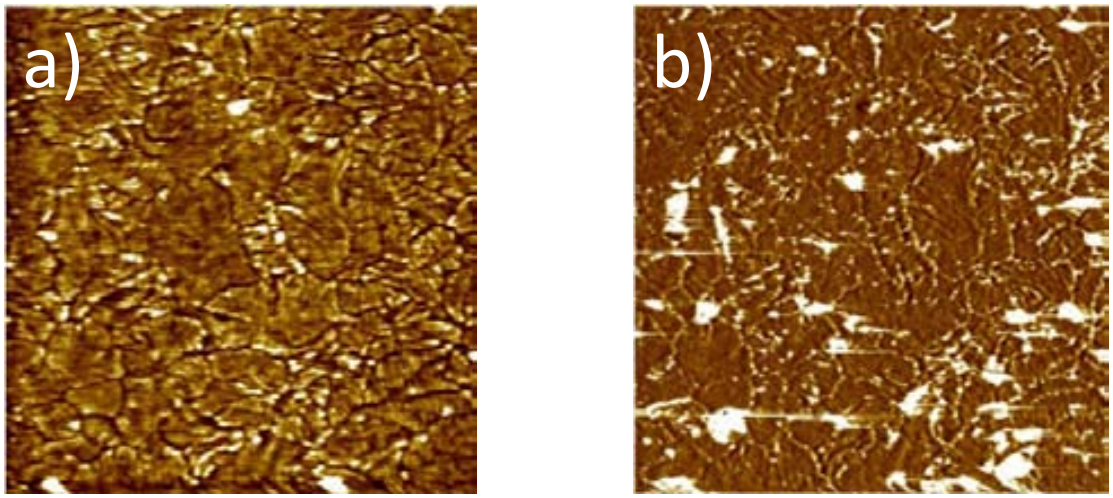

Figure 1.19. Topographical (a) and current (b) image obtained on a $HfO_2/SiO_2/Si$ structure with an area of $1x1\mu m^2$. Note that leakage sites at the pA range in (b) are related to GBs in (a) [Iglesias 10].

Furthermore, due to the local character of some RS mechanisms, CAFM has been used to investigate Resistive Random Access Memory (ReRAM) devices [Iglesias 12, Jeong 12, Bersuker 11, Lanza 12, Polspoel 12]. The study of the transport characteristics of reduced oxide metal nanoparticle interfaces, as well as the influence of the contact size at the interface can be used to understand resistive switching mechanisms and the effects of ohmic and tunnel contacts to switching phenomena [Kraya 12]. The nanoscale current distribution and switching properties of thin film heterostructures, as well as the investigation of the scaling capabilities of MIM structures can prove the coexistence of different switching mechanisms [Muenstermann 10].

Finally, CAFM has also been used to investigate different electrical properties of graphene. One of them is the charge transport in graphene [Giannazzo 11]. Several aspects related to the charge transport, including the electron mean free path and the role of the graphene/substrate interface have been studied. A great influence on electrical conduction is attributed to grain boundaries and morphological deformations of the graphene film, where a lower conductivity was found. Even different grains inside the graphene layer show different conductivity leading to the conclusion that the conduction of an entire graphene domain highly depends on its interconnection with its neighbored domains via the grain boundaries [Nirmalraj 10, Ahmad 12]. Moreover, a change in the conductivity can also be provoked by localized nano-defects induced by irradiation with ions [Prevel 12] or local anodic oxidation via a CAFM setup [Kurra 11].

In summary, during the last two decades, CAFM has been extensively demonstrated to be a very powerful tool to investigate the electrical properties of materials for nanoelectronics applications, as SiO_2, high-k dielectrics, graphene, etc., providing a lot of details thanks to its high lateral resolution. In this thesis, a CAFM will be also used to study at the nanoscale different aspects related to the variability and reliability of high-k gate dielectrics and the topographical and electrical properties of graphene layers deposited on different substrates.

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Chapter 2: Atomic Force Microscope and related techniques

As introduced in chapter 1, one of the most important tools used for the characterization of surfaces at the nanoscale is the AFM – Atomic Force Microscope. In this chapter, AFM and those related techniques used in this thesis, such as Conductive Atomic Force Microscopy (CAFM) and Kelvin Probe Force Microscopy (KPFM), will be described. Both techniques, derived from the AFM, allow detecting different electrical properties of the material under investigation. As the AFM resolution highly depends on the tip properties, a section is dedicated to introduce them. Finally, the AFM measurement setups used in this thesis are also presented.

2.1 Atomic Force Microscope

The AFM is an instrument that allows measuring topographical images of the sample under study. It basically consists of a sharp tip that scans a given surface and measures the interaction force between the tip and the sample, when they get very close (Fig. 2.1). As the tip is located at the end of a cantilever, it flexes due to the force interaction according to Hooke's law, F=-k*x, being k its spring constant. This cantilever deflection is detected by an optical system that consists of a laser and a four side-by-side photodiodes. The backside of the cantilever is coated by a reflective layer that guides the focused laser beam into the photo-detector, which is able to register the reflected laser beam position on the diode system. Since this position depends on the cantilever defection, and therefore, on the force applied to the tip and that on the topography of the surface, using this setup, information of the topography can be obtained. Finally, the vertical position of the tip and its lateral movement during the scan is controlled by a piezoelectric material.

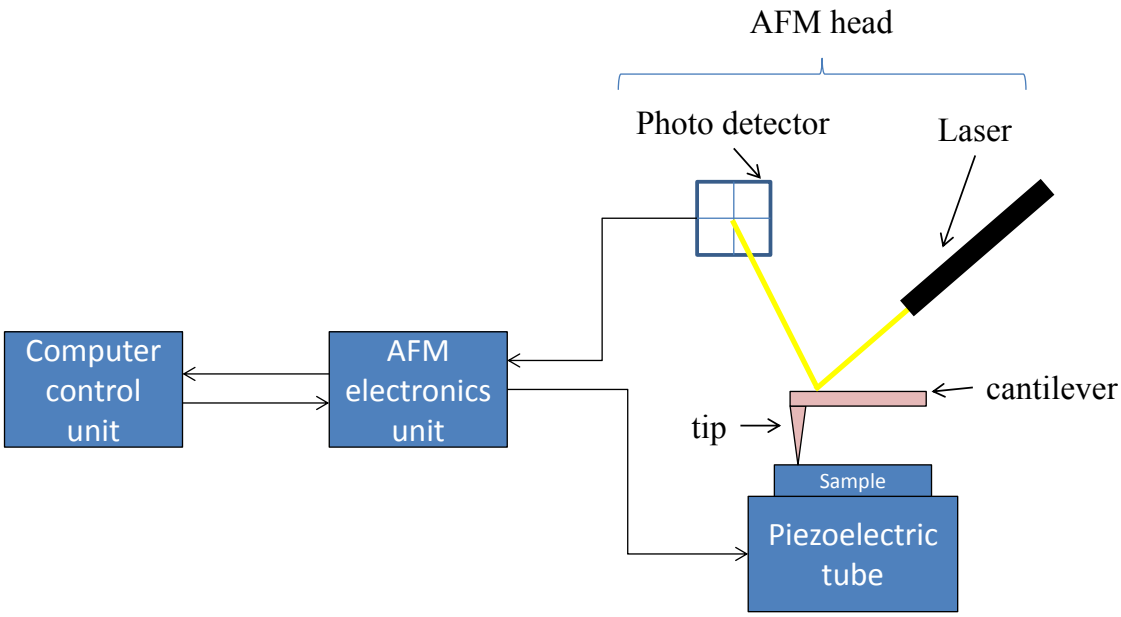

Figure 2.1. Block diagram of a conventional AFM instrumentation system consisting of the AFM head, the AFM electronics unit, which receives signals from the AFM head and transforms them into interpretable information, and the computer control unit.

AFMs normally operate in a constant force mode, which means that the force applied to the tip is maintained constant during the scan. To do so, a feedback circuit in the AFM electronics unit is needed, which will keep the cantilever deflection and, therefore, the tip-sample distance constant (which value is established by the user as setpoint) by applying the necessary voltage to the piezoelectric scanner during the scan. Such a feedback loop is necessary when investigating, for example, samples with large changes in topography, in order not to cause damage to, both, the tip and the sample. A very important issue is the interference of mechanical vibrations with running measurements, which are also detected but undesired. To avoid them, AFMs are situated on vibration absorbing systems.

2.2 AFM Operation Modes

The distance between tip and sample and, therefore, the forces applied to the tip during the scan, determines different AFM operation modes (Fig. 2.2).

Contact mode

The atoms at the end of the tip are "touching" the surface (at a distance of 1-3Å, being in the repulsive force regime [San Paulo 00]) (Fig. 2.2) and interact with the sample surface. As the tip is in permanent contact during the entire scan, it wears out fast. Actually, this is one of the main drawbacks of this mode. However, its resolution is better compared to the non-contact mode.

Non-contact mode

In this mode (which corresponds to the measurement of the attractive forces, Fig. 2.2), the tip-sample contact is reduced to a minimum, since the tip does not touch the surface like in the contact mode. This mode, on the other hand, provokes a vertical resolution reduction [Kitamura 95]. Kitamura et al., however, could obtain atomically resolved topographical images of Si(111) in ultra-high vacuum conditions. Since the measureable forces in this mode are smaller, they are detected by exciting the tip and making it oscillate. Measuring the change in amplitude, phase or resonant frequency of the cantilever allows determining the applied force, and therefore, the topography of the sample.

Tapping mode

Tapping mode [Zhong 93] combines elements of the contact and non-contact mode above described in order to overcome or reduce disadvantages presented by both, such as friction. In this mode, a near to its resonance frequency oscillating cantilever touches the surface intermittently at the extreme points of the amplitude. During tapping mode operation, the cantilever oscillation amplitude is maintained constant by the feedback loop and the force on the sample is automatically maintained at the lowest detectible level. Therefore, when, for example, the tip detects an obstacle on the surface, the tip-sample distance is reduced (as well as the oscillation amplitude). Given the case of a depression the oscillation amplitude is increased. As the feedback loop intents to maintain the amplitude at a constant level, it adjusts the tip-sample separation.

It has to be taken into account that, operating an AFM in ambient air conditions involves a thin water layer, which is present on the sample surface due to the ambient humidity. A water meniscus exerts an attractive force between tip and sample pulling the cantilever towards the sample surface [San Paulo 00] and, therefore, affecting also the measurement. In order to minimize this aspect, optionally, the sample can be investigated in nitrogen ambient or even in vacuum conditions [Lanza 10].

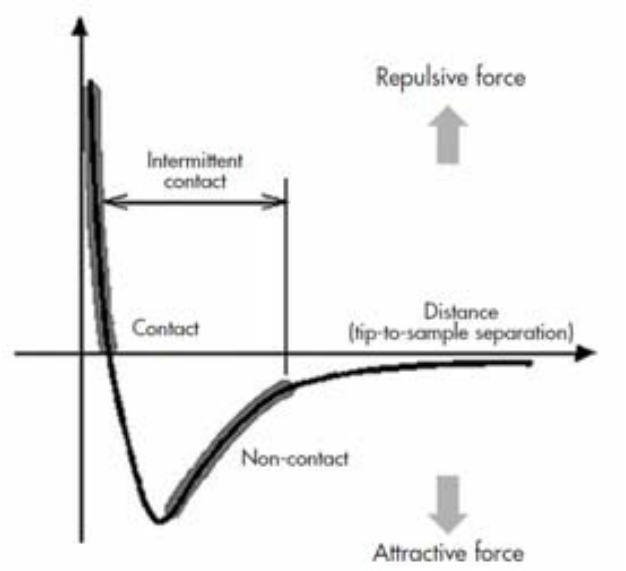

Figure 2.2. Attractive and repulsive forces as a function of the tip/sample distance, which define the non-contact and contact operation modes, respectively.

2.3 Conductive Atomic Force Microscopy (CAFM)

The AFM based technique mostly used to carry out the experiments presented in this thesis is the CAFM (Conductive AFM), which detects simultaneously topography and electrical current. In order to be able to measure current, conventional AFM has to be additionally equipped with (a) a conductive tip, (b) a voltage source and (c) a very low noise preamplifier (Fig. 2.3).

In general, in a CAFM experiment, a constant voltage is applied between the tip and the sample while scanning with the tip a given area of the structure under study. That allows collecting the current via the conductive AFM tip at the same time than the topography. This provides the possibility to correlate directly topography with electrical information from the measurement of topographical and current maps, which represent the electrical conduction for each point at a given bias voltage. Apart from this method, the CAFM also provides the option of spectroscopic analysis. In this case, the AFM maintains the tip at a fixed position of interest on the sample, performs the desired test and records the collected current. Different types of tests can be performed, as for example, ramped voltage stresses (RVS) or constant voltage stresses (CVS), leading to the corresponding current-voltage (I-V) and current-time (I-t) measurements. Although CAFM has been a technique widely used to study the electrical properties of gate oxides, its current dynamic range is limited to ~3 orders of magnitude (~pA to nA). To increase it, modified techniques, as the ECAFM (Enhanced CAFM) [Blasco 05] or specially designed modules, as the log CAFM [Aguilera 08] or Resiscope [Scientec] have been developed. In these cases, currents from pA to mA can be measured in a single test. This is especially important when measuring the post-BD behavior or the RS phenomenon, since currents can vary for many orders of magnitude.

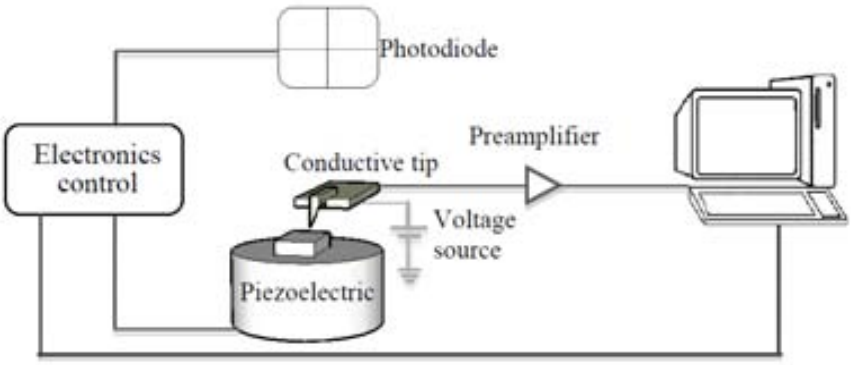

Figure 2.3. Block diagram of a CAFM setup, including the conductive tip, the voltage source and the pre-amplifier.

2.4 Kelvin Probe Force Microscopy (KPFM)

Developed in 1991 by Nonnenmacher, the Kelvin Probe Force Microscope (KPFM) allows measuring the contact potential of the sample simultaneously to the topography. In particular, KPFM detects the work function difference between the tip and the sample, the so-called contact potential difference (CPD). Therefore, KPFM can provide complementary information to that measured with a CAFM.

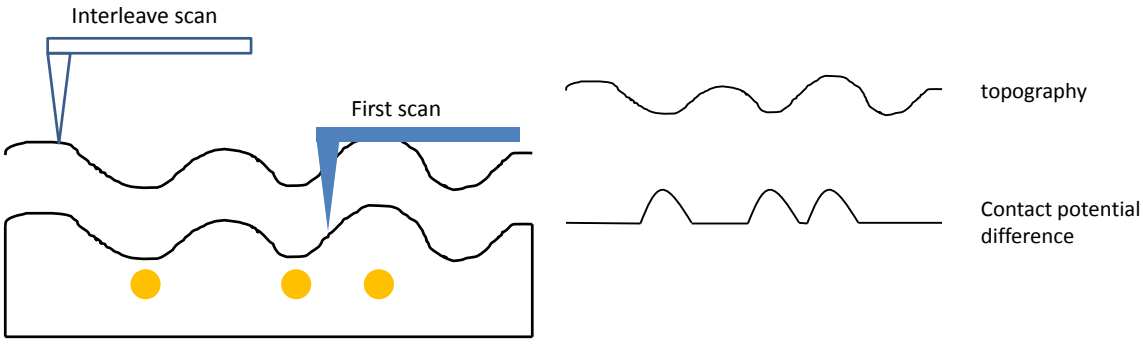

Figure 2.4. Schematic representation of the KPFM method. In a first scan the topography is recorded in tapping mode, for subsequently scan again the surface at an operator-given distance to detect the CPD signal.

Traditional KPFM is a double-pass technique, which means that every single line of an image is scanned twice. The first pass is used to capture the topography in tapping mode (Fig. 2.4). Based on this information and a defined lift height with respect to the topography, the tip scans again the surface in order to detect the CPD (Fig. 2.4). To measure the CPD, during the second (interleave) scan the cantilever is excited by biasing the tip with a voltage V_{Tip} containing a DC and AC components.

$$V_{Tip} = V_{dc} + V_{ac} * \sin(\omega t) \qquad \text{(Eq. 1)}$$

where ω is the resonant frequency of the cantilever. Assuming that the tip-sample system is equivalent to a nano-capacitor, the electrostatic energy stored at this capacitor is:

$$U = \frac{1}{2} C \Delta V^2 \quad \text{(Eq. 2)}$$

So, the resulting electrostatic force applied to the tip is given by:

$$F_{elec}(z) = \frac{\partial U}{\partial z} = \frac{1}{2} \frac{\partial C}{\partial z} \Delta V^2 \quad \text{(Eq. 3)}$$

Taking into account Eq. 2:

$$F_{elec}(z) = \frac{1}{2} [V_{CPD} - V_{dc} - V_{ac} * \sin(\omega t)]^2 \quad \text{(Eq. 4)}$$

This equation can be separated into three contributions: one due to the continuous component (Eq. 5) and two due to the frequential components ω and 2ω (Eq. 6 and Eq. 7, respectively):

$$F_{dc}(z) = \frac{1}{2} \frac{\partial C}{\partial z} (V_{CPD} - V_{dc})^2 + \frac{1}{2} {V_{ac}}^2 \quad \text{(Eq. 5)}$$

$$F_{\omega}(z) = -\frac{\partial C}{\partial z} [(V_{CPD} - V_{dc}) * V_{ac} * \sin(\omega t)] \quad \text{(Eq. 6)}$$

$$F_{2\omega}(z) = -\frac{1}{4} \frac{\partial C}{\partial z} {V_{ac}}^2 * \cos(2\omega t) \quad \text{(Eq. 7)}$$

As the AC component with frequency ω provokes as much larger oscillation, the part corresponding to 2ω can be neglected. In order to obtain the contact potential difference (V_{CPD}) during the second scan, the oscillations have to be nullified. As for equation 6 the AFM electronics changes V_{DC} in such a way, that equation 6 becomes zero and therefore the oscillations vanishes. This is given for $V_{DC} = V_{CPD}$. The changes of V_{DC} are subsequently combined to a CPD map.

Since, when measuring a bare gate dielectric, CPD depends not only on the contact potential of the substrate but also on the presence of charge in the dielectric or at the interface, plenty of the phenomena that involve a change of charge distribution can be investigated based on that effect. Therefore, KPFM provides the opportunity to investigate the charge trapping on as-grown and/or stressed gate dielectrics, which can be considered to be related to the density of defects present in the oxide. In this thesis, KPFM is used to characterize and evaluate the stress level on MOS structures based on the charge trapped in capacitive structures.

2.5 AFM Probes

When investigating samples with an AFM, the characteristics of the tip (see a schematic of a commercial tip in Fig. 2.5) play a key role, as on them depend the lateral resolution of the topographical maps. Moreover, the tip is a mechanical system and by nature it can suffer mechanical stress such as abrasion during the scan. In KPFM experiments, for example, the tip intermittently taps the surface, which leads to much lower mechanical stress. However, in the case of CAFM, in which the tip is in contact with the surface during the whole experiment, tips wear out fast. Therefore, not only on the initial characteristics of the tips, but also on their evolution during the scan, clearly depends the quality of the obtained images.

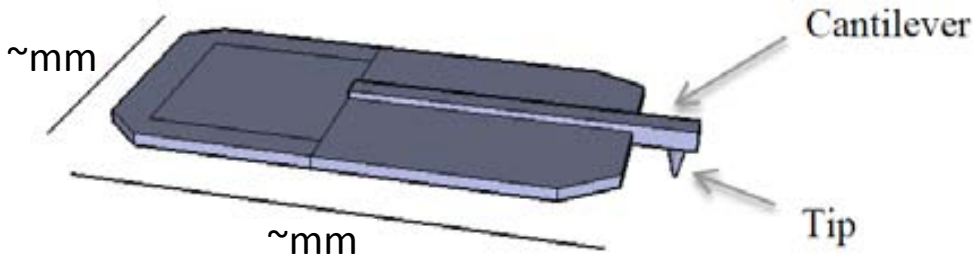

Figure 2.5. Typical mounting of supporting chip and cantilever.

AFM tips are modeled as a cone with a semi-sphere at its apex (shown in Fig. 2.6a) [Sadewasser 11]. The curvature radius, R, is defined as the radius of the semi-sphere located at the apex and marks the limit to detect structures with lateral dimensions (lateral resolution) in the order of the tip diameter (Fig. 2.6b). By increasing the tip radius the lateral resolution decreases. Fig. 2.7a and 2.7b shows an example image obtained on the same sample with a tip of radius of 30nm and 50nm, respectively [Rezek 11].

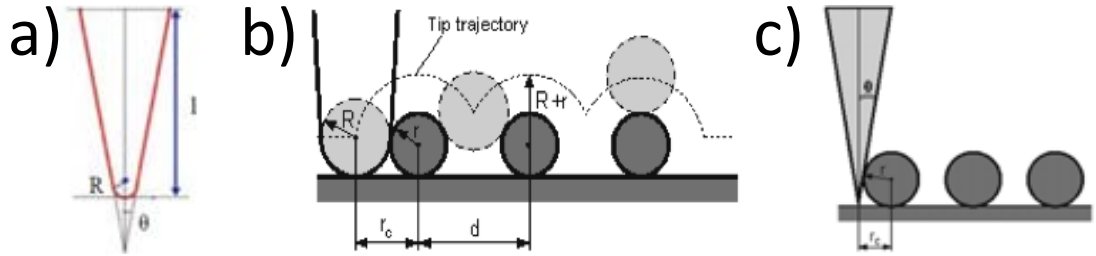

Figure 2.6. (a) Geometrical cross-section of a tip, with a finite length *l*, half-cone angle θ, and spherical apex radius *R*. (b) Influence of the curvature radius to detect structures. A smaller tip radius leads to a better AFM resolution. (c) Influence of the half-cone angle to image steep side-walls. Smaller θ leads to a better definition of top side walls. (Image extracted from www.ntmdt.com)

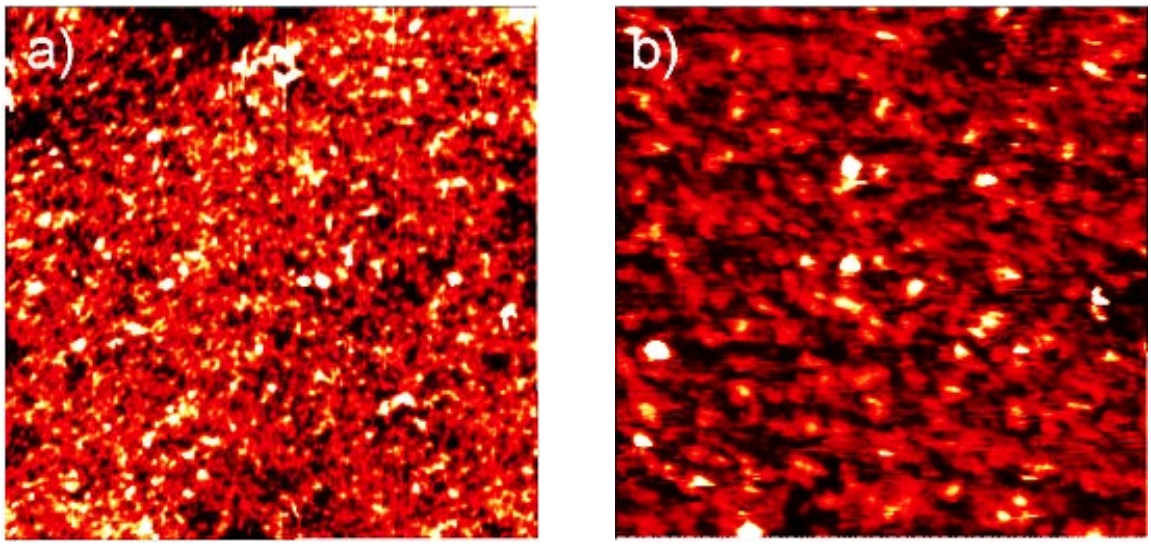

Figure 2.7. Topography of serum on mono crystalline diamond obtained with AFM tips with an estimated tip radius of (a) r ~ 30 nm and (b) r ~ 50 nm [Rezek 11].

Note that in Fig. 2.7a, smaller features can be distinguished. On the other hand, the half-cone angle, θ (Fig. 2.6a), indicates the ability to image steep side-walls (Fig. 2.6c). Therefore, the quality of an AFM image strongly depends on the shape and size of the tip, since it is a convolution between the real topography and the tip geometry. To get high resolution images, small curvature radius and half-cone angles are required (Fig. 2.7a).

However, it is important to take into account that the material composition of the tip can also determine its geometrical characteristics. Some AFM applications can require, for example, conductive tips. This is the case of tips for CAFM experiments. In that case, since we are working in contact mode and we want to measure current, tip material must be very resistant from a mechanical point of view, and conductive. But depending on the fabrication method and materials used, that can change the geometrical, mechanical and electrical characteristics of the tip. Traditionally, metal-varnished silicon tips are commonly utilized in these kinds of applications [Frammelsberger 07]. However, due to the low stability of some of the metallic varnish, these tips can wear out quite fast when driving high current densities due to Joule heating and/or because of intense tip–sample frictions since CAFM works in contact mode. The low reliability of the tips results in false imaging and unnecessarily high costs of measurements. Fig. 2.8 shows an example of what happens when a surface is scanned with a new (Fig. 2.8a) and worn out (Fig. 2.8b) coated tip during CAFM experiments. The current image of Fig. 2.8a was obtained with a new Co/Cr coated Si tip while in Fig. 2.8b an old Co/Cr coated tip was used. Conductive rings (darker areas implies larger currents) are observed when the wearing of the tip is too high (Fig. 2.8b) leading to wrong information and an impoverishment of the resolution of the measure [Lanza 10]. Therefore, finding alternatives to avoid fast tip wearing is essential for cheap and reliable nanoscale electrical characterization.

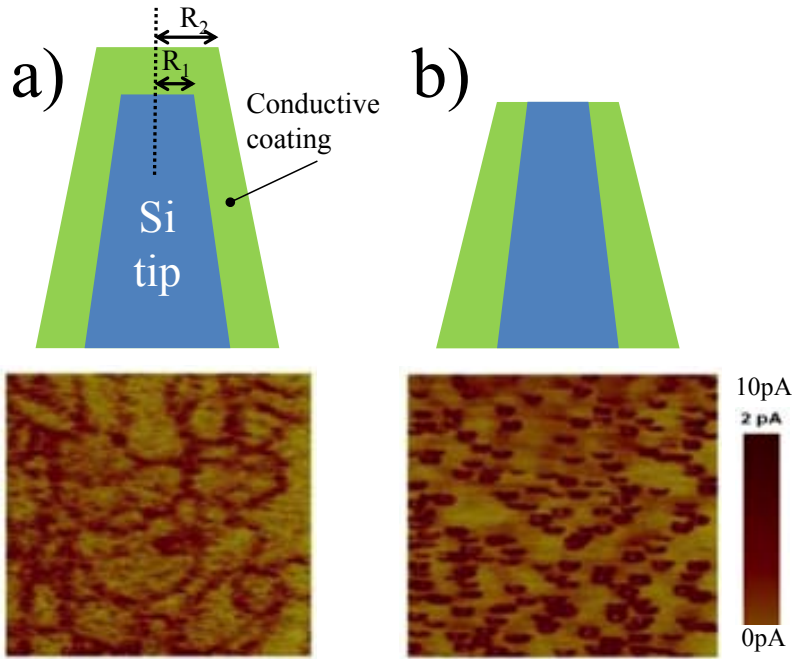

Figure 2.8. Current maps obtained with a new, (a), and a used, (b) Co-Cr coated tip. In (b) the lateral resolution is worse due to the tip wearing. Moreover, no-conductive areas surrounded by conductive regions (darker areas) can be measured, related to the wear out of the coating of the tip apex [Lanza 10]. The size of the current images is 2µm x 2µm.

An approach to preserve CAFM tip properties is to varnish them with a mechanically stable and conductive material, such as doped diamond (Fig. 2.9a). However, this alternative not only reduces the lateral resolution of measurement (due to a larger tip radius), but also significantly increases the price of the tips. A possibility to overcome this drawback is by changing drastically the tip design, in such a way that its bulk material is entirely made up of a conductive material like a metal (Fig. 2.9b) or doped diamond. Regarding solid metallic tips, recent progress in fabrication technology made possible to plan and realize tip design with radii below 8nm [Bruker]. This, in fact, is a great leap ahead taking into account that handling process technology for metal bulk tips is quite more difficult than, for example, for silicon, which already is industrially established. Currently, metallic bulk AFM tips based on platinum are commercially available [Bruker]. The most obvious advantage is that the tip does not loose conductivity, as it is made entirely of a conductive material. But because of the abrasive character of CAFM, with an ongoing measurement, the tip radius is negatively affected due to mechanical wear out. Moreover, their price is comparable with those of diamond-varnished silicon tips which also preserve conductivity much longer (although resolution is worse). Bulk doped-diamond tips (which are already commercial) are also a very good option, which exhibit a superior endurance compared to coated silicon and metallic bulk AFM tips. However, they are also very expensive.

Another possibility to increase AFM probes lifetime is by using tips based on CNT (carbon nanotubes, shown in Fig. 2.9c). The concept of introducing CNT in tips for scanning probe microscopy related techniques was firstly discussed by Dai [Dai 96]. In this case, a nanotube of carbon is fixed to a standard AFM tip with a typical radius of 10nm and is used to scan the surface under analysis. Initially, their fabrication was very

difficult due to problems related to the growth and/or attachment of the CNT on the apex of the AFM tip. However, after roughly 15 years of research, many obstacles have been resolved, such as the selective fabrication of carbon nanotubes instead of their initial uncontrolled growth and the method to fix it on the AFM tip. Nowadays, for example, methods to manually attach CNT on silicon tips or to grow them directly on the tip by CVD-based methods are already available [Hafner 99]. Such probes offer a much greater scanning lifetime than standard ones and combine the abilities to achieve high resolution and measure high-aspect ratio features at the same time in tapping/intermittent contact mode. But on the other side, they triple the costs compared to doped diamond-coated tips and for some applications they are not suitable.

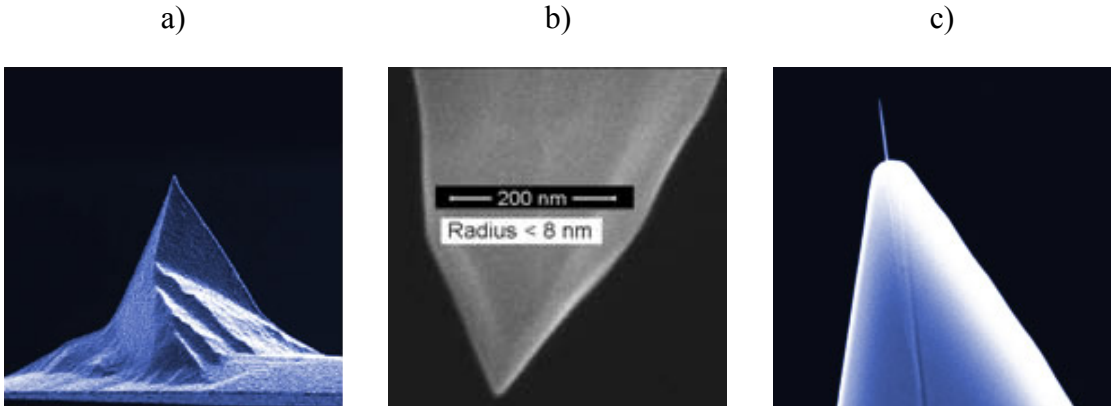

Figure 2.9. SEM images of a (a) diamond-coated [Bruker], (b) solid-metal [Bruker II], and (c) carbon-nanotube [Bruker III] AFM probes.

For example, in [Martinez 05] it was demonstrated that, when working in tapping mode, the use of longer CNT better reproduce sharper topographical changes but, on the other hand, artifacts are also measured, probably due to bending effects during oscillation. For contact mode measurements, CNT based tips aren't also suitable since bending effects when scanning the surface provoke false topographical information. Therefore, due to the mechanical properties of CNT, in order to integrate them into contact mode AFM applications, such as CAFM experiments, more research effort has to be made. One step into this direction was made by [Austin 06], where the transport properties as a function of the contact quality were investigated. To do so, a p-doped silicon and a metallic surface is contacted with a multi-walled carbon nanotube (MWCNT), showing diode-like and linear IV behavior, respectively. An approach to determine electrical properties of CNT AFM tips in standard measurements such as IV curves, is presented in [Austin 06], where local IV characteristics on Platinum surfaces are carried out with a Ni coated AFM tip with a CNT attached. The experiment reveals a different metallic conduction behavior between Ni and the CNT. However, reliable topographical and current images cannot be obtained due to bending effects.

Therefore, despite the CAFM experiments are normally performed with Si tips coated by special alloys, such as Pt-Ir or doped diamond, alternative tips to overcome all these inconvenients are still needed. In this thesis (chapter 5), a novel graphene coated tip for CAFM measurements is presented.

2.6 Setups used in this investigation

In this thesis different experimental setups have been used to perform CAFM experiments. In the following, their main characteristics are described.

Setup A: Agilent 5100

This AFM is located at the laboratories of the Electronic Engineering department of the UAB (Autonomous University of Barcelona). It allows performing topographic (in contact and tapping mode), current and CPD measurements, in ambient air and under controlled conditions. The detectable current ranges between 500fA and 10nA at a maximum voltage of ±10V, although it can be increased to 1mA when using the ECAFM or log CAFM configuration [Aguilera 08]. An external temperature module that can operate at temperatures of up to 240°C can be connected.

Setup B: Digital Instruments 3100

The setup is located at the University of Applied Sciences Deggendorf (Germany). This setup was provided with CAFM and KPFM modules (to measure current and CPD, respectively). It can be operated in ambient air conditions and allows to detect a current between 0.2pA and 100pA.

Setup C: Seiko SPA300HV

The setup is located at the Department of Physics, State Key Laboratory for Mesoscopic Physics at the Peking University. It offers the possibility to perform measurements such as CAFM and KPFM under high-vacuum conditions ($<10^{-6}$Torr). Its current range starts at 0.5pA and reaches 100nA.

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Chapter 3: Nanoscale and Device Level Electrical Properties and Reliability of HfO_2 based MOS devices

In chapter 1 it was introduced that the inclusion of high-k dielectrics in CMOS technologies has associated some drawbacks that have been and are still being deeply investigated. For example, the SiO_2 substitute must, among many other properties, be thermodynamically stable on Si and compatible with the gate electrode material and high temperature CMOS processes [Casey 10]. In terms of intrinsic defects, thermal stability, carriers mobility in the channel region and interaction with Silicon bulk, HfO_2 shows much better performance than many of the high-k materials investigated to date, which made it one of the best candidates to replace the SiO_2 in future MOS applications. This chapter will be devoted to the analyses of how fabrication process related parameters of high-k based MOS capacitors affect their electrical properties and reliability. In particular, it will be dedicated to the study of the electrical properties of HfO_2 based gate stacks grown with different ALD precursors and subjected to different annealings. The effect of an electrical stress will be also considered. Although global information of the electrical properties of the devices is very important to know their performance and to make reliability predictions, to study in detail the uniformity of such dielectrics, standard electrical characterization techniques at wafer level are not the most suitable because they can only provide averaged information of the properties of the entire gate oxide of the device under investigation. In this sense, Conductive Atomic Force Microscopy (C-AFM), which can study areas of a few hundred of nm^2, has become a very useful technique in the study of CMOS gate oxides. In this chapter, the study has been performed at both, the nanoscale, using a CAFM (Conductive Atomic Force Microscope) and a KPFM (Kelvin Probe Force Microscope), and at device level. Both analyses have allowed establishing a link (if any) between the nanoscale properties and the reliability and gate conduction homogeneity of fully processed MOS devices.

3.1 Gate Conduction variability and Reliability of HfO_2-bases MOS devices

Intrinsic process variability and aging mechanisms strongly affect the device performance and reliability, especially in ultra-scaled MOS devices [Asenov 08]. Electrical characteristics of such devices may show large device-to-device variability, which is ultimately associated with the discrete nature of matter and charge (see chapter 1). The homogeneity of the morphological and electrical properties of the high-k gate stack is also expected to affect the variability of the electrical properties of scaled devices. However, few works have been devoted to investigate the link between the nanoscale electrical properties and the variability and reliability observed at device level, i.e., on fully processed MOS devices. In this section, a CAFM and KPFM have been used to investigate how the thickness and the crystallization of an HfO_2 layer affect the nanoscale properties of the gate stack. The impact of such nanoscale properties on the reliability and variability of the electrical properties of fully processed MOS devices was also studied. Finally, how an electrical stress affects the nanoscale and device level properties of amorphous and polycrystalline structures is also investigated (**PUBLICATION 1 and 2**).

3.1.1 Experimental

The investigated samples consist of MOS capacitors ($3x3\mu m^2$) with an Aluminum gate electrode and a HfO_2 film as gate dielectric deposited at 225ºC by atomic layer deposition (ALD) on a Si (n-type) substrate (Fig. 3.1.a) using Tetrakis(dimethylamino)hafnium (TDMAHf) and H_2O as precursors. The oxide thickness (3.6 or 5.3nm thick, as measured by ellipsometry on as-deposited layers) was chosen thick enough to get a HfO_2 monolayer with crystals as big as possible (which improves the experiments resolution, Fig. 3.1b) and thin enough to avoid the growth of a multilayer stack [Vanessa 10]. A multilayer stack would make the analysis of individual nanocrystals more difficult (Fig. 3.1c). Some of the structures were annealed before gate deposition in nitrogen ambient during 30 minutes at high temperature ($T_{Annealing}$=800°C) to get a polycrystalline high-k layer, while others were kept amorphous ($T_{annealing}$ = 350°C). The schematics of the samples and their main features are shown in Fig. 3.1a. For both $T_{Annealing}$, fresh (non-stressed) and stressed (by a Constant Current Stress, CCS, at 5nA during 300s or until BD) capacitors were analyzed at the nanoscale and at device level to evaluate the impact of an electrical stress. The nanoscale electrical properties of the structures were investigated with CAFM and KPFM after the Aluminum (the Aluminum alloy has a content of 0.5% Cu in order to avoid electro migration) gate was removed with a highly selective wet etching.

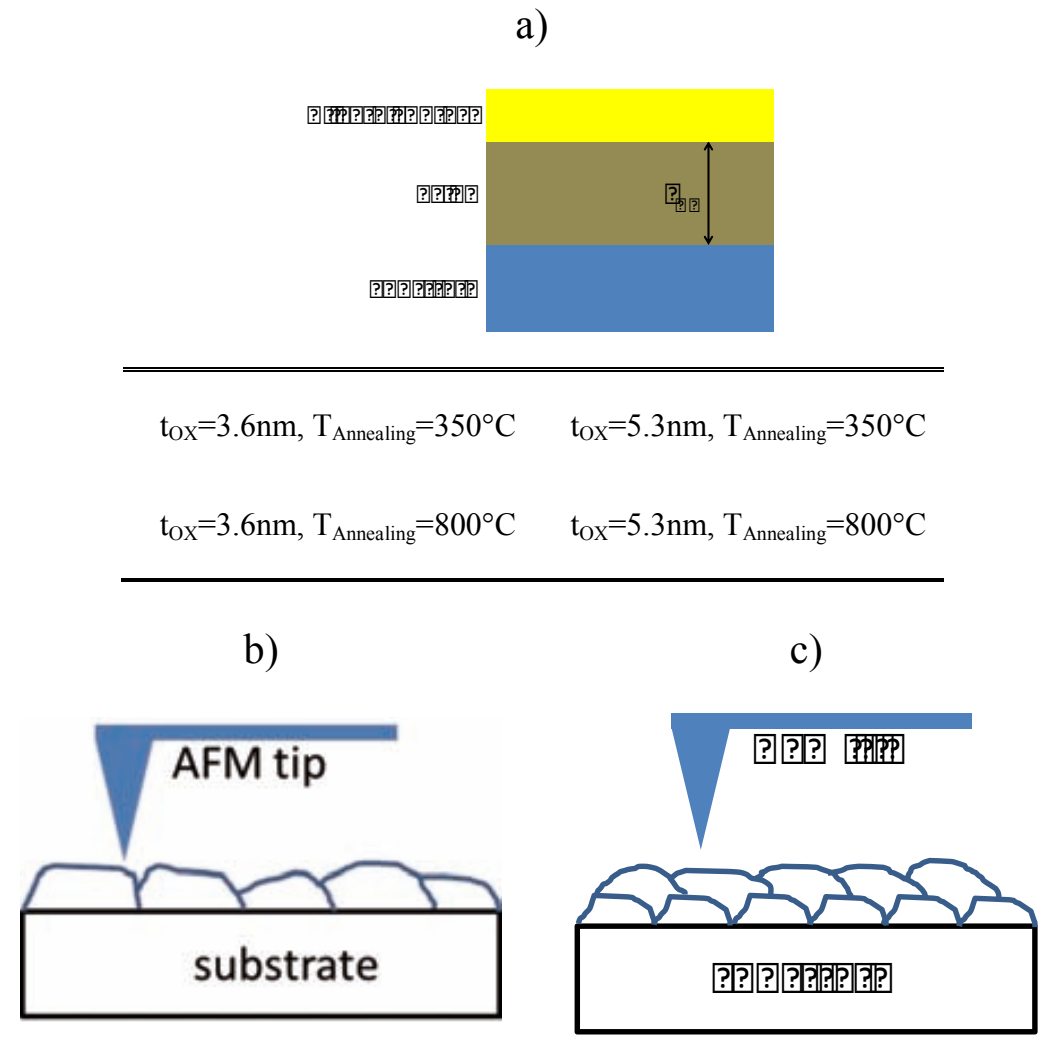


Figure 3.1. (a) Schematic of the analyzed high-k structure. Different temperature treatments ($T_{Annealing}$) and high-k dielectric thicknesses (t_{ox}) were studied. (b) and (c) correspond to different polycrystalline high-k layer structures depending on the thickness of the HfO_2 film. (b) Monolayer with nanocrystals as big as possible which allows studying individual grains. (c) Multilayer of nanocrystals which makes the analysis of single grains more difficult.

The etching selectivity between gate dielectric and contact material must be high, in order to assure that the layer of interest is not affected or at least left in proper conditions for consecutive experiments without having changed its structural and electrical properties. In this case a chemical etching solution known as "piranha" consisting of H_2SO_4(85%):H_2O_2(30%) = 1:1 was used. Several tests removing the gate material were made with different etching times until no residues could be detected in the topography. Fig. 3.2 illustrates the corresponding AFM topographical images at different stages of the etching process: (a) corresponds to the sample with the Al gate contact (prior to etching), (b), (c) and (d) after the partial/complete removal of the gate contact when different etching times were used. In (b) and (c), big islands of the gate material are still present. However, in (d), after an etching of 5 minutes the image

appears quite homogeneous without topographic indications of residual material coming from the gate electrode. This leads to the conclusion that the etching solution is appropriate for reaching the gate dielectric and does not cause morphological damage of the HfO_2 layer.

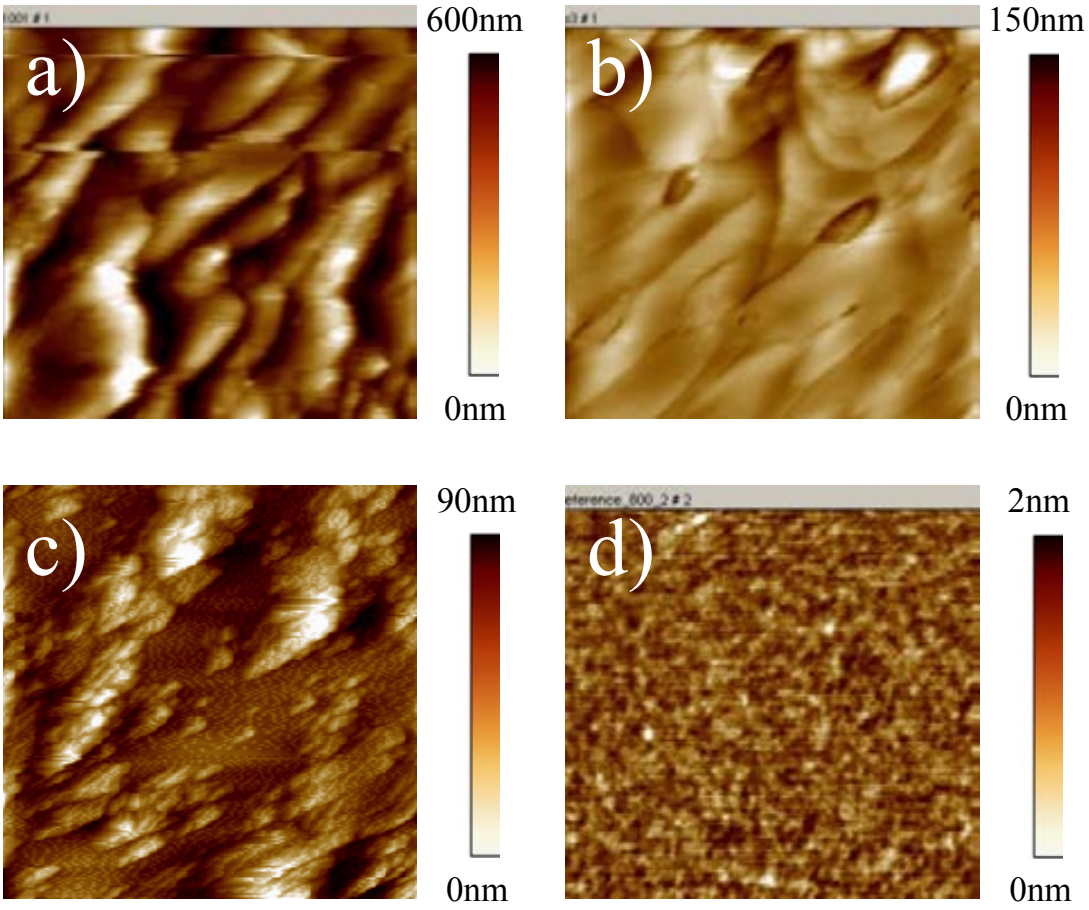


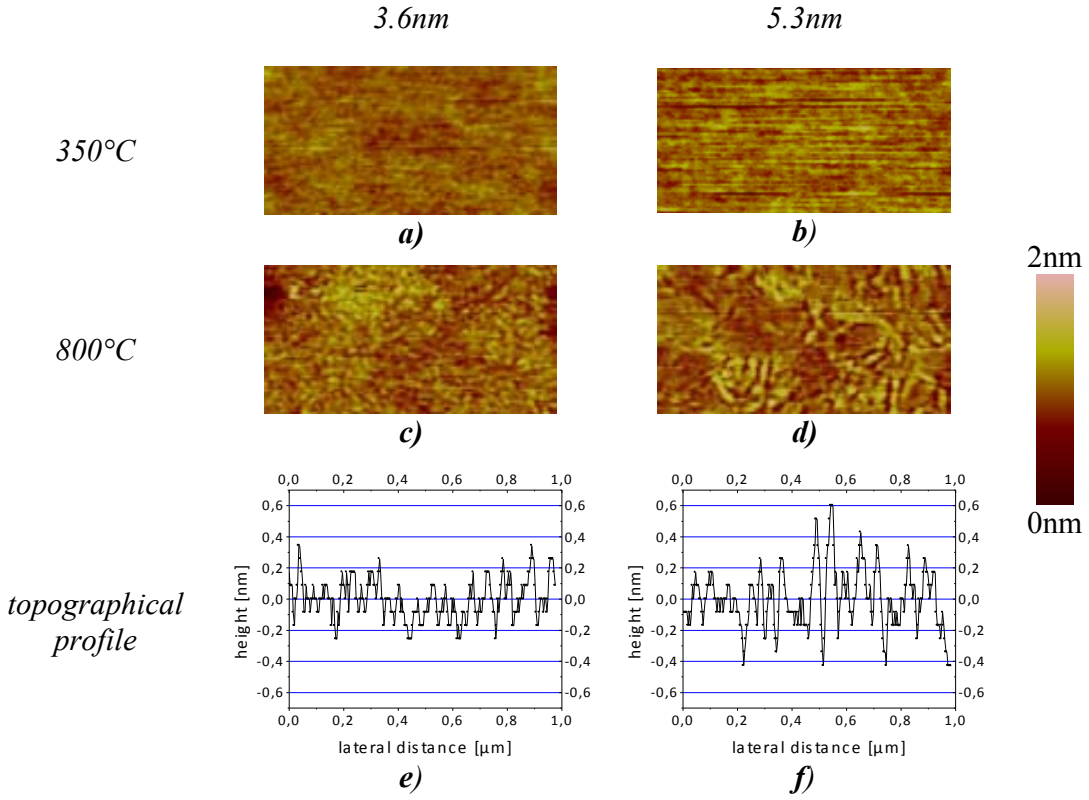
Figure 3.2. AFM topographic maps after different etching times. (a) as-received sample, where the metal contact layer still was not exposed to the etching solution. (b), (c) and (d), after 1min, 4mins and 5mins, respectively. The images represent an area of 1x1µm²

After the etching of the gate electrode, with the C-AFM, current and topography maps were obtained when applying a constant voltage between the tip and the sample during the scan. I-V curves measured at different oxide locations were also registered. With the KPFM, the contact potential difference (CPD) between the tip and the substrate can be obtained. Since in a MOS capacitor the CPD depends not only on the materials of the structure but also on the presence of charge in the dielectric, this technique can provide information about the charge trapped in the gate stack, which can be considered to be proportional to the density of defects. In CAFM and KPFM experiments, Silicon tips coated with a layer of Pt/Ir have been used and the measurements have been performed in air. The impact of the observed nanoscale properties on the variability of the global electrical behavior and on the reliability of fully processed MOS devices was analyzed from the measurement of their I_G-V_G curves with a semiconductor parameter analyzer. Device level and nanoscale measurements were performed on capacitors of the same wafer and in the same die, to avoid wafer-to-wafer and die-to-die variability.

3.1.2 Analysis at the nanoscale of as-grown structures

a) Morphology

To begin with, the impact of the annealing and the oxide thickness on the nanoscale morphological properties was investigated with CAFM from the analysis of topographical maps after removing the gate contact. Fig. 3.3 shows topographical images of the (a), 3.6nm-350ºC, (b), 5.3nm-350ºC, (c), 3.6nm-800ºC and (d), 5.3nm-800ºC high-k layer. The figure also includes a table with the root mean square, rms, values of the heights measured on the different images, which is indicative of the surface roughness. Note that images (c) and (d), corresponding to the annealing at 800ºC, show a granular structure which is not visible in the gate stacks annealed at 350ºC, leading to a larger rms value. This granularity has been attributed to the polycrystalline microstructure of the high-k layer after the high temperature treatment, as other works have observed [Paskaleva 08, Gusev 03, Vanessa 10], whereas thermal treatment at the lowest temperature (350°C) maintained samples in their amorphous phase. In the polycrystalline structure (annealed at 800ºC), the grains observed in the topographical map are related to individual (or a cluster of) randomly oriented nanocrystals separated by grain boundaries (GBs), which correspond to the depressed regions in the image. Although the local thickness (t_{ox}) of the gate dielectric depends not only on the scanned top surface (gate/dielectric) but also on the dielectric/bulk interface (information not available in this experiment, since topographical maps only provide information on the top interface), it is reasonable to assume similar characteristics of both interfaces. Therefore, the larger topographical inhomogeneity observed in the higher temperature annealed samples suggests larger local thickness (t_{ox}) fluctuations within the polycrystalline structures. A statistical analysis of the grains in the polycrystalline structures shows that their average size is ~130 and ~230 nm² in the case of the 3.6 and 5.3nm thick gate dielectric, respectively, suggesting that the grain size, which is compatible with the results in [Lanza 11], depends on the high-k layer thickness, as reported in [Gusev 03]. Note that, although in thicker polycrystalline high-k layers nanocrystals are bigger, their surface roughness is also larger, which could be related to the fact that, in thicker oxides, GBs could be deeper (see Fig. 3.3 e and f, which correspond to topographical profiles of the images shown in Fig. 3.3 c and d). When comparing samples annealed at the same temperature but with different thickness (e. g. samples (*a)* and *(b)* or *(c)* and *(d)* in Fig. 3.3), the results show that the thicker stack is more inhomogeneous than the thinner one, leading to larger rms values (although to a lesser extent than that due to the polycrystalline microstructure). In the thicker amorphous samples, the larger rms value could be a consequence of the larger defect density in these oxides [Garcia 08], which can provoke additional topographical fluctuations due to the electrostatic interaction between the tip and trapped charge in those defects [Porti 02], i. e. an artifact of the technique. On the other hand, in polycrystalline samples, the increase of the topographical fluctuations in thicker dielectrics can be related to the dependence of the crystallization temperature (T_C) on the thickness. Gusev et al. [Gusev 03] demonstrated that, for HfO_2 stacks, the larger the oxide thickness, the lower T_C. Since crystallization is a progressive process, for the same annealing temperature, crystal development could be in a more advanced phase in thicker dielectrics and, consequently, resulting in a larger topographical inhomogeneity in these stacks.



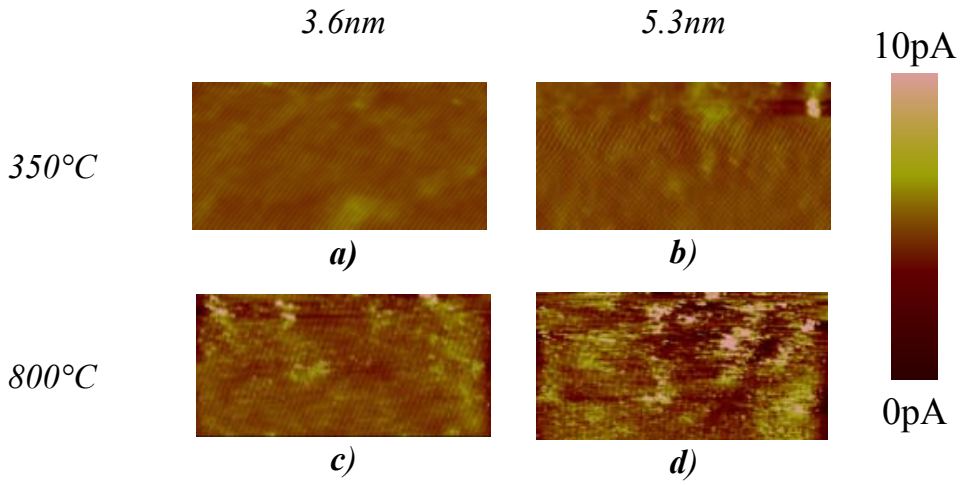
Rms value			
350°C		*800°C*	
3.6nm	*5.3nm*	*3.6nm*	*5.3nm*
0.13nm	*0.15nm*	*0.18nm*	*0.23nm*

Figure 3.3. Topographical images of 3.6nm (a,c) and 5.3nm (b,d) thick HfO_2 layers annealed at 350°C (a,b) and 800°C (c,d). The size of all images is 1x0.5µm². After the 800°C annealing, the topographical images show a granular structure that suggests a polycrystalline microstructure of the high-k layer. e) and f) correspond to topographical profiles of images c) and d), respectively. A table with the rms value measured on the different images is included.

b) Electrical conduction

The impact of the high-k layer polycrystalline microstructure on the nanoscale conduction properties of the stack has been investigated from the measurement of current images and I-V curves by CAFM. Fig. 3.4 shows current images of the (a), 3.6nm-350ºC, (b), 5.3nm-350ºC, (c), 3.6nm-800ºC and (d), 5.3nm-800ºC high-k layer obtained at those voltages at which current is measured just above the noise level (i.e., the same amount of current and, therefore, equivalent electrical fields) to guarantee equivalent measurement conditions. The table in Fig. 3.4 indicates the rms value of the current registered in each image. The electrical effects of the polycrystalline microstructure have been analyzed by comparing images *(a)/(c)* and *(b)/(d)* (same thickness, different phase). Note that current images do not show a clear granular structure as topographical maps (Fig. 3.3). This could be related to the fact that the

measurements were carried out in air, which reduces the CAFM resolution. Actually, in [Vanessa 11b] it was demonstrated that UHV conditions improve the electrical resolution of CAFM experiments. However, leaky sites show larger currents on the polycrystalline samples ((*c)* and (*d),* annealed at 800ºC), which leads to higher rms values of the current compared to the amorphous structures ((*a)* and (*b))*. Since in polycrystalline samples GBs are more conductive [Vanessa 10], the leaky sites measured in these structures would correspond to the GBs measured in Fig. 3.3. These results are further supported by CAFM I-V curves. Fig. 3.5 shows four sets of 15 I-V characteristics registered at different positions on the 3.6nm and 5.3nm-thick gate stack at both annealing temperatures. A maximum current of 100pA can be measured due to the saturation of the CAFM electronics. Note, for example, that, for the same annealing temperature, the electrical conduction is higher for thinner oxides, as expected.



Rms value			
350°C		*800°C*	
3.6nm	*5.3nm*	*3.6nm*	*5.3nm*
0.24pA	0.55pA	1.02*pA*	*6.57pA*

Figure 3.4. Current images of 3.6nm (a,c) and 5.3nm (b,d) thick HfO_2 layers annealed at 350°C (a,b) and 800°C (c,d). A table with the rms value of the different images is included. Note that, in polycrystalline structures, the electrical inhomogeneity of the HfO_2 layers increases. The size of all images is 1x0.5μm².

However, when comparing structures with the same thickness but different annealing temperature, the electrical conduction is reduced after the high temperature treatment. This apparent contradiction with Fig. 3.4 can be explained by considering that although GBs are more conductive, the IV curves shown in Fig. 3.5 (obtained on randomly distributed positions over the surface) probably have been obtained on nanocrystals (which cover a much larger area than GBs), being less conductive [Lanza 11]. Moreover, it must be also to taken into account that an annealing can also lead to changes in the thickness of the layer of the stack through oxidation of the silicon substrate, as demonstrated in other works [Lanza 11], and/or to a defect density reduction. However,

the goal of this section is not to evaluate the absolute value of the electrical current (which could also depend on many experimental factors, such as the contact area between the tip and the sample, tip wear out …), but the homogeneity of the electrical properties. To investigate the electrical homogeneity obtained at the nanoscale, the dispersion of the gate current has been evaluated considering the gate voltage necessary to measure a current of 20pA (V_I) as parameter (Table 3.1, first row). Therefore, using this parameter, the smaller the V_I, the larger the oxide conductivity. Note that the dispersion of V_I and, therefore, of the electrical conduction, increases in the polycrystalline samples, in agreement with the data obtained from current images. Finally, although the most important source of dispersion in the electrical conduction is the gate dielectric polycrystalline microstructure, the thickness of the high-k layer has also an effect (though smaller) on the gate current, leading to larger dispersions in thicker oxides (see the rms value of the current images and the I-V curves shown in Fig. 3.4 and 5, respectively).

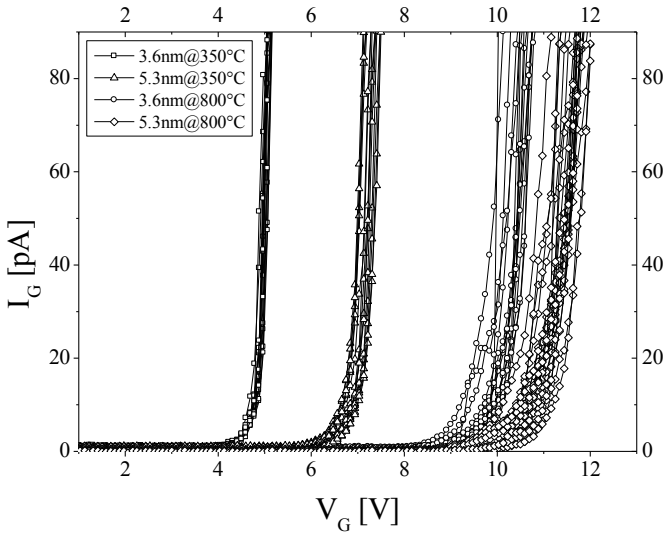


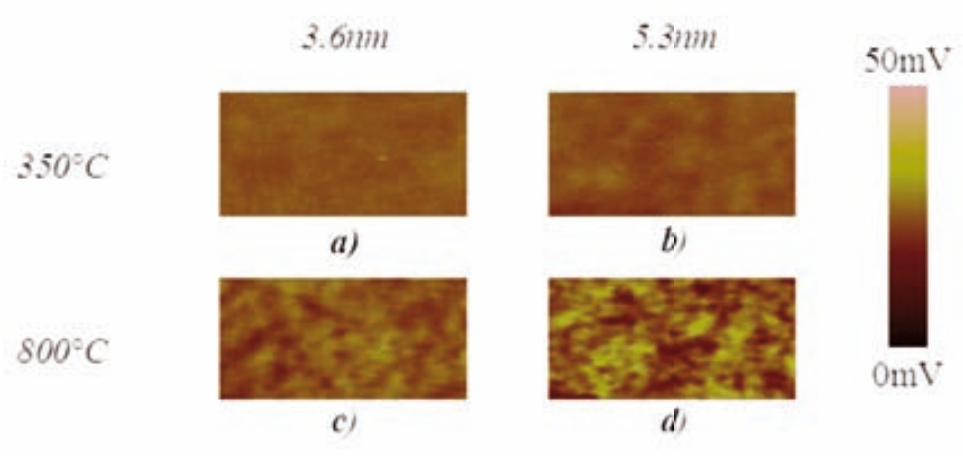
Figure 3.5. Sets of I-V curves measured with the CAFM (areas of ~100nm^2) on HfO_2 layers with different thickness and annealed at different temperatures. Note that, as the thickness and annealing temperature increases, samples show a larger dispersion.

	Dispersion of V_I [mV]			
Sample	3.6nm @350°C	5.3nm @350°C	3.6nm @800°C	5.3nm @800°C
Nanoscale measurements	50	105	150	265
Device level measurements	4	16	44	81

Table 3.1. Dispersion of the gate voltage (V_I) necessary to measure a current of 20pA and 20nA in the I-V curves obtained with CAFM (first row, nanoscale measurements) and at device level (second row, device level measurements), respectively.

c) Charge trapping

Finally, the different samples have been also analyzed with KPFM, which can provide information about the presence of charge and trapping centers in the stack. Fig. 3.6 shows CPD images of the (a) 3.6nm-350ºC, (b) 5.3nm-350ºC, (c) 3.6nm-800ºC and (d) 5.3nm-800ºC high-k layers. The table in the same figure shows the CPD rms value obtained on each image. Note again that CPD maps do not show a granular structure as topographical images, probably due to a lack of resolution in air conditions [Vanessa 11b]. However, a statistical analysis of the CPD images shows that the rms value increases again with thickness but, specially, after crystallization. This increase of the CPD signal fluctuations on crystalline samples could be related to the fact that the defects or trapping sites generated in the polycrystalline microstructure of the HfO_2 layer are less uniformly distributed (probably they are mostly localized around the grain boundaries), which could also enhance the non-homogeneity observed in current images [Vanessa 10]. The excess of charge and/or trapping centers at GBs could be related to the segregation of positively charged oxygen vacancies near the GBs, which were shown to form a percolation path [Bersuker 10], which allows charge carrier transport along GBs.



Rms value			
350°C		*800°C*	
3.6nm	*5.3nm*	*3.6nm*	*5.3nm*
1.6mV	*2.5mV*	*4.1 mV*	*8.4 mV*

Figure 3.6. CPD images of HfO_2 layers with different oxide thickness and annealed at different temperatures. A table with the rms value of the different images is included. Note that, in polycrystalline structures, the CPD inhomogeneity of the HfO_2 layers increases. The size of all images is 1x0.5μm².

3.1.3 Device level analysis of as-grown structures

In this section, in an effort to evaluate the impact of the previously analyzed nanoscale variability sources on the global electrical properties of MOS capacitors, fully-processed devices with equal gate dielectrics than those studied with CAFM have been investigated with standard characterization techniques. In particular, the gate conduction

and electric field at breakdown (E_{BD}) of Al-gated MOS devices have been studied. To avoid die-to-die variability, all the measured devices were on the same die.

a) Impact of nanoscale variability sources on the device level electrical conduction variability of MOS capacitors

The impact of the nanoscale variability sources on the gate electrical conduction of fully processed MOS devices is analyzed in this section. Fig. 3.7 shows some examples of I-V curves obtained on MOS capacitors ($3x3\mu m^2$) with a (a) 3.6 and (b) 5.3nm-thick HfO_2 layer, annealed at 350ºC (squares) and at 800ºC (triangles). The I-V curve in circles corresponds to a typical post-breakdown (BD) I-V characteristic as reference, which shows larger currents due to the loss of the dielectric properties of the gate stack. The gate current dispersion has been evaluated from the gate voltage at which a current of 20nA flows through the MOS capacitor, V_I, which is included in table 3.1 (second row).

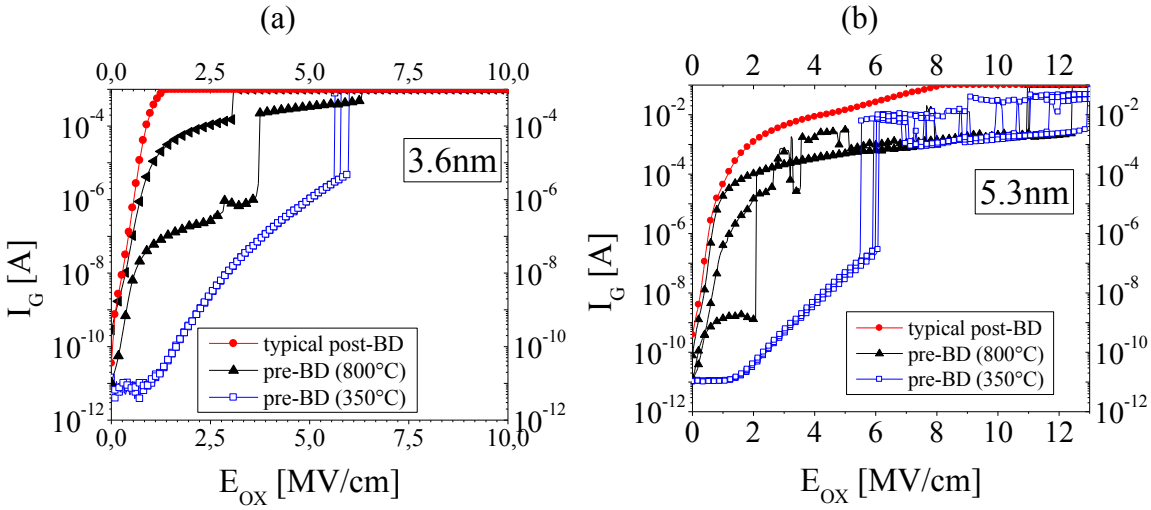


Figure 3.7. Examples of I-E_{OX} curves obtained on MOS capacitors (Area of 9µm²) with a (a) 3.6 and (b) 5.3nm thick HfO_2 layer. Note that after the high temperature annealing (800ºC, triangles), pre-BD conduction is higher and more erratic that that measured in samples with a low temperature annealing (350ºC, squares).

Note that two clear different behaviors can be identified in Fig. 3.7a and b, which correspond to amorphous and polycrystalline samples. In the amorphous structures (squares), before BD, the current follows the typical Fowler-Nordheim behavior for these kind of structures, with a very small dispersion, which slightly increases in thicker oxides (Table 3.1, second row), in agreement with the CAFM I-V curves (Fig. 3.5). However, in polycrystalline samples (triangles), at low fields, the gate conduction is larger than in amorphous gate dielectrics, with a very erratic and non-stable behavior (leading to larger V_I dispersions, Table 3.1), suggesting different conduction modes, which can change from sample to sample. At high fields, current increases even more, and show the typical post-BD behavior. Since in polycrystalline structures a larger nanoscale morphological and electrical inhomogeneity was observed due to the presence of GBs, the erratic behavior observed in these gate stacks at device level could be related to the differences in the electrical behavior of nanocrystals and GBs, the last ones being much more conductive (probably due to the high density of oxygen

vacancies [Bersuker 10b] located at these positions) and whose conduction mechanisms are still not clear. Note, moreover, that the total current through fully processed polycrystalline structures is larger than in amorphous samples (Fig. 3.7), which suggests that polycrystalline layers show a larger conductivity. This seems to be in contradiction with the CAFM currents (Fig. 3.5). Moreover, at the nanoscale, although the dispersion increases in the polycrystalline samples, the I-V curves measured with the CAFM didn't show the erratic and non-stable behavior observed at device level (Fig. 3.7). This apparent contradiction, however, can be explained by taking into account the different areas analyzed in each case. At device level, the current through the complete gate area is measured ($9\mu m^2$), which corresponds to the superposition of currents flowing through about 10^4 spots like those measured with the CAFM (Fig. 3.4). That is, currents through all the leaky sites (probably at GBs) are measured which, in addition, could have suffered from a BD event during the measurement [Vanessa 11b]. Contrarily, at the nanoscale, a much reduced number of spots can be measured, so that the probability of finding such leaky or broken down sites is very small. Moreover, the reduced current dynamic range of the CAFM does not allow determining whether the spots broke down during their characterization. All these factors make not possible to draw definitive conclusions on the current absolute value, but only on its variability.

b) Impact of nanoscale variability sources on the reliability of MOS capacitors

The impact of the polycrystalline microstructure of the high-k layer on the reliability of the MOS capacitors was also investigated by measuring the electrical field at which the structures break down, E_{BD}, during a RVS (ramped voltage stress). The Weibull distributions obtained on gate stacks with different HfO_2 thicknesses and subjected to annealing processes at different temperatures are shown in Fig. 3.8, which includes the corresponding values of the Weibull slope (β) and the electric field for 63% broken down capacitors ($E_{BD,63\%}$). Note that smaller electric fields and slopes (which correspond to larger dispersions of E_{BD}) are measured on the polycrystalline structures (and on thicker oxides), that is, in those samples in which the variability observed at the nanoscale was larger. The reduction of β in the polycrystalline samples is of special relevance.

Since, from the percolation model, β is proportional to the number of traps needed to trigger BD [Suñé 11], the smaller value of β obtained in the polycrystalline samples indicates that, in this case, less traps have to be generated during the stress to create a BD path. This could be related to the fact that the as-grown polycrystalline structures already have a higher density of native defects (before the stress) [Raghavan 09], probably related to O-vacancies [Bersuker 10b], which favor the excess of leakage current measured in current maps [Vanessa 10]. Since less traps have to be generated during the stress, BD is triggered at smaller voltages ($E_{BD,63\%}$) in those devices with polycrystalline high-k dielectrics. Therefore, these results indicate that the nanoscale variability sources (polycrystalline microstructure in particular) not only affect the variability of the electrical properties of non-stressed MOS devices, but also their reliability (**PUBLICATION 1**).

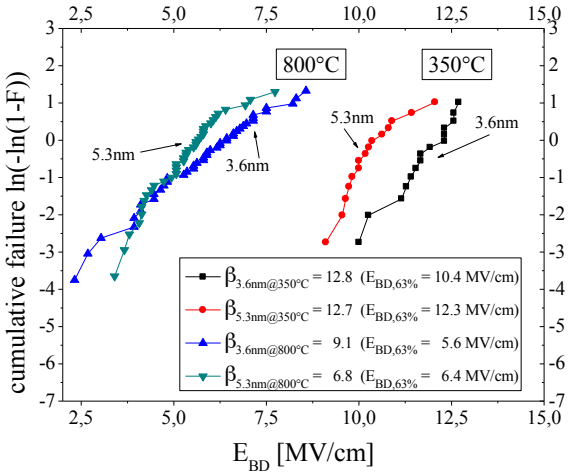


Figure 3.8. E_{BD} Weibull distributions obtained after applying a RVS on MOS capacitors with different HfO_2 layer thickness and subjected to an annealing at different temperatures. The Weibull parameters are also included in the figure.

3.1.4 Effect of an electrical stress on the nanoscale properties and device level variability

Once the impact of the annealing process and oxide thickness of the high-k dielectric on the nanoscale properties and device level variability and reliability of as-grown MOS capacitors was investigated, the effect of an electrical stress is also analyzed **(PUBLICATION 2)**. In this case, MOS capacitors were first stressed at device level by means of a CCS of 5nA during 300s. As an example, Fig. 3.9 shows the V-t curves measured in some of the capacitors. Note that the voltage applied to inject 5nA is quite constant (triangles). In some of them, it suddenly drops (squares and circles), indicating the breakdown of the structure. To study the effect of the stress, only those not broken down were considered. After that, I-V curves were measured to compare the effect of the stress on the device conduction and its variability (see section 3.1.4b). Finally, the gate electrode was removed by means of an etching described in section 3.1.1 and the gate area was scanned with the CAFM. Some structures were not stressed, which have been considered as reference.

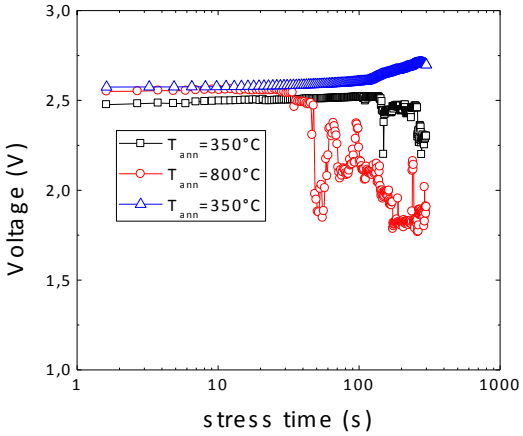


Figure 3.9. V-t characteristics obtained on MOS capacitors annealed at 350°C (squares and triangles) and at 800°C (circles) that have been stressed at device level by means of a CCS of 5nA during 300s.

a) Nanoscale variability

We will start investigating the impact of the stress on the nanoscale properties. As an example, Fig. 3.10 shows topographical images of amorphous (a and c) and polycrystalline (b and d) HfO_2 layers before (a and b) and after (c and d) being electrically stressed with the CCS. In this case, only capacitors with a 3.6nm thick high-k layer were studied. Again, before the stress, the polycrystalline sample (Fig. 3.10b) shows a granular structure, leading to a larger rms value of the surface, which is not observed in Fig. 3.10a (amorphous). After the stress (Fig. 3.10c and d, obtained on amorphous and polycrystalline gate stacks, respectively), the topographical inhomogeneity increases with respect to unstressed samples (Fig. 3.8a and b). This effect can be probably related to artifacts of the measuring technique associated to charge trapping in the defects generated during the CCS [Porti 02]: the trapping/detrapping of elementary charges in/from the defects created during the stress can lead to additional electrostatic interactions between the C-AFM tip and the gate stack. These interactions are interpreted by the C-AFM setup as topographical fluctuations which, actually, are not real. Since Fig. 3.10 shows, after the stress, a larger increase of the rms value on polycrystalline samples, these results suggest that the spatial distribution of the defects is more inhomogeneous in those samples compared to those that are amorphous. The more inhomogeneous behavior observed in polycrystalline samples could be related to the fact that these defects are mostly concentrated at GBs, since it was demonstrated that these regions are weaker from an electrical point of view and degrade faster than NC [Vanessa 10].

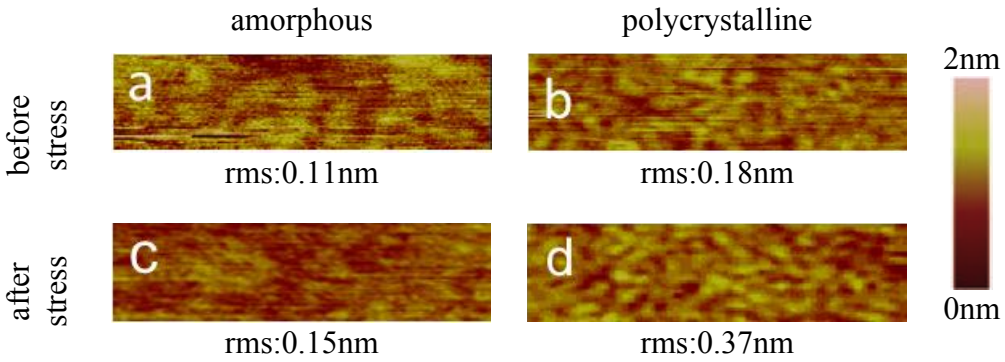


Figure 3.10. Topographical images obtained on the (a and c) amorphous and (b and d) polycrystalline gate stack, before (a and b) an after (c and d) the electrical stress. The surface roughness is also included in the figure. The size of all images is 1x0.25µm².

The impact of an electrical stress on the nanoscale electrical conduction of amorphous and polycrystalline gate stacks has been investigated from the measurement of current images and I-V curves with the C-AFM. Fig. 3.11 shows, as an example, current images measured by applying the minimum voltage that forces a current just above the noise level on amorphous (a and c) and polycrystalline (b and d) samples before (a and b) and after (c and d) the electrical stress. Note that the current rms value follows the same tendency as surface roughness: polycrystalline samples are more inhomogeneous and the stress has a larger impact on such structures, that is, larger changes in the rms values are measured after the stress. These results are further supported by the measured I-V curves.

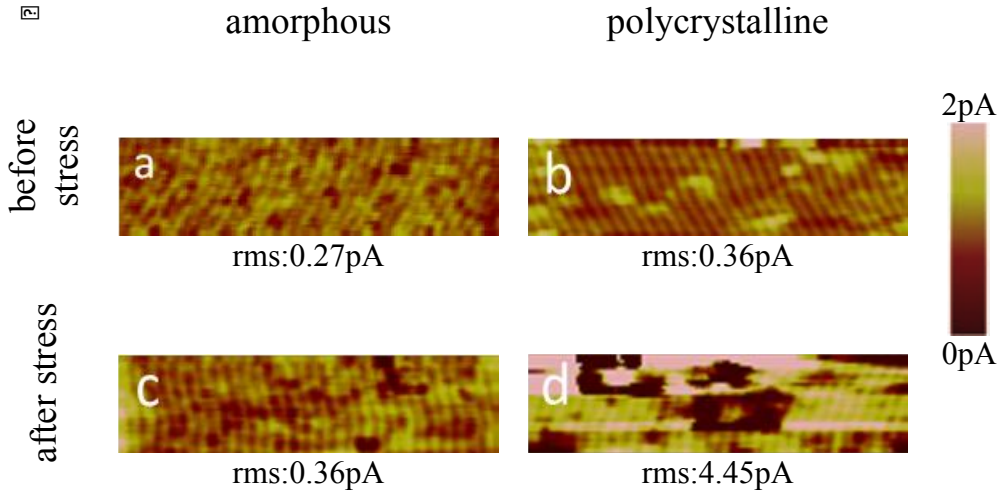


Figure 3.11. Current images obtained on the (a and c) amorphous and (b and d) polycrystalline gate stack, before (a and b) and after (c and d) the electrical stress. The rms value before and after the electrical stress is also included. The size of all images is 1x0.25µm².

Fig. 3.12 shows two sets of I-V characteristics obtained with C-AFM on amorphous (a) and polycrystalline (b) samples, before (fresh) and after the stress (stressed). Table 3.2 (1st and 2nd rows) indicates the mean value and standard deviation of the gate voltage necessary to measure a current of 10pA (V_I), obtained from the I-V curves in Fig. 3.12. Note that, the smaller V_I, the larger the conductivity of the stack. Fig. 3.12 and Table 3.2 show that after the stress, the average electrical conduction is reduced (shift onto larger V_I values), probably due to charge trapping in the defects generated during the CCS.

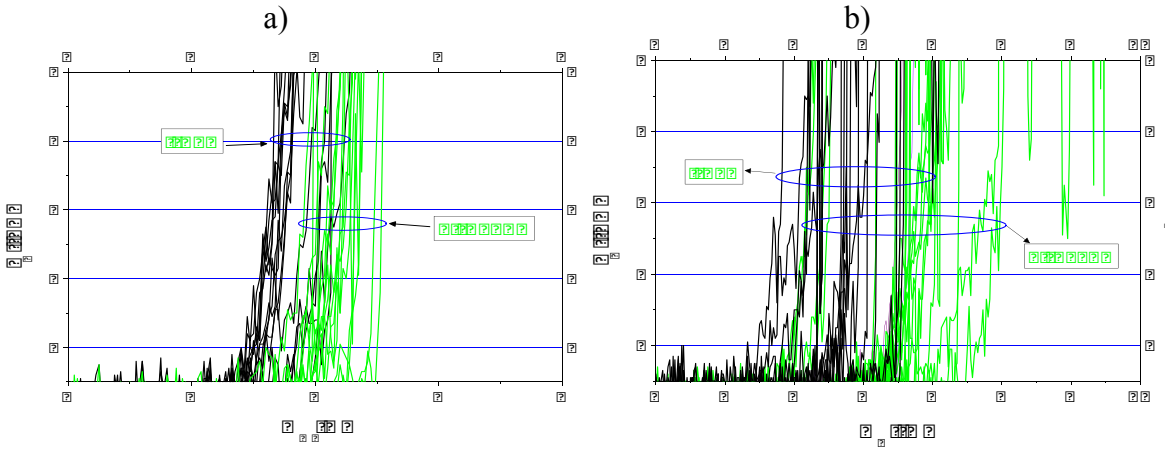


Figure 3.12. I–V curves obtained with CAFM, before and after the stress, on the (a) amorphous and (b), polycrystalline annealed samples. The area of the MOS structure under analysis is determined by the tip-sample contact region, which is of the order of few hundreds of nm^2.

Moreover, again, the dispersion, which is larger after polycrystallization, as already observed in last section, increases and becomes much larger after the stress in polycrystalline structures. This effect could be related to the different electrical properties between GBs and nanocrystals in polycrystalline structures. GBs, probably with an initial excess of some kind of native defects, such as O vacancies (generated during polycrystallization), could be even more affected by the electrical stress, leading to larger fluctuations of the electrical conduction after the stress, detected as an increase of the conductivity deviation (Table 3.2 and Fig. 3.12). Therefore, the results obtained with C-AFM show that the polycrystallization of the high-k layer is an important source of nanoscale electrical variability, which further increases after an electrical stress.

		amorphous		***polycrystalline***	
		fresh	stressed	fresh	stressed
Nanoscale 10pA	$\langle V_I \rangle$ ***[V]***	3.74	4.09	5.72	6.61
	σ [mV]	129	154	247	343
Device level 1nA	$\langle V_I \rangle$ ***[V]***	0.86	0.87	0.25	-
	σ [mV]	4.2	4.9	110	-

Table 3.2. Mean value and deviation of the gate voltage (V_I) necessary to measure a current of 10pA (nanoscale measurements) and 1nA (device level measurements), obtained from the I–V curves in Figs. 3.12 and 3.13, respectively. At device level, in the polycrystalline sample, no data is added since all capacitors were broken down during the stress and post-BD currents are larger than 1nA for very low voltages.

b) Device level variability

Finally, in this section, in an effort to evaluate the impact of the previously analyzed nanoscale variability sources and the effect of an electrical stress on the global electrical properties of MOS capacitors, some of the fully-processed devices have been investigated with standard characterization techniques. In particular, the gate conduction has been evaluated from the I-V characteristics measured before and after the electrical stress. Fig. 3.13 shows some I-V characteristics measured on the amorphous (a) and polycrystalline (b) Al-gated capacitors, before (squares) and after (triangles) the stress. The mean value and dispersion of the onset voltage, V_I, necessary to detect a current of 1nA has been used to quantify oxide conductivity (Table 3.2, rows 3 and 4). At device level (after the stress), in the polycrystalline samples, no data is added since all capacitors were broken down during the stress and post-BD currents are larger than 1nA at very low voltages (see Fig. 3.13b).

First, it must be noted that a direct comparison between the currents in Fig. 3.13a (capacitors data) and Fig. 3.12 (CAFM data) is not meaningful, because experimental factors (such as changes on the tip conductivity, contact area, small variations of the oxide thickness or different gate electrodes) can affect the value of the measured current. However, since we are only interested in relative variations of conductivity, the experimental related differences do not change the conclusions of the work.

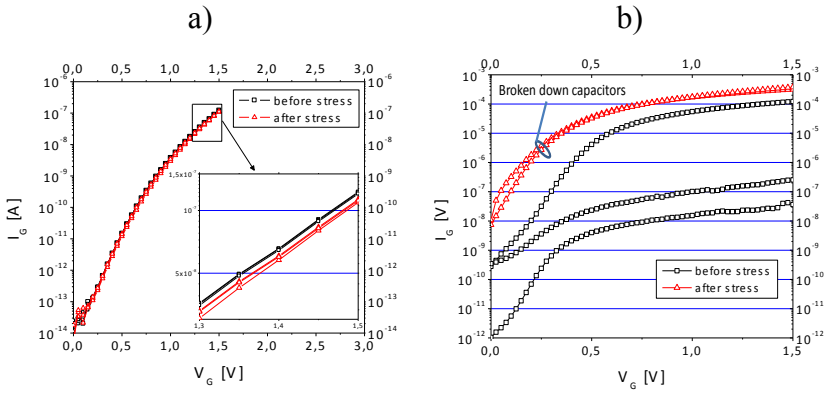


Figure 3.13. I–V curves obtained on Al-gated structures ($3x3\mu m^2$), before (squares) and after (triangles) the stress, on the (a) amorphous and (b) polycrystalline samples.

In Fig. 3.13a (amorphous), those capacitors that do not break down during the CCS show a reduction of the electrical conduction and an increment of the dispersion (table 3.2) compared to fresh structures. Both effects could be related to the random generation of defects during the stress, which could trap charge (shift onto higher voltages) and modify locally the gate stack conductivity (larger fluctuations). In (b), (polycrystalline samples), before the stress, the gate conduction is larger and shows a higher dispersion than that in amorphous gate dielectrics (Fig. 3.12.a), probably due to presence of grain boundaries, which have been found to be leakier [Vanessa 10]. Moreover, all of the capacitors broke down during the CCS. Therefore, these results indicate that polycrystallization of the high-k layer not only affects the variability of the electrical properties of MOS devices, but also their reliability, since they suffer BD events in shorter times (Fig. 3.9) or smaller E_{BD} (Fig. 3.8).

To conclude section 3.1 (**PUBLICATION 1 and 2**), Atomic Force Microscopy (AFM) related techniques have been used to investigate the impact of the thickness and crystallization of high-k dielectrics on the nanoscale morphological and electrical properties of the gate stack. The results show that high-k polycrystalline microstructure and, to a lesser degree, its thickness, affect the homogeneity of the nanoscale surface morphology, conductivity and trapping properties: larger inhomogeneities are observed in thicker and polycrystalline dielectrics. The results obtained in fully processed MOS devices suggest that these nanoscale fluctuations have an effect on their global properties, since smaller E_{BD}, larger gate currents and increased sample-to-sample variability are measured, especially in polycrystalline structures. The results also show that an electrical stress affects differently to amorphous and polycrystalline structures. It was observed that the larger the initial (before any stress) variability of the gate stacks properties (due to polycrystallization of the high-k dielectric in this case), the larger the impact of an electrical stress on their nanoscale and device level electrical properties and reliability. In the case of the polycrystalline samples, this phenomenology has been attributed to an excess of current through the grain boundaries, which have been shown to be more conductive and electrically weaker due to presence of O vacancies in that positions compared to nanocrystals. Therefore, the results show that the fluctuations observed at the nanoscale are transferred to the global electrical characteristics and high-k dielectric reliability of MOS devices: gate dielectrics with polycrystalline microstructure can be an important source of variability and cause of reliability reduction.

3.2 Nanoscale and device level electrical behavior of annealed ALD Hf-based gate oxide stacks grown with different precursors

One of the factors influencing the quality of high-k dielectric films is the deposition process. In particular, Atomic Layer Deposition (ALD), a series of sequential supply alternating an oxidant agent (in this work, H_2O) with a precursor, is described as one of the most promising techniques to obtain excellent uniformity of the deposited layers and accurate film thickness control [Cho 07]. In this case, the precursor used during the growing process is also important to determine the gate stack electrical properties. The homogeneity of the electrical properties of a high-k layer can also be affected by high temperature annealing processes, which are typically used in CMOS technology to, for example, activate dopants. In this section, a CAFM and standard characterization techniques have been used to study, at device level and at the nanoscale, the electrical properties of HfO_2 based gate oxide stacks grown using different ALD precursors (**PUBLICATION 4**). The goal is to analyze the impact of the different precursors on the quality of the resulting high-k layer. In particular, HfO_2 films deposited by ALD using a Hafnium tetrachloride $HfCl_4/H_2O$ (ALD samples) or a tetrakis [ethyl methylaminohafnium] (TEMAHf)-O_3 process (MOALD samples) have been compared. The impact of an annealing treatment (before or after the gate electrode deposition) on the thermal stability and electrical properties of the gate stack, which is a common process in CMOS technologies, is also considered.

3.2.1 Experimental

To study the nanoscale electrical properties of high-k dielectrics and correlate them with those measured at device level, a set of samples were specifically designed and fabricated to allow both kinds of analysis in structures with identical dielectrics [Aguilera 10]. On one hand a set of blankets on a silicon substrate was fabricated. This set was used in order to study at the nanoscale the characteristics of high-k materials grown with different deposition techniques and subjected to different thermal treatment during device processing. This set consists of a HfO_2/SiO_2 gate stack formed by a 2nm thick HfO_2 layer, deposited by ALD or MOALD, above a chemically grown 1nm-thick SiO_2 layer on silicon substrate. The interfacial layer is used to avoid uncontrolled interactions between the substrate and Oxygen atoms of the HfO_2 stack. On this structure, a layer of TiN/polySi is deposited which has a protective function of the dielectric layer to prevent contamination. Fig. 3.14 shows a cross section of the analyzed structures and the technological process that were studied.

Apart from the blanket samples, a set of wafers with squared MOS capacitors ranging from $1x1\mu m^2$ to $50x50\mu m^2$ were also fabricated with identical gate stacks. The values of the areas of the MOS capacitors were chosen to make possible measurements at the nanoscale with the CAFM and at device level, as well, in the same structures. In the case of MOS devices, layers of TiN/PolySi have the function of gate terminal contact.

High-k	Annealing @ 1030°C
ALD MOALD	Before After No annealing

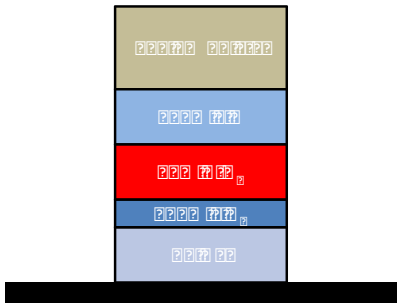


Figure 3.14. Cross-section of the sample stacks under investigation. Table: Technological processes that were analyzed.

Within the sets of samples under investigation, half of them were manufactured by depositing the 2nm thick HfO_2 layer by an ALD (Atomic Layer Deposition) process using H_2O and $HfCl_4$ as precursors at a temperature of 350°C and the other half by a MOALD (Metal-Organic ALD) process, using as precursor Tetrakis (EthylMethylAmino)Hafnium (TEMAHf) at a growth temperature of 300°C. The objective was to study whether the type of precursor used in the growth process can affect the quality of the resulting dielectric layer and, therefore, the electrical behavior and device reliability.

The impact of an annealing on the dielectric properties of the devices was also investigated. To do so, different thermal treatments were performed in the manufacturing process of the devices. Some wafers (blankets and those with MOS capacitors) were annealed at 1030°C after (ann-after) or before (ann-before) the gate electrode deposition. Others were not subjected to any annealing process, which will be considered as reference. The goal was to determine when the annealing must be performed within the fabrication process of the devices to optimize their performance.

For the CAFM analysis, the protective layer is wet-etched with a chemical bath to expose the bare high-k. The elimination of the protective layers of polysilicon and TiN was performed by selectively removing each single layer of the contact stack. The polysilicon layer can be removed very selectively using potassium hydroxide (KOH) while the TiN layer is removed by hydrogen peroxide (H_2O_2). An optimized process sequence consists of the following three steps [Aguilera 10]:

1. 10% HF during 10 seconds to eliminate the native SiO_2 on top of the polysilicon layer
2. 10% KOH for 20 min at ambient temperature to remove the layer of polysilicon.
3. H_2O_2 10% to 50°C for 30 minutes to remove the TiN layer.

Once the TiN/Poly gate was previously removed with a very selective etching (Fig. 3.15), nanoscale current maps were obtained with the CAFM (Pt/Ir coated Si tips). In order to improve the lateral resolution of the AFM [Lanza 10], topographical images were measured in vacuum environmental conditions ($3 \cdot 10^{-5}$ mbar) [Aguilera 08v] using Silicon tips (with a smaller radius and, therefore, a smaller contact area) [Vanessa 11b]. $1x1\mu m^2$ sized MOS structures with equal gate oxides and gate electrode were also characterized at device level with a Semiconductor Parameter Analyzer.

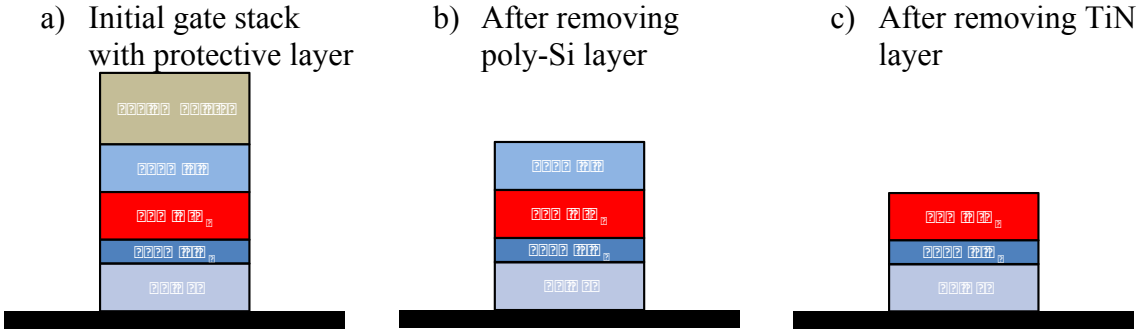


Figure 3.15. Process procedure of gate contact stripping [tesis lidia]. After 3 consecutive wet etching steps with HF, KOH and H_2O_2 (step a), b) and c), respectively) the bare gate dielectric is exposed.

3.2.2 Electrical conduction of gate stacks at device level

In this section, the electrical gate conduction of fully-processed MOS capacitors subjected to different annealing treatments and with HfO_2 layers grown with different precursors has been analyzed. To do so, I-V curves measured on different capacitors have been compared. Fig. 3.16a shows, as example, the mean of 17 I-V curves measured at device level on the different MOS structures. See the legend inside the figure to identify which symbol corresponds to any of the analyzed structures. If we compare the electrical conduction of non-annealed samples (black curves), at low fields MOALD structures show a larger conductivity than ALD capacitors. On the other hand, the breakdown voltage (V_{BD}) and the conductivity at high fields are similar. In [Blasco 05] it was observed with ECAFM [Blasco 04], that HfO_2/SiO_2 gate stacks show different conduction regimes depending on the applied bias. From the stack band diagram, low voltage regime could be associated to carrier injection through a triangular HfO_2 barrier (and the SiO_2 barrier) while conduction at high voltages would be associated to carrier injection at energies above the HfO_2 barrier [Blasco 05]. That is, at low voltages the conduction is controlled by the HfO_2 film and at high voltages by the SiO_2 layer. Therefore, the results shown in Fig. 3.16a suggests a worse quality of the high-k layer in MOALD samples (higher leakage currents at low fields), which is attributed to a larger density of defects when using organic precursors [Swerts 10]. Some other possible reasons as, for example, changes in the SiO_2 thickness, are discussed later. When an annealing is applied, the ALD sample annealed before the gate electrode deposition (ann-before, red circles in Fig. 3.16a) shows the typical post-breakdown (BD) behavior.

On the contrary, the annealing prior to the gate electrode deposition seems to have no remarkable effects on the conductivity of the MOALD sample (red diamonds in Fig. 3.16a). When the annealing is performed after the gate electrode deposition (blue symbols in Fig. 3.16a), the results are different. The ALD and MOALD samples annealed after the gate electrode deposition (ann-after) show the largest V_{BD} compared to those without annealing. As an example, Fig. 3.16b shows the Weibull plot obtained on MOALD samples that were non-annealed (squares) or annealed after (circles) the gate electrode deposition. Note that the gate voltage for 63% break down probability capacitors ($V_{BD,63\%}$) is larger after the annealing. Moreover, the samples annealed after

the gate electrode deposition (ann-after) also show the smallest conduction at high fields (Fig. 3.16a). This conductivity reduction, not registered for the ann-before samples, somehow involves an interaction between the HfO_2 and the TiN/Poly layers at high annealing temperatures, which has to be further analyzed in detail.

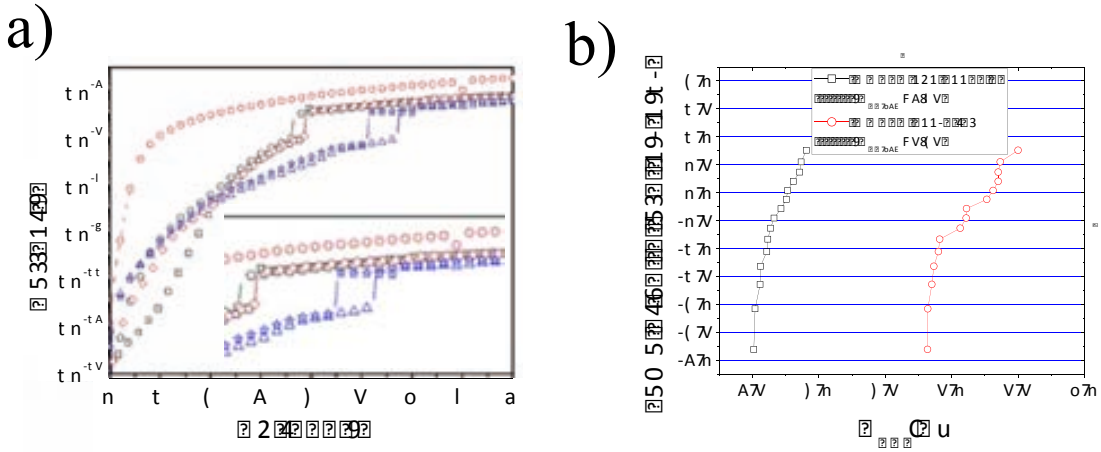


Figure 3.16. (a) Average device level I-V curves obtained in 1x1μm^2 MOS structures for all the analyzed samples. (b) Weibull plot of MOALD samples that were non-annealed or annealed after the gate electrode deposition.

3.2.3 Electrical conduction of gate stacks at the nanoscale

CAFM was also used to investigate the nanoscale properties of the different samples from the measurement of current and topography maps after the gate electrode removal. Note that the CAFM measured currents (Fig. 3.17) are in the range of few pA, which are very small. However, since these currents flow through extremely small areas, the minimum current density that can be registered with CAFM is quite high (~5pA through an area of ~100nm^2, that is, ~5A/cm^2). Therefore, the CAFM results can only be compared with those obtained at the device level for higher electrical fields, which corresponds to the high voltage regime in Fig. 3.16a.

Fig. 3.17 shows typical current maps obtained on ALD (a-c) and MOALD (d-f) non-annealed (a and d), annealed before (b and e) and annealed after (c and f) the gate deposition samples. Different regions were measured to avoid local inhomogeneities within the same sample. The current maps shown in Fig. 3.17 were obtained by applying the minimum voltage (V_G) needed to measure current above the noise level, so that, the larger the V_G, the smaller the electrical conduction. Note, first, that the conductivity of the non-annealed ALD (a) and MOALD (d) samples is similar (V_G is 3.4 and 3.3V, respectively). These results are compatible with those shown in Fig. 3.16a, where at high fields, both samples show a similar conductivity. When the impact of the annealing is investigated, the ALD ann-before sample (b) shows the largest conduction (smallest applied voltage). Finally, since the ann-after samples (c and f) were obtained by applying the largest V_G (4.2 and 5V, respectively), the results show that these structures have the smallest electrical conduction. Note that all these results are compatible with Fig. 3.16 (high field region), that is, the samples that show a smaller/larger conduction at device level are those with a smaller/larger average conductivity at the nanoscale. Therefore, these results demonstrate a clear link between the nanoscale and device level electrical properties of the MOS devices.

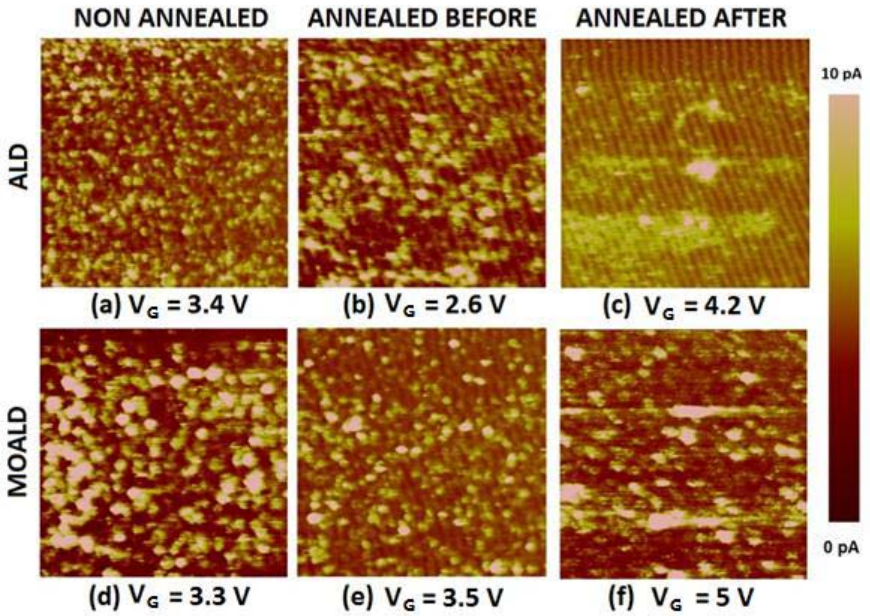
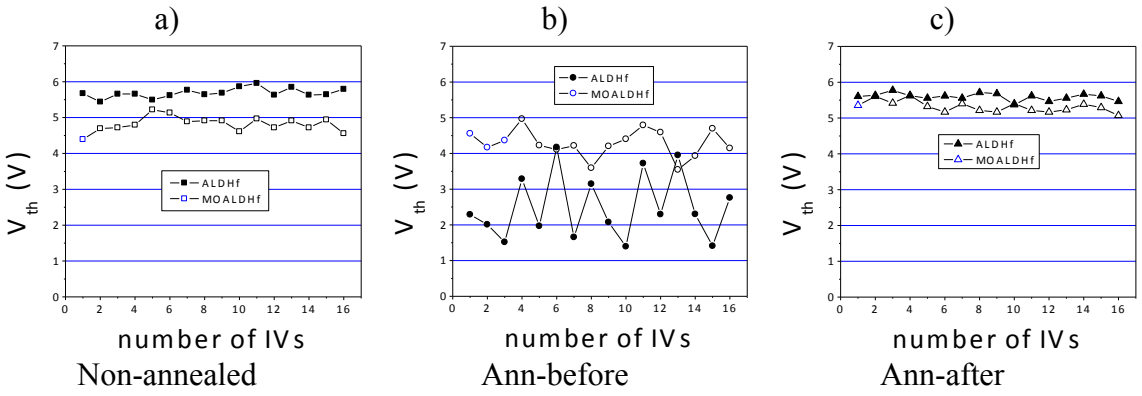


Figure 3.17. Current images (500 nm x 500 nm) obtained with CAFM on ALD (a-c) and MOALD (d-f) samples non-annealed (a, d), annealed before (b, e) and annealed after (c, f) the gate electrode deposition.

The nanoscale conduction homogeneity of the gate oxide stack was also studied. Since current images were obtained at different V_G, a direct comparison of the data is not meaningful, so that the homogeneity of the gate oxide conductivity was analyzed from the measurement with the CAFM tip of I-V characteristics at different positions on the stack (Fig. 3.18).



Analysis of the homogeneity from nanoscale IV curves						
Precursor	ALD			MOALD		
Annealing	non annealed	ann-before	ann-after	non annealed	ann-before	ann-after
Deviation V_{TH} (V)	0.13	0.90	0.10	0.21	0.39	0.15

Figure 3.18. Threshold voltage (V_{TH}) at a current level of 5pA for (a) non-annealed, (b) ann-before and (c) ann-after gate contact deposition. The table corresponds to an analysis of the conduction homogeneity of the samples obtained from nanoscale I-V curves. 16 positions were analyzed at each sample.

For each sample, 16 positions were analyzed in order to have representative data for statistical analysis. The gate oxide conduction was evaluated from the gate voltage at which a 5pA-current is measured (V_{TH}) on local I-V curves. Fig. 3.18 depicts the different V_{TH} for non-annealed (a), ann-before (b) and ann-after (c) samples. The dispersion of V_{TH} obtained on the different samples is shown in the table of Fig. 3.18. Note that the ann-before samples (Fig. 3.18b) show a larger dispersion of V_{TH} (especially in the case of the ALD precursor), i.e., their conduction is more inhomogeneous. However, no remarkable differences are observed between non-annealed and ann-after samples, independently of the precursor, although ann-after samples show a slightly larger homogeneity.

To investigate if there is a relation between the nanoscale electrical properties and the morphology of the HfO_2 layer, topographical images of the different samples were also measured. To increase the lateral resolution of the experiment, the topographical images were obtained with non-coated Si tips and in vacuum environmental conditions. Fig. 3.19 shows topographical images of the ALD (a-c) and MOALD (d-f) non-annealed (a and d), ann-before (b and e) and ann-after (c and f) samples. Note that the ann-before ALD sample (Fig. 3.19b) shows some voids, which were not measured in any other structure included in this study. Lysaght et al. [Lysaght 03] described an ALD process including chlorine based precursor and ex situ annealing with Nitrogen. In [Lysaght 03], the authors reported that annealing ambient contains sufficient oxygen to oxidize the exposed silicon substrate due to the formation of voids at annealing temperatures above 900°C. Actually, in [Lysaght 03], XPS measurements showed a Cl higher concentration at grain boundaries (formed from impurity precipitation during grain formation) at a sufficient level so this can contribute to void formation due to dry etching of the Si substrate. Note that when using a chlorine-free precursor (Fig. 3.19e) such voids are not observed. Therefore, such voids could be attributed to the use of chlorine in Fig. 3.19b. In our case, the formation of such voids can be the origin of the larger nanoscale electrical conduction and inhomogeneity observed in Fig. 3.17 and the unique properties observed at device level: the post-BD behavior registered in Fig. 3.16a.

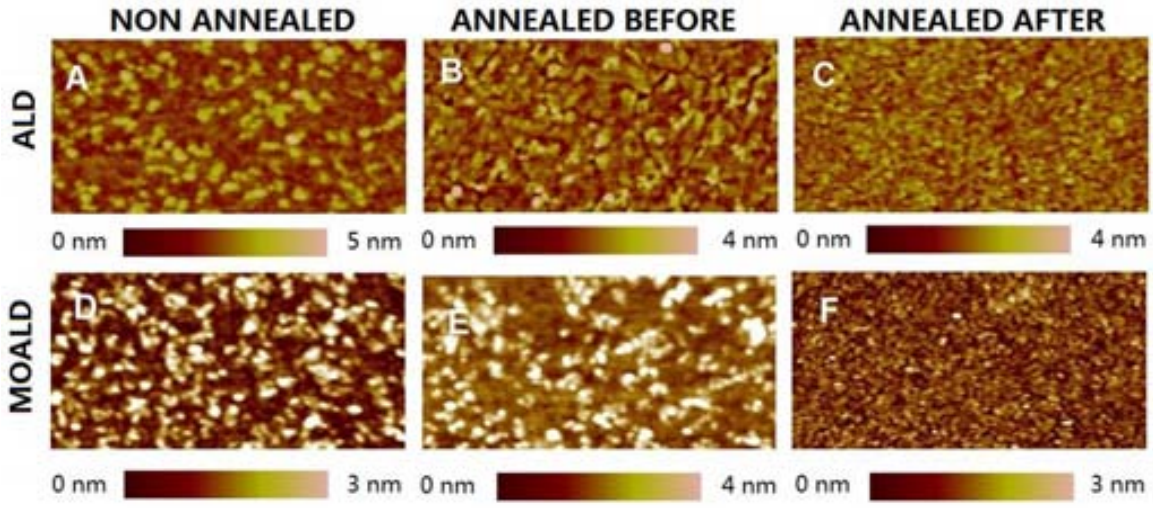


Figure 3.19. Topographical images (500 nm x 250 nm) obtained with AFM on ALD (a-c) and MOALD (d-f) samples, non-annealed (a, d), annealed before (b, e) and annealed after (c, f) the gate electrode deposition.

Fig. 3.19 also shows that the ann-after structures (c and f) are less rough than samples without annealing (a and d). In some works [Vanessa 10, Paskaleva 08, Yew 10] and in section 3.1 it was demonstrated that, after a high temperature annealing, some HfO_2 based stacks can polycrystallize, leading to a significant topographical surface rearrangement and a granular structure (not observed in amorphous layers) which can be attributed to randomly distributed nanocrystals within the high-k layer. However, there is not unanimity about the conditions at which ultra-thin HfO_2 stacks polycrystallize. While some authors [Cosnier 07] suggest that HfO_2 layers with a thickness smaller than 2.5nm remain amorphous for annealing temperatures even larger than 1030ºC, others indicate that they can actually polycrystallize [Lanza 11, Bohra 07]. In our case, for the samples analyzed in this study, the absence of such granular pattern (compared to non-annealed structures) could rule out the polycrystallization of the high-k dielectric [Bohra 07]. On the contrary, the observation of smoother surfaces after the annealing in ann-after samples (suggesting smaller oxide thickness fluctuations), could explain their smaller electrical conduction and their larger homogeneity and V_{BD} (Fig. 3.16 and 3.17).

However, other factors could also be responsible of this phenomenology, like changes in the thickness of the different layers or a reduction of the density of defects after the annealing process. For example, it is widely accepted that an annealing process can lead to a decrease (increase) of the HfO_2 (SiO_2) layer thickness, respectively [Bohra 07]. The increase of the SiO_2 thickness could be related to an oxidation of the Si-SiO_2 interface. On the other hand, the reduction of the thickness of the high-k layer can be interpreted as a "densification of the HfO_2" film, as demonstrated from TEM images on n-channel MOSFET devices with HfO_2 [Kim 01]. The modification of the thickness of the different layers during the annealing can modify the electric field distribution on them and, therefore, the gate oxide conductivity. In our case, since larger breakdown voltages are observed in the ann-after samples and the breakdown event is related to the failure of the SiO_2 layer [Pétry 04], the shift of V_{BD} has been attributed to the growth of the SiO_2 interfacial oxide layer [Swerts 10, Lysaght 03]. This effect could also explain the gate oxide conductivity reduction at high electric fields. However, further experiments with complementary techniques should be performed to clarify this point.

To conclude, in this section (**PUBLICATION 4**) HfO_2 gate stacks grown by ALD and MOALD have been characterized. The goal was to compare the electrical properties of HfO_2 layers grown using different precursors. The effect of an annealing before or after the gate electrode deposition has also been analyzed to investigate their thermal stability. This analysis has been performed at device level using standard characterization techniques and at the nanoscale with CAFM to obtain complementary information. At device level, non-annealed MOALD samples show larger low field leakage currents, which suggests that the high-k layer is richer in defects when it is grown with organic precursors. At high fields, the electrical conduction and V_{BD} in ALD and MOALD samples are similar. When the annealing is done before the gate electrode deposition, typical post-BD electrical behavior is observed in ALD structures. The CAFM characterization shows that in ann-before samples, the nanoscale properties are more inhomogeneous independently of the precursor.

In particular, voids are measured on the topography of the ALD structures, which could be the origin of the post-BD behavior observed at device level and the larger inhomogeneity measured at the nanoscale. When the annealing is performed after the

gate electrode deposition, smoother surfaces are observed, which could explain, among other factors, the reduction of leakage current and the increase of V_{BD} observed in those samples (ALD and MOALD). Therefore, the annealing seems to have beneficial effects only when it is carried out after the gate electrode deposition.

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Chapter 4: A nanoscale analysis of Negative Bias Temperature Instability (NBTI) and Channel Hot Carrier (CHC) degradation in MOSFETs

In chapter 3, the influence of different fabrication parameters, such as the growth precursor, the gate oxide thickness and the post-deposition thermal annealing temperature, on the nanoscale and device level properties of MOS devices have been investigated. This chapter will be devoted to the analyses of how electrical stress, which can trigger different aging mechanisms, affects the electrical properties of MOSFETs. Because of the differences of electric field distributions in the device during BTI and CHC stresses (see chapter 1), the oxide damage is expected to be uniformly distributed over the gate oxide area for BTI aging, whereas it should be mostly located close to the drain for CHC degradation. The CHC non-uniform aging has been experimentally verified from the differences in the values of the drain currents measured when the roles of source and drain are exchanged in the device during the test [Amat 09]. However, details on the spatial distribution of damage after an electrical stress can only be revealed using other high resolution characterization techniques. In this sense, Conductive Atomic Force Microscopy (CAFM) can be very helpful because it has been demonstrated to be a very effective technique in providing valuable information on the electrical properties [Porti 01, Iglesias 10, Yanev 08] and failure mechanisms (as TDDB) [Fiorenza 06, Porti 02, Wu 12] of the gate dielectric of MOS devices at the nanoscale. Some studies on the gate oxide aging under electrical stress have been already performed, but most of them use the AFM tip as the gate electrode for stress and aging monitoring [Fiorenza 06, Porti 02]. Nonetheless, due to experimental limitations, few works have combined device level stresses and nanoscale characterization to analyze the impact of such stresses on the nanoscale gate oxide properties ([Lanza 09] and chapter 3). The combination of both analyses is especially difficult because, once the device is stressed and its electrical properties analyzed, the structure under investigation must be deprocessed to expose the gate oxide to the CAFM tip, and many experimental difficulties appear. In this sense, structures that allow both kinds of studies should be used which, for example, allow an easy gate electrode removal and have the proper dimensions for the scanning of the whole gate area of the device. Such experimental difficulties are especially remarkable for the case of MOSFETs, so that the few studies performed in this direction have been focussed on MOS capacitors and, therefore, the studies are restricted to stresses that are uniform over the gate active area [Lanza 09] as the BTI. In this chapter (**PUBLICATION 5**), the nanoscale electrical properties of the gate oxide of MOSFETs after homogeneous (BTI) and non-homogeneous (CHC) device level stresses have been studied with CAFM. Since with the CAFM tip very small areas can be analyzed, the measurement of the bare oxide electrical properties has allowed evaluating the degradation induced at different regions of the gate oxide along the channel.

4.1 Experimental and device level measurements

pMOSFETs (L=1μm and W=0.5μm) with a 1.4nm thick SiON layer as gate dielectric have been analyzed. The gate electrode consisted of a 60nm thick layer of polysilicon and a 40nm thick layer of NiSi. Some devices were subjected to NBTI stress by applying –2.6V at the gate and others were subjected to CHC stress by applying -2.6V at the drain and gate while the other terminals were grounded. In both cases, the stress time was 200sec. Other transistors were not stressed, which have been considered as reference. In the case of CHC stress, this voltage configuration (V_G=V_D) is the most damaging stress condition for pMOSFETs [Sheu 08, Amat 10], independently of the channel length, because it provokes a larger hole injection into the oxide [Amat 10]. A current compliance of 1mA was applied during the stress. Fig. 4.1 shows typical I_D-V_D (a), I_D-V_G (b) and I_G-V_G (c) characteristics obtained before (continuous line) and after a NBTI (open symbols) and CHC (solid symbols) stress on a MOSFET. The post-stressed characterization revealed a threshold voltage shift of 25/125mV, a decrease of 4/19% in the drain current at V_D=-1.2V and an increase of 4/227% in the gate current at V_G=-1V for NBTI and CHC stressed devices. The breakdown voltage was also estimated from the measurement of the I_G-V_G characteristics obtained after applying ramped voltage stresses until BD to the gate of some MOSFETs (Fig. 4.1c). V_{BD}(63%), that is, the voltage for a 63% probability of BD occurrence, was estimated to be 3.8V (Fig. 4.1d).

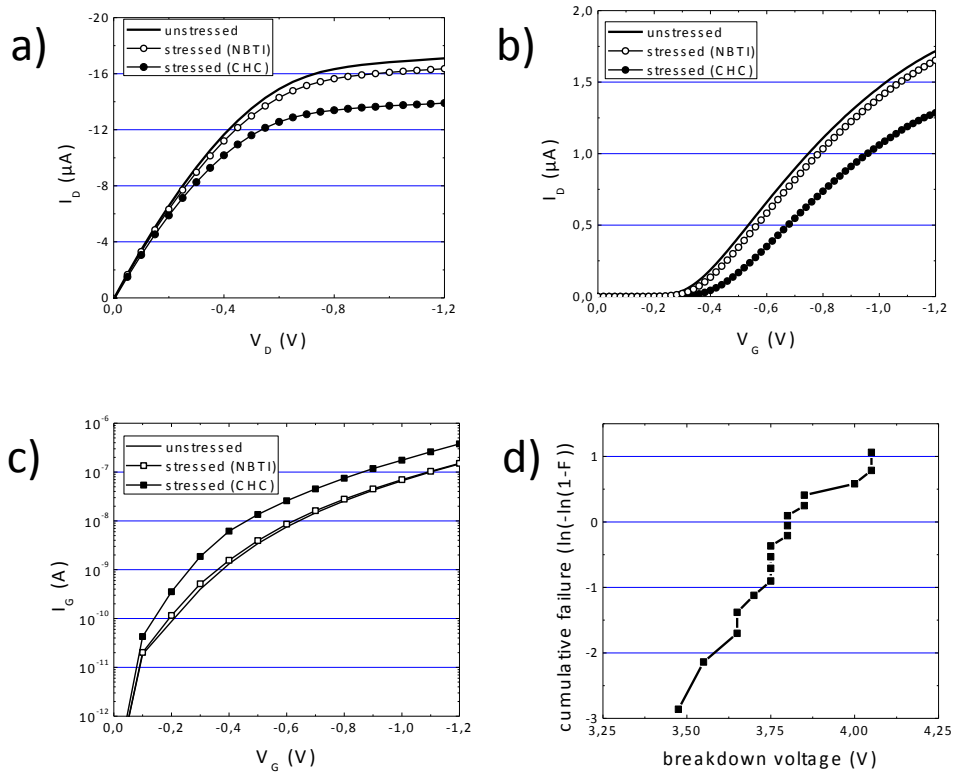


Fig. 4.1. Typical I_D-V_D (a) I_D-V_G (b) and I_G-V_G (c) characteristics of a MOSFET recorded before (continuous line) and after NBTI (open symbols) and CHC (full symbols) stress. (d) corresponds to a breakdown statistics from which V_{BD}(63%) was estimated.

Once the device level stress (NBTI or CHC) was applied and the device aging characterized, the polysilicon and NiSi layers on top of the gate dielectric were removed

with a very selective wet etch to expose the gate dielectric and make it accessible to nanoscale electrical measurements with the CAFM tip (Fig. 4.2). The etching consisted of a solution of phosphoric acid, 85%, at a temperature of 125ºC, during 90 sec. Fig. 4.2 d-f show some examples of topographical maps obtained after an etching of 30, 60 and 90s, respectively. Note that only after the 90s etch, the gate area is smooth enough to consider that no rests of the gate electrode is present on the surface.

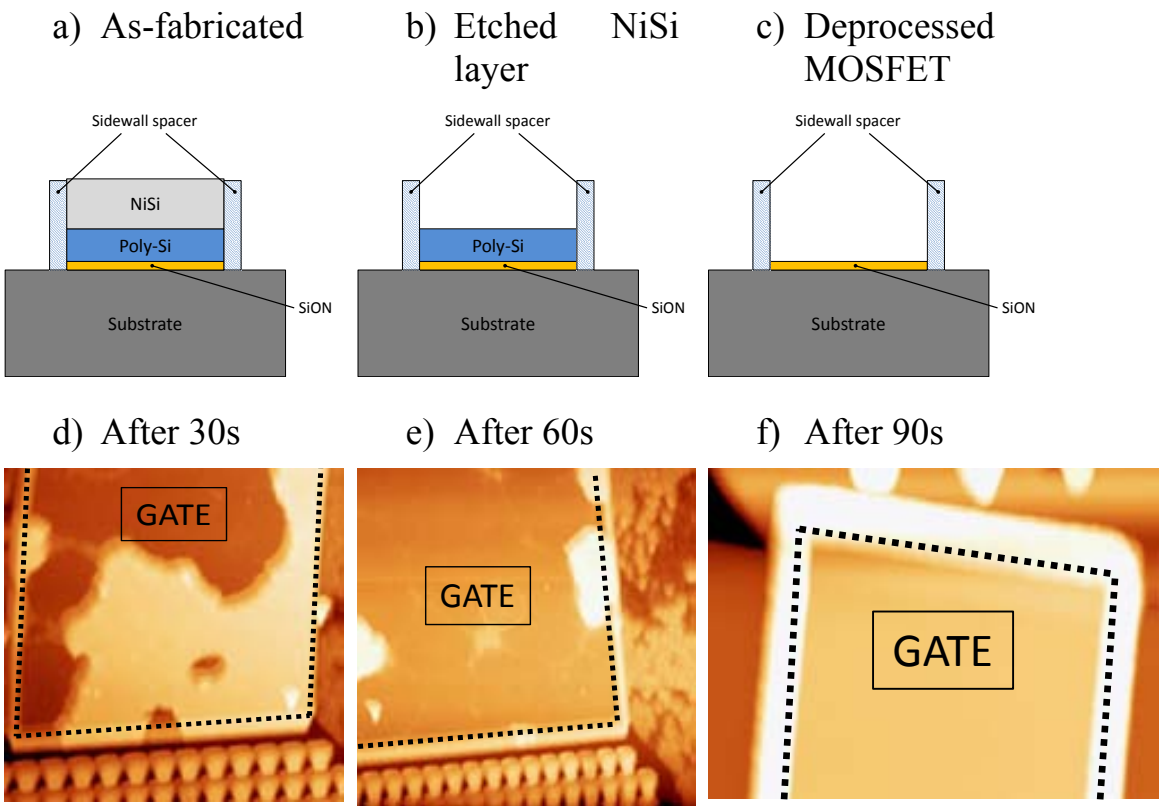


Figure 4.2. Schematic of (a) an as-fabricated and (b) partially etched and (c) a completely deprocessed MOSFET. Topographic maps of a MOSFET after (d) 30s, (e) 60s and (f) 90s in the etching solution.

After the etching, the gate oxide was scanned with the AFM tip to investigate its morphology. Fig. 4.3 shows a 3D typical topography map obtained on a MOSFET. Note that the gate region can be easily distinguished and measured between the two spacers. However, the presence of such sidewall spacers does not allow to measure at the extreme positions of the channel (<0.1µm or >0.9µm) because they impede the CAFM tip (which has a conical shape) contacting the gate area (Fig. 4.3). The roughness of the exposed dielectric was determined to be below 0.2nm, which is comparable to other results in literature [Polspoel 08]. This value demonstrates that the gate oxide is not affected by the removal of the top electrode.

The nanoscale electrical properties of the dielectric were studied by scanning the bare gate area with the CAFM tip (Fig. 4.3). As an example, in Fig. 4.4a and b, the topography and current map of a non-stressed SiON area was recorded by a applying a positive voltage with respect to the sample. Local IV characteristics show that oxide breakdown happens at ~4V. PtIr coated Si tips with a nominal tip radius of 20nm were

used. To avoid anodic oxidation [Murrell 93, O'Shea 95], we positively polarized the tip (substrate injection of negative charge carriers) and carried out the CAFM measurements in a dry nitrogen ambient, keeping the humidity level inside the AFM chamber below 0.5%. Due to the saturation of the electronics of the setup, maximum currents of 100nA can be measured. An important point that must be emphasized when performing conductivity measurements with CAFM is that the currents measured with this technique are very sensitive to experimental factors as the contact area between the tip and the sample and the resistivity of the tip, which can change from tip to tip and even during the measurements due to the tip wear out. Therefore, the comparison of absolute values of the current measured in different experiments could not be really meaningful. Only relative variations in the same experiment are really reliable. Therefore, in this section, we will center our attention on conductivity variations along the channel in the same sample.

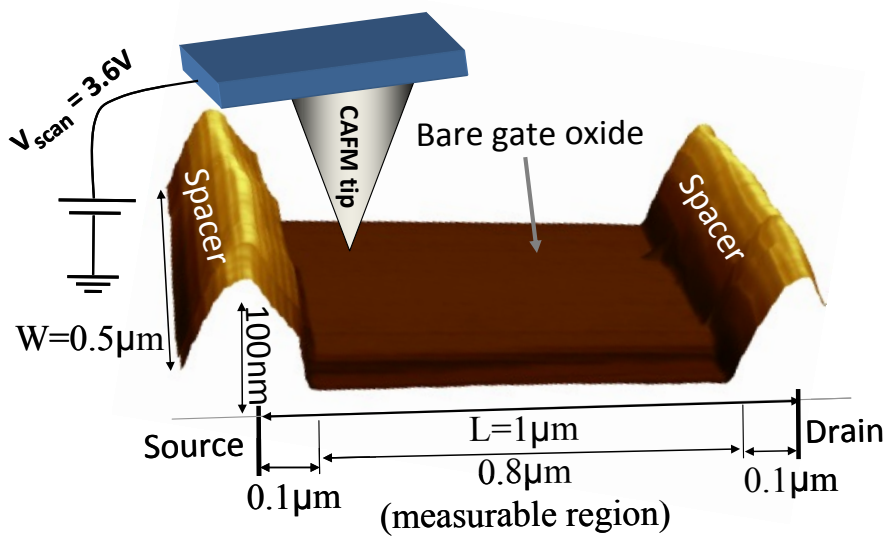


Fig. 4.3. AFM 3D topographic image of a pMOSFET after removal of the gate electrode, showing a very flat surface (RMS<0.2nm) between the two spacers. Placing the CAFM tip on the gate oxide region, the conduction through the oxide can be studied with nanometer lateral resolution. The dimensions of the area under study and structure polarization are indicated.

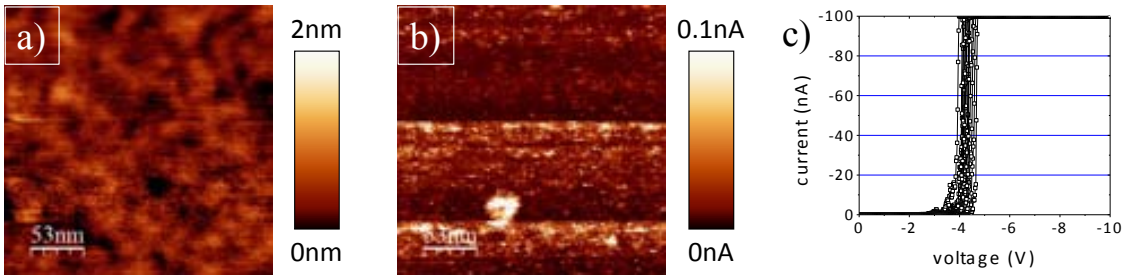
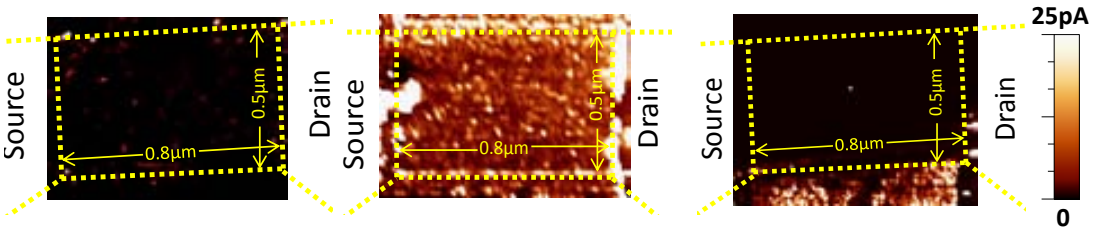


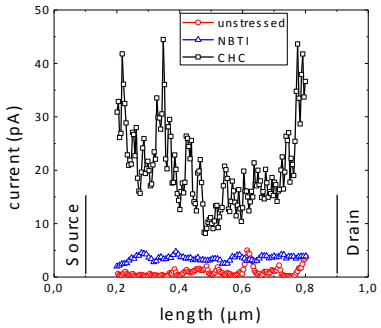
Figure 4.4. (a) topograhic and (b) current map of the bare SiON gate dielectric layer. (c) local IV curves measured at different positions.

4.2 Nanoscale characterization of BTI and CHC stressed MOSFETs

The gate oxide electrical properties before and after the electrical stress have been studied at the nanoscale with the CAFM. Fig. 4.5a - c show, respectively, current maps (on the same current scale) obtained on (a) a reference (non-stressed), (b) NBTI and (c) CHC stressed MOSFET, where the measurable gate area has been delimited by a dotted line. In all cases, current images were obtained at 3.6V. While in the non-stressed samples, (Fig. 4.5a), only noise level is basically measured, NBTI and CHC stressed MOSFET show brighter areas, representing larger currents, which correspond to leaky sites in the dielectric.



d)



e)

	Source		Centre		Drain	
	$\langle I \rangle$ [pA]	σ_I [pA]	$\langle I \rangle$ [pA]	σ_I [pA]	$\langle I \rangle$ [pA]	σ_I [pA]
reference	0.4	0.1	1.1	0.2	1.1	0.9
NBTI	3.3	0.7	3.1	0.1	3.2	0.1
CHC	24.9	38.9	13.6	18.4	25.4	75.6

Fig 4.5. Current images obtained at a gate voltage of 3.6V in non-stressed (a) and NBTI (b) and CHC (c) stressed MOSFETs. (d) Average current measured with the CAFM tip along the channel for the non-stressed (circles), NBTI (triangles) and CHC (squares) stressed MOSFETs. (e) Table indicating the average and dispersion of the current measured in a channel length of 100nm close to the source, drain and at the center of the channel. (b) to (e) clearly show the effect of the degradation induced by the previous NBTI and CHC stress, with larger currents (brighter areas), which are not homogeneously distributed after CHC stress.

The comparison of the images in Fig. 4.5a (non-stressed sample) with the images in Fig. 4.5b (NBTI stressed sample) and Fig. 4.5c (CHC stressed sample) allows to conclude that (i) the number of leaky sites on the stressed MOSFETs is considerably larger and (ii), the distribution of leaky sites over the gate region can change after the stress. These observations are quantitatively evaluated in Fig. 4.5d and e. Fig. 4.5d shows the average of 25 current profiles obtained with the CAFM tip at different positions along the channel for the non-stressed (circles) and NBTI (triangles) and CHC (squares) stressed MOSFETs. In the non-stressed sample, current is close to the noise level of the CAFM and homogeneously distributed along the channel. The stressed MOSFETs (triangles and squares) show larger currents. However, a difference between NBTI and CHC

stressed MOSFET can be detected: while the first one shows also an homogeneous distribution of the current along the channel, in CHC stressed MOSFET, gate current is especially larger in the regions close to the diffusions. The table in Fig. 4.5e, which shows the rms value, σ_I, and average current, <I>, measured from Fig. 4.5d in a channel length of 100nm close to the source, drain and at the center of the channel of the three MOSFETs, further supports this data. Note that, in the CHC stressed MOSFET, the current close to the source and drain is larger than in the center of the channel, and also shows a higher dispersion. However, in non-stressed and NBTI stressed MOSFETs current distribution is more homogeneous, although larger currents and dispersions were measured after the NBTI stress.

The spatial distribution of the leaky sites has been analyzed in more detail from the current images. Randomly located leaky spots are measured on the fresh oxide, which can be assigned to currents through native defects and/or local thinning of the dielectric. On the previously stressed dielectrics, however, the number of leaky sites is larger and drive more current. In this case, the leaky spots can be considered to be related to the defects generated during the stress. Moreover, since the current through the leaky spots does not reach the CAFM maximum current (100nA) and device level measurements didn't show a post-BD behaviour in the gate current, they cannot be BD spots. Consequently, the current measured with the CAFM through the stressed oxides can be assumed to be indicative of the degradation induced during the NBTI or CHC stress. So, the current images in Fig. 4.5b and c lead to conclude that degradation measured in the gate is specially concentrated close to source and drain in the CHC stressed MOSFET. To analyse in more detail the distributions of generated defects along the channel, the cumulative distribution of currents measured in 0.05µm^2 regions centered at channel distances L=0.15µm and L=0.85µm (i.e., close to source and drain respectively), and L=0.5µm (in the center of the channel) are represented in Fig. 4.6a for NBTI and Fig 4.6b for CHC stressed MOSFETs. Note that in the case of the NBTI stressed devices (Fig. 4.6a), similar cumulative distributions are found in the three regions. On the other hand, after the CHC stress (Fig. 4.6b), lower currents are measured in the centre whereas larger currents are observed in the distributions measured close to the diffusions. The current distributions at the extremes of the channel do not show remarkable differences, which indicates that a similar degradation effect is produced close to the diffusions.

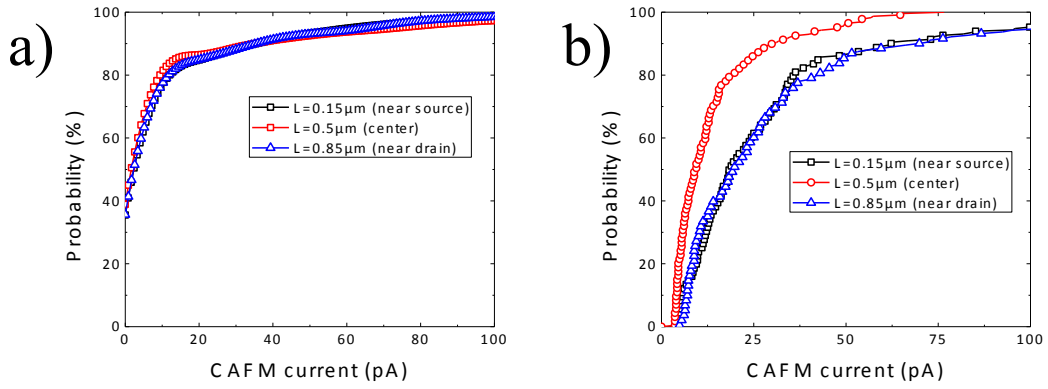


Figure 4.6. Cumulative distributions of the current measured with the CAFM in 0.05µm^2 regions centered close to the source (L=0.15µm) and drain (L=0.85µm) and in the centre of the channel (L=0.5µm) for (a) NBTI and (b) CHC stressed MOSFETs.

The number of leaky sites on reference and stressed samples has been also analysed, as determined from 20 current profiles along the channel width extracted from the current maps of Fig. 4.5. Fig. 4.7a shows the average number of leaky sites that drive currents larger than 10pA versus their position along the channel. Squares and circles correspond, respectively, to NBTI and CHC stressed MOSFETs, while triangles show the data on the non-stressed transistor. Clearly, the number of leaky sites is larger in both stressed MOSFETs. Moreover, in the CHC stressed MOSFET, leaky sites are mostly located close to the diffusions whereas on the NBTI stressed and fresh oxides the spots are uniformly distributed along the channel.

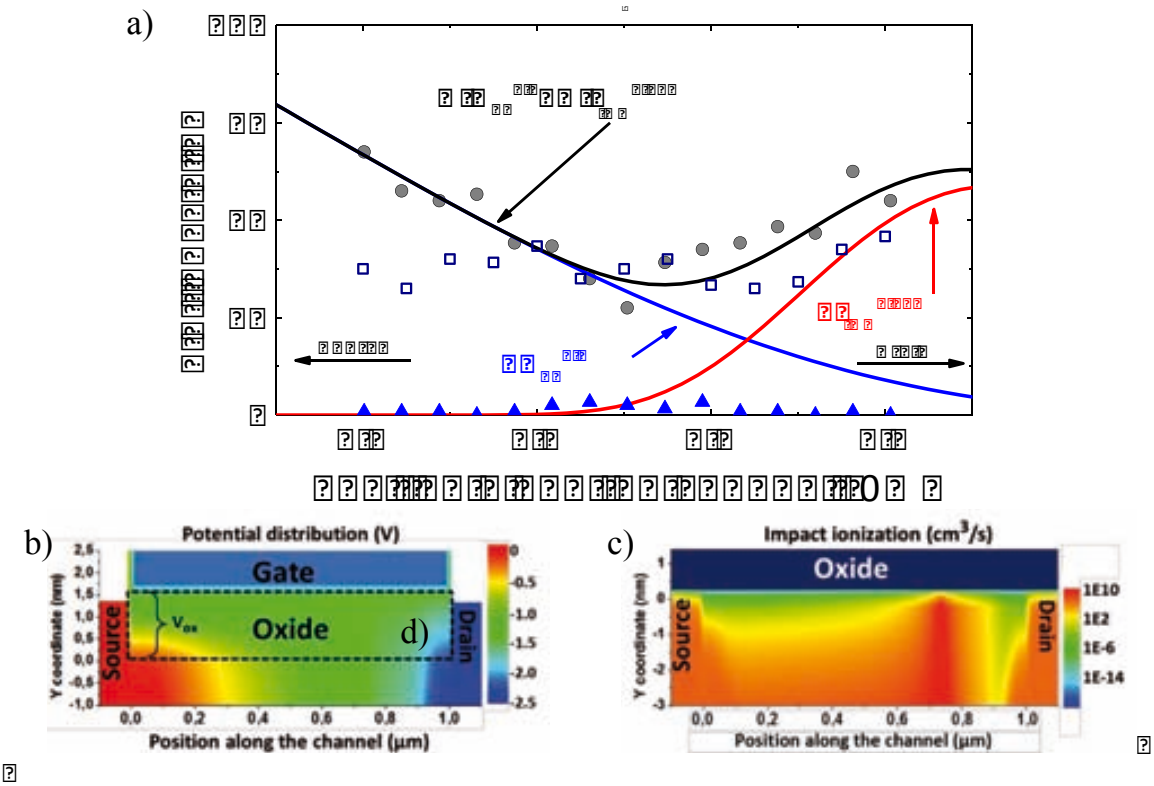


Figure 4.7. (a) Average number of leaky sites (CAFM current >10pA) obtained at different positions along the channel in a fresh (triangles), NBTI (squares) and CHC (circles) stressed device, obtained from 20 profiles registered along the channel width in the current images in Fig. 4.5. Lines correspond to the fitting of the number of leaky sites to $A \bullet E_{ox}\gamma$ (blue) and $B \bullet I_{ion}\alpha$ (red) and their sum (black). TCAD simulation of the potential distribution (b) and impact ionization (c) for a pMOSFET at the stress conditions, used to obtain the E_{OX} and I_{ION} profiles along the channel.

Simulation

TCAD simulations of a pMOSFET under CHC stress biasing have been performed in order to explain the experimental distribution of leaky sites observed with CAFM (circles in Fig. 4.7a). In particular, the potential distribution (Fig. 4.7b) and the impact ionization (Fig. 4.7c) at the CHC stress conditions have been obtained. The dashed rectangle in Fig. 4.7b indicates the region that corresponds to the gate oxide. Clearly the potential distribution in the oxide is not homogeneous along the channel direction. The

voltage drop at the gate oxide (V_{ox}) is especially large close to the source because of the different biasing applied to the gate and source terminals (-2.6V and 0V respectively). On the contrary, V_{ox} is small close to the drain because the same voltage is applied at gate and drain terminals during the CHC stress. Consequently, the vertical electric field, which leads to the NBTI degradation, is more intensive close to the source and decreases along the channel direction from source to drain [Amat II 09]. The impact ionization (Fig 4.7c) reaches the maximum in a position close to the drain, where the carriers are more energetic, being this point the more susceptible for the hot carrier degradation. Then, the TCAD simulation allows investigating the two degradation sources during the CHC stress: the high vertical electric field and the impact ionization. Therefore, the leaky sites of Fig 4.7a located near the drain should be related to the traps created by impact ionization (I_{ION}) caused by hot-carriers [Amat 10]. On the other hand, those leaky sites located close to the source should have been created by the high electric field applied to the oxide (E_{OX}) during the CHC stress, which can induce NBTI damage [Sheu 08]. In the last case, due to the long time elapsed between the CHC stress and the CAFM characterization (some days), the measured degradation is related only to the permanent (or slow component) of BTI. Consequently, the damage produced in the oxide seems to be caused by the combination of E_{OX} and I_{ION} effects. Moreover, as shown in Fig. 4.6b, both aging mechanisms cause a similar effect, at least from the CAFM currents point of view. Both observations suggest that their contribution to the number of leaky sites could be additive. This hypothesis can be confirmed by fitting the leaky sites profile in Fig. 4.7a. The experimental profile can be well reproduced assuming the contribution of both mechanisms, blue/red lines show the fitting of the data to a potential law on E_{OX}/I_{ION}, that is, to $\sim E^{\gamma}_{OX}$ and to $\sim I^{\alpha}_{ION}$. For the fittings, the values of E_{OX} and I_{ION} in Fig. 4.7b and 4.7c have been considered. From these fittings (Fig. 4.7a), exponents of γ= 3.10 and α=0.113 have been obtained. The γ value is consistent with exponents given in the literature for the permanent component of BTI that ranges between 3-5 [Grasser 10]. The black line shows that the number of leaky sites can be fitted by the sum of the two exponential laws. Then, the leaky sites profile in Fig. 4.7a can be explained by the combination of permanent damage caused by NBTI in the region close to source and hot-carrier injection close to the drain, and confirms the degradation scheme proposed from conventional characterization techniques [Amat 09, Amat 10], where the CHC degradation is divided in two different stress components: i) a CHC aging component located at the drain side (pinch-off region) and ii) a BTI-component distributed between the source and the pinch-off region [Amat 09, Amat 10]. The CAFM results show, additionally, that, at the nanoscale, from a gate oxide current point of view, the generated defects are not significantly different, though created by different aging mechanisms. If this interpretation is true, the damage induced close to the source in the CHC stressed MOSFET should be equivalent to that induced in the NBTI stressed MOSFET. However, the current differences measured in both cases (Fig. 4.5e) could be explained taking into account the experimental considerations described in section 4.1.

In conclusion, a Conductive Atomic Force Microscope (CAFM) has been used to investigate at the nanoscale the impact of a Negative Bias Temperature Instability (NBTI) and a channel hot-carrier (CHC) stress on the gate electrical properties of MOSFETs. The high lateral resolution of the microscope has allowed investigating the differences of the degradation induced along the channel, by assuming that the defects generated by the stress assist tunnelling through the gate when the tip-sample system is

biased. After the stress, a larger number of leaky sites and larger currents (suggesting a larger degradation) are measured. However, while after the NBTI stress, the degradation of the gate oxide area is homogeneous, in the CHC stressed MOSFET, regions close to the source and drain show a larger degradation than the centre of the channel, which is indicative of the non-uniformity of the CHC stress. TCAD simulations of the magnitudes involved in the CHC stress (oxide voltage drop and impact ionization) suggest that the generated defects close to source and drain can be attributed to NBTI and to CHC degradation, respectively. However, although the aging mechanisms are different, from the gate oxide conductivity point of view, the created defects are not significantly different.

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Chapter 5: Graphene-Coated Atomic Force Microscope Tips for Conductive Measurements at the nanoscale

Topographical and electrical characterization of surfaces at the nanoscale is an essential procedure for analyzing the performance of many materials used in both industry and academia. In this field, scanning probe microscopy and, especially, atomic force microscopy, AFM, related techniques have demonstrated to be very powerful tools for surface metrology, being able to measure surface features whose dimensions are in the nanometer range (or even less) and the electrical properties of the material under analysis. Its capability of imaging conductive and non-conductive samples in ambient air condition with a lateral resolution of just a few nm and a vertical resolution better than 1nm has led the AFM to become a very useful tool in so diverse fields as Health Sciences [Mou 95, Chena 06], Materials Sciences [Magonova 06], Chemistry [Lee 07], Biotechnology [Müller 08] or Microelectronics [Celano 13]. However, the main challenge associated with this technique is the poor reliability of the conductive tips when, for example, conductivity measurements are needed to be performed with a CAFM.

In chapter 2, it was introduced that CAFM tips are one of the most important elements to obtain reliable results when performing topographical and conductivity measurements at the nanoscale with this technique. CAFM tips should be very sharp in order to have a very high resolution and the coating material should be very conductive and resistant from a mechanical point of view to avoid a premature wear out during the surface scan. On the other hand, in chapter 1, graphene was also introduced. It was presented as a material with excellent electrical and mechanical properties which is nowadays being widely studied for applications in many fields such nanoelectronics.

In the beginning, the only known method to obtain graphene was from mechanical exfoliation (repeated peeling) of small mesas of highly oriented pyrolytic graphite. However, recently, a new method to produce graphene by chemical vapor deposition (CVD) was proposed in [Reina 08]. This new method was revolutionary since graphene can not only be grown on different but is also transferrable to arbitrary substrates using a very ingenious process [Li 09]. This method not only permits the study of the interaction between graphene and other materials [Park 11] (see chapter 6), but also extends the use of graphene to other applications [Chen 11, Rafiee 12]. In this chapter, it is explained how the intrinsic properties of a commercially available CAFM tip can be modified if it is coated with a sheet of CVD-grown graphene using the transfer method proposed in [Li 09]. For the first time, a novel graphene coated CAFM tip is used for electrical characterization of nanostructured materials (**PUBLICATION 3**). The only similar device reported to date was recently presented by Wen et al. [Wen 12]. In this work, a graphene coated tip was used as an electrode in molecular junctions. Moreover, graphene was directly grown by CVD on Au-varnished AFM tips. W. Shim et al., [Shim 12] described experiments depositing graphene onto an array of scanning probes. Nevertheless, in their experiments they used commercially available silicon tips in order to investigate mechanical properties of graphene-multi-layer. In this chapter,

graphene single layer (GSL) sheets grown on copper foils by CVD [Zhang 11] were directly transferred onto different Pt-Ir varnished CAFM tips. This prototype has been used to perform nanoscale electrical characterization of both conductive and thin insulating materials (**PUBLICATION 3**).

5.1 Fabrication of a graphene-coated tip

The tips on which GSL was deposited were standard and commercially available AFM tips from Nanosensors (model PPP-CONTPt). These tips are made of silicon and are coated with a 20 nm thick layer of Pt-Ir, which is a 95% Platinum and 5% Iridium alloy (the Iridium is used to enhance the stability of the Platinum layer). Their characteristics are (Fig. 5.1): (i) Cantilever thickness T = 2µm, (ii) Cantilever width W= 50µm, (iii) Cantilever length L= 450µm, (iv) spring constant K= 0.2 N/m, (v) resonance frequency f_0=13 kHz, and (vi) nominal tip radius r_{tip}= 10 nm.

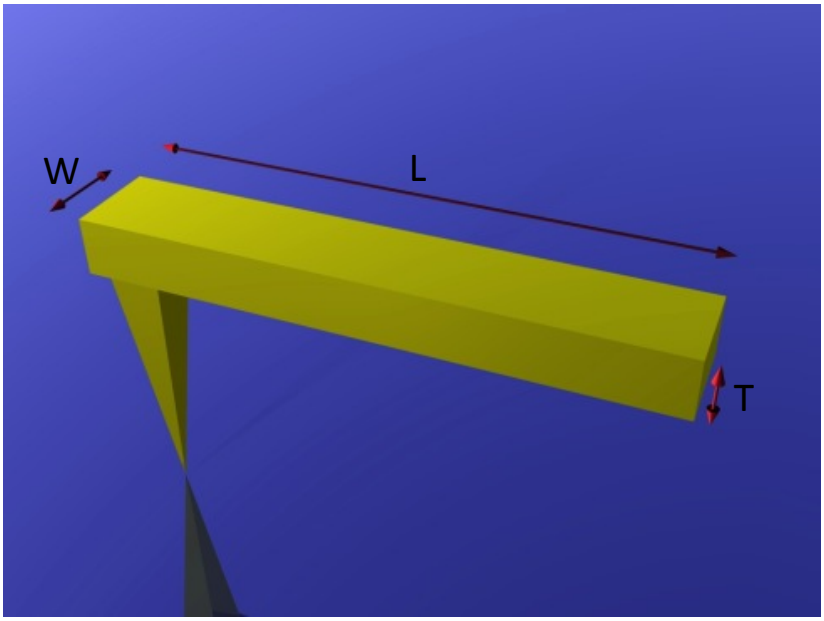

Figure 5.1. Schematic of an AFM cantilever indicating its physical dimensions.

The process to cover the Pt-Ir coated tip with GSL consisted of three steps: first, the immobilization of the tip to avoid that it breaks during the process, second the transfer of the GSL on it, and finally the delivery of the final product. The immobilization of the tip is performed on a piece of silicon wafer with Poly-methyl Methacrylate (PMMA) below and on it. PMMA is a polymer normally used in lithographic processes. PMMA powder was acquired from Sigma-Aldrich with a molecular weight of 996 000 determined by gel permeation chromatography (GPC), which was dissolved in ethyl lactate (concentration 4 wt %). The silicon substrate was spin-coated at a rotation speed of 1000rpm during one minute to leave a ~200nm thick layer of PMMA (Fig. 5.2d). Before the PMMA dries, we attach the AFM tip and the whole structure is heated for 10 minutes at 130°C on a hot plate to immobilize it (Fig. 5.2 e and i). Then, the AFM tip/PMMA/silicon was again spin-coated with ~200nm PMMA using the spinner and

the hot plate. The solid PMMA/AFM tip/PMMA/silicon stack (Fig. 5.2f) was used as target substrate on which the graphene sheet was transferred. It is worth noting that when the PMMA covers the tip, the cantilever, which is sensitive to extremely small forces (~nN), can flex (Fig. 5.2f) due to the weight of the PMMA.

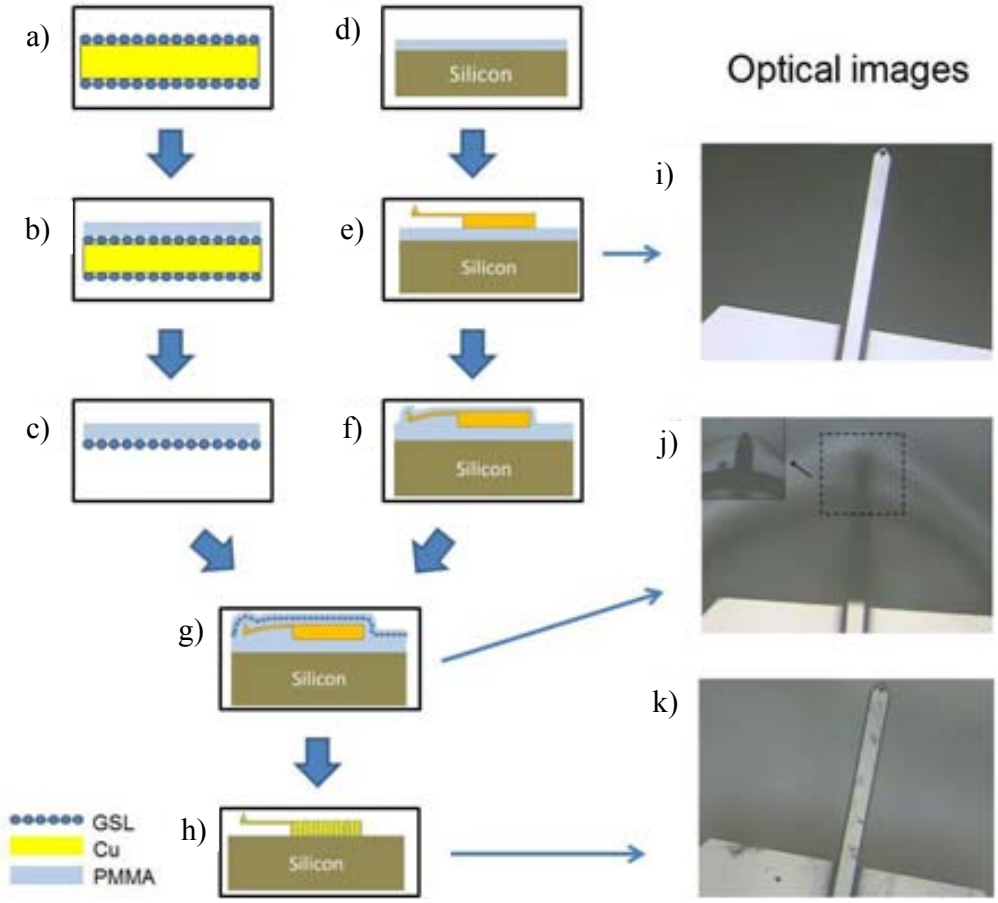

Figure 5.2: Schematic of the tip fabrication: (a) As-grown GSL on both sides of a Cu foil; (b) One side of the sample is covered with spin coated PMMA; (c) The bottom GSL and the Cu foil are etched; (d) A piece of Silicon is covered with spin coated PMMA; (e) The tip is attached on the sample and heated to fix the structure; (f) The AFM tip / PMMA / Si structure is again spin coated with PMMA; (g) the Graphene/PMMA stack in (c) is transferred on the tip; (h) the PMMA is removed using Acetone and maintaining the tip completely horizontal.(i), (j) and (k) are the optical images of the structure after steps (e), (g) and (h) respectively.

Graphene was commercially purchased at Alfa Aesar, which was grown by CVD on a 25µm thick copper foil. During the CVD process, GLS were grown on both sides of the copper substrate (Fig. 5.2a). The graphene growth process is as follows: i) load the cut Cu foil into the 25 mm inner tube of the CVD apparatus, flush the chamber with 400 sccm (Standard Cubic Centimeters per Minute) Ar and 50 sccm H_2 for 5min, close the gas flows and then pump the chamber down to 1 mTorr; ii) introduce 10 sccm H_2 into the system, heat the chamber to the growth temperature (1000°C) and anneal the Cu foil for 30 min at this temperature to enlarge the Cu grains and remove residual copper oxide and impurities; iii) introduce 20 sccm of methane gas into the chamber, perform

the synthesis for 15 min and then close the methane flow; iv) cool the sample down to room temperature with protection of 10 sccm H_2 flow. Fig. 5.3a shows a Raman analysis of the as-grown graphene/Cu samples used in this work, demonstrating that it corresponds to a GSL whereas Fig. 5.3b corresponds to a STM image of the graphene sheet. Note that the typical three-for-six lattice distortion of graphene single layers is observed, further supporting this hypothesis.

The transfer process of the graphene on the solid PMMA/AFM tip/PMMA/Silicon block consisted of the following steps: i) covering one of the sides of the GSL/Cu stack with ~ 200 nm PMMA media using the spinner (Fig. 5.2b); ii) etching the Copper using 1g/mol $FeCl_3$ during 5 minutes (Fig. 5.2c); iii) washing the PMMA/GSL (Fig. 5.2c) in HCl; iv) washing the PMMA/GSL in pure water; and v) picking up the PMMA/GSL stack with the target substrate (Fig. 5.2 g and j), which in our case was the PMMA/AFM tip/PMMA/silicon structure (Fig. 5.2f). This is a critical point since manual manipulation can break the cantilever although it is covered by a PMMA layer.

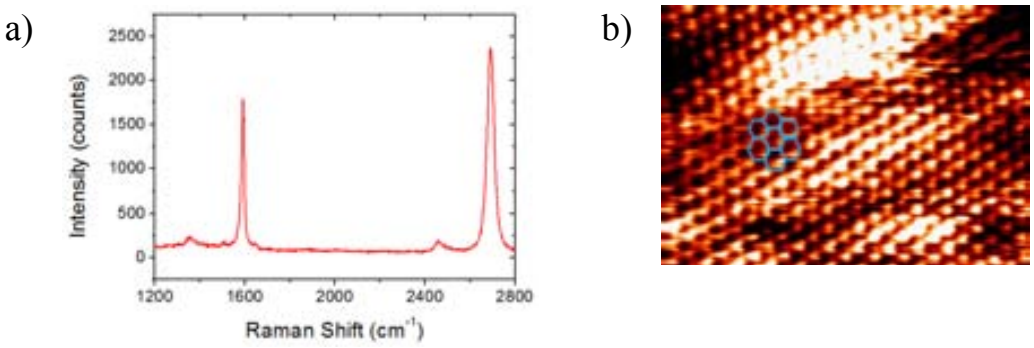

Figure 5.3. (a) shows a Raman analysis of the as-grown graphene/Cu samples used in this work, demonstrating that it corresponds to a GSL. (b) corresponds to a STM image of the graphene sheet. The typical three-for-six lattice of GSL is observed, further supporting this hypothesis.

Finally, when the PMMA/GSL is deposited on the PMMA/AFM tip/PMMA/Silicon stack, to conclude the tip preparation, the different PMMA layers are removed using acetone to deliver the final product (Fig. 5.2 h and k). This is also a critical point because a bad etching would result in PMMA contamination that could reduce the performance of the tips. To remove the PMMA layers, commercially available acetone is heated up to its boiling point of ~68°C. While in a standard transfer process the normal time to remove the PMMA is 5 min (using liquid acetone), in our case, PMMA was etched in vaporized acetone during 30 min. The reasons are, first, because it is necessary to maintain the sample completely horizontal during all the time, otherwise the tip would fall into the acetone and break when the PMMA melts, and second, while the standard transfer process of graphene only uses one PMMA layer, in our structure three PMMA layers must be removed, being especially critical the one between the AFM tip and the graphene (which is necessary to mechanically stabilize the cantilever). To avoid tip contamination by residues left over in the acetone and carefully remove the PMMA, the sample is placed on top a glass container (Fig. 5.4, container A), which contains boiling acetone, being therefore exposed only to vaporized acetone. The second container (Fig. 5.4, container B) serves as vapor enclosure to increase etching

yield. Container B remains opened on the top to avoid that drops of condensed acetone precipitate on the sample (Fig. 5.4). Once PMMA is removed, the tip, covered by the graphene layer, flexes back to its initial position.

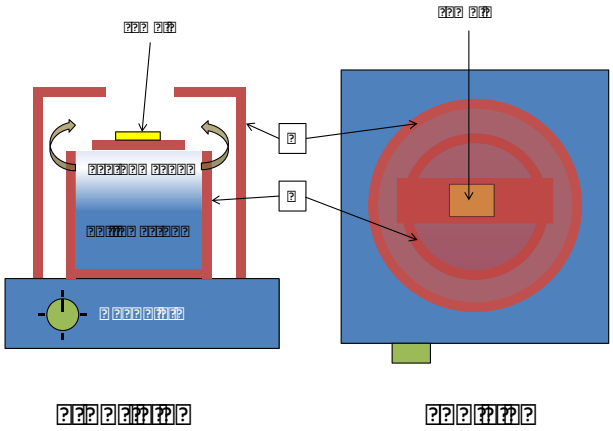

Figure 5.4: Schematic of the home-made engine to remove the PMMA layer while maintaining the sample completely horizontal.

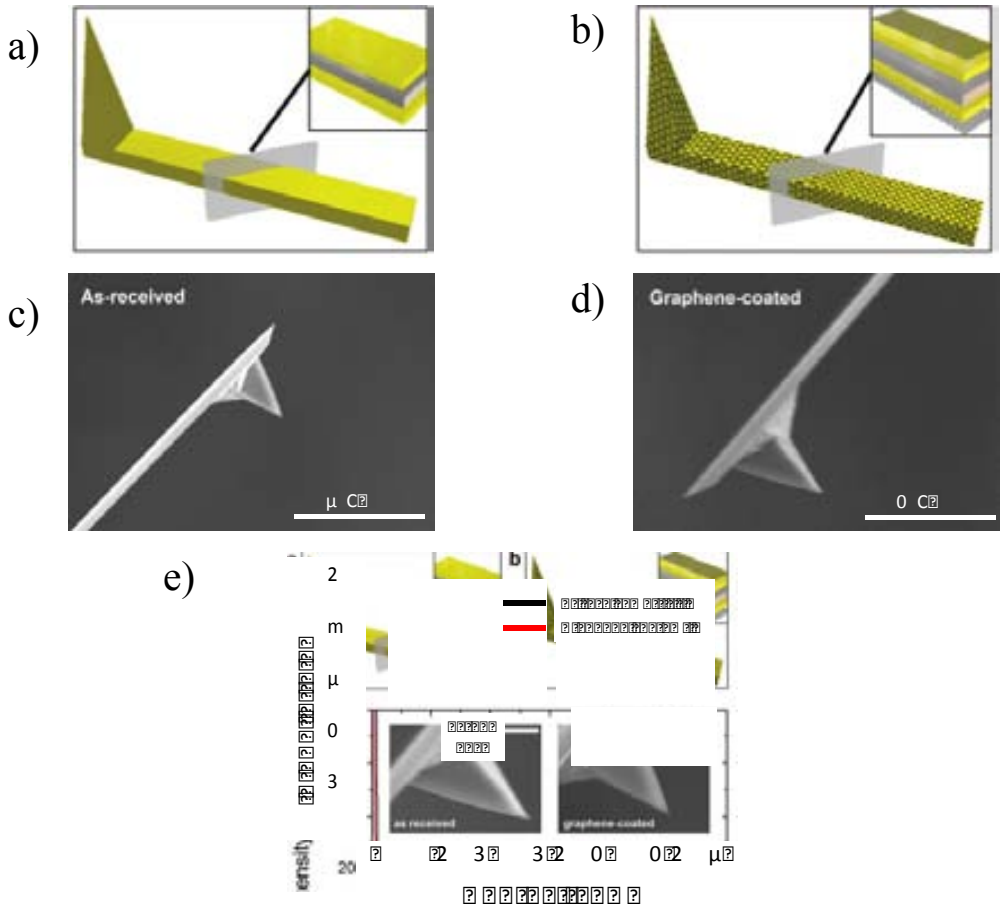

Figure 5.5. Schematic of an (a) as-received, and (b) graphene-coated, commercially available Pt-Ir varnished tip. The bulk of the tip consists of doped silicon (grey), which is varnished with a Pt-Ir alloy (yellow), and the graphene is highlighted with the typical hexagonal lattice. Large area SEM images of both as-received (c) and graphene-coated tips (d). The images show similar sizes and shapes. (e) EDS analysis of both as-received (red line) and graphene-coated (black line) tips.

To confirm that tips were successfully covered with graphene, the chemical composition and size/shape of both, as-received and graphene-coated tips, was analyzed using energy-dispersive X-ray spectroscopy (EDS) and scanning electron microscope (SEM), respectively, using the Hitachi S4800 equipment. Fig. 5.5 shows a schematic (a and b) and a SEM image (c and d) of a Pt-Ir tip before (a and c) and after (b and d) GSL coating. Fig. 5.5e shows the typical surveys measured with EDS on the surface of an as-received (red line) and a graphene-coated (black line) tip. As it can be observed, the only main difference is the carbon content, which is found to be higher on the graphene-coated tip, demonstrating the presence of graphene on it. On the other hand, SEM images (Fig. 5.5c and d) reveal very similar shape and tip radius before and after the graphene coating, and no imperfections related to residual PMMA can be observed.

5.2 Performance of Graphene-Coated Tips

In this section, the graphene-coated tips' performance has been assessed by characterizing different samples.

5.2.1 Experimental: samples and setup

To analyze the performance of graphene-coated tips, their conductivity and mechanical resistance were assessed from the measurement of insulating and conductive surfaces. As insulators, HfO_2/SiO_2 gate stacks (3nm/1nm thick) deposited on an n-doped Si substrate, which is a commonly used standard sample in nanoelectronics, were characterized [Uppal 09, Aguilera 09]. Such gate stack was annealed at 1030°C, leading to the polycrystallization of the HfO_2 layer. Conductive samples were also used to intentionally increase the current that flows through the tips. The conductive samples consisted of as-grown GSL on copper. The properties of the tips were investigated from the measurement of I-V curves and current maps using a Seiko SPI3800N AFM working in high-vacuum (10^{-7} torr), which excludes the effect of the water meniscus formed between the tip and the sample as it would be the case in air conditions. High-vacuum conditions also avoid anodic oxidation and allow measuring currents in both polarities (injecting electrons from the substrate and from the tip). When acquiring I-V curves, the CAFM's current range is raised by combining it with a Keithley 6430 Sub-FemtoampRemote Sourcemeter [Blasco 05]. Due to its excellent current/voltage configurability and ultra-low current noise, it provides the needed functionality to carry out the experiments in the next section, such as the measurement of I–V characteristics with a very wide current dynamic range (1pA–1mA) and different current compliances (CC).

5.2.2 Conductivity of Pt-Ir and graphene-coated tips

The conductivity of graphene-coated tips has been first assessed from the analysis of $HfO_2/SiO_2/Si$ gate stacks. I-V curves at different positions have been measured and analyzed. Fig. 5.6 shows the 1st, 3rd, 5th, 10th, 15th, and 20th I–V curve measured at different random locations on the sample using an as-received tip (Fig. 5.6a) and a graphene-coated tip (Fig. 5.6b). Note that a maximum current of 10^{-4}A is measured,

which corresponds to the CC set in this experiment. For voltages < 7V only noise is measured. As it can be observed, the Ramped Voltage Stresses (RVS) performed with the as-received tip (Fig. 5.6a) show a decrease of the measured current with the number of recorded I-V curves. Since this sample is very homogeneous [Aguilera 09] and each I–V curve was measured at a different location, the changes observed on the I-V curves during the RVS sequence should be attributed to changes in the properties of the tip, and not to the sample. Therefore, Figure 5.6a shows that the as-received tip loses its conductivity or, in other words, the Pt-Ir varnish is worn out due to the highly localized currents flowing through the structure ($J \approx 10^8$ A/cm^2 when current reaches the current compliance, that is, 100μA through an area of 100 nm^2) [Blasco 05]. Note that in this experiment, the tip is not scanned over the surface, so that the reduction of the measured current cannot be attributed to the frictions, but to changes on the electrical properties of the tip. On the other hand, the graphene-coated tip supports several measurements (Fig. 5.6b), which entirely reached the current compliance level approximately at the same voltage without appreciable wearing. The observed differences among the I-V curves of Fig. 5.6b have been demonstrated to be related to the intrinsic inhomogeneities of these kinds of materials [Aguilera 09, Lanza 07, Lanza 11]. Therefore, comparing Fig. 5.6 a and b, the results demonstrate that graphene-coated tips can stand higher current levels than Pt-Ir varnished tips.

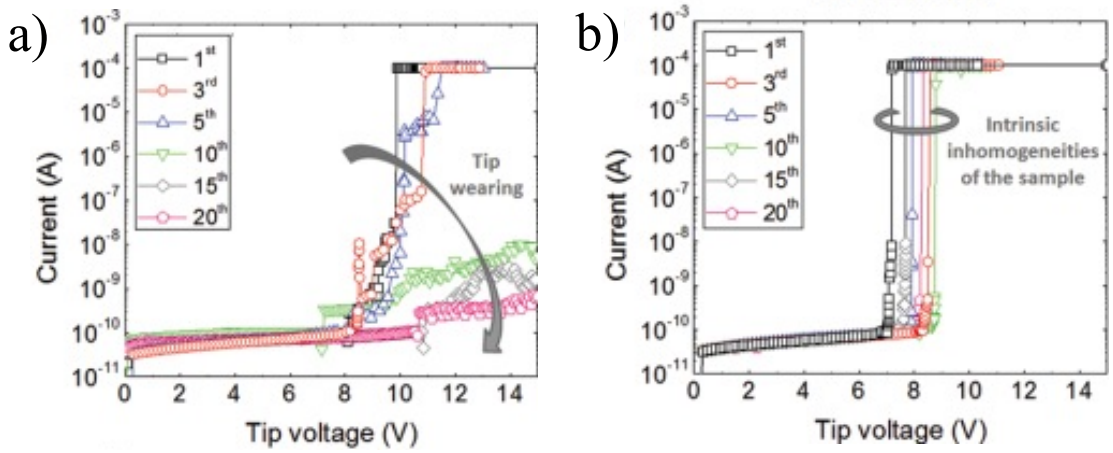

Figure 5.6. *I–V* curves measured on the bare surface of a HfO_2/SiO_2 stack using (a) a Pt-Ir-coated tip, and (b), a graphene-coated tip. Each graph shows the 1st, 3rd, 5th, 10th, 15th, and 20th measured *I–V* curve. All *I–V* curves were collected at different locations by applying a RVS to the tip (sample substrate grounded).

5.2.3 Resistance to mechanical wear-out of Pt-Ir and graphene-coated tips

In this section, the resistance of graphene-coated tips to high frictions is analyzed from topographical and current maps. Only one previous work used graphene-coated tips [Wen 12] to investigate different samples, but in that case, just local I-V curves were measured, so that resistance to frictions was not evaluated. In order to generate a more accelerated tip wearing, conductive samples are used so that higher currents could be easily driven. Fig. 5.7 shows AFM topography (a, b, e and f) and current (c, d, g and h) maps obtained with an as-received Pt-Ir tip (a - d) and a graphene-coated tip (e – h) on a GSL grown on Cu stacks. With both kinds of tips, left images (a, c, e and g)

correspond to those obtained during the first scan while the right images (b, d, f and h) correspond to those obtained after an area of 16μm² and 903μm² was scanned with as-received and graphene-coated tips, respectively. The current maps are recorded by biasing the samples at –0.1V (e. g., substrate injection of electrons) and keeping them under the high vacuum ambient conditions (always below 5×10^{-7} Torr). From all the topographic images (a, b, e, f) the typical stepped copper surface (covered by GSL) can be observed [Han 11]. On the other hand, the current maps (c, d, g, h) clearly overlap with the topographic images, showing current everywhere except at the step edges, probably due to the loss of contact between the tip and the sample at those locations. Comparing the images obtained with the two kinds of tips, one can easily see that as-received tips allow scanning an area of $6\mu m^2$ (6 scans of 1μm × 1μm) before the tip loses its conduction (using a contact force of 5nN). The tip wearing can be observed from the lowering of the current scale in Fig. 5.7d (100pA). However, the maps collected using graphene-coated tips suggest that these tips preserve their intrinsic properties since no loss of conductivity is observed even after scanning a larger area and using contact forces up to 50nN. The total area scanned with the graphene-coated tip was $903\mu m^2$ (150 times larger than using as-received tips) and consisted of 6 scans of 10μm×10μm, 9 scans of 5μm×5μm, 12 scans of 2μm × 2μm, and 30 scans of 1μm × 1μm. The only plausible explanation for this observation is that the graphene layer is effectively protecting the metallic tip varnish from frictions with the substrate, enhancing its lifetime.

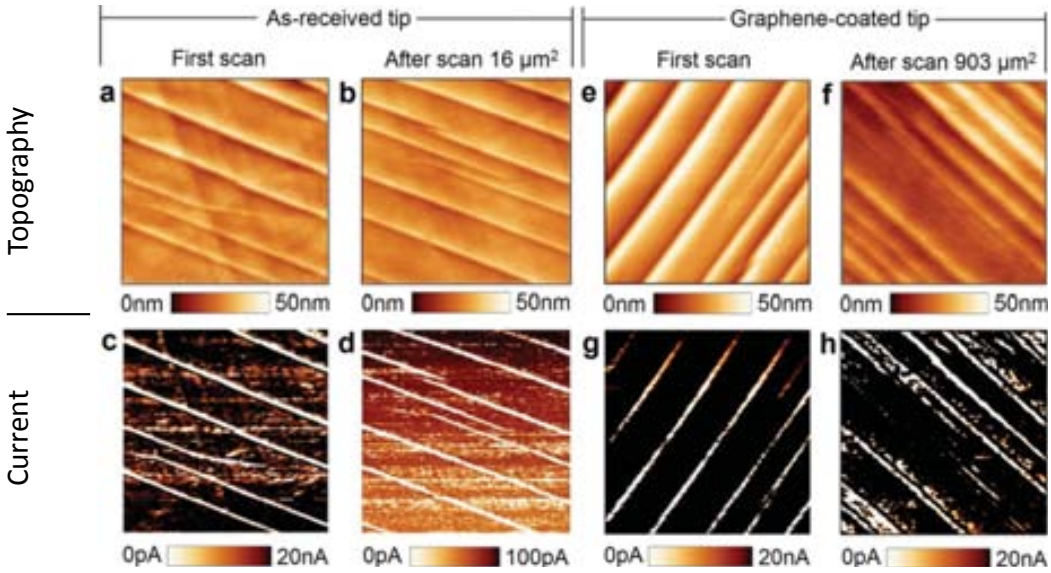

Figure 5.7. Topographic (a,b,e,f) and current (c,d,g,h) maps measured on the surface of GSL/Cu stacks recorded with as-received (a–d) and graphene-coated tips (e–h). All scans are 1μm x 1μm, and the images of each column have been collected simultaneously. The images clearly show that as-delivered tips experiment a substantial conductivity loss after 6 scans, while in contrast, the graphene-coated tips keep measuring current even after have been used to scan an area 150 times larger.

Current maps recorded on high-k dielectrics, for which obtaining reliable consecutive scans is especially difficult [Lanza 10], also confirm this behavior. Fig. 5.8 shows typical current maps obtained on $HfO_2/SiO_2/Si$ stacks with an (a) as-received and (b) graphene-coated tips. Both were obtained after scanning an area of 16μm² and

measuring 20 I-Vs. Note that, the tip only keeps its conductivity when its covered by graphene, further supporting the results shown in Fig. 5.7. Therefore the results show that Pt-Ir tips wear out faster than graphene-based tips. Actually, Fig. 5.9 a and b show the SEM images of both Pt-Ir and graphene-coated tips after 20 *IV* curves and one topographic map similar to those shown in Figures 5.8 a and b. As it can be observed, the Pt-Ir varnish of the tip without graphene can easily be worn out due to the high currents, while the graphene-coated tip keeps its initial sharp shape (and high conductivity).

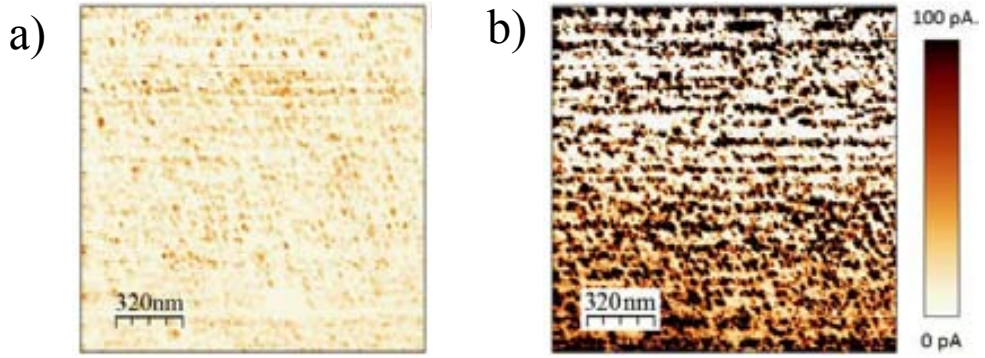

Figure 5.8: Typical current images measured on HfO_2/SiO_2 stacks obtained with an (a) Pt-Ir and (b) graphene-coated tip. Before these images, for each tip, an area of $18\mu m^2$ was scanned, and 20 I-V curves until BD were performed.

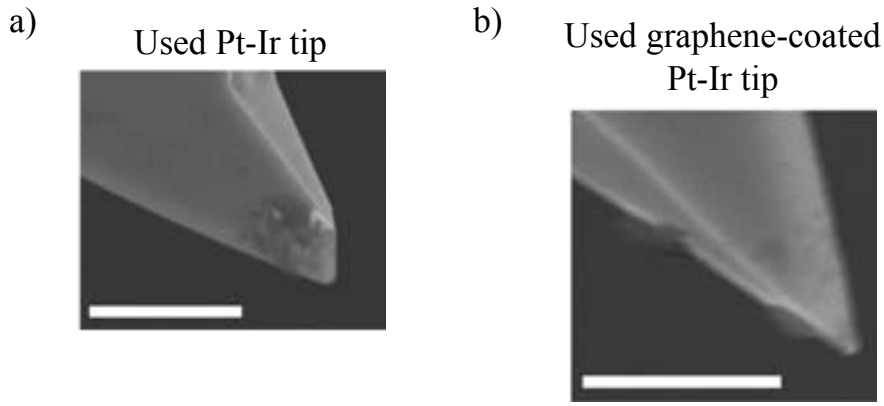

Figure 5.9. SEM images of (a) Pt–Ir, and (b) graphene-coated tips, after 20 *IV* curves and one topographic map. The scale bars in (a) and (b) are 5 μm and 3 μm, respectively.

In conclusion, it has been successfully shown that high performance conductive tips for CAFM experiments can be fabricated by coating commercially available metal-varnished tips with a sheet of GSL with an established standard transfer process. In total, seven different graphene-coated tips have been fabricated and characterized using the procedures here described, and successful results for all of them were observed. Graphene-coated tips are much more resistant to both high currents and frictions than commercially available metal-varnished CAFM tips, leading to much longer lifetimes and preventing false imaging due to tip–sample interaction.

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Chapter 6: Analysis at the nanoscale of graphene layers for nanoelectronic applications

In chapter 1, graphene was introduced as a material with remarkable electronic and mechanical properties which, for example, has been demonstrated to be able to protect the conductive metal varnish of coated CAFM tips (chapter 5). In this chapter, graphene will be investigated for nanoelectronic applications. One aspect that will be analyzed is the presence of corrugations and wrinkles on graphene layers, since they can degrade the transport properties of graphene, increasing the device-to-device variability. The impact of the substrate on which graphene is transferred will be also studied. Since the presence of grain boundaries (GBs) on graphene-single-layers (GSL) can also affect the substrate where it is deposited and graphene electrical properties itself, this topic will be also studied in detail. GSLs will be exposed to oxidative environments to modify the properties of GBs and its influence on various substrates and on the electrical conduction of GFETs will be investigated. Finally, since graphene has been recently started to be used as top electrode in memory devices, the variability and reliability of Graphene-Insulating-Semiconductor (GIS) structures based on Hafnium will be investigated and compared to capacitors with Titanium-Nitride (TiN) as electrode material.

6.1 Nanoscale morphology of graphene on different substrates

In chapter 1, it was introduced that CVD-grown graphene on Cu can be transferred to other substrates using a simple method [Li 09]. That allows the study of the interaction of graphene with other materials, such as SiO_2 or high-k dielectrics, which is essential for the fabrication of graphene-based electronic devices. However, the graphene flakes fabricated by this method can contain many kind of defects, such as topographic imperfections (wrinkles and/or corrugations, see section 1.6.1), that can impoverish their electronic properties and, as uncontrollable defects, can increase the device-to-device variability and could also affect to their reliability [Myer 07, Barnarda 12]. Therefore, the mechanisms of corrugation and wrinkle formation must be clearly investigated. In this section (**PUBLICATION 6**), nanoscale and atomic scale techniques (SEM, STM and AFM) are used to study the density and shape of the morphological imperfections of as-grown (grown on Cu, see section 6.1.1) and transferred graphene sheets on different substrates (section 6.1.2). The transfer process of graphene is the same than that described in section 5.1. In [Zhang 11] (and section 5.1) it was already demonstrated from Raman spectroscopy that the graphene sheets grown by CVD used in this thesis were mainly monolayers.

6.1.1 As-grown graphene on copper substrate

First, we investigated the morphology of as-grown graphene on a copper substrate by scanning the surface with SEM. As Fig. 6.1a shows, the copper substrate is polycrystalline, due to the high temperatures used during the graphene growth process [Han 11]. Moreover, in the zoom-in image (Fig. 6.1b), not only the Cu grain boundaries can be distinguished (blue arrows in Fig. 6.1a and 6.1b) but also a network of long and straight dark lines (which can propagate from one Cu grain to the other, red arrow) can be also detected. Fig. 6.1b also reveals an additional feature: some dark islands, which correspond to multilayer graphene (green arrows), as corroborated by Auger Electron Spectroscopy (AES, which allows to measure the chemical composition). In order to discern whether the dark lines (red arrows) in Fig. 6.1b correspond to wrinkles or not, we analyzed the chemical composition at particular positions of the sample using AES. Fig. 6.1c corresponds to an AES image showing the carbon signal on the plateaus and on the dark lines / red arrow. The results indicate that there is a remarkable increase of the carbon signal on that features (Fig. 6.1c), probably due to the high density of electrons on the top of the wrinkle, a phenomenon also called sub network polarization [Wehling 08]. Moreover, this is accompanied by a reduction of the Cu signal, indicating graphene-copper delamination (yellow arrow). These wrinkles are known to be formed due to the high compressive strain originated from the cooling down after the CVD growth process [Prakash 10, Zhang 11]. The morphology of as-grown samples was also analyzed from topographic AFM maps in which the Cu steps and wrinkles can be clearly distinguished (Fig. 6.1d). The wrinkles induced by the thermal compressive strain do not align to the substrate steps and grain boundaries; instead, they are random. Moreover, in Fig. 6.1d, we can observe that most of the graphene follows the morphology of the material underneath, e.g., the steps on the copper substrate. Comparing the wrinkles and substrate steps in Fig. 6.1d, the results reveal that the height of the wrinkles induced by the thermal strain (~1.6 nm) is larger than the copper steps (~0.5 nm).

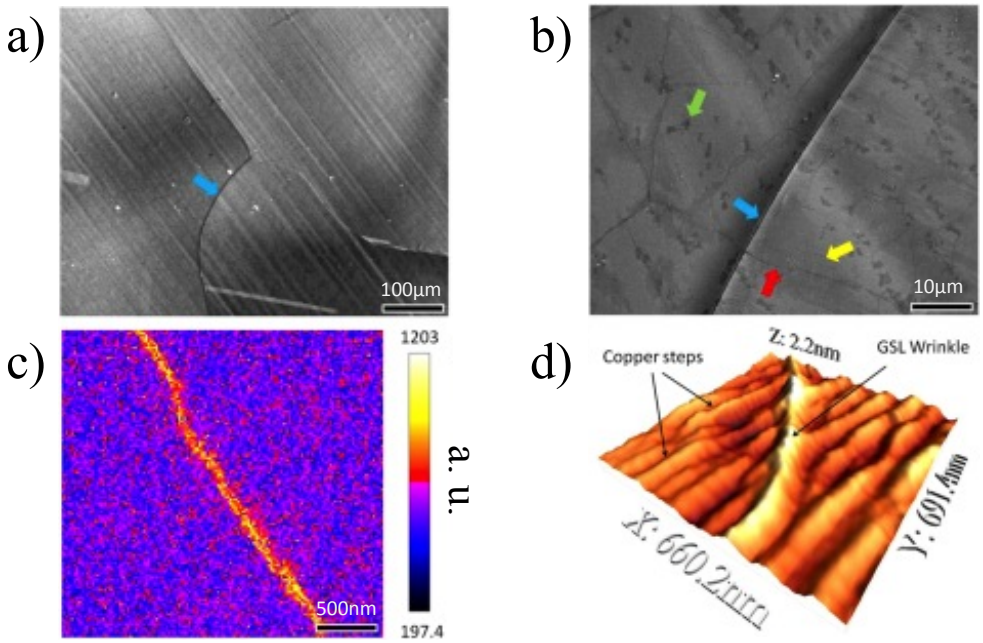

Figure 6.1. (a) Large area SEM image of the as-grown graphene single layer on copper. (b) Zoom-in SEM image which reveals: copper grain boundaries (blue arrow), graphene wrinkles (red arrow), copper lamination (yellow arrow), and multilayer graphene islands (green arrow). (c) AES image showing the carbon signal on the plateaus and on the wrinkle. (d) AFM topographic scan.

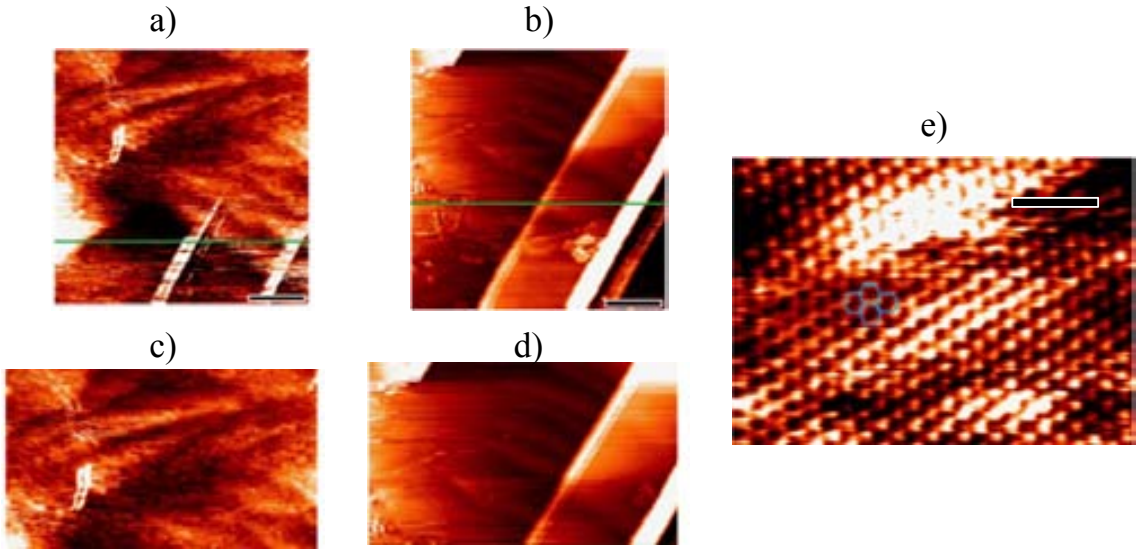

Figure 6.2. STM images of as-grown graphene on Cu where (a) typical wrinkles, and (b) a singular wrinkle followed by lateral delamination, can be observed (the images have been captured with V_{BIAS}=-0.04 V, I_T=-3.43 nA); (c) and (d) show the cross-sections highlighted by green lines in (a) and (b), respectively, which reveal that, in spite of the increase of height and width, the aspect ratio keeps constant. (e) 7nm x 7nm atomic scale image of an area measured at a plateau, where the hexagonal atomic distribution of carbon atoms can be observed (V_{BIAS}=-0.002 V, I_T=9.2 nA). The scale bar is 40 nm for (a), 50 nm for (b), and 1.4 nm for (e).

The morphology of graphene on as-grown samples was also analyzed using STM, which has a larger lateral resolution compared to the AFM. Fig. 6.2 shows two STM images (a and b) and two profiles (c and d) obtained on the green lines marked in (a) and (b) maps. Our experiments have corroborated the existence of wrinkles. Most of them are similar to the ones shown in Fig. 6.2a in which two narrow (<15 nm) wrinkles can be discerned. On the other hand, a lower amount of wrinkles accompanied by lateral delamination has been observed as well (Fig. 6.2b). Curiously, the aspect ratio of both features is very similar (Fig. 6.2c and d, height/width, ~1/6), which is in agreement with the values previously reported for as-grown samples [Zhang 11]. Furthermore, the enhanced resolution of STM provided atomic information about the sample. Fig. 6.2e shows a 7nm x 7nm image measured at a plateau, where the hexagonal atomic distribution of carbon atoms (typical of monolayer sheets, blue hexagons) can be clearly observed at very flat regions.

6.1.2 Graphene transferred on different substrates

The previous section showed that, in as-grown samples, most of the graphene adheres to the copper substrate, but, on the other hand, the compressive strain induced during the cooling process produces wrinkles. However, graphene is generally transferred to target substrates when used in semiconductor devices [Yang 12, Stützel 10, Liu 10, Park 11]. To analyze the impact of the transfer process on the morphology of the graphene layers, we transferred 8mm × 5mm graphene flakes on substrates with different characteristics by keeping the same transfer medium and conditions. The substrates under analysis were flat SiO_2 (RMS = 73.2pm), flat HfO_2 (RMS = 86.3pm) and rough HfO_2 (RMS = 693pm) layers, where RMS (root mean square) refers to the topography. Fig. 6.3a - c show the topographic AFM images of these substrates before the graphene transfer. After using the transfer process described in [Suk 09], at some locations we observed that the corrugations related to the Cu steps and grain boundaries could be transferred to the target substrate, generating folds and buckles. Then, we optimized the transfer process by soaking the sample in pure water for different times [Liu 11]. We observed that, for soaking times above 1 hour, the substrate-induced corrugations could be successfully relaxed; leading to the surface morphology shown in Fig. 6.3d - f, in which the wrinkles induced by the thermal strain can be observed. Interestingly, the shape and density of the wrinkles clearly depend on the roughness of the substrate. In particular, we have observed that the amount of wrinkles on very flat substrates (Fig. 6.3d and 6.3e) is much larger than that on the rough one (Fig. 6.3f). On the other hand, the wrinkles observed in the rough substrate are taller (note that the Z-scales in Fig. 6.3d - f are different) [Prakash 10, Duan 11]. When a compressive strain is applied to a graphene sheet, there is a critical value for which the onset of delamination occurs and, as the strain proceeds, the wrinkles grow in height to minimize it [Mei 07]. Actually, for a given strain, the density and shape of the wrinkles of graphene on different substrates depend on the competition between the elastic energy of graphene and the interaction energy between the graphene and the substrate [Li 10a]. Therefore, the observation of fewer wrinkles in Fig. 6.3f indicates that, in rough substrates, more compressive strains can be relaxed. Moreover, it has been observed that graphene adheres better to high-k materials compared to the SiO_2 substrate (probably due to different interaction forces between the substrate and the graphene), which may lead to the difference of wrinkles between them (Fig. 6.3d and e) [Song 10]. These experimental results have been corroborated from damped dynamic simulations on the morphology of graphene on a

very flat and rough substrates [Lauffer 08]. Preliminary results of such simulations [Brar 07, Lanza 13] show that the density of wrinkles is lower in rough substrates and that the wrinkles formed in rough substrates are taller, further supporting the experimental data of Fig. 6.3.

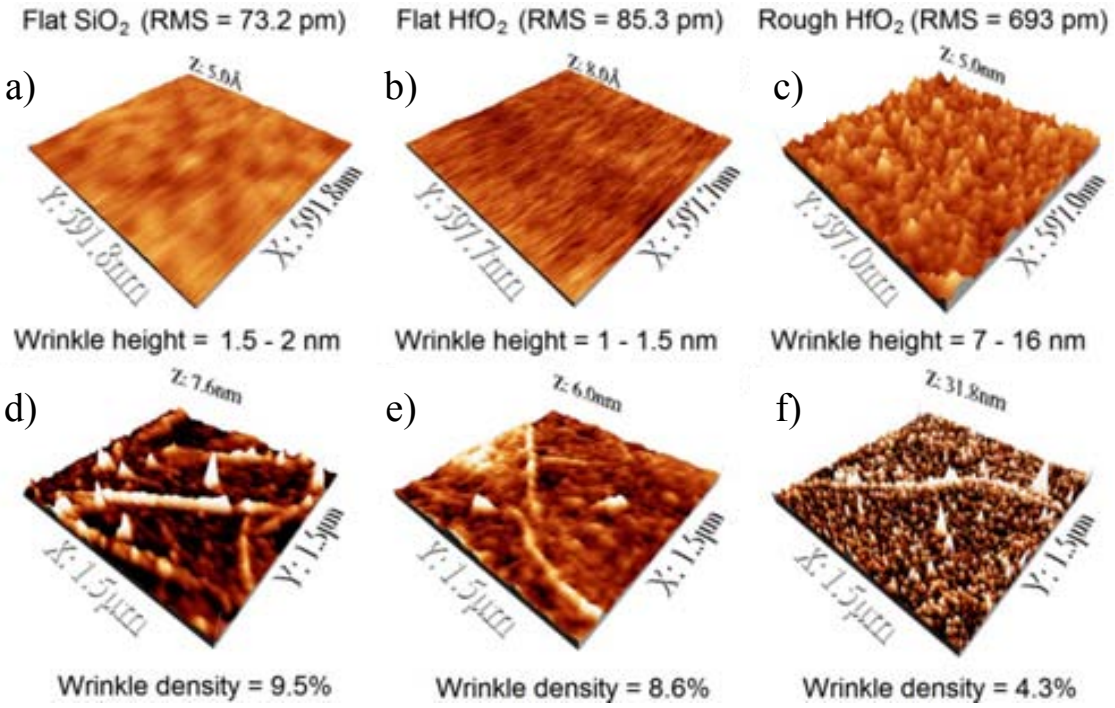

Figure 6.3. (a), (b) and (c): Topographic AFM maps of the three substrates (flat SiO_2, flat HfO_2 and rough HfO_2), respectively. (d), (e) and (f): Typical AFM images of graphene after being transferred onto the substrates in (a), (b) and (c), respectively. The wrinkles height and density reflect the values measured in an area as large as 1800μm^2 and are calculated as the mean distance and percentage of an area above the mean topographic value measured at the plateaus.

6.1.3 Morphology of multilayer graphene

We also analyzed the morphology of multilayer graphene flakes transferred on ultra-flat SiO_2 substrates (similar to the one shown in Fig. 6.3a). Figures 6.4a and b show an optical and AFM topographic image, respectively, in which the typical wrinkles and some graphene bilayer (G2L) or even trilayer (G3L) islands can be clearly discerned. Some bright spots in the AFM image, which correspond to PMMA residues from the transfer process, can be also observed. To corroborate the multilayer nature of the film at some locations, Fig. 6.4c also displays the A-B cross section highlighted in Fig. 6.4b. Note that the height between the different atomic layers (~0.42nm) is comparable to that shown by other authors in [Lauffer 08]. Then, we analyzed the topographic images obtained with the AFM depending on the amount of graphene layers. Figure 6.5a shows the histogram of heights and the RMS value (inset) of the topographic maps measured on the plateaus of G2L/SiO_2 and GSL/SiO_2. The histogram and RMS values of the SiO_2 are also shown as a reference. Each histogram is the mean value of 8 scans that sum a total plateau area of 6μm x 6μm.

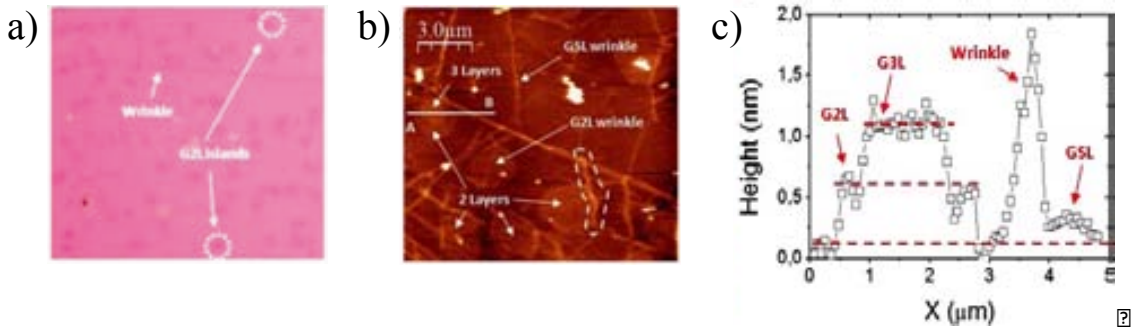

Figure 6.4. Optical (a) and topographic AFM (b) images of a GSL sheet on SiO_2 with a lot of multilayer islands. A typical wrinkle is outlined in (b). (a) is 50µm x 50µm and Figure (b) is 15µm x 15µm. (c) Section AB in (b) where the topographic profile of graphene sheets with different atomic thicknesses can be observed.

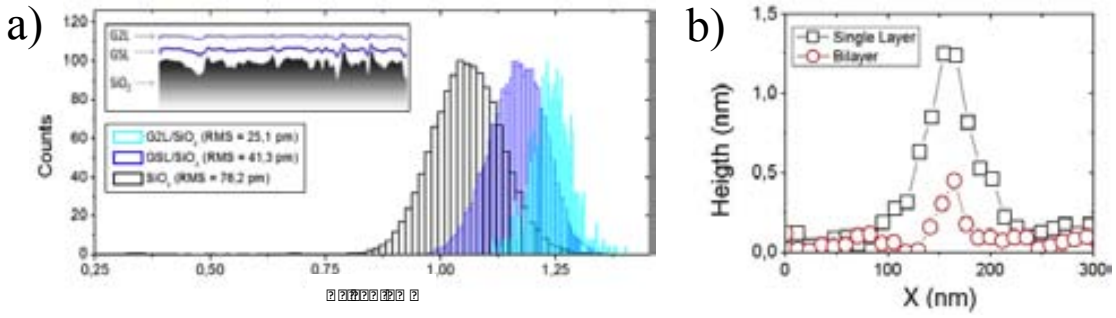

Figure 6.5. (a) Histogram and root mean square (RMS) value of topographic maps measured on the plateaus of GSL on SiO_2 (GSL/SiO_2) and graphene bilayer on SiO_2 ($G2L/SiO_2$). The histrogram and RMS value of the SiO_2 substrate is also shown as a reference. The inset is a schematic displaying the shape of the graphene depending on the amount of layers. (b) Comparison of GSL and G2L wrinkles centered at their respective maximum values.

The results clearly show that the RMS value of the topography decreases with the number of graphene layers, which means that the GSL sheet tries to follow the substrate morphology, but it cannot adhere perfectly, leaving suspended regions (inset in Fig. 6.5a). Note that this behavior was previously observed for as-grown epitaxial SiC-0001 Graphene sheets [Lauffer 08] but, on the other hand, our topography RMS values are slightly larger and comparable to those measured in [Brar 07] for SiC. Finally, we analyzed the size of the wrinkles observed in both layers. Fig. 6.5b shows the cross section of two typical GSL and G2L wrinkles. Curiously, as in GSL on substrates with different roughness (Fig. 6.3), the wrinkles are larger in the rougher media, that is, the wrinkles in GSL are taller than in G2L. Since taller wrinkles are known to contain larger compressive strains [Duan 11] these observations clearly indicate that lower compressive strains in graphene can be effectively relaxed by placing them on a rough substrate.

In conclusion, in this section, we have demonstrated that substrate induced corrugations and strain-related wrinkles present in CVD-grown graphene on copper, which are harmful in device fabrication, can be effectively reduced by optimizing the transfer

process and adequately tuning the morphology of the substrate, respectively. Our results indicate that, while the compressive strain in graphene on flat substrates is minimized by creating wrinkles, on rough substrates, it is minimized by improving the graphene-substrate adhesion. Those experimental observations are further supported by damped dynamic simulations. This new methodology to tune the amount of wrinkles in graphene flakes could pave the way to the design of high quality graphene based devices.

6.2 Modification of graphene properties in oxidative environments and impact on GFETs performance

As introduced in chapter 1, graphene has been proved to protect the underlying material from oxidation when exposed to different media. However, the passivizing properties of graphene in air atmosphere and at room temperature, which fits the operating conditions of many electronic devices, still remain unclear and can strongly depend on its polycrystalline structure. In this section, we analyze the oxidation kinetics of Graphene/Cu samples in air atmosphere and at room temperature for a long period of time and we compare these results with those obtained for similar samples treated in H_2O_2. In this very preliminary study, the effect of the local oxidation on the electrical properties of GFETs is also investigated (**PUBLICATION 7**).

6.2.1 Experimental

The samples under analysis consist of polycrystalline GSL grown by Chemical Vapor Deposition (CVD) on Cu, following the process described in reference [Li 09] and in section 5.1. The typical diameter of the graphene domains in samples fabricated by this method is 1-3 μm [Ahmad 11, Kwon 12, Orofeo 12, Ismach 10, Han 11, Robertson 11]. Although recent works achieved larger graphene domain sizes [Li 10b], in this section we strategically used these samples (with domains in the μm range) to be easily analyzed with the nanoscale techniques. The oxidation of the samples was induced in two ways: i) some sets of samples were kept in air atmosphere and at room temperature (relative humidity 35%) for different times; and ii) accelerated oxidation tests were performed by immersing the samples into hydrogen peroxide (H_2O_2) at room temperature for different times [Chen 11]. Therefore, in total we analyzed six sets of GSL/Cu stacks: as-grown, kept in air atmosphere for 1, 29 and 113 days, and soaked in H_2O_2 for 1 and 4 hours. Moreover, we transferred as-grown and treated (soaked in H_2O_2) GSL sheets to different insulating substrates using Poly-methyl Methacrylate (PMMA) as solid medium (see chapter 5), and etching the original Cu substrate [Suk 11, Regan 10]. Two different target substrates were used: the first consists of a 2.5nm thick Hafnium Dioxide (HfO_2) layer on a p-type silicon substrate with 1nm SiO_2 interfacial layer (2.5nm HfO_2 / 1nm SiO_2 / p-type Si); and the second is a 300nm thick SiO_2 gate oxide on a p-type silicon substrate. The lateral electrical properties of both, as-grown and treated GSL sheets, were measured by patterning GFETs with Electron Beam Lithography (EBL). Single back-gate GFETs with L=40μm and W=20μm were fabricated. To do so, after the graphene sheet was transferred to the desired substrate, the samples have been covered with PMMA (Fig. 6.6 step 1). After that, the active areas of the device are defined with EBL and etched with Methyl-Isobutyl-Ketone (MIBK) (Fig. 6.6 step 2). Once the PMMA of the selected areas is removed, the etching of

Graphene was done with a Diener Femto plasma furnace (Fig. 6.6 step 3) using energies of 90W during 3 minutes (although these parameters may vary depending on the equipment). Then, the rest of PMMA is removed (Fig. 6.6 step 4), normally with acetone. Once the areas with and without Graphene are delimited, we have to deposit the electrodes on the desired parts. To do this, we covered again the sample with PMMA and removed some parts of the PMMA using EBL and MIBK (Fig. 6.6 steps 5 and 6 respectively). Once those areas have been delimited, a 40-80 nm thick palladium layer was deposited on the sample (Fig. 6.6 step 7). Finally, the PMMA will be removed with acetone (Fig. 6.6 step 8) and the metallic layer will only remain on those areas that we delimited. The measurements presented in this section have been obtained by using Scanning Electron Microscope, Conductive Atomic Force Microscope and Auger Electron Microscope,

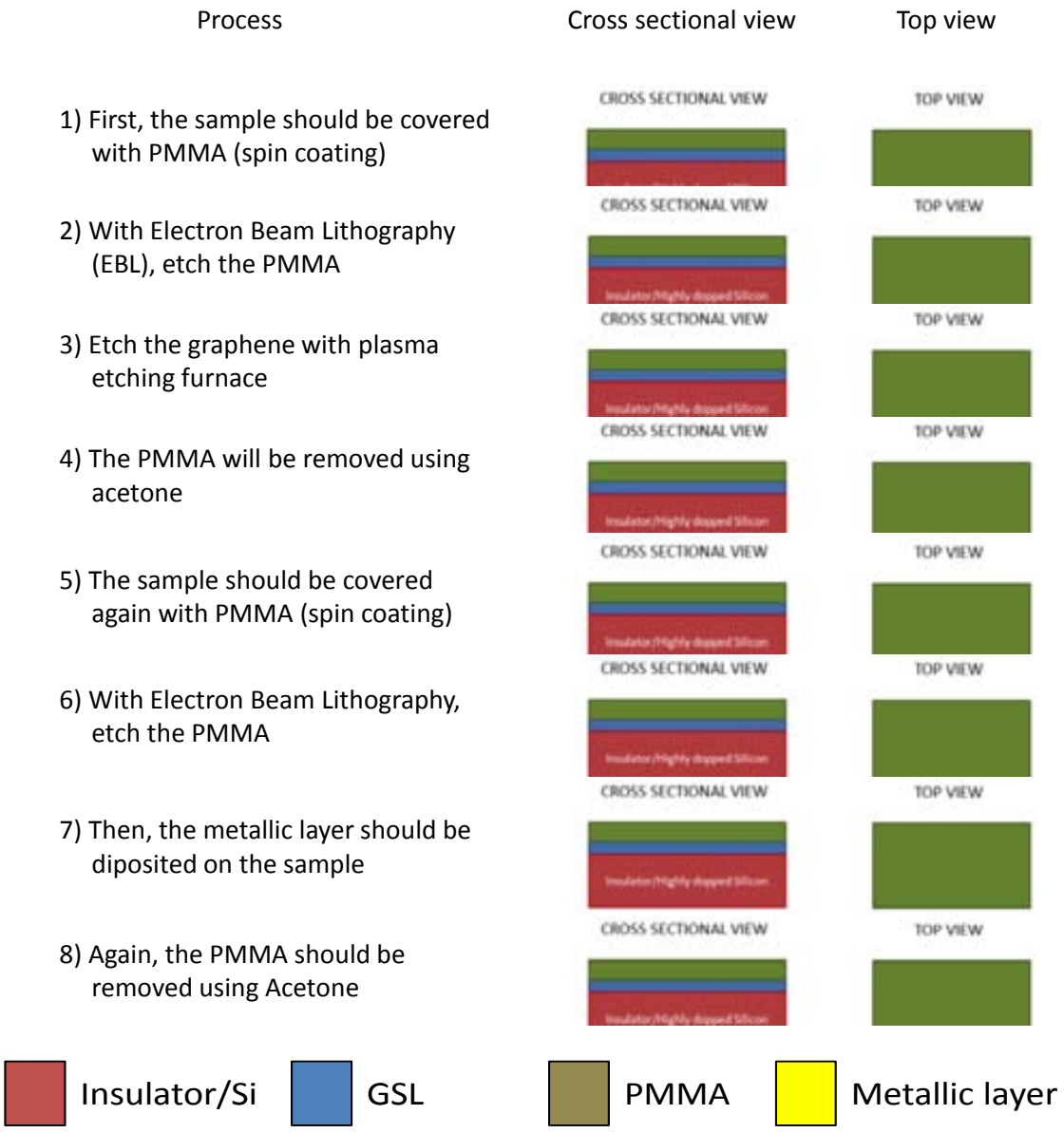

Figure 6.6. Process description of the fabrication of Single Back Gate GFETs.

6.2.2 Oxidation of graphene grown on copper substrate

In this section, the morphological and the electrical properties of GSL/Cu stacks subjected to different oxidative environments are presented. SEM images of different GSL/Cu stacks are shown in Fig. 6.7. Fig. 6.7a shows a typical image obtained on the as-grown GSL. The different features of the copper surface, such as copper grain boundaries and copper steps, can be easily distinguished [Han 11]. These features are generated due to the high temperatures used during the CVD growth of graphene [Zhang 11]. On the other hand, when a GSL/Cu stack is exposed to an oxidative environment (H_2O_2 or air atmosphere) its morphology remarkably changes. As an example, Fig. 6.7b shows the typical SEM image of the same sample after being immersed in H_2O_2 for 4 hours. As it can be observed, a very dense network of corrugations was formed on the GSL. Fig. 6.7c and d show zoom-in SEM images obtained on GSL/Cu samples soaked in H_2O_2 for 1 and 4 hours, respectively. The images show that, after 1 hour (Fig. 6.7c), a large amount of bright spots have been formed (red lines). Interestingly, these bright spots delimitate areas with typical diameters of 1-3 µm, in agreement with the domain sizes previously reported for this fabrication method [Ahmad 11, Kwon 12, Orofeo 12, Ismach 10, Han 11, Robertson 11]. At the longest immersion time (Fig. 6.7d), these bright spots can propagate to the surrounding areas and, after 4 hours, those corrugations partially covered the graphene domains (the schematic red lines became wider in Fig. 6.7d).

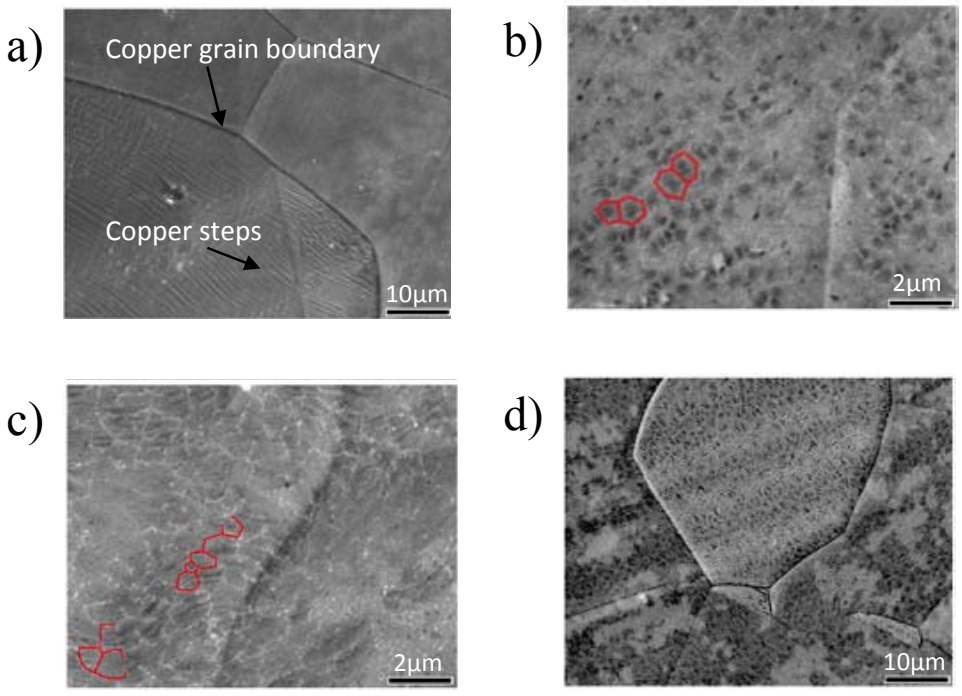

Figure 6.7. Large area SEM images of (a) an as-grown GSL on Cu, and (b) a GSL on Cu after soaking it in H_2O_2 for 4 hours. (c) and (d) show zoom-in images of samples soaked in H_2O_2 for 1 and 4 hours, respectively. The solid red lines in (c) and (d) represent oxidation at the domain boundaries, which can propagate with the soaking time (they become wider in (d)).

To be completely sure that these features are related to the H_2O_2 treatment, we partially immersed a fresh GSL/Cu sample in the H_2O_2 for one hour and we measured topographic AFM maps at the border. The results indicate the presence of corrugations only at the immersed area (see Fig. 6.8). Such corrugations were also observed in samples that were kept in air atmosphere. Since these corrugations delimitate areas of the order of the graphene domain sizes, they could be related to graphene grain boundaries, which surround graphene domains. Such GBs do not protect the substrate underneath, leading to the oxidation of Cu at the sites, which can widen by increasing the time of exposure to oxidative ambient.

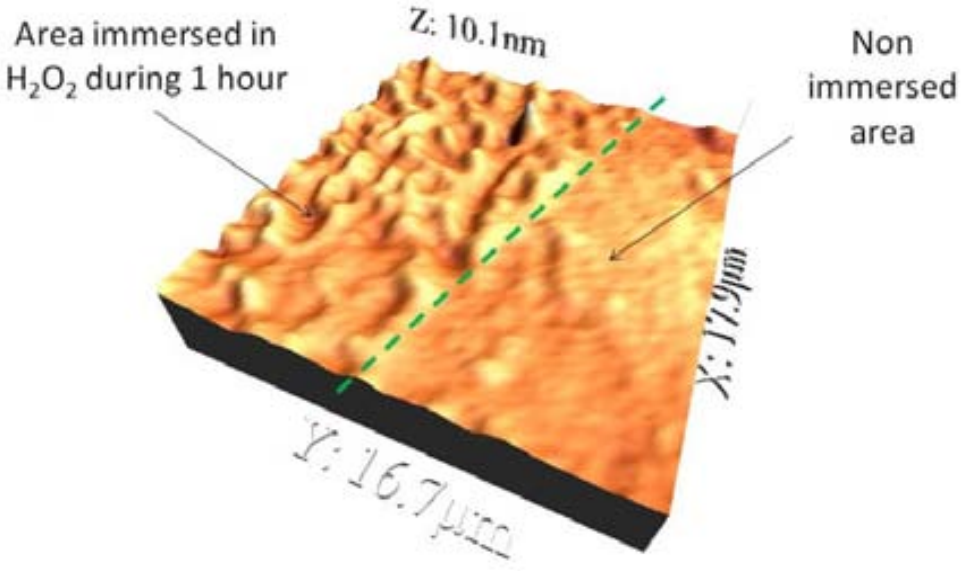

Figure 6.8: AFM topographic map of a GSL/Cu sample after being partially immersed in H_2O_2 during one hour. Surface modification only takes place at the immersed area.

A comparison between the samples immersed in H_2O_2 and those kept in air atmosphere was performed from the measurement of the height, width and density of the topographic changes detected by AFM. The topographic AFM image of the as-grown GSL/Cu sample (Fig. 6.9a) just shows the typical copper grain boundaries and steps, in agreement with Fig. 6.7a. Fig. 6.9b and c show the typical topographic AFM images for the samples soaked in H_2O_2 for 1 and 4 hours, respectively. As it can be observed, the whole area of the sample is covered by a very dense and quasi-periodic network of corrugations (brighter areas) similar to that observed in Fig. 6.7c and d. Using the AFM software, we statistically analyzed the density and size of these hillocks, and the results are summarized in Table 6.1. Note that, the height, width and density of the hillocks (defined as the surface area that is slightly above the average height of the map) increase with the soaking time. The effect of the air atmosphere on the morphology of the samples was also analyzed. After 1 day, no corrugations have been observed (Fig. 6.9d and zoom-in); after 29 days we observed some areas with a high density of hillocks while others kept unaltered (Fig. 6.9e); finally, after 113 days, the whole surface showed the typical quasi-periodic network of hillocks along the graphene domain boundaries (Fig. 6.9f). Note in table 6.1 that the hillocks formed after 29 days (Fig. 6.9e), when found, showed similar sizes as those observed after 113 days (Fig. 6.9f), indicating that the width and height of these hillocks tends to saturate. On the other

hand, the samples soaked in H_2O_2, showed morphological changes that took place much faster, although oxidation kinetics also shows saturation. Comparing the images of Fig. 6.9c and f it can be concluded that the corrugations observed in samples kept in air atmosphere for a long time (~100 days) look similar to those formed in the samples treated with H_2O_2 during 4 hours. These hillocks outline plateaus which shapes and sizes that agree with those previously observed [Ahmad 11, Kwon 12, Orofeo 12, Ismach 10, Han 11, Robertson 11], indicating that hillock formation, related to the oxidation of the substrate underneath, only takes place at the graphene domain boundaries [Chen 11]. It is worth noting that, even if graphene domain boundaries are normally 0.5 nm wide [Huang 11], the paths of hillocks that outline the graphene domains in Fig. 6.9b are much wider. That indicates that, even if the onset of surface modification takes place at the domain boundary, this reaction (the substrate oxidation) can diffuse to surrounding areas with time, which can drastically reduce the performance of a whole graphene sheet.

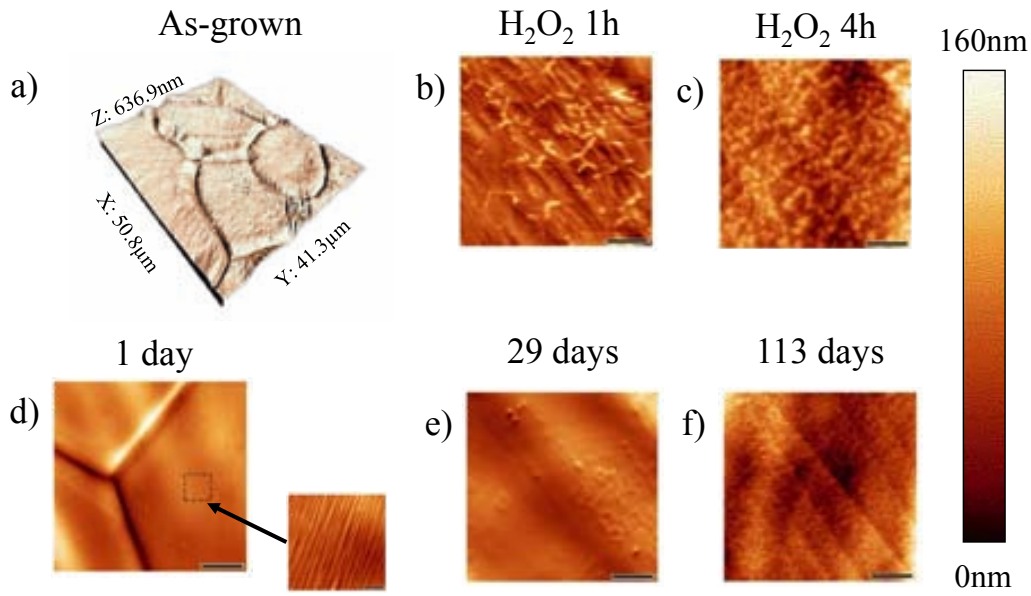

Figure 6.9. Topographic AFM images measured on the surface of as-grown GSL/Cu samples (a), soaked in H_2O_2 for (b) 1 hour and (c) 4 hours, and kept in air atmosphere for (d) 1 day, (e) 29 days and (f) 113 days. The scale bars are 3µm for image (b), 4µm for image (c), 7µm for images (d), (e) and (f), and 1µm for image (d), zoom-in.

	Height (nm)	Width (nm)	Density (% area)
(a) In RA 1 day	-	-	1.03
(b) In RA 29 days	11.5±2.6	204.1±20.1	12.6
(c) In RA 113 days	11.0±2.1	200.7±15.3	35.3
(d) In H_2O_2 1 hour	10.8±3.2	178.1±32.5	23.6
(e) In H_2O_2 4 hour	11.6±2.0	197.3±19.2	37.22

Table 6.1 Height, width and density of hillocks formed on the samples after the exposure to room atmosphere (RA) and H_2O_2.

Once the kinetics of surface modification was explored for each sample, the intrinsic properties of the hillocks have been analyzed by CAFM and AES. Figures 6.10a and b show a typical simultaneously topographic and current image (respectively) measured on the sample that was immersed in H_2O_2 for one hour. As it can be observed, both images clearly overlap, indicating a drastic conductivity reduction at those locations where the hillocks were formed and leading to an inhomogeneous current distribution. Similar current behaviors have been observed at the hillocks formed in the samples oxidized in air atmosphere. Fig. 6.10c and d correspond to current maps of samples oxidized in air atmosphere during 29 and 113 days, respectively. Note that electrical properties depend on time. Fig. 6.10d shows smaller current than Fig. 6.10c. Therefore, the oxidation of the sample can degrade and change the electrical properties of graphene-based devices with time.

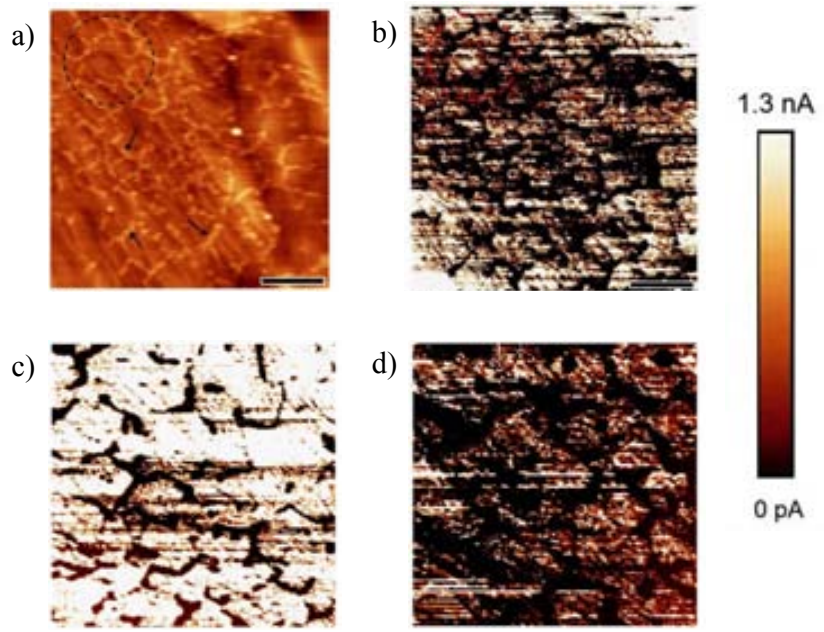

Figure 6.10. Simultaneously obtained (a) topographic and (b) current maps when scanning the surface of a GSL/Cu sample that was soaked in H_2O_2 for 1 hour. Current maps corresponding to the samples oxidized in air atmosphere and at room temperature during (c) 29 days and (d) 113 days. The scale bars in (a) and (b) are 3μm, Figure (c) is 11 μm x 11 μm and (d) is 7.8 μm x μ7.8 μm. The current signal is impoverished as the time increases.

To confirm that this network of hillocks is not related to ripples and/or wrinkles on the graphene layer, we etched the GSL using plasma furnace. Fig. 6.11a shows the typical topographic AFM image after the etching process, where the remaining corrugations can be easily observed. In the next step, we analyzed the chemical composition of the hillocks using AES. Fig. 6.11b shows the typical survey obtained on a plateau and on a hillock formed along the graphene domain boundaries on the sample immersed in H_2O_2. The AES intensity vs. kinetic energy plot clearly shows a remarkable increase of the oxygen peak when measuring on the hillocks. This result is also supported by AES oxygen maps (Fig. 6.11c), which reflects differences in the amount of oxygen measured on the plateaus and boundaries. Note that the oxygen signal and the bright spots observed in the SEM and AFM images (inset in Fig. 6.11c) clearly show the same pattern. Therefore, the immersion of the GSL/Cu sample in H_2O_2 produces high

concentrations of oxygen at the GSL domain boundaries (Fig. 6.11c). These results suggest again that the topographical changes, although triggered at the GBs of the graphene, also affect the substrate. The presence of an excess of oxygen in that positions demonstrates that the hillocks can be related to the oxidation of the underneath substrate. This oxidation affects also the graphene, making GBs less conductive and the GSL much more inhomogeneous, which can remarkably degrade the performance of a graphene based device and can increase the device-to-device and time variability dependence of their electrical properties. Therefore, this phenomenon can represent a very important source of variability in graphene-based electronic devices [Ouyang 10], in which the current must be transported through/along a graphene flake, like graphene transistors, super capacitors and all devices containing graphene electrodes [Ouyang 10, Chen 10, Wang 11].

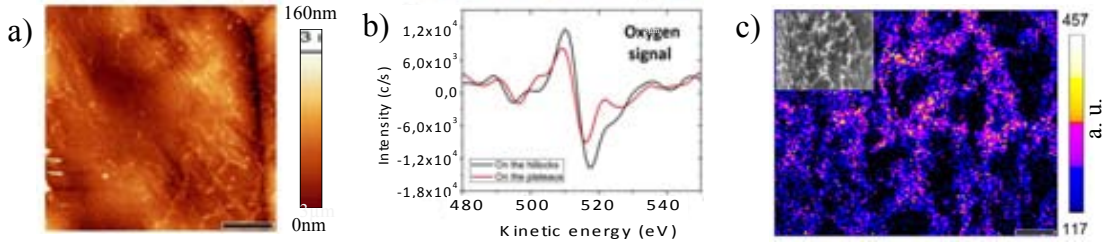

Figure 6.11. (a) shows the typical topographic image obtained on the sample soaked in H_2O_2 for 1 hour after etching the GSL layer by plasma etching. (b) AES oxygen signal measured on the plateaus and hillocks of the same sample. (c) AES map showing the content of oxygen on the GSL/Cu sample soaked for one hour. The inset shows the SEM image obtained at the same location.

6.2.3 Transfer of oxidized graphene on dielectric substrates

In the previous experiments we have seen how the presence of grain boundaries in GSL can lead to the oxidation of the GSL/Cu stack and, therefore, alter its roughness and conductivity characteristics. Now we will analyze the morphological and electrical properties of as-grown and locally oxidized graphene sheets after being transferred to different substrates. The graphene sheet of both, as-grown and treated (immersed in H_2O_2 during 1 hour) GSL/Cu samples, was transferred (using the same methodology described in chapter 5) to a substrate that consists of a 2.5nm HfO_2 / 1nm SiO_2/ p-type Si stack. Fig. 6.12 a and b show typical SEM images obtained on as-grown and treated samples respectively. Note that in the as-grown sample, some morphological changes can be observed. From the measurement of AES maps, which show an increase of the carbon at these sites, it can be concluded that they can be attributed to wrinkles related to the compressive strain. On the other hand, a network of plateaus outlined by bright lines can be distinguished in the SEM image obtained from the treated sample (Fig. 6.12b). It is worth noting that, unlike in GSL/Cu sample, no substantial topography increase has been observed with the AFM at those locations, discarding the presence of hillocks. The composition of these bright lines was analyzed by AES. Fig. 6.12c and d show the carbon and oxygen maps measured with AES on the treated sample. As it can be observed, the carbon signal is drastically reduced at the boundaries, indicating that the graphene is physically broken at those locations [Wei 12]. This hypothesis is further supported by the oxygen map (Fig. 6.12d), which indicates that those locations are rich

in oxygen (from the underlying HfO_2 stack). Again, it is worth noting that the size of these features perfectly agrees with the size of the hillock paths observed in Fig. 6.9-11 and with the graphene domain boundaries in references [Ahmad 11, Kwon 12, Orofeo 12, Ismach 10, Han 11, Robertson 11]. Therefore, these observations clearly indicate that oxide hillocks formed along the graphene domain boundaries before the transfer to other substrates could generate cracks at those locations and alter the electrical properties of the GSL even when transferred to other substrates.

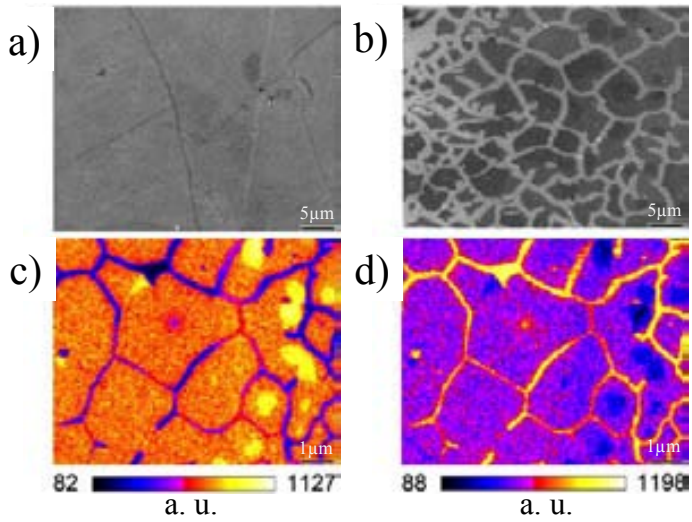

Figure 6.12. (a) Typical SEM image obtained for an as-grown GSL on an $HfO_2/SiO_2/Si$ substrate. The typical graphene wrinkles can easily be observed. (b) SEM image of the same sample with graphene that was soaked in H_2O_2 for 1h. (c) and (d) show the carbon and oxygen AES maps (respectively) of an area shown in (b). The grain boundaries show an increase/reduction of the carbon/oxygen concentration.

6.2.4 Graphene based transistors

In this section, the effect of local oxidation of the graphene grain boundaries on the electrical characteristics of graphene based transistors (GFETs) is analyzed. We evaluated the lateral conductivity of GFETs fabricated (see section 6.2.1) from as-grown and 1h-H_2O_2 immersed GSL, which have been transferred to $HfO_2/SiO_2/Si$ stacks. Fig. 6.13a shows a schematic for both devices, where the graphene domain boundaries in the treated device are highlighted with dashed lines. The topographic AFM image of a treated GFET can be observed in Fig. 6.13b. The GSL channel between both electrodes is delimited by dashed lines.

Four as-grown and four treated devices were characterized using the Agilent 4156C semiconductor parameter analyzer and the probe station. Fig. 6.13c shows the drain current vs. gate voltage (I_{DS}-V_G) curves for both as-grown (triangles) and treated (circles) devices when keeping constant the drain-source voltage (V_{DS}) to 0.1V. Note that the variability is large in both cases, suggesting that the inhomogeneities introduced by the presence of oxidized paths, although they could be important, are not the only factor that leads to such device-to-device variability. However, a remarkable reduction of I_{DS} for the same gate and drain voltages can be observed in treated devices, which is probably related to oxidized paths and cracks along the graphene domain boundaries (Fig. 6.12), indicating a huge reduction of the effective area through which the electrons can flow.

We also analyzed the effect of high lateral electrical fields. In this case, to avoid the dielectric breakdown of the underlying oxide stack, we fabricated similar GFET devices placing as-grown and treated GSL sheets on a 300 nm thick layer of SiO_2 grown on an n-type Silicon (GSL/SiO_2/Si). For this experiment V_G was kept constant to 40V and V_{DS} was ramped (Fig. 6.13d). For both, the as-grown and treated devices, the current increases until a given voltage in which the current from source to drain immediately decreases until zero. We believe that at very high voltages the graphene sheet cannot withstand such high current densities and physically breaks, a phenomenon also called electro migration [Chen 12]. The interesting point is that, not only the current driven by the treated graphene sheet is lower (in agreement with Fig. 6.13c), but the voltage necessary to induce the physical breakdown is also lower, pointing out again that treated samples show a lower mechanical performance. Therefore, local oxidation of graphene in both H_2O_2 and air atmospheres can be very harmful in applications that require graphene sheets with a high lateral conductivity, like GFET, among others [Bae 12].

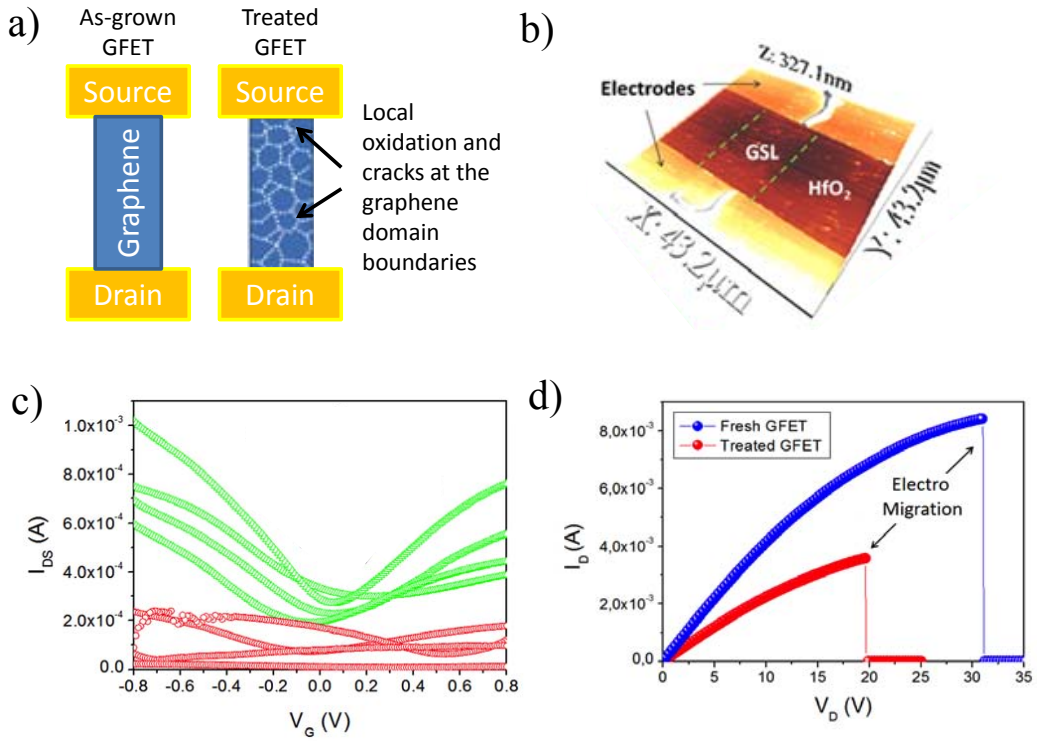

Figure 6.13. (a) Schematic of two GFETs with a as-grown and locally oxidized graphene channel. (b) shows a topographic AFM image of a single back-gate GFET with a locally oxidized graphene channel. (c) I_{DS}-V_G curves for four different fresh (triangles) and locally oxidized (circles) GFETs with W = 20 μm and L = 40 μm. (d) Typical I_D-V_D curves for a as-grown and a treated device showing the voltages in which electro migration takes place in.

In conclusion, in this section we have seen that the presence of grains boundaries on graphene layers can affect the substrate underneath. The material below the graphene domain boundaries can oxidize just by keeping the samples in air atmospheres for long periods of time. Such oxidation leads to insulating hillocks which can grow along the graphene domain boundaries until reaching saturation. Our experiments point out that local oxidation remarkably impoverishes the roughness, conductivity and mechanical resistance characteristics of the graphene sheets, which affects the performance of GFETs by reducing their conductivity and impoverishing their reliability.

6.3 Dielectric breakdown and Variability of Graphene-Insulator-Semiconductor structures

To date, Graphene has been widely studied as conductive channel in Graphene-based transistors [Schwierz 10, Britnell 12]. In particular, in section 6.2 we investigated how graphene properties can affect the performance of GFETs when it is used as conductive channel. However, recently, graphene has been started to be used as top electrode in non-volatile memory devices [Son 10], showing excellent retention times [Ji 11]. In spite of this, currently, the use of Graphene-Insulating-Semiconductor structures (GIS) is still incipient, and more information about their electrical performance is necessary. In this section, a study of the variability and reliability of Hafnium-based GIS structures using the Conductive Atomic Force Microscope (CAFM) is presented. Their electrical properties have been compared to identical capacitors with top Titanium Nitride (TiN) electrode.

6.3.1 Experimental

Standard 1μm^2 MIS structures with an n-type silicon substrate and a ~2nm thick Atomic Layer Deposited (ALD) HfO_2 film grown at 300ºC on a 1nm thick SiO_2 interface layer were initially considered. A stack of Poly-Silicon/TiN was deposited on top of the HfO_2 layer as gate electrode, leading to Poly-Silicon/TiN/HfO_2/SiO_2 gate stacks, called from now on MIS structures (Fig. 6.14). The HfO_2 layers here studied were not subjected to any annealing other than the thermal budget applied during Si deposition, at 500ºC, remaining therefore, amorphous.

On some of blanket identical structures, the top Poly-silicon/TiN electrode was etched (Fig. 6.14). The etching process consists of 3 steps:

1) An etch of the native oxide of the Poly-Si with HF (10%) during 10s.

2) An etch of the poly-Si layer with KOH (10%) during 20 minutes at room temperature.

3) An etch of the TiN layer with H_2O_2 (10%) during 30 minutes at 50°C.

After the etching of the Poly-Silicon/TiN electrode, a Graphene Single Layer (GSL) sheet was directly transferred onto the bare HfO_2/SiO_2 stack following the procedure described in section 5.1. The active area of the GIS capacitors was patterned via Local Anodic Oxidation (LAO) using a CAFM tip [Weng 08, Giannazzo 11]. Fig. 6.15a shows a topographical image of a 1μm^2 squared GIS structure, where the active area of the GIS device is electrically isolated by the LAO graphene oxide. The observation of wrinkles in some of the GIS devices, as those shown in Fig. 6.15b, indirectly demonstrates that graphene was successfully transferred to the HfO_2/SiO_2 stack. The electrical characteristics of GIS and MIS devices have been obtained from CAFM and standard characterization techniques, respectively.

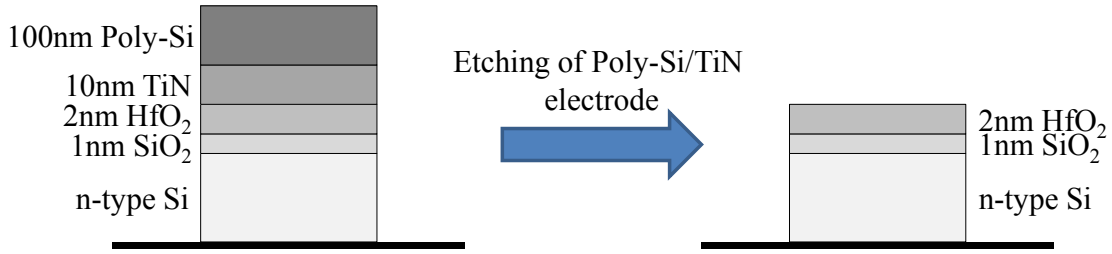

Figure 6.14. Schematic of the etching process to remove the Poly-Si/TiN electrode.

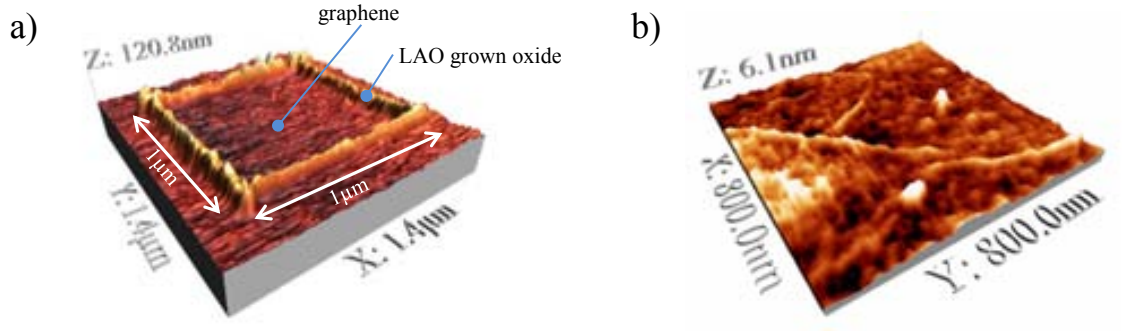

Figure 6.15. (a) Topographic AFM image of an area containing the GIS structure after being patterned by local anodic oxidation using the CAFM tip. The active area of the GIS device is outlined by the LAO-grown Graphene oxide. (b) Topographic scan inside a GIS structure that shows the typical wrinkles of Graphene/HfO_2 substrates.

6.3.2 Variability

The variability of the electrical properties of MIS and GIS structures was analyzed from the I-V curves obtained after applying Ramped Voltage Stresses (RVS) on different devices. Fig. 6.16a and b show, respectively, some examples of representative J-V curves obtained on different MIS and GIS capacitors. Squares correspond to J-V curves measured on fresh devices, while circles are measured once breakdown is triggered. In the MIS structures, the J-V curves were obtained at device level and in the GIS capacitors, with CAFM. Note that in the case of GIS structures, since the measurements have been performed with CAFM, the contact area and, therefore, the mean free path of carriers on graphene should be estimated. However, in this topic there is some controversy and moreover, the mean free path can depend on many factors, among them the substrate properties [Giannazzo 11]. Taking into account the results reported, the mean free path of the carriers in graphene sheets over dielectrics ranges from 100nm on SiO_2 to 200nm on SiC, the measured CAFM I-V curves correspond to the current flowing through an area of $10^5 nm^2$. Therefore, to compare the electrical properties of both structures, J-V curves should be taken into account (Fig. 6.16a and b). Comparing both figures, we can conclude that the intrinsic variability of devices is larger on GIS structures, which could be related to defects/imperfections and/or grain boundaries formed on the graphene layer (Fig. 6.15b), also described in section 6.1 and 6.2. Such imperfections may prohibit adhesion of graphene on a substrate or alter its electrical properties, being especially harmful in large area devices [Zhang 11]. More specifically, as shown in previous sections, they can degrade the electronic structure, transport, and mobility of graphene [Myer 07], and as uncontrollable and unavoidable defects, they increase the device-to-device variability (also observed in section 6.2.4).

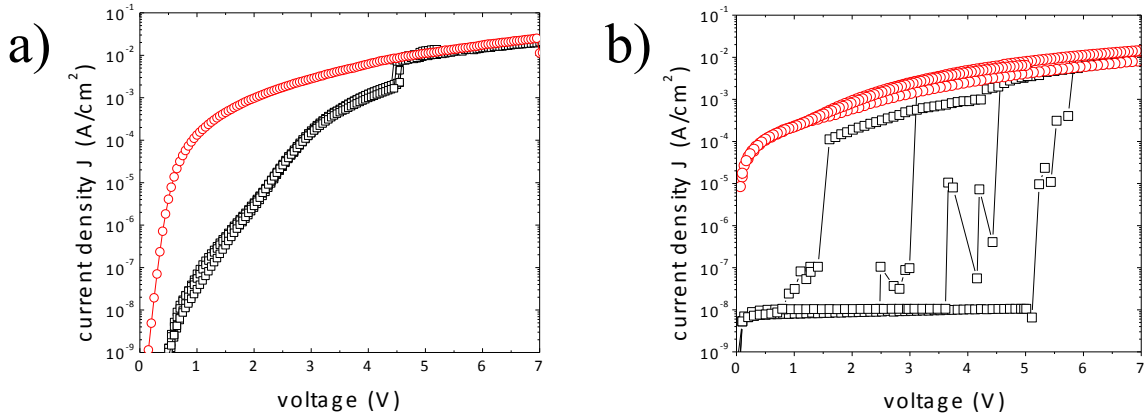

Figure 6.16. (a) J-V curves for different TiN/HfO_2/SiO_2/Si capacitors. (b) shows some J-V curves collected with CAFM on different Graphene/HfO_2/SiO_2/Si structures.

6.3.3 Reliability

The dielectric BD of MIS and GIS structures was studied from the measurement of topographical (Fig. 6.17a and c) and current (Fig. 6.17b and d) maps after applying a RVS in the center of the image. Fig. 6.17a and b correspond to a MIS device and Fig. 6.17c and d to a GIS structure. In the case of the MIS structure, the top electrode was previously removed, so that the CAFM tip played the role of the metal electrode. Note that the current image measured on the MIS structure (Fig. 6.17b) clearly shows that the material is highly damaged at the BD location: higher currents were measured at this site. In the topographical image, the BD site correlates to a hillock ~31nm tall. On the contrary, when the BD is induced on a GIS structure, a different behavior is observed. In the current map of the GIS structure (Fig. 6.17d), for example, the BD spot cannot be distinguished. However, the current images obtained on the GIS and MIS structures are not comparable, because of the size of the metal electrode. Due to the mean free path of charge carriers in the GIS structure (~200nm), the current through an area of $10^5 nm^2$ is registered by the tip while in MIS devices only ~$100nm^2$ areas are studied.

Regarding the topographical image, note that despite the typical wrinkles and folds that can be measured on graphene layers, no surface modification is observed in GIS structures after BD (Fig. 6.17c). A similar result is observed when using graphene coated tips as top electrode on high-k-based gate stacks. Pt-Ir and graphene-coated tips (those described in chapter 5) have been used to induce a BD spot by the application of a RVS at a fixed location of an HfO_2/SiO_2 gate stack. After BD, the influence of the tip varnish and, therefore, the material of the electrode (in this case the CAFM tip) is analyzed from the measurement of topographical maps on the BD sites. Fig. 6.18a and b show the typical topographic maps collected at two regions where the BD was previously induced at the center of each image using Pt-Ir and graphene-coated tips, respectively. As the images show, remarkable differences can be observed at the location where the BD event was induced and, therefore, at the location where high current densities were injected. For Pt-Ir tips (Fig. 6.18a) the BD site correlates to a huge hillock of up to 31.2 nm tall. On the contrary, when the BD of the HfO_2/SiO_2 stack is induced using graphene-coated tips, no surface modification is observed at the conductive path, but it just follows the flat pattern of unstressed locations.

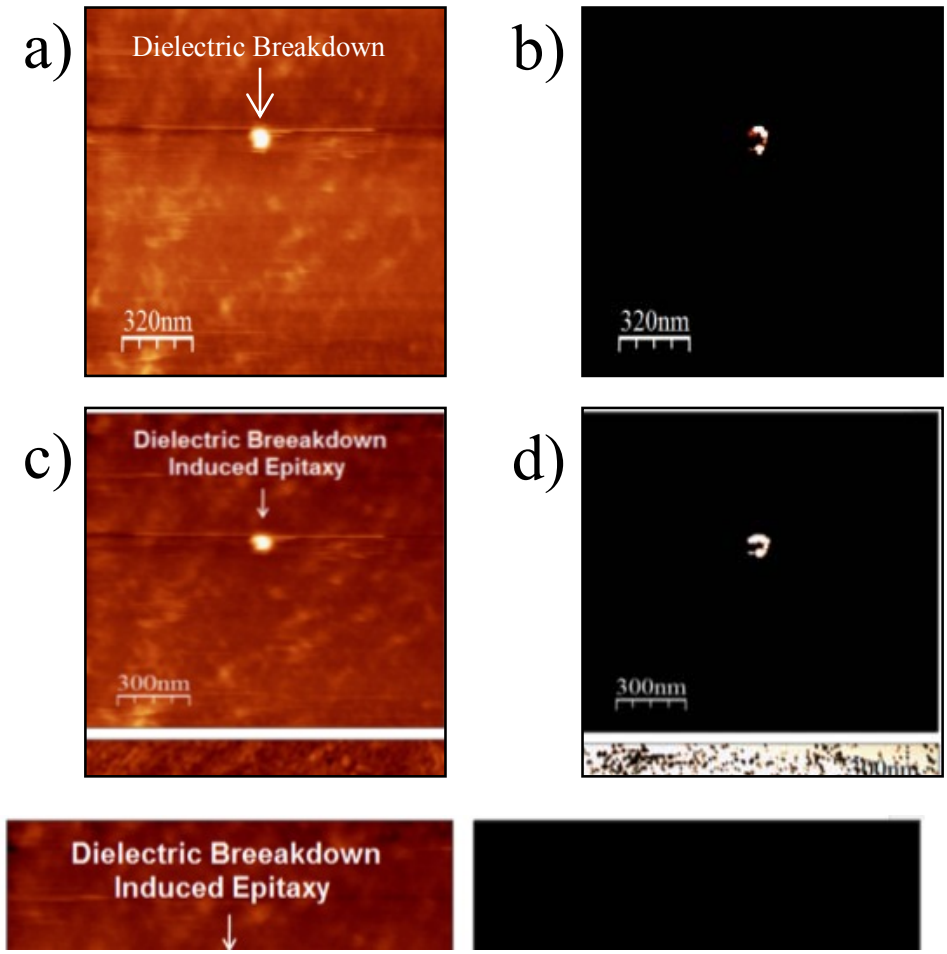

Figure 6.17. Topographic (a) and current (b) maps measured on the MIS samples, where a Ramped Voltage with a current limitation of 10 μA was previously applied in the center of the image until BD took place. Topographic (c) and current (d) maps measured on one of the graphene-based capacitors (as that shown in Figure 6.15a) after applying a similar Ramped Voltage with CAFM tip until BD.

The observation of morphological changes at the BD site, which is related to the violence of the uncontrolled BD event in the insulating samples [Porti 07], has been previously observed by other research groups, and has been mainly related to three phenomena. The first is the so-called Dielectric Breakdown Induced Epitaxy (DBIE) [Pey 05], which is related to microstructural damage triggered by BD-induced thermo-chemical reactions in the oxide. Secondly, it has also been demonstrated that the presence of the hillock at the BD site could be related to artifacts of the measurement technique due to a high concentration of charges at the conductive path during BD [Porti 02]. Finally, the observed hillock could also be related to atoms coming from the metallic electrode, which could be melted due to thermal effects [Porti 04]. Note that the last case is especially harmful when inducing the BD with the CAFM tip [Porti 07] due to the unstable nature of the CAFM tip metallic varnish. Platinum and Iridium atoms from the tip can break their bonds and penetrate in the analyzed HfO_2 layer.

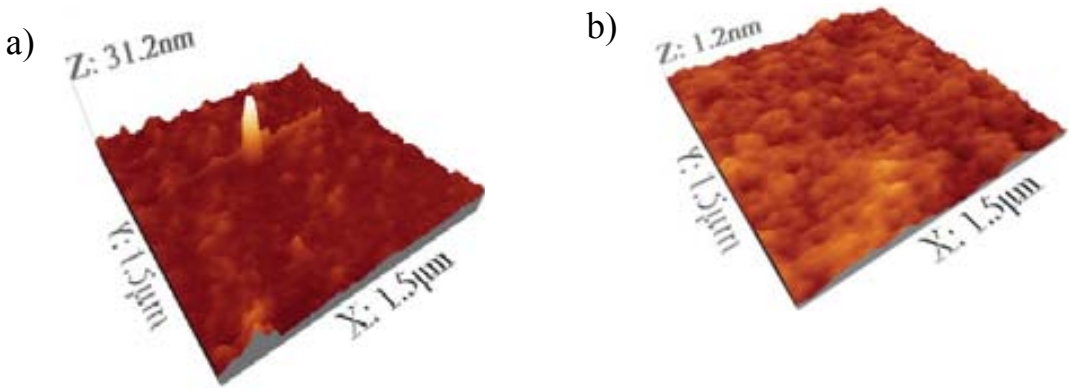

Figure 6.18. Typical topographic maps recorded after inducing the dielectric breakdown (BD) on HfO_2/SiO_2 gate stacks at the center of the scanned area using (a) Pt-Ir and (b) graphene-coated tips. Graphene-coated tips effectively minimize the interaction between the tip and sample.

Since this phenomenon is not observed when the top electrode is a GSL deposited on the high-k dielectric or a graphene-coated tip, these results demonstrate that graphene-coated tips or structures with graphene as electrode avoid any tip-sample interaction during the BD event. That suggests that the graphene somehow protects the sample from being completely destroyed during BD, preventing DBIE or the accumulation of charges, or avoids the tip varnish destruction and the consequent sample contamination. The final result is that when graphene is used as electrode, the gate stack is much more stable, which avoid false imaging of the sample.

To conclude this section, the electrical properties of GIS structures have been compared to MIS devices with the same gate stack. The time-zero variability of graphene-based devices is still far from that of the well-known MIS structures probably due to graphene imperfections such as wrinkles and other effects. Therefore, further studies to improve the quality of graphene-insulating interfaces should be performed. However, our measurements indicate that graphene electrodes avoid catastrophic BD of HfO_2/SiO_2insulator stacks, probably due to the higher stability of graphene, which prevents larger microstructural damage.

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Conclusions

The progressive scaling down of CMOS technologies has improved the performance of integrated circuits. Besides the reduction of the MOSFET dimensions, the introduction of strain engineering since the 90nm node, to increase the channel mobility, and the high-k/metal gate stack since the 45nm node, to reduce the gate leakage and power consumption, have been just some of the solutions proposed by the semiconductor industry for the scaling during the last years. However, to sustain current scaling in the future, other technological solutions are expected, such as the use of high-mobility materials or the introductions of 3D device architectures as FinFETs, etc. The use of graphene as a channel replacement material for graphene based FETs is also a promising alternative. However, so far, since its investigation is in a very premature phase, many aspects with respect to their integration into already established device technology still are to be investigated. Whatever the materials and technology considered, submicron technologies suffer from several problems, being some of the most important new variability and reliability effects. Intrinsic process variability has an unpredictable effect in the device performance and is ultimately associated with the discrete nature of matter and charge. On the other hand, the progressive degradation of the MOSFET electrical characteristics due to aging mechanisms affecting the gate oxide, such as Dielectric Breakdown (BD), Bias Temperature Instabilities (BTI) and Channel Hot Carrriers (CHC), can also affect the performance of integrated circuits.

This thesis is a contribution in the field of the electrical properties, variability and reliability of MOS devices and graphene as material for nanoelectronics. Since standard characterization techniques are blind to the sources of variability and failure mechanisms because they take place at the nanoscale, techniques with a large lateral resolution are required to investigate these phenomena in detail. A set of techniques that provide such an elevated and necessary spatial resolution is the Atomic Force Microscope (AFM), making possible the investigation of such effects at the nanoscale. In this thesis, AFM related techniques have been used to investigate the variability and reliability of MOS devices based on SiON and high-k dielectrics. In particular, aging mechanisms (as BTI and CHC) and how fabrication processes like an annealing (which leads to the polycrystallization of high-k dielectrics) can affect the electrical properties of high-k based MOS devices, is studied. The influence of the precursor used to grow an HfO_2 layer was also analyzed. Finally, graphene was investigated in several senses: On one hand, as conductive layer for commercially available CAFM probes and, on the other, as conductive channel in GFETs or electrode in GIS structures.

CAFM and standard wafer level characterization techniques have been combined to investigate how the polycrystalline microstructure (after a thermal annealing) and the thickness of HfO_2 based MOS capacitors influence the nanoscale morphological and electrical properties of fresh (before any electrical stress) and stressed gate stacks and how such nanoscale properties affect the reliability and variability of the device level electrical characteristics of fully processed MOS devices.

- Larger topographical inhomogeneities were detected in dielectrics with higher thickness and polycrystalline microstructure. A granular structure was observed after polycrystallization, related to the presence of grains surrounded by grain boundaries (GBs). The average grain size and roughness of the HfO_2 layer

depends on the thickness, being larger on thick layers, which can be related to dependence of the crystallization temperature on that parameter.

- The impact of thickness and polycrystallization of the HfO_2 on the nanoscale electrical properties of the gate stack was analyzed from CAFM and KPFM maps. Polycrystalline samples show larger leaky sites, associated to GBs, provoking a larger electrical inhomogeneity. A larger inhomogeneity was also observed when polycrystalline structures were analyzed with KPFM.

- From these results we can conclude that polycrystalline microstructure of the high-k layer and, to a lesser degree, its thickness, is an important source of variability of its electrical properties at the nanoscale. In the case of the polycrystalline dielectrics, the variability could be attributed to the different electrical properties of nanocrystals and grain boundaries. Nanocrystals are more insulating whereas the grain boundaries show a larger conductivity. The increase of the conductivity at GBs could be related to an excess of some kind of defects or trapping sites generated around the grain boundaries, such as oxygen vacancies, which could enhance the non-homogeneity observed in current images.

- The impact of such nanoscale variability sources on the device level characteristics of MOS capacitors was also studied. The results suggest that these nanoscale variability sources greatly affect the device level characteristics. In capacitors with amorphous dielectrics, a very small dispersion in the gate current is observed, which slightly increase in thicker oxides. However, in polycrystalline devices, the gate conduction is larger, with a very erratic and unstable behavior, attributed to the different electrical properties of nanocrystals and GBs.

- From Weibull plots, smaller breakdown electric fields and larger dispersions were observed in the polycrystalline structures, that is, on the devices in which variability at the nanoscale was larger. Therefore, these results demonstrate that nanoscale variability sources (as polycrystalline microstructure in particular) not only affect the variability of the electrical properties of non-stressed MOS devices, but also their reliability.

- The effect of an electrical stress on the nanoscale properties and device level variability of amorphous and polycrystalline based MOS devices was also analyzed. It has been observed that the larger the initial variability of the gate stacks properties, the larger the impact of an electrical stress on their nanoscale and device level electrical properties and reliability. In polycrystalline samples, this observation has been attributed to current through the grain boundaries, which are more conductive and electrically weaker due to presence of oxygen vacancies compared to grains (nanocrystals).

- As a consequence, the nanoscale electrical properties variations are translated to the device-level electrical characteristics of MOS devices, which can increase their variability and reduce their reliability.

HfO_2/SiO_2 gate stacks grown by ALD using different precursors as $HfCl_4/HfO_2$ (ALD sample) or (TEMAHf)-O_3 (Metal Organic ALD, MOALD sample) have been characterized and compared. The effect of an annealing process before or after the gate electrode deposition has also been taken into account. This analysis has been performed at device level using standard characterization techniques and at the nanoscale with CAFM.

- At device level, non-annealed MOALD samples show larger low field leakage currents, which suggests that the high-k layer is richer in defects when it is grown with organic precursors. At high fields, when the tunneling current is controlled by the SiO_2 layer, the electrical conduction and V_{BD} in ALD and MOALD samples are similar.

- When the annealing is done before the gate electrode deposition, typical post-BD behavior is observed in ALD structures. Moreover, the CAFM characterization shows that the nanoscale properties of the HfO_2 layer are more inhomogeneous independently of the precursor. In particular, voids are measured on the topography of the ALD structures, which could be the origin of the post-BD behavior observed at device level and the larger inhomogeneity measured at the nanoscale.

- When the annealing is performed after the gate electrode deposition, smoother surfaces are observed, which could explain, among other factors, the reduction of leakage current and the increase of V_{BD} observed in those samples (ALD and MOALD) compared to non-annealed ones.

- Therefore, the annealing seems to have beneficial effects only when it is carried out after the gate electrode deposition.

CAFM has also been used to investigate at the nanoscale the impact of a Negative Bias Temperature Instability (NBTI) and Channel-Hot-Carrier (CHC) stress on the gate electrical properties of SiON based MOSFETs. The high lateral resolution of the microscope has allowed investigating the degradation induced along the channel. In particular, the main results are:

- When comparing non-stressed with NBTI and CHC stressed MOSFETs, the results show that after the stress a larger number of leaky sites and larger currents (suggesting a larger degradation) are measured along the channel.

- However, while after the NBTI stress the effect on the gate oxide is homogeneous, in the CHC stressed MOSFET regions close to the source and drain show a larger degradation than the center of the channel, which is indicative of the non-uniformity of the CHC stress.

- TCAD simulations of the magnitudes involved in the CHC stress (oxide voltage drop and impact ionization) suggest that the generated defects close to source and drain can be attributed to NBTI and to CHC degradation, respectively. However, although the aging mechanisms are different, from the gate oxide conductivity point of view, the created defects are not significantly different and lead to similar effects.

Due to the excellent mechanical and electrical properties of graphene, two applications of this material have also been studied in detail. The first one, as coating material of conductive AFM tips to improve their performance. Secondly, as conductive channel or top electrode in Graphene-based transistors or capacitors. As coating layer for CAFM tips:

- A method to transfer graphene single layers (GSL) grown on Cu substrates on commercially available AFM tips was developed and used to fabricate graphene-coated AFM tips for conductive measurements in contact mode. The graphene based tips have shown very similar morphological characteristics compared to commercially available conductive ones.

- A comparison of commercial Pt-Ir coated tips with those coated with graphene shows that the graphene-based tips provide a significant improvement of their intrinsic mechanical and electrical properties when measuring conductive and non-conductive surfaces. In particular, the properties of graphene in combination with a conductive AFM tip can lead to a substantial improvement in terms of durability and wear resistance, while preserving its conductive properties.

CVD grown graphene for nanoelectronic applications was also investigated. When used as conductive channel, the presence of grain boundaries and/or corrugations and wrinkles coming from the metallic substrate can alter the transport properties of graphene, leading to device-to-device variability. This issue has been investigated in detail with nanoscale techniques as CAFM and SEM. The main conclusions are the following:

- It has been demonstrated that substrate induced corrugations and strain-related wrinkles present in CVD-grown graphene on copper, which are harmful in device fabrication, can be effectively reduced by optimizing the transfer process and adequately tuning the morphology of the substrate, respectively. The results indicate that, while the compressive strain in graphene on flat substrates is minimized by creating wrinkles, on rough substrates, it is minimized by improving the graphene-substrate adhesion. Those experimental observations are further supported by damped dynamic simulations.

- When graphene is exposed to oxidative environments (such as the ambient air), the substrate underneath can be affected due to the presence of grain boundaries on the graphene layer. The material below the graphene domain boundaries can oxidize just by keeping the samples in air atmospheres for sufficiently long periods of time.

- Such oxidation leads to insulating hillocks which preferably grow along the graphene domain boundaries until reaching saturation. Such local oxidation considerably impoverishes the graphene properties, increasing its roughness and reducing its conductivity and mechanical resistance, and affects the performance of GFETs by reducing their conductivity and decreasing their reliability.

- The electrical properties of graphene-insulator-semiconductor (GIS) structures have been compared to MIS devices with equal gate dielectrics. The time-zero

variability of graphene-based devices reveals to be still far from that of the MIS structures probably due to imperfections in graphene morphology such as wrinkles and other effects. However, our measurements indicate that graphene electrodes avoid catastrophic BD of the HfO_2/SiO_2 insulator, most likely due to the intrinsic stability of graphene, which prevents larger microstructural damage.

So, to conclude, this thesis has shown that CAFM is an appropriate tool to investigate many topics related to nanoelectronics, as reliability and nanoscale variability sources of MOSFETs, giving a more detailed insight into how they affect the global device behavior. Moreover, it has also been used to study the nanoscale morphological and electrical properties of graphene layers for nanoelectronic applications, being able to detect imperfections that can affect the performance of devices based on graphene.

Compendium of publications included in this thesis

Publications 1-4

and other publications included in this thesis

Publications 5-7