Thesis submitted to the Universitat Politècnica de Catalunya
for the Degree of Doctor of Philosophy, November 2011.

MODULATION STRATEGIES FOR THE NEUTRAL-POINT-CLAMPED CONVERTER AND CONTROL OF A WIND TURBINE SYSTEM

by

Jordi Zaragoza i Bertomeu

Supervised by

Dr. Josep Pou i Fèlix

**UNIVERSITAT POLITÈCNICA
DE CATALUNYA**
Departament d'Enginyeria Electrònica

ACTA DE QUALIFICACIÓ DE LA TESI DOCTORAL

Reunit el tribunal integrat pels sota signants per jutjar la tesi doctoral:

Títol de la tesi: MODULATION STRATEGIES FOR THE NEUTRAL-POINT-
CLAMPED CONVERTER AND CONTROL OF A WIND TURBINE
SYSTEM

Autor de la tesi: Jordi Zaragoza i Bertomeu

Acorda atorgar la qualificació de:

- ☐ No apte
- ☐ Aprovat
- ☐ Notable
- ☐ Excel·lent
- ☐ Excel·lent Cum Laude

Terrassa, …………… de/d'…..............…….. de ....….

El President   El Secretari   El vocal

....
(nom i cognoms)   (nom i cognoms)   (nom i cognoms)

Als meu pares,

que ho són tot per mi i

que tant suport i afecte m'han donat.

A Natàlia,

per estar sempre al meu costat

i compartir la seva vida amb mi.

ACKNOWLEDGMENTS

First of all, I would like to thank my supervisor, Dr. Josep Pou, for his guidance, support in this work and for always demanding the best from me. His friendship and dedication have made the realization of this thesis possible. During the development of this work, we spent several years researching together. His knowledge, humility and work have instilled in me great admiration.

I would like to thank Dr. Salvador Ceballos (Salva, to his friends) for the good and fun times we spent together researching. His support and collaboration made several results in this thesis possible. I hope to return the favor someday.

I would like to thank Dr. Pedro Ibáñez for giving me the opportunity to stay at the Energy Unit of the Robotiker-Tecnalia research center. My research in Robotiker was a pleasant experience thanks to the staff. They helped me integrate myself and enjoy the experience during my stay. For this reason I would like to thank all my colleagues in Robotiker. I would especially like to thank Dr. Eider Robles for the moments that we shared inside and outside the technological center.

I would also like to thank Dr. Cyril Spiteri for giving me the opportunity to stay at the Industrial Electrical Power Conversion Department in the Faculty of Engineering at the University of Malta. I am grateful for his guidance during my stay.

I would like to thank all my colleagues from the Technical University of Catalonia, especially those in the Department of Electronic Engineering in Terrassa, for sharing so many coffees and meals during these years. Particularly, I would like to thank my friends Juan and Nestor for all the joyful moments we shared and adversities we overcame. I am especially grateful to Dr. Antoni Arias for his technical advice and suggestions.

Finally, I would like to dedicate this dissertation to my parents Salvador and Teresa, my brother Juan Salvador, my grandparents and the rest of my family for their support and love. I would also like dedicate this dissertation to my love Natàlia for sharing her life with me.

MODULATION STRATEGIES FOR THE NEUTRAL-POINT-CLAMPED CONVERTER AND CONTROL OF A WIND TURBINE SYSTEM

RESUM

Els convertidors multinivell són topologies de convertidors d'electrònica de potència que poden generar tres o més nivells de voltatge en cadascuna de les fases de sortida. Com a resultat, els voltatges i corrents generats per aquestes topologies presenten una distorsió harmònica baixa. Hi ha diferents configuracions de convertidors multinivell, les quals es basen en connectar dispositius de potència o convertidors en sèrie. El resultat d'aquestes connexions permet obtenir voltatges alts, tant en la part de corrent continu com en la de corrent altern del convertidor. A més, cada dispositiu sols ha de suportar una fracció del voltatge total del bus de corrent continu. Per aquestes raons, els convertidors multinivell són generalment utilitzats en aplicacions d'alta potència.

El convertidor de tres nivells amb connexió a punt neutre (*neutral-point-clamped*) és el més utilitzat. La recerca d'aquesta tesis doctoral està focalitzada en aquesta topologia de convertidor, i el principal objectiu és l'aportació de noves tècniques de modulació. Aquestes tenen en compte diferents aspectes: la velocitat computacional dels algorismes, l'equilibrat de les tensions dels condensadors del bus de contínua, les pèrdues de commutació i les oscil·lacions de baixa freqüència en el punt neutre del convertidor.

Totes les estratègies de modulació proposades en aquesta tesis són modulacions d'amplada de polses basades en portadora. En la primera modulació que es presenta, s'injecta un senyal comú (seqüència zero) a totes les moduladores, que es basa en els patrons de la modulació vectorial que utilitza tres vectors dels més propers al de referència (*nearest-three-vector modulation*). S'estudien i es comparen els resultats d'aquesta modulació amb la seva homòloga, basada en

perspectiva vectorial. Una segona proposta és l'anomenada modulació d'amplada de polses de doble senyal (*double-signal pulse-width modulation*)*.* Aquesta modulació és capaç d'eliminar completament les oscil·lacions de voltatge en el punt neutre del convertidor. No obstant això, es produeix un increment de les pèrdues de commutació en els dispositius de potència i, a més, no hi ha un equilibrat natural de les tensions en els condensadors del bus. Una última estratègia de modulació, anomenada modulació híbrida (*hybrid pulse-width modulation*)*,* es basa en la combinació de la modulació sinusoïdal (*sinusoidal pulse-width modulation*) i la de doble senyal. Aquesta presenta una solució de compromís entre reduir les pèrdues de commutació, en detriment d'un augment de l'amplitud de les oscil·lacions de voltatge en el punt neutre.

Una segona part d'aquesta tesis es centra en les aplicacions a generació eòlica, ja que els convertidors multinivell estan començant a ser utilitzats en aquest camp. Això es produeix fonamentalment per l'augment continu de les dimensions de les turbines eòliques. En aquesta part de la recerca s'ha considerat la configuració de dos convertidors multinivell connectats a un mateix bus de contínua (*back-to-back*), tot i que els convertidors han estat estudiats independentment. Inicialment s'ha estudiat el convertidor que va connectat a la xarxa elèctrica i s'ha aplicat l'estratègia de control coneguda com a control orientat a tensió (*voltage-oriented control*). S'han utilitzat controladors estàndard (proporcional-integral), als quals s'ha afegit un control difús que supervisa i modifica els valors de les constants dels controladors. Aquest supervisor difús millora la dinàmica de la tensió del bus de contínua davant canvis de càrrega quan el convertidor treballa com a rectificador. Per una altra part, s'ha estudiat el control d'una turbina eòlica basada en un generador d'imants permanents. En aquest cas, s'ha aplicat l'estratègia de control coneguda com a control orientat a camp (*field-oriented control*). S'han avaluat i comparat els avantatges i inconvenients de diferents formes de sintonitzar els controladors.

MODULATION STRATEGIES FOR THE NEUTRAL-POINT-CLAMPED CONVERTER AND CONTROL OF A WIND TURBINE SYSTEM

ABSTRACT

Multilevel converters are power electronic topologies that can generate three or more voltage levels in each output phase. As a result, the voltage and current waveforms generated have lower total harmonic distortion. Multilevel topologies are based on connecting power devices or converters in a series. Consequently, high voltages can be handled on the dc and ac sides of the converter, while each device stands only a fraction of the total dc-link voltage. For these reasons multilevel converters are generally applied to high-power applications.

The three-level neutral-point-clamped converter is the most extensively used multilevel topology. This topology is the main focus of research in this dissertation. The main objective is to propose new modulation strategies that are able to meet a compromise solution while considering computational algorithm speed, voltage balance in the dc-link capacitors, switching losses and low frequency voltage oscillations at the neutral point.

All the modulation strategies proposed here are based on carrier-based pulse-width modulation. A new modulation strategy has been implemented using a proper zero-sequence signal injected into the modulation signals. The zero sequence is determined from a space-vector modulation standpoint, particularly the nearest-three-vector modulation strategy. The proposed carrier-based technique is compared with its space-vector modulation counterpart. It shows some advantages, such as easier implementation and reduced switching events; however, it still produces oscillations in the neutral-point voltage for some operating conditions. A new modulation strategy able to completely remove such voltage oscillations is also presented. It is called double-signal pulse-width modulation. The main drawback of this strategy is that it

increases the switching frequency of the power devices and has no natural capacitor voltage balance. Some balancing strategies are proposed in this dissertation for this specific modulation. Furthermore, a hybrid pulse-width modulation approach is presented which is able to combine sinusoidal pulse-width modulation with double-signal pulse-width modulation; this represents a compromise solution between switching losses and neutral-point voltage oscillation amplitudes.

The second part of this thesis is focused on wind generation applications. Multilevel converters are starting to be used in such a field nowadays, and are expected to be further applied in the near future as the sizes of wind turbines grow. Two back-to-back-connected power converters are considered in this application, although they are analyzed independently. First of all, the control of the grid-connected converter is studied. A voltage-oriented control is used with standard proportional-integral controllers. The originality of the method is that a fuzzy supervisor is designed and included in the structure; the fuzzy supervisor is able to modify the proportional-integral parameters online. It is shown how the control of the total dc-link voltage improves significantly under load changes when the converter is working as a rectifier. On the other hand, a control study is performed on the wind turbine side. The variable speed wind turbine is based on a permanent magnet synchronous generator. A field-oriented control strategy is applied. The controllers are evaluated and compared using different tuning strategies which highlight the advantages and drawbacks of each.

Contents

List of Figures

List of Tables

List of Abbreviations and Acronyms

A/D: analog-to-digital (converter)

ac: alternating current

AVG: average

CB: carrier-based

D/A: digital-to-analog (converter)

dc: direct current

DFIG: double-fed induction generation

DEE: Department of Electronic Engineering

DTC: direct torque control

DSPWM: double-signal pulsewidth modulation

DSP: digital signal processor

EMI: electromagnetic interference

EPE: European conference on Power Electronics and applications

FOC: field-oriented control

HPWM: hybrid pulse-width modulation

PLD: digital logic programmable

IDF: imposed damping factor

IEEE: Institute of Electrical and Electronics Engineers

IGBT: insulated gate bipolar transistor

LQR: linear quadratic regulator

max: maximum

min: minimum

NP: neutral point

NPC: neutral-point-clamped (converter)

NTV: nearest-three-vector (modulation)

PESC: Power Electronics Specialists Conference

PF: power factor

ph: phase

PD: proportional derivative

PI: proportional integral

PID: proportional integral derivative

PMSG: permanent-magnet synchronous generator

PWM: pulse-width modulation

RMS: root mean square

SHE: selective harmonic eleminatuion

SPWM: sinusoidal pulse-width modulation

SV: space vector

SVM: space-vector modulation

SV-PWM: space-vector pulse-width modulation

THD: total harmonic distortion

UPC: Universitat Politècnica de Catalunya

VA: volt-ampere

VAR: volt-ampere reactive

VOC: voltage oriented control

VSI: voltage-source inverter

WECS: wind energy conversion system

WT: wind turbine

WTHD: weighted total harmonic distortion

ZPC: zero-pole cancelation

Terminology

$\vec{a} = e^{j\frac{2\pi}{3}}$

B: rotational friction

C: capacitor

C_f: floating capacitor

C_p: power coefficient

d: duty cycles

D: control variable of the hybrid modulation that takes values within the interval [0, 1] (D=0 and D=1 means applying DSPWM and SPWM, respectively)

D_f: damping factor

d_x: duty cycle

e_a, e_b and e_c: grid phase voltages

e_d, e_q and e_o: dq transformed utility phase voltages

E_{RMS}: RMS line-to-line utility voltage

f: line frequency

f_m: modulation frequency

f_s: sample frequency or switching frequency

$\bar{i}_0$: locally-average NP current

i_a, i_b and i_c: phase currents in the dc side of a converter

i_{ao}, i_{bo} and i_{co}: zero sequence of currents

i_{Cx}: current thought a capacitor

i_d, i_q and i_o: dq transformed phase currents

$Im(\vec{x})$: imaginary part of $\vec{x}$

$\mathbf{i}_{ph} = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^{\mathsf{T}}$

$\mathbf{i}_{LL} = \begin{bmatrix} i_{ab} & i_{bc} & i_{ca} \end{bmatrix}^{\mathsf{T}} = \begin{bmatrix} i_a - i_b & i_b - i_c & i_c - i_a \end{bmatrix}^{\mathsf{T}}$

$\bar{i}_{0min}$: minimum local-averaged NP current

$\bar{i}_{0avg}$: average NP current over a line period

$\hat{I}$: current amplitude (fundamental)

I_{RMS}: RMS value of the phase currents of the converter (fundamentals)

J: rotational inertia

L: inductance

m: modulation index for the SVM (under linear modulation mode $0 \le m \le 1$)

$m_a = \hat{V}_m / \hat{V}_{carrier}$: modulation index for SPWM

$m_a = \dfrac{2}{\sqrt{3}} m$; relationship between modulation indices

(m_1, m_2) : normalized components of the equivalent reference vector in the first sector (given in the non-orthogonal limiting axes of this sector).

$$m_{12} = 2 - m_1 - m_2$$

$\vec{m}$: reference vector

$m_f = \dfrac{f_s}{f_m}$; frequency-modulation ratio

$\vec{m}_n$: normalized reference vector

$m_n = \dfrac{\sqrt{3}}{2}(n-1)\,m$; amplitude of the normalized reference vector

n: number of available voltage levels in each leg of a multilevel converter. This number typifies an n-level converter

p_{ac}: instantaneous power at the ac side

p_{dc}: instantaneous power at the dc side

p: pole pairs

P_m: mechanical power

$\vec{p}_x$: vector projection

R: electrical resistance

R_b: blade radius

$Re(\vec{x})$: real part of $\vec{x}$

R_s : stator resistance

s_{ij}: switch control variable, $s_{ij} \in \{0, 1\} = \begin{cases} 1 & \textit{the switch is ON, and} \\ 0 & \textit{the switch is OFF;} \end{cases}$ where $i=\{a,b,c\}$ is the output phases, and $j=\{1,0,-1\}$ is the dc-link level

t: time

T: line period

$t_B = \dfrac{2C\Delta V_C}{\alpha\,I_{RMS}}$ where $\alpha = \dfrac{I_{NP_{AVG}}}{I_{RMS}}$; capacitor voltage balancing time for DSPWM

T_s: sampling period

T_m: mechanical torque

T_r: rise time

$\mathbf{T}_{dq}$: dq transformation or park transformation

v_a, v_b, and v_c: modulation signals

v_{ip} and v_{in}: positive and negative modulation signals. v_{ip} will only cross the upper carrier, and v_{in} will only cross the lower carrier

v_{a0}, v_{b0} and v_{c0}: output voltages of a multilevel converter refereed to the NP dc-link voltage

$\hat{V}_{carrier}$: carrier amplitude of the SPWM

v_{Cx}: voltage of a dc-link capacitor ($x=\{1, 2, 3, \ldots, n\text{-}1\}$)

v_{dc}: dc-link voltage regulated by a controller

v_{dc}^{*}: dc-link voltage control reference

V_{dc}: dc-link voltage provided by a voltage source

v_{c1}: voltage in the lower dc-link capacitor

v_{c2}: voltage in the upper dc-link capacitor

v_{off}: common offset (or zero sequence) added to the three-phase modulation signals in carrier-based NTV modulation

v_{i_off}: offset applied to two modulation signals of phase i ($i = \{a, b, c\}$) in DSPWM

$v_{i\_off\_HPWM}$: offset applied to two modulation signals of phase i ($i = \{a, b, c\}$) to generate HPWM

v_{m}: modulation signal

$\hat{V}_{m}$: amplitude of the modulation signal for the SPWM

v_{N0}: neutral voltage of a star-connected load refereed to the NP dc-link level

$\vec{V}_{REF}$: reference vector

v_{wind}: wind speed

$v_{0} = \dfrac{\max(v_{a}, v_{b}, v_{c}) + \min(v_{a}, v_{b}, v_{c})}{2}$: common offset (or zero sequence) added to the three-phase modulation signals to achieve maximum modulation range (modified SPWM)

$\vec{x}$: generic vector

$\overline{x}$: local-averaged variable

$\tilde{x}$: small-signal variable

X^{*}: reference value

$\hat{X}$: amplitude of a sinusoidal variable

x_{op}: operation point value of a variable

X_{RMS}: RMS value of a periodic waveform

$x_{(k)}$: sampled variable at period k

$x_{(t)}$: time-dependent variable

x: state vector in the state-space representation

y: output vector in the state-space representation

α, β: orthogonal axes in a two-dimensional representation

$\Delta O_{NP} = \dfrac{v_{C1} - v_{C2}}{2}$; instantaneous oscillations around the NP

$\Delta v_C = v_C - \dfrac{V_{dc}}{n-1}$; voltage error in a dc-link capacitor

Δv_{NP} : low-frequency peak-to-peak NP voltage ripple

$\Delta v_{NPn} = \dfrac{\Delta v_{NP}}{I_{RMS}/fC}$; normalized low-frequency peak-to-peak NP-voltage ripple

θ : angle

θ_n : angle of the normalized reference vector (first sextant)

θ_o : initial angle

θ_r : rotating coordinated angle of the dq transformation

η : efficiency

$\omega = 2\pi f$; angular frequency

ω_e : electrical speed

ω_r : rotational speed

ρ: air density

Ψ: parameter for the position of the camping interval using HPWM

Ψ_m: magnetic flux

ε : error

Ω_{opt}: optimal speed

β: pitch angle

$\lambda = \dfrac{\Omega R_b}{v_{wind}}$; tip speed ratio

Chapter 1.

Introduction

T his chapter presents the context of this research work and makes an introduction of this thesis. There is a brief overview of multilevel converter topologies, modulation strategies, and applications are employed. The chapter also includes the main objectives of this thesis and presents the structure of this document.

1.1. Context of the Research

The present thesis has been developed in the Department of Electronic Engineering of the Universitat Politècnica de Catalunya (UPC), within the research group called Terrassa Industrial Electronic Group (TIEG). The main research interests of this group are power electronics, renewable energy, multilevel converters, motion control, power quality, and electromagnetic compatibility.

This research has been carried out with the collaboration of two other institutions; the Energy Unit of the Robotiker-Tecnalia research center, Basque Country, Spain; and the Industrial Electrical Power Conversion Department in the Faculty of Engineering at the University of Malta, Malta. Several research stays have been made in both institutions in order to share knowledge and develop some parts of this work.

This research is also part of the activities of three administration supported competitive projects:

-RECENER (ENE2004-07881-C03-03), entitled *Advanced power converter topologies to improve efficiency and power quality in the integration of wind energy in the electrical network*, funded by the Ministerio de Educación y Ciencia of Spain.

-CEBATE (ENE2007-67033-C03-01), entitled *Study of low-voltage energy converters for cost reduction and reliability improvement in wind energy systems*, funded by the Ministerio de Ciencia e Innovación of Spain.

-CONSOLIDER RUE (CD2009-00046), entitled Advanced wide band gap semiconductor devices for rational use of energy, funded by the Ministerio de Ciencia e Innovación of Spain.

1.2. Introduction of this Thesis

Multilevel converters are widely used in high-power applications. These topologies are based on connecting power devices or converters in series. Consequently, high voltages can be handled on the dc and ac sides of the converter, while each device stands only a fraction of the total dc-link voltage.

This thesis focuses on the neutral-point-clamped (NPC) converter (Baker May 13, 1980). Since its introduction in 1981 (Nabae et al. 1981), the NPC and other multilevel topologies have been widely studied. Some of these topologies are the floating or flying capacitor multilevel converter, which include some capacitors to provide the output voltages and to clamp the voltages of the switches. This topology has been of great interest since its introduction in the early 1990s (Meynard and Foch 1992a, b). Another multilevel topology is based on cascading H-bridge inverters. One of the earliest applications of this topology was for plasma stabilizations (Marchesoni et al. 1990); and later it was extended to three-phase applications (Fang Zheng et al. 1996).

Nowadays, the NPC topology is largely used in practical applications. One of the main concerns in this topology is how to keep the neutral point (NP) at one-half of the dc-link voltage. This is necessary to take full benefit of the converter.

Several modulation strategies can be used in multilevel converters. When dealing with a carrier-based modulation, the number of carriers needed is *n*-1, *n* being the number of levels that each phase of the converter can provide (Rodriguez et al. 2007). The standard carrier-based pulse-width modulation (PWM) is sinusoidal PWM (SPWM), in which the modulation signals are sinusoidal waveforms in the steady state. However, in multiphase systems, the modulation signals can be modified by the addition of a proper zero-sequence, which allows extending the range of the modulation index in the linear mode (Bowes and Yen-Shin 1997, van der Broeck et al. 1988). On the other hand, in three-phase systems, the most extended modulation technique is space-vector modulation (SVM), based on PWM (SV-PWM) (Ogasawara and Akagi 1991). These strategies can directly achieve large amplitudes of the output voltages in the linear operation mode, and low switching frequencies in power devices (Kaku et al. 1997). However, processing the algorithms used in SV-PWM may take a long time for its implementation. A summary of the main modulation strategies is shown in (Rodriguez et al. 2002).

In the NPC converter, the NP potential variation is analyzed in (Ogasawara and Akagi 1993) for ac motor drives and static volt-ampere reactive (VAR) compensators. In general terms, introducing a zero-sequence to the reference voltages can control

the NP voltage. In SPWM, this is equivalent to shifting up or down the phase signals of the modulator within a limited interval (Newton and Sumner 1997).

Although the NP voltage of the NPC converter can be generally controlled, a low-frequency voltage oscillation may appear at the NP under some operating conditions (Celanovic and Boroyevich 2000, Ogasawara and Akagi 1993, Pou et al. 2004, 2005a). Therefore, the power devices of the converter and the dc-link capacitors must be oversized in order to stand this voltage. Some recent modulation strategies are able to solve this problem (Busquets-Monge et al. 2004, Pou et al. 2005b). However, these modulation strategies increase the number of transistor switching events and, subsequently their switching losses. Furthermore, they do not naturally balance the voltages in the capacitors. Therefore, this thesis is focused on improving these voltage balancing issues.

Multilevel converters are especially interesting for high power applications. In this sense, the NPC topology is being used in wind energy conversion systems (WECS), since such systems have increased their rated power in recent years. For this reason, the NPC converter is becoming a preferred alternative to the standard two-level converter.

The back-to-back configuration of inverter topologies (Baroudi et al. 2007, Zhe et al. 2009) is used in variable-speed windmills. They require the use of ac-dc-ac converters to make the rotational speed of the blades independent of the utility frequency. Some advantages of this indirect connection are efficiency improvement, reduction of mechanical stresses, voltage control of the local grid, improvement in power quality, and better integration of wind energy into the electrical grid. Furthermore, in many European countries specific regulations make decisive the use of power electronics converters for the integration of wind energy to the grid.

Permanent-magnet synchronous generators (PMSG) are expected to be the standard generators in the future wind turbines. When designed as multipole machines, they may avoid the use of a gearbox and give rise to the so-called direct drive configurations. Unlike in the double-fed induction generator (DFIG), power electronic converters have to process 100% of the energy generated in a PMSG-

based system. Avoiding the use of a gearbox implies both an increase in system efficiency as well as fewer maintenance requirements. In addition, the PMSG configuration has more control over the currents injected into the electrical grid and thus over the reactive power. This is an important advantage for fulfilling grid-connection regulations.

Different control strategies can be implemented in an ac-dc-ac configuration for both the converter that drives the wind turbine and the grid-connected converter. Some standard control schemes are direct torque control (DTC) (Casadei et al. 2002, Zhong et al. 1999) and field-oriented control (FOC) (Casadei et al. 2002, Murray et al. 2008) in the case of the converter driving the wind turbine (WT). Similarly, the counterparts are direct power control (DPC) (Kazmierkowski and Malesani 1998) and voltage-oriented control (VOC) (Noguchi et al. 1998)] in the case of the grid-connected converter. In a WT system, the electrical and mechanical parts are mostly linear; however, the aerodynamics of the blades are highly nonlinear (the system behaves globally as a nonlinear system). Also, the dc-link voltage is defined by a nonlinear equation and therefore the controller of the grid-connected converter should be designed with this nonlinear feature in mind.

The use of linear or nonlinear controllers and a method to tune standard controllers such as proportional-integrative (PI) is performed in Chapter 6 and 7 of this thesis. The research focuses on using an NPC converter connected to the grid (Chapter 6) and on a converter driving the WT (Chapter 7).

1.3. Objectives

This thesis focuses on new modulation strategies and control techniques for the NPC converter. The primary objectives are to find new modulation strategies that improve the main problems with the NPC converter, such as: (1) removing the low-frequency voltage oscillation that appears at the NP under some operating conditions, (2) improving balancing dynamic of the voltages in the dc-link capacitors, and (3) finding a compromise solution between switching losses and NP voltage

oscillation amplitudes. Also this thesis is devoted to studying and developing control strategies for the NPC converter in wind turbine energy applications.

For these purposes, the following objectives are defined in this thesis:

- Analyze the current modulation strategies and propose new alternatives in order to improve the main drawbacks commented upon previously.

- Evaluate and compare standard modulation strategies with those proposed under some aspects: conduction and switching losses, harmonic distortion, low-frequency oscillations at the NP of the NPC converter, and the balancing dynamic of the dc-link capacitor voltages.

- Propose control techniques for a grid-connected NPC converter.

- Analyze and propose tuning strategies to improve the control of a converter driving a PMSG in a wind turbine application.

1.4. Structure of the Document

This document is composed of eight chapters and one appendix. The following summary indicates the main contents of each of them.

Chapter 2 starts with a revision of the main multilevel converter topologies. It also describes the NPC converter prototype used for the experimental results presented in this dissertation. Furthermore, it introduces some general modulation strategies used in both two-level and multilevel inverters. This helps in understanding the novel modulation strategies presented in the following chapters.

Chapter 3 describes and analyzes a CB-PWM strategy for the three-level NPC converter with a zero-sequence voltage injection. The proposed strategy explores and exploits the duality between the nearest-three-vector (NTV)-SVM strategy and the CB-PWM strategy with a zero-sequence voltage injection in order to (i) balance the voltage, (ii) reduce the switching frequency and consequently switching losses, and (iii) mitigate the voltage oscillations of the NP. A theoretical basis for the proposed CB-PWM strategy is developed based on the analysis of the NTV-SVM strategy.

Chapter 4 proposes another modulation strategy that overcomes the problem of low-frequency NP voltage oscillation in the NPC converter. This modulation strategy is characterized by the use of two modulation signals per phase, and it is the so-called double-signal PWM (DSPWM). One of the main drawbacks of this modulation strategy is that it does not provide natural voltage balancing; therefore, an optimal compensator is also presented in this chapter.

Chapter 5 proposes a hybrid modulation strategy (HPWM), based on the modulation strategy presented previously in Chapter 4. This new modulation combines the DSPWM with the SPWM in order to minimize the switching losses. The main characteristic of this HPWM is the reduction of the switching losses at the cost of some low-frequency voltage oscillations at the NP. Furthermore, a tracking method and an amplitude control of the NP voltage are also proposed in this chapter in order to achieve the maximum reduction of the voltage oscillation amplitudes in HPWM and to control the maximum amplitude of the NP voltage oscillations

Chapter 6 presents a grid–side VOC strategy. The controller proposed in this chapter is based on PI regulators, where a zero-pole cancelation strategy to tune the parameters of the PI is used. However, taking into account that the system is nonlinear, a fuzzy supervisor is proposed which takes care of adjusting the PI parameters during transitory processes. Therefore, the main objective is to improve the response of the NPC converter under load changes.

Chapter 7 focuses on the control of a variable-speed wind energy conversion system (WECS) based on a permanent-magnet synchronous generator (PMSG). Different control tuning strategies for FOC are studied and compared. The main goal is to know the best tuning strategy to achieve a better performance of the system.

Chapter 8 summarizes the conclusions of the thesis and the main contributions. In addition, a list of the publications and patents derived from this thesis is included. Finally, the chapter presents the lines for future research.

The appendices describe a mathematical switching model of the NPC converter; the characterization of the IGBTs used for the calculation of power losses in the NPC converter; the equations used to analyze harmonic distortion and to evaluate the NP

voltage ripple amplitudes of the NPC converter; and finally, the values used in the set-up of the wind system generator platform used in chapter 7.

1.5. Chapter References

Baker RH. May 13, 1980. High-voltage converter circuit in United States Patent, ed.

Baroudi JA, Dinavahi V, Knight AM. 2007. A review of power converter topologies for wind generators. Renewable Energy 32: 2369-2385.

Bowes SR, Yen-Shin L. 1997. The relationship between space-vector modulation and regular-sampled PWM. Industrial Electronics, IEEE Transactions on 44: 670-679.

Busquets-Monge S, Bordonau J, Boroyevich D, Somavilla S. 2004. The nearest three virtual space vector PWM - a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter. Power Electronics Letters, IEEE 2: 11-15.

Casadei D, Profumo F, Serra G, Tani A. 2002. FOC and DTC: two viable schemes for induction motors torque control. Power Electronics, IEEE Transactions on 17: 779-787.

Celanovic N, Boroyevich D. 2000. A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. Power Electronics, IEEE Transactions on 15: 242-249.

Fang Zheng P, Jih-Sheng L, McKeever JW, VanCoevering J. 1996. A multilevel voltage-source inverter with separate DC sources for static VAr generation. Industry Applications, IEEE Transactions on 32: 1130-1138.

Kaku B, Miyashita I, Sone S. 1997. Switching loss minimised space vector PWM method for IGBT three-level inverter. Electric Power Applications, IEE Proceedings - 144: 182-190.

Kazmierkowski MP, Malesani L. 1998. Current control techniques for three-phase voltage-source PWM converters: a survey. Industrial Electronics, IEEE Transactions on 45: 691-703.

Marchesoni M, Mazzucchelli M, Tenconi S. 1990. A nonconventional power converter for plasma stabilization. Power Electronics, IEEE Transactions on 5: 212-219.

Meynard TA, Foch H. 1992a. Multi-level conversion: high voltage choppers and voltage-source inverters. Pages 397-403 vol.391. Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE.

—. 1992b. Multi-level choppers for high voltage application. EPE Journal 2: 45-50.

Murray A, Palma M, Husain A. 2008. Performance Comparison of Permanent Magnet Synchronous Motors and Controlled Induction Motors in Washing Machine Applications Using Sensorless Field Oriented Control. Pages 1-6. Industry Applications Society Annual Meeting, 2008. IAS '08. IEEE.

Nabae A, Takahashi I, Akagi H. 1981. A New Neutral-Point-Clamped PWM Inverter. Industry Applications, IEEE Transactions on IA-17: 518-523.

Newton C, Sumner M. 1997. Neutral point control for multi-level inverters: theory, design and operational limitations. Pages 1336-1343 vol.1332. Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE.

Noguchi T, Tomiki H, Kondo S, Takahashi I. 1998. Direct power control of PWM converter without power-source voltage sensors. Industry Applications, IEEE Transactions on 34: 473-479.

Ogasawara S, Akagi K. 1991. A vector control system using a neutral-point-clamped voltage source PWM inverter. Pages 422-427 vol.421. Industry Applications Society Annual Meeting, 1991., Conference Record of the 1991 IEEE.

Ogasawara S, Akagi H. 1993. Analysis of variation of neutral point potential in neutral-point-clamped voltage source PWM inverters. Pages 965-970 vol.962. Industry Applications Society Annual Meeting, 1993., Conference Record of the 1993 IEEE.

Pou J, Pindado R, Boroyevich D, Rodriguez P. 2004. Limits of the neutral-point balance in back-to-back-connected three-level converters. Power Electronics, IEEE Transactions on 19: 722-731.

—. 2005a. Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter. Industrial Electronics, IEEE Transactions on 52: 1582-1588.

Pou J, Rodriguez P, Sala V, Busquets-Monge S, Boroyevich D. 2005b. Algorithm for the virtual vectors modulation in three-level inverters with a voltage-balance control loop. Pages 9 pp.-P.9. Power Electronics and Applications, 2005 European Conference on.

Rodriguez J, Jih-Sheng L, Fang Zheng P. 2002. Multilevel inverters: a survey of topologies, controls, and applications. Industrial Electronics, IEEE Transactions on 49: 724-738.

Rodriguez J, Bernet S, Bin W, Pontt JO, Kouro S. 2007. Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives. Industrial Electronics, IEEE Transactions on 54: 2930-2945.

van der Broeck HW, Skudelny HC, Stanke GV. 1988. Analysis and realization of a pulsewidth modulator based on voltage space vectors. Industry Applications, IEEE Transactions on 24: 142-150.

Zhe C, Guerrero JM, Blaabjerg F. 2009. A Review of the State of the Art of Power Electronics for Wind Turbines. Power Electronics, IEEE Transactions on 24: 1859-1875.

Zhong L, Rahman MF, Hu WY, Lim KW, Rahman MA. 1999. A direct torque controller for permanent magnet synchronous motor drives. Energy Conversion, IEEE Transactions on 14: 637-642.

Chapter 2.

Multilevel Topologies. Prototype Description and Modulation Techniques

This chapter introduces the main multilevel converter topologies. It also describes the prototype used for the experimental results presented in this dissertation, which is a part of a back-to-back-connected system.

The chapter begins with some general concepts of SVM and explains in detail how to calculate the duty cycles in the modulation process. Some traditional methods to help balance the voltage in the dc-link capacitors in a three-level NPC converter are also described. Some common modulation strategies are briefly described to help understand the new modulation strategies proposed in the following chapters.

2.1. Multilevel Converter Topologies

Nowadays, there is a growing interest in multilevel converter topologies since they can extend the application of power electronics systems to higher voltage and power ratios. Multilevel converters are the most attractive technology for the medium- to high-voltage range (2-13 kV), which includes motor drives, power distribution, power quality and power conditioning applications.

Multilevel converters can synthesize waveforms by using more than two voltage levels; hence, the quality of the spectra is significantly improved compared with the classic two-level topology.

The main drawbacks of the multilevel converters are that:

- these topologies require a high number of switches,

- their control is difficult due to the number of devices, and

- several dc voltage sources are required, which are usually provided by capacitors. Balancing the voltages of these capacitors according to an operating point is a difficult challenge.

Despite these drawbacks, multilevel converters have turned out to be a very good alternative for high-power applications, since the cost of controlling these cases is a small portion of the whole cost of the system. Furthermore, as the price of power semiconductors and DSPs continues to decrease, the use of multilevel topologies is expected to extend to low-power applications (those of less than 10 kW) as well. Fast power devices (CMOS transistors), which can operate at very high switching frequencies, can be used for low voltages. Therefore, the values of the reactive components will undergo significant reduction. Furthermore, new power devices are expected to appear in the coming years, and these may also extend the application of multilevel topologies.

So far, the most actively developed multilevel topologies are:

- the diode-clamped converter,

- the floating-capacitor converter, and

- the cascaded H-bridge converter.

Fig.2.1 shows an example of voltage waveform obtained from an n-level diode-clamped converter in the case of balanced voltages in the capacitors. The voltage levels shown in this figure are referenced to the lower dc-link voltage.
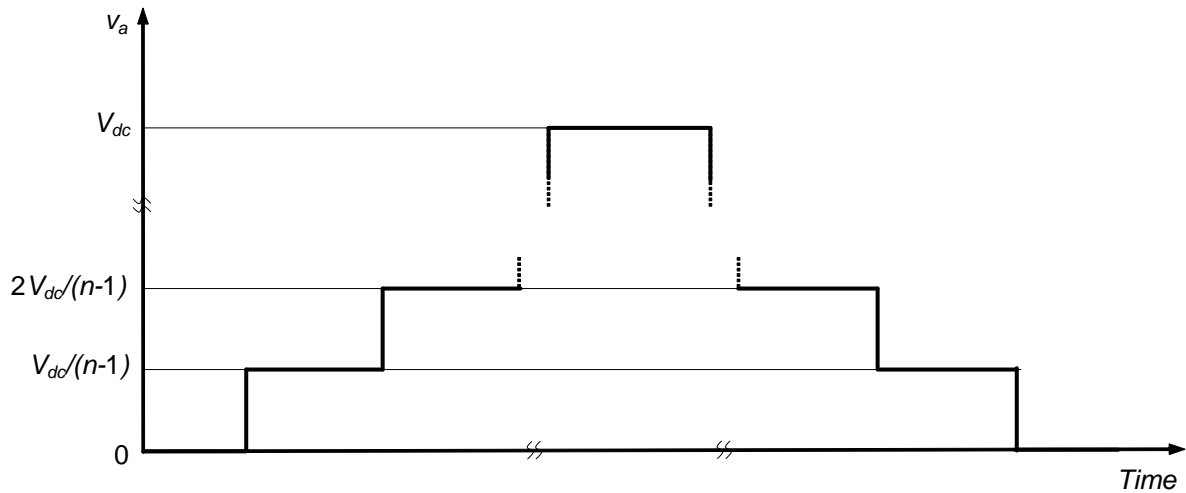
Fig.2.1. Example of voltage waveform generated by an n-level converter.

2.1.1. Diode-Clamped Converter

The three-phase diode-clamped converter is well known as a NPC converter. Since its introduction in 1981 by (Nabae et al. 1981), the NPC converter has been the most practical and widely studied multilevel topology (Fig.2.2).

In the NPC converter, the dc bus is divided into three levels by two series-connected capacitors. The middle point of both capacitors ("0" reference) can be defined as the NP. At any time that the two inner switches of a leg are turned on, the NP potential is transferred to the output of that phase by means of the clamping diodes. Additionally, the voltages of the two series-connected dc-link capacitors must be confined to one-half the level of the dc-link voltage to take full benefit of this converter.

Taking the NP potential (level "0") as a reference for the output voltages, and assuming balanced voltages in the dc-link capacitors $v_{C1}=v_{C2}=V_{dc}/2$, each of the phases can provide three voltage levels: $V_{dc}/2$, 0 and $-V_{dc}/2$. These output voltages are obtained by the switching states shown in Table 2.2, where the values "1" and "0"

indicate the ON and OFF switch states, respectively. There are other feasible states; however, since they are either useless or prohibited, they are not considered. All the possible states that this converter can take and some considerations are given in Appendix A.
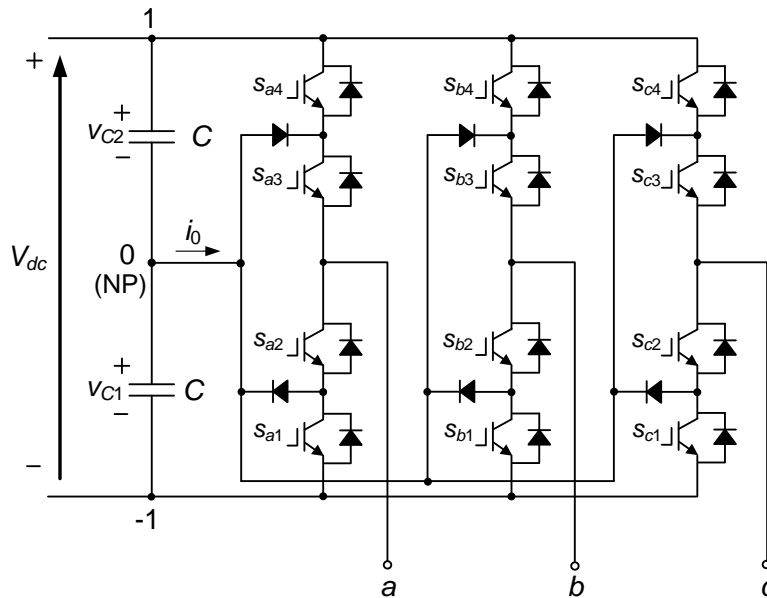
Fig.2.2.Three-level diode-clamped converter.

Table 2.1. Switching states of an NPC converter.

S_{a4}	S_{a3}	S_{a2}	S_{a1}	Output Voltage
ON	ON	OFF	OFF	$v_{a0} = V_{dc}/2$
OFF	ON	ON	OFF	$v_{a0} = 0$
OFF	OFF	ON	ON	$v_{a0} = -V_{dc}/2$

The topology has been extended to higher numbers of levels. Fig.2.3 shows a leg of the four- and five-level versions of this converter. In the general case, under balanced conditions, each capacitor has to withstand a voltage of $V_{dc}/(n-1)$, n being the number of converter levels. Consequently, the voltage stress in each power device is limited to a single capacitor voltage. Table 2.2 shows the switching states and the output phase voltages with reference to the NP ("0" level).
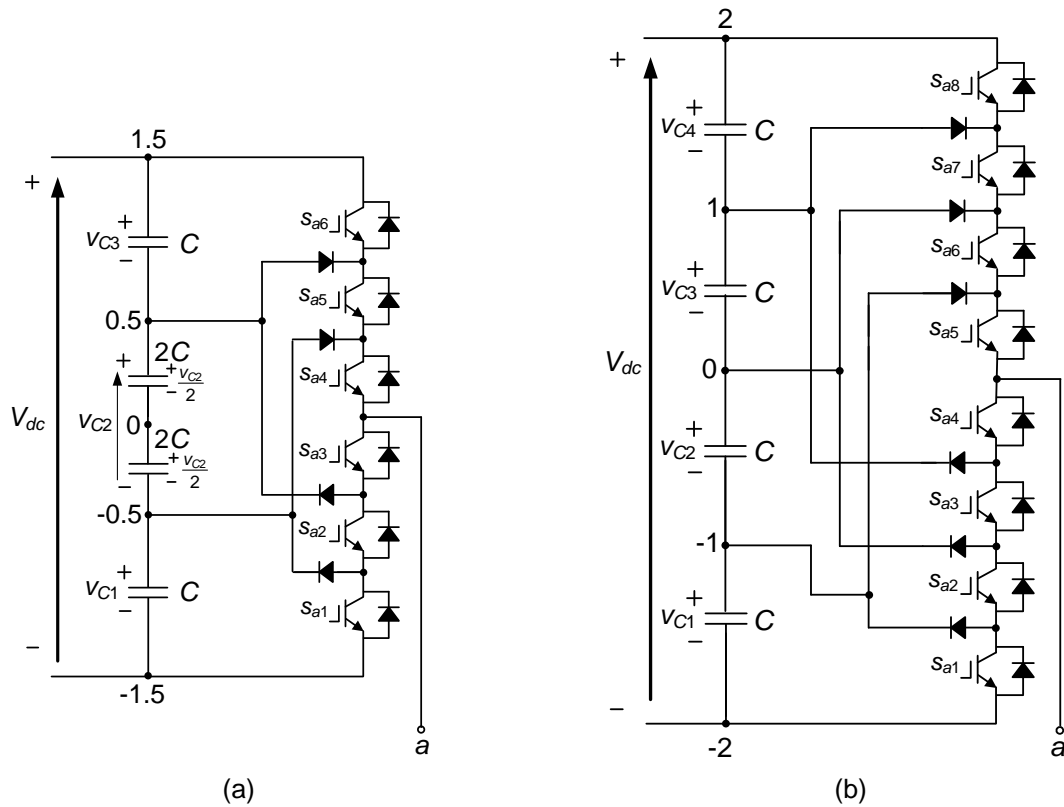
Fig.2.3. Diode-clamped multilevel converters (one phase leg): (a) four-, and (b) five-level topologies.

Table 2.2. Switching states and output voltages: (a) four-, and (b) five-level topologies.

S_{a6}	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	Phase voltage
ON	ON	ON	OFF	OFF	OFF	$v_{a0}=V_{dc}/2$
OFF	ON	ON	ON	OFF	OFF	$v_{a0}=V_{dc}/6$
OFF	OFF	ON	ON	ON	OFF	$v_{a0}=-V_{dc}/6$
OFF	OFF	OFF	ON	ON	ON	$v_{a0}=-V_{dc}/2$

(a)

S_{a8}	S_{a7}	S_{a6}	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	Phase voltage
ON	ON	ON	ON	OFF	OFF	OFF	OFF	$v_{a0}=V_{dc}/2$
OFF	ON	ON	ON	ON	OFF	OFF	OFF	$v_{a0}=V_{dc}/4$
OFF	OFF	ON	ON	ON	ON	OFF	OFF	$v_{a0}=0$
OFF	OFF	OFF	ON	ON	ON	ON	OFF	$v_{a0}=-V_{dc}/4$
OFF	OFF	OFF	OFF	ON	ON	ON	ON	$v_{a0}=-V_{dc}/2$

(b)

The advantages of the diode-clamped converter compared with other multilevel topologies are that:

- They use a low number of capacitors. Although these topologies require some additional clamping diodes, their low number of reactive components is usually preferred from the standpoint of cost.

- They can be connected to a single dc-link voltage. The floating-capacitor topology also shares this advantage, but the cascade converter does not, since this converter requires multiple isolated dc power supplies.

Nevertheless, some practical experience with this topology reveals technical difficulties that complicate its application, as follows:

- Overvoltage produced on semiconductor devices due to inductance elements that appear during transient states (Bum-Seok and Dong-Seok 1997, Xiaoming and Barbi 2000).

- Uneven time conduction sharing among the semiconductors.

- For topologies with more than three levels, the clamping diodes are subject to high voltage stress equal to $V_{dc}(n-2)/(n-1)$. As a result, a series connection of the diodes is required, where the number of diodes required for each phase will be $(n-1) \times (n-2)$. This issue complicates the design and raises reliability and cost concerns.

- The objective of maintaining the charge balance of the capacitors in topologies with a high number of levels (more than three) was demonstrated to be impossible for some operating conditions if standard modulation techniques are applied (Marchesoni and Tenca 2001, Pou J. et al. 2005a). These balancing problems appear when dealing with deep modulation indices and active currents. Therefore, high ac output voltages cannot be achieved, which inhibits the most important attribute of multilevel converters. Significant balancing improvements are obtained when two or more converters are connected to the same dc link. These converters are also used for static VAR compensation circuits in which no active power is transmitted and the balancing problem can be handled.

Although proper control of the three-level topology overcomes the voltage balance concern, a low-frequency ripple in the NP potential appears when dealing with large modulation indices and low power factors (PFs). The maximum voltage applied to the devices is higher due to this oscillation, and additionally, it produces low-frequency distortion in the ac output voltages. Nevertheless, the output distortion can be compensated for by using the feedforward modulation (Nikola Celanovic, Josep Pou).

In recent years, some modulation strategies have appeared that can completely remove the low-frequency NP voltage oscillations in the NPC converter (Busquets-Monge et al. 2004), (Pou J. et al. 2007). Additionally, (Busquets-Monge et al. 2008) demonstrated that charge balance in the capacitors can be achieved even for a converter with a number of levels greater than three. Nevertheless, all these strategies significantly increase the switching losses of the converter, generate lower quality output voltage spectra, and do not provide natural voltage balancing.

A solution to provide some voltage balancing control is presented in (Pou J. et al. 2007). Further contributions to that modulation technique are proposed in this dissertation.

2.1.2. Floating-Capacitor Converter

Meynard et al. in 1992 (Meynard and Foch 1992a, b) introduced the floating-capacitor converter. In this topology, voltage clamping is achieved by means of capacitors that "float" with respect to the ground potential ("0" reference). In Fig.2.4, the three and four-level versions of this converter are shown.

Each leg of these topologies can be seen as an imbricate cell, where the output voltage is synthesized by connecting a defined number of capacitors in series (Fig.2.5).

One out of each pair of switches s_{Hi} and s_{Li} must be in the on-state for a proper connection to exist between the dc-link potential and the output through some capacitors. Additionally, both switches cannot be ON at the same time or else short circuits will occur in the capacitors. Table 2.3 shows all the possible states of the

switches in three- and four-level converters (only the upper switches' states are given).

(a)

(b)
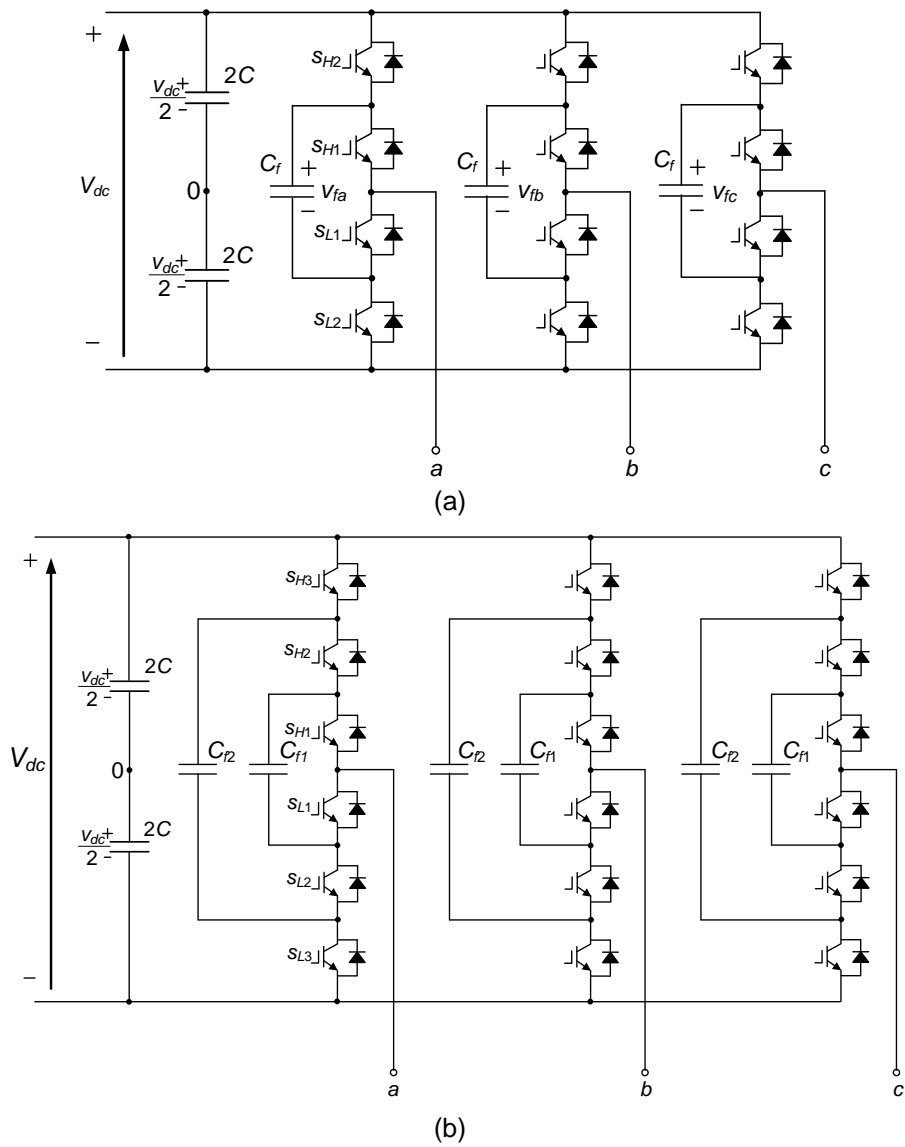
Fig.2.4. (a) Three-level and (b) four-level floating-capacitor converters.
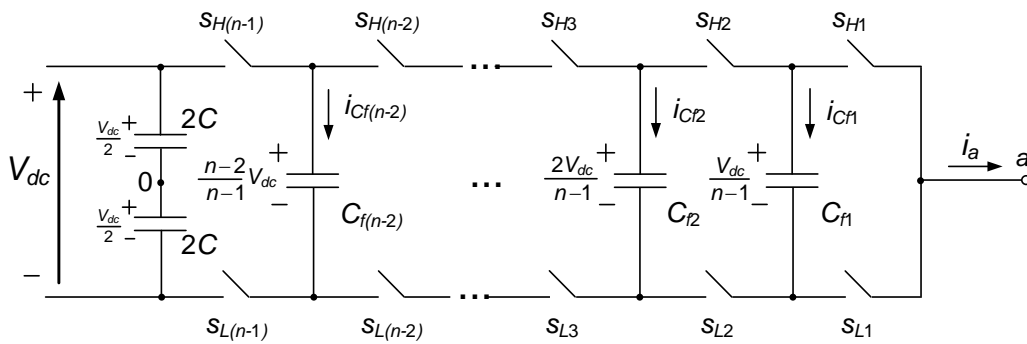
Fig.2.5. Imbricate cell, base of the floating-capacitor converter.

Table 2.3. Possible states of the switches in (a) the three-level, and (b) the four-level floating-capacitor converters.

s_{H2}	s_{H1}	v_{a0}	i_{Cf1}
OFF	OFF	$V_{dc}/2$	0
OFF	ON	0	$-i_a$
ON	OFF	0	i_a
ON	ON	$V_{dc}/2$	0

(a)

s_{H3}	s_{H2}	s_{H1}	v_{a0}	i_{Cf2}	i_{Cf1}
OFF	OFF	OFF	$-V_{dc}/2$	0	0
OFF	OFF	ON	$-V_{dc}/6$	0	$-i_a$
OFF	ON	OFF	$-V_{dc}/2$	$-i_a$	i_a
ON	OFF	OFF	$V_{dc}/6$	i_a	0
OFF	ON	ON	$-V_{dc}/6$	$-i_a$	0
ON	OFF	ON	$V_{dc}/2$	i_a	$-i_a$
ON	ON	OFF	$V_{dc}/6$	0	i_a
ON	ON	ON	$V_{dc}/2$	0	0

(b)

Different combinations of switch states define the same output voltage. This redundancy is enough to guarantee balanced voltages in the floating capacitors for any operation conditions using proper modulation. For example, in the case of the three-level converter, there are only two states that affect the voltage of the floating capacitor, and both provide the same output voltage ($V_{dc}/2$). However, the current through the capacitor flows in the opposite direction. Hence, by choosing the suitable state according to the direction of the output current, this voltage can always be controlled.

For the three-level converter, all of the eligible states between consecutive output voltage steps are adjacent. This statement is not valid for converters with higher numbers of levels that produce significantly increased switching frequencies. Fig.2.6 shows the transitions between two consecutive voltage levels in the four-level converter. Some of these transitions (dashed lines) force all of the switches of the leg to switch. Nevertheless, these critical transitions must be used to achieve full control of the voltages of the floating capacitors.

Some important conclusions related to the voltage balancing issue in the floating-capacitor converters are as follows:

- Each leg can be analyzed independently from the others. This is an important difference from the diode-clamped converter, in which the entire three-phase system must be considered for the balancing issue.

- These converters can control the voltages of the floating capacitors thanks to their redundancy of states. However, in converters with more than three levels, some transitions between two consecutive voltage levels produce high switching frequencies. If these transitions are avoided, the amplitude of the voltage ripple in the capacitors will increase, and it might not be controllable.

$v_{a0}=-V_{dc}/2$	$v_{a0}=-V_{dc}/6$	$v_{a0}=V_{dc}/6$	$v_{a0}=V_{dc}/2$

s_{H3}, s_{H2}, s_{H1}

OFF   OFF   OFF

OFF OFF ON

OFF ON OFF

ON OFF OFF

OFF ON ON

ON OFF ON

ON ON OFF

ON ON ON
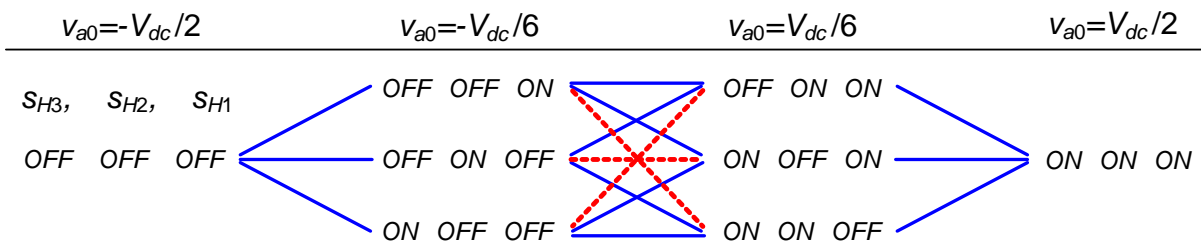
Fig.2.6. Transitions between consecutive voltage levels.

On the other hand, regarding Fig.2.4(b), the floating capacitor C_{f2} has a double voltage applied as compared with capacitor C_{f1}. Additionally, as the current level through all the floating capacitors is the same, they should have the same capacitance to produce similar amplitudes of their voltage ripple. Therefore, assuming series and parallel connections based on the same elementary component, capacitor C_{f2} requires four times the number of components required by C_{f1}. Provided that the voltage that each capacitor has to stand is $V_{dc}/(n-1)$, an n-level converter will require a total of $(n-1)\times(n-2)/2$ clamping capacitors per phase leg.

In conclusion, one of the major drawbacks of this topology is its high number of capacitors, not only those in the topology itself, but also those required for the series and parallel connections.

2.1.3. Cascaded H-bridge Converter

One of the earliest applications for the series connection of single-phase full-bridge inverter topology was its use for plasma stabilization in (Marchesoni et al. 1990). Later, this approach was extended to include three-phase systems.

The basic three-phase structure used in the cascade converter is shown in Fig.2.7.
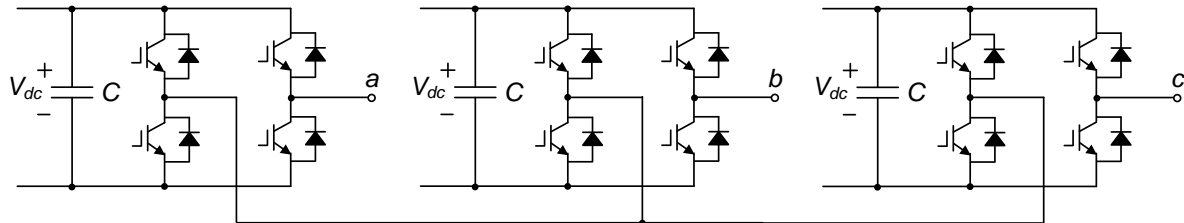
Fig.2.7. Three-level converter.

A chain of H-bridge topologies can perform as a converter with higher numbers of levels (Fig.2.8).
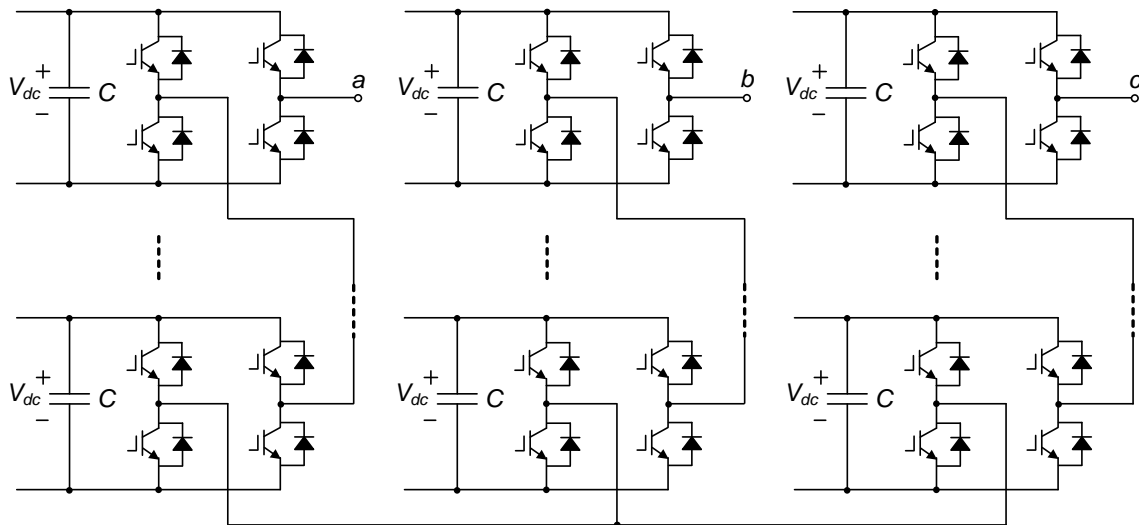
Fig.2.8. Multilevel cascade converter.

To achieve an even number of levels, a half-bridge topology must be added to the chain of H-bridge converters. Fig.2.9 shows the structure of a four-level converter.

The modularity of this topology is an important feature. However, the fact that the dc-link voltages must be isolated is the major drawback in the application of these

structures. Several independent dc power supplies are required, which can be provided either by a transformer with multiple isolated secondary wirings or by several transformers. For electric vehicles, batteries or fuel cells can also be used.
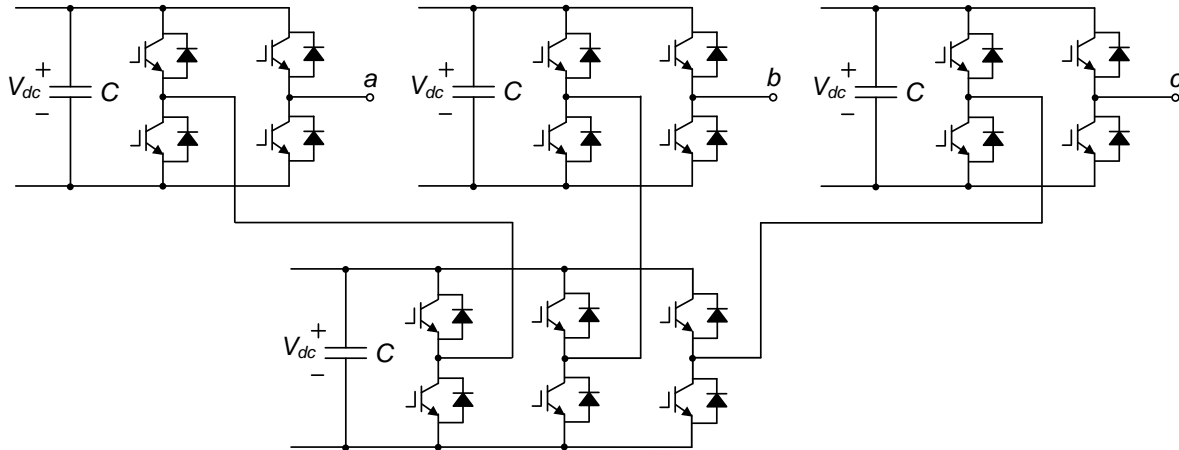
Fig.2.9. Four-level cascade converter.

In order to balance the power provided by the dc voltage sources, each cell can be used cyclically throughout each semi-cycle of a line period (Schibli et al. 1998). Another benefit of this circulating method is that it achieves the same switching frequencies for all of the devices.

On the other hand, in applications which do not handle active power –such as active filters, static compensators (STATCOM), etc.– the dc buses may not need power supplies, but only capacitors.

For a given topology, a higher number of levels can be obtained if each cascade level is fed by a different dc voltage value. Different devices would make up each cell, so that the fastest ones, which may synthesize the cell fed by the lower voltage, will define the output voltage switching frequency (Manjrekar et al. 2000).

2.1.4. General Data for Basic Multilevel Topologies

Table 2.4 summarizes the general characteristics of basic multilevel topologies (Pou Josep 2002).

Table 2.4. Summarizes the general characteristics of basic multilevel topologies.

Topology		a	b	c	d	e	f	g	h	i	j
Diode-Clamped Converter	*n*-Level	$6(n-1)$	$6(n-2)$	$3(n-1)(n-2)$	$n-1$	$n-1$	$V_{dc}(n-1)$	$2n-1$	$4n-3$	n^3	$n^3-(n-1)^3$
	3-Level	12	6	6	2	2	$V_{dc}/2$	5	9	27	19
	4-Level	18	12	18	3	3	$V_{dc}/3$	7	13	64	37
	5-Level	24	18	36	4	4	$V_{dc}/4$	9	17	125	61
Floating-Capacitor Converter	*n*-Level	$6(n-1)$	0	0	$3n-5$	$(n-1)^2+3\sum_{i=1}^{n-2}i^2$	$V_{dc}/(n-1)$	$2n-1$	$4n-3$	$2^{3(n-1)}$	$n^3-(n-1)^3$
	3-Level	12	0	0	4	7	$V_{dc}/2$	5	9	64	19
	4-Level	18	0	0	7	24	$V_{dc}/3$	6	13	512	37
	5-Level	24	0	0	10	58	$V_{dc}/4$	9	17	4096	61
Cascade Converter	*n*-Level	$6(n-1)$	0	0	(Even) $3n/2-1.5$ (Odd) $3n/2-2$	(Even) $3n/2-1.5$ (Odd) $3n/2-2$	$V_{dc\ equiv}/(n-1)$	$2n-1$	$4n-3$	$2^{3(n-1)}$	$n^3-(n-1)^3$
	3-Level	12	0	0	3	3	$V_{dc\ equiv}/2$	5	9	64	19
	4-Level	18	0	0	4	4	$V_{dc\ equiv}/3$	6	13	512	37
	5-Level	24	0	0	6	6	$V_{dc\ equiv}/4$	9	17	4096	61

a): Switches (with free-wheeling diodes).

b): Independent diodes (with different reverse voltage possible.

c): Real number of independent diodes (series connection for same reverse voltage distribution).

d): capacitors (with different voltage possible).

e): real number of capacitors (series and parallel connection for the same voltage distribution and capacitance.

f): maximum voltage applied.

g): line-to-line output voltage levels.

h): phase voltage levels for star load connection.

i): states of the converter (total vectors of the SV diagram, including multiple ones).

j): states of the converter with different line-to-line voltage (different vectors of the SV diagram).

2.2. Prototype Description

The major experimental results of this dissertation have been obtained using the platform shown in Fig.2.10, which was built by Robotiker-Tecnalia Technology Corporation, Zamudio, Basque Country, Spain.

The experimental platform is composed of a control board based on a DSP, a PLD board, and an NPC converter. The system can operate both by transferring energy from the dc side to the ac side (inverter mode) or vice versa (rectifier mode). It has been used to test the modulation and control techniques proposed in this dissertation.
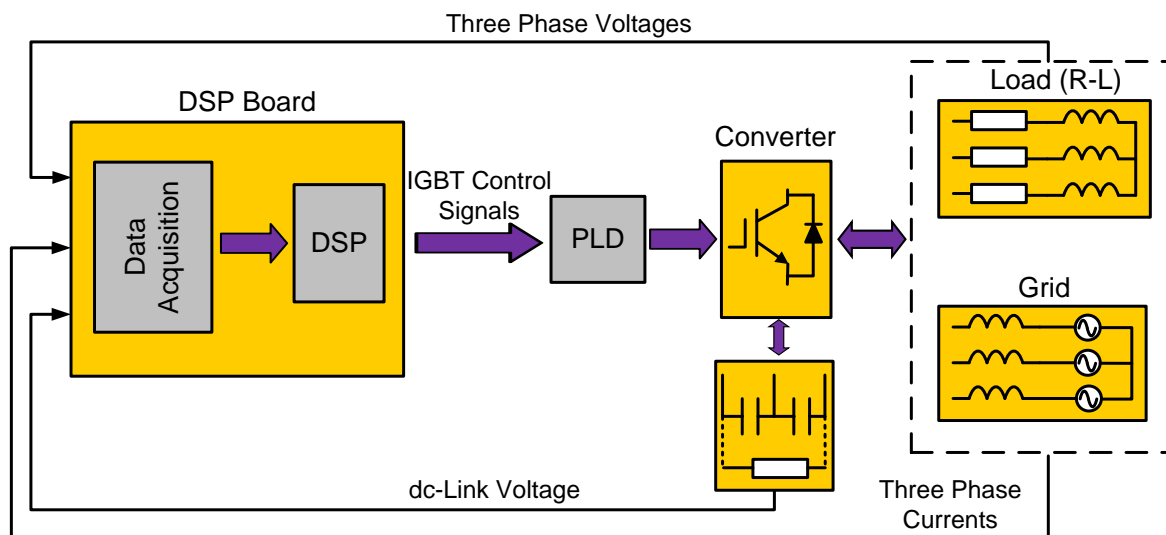
Fig.2.10. General diagram of the experimental platform.

2.2.1. NPC Converter Description

Fig.2.11(a) shows a general diagram of the NPC converter, including its voltage and current sensors. Fig.2.11(b) shows a picture of the converter.

All phase legs in Fig.2.11 are built based on IGBTs of SEMIKRON (SKM100). The system is rated at 20 kVA while switching at 10 kHz. The maximum dc-link voltage is 900 V and the rated RMS output voltages and currents are 400 V and 30 A, respectively. The converter has a total dc-link capacity of 2.2 mF. It is composed of four capacitors, each one a unit of 2.2 mF/450 V that is connected as shown in

Fig.2.11(a). Therefore, with this configuration, the upper and lower capacitors shown in the NPC scheme in Fig.2.11(a) are *C*=4.4 mF. However, depending on the test that is performed, the connection may be changed to highlight some effects. The value of capacitor *C* is defined in each experimental test.

As shown in Fig.2.11(a), this converter has five voltage sensors (ABB VS 500B) and seven current sensors; the I_{bus2}, I_{bus3} and I$_{bus5}$, correspond to HAL 50-S sensors, which measure the currents at the dc-link side between the capacitors and the converter legs. The other current sensors (I_{bus1}, I_{bus4}, I_{phase1}, I_{phase2} and I_{phase3}) are LEM LA 205-S and they measure the currents before the capacitors and the ac output currents.

Fig.2.11(b) shows the NPC converter assembly. At the top of this picture one can see the twelve drivers that provide the correct signals to switch the IGBTs on and off. These drivers are SKI 10/17, which integrate proper circuitry for transistor protection.

(a)

(b)
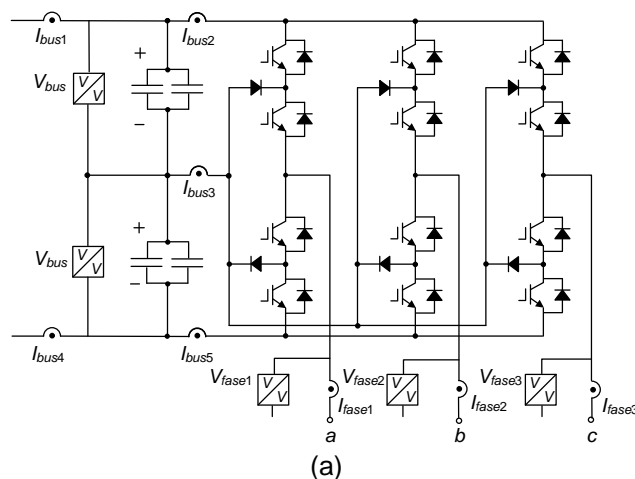
Fig.2.11. NPC converter: (a) general diagram, and (b) converter set up.

2.2.2. Digital Control Hardware

The complexity of control in multilevel converters results in the almost exclusive application of digital control hardware for these systems. In addition, the versatility of modern microprocessors allows implementation of any type of control and modulation algorithms.

The main aspects of the digital control of the NPC converter are presented in the following Fig.2.12.

(a)
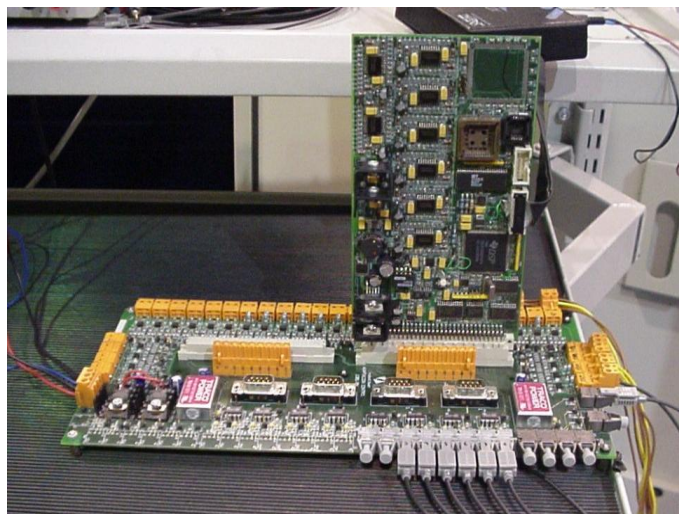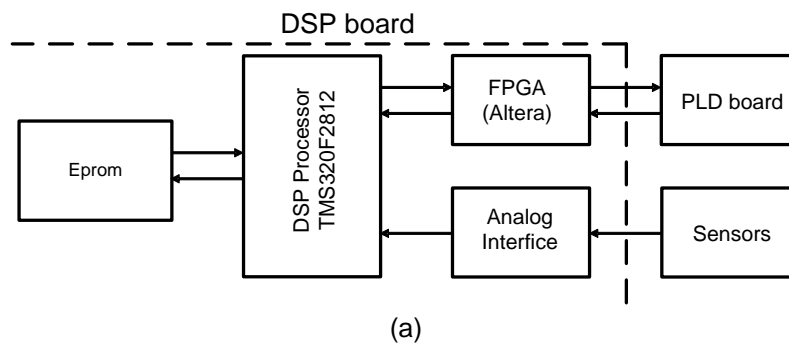
Fig.2.12. Control hardware: (a) architecture and (b) DSP board.

Fig.2.12(a) shows the block diagram of the DSP-based controller of the three-level dc-ac converter. It is divided into the three following functional subsystems, implemented on separate printed circuit boards:

- DSP subsystem,

- digital interface subsystem with flex erasable and programmable logic devices (FPGA), and

- analog interface subsystem with A/D and D/A converters.

2.2.2.1. Digital Signal Processor

The DSP used is the TMS320F2812 from Texas Instruments. It is highly integrated and provides high-performance solutions for demanding control applications. It is a 32-bit fixed-point processor with a frequency of 150 MHz. It incorporates an analog-to-digital (A/D) convertor of 16 channels with a conversion time of 80 ns. With the most demanding software implemented in the DSP, the total execution time of the control loops and modulation is less than 25 µs. This allows the system to work at a switching frequency of up to 20 kHz.

2.2.2.2. PLD Board

The PLD board shown in Fig.2.13(b) is based on a programmable logic device (PLD). The switching and control signals are transmitted with optical fiber connections between the DSP and this PLD board. There are six switching signals that define the state of all the transistors of the converter. The PLD board decodes

(a)   (b)
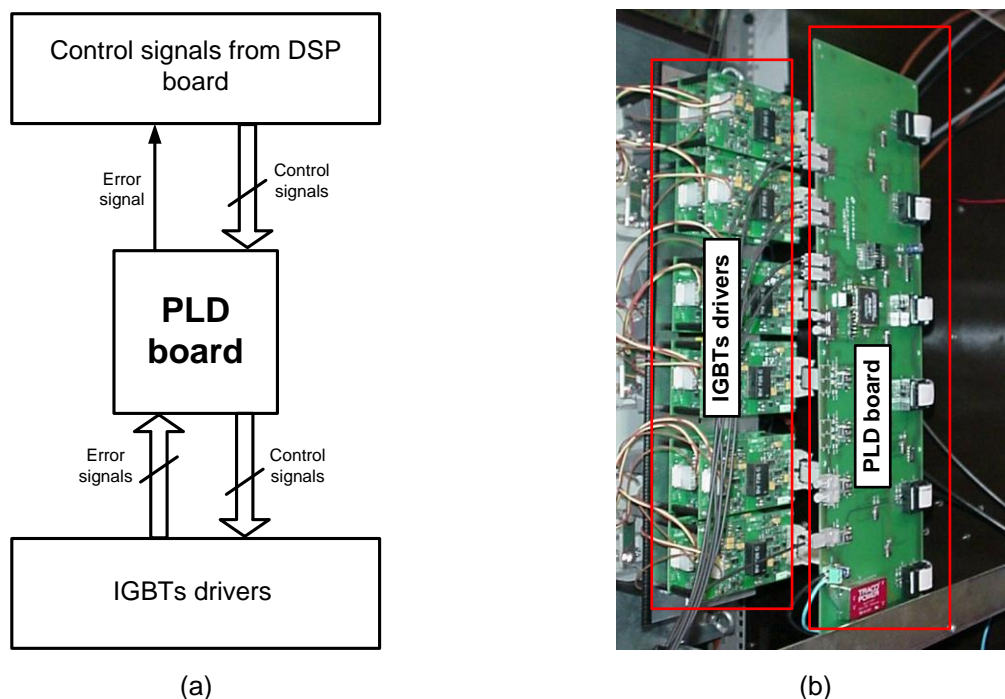
Fig.2.13. PLD board and IGBTs drivers: bloc diagram and, b) building.

the switching signals and generates proper dead times for the transistors. This board is also responsible for managing protection of the transistors whenever an error signal from a transistor driver appears.

2.3. Modulation Techniques

This section classifies the main modulation techniques. It also presents and analyses some of those that are most widely used. The modulation consists of determining the state of each power device of the converter and how long it should be maintained in order to obtain the desired output voltages or currents (taking into account their locally-averaged values over a sampling period).

Fig.2.14 shows a classification of the modulation strategies (Rodriguez J. et al. 2002a) according to the switching frequency.
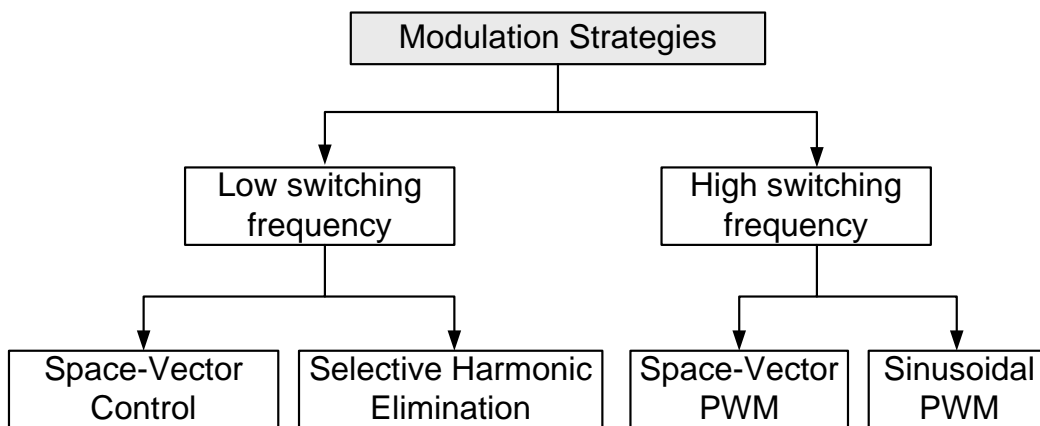
Fig.2.14. Classification of modulation strategies.

Some high switching frequency modulation strategies are discussed in the following sections. A summary of the more representative low switching frequency modulation techniques, such as selective harmonic elimination (SHE) and space-vector control (SVC), can be found in (Li et al. 2000, Sirisukprasert et al. 2002) and (Rodriguez J. et al. 2002b, Rodriguez J. et al. 2003) respectively.

2.3.1. Space-Vector Modulation (SVM)

The most extended modulation strategy in three-phase multilevel converters is the SVM (Pou J. et al. 2005c, Yo-Han et al. 1999). This is because it allows larger

amplitudes of the output voltages than the standard sinusoidal PWM. Furthermore, it is very simple to implement strategies to help for voltage balance in the dc-link capacitors through proper use of the redundant vectors from the space-vector diagrams.

The SVM comes from the idea of representing each of the possible states of the converter in a three-dimensional representation. Three stationary and orthogonal axes are used for the representation. Joining the tips of the vectors obtained from conventional topologies of inverters shows geometrical cubes in this 3D representation (Prats et al. 2003, Rodriguez P. et al. 2005).

The same vectors can be seen from another orthogonal and stationary base called $\alpha\beta\gamma$ (or $\alpha\beta o$), in which the γ component (or zero sequence) does not have a significant roll in the modulation. This is generally true if the load is not connected to the dc-link side of the inverter. Due to this fact, the only variables of interest are the ones on the $\alpha\beta$ plane.

The well known Clarke transformation allows the three-dimensional vector representation to be displayed directly in a two-dimensional diagram, i.e. the $\alpha\beta$ plane (Fig.2.15). Given the three output voltages of the converter (v_{a0}, v_{b0} and v_{c0}), the projection on the plane $\alpha\beta$ (v_α, v_β) of a three-dimensional vector is:

$$\vec{V} = v_\alpha + j\, v_\beta = v_{a0}\, \vec{a}^0 + v_{b0}\, \vec{a}^1 + v_{c0}\, \vec{a}^2 , \qquad (2.1)$$

where $\vec{a} = e^{j\frac{2\pi}{3}}$.

Fig.2.15(a) shows the three unitary director vectors of this transformation, while Fig. 2.15(b) shows an example of the case in which v_{a0}=200 V, v_{b0}=300 V, and v_{c0}=−100 V.

The aim of the SVM is to generate a reference vector ($\vec{V}_{REF}$) in the same plane for each modulation cycle. As the reference vector may not be the same as any vector produced by the converter, its average value can be generated using more than one vector per modulation cycle by PWM-averaged approximation. Selecting proper vectors and applying them in a suitable order helps the devices achieve low switching frequencies.

(a)   (b)
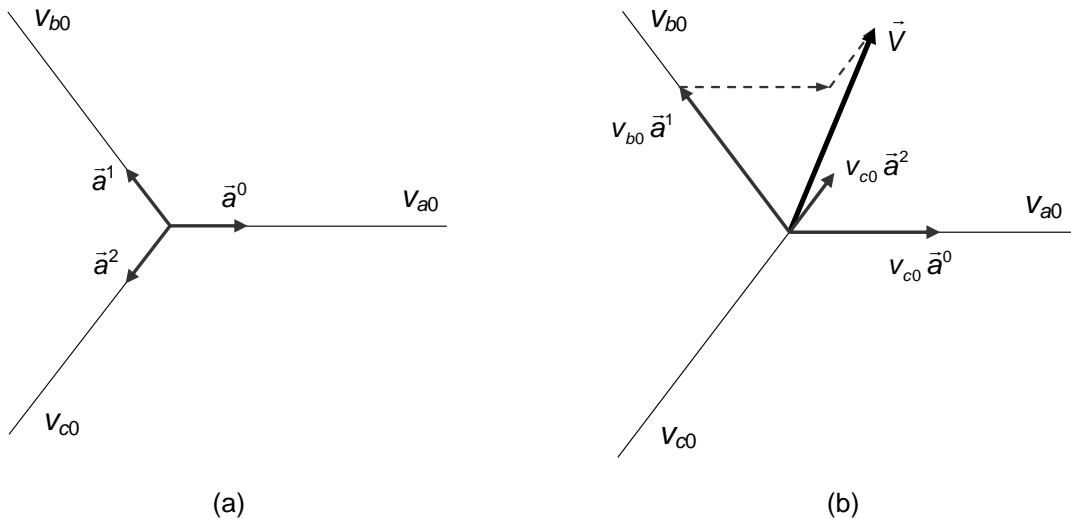
Fig.2.15. Clarke's Transformation: (a) director vectors, and
(b) example of spatial vector for v_{a0}=200 V, v_{b0}=300 V, and v_{c0}=-100 V.

In steady-state conditions, the reference vector rotates at a constant angular speed (ω), which defines the frequency of the output voltages. The amplitude of the fundamentals of those voltages is proportional to the length of the reference vector.

There are eight possible states for the two-level converter ($n^3=2^3=8$), which produce the voltage vectors shown in Fig.2.16. In this figure, the switching states are illustrated by 1 and -1, which denote the corresponding voltage levels of V_{dc}/2 and -V_{dc}/2 with respect to the NP. Six of the space vectors have equal lengths and are located every sixty degrees (1-1-1, 11-1, -11-1, -111, -1-11, 1-11). The other two vectors are in the origin because of their null lengths (-1-1-1, 111).
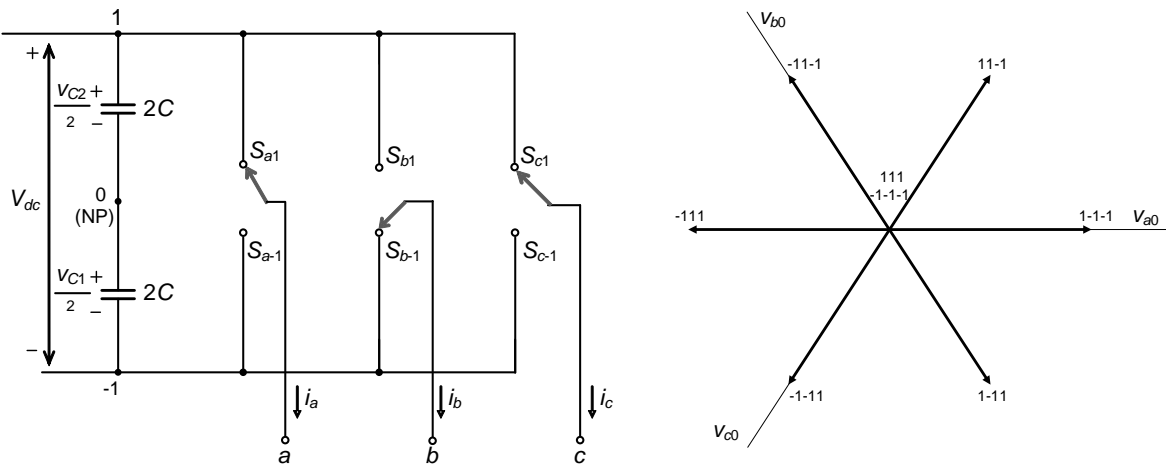
Fig.2.16. SV diagram of the two-level converter.
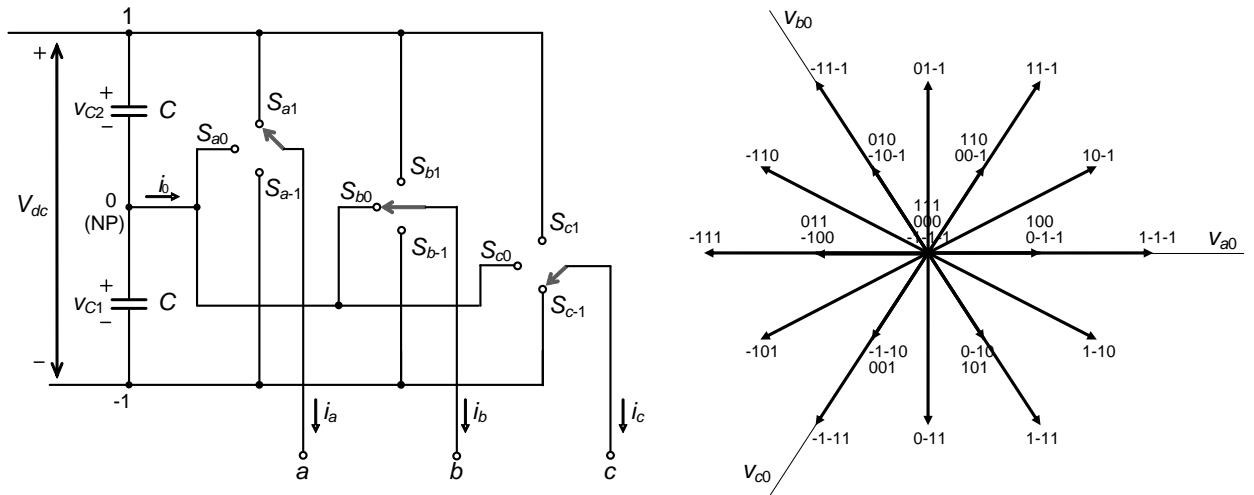
Fig.2.17.SV diagram of the three-level converter.

The SV diagram of the three-level converter has twenty-seven vectors (Fig.2.17). The redundant vectors in this diagram produce the same line-to-line voltages. The three-level converter has six double vectors and one triple vector in the origin. Proper utilization of these vectors will help the voltages of the capacitors to achieve balance.

In the following subsections, some general aspects of the SVM will be revised.

2.3.2. Limiting Area

Any set of three vectors $\vec{v}_1$, $\vec{v}_2$ and $\vec{v}_3$ in a plane ($\alpha\beta$ in Fig.2.18) can generate any reference vector $\vec{V}_{REF}$ in the same plane using PWM-averaged approximation, if the reference vector lies in the triangle connecting the tips of $\vec{v}_1$, $\vec{v}_2$ and $\vec{v}_3$.

The average reference vector can be obtained by sequentially applying these vectors in a modulation period in accordance with:

$$\frac{1}{T_s}\int_0^{T_s} \vec{V}_{REF}\vec{m}\,dt = \frac{1}{T_s}\int_0^{T_1} \vec{v}_1\,dt + \frac{1}{T_s}\int_{T_1}^{T_1+T_2} \vec{v}_2\,dt + \frac{1}{T_s}\int_{T_1+T_2}^{T_s} \vec{v}_3\,dt, \qquad (2.2)$$

where T_s is the sampling period, and $T_1+T_2 \leq T_s$.

Assuming that $\vec{V}_{REF}$ remains approximately constant during a sampling or switching period, which is acceptable if T_s is much smaller than the line period (T), then (2.2) can be approximated as:

$$\vec{V}_{REF} = d_1\vec{v}_1 + d_2\vec{v}_2 + d_3\vec{v}_3, \tag{2.3}$$

in which d_1, d_2 and d_3 are the duty cycles of vectors $\vec{v}_1$, $\vec{v}_2$ and $\vec{v}_3$, respectively. They must satisfy the following condition:

$$d_1 + d_2 + d_3 = 1. \tag{2.4}$$
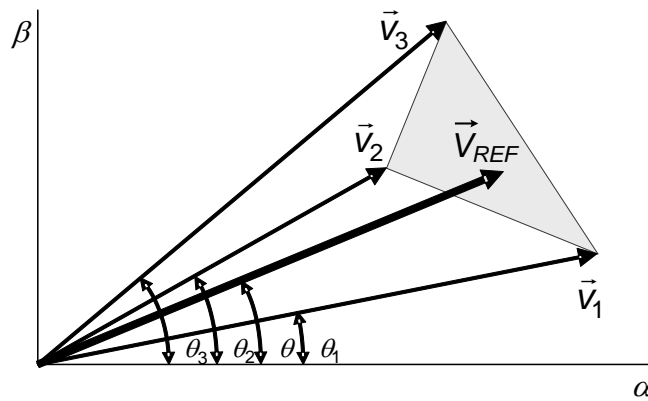
Fig.2.18. Limiting area to generate the reference vector ($\vec{V}_{REF}$) by using three vectors.

The boundaries of the area that allows the reference vector to be generated can be determined by assigning a zero value to one of the duty cycles. For example, imposing d_3=0, and by means of (2.3) and (2.4), the vector $\vec{V}_{REF}$ can be expressed as follows:

$$\vec{V}_{REF} = \vec{v}_2 + d_1(\vec{v}_1 - \vec{v}_2). \tag{2.5}$$

As all the duty cycles could potentially utilize values in the interval $[0, 1]$, the tip of the reference vector is on the line that joins the extremes of the vectors $\vec{v}_1$ and $\vec{v}_2$ (Fig.2.19), which can be verified by simply making d_1 vary within that interval. Therefore, this segment is one boundary of the limiting area. The other two remaining segments of the triangular region in Fig.2.18 can be determined by assigning zero to d_1 and d_2 separately.

Any reference vector outside of the gray area in Fig.2.18 requires that one or more duty cycles be negative. This fact does not make physical sense; thus, it cannot be generated by this set of three vectors.
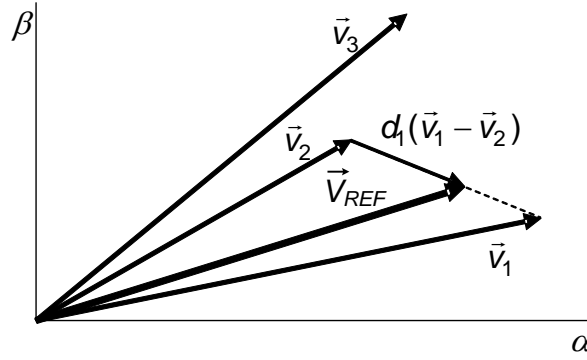
Fig.2.19. Boundary of the area, determined when $d_3=0$.

2.3.3. Calculation of Duty Cycles

Equation (2.3) can be expressed by the following exponential notation:

$$\vec{V}_{REF} = V e^{j\theta} = d_1 v_1 e^{j\theta_1} + d_2 v_2 e^{j\theta_2} + d_3 v_3 e^{j\theta_3} . \tag{2.6}$$

Therefore, the duty cycles of the vectors can be calculated according to either of the following equation systems:

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} v_1\cos\theta_1 & v_2\cos\theta_2 & v_3\cos\theta_3 \\ v_1\sin\theta_1 & v_2\sin\theta_2 & v_3\sin\theta_3 \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} V\cos\theta \\ V\, sen\theta \\ 1 \end{bmatrix}, \text{ or} \tag{2.7}$$

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} \mathrm{Re}(\vec{v}_1) & \mathrm{Re}(\vec{v}_2) & \mathrm{Re}(\vec{v}_3) \\ \mathrm{Im}(\vec{v}_1) & \mathrm{Im}(\vec{v}_2) & \mathrm{Im}(\vec{v}_3) \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} \mathrm{Re}(\vec{V}_{REF}) \\ \mathrm{Im}(\vec{V}_{REF}) \\ 1 \end{bmatrix} . \tag{2.8}$$

In general terms, given any bi-dimensional stationary base frame, whether orthogonal or not, the expression would be:

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \begin{bmatrix} \left|\vec{v}_1\right|_x & \left|\vec{v}_2\right|_x & \left|\vec{v}_3\right|_x \\ \left|\vec{v}_1\right|_y & \left|\vec{v}_2\right|_y & \left|\vec{v}_3\right|_y \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} \left|\vec{V}_{REF}\right|_x \\ \left|\vec{V}_{REF}\right|_y \\ 1 \end{bmatrix} . \tag{2.9}$$

The calculation process for any of these equation systems requires inverting a matrix, which complicates the application of this method to a real-time processor system. Additionally, the equation system may need to be solved more than once per

modulation period (T_s), since the region where the reference vector lies is previously unknown. A simplified mathematical process should be found.

2.3.4. Calculation of Duty Cycles by Projections

A general method for calculating duty cycles of vectors is explained in this section. This method is based on determining some projections of the reference vector, and it will be applied in order to simplify the modulation process later.

The vectors $\vec{p}_1$ and $\vec{p}_2$ in Fig.2.20 are the projections from the reference vector $\vec{V}_{REF}$ onto the segments that join the extreme of $\vec{v}_3$ to $\vec{v}_1$ and to $\vec{v}_2$, respectively.
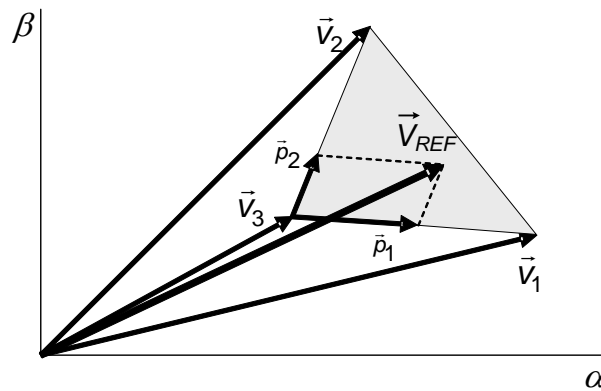
Fig.2.20.Projections of the reference vector $\vec{V}_{REF}$ ($\vec{p}_1$ and $\vec{p}_2$).

Therefore, the reference vector can be expressed as follows:

$$\vec{V}_{REF} = \vec{p}_1 + \vec{p}_2 + \vec{v}_3 \text{ or} \tag{2.10}$$

$$\vec{V}_{REF} = p_1 \frac{\vec{v}_1 - \vec{v}_3}{l_1} + p_2 \frac{\vec{v}_2 - \vec{v}_3}{l_2} + \vec{v}_3, \tag{2.11}$$

where l_1 and l_2 are the lengths of the vectors $\vec{v}_1 - \vec{v}_3$ and $\vec{v}_2 - \vec{v}_3$, respectively. Finally, the reference vector $\vec{V}_{REF}$ can be expressed as:

$$\vec{V}_{REF} = \frac{p_1}{l_1}\vec{v}_1 + \frac{p_2}{l_2}\vec{v}_2 + \left(1 - \frac{p_1}{l_1} - \frac{p_2}{l_2}\right)\vec{v}_3. \tag{2.12}$$

From (2.12), the duty cycles of the vectors can be directly deduced as follows:

$$d_1 = \frac{p_1}{l_1}, \quad d_2 = \frac{p_2}{l_2}, \quad \text{and} \quad d_3 = 1 - \frac{p_1}{l_1} - \frac{p_2}{l_2}. \qquad (2.13)$$

If the balanced SV diagram is normalized to have triangular regions with unity lengths ($l_1 = l_2 = 1$), the calculation of those duty cycles is simplified as:

$$d_1 = p_1, \quad d_2 = p_2, \quad \text{and} \quad d_3 = 1 - p_1 - p_2. \qquad (2.14)$$

Calculation of duty cycles using this method is actually very functional. However, the former condition that all the areas must be equilateral triangles is only possible if the voltages of the dc-link capacitors are balanced. Thus, when dealing with the unbalanced case, these lengths can no longer be considered to be unity because they change according to the present imbalance. In that case, (2.13) must be applied.

2.3.5. Three-Level Converter

2.3.5.1. SVM under Voltage-Balanced Conditions

Suitable vectors from the SV diagram should be chosen for each modulation cycle in order to generate the reference vector ($\vec{V}_{REF}$). The vectors nearest to $\vec{V}_{REF}$ are the most appropriate selections in terms of their ability to minimize the switching frequencies of the power devices, improve the quality of the output voltage spectra, and the electromagnetic interference (EMI).

In Fig.2.21, the SV diagram of the three-level converter is divided into sectors, and each sector is then divided into four triangular regions in order to show the vectors nearest to the reference. It also shows the 27 switching states illustrated by 1, 0, and -1, which denote the corresponding voltage levels of $V_{dc}/2$, 0, and $-V_{dc}/2$ with respect to the NP.

Four groups of vectors can be distinguished in this diagram, as described in the following.

(1) The "large vectors" (1-1-1, 11-1, -11-1, -111, -1-11 and 1-11) assign the output voltages of the converter to either the highest or the lowest dc voltage levels.

As they do not connect any output to the NP, they do not affect the voltage balance of the capacitors. These vectors can generate the highest ac voltage amplitudes because they have the greatest lengths. In fact, these six vectors are equivalent to the active ones in the two-level converter.
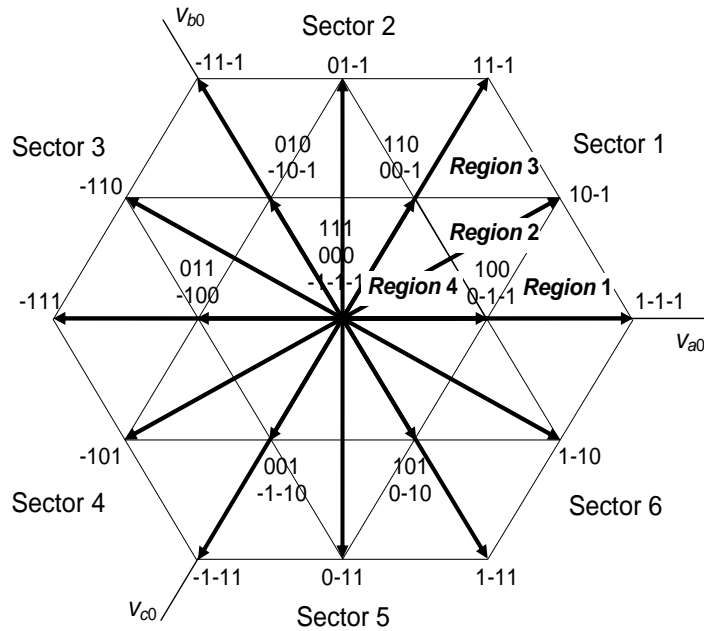
Fig.2.21. Three-level vector diagram divided into sectors and regions.

(2) The "medium vectors" (10-1, 01-1, -110, -101, 0-11 and 1-10) connect each output to a different dc-link voltage level. Under balanced conditions, their tips end in the middle of the segments that join two consecutive large vectors. The length of the medium vectors defines the maximum amplitude of the reference vector for linear modulation and steady-state conditions, which is $\sqrt{3}/2$ times the length of the large vectors. Since one output is always connected to the NP, the corresponding output current will define the NP current (i_0). This connection produces voltage imbalances in the capacitors, and these must be compensated.

(3) The "short vectors" (0-1-1 or 100, 00-1 or 110, -10-1 or 010, -100 or 011, -1-10 or 001 and 0-10 or 101) connect the ac outputs to two consecutive dc-link voltage levels. Their length is half the length of the large vectors. They are double vectors, which means that two states of the converter can generate the same voltage vector.

As they affect the NP current in opposite ways, proper utilization of these vectors will help the NP voltage to achieve balance.

(4) The "zero vectors" (-1-1-1, 000 and 111) are in the origin of the diagram. They connect all of the outputs of the converter to the same dc-link voltage level, and therefore, they do not produce any current on the dc side.

2.3.5.1.1. Simplified Calculation of Duty Cycles

Taking into account the symmetry of all the sectors, it is interesting to reflect the reference vector into the first sector in order to reduce the number of relevant regions. Also, the amplitude of the reference vector must be normalized to fit into a diagram in which the triangular regions have unity lengths.

The theoretical maximum length of the normalized reference vector ($\vec{m}_n$) is the two-unity value. However, in steady-state conditions, its length is limited to $\sqrt{3}$, due to the fact that longer lengths of this vector will be outside of the vector-diagram hexagon (Fig.2.22), and thus cannot be generated by modulation. Overmodulation is produced if the normalized reference vector assumes lengths longer than $\sqrt{3}$ for some positions of this vector, but it can never be outside of the hexagon.
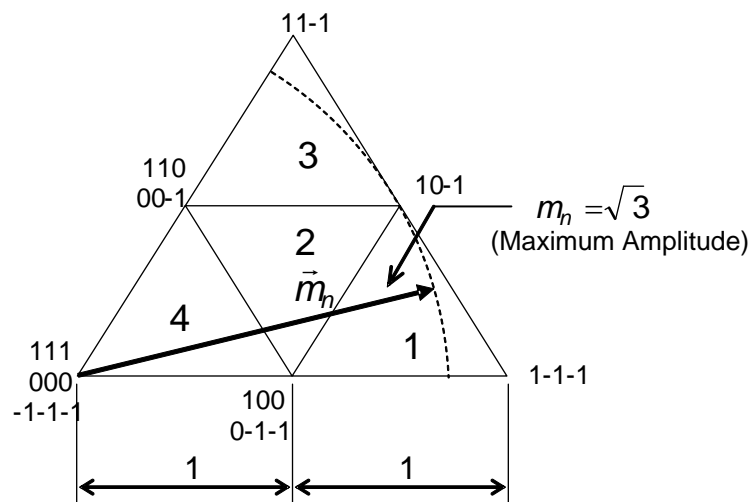
Fig.2.22. Maximum length of the normalized reference vector in steady-state conditions.

Defining a modulation index m that potentially uses values in the interval $m \in [0, 1]$ for linear modulation, the length of the normalized reference vector would be:

$$m_n = \sqrt{3}\, m \qquad \left(0 \le m_n \le \sqrt{3}\right). \tag{2.15}$$

In Fig.2.23, the normalized reference vector is decomposed into the axes located at zero and sixty degrees, obtaining projections m_1 and m_2, respectively.
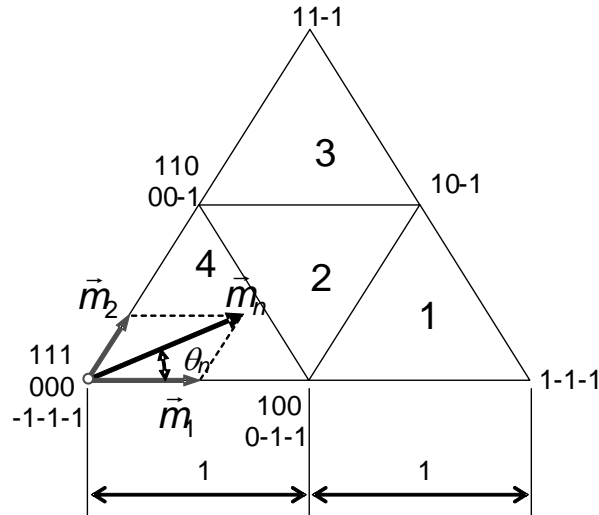
Fig.2.23. Projections of the normalized reference vector in the first sector.

The lengths of the new vectors are determined as follows:

$$m_1 = m_n\left(\cos\theta_n - \frac{\sin\theta_n}{\sqrt{3}}\right) \qquad and \qquad m_2 = 2m_n\frac{\sin\theta_n}{\sqrt{3}}. \tag{2.16}$$

In accordance with the general method revealed in Section 2.3.4, these values are the direct duty ratios of the vectors, as in the following:

$$d_{0-1-1/100} = m_1, \quad d_{00-1/110} = m_2 \quad \text{and} \quad d_{000} = 1 - m_1 - m_2. \tag{2.17}$$

Even though there are three redundant vectors in the origin, only the combination "000" is considered because it achieves the best modulation sequences in terms of switching frequency.

The cases for which the normalized reference vector is located in Regions 1, 2 and 3 are shown in Fig.2.24.

For all cases, it is assumed that the sum of m_1 and m_2 is not greater than 2; otherwise, the reference vector would be outside of the hexagon, and thus could not be reproduced by modulation.

Table 2.5 summarizes the information needed to ascertain the region where the reference vector lies the duty cycles of the nearest vectors in the first sector.
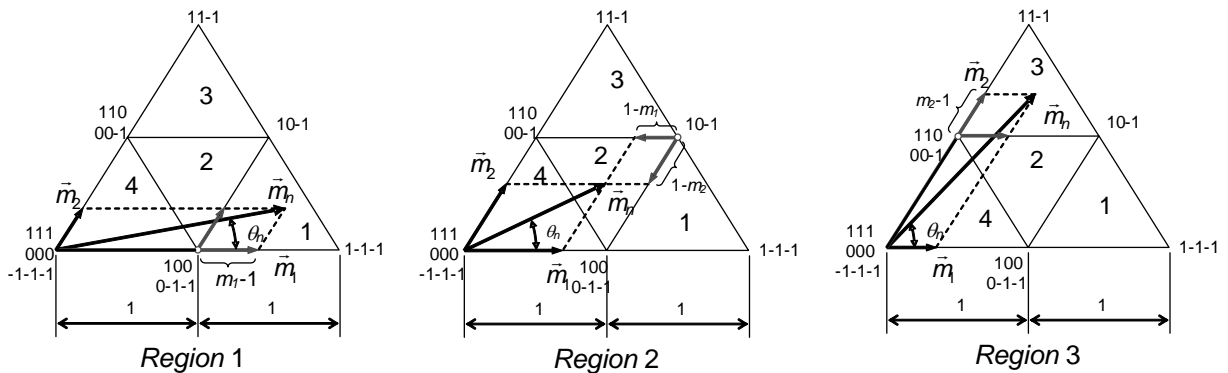
Fig.2.24. Projections for Regions 1, 2 and 3.

Table 2.5. Summary of information for the SVM.

Case	Region	Duty Cycles
$m_1 > 1$	1	$d_{1\text{-}1\text{-}1} = m_1 - 1$ $d_{10\text{-}1} = m_2$ $d_{0\text{-}1\text{-}1/100} = 2 - m_1 - m_2$
$m_1 \leq 1$ $m_2 \leq 1$ $m_1 + m_2 > 1$	2	$d_{0\text{-}1\text{-}1/100} = 1 - m_2$ $d_{00\text{-}1/110} = 1 - m_1$ $d_{10\text{-}1} = m_1 + m_2 - 1$
$m_2 > 1$	3	$d_{10\text{-}1} = m_1$ $d_{11\text{-}1} = m_2 - 1$ $d_{00\text{-}1/110} = 2 - m_1 - m_2$
$m_1 \leq 1$ $m_2 \leq 1$ $m_1 + m_2 \leq 1$	4	$d_{0\text{-}1\text{-}1/100} = m_1$ $d_{00\text{-}1/110} = m_2$ $d_{000} = 1 - m_1 - m_2$

2.3.5.2. NTV Modulation

The NTV modulation technique uses only three of the closest vectors per modulation cycle. Thus, a single short vector will be selected from each pair. The choice is made according to the objective of maintaining balanced voltages in the dc-link capacitors; therefore, the present voltage imbalance and the direction of the instantaneous output currents must be known. The NP current (i_0) must be positive in order to discharge the lower capacitor, and must be negative to charge it. For example, if i_a is positive, vector 0-1-1 will discharge the lower capacitor ($i_0 = i_a > 0$), and vector 100 will charge it ($i_0 = i_b + i_c = -i_a < 0$).
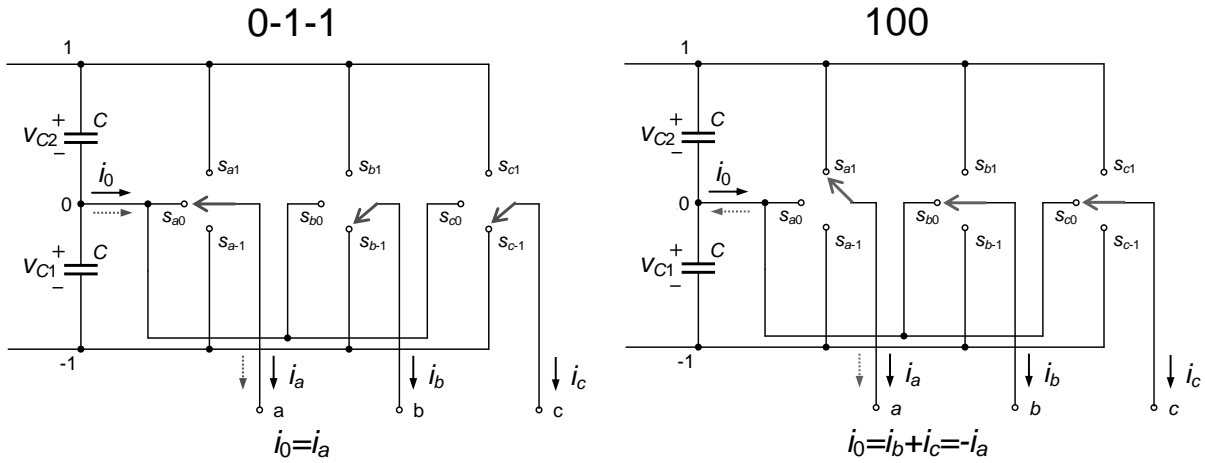
Fig.2.25. Example of control of the NP current by proper selection of the double vectors. Vector 0-1-1 produces $i_0=i_a$, whereas vector 100 produces $i_0=i_b+i_c=-i_a$.

Since all of the modulation will be calculated in the first sector, this criterion can be expressed as shown in Table 2.6(a). When the reference vector lies in the first sector, currents i_a' and i_c' in these tables will be i_a and i_c, respectively, but they must be changed when it lies in another sector. These equivalences are given in Table 2.6(b).

Table 2.6. (a) Criteria for selection between vectors 0-1-1 and 100, and vectors 00-1 and 110; and (b) equivalences of currents to process calculations in the first sector.

(a)

Selection between 0-1-1 and 100		Selection between 00-1 and 110	
$\Delta v_{NP} i_a' >0$	y_1	$\Delta v_{NP} i_c' >0$	y_2
0	1 (100)	0	0 (00-1)
1	0 (0-1-1)	1	1 (110)

$$y_1 = (\Delta v_{NP} i_a' > 0) \qquad y_2 = \Delta v_{NP} i_c' > 0$$

(b)

Equivalences	1st Sect.	2nd Sect.	3rd Sect.	4th Sect.	5th Sect.	6th Sect.
i_a'	i_a	i_b	i_b	i_c	i_c	i_a
i_c'	i_c	i_c	i_a	i_a	i_b	i_b

Table 2.7 shows the sequences of the vectors in the first sector that are more capable of minimizing the switching frequencies of the devices. These sequences depend on the short vectors that are selected according to voltage-balance

requirements. The number of changes or steps between consecutive vectors associated with each sequence is also indicated in this table. The worst cases are Region 2 (vectors 100-110) and Region 4 (vectors 100-110), both of which require four switching steps, which is twice the number required by any other sequences. When a sequence is repeated in a subsequent modulation period, the sequence is flipped in order to minimize the number of steps from one cycle to the next.

Table 2.7. Sequences of vectors in the first sector by NTV modulation.

Region	Short Vectors	Sequences	Steps
1	0-1-1	0-1-1/1-1-1/10-1 // 10-1/1-1-1/0-1-1	2 // 2
	100	1-1-1/10-1/100 // 100/10-1/1-1-1	2 // 2
2	0-1-1/00-1	0-1-1/00-1/10-1 // 10-1/00-1/0-1-1	2 // 2
	0-1-1/110	0-1-1/10-1/110 // 110/10-1/0-1-1	4 // 4
	100/00-1	00-1/10-1/100 // 100/10-1/00-1	2 // 2
	100-110	10-1/100/110 // 110/100/10-1	2 // 2
3	00-1	00-1/10-1/11-1 // 11-1/10-1/00-1	2 // 2
	110	10-1/11-1/110 // 110/11-1/10-1	2 // 2
4	0-1-1/00-1	0-1-1/00-1/000 // 000/00-1/0-1-1	2 // 2
	0-1-1/110	0-1-1/000/110 // 110/000/0-1-1	4 // 4
	100/00-1	00-1/000/100 // 100/000/00-1	2 // 2
	100/110	000/100/110 // 110/100/000	2 // 2

Since the selection of the double vectors in the NTV modulation is based on comparators and logical functions, a nonlinear control is performed. Although it is not possible to achieve a value that is precisely zero for the average NP current over a modulation period, the sign of this average current tends to balance those voltages so long as the short vectors are properly chosen; and thus the objective is nonetheless generally achieved.

Despite the simplicity of using only three vectors per modulation cycle, the following drawbacks exist:

- There are significant switching-frequency ripples in the voltages of the capacitors; and

- when changing sequences due to a new region or different selection of short vectors, two switching steps can be produced (two legs must switch one level). Due to this fact, and that there are some sequences that require four steps (Table 2.7), the switching frequencies will not be constant.

The symmetric modulation approach can overcome these disadvantages and keep the switching frequency constant.

Further insight into the NTV modulation with some experimental results and voltage ripple analysis can be found in (Pou J. et al. 2005b).

2.3.5.3. Symmetric Modulation

Symmetric modulation is characterized by using four vectors per modulation sequence. Dealing with another variable in the calculation of the duty cycles allows the equation of the NP current to be included in the equation system:

$$\vec{V}_{REF} = d_1\vec{v}_1 + d_2\vec{v}_2 + d_3\vec{v}_3 + d_4\vec{v}_4 \,, \tag{2.18a}$$

$$d_1 + d_2 + d_3 + d_4 = 1, \text{ and} \tag{2.18b}$$

$$\bar{i}_0 = \sum_{i,j,k \in \{0,2\}} \left[\left(d_{1jk} - d_{i11} \right) i_a + \left(d_{i1k} - d_{1j1} \right) i_b + \left(d_{ij1} - d_{11k} \right) i_c \right] = 0 \,. \tag{2.18c}$$

Equation (2.18a) is, in fact, a pair of equations. Equation (2.18c) shows the relationship between the local averaged value of the NP current, the duty cycles of the vectors, and the ac currents. Mathematically speaking, this new equation allows the NP current to equal zero in each modulation period.

Symmetric modulation is very similar to NTV in some respects. The new vector added to the sequence is one of the short vectors that was not selected using NTV. Thanks to this, the duty cycles are basically calculated by the same process, the only difference being that the duty cycle is applied in NTV to only one of the dual vectors and it is now shared between both of them. For instance, if the reference vector lies in Region 1, the sequence will be 0-1-1/1-1-1/10-1/100. To satisfy the zero-NP-current condition, the duty cycle calculated for 0-1-1/100 should now be properly distributed between them.
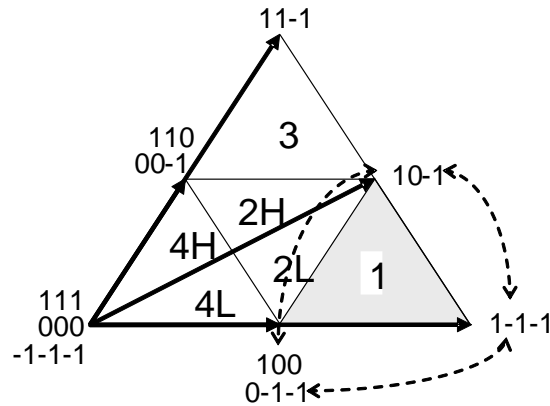
Fig.2.26. New regions for symmetric modulation. Example of vector sequence for Region 1.

For this modulation, Regions 2 and 4 are now split into 2L, 2H, 4L and 4H. The line that divides such regions, which coincides with vector 10-1, has been drawn according to a geometric-symmetry criterion. The best vector sequences in the first sector are given in Table 2.8; these sequences best minimize the switching frequencies of the devices.

Table 2.8. Sequences of vectors in the first sector by symmetric modulation.

Regions	Sequences	Steps
1	0-1-1/1-1-1/10-1/100 // 100/10-1/1-1-1/0-1-1	3 // 3
2L	0-1-1/00-1/10-1/100 // 100/10-1/00-1/0-1-1	3 // 3
2H	00-1/10-1/100/110 // 110/100/10-1/00-1	3 // 3
3	00-1/10-1/11-1/110 // 110/11-1/10-1/00-1	3 // 3
4L	0-1-1/00-1/000/100 // 100/000/00-1/0-1-1	3 // 3
4H	00-1/000/100/110 // 110/100/000/00-1	3 // 3

In general terms, the local averaged NP current must be zero to achieve constant voltage in the NP. However, the exact NP current required must be calculated for each modulation period in order to compensate for errors that occur due to tolerances and some assumptions. A modulation period delay is taken into account in order to obtain the reference NP current, and therefore the value calculated during the present period will be applied to the next modulation period. A detailed analysis on how the duty cycles in this modulation strategy would be calculated can be found in (Pou J. et al. 2005b).

2.3.5.4. Virtual-Vector Modulation

The modulation strategy based on virtual vectors can remove the low-frequency voltage oscillation that appears in the neutral point of the three-level inverter (Busquets-Monge et al. 2004). However, this strategy has no natural voltage balancing. In (Pou J. et al. 2005d), a fast-processing modulation algorithm is presented, which includes voltage-balancing control and therefore can remove any possible imbalance. Since the algorithm takes advantage of symmetry in the space-vector diagram, it can be processed quickly in a digital-signal processor.

An important advantage of this modulation strategy is that nonsinusoidal waveforms of the output currents from nonlinear loads will no longer produce instability.
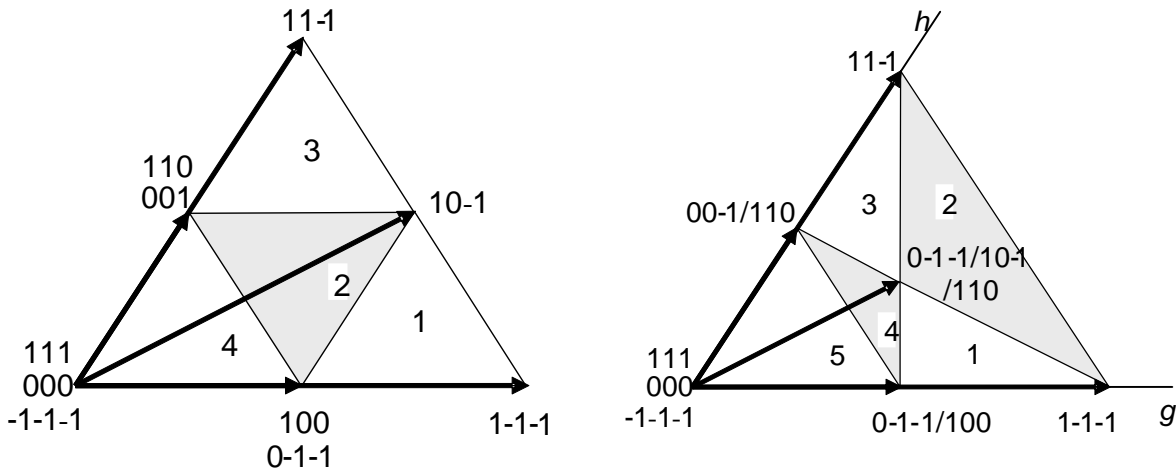
Fig.2.27. Triangular regions in the first sector of the space-vector diagram for: (a) standard modulation techniques and (b) the modulation based on virtual vectors.

The modulation strategy based on virtual vectors is explained as follows: taking into account that the short vectors of a set of redundant vectors produce opposite NP-current directions, if the time assigned to a pair of short vectors is shared equally between them, the averaged NP current will be zero. In accordance with this use of redundant vectors, the pairs 0-1-1/100 and 00-1/110 can be understood as zero-NP-current vectors. If no zero sequence is assumed in the output currents ($i_a+i_b+i_c=0$), this is also the case for vectors 0-1-1, 10-1 and 110, when equal time (33.33%) is applied to each of them. As a result, the SV diagram shown in Fig.2.27(b) is composed only of

vectors that produce an average NP current equal to zero. Calculation of duty cycles should be made in the new regions.

In general terms, the reference vector ($\vec{V}_{REF}$) can be obtained by PWM-averaged approximation making use of three vectors per modulation cycle in the new diagram.

Since two or more vectors generate the short vectors, the switching frequency of the power switches is higher than with other standard modulation strategies. In addition, the output voltages contain a higher switching frequency. These are the main drawbacks of this modulation strategy.

2.3.5.5 SPWM

The SPWM is widely used in industrial applications (N. Mohan et al. 2003). It is based on comparing a sinusoidal reference with a triangular carrier of significantly larger frequency (Fig.2.28).

Fig.2.28 shows the modulation signal $v_m(t) = \hat{V}_m \sin \omega t$, where the variable of the transistor control can be defined as follows:

$$\text{If } v_m \geq v_{carrier} \rightarrow s_a \text{ ON} \rightarrow v = v_{a0} = +V_{dc}/2,$$

$$\text{If } v_m < v_{carrier} \rightarrow s_a' \text{ ON} \rightarrow v = v_{a0} = -V_{dc}/2.$$

It can be observed that the switching frequency of the transistors is the same as the carrier's frequency (triangular waveform), and the modulation signal regulates the duration (width) of the output voltage (duty cycle).

Some parameters characterize the modulation, modulation index (m_a) and frequency index (m_f) as defined by (2.19) and (2.20), respectively.

$$m_a = \frac{\hat{V}_m}{\hat{V}_{carrier}} \Rightarrow \text{Linear modulation } (m_a \leq 1). \tag{2.19}$$

$$m_f = \frac{f_s}{f_m} \Rightarrow \text{Frequency index } (m_f > 1). \tag{2.20}$$
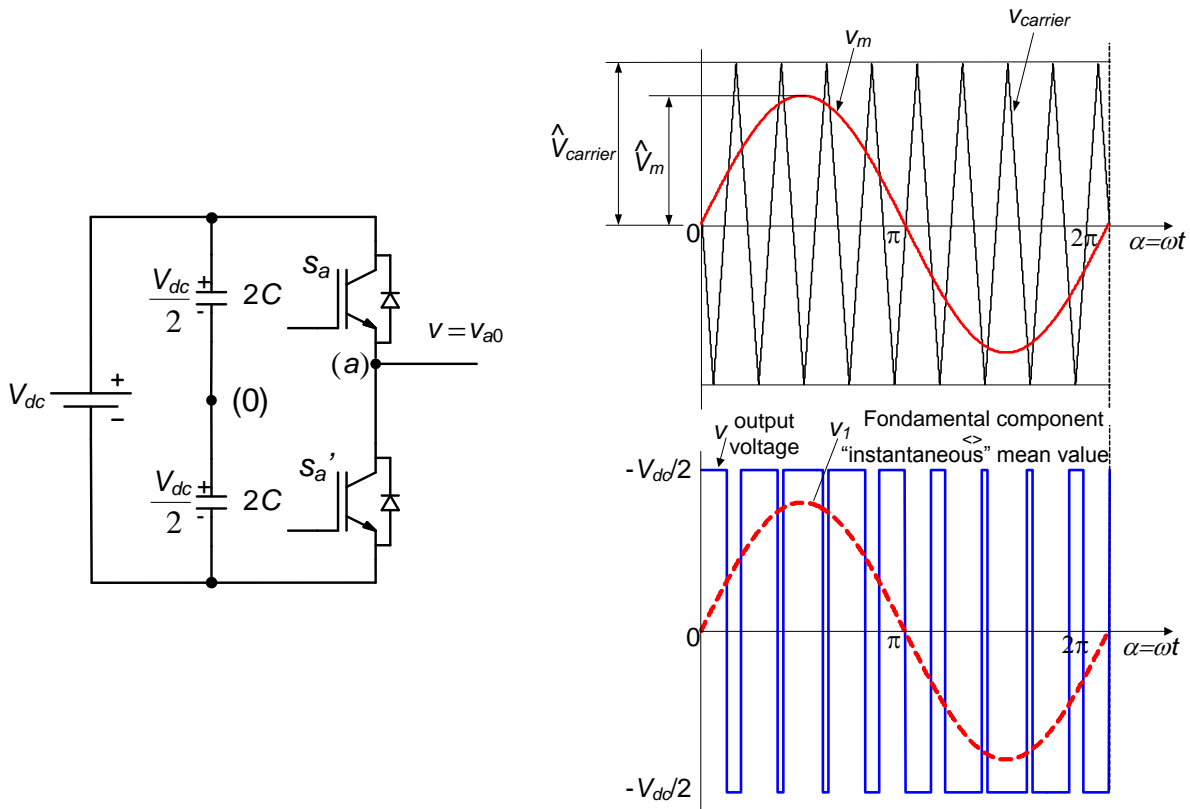
Fig.2.28. Output voltage representation using SPWM.

In (2.20) the f_s is the sampling of switching frequency, which is equal to the carrier frequency.

In the case of a multilevel converter, the number of carriers needed for the modulation is n-1, n being the number of levels of the converter. The carriers are usually shifted sequentially into the margin [-1,1] and therefore the pick-to-pick value of the carriers is $A_{p\text{-}p}=2/(n\text{-}1)$. Different carrier layouts are analyzed in the literature (Carrara et al. 1992), some of those patterns are shown in Fig.2.29.

Fig.2.29(a) shows the first layout when the carriers are alternatively in phase opposition (APO). Another possible layout is shown in Fig.2.29(b), in which the carriers above the zero value are in phase among themselves, but in phase opposition (PO) with the lower carriers. Finally, in the alternative shown in Fig.2.29(c), all the carriers have the same phase (PH).
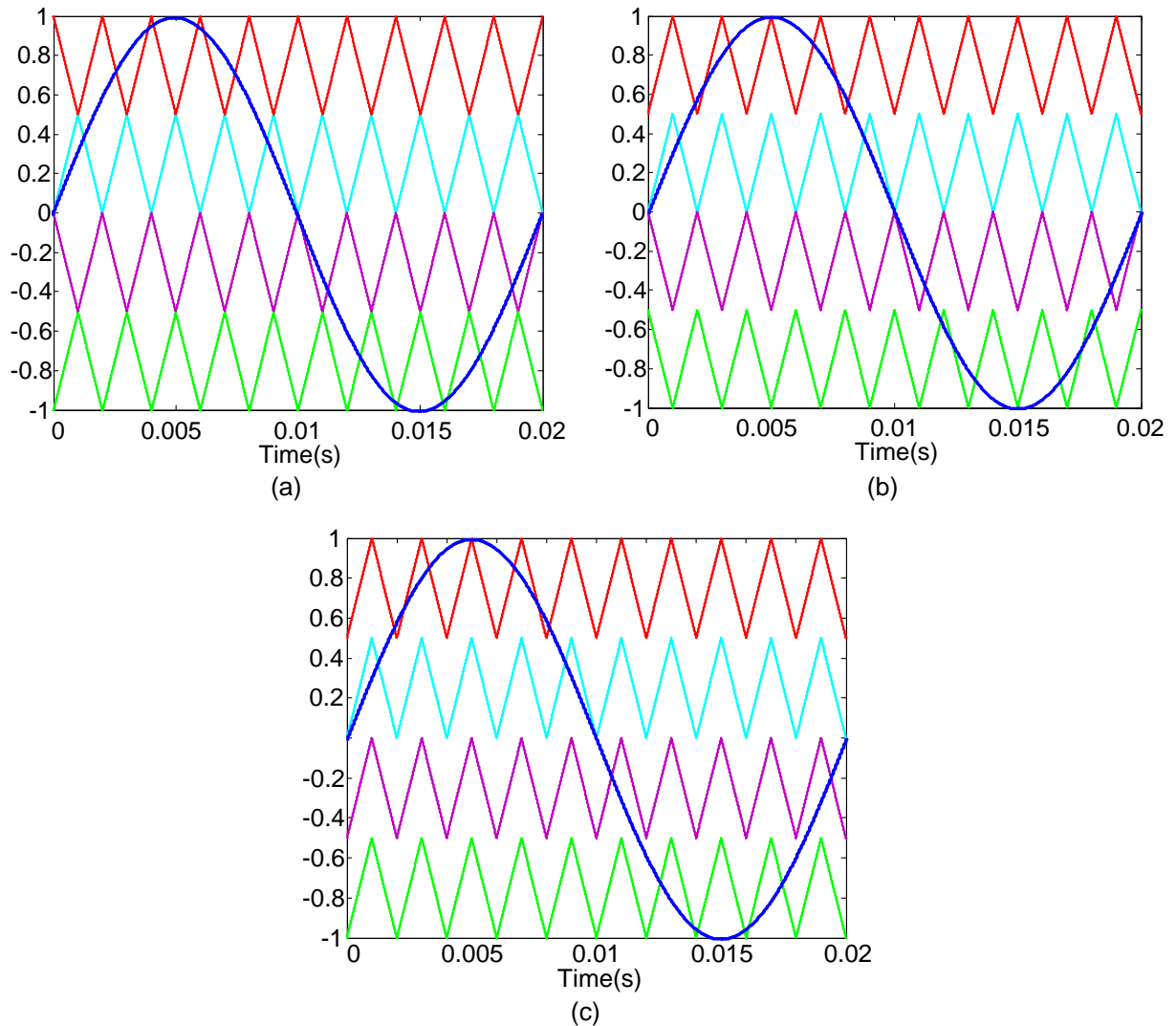
Fig.2.29. Examples of the three techniques. (a) APO, (b) PO and (c) PH.

In single-phase systems, the first two layouts of carriers (APO, PO) are the most interesting ones. This is because the spectra are not as concentrated as in the third layout, in which all modulation indices have a significantly large carrier frequency harmonic. In three-phase systems, on the other hand, the switching frequency harmonic is cancelled out when looking into the line-to-line voltages. Additionally, most of the remaining harmonics have lower amplitudes than with APO and PO. Consequently, the best carrier layout for three-phase systems is PH.

In the three-level NPC converter topology, the low-frequency voltage ripple that may appear at the NP occurs independently of the carrier layout used for the modulation. The NPC converter topology is characterized by ripples on dc-bus when

a high modulation index is applied. There are numerous works that analyze this problem (Newton and Sumner 1997, Ratnayake et al. 1999, Steinke 1992, Yo-Han et al. 1999).

2.3.5.6 Modified SPWM

The SPWM can be easily modified in order to obtain the maximum fundamental operation under lineal mode (Bowes and Yen-Shin 1997, Keliang and Danwei 2002, van der Broeck et al. 1988). It is 15% larger than the maximum achieved using standard SPWM. This modified SPWM will be used in the next chapters as a pattern to design new carrier modulation strategies.

The modulation signals for each phase (*a*, *b* and *c*) are modified to obtain an SVM pattern as follows:

$$\begin{cases} v_a' = v_a - v_0 \\ v_b' = v_b - v_0, \text{ and} \\ v_c' = v_c - v_0, \end{cases} \tag{2.21}$$

where $v_0 = \dfrac{\max(v_a, v_b, v_c) + \min(v_a, v_b, v_c)}{2}$.

Fig.2.30 shows the waveform of a phase modulation signal when the zero sequence component v_0 has been added.
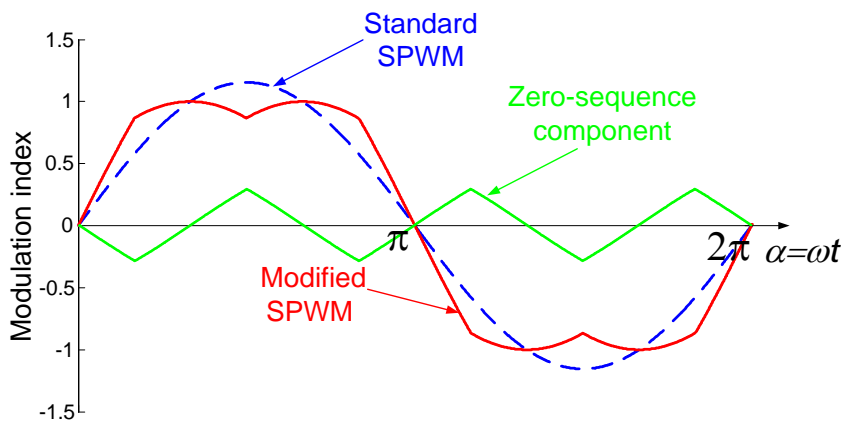
Fig.2.30. Modified SPWM.

The modulation index m_a defined in (2.19) considers that the modulation signals are sinusoidal. Therefore, under linear operation mode, m_a can take values within the

interval [0,1]. However, when using a proper zero-sequence injection, such as the one given in (2.21), the modulation signals are no longer sinusoidal. In this case, m_a can take values in the interval [0, 1.1547] and still make the converter operate under linear operation mode.

On the other hand, SVM adds a proper zero sequence to the output voltages spontaneously. Therefore, when the modulation index defined for SVM (m) takes the unity value, maximum benefit of the dc-link voltage is already achieved. This leads to the following relationship between the two indices:

$$m = \frac{\sqrt{3}}{2} m_a \qquad (2.22)$$

2.4. Conclusions of the Chapter

This chapter has shown the main multilevel topologies with special emphasis on the NPC converter, since most of the research performed in this dissertation is focused on this topology. Furthermore, a description of the set up used to obtain experimental results has been made.

Some general modulation issues are also presented in this chapter. In the case of the NPC converter, two particular modulation techniques are of significant relevance for some contributions developed in this thesis: the NTV and the virtual-vector modulations. The first one shows good NP voltage balance control for the whole range of linear modulation indices. However, some NP voltage oscillations appear under some operating conditions. On the other hand, the NTV modulation produces relatively low switching losses and the voltages generated contain low harmonic distortion. In the case of the second strategy (virtual-vector modulation), the NP voltage oscillations can be completely eliminated for all converter operating conditions. However, the number of switching events increases significantly and thus the switching losses also increase. Output voltages were also produced with higher harmonic distortion. Fortunately, this increment in the harmonic distortion is due to harmonics that are around and above the switching frequency; therefore, they can be easily attenuated with a filter or with the intrinsic inductors of an electrical motor. The virtual-vector modulation does not have a

natural NP voltage balance, therefore some voltage balancing control should be included in the modulation algorithm.

Both modulation strategies were originally developed from an SVM perspective, but they could be implemented from a carrier-based standpoint.

2.4. Chapter References

Bowes SR, Yen-Shin L. 1997. The relationship between space-vector modulation and regular-sampled PWM. Industrial Electronics, IEEE Transactions on 44: 670-679.

Bum-Seok S, Dong-Seok H. 1997. A new n-level high voltage inversion system. Industrial Electronics, IEEE Transactions on 44: 107-115.

Busquets-Monge S, Bordonau J, Boroyevich D, Somavilla S. 2004. The nearest three virtual space vector PWM - a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter. Power Electronics Letters, IEEE 2: 11-15.

Busquets-Monge S, Alepuz S, Bordonau J, Peracaula J. 2008. Voltage Balancing Control of Diode-Clamped Multilevel Converters With Passive Front-Ends. Power Electronics, IEEE Transactions on 23: 1751-1758.

Carrara G, Gardella S, Marchesoni M, Salutari R, Sciutto G. 1992. A new multilevel PWM method: a theoretical analysis. Power Electronics, IEEE Transactions on 7: 497-505.

Keliang Z, Danwei W. 2002. Relationship between space-vector modulation and three-phase carrier-based PWM: a comprehensive analysis [three-phase inverters]. Industrial Electronics, IEEE Transactions on 49: 186-196.

Li L, Czarkowski D, Yaguang L, Pillay P. 2000. Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters. Industry Applications, IEEE Transactions on 36: 160-170.

Manjrekar MD, Steimer PK, Lipo TA. 2000. Hybrid multilevel power conversion system: a competitive solution for high-power applications. Industry Applications, IEEE Transactions on 36: 834-841.

Marchesoni M, Tenca P. 2001. Theoretical and Practical Limits in Multilevel MPC Inverters with Passive Front Ends. EPE'01. Graz, Austria.

Marchesoni M, Mazzucchelli M, Tenconi S. 1990. A nonconventional power converter for plasma stabilization. Power Electronics, IEEE Transactions on 5: 212-219.

Meynard TA, Foch H. 1992a. Multi-level conversion: high voltage choppers and voltage-source inverters. Pages 397-403 vol.391. Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE.

—. 1992b. Multi-level choppers for high voltage application. EPE Journal 2: 45-50.

N. Mohan, T. Undeland, Robbins W. 2003. Power Electronics: Converters, Applications and Design

Nabae A, Takahashi I, Akagi H. 1981. A New Neutral-Point-Clamped PWM Inverter. Industry Applications, IEEE Transactions on IA-17: 518-523.

Newton C, Sumner M. 1997. Neutral point control for multi-level inverters: theory, design and operational limitations. Pages 1336-1343 vol.1332. Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE.

Pou J. 2002. Modulation and Control of Three-Phase PWM Multilevel ConvertersUniversitat Politècnica de Catalunya, Terrassa.

Pou J, Pindado R, Boroyevich D. 2005a. Voltage-balance limits in four-level diode-clamped converters with passive front ends. Industrial Electronics, IEEE Transactions on 52: 190-196.

Pou J, Pindado R, Boroyevich D, Rodriguez P. 2005b. Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter. Industrial Electronics, IEEE Transactions on 52: 1582-1588.

Pou J, Rodriguez P, Boroyevich D, Pindado R, Candela I. 2005c. Efficient Space-Vector Modulation Algorithm for Multilevel Converters with Low Switching Frequencies in the Devices. Pages 2521-2526. Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th.

Pou J, Rodriguez P, Sala V, Busquets-Monge S, Boroyevich D. 2005d. Algorithm for the virtual vectors modulation in three-level inverters with a voltage-balance control loop. Pages 9 pp.-P.9. Power Electronics and Applications, 2005 European Conference on.

Pou J, Zaragoza J, Rodriguez P, Ceballos S, Sala VM, Burgos RP, Boroyevich D. 2007. Fast-Processing Modulation Strategy for the Neutral-Point-Clamped Converter With Total Elimination of Low-Frequency Voltage Oscillations in the Neutral Point. Industrial Electronics, IEEE Transactions on 54: 2288-2294.

Prats MM, Franquelo LG, Portillo R, Leon JI, Galvan E, Carrasco JM. 2003. A 3-D space vector modulation generalized algorithm for multilevel converters. Power Electronics Letters, IEEE 1: 110-114.

Ratnayake KRMN, Murai Y, Watanabe T. 1999. Novel carrier PWM scheme to control neutral point voltage fluctuations in three-level voltage source inverter. Pages 663-667 vol.662. Power Electronics and Drive Systems, 1999. PEDS '99. Proceedings of the IEEE 1999 International Conference on.

Rodriguez J, Jih-Sheng L, Fang Zheng P. 2002a. Multilevel inverters: a survey of topologies, controls, and applications. Industrial Electronics, IEEE Transactions on 49: 724-738.

Rodriguez J, Moran L, Correa P, Silva C. 2002b. A vector control technique for medium-voltage multilevel inverters. Industrial Electronics, IEEE Transactions on 49: 882-888.

Rodriguez J, Moran L, Pontt J, Correa P, Silva C. 2003. A high-performance vector control of an 11-level inverter. Industrial Electronics, IEEE Transactions on 50: 80-85.

Rodriguez P, Pou J, Luna A, Ghizoni D, Guo J, Francis G, Burgos R, Boroyevich D. 2005. Three-dimensional SVM for modular power electronics systems. Pages 6 pp. Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE.

Schibli NP, Tung N, Rufer AC. 1998. A three-phase multilevel converter for high-power induction motors. Power Electronics, IEEE Transactions on 13: 978-986.

Sirisukprasert S, Jih-Sheng L, Tian-Hua L. 2002. Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters. Industrial Electronics, IEEE Transactions on 49: 875-881.

Steinke JK. 1992. Switching frequency optimal PWM control of a three-level inverter. Power Electronics, IEEE Transactions on 7: 487-496.

van der Broeck HW, Skudelny HC, Stanke GV. 1988. Analysis and realization of a pulsewidth modulator based on voltage space vectors. Industry Applications, IEEE Transactions on 24: 142-150.

Xiaoming Y, Barbi I. 2000. Fundamentals of a new diode clamping multilevel inverter. Power Electronics, IEEE Transactions on 15: 711-718.

Yo-Han L, Rae-Young K, Dong-Seok H. 1999. A novel SVPWM strategy considering DC-link balancing for a multi-level voltage source inverter. Pages 509-514 vol.501. Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual.

Chapter

3.

A Carrier-Based PWM Strategy with Zero-Sequence Voltage Injection

Several PWM strategies have been proposed and extensively investigated in order for the three-level NPC converter to achieve the following main objectives:

- to carry out the voltage balancing task of the dc-link capacitors, which is the primary technical challenge of the NPC converter, and

- to eliminate the low-frequency oscillations of the neutral point voltage, which appear under certain operating conditions and, if not mitigated, impose stress on the converter components.

The proposed PWM strategies for a three-level NPC are mainly classified into the carrier-based PWM (CB-PWM) strategies and the SVM strategies. The CB-PWM strategies are mostly based on pure SPWM or an SPWM strategy in conjunction with

a zero-sequence voltage injection (Bowes and Yen-Shin 1997, Keliang and Danwei 2002, N. Mohan et al. 2003, van der Broeck et al. 1988). Compared with the SPWM strategy, inclusion of a zero-sequence voltage extends the linear modulation range of the converter.

The existing CB-PWM strategies do not provide natural voltage balancing; therefore, additional control effort is required in order to control and balance the voltages (Carpita et al. 2008, Franquelo et al. 2008). The additional control effort imposes relatively high switching frequencies in the switching devices and also distorts the ac-side voltage spectra (Bruckner and Holmes 2005, Chenchen and Yongdong 2008, McMurray 1969, Newton and Sumner 1997). In the technical literature, there has been neither a proposal nor any investigation into a CB-PWM strategy with a proper zero-sequence voltage that (i) autonomously carries out the voltage balancing task, with no requirement for additional control effort, (ii) reduces the switching frequency, and (iii) mitigates the low-frequency voltage oscillations of the NP.

This chapter proposes a CB-PWM strategy for a three-level NPC converter with a zero-sequence voltage injection. The proposed strategy explores and exploits the duality between the NTV-SVM strategy (Keliang and Danwei 2002, Pou et al. 2002, Pou et al. 2005) and the CB-PWM strategy with a zero-sequence voltage injection. A theoretical basis for the proposed CB-PWM strategy has been developed, based on the analysis of the NTV-SVM strategy. Salient features of the proposed scheme as compared with the NTV-SVM strategy are:

- Its computational efficiency since it does not require NTV-SVM calculations and reduces the required processing time for digital implementation, and

- its reduced switching losses because the four-step switching sequences are avoided.

Comparing the proposed scheme and the existing CB-PWM strategies, not only the switching losses are reduced but it also has superior capability to balance the capacitor voltages.

Based on time-domain simulation studies in the MATLAB/SIMULINK environment, the performance of the proposed CB-PWM strategy for a three-level NPC is evaluated and experimentally verified.

3.1. Proposed CB-PWM Strategy

The three-level NPC of Fig.3.1 has 27 switching states in the *αβ* frame. A two-layer hexagon, centered at the origin of the plane, identifies the space voltage vectors (Fig.3.2). The switching states are illustrated by -1, 0, and 1, which denote the corresponding voltage levels of $-V_{dc}/2$, 0, and $V_{dc}/2$ with respect to the NP, as shown in Fig.3.1. At any sampling instant, the tip of the voltage vector $\vec{V}_{REF}$ is located in a triangle formed by the NTV adjacent to the voltage vector (Fig.3.2). The three adjacent switching vectors constitute the best choice for synthesizing the reference voltage vector.
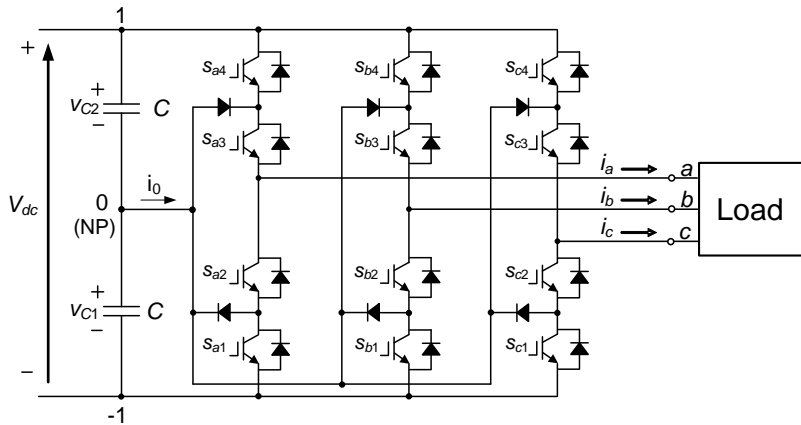
Fig.3.1. NPC converter.
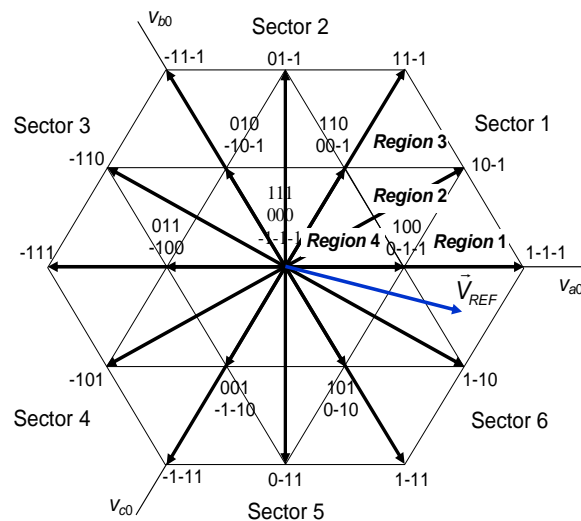
Fig.3.2. SV diagram of the NPC converter.

The determination of the adjacent switching vectors and calculation of their corresponding duty cycles are explained in Chapter 2. Subsequently, the next step is to identify the appropriate switching states and generate the switching sequence that controls capacitor voltages.

Through proper selection of short vectors (i.e., 0-1-1/100, 00-1/110, -10-1/010, -100/011, -1-10/001, and 0-10/101), the voltage balancing task of the dc-link capacitors is carried out. The short vectors provide redundant switching states and generate the same line-to-line ac-side voltage. However, they provide currents flow into the NP from the opposite direction. For instance, Vector 0-1-1 imposes current i_a to the NP ($i_0=i_a$), while Vector 100 imposes the same current in the NP but in the opposite direction ($i_0=-i_a$). Adding one level to all three integer numbers that define the "low" short vectors (i.e., 0-1-1, 00-1, -10-1, -100, -1-10, and 0-10) results in the "high" short vectors (i.e., 100, 110, 010, 011, 001, and 101, respectively). Note that applying the "low" vectors results in having one or two phases connected to the lower dc-link rail, while the "high" vectors connect one or two phases to the higher dc-link rail. In any case, the line-to-line voltages do not depend on the specific vector which is applied from a set of redundant vectors.

To analyze the NTV-SVM in detail and explore a correlation between it and the CB-PWM with a zero-sequence voltage injection, only Sector 1 is considered; then, based on minor adjustments, the analysis is generalized for all sectors.

Table 3.1 shows all possible switching sequences in Sector 1 for the NTV strategy. Throughout each sampling period, the NTVs are selected and —based on the voltage balancing criteria— the appropriate short vector/vectors are selected. Then, with the objective of minimizing switching frequency, the optimal switching sequences are determined. With the same objective, the switching sequences are flipped afterwards so that there are no switching events in the sequence transitions. In Table 3.1, the so-called "Increasing Sequences" are the ones in which the indices of the vectors increase throughout the sequence; the following "Decreasing Sequences" are those where the indices decrease. Based on the various switching sequences presented in Table 3.1, one phase does not change its switching state in

most cases. This is a salient feature of the NTV strategy which, in comparison with the other SVM strategies, reduces the switching frequency of the switching devices.

In a CB-PWM strategy for a three-level NPC, two carrier waveforms are displaced symmetrically with respect to the zero axis. The switching signals are generated by comparing the sinusoidal modulating waveform with the carrier waveforms as shown in Fig.3.3. When one phase does not switch in SVM strategy, it is equivalent to maintaining the corresponding modulation reference signal clamped to one, zero, or minus one (1, 0, -1) throughout the entire PWM cycle. For example, to clamp phase *a* to one (the higher dc-link rail), the corresponding modulation signal should be maintained as equal to one. To clamp the ac-side voltages to a particular voltage level, a zero-sequence signal can be added to the sinusoidal modulation reference signals. As an example, Fig.3.3 shows that a zero-sequence signal, v_{off}, is added to the sinusoidal modulation reference signals and, as a result, the modulation signals are clamped at one during some intervals. Thus, each phase does not switch during the corresponding interval. Since only a zero-sequence signal is added to the sinusoidal waveforms, the line-to-line sinusoidal voltages are preserved. However, the NP current is affected by the injection of the zero-sequence signal. Therefore, a proper injected signal can assist in carrying out the voltage balancing task.

The relationship between the locally-averaged NP current and the modulation signals is as follows:

$$\bar{i}_0 = \left(1 - \left|v_a^{'}\right|\right) i_a + \left(1 - \left|v_b^{'}\right|\right) i_b + \left(1 - \left|v_c^{'}\right|\right) i_c, \tag{3.1}$$

where the modulation signals $v_i^{'}$ for $i=\{a, b, c\}$ are $v_i^{'} = v_i + v_{off}$. v_i is the sinusoidal modulation reference signal and v_{off} is a signal common to the three phases.

In the NTV-SVM strategy, the short vectors are chosen based on the knowledge of phase currents and the impact of the short vectors on the NP. For instance, if during a sampling cycle, the tip of the reference vector is located within Region 1 and the lower dc-link capacitor of the NPC of Fig.3.1 has a higher voltage level than the upper one, $v_{C1} > v_{C2}$, the NP current must be positive ($i_0 > 0$) in order to decrease the NP voltage. Therefore, Vector 0-1-1 should be selected if i_a is positive. Otherwise, Vector 100 is selected. If Vector 0-1-1 is selected, the sequence of vectors in Region

1 would be 0-1-1/1-1-1/10-1 and, as a result, phase *c* is clamped to minus one. Otherwise, if Vector 100 is chosen, the sequence of vectors would be 1-1-1/10-1/100 and, subsequently, phase *a* is clamped to one.

Table 3.1. Vector Sequences in Sector 1.

Region	Short Vectors	Sequences of Vectors (Increasing and Decreasing Sequences)	Switching Steps	No Switching Phases
1	0-1-1	0-1-1/1-1-1/10-1 // 10-1/1-1-1/0-1-1	2 // 2	*c* clamped to -1
	100	1-1-1/10-1/100 // 100/10-1/1-1-1	2 // 2	*a* clamped to 1
2	0-1-1/00-1	0-1-1/00-1/10-1 // 10-1/00-1/0-1-1	2 // 2	*c* clamped to -1
	0-1-1/110	0-1-1/10-1/110 // 110/10-1/0-1-1	4 // 4	None
	100/00-1	00-1/10-1/100 // 100/10-1/00-1	2 // 2	*b* clamped to 0
	100/110	10-1/100/110 // 110/100/10-1	2 // 2	*a* clamped to 1
3	00-1	00-1/10-1/11-1 // 11-1/10-1/00-1	2 // 2	*c* clamped to -1
	110	10-1/11-1/110 // 110/11-1/10-1	2 // 2	*a* clamped to 1
4	0-1-1/00-1	0-1-1/00-1/000 // 000/00-1/0-1-1	2 // 2	*a* clamped to 0
	0-1-1/110	0-1-1/000/110 // 110/000/0-1-1	4 // 4	None
	100/00-1	00-1/000/100 // 100/000/00-1	2 // 2	*b* clamped to 0
	100/110	000/100/110 // 110/100/000	2 // 2	*c* clamped to 0
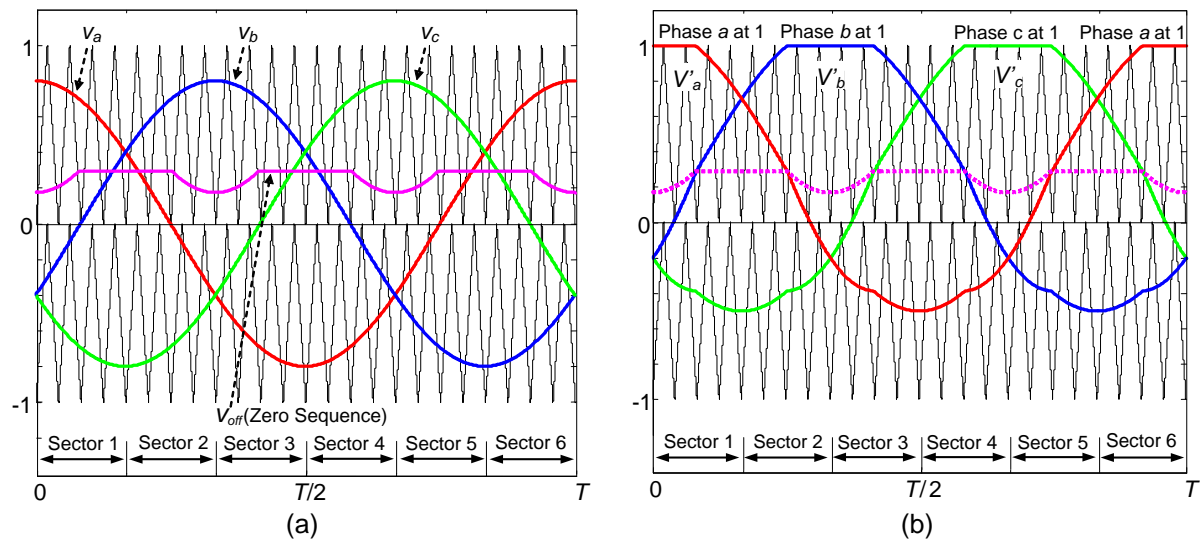
Fig.3.3. Modulation signals: (a) sinusoidal references, and (b) addition of a positive zero-sequence signal.

If the tip of the reference vector is located within Region 2, two short vectors should be selected: one from the pair of vectors 0-1-1 and 100; the other from the pair 00-1 and 110.

Fig.3.4 shows an example in which the v_{max} (v_a) is clamped to +1. In this case, the sequence of vectors generated would be 10-1/100/110; that is to say, the short vectors 100 and 110 are selected. The phase *a* current does not have any effect on the NP current, since it is defined by:

$$\bar{i}_0 = \left(1 - \left|v_b'\right|\right)i_b + \left(1 - \left|v_c'\right|\right)i_c. \tag{3.2}$$
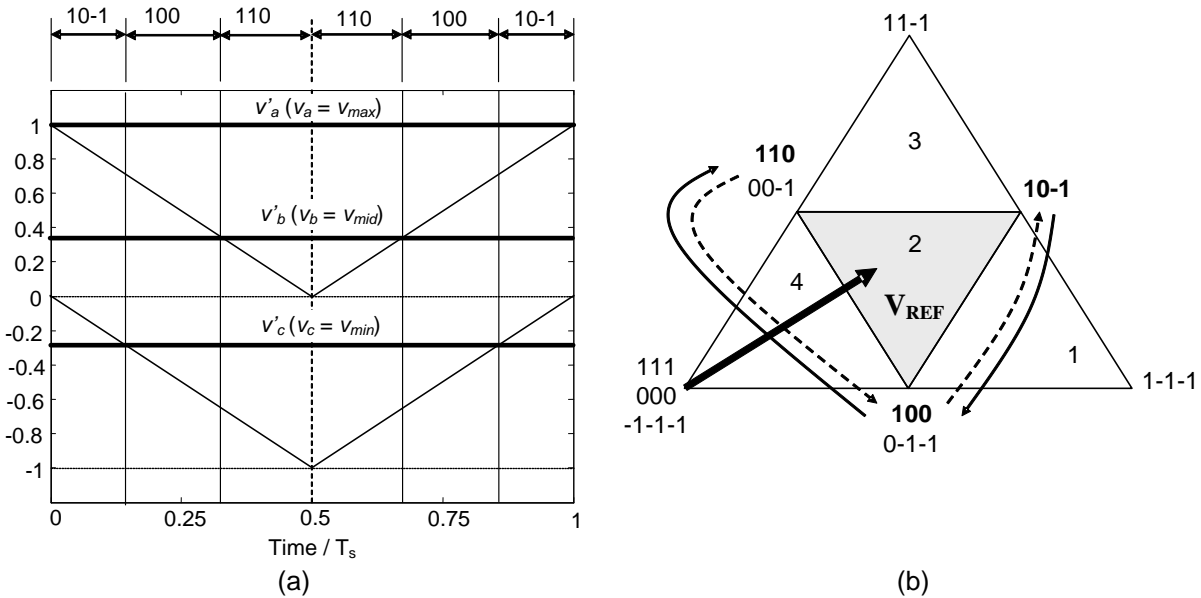
Fig.3.4. Co-relation between the CB-PWM and NTV-SVM strategy when phase *a* is clamped to +1: (a) CB-PWM switching sequence, and (b) NTV-SVM strategy.

Fig.3.5 shows an example in which the v_{mid} (v_b) is clamped to zero. In this case, the selected short vectors are 100 and 00-1; thus, the sequence of vectors is 00-1/10-1/100. The NP current is expressed by:

$$\bar{i}_0 = \left(1 - \left|v_a'\right|\right)i_a + i_b + \left(1 - \left|v_c'\right|\right)i_c. \tag{3.3}$$

In Fig.3.6, the modulation signal v_{min} (v_c) is clamped to -1. As a result, the short vectors 0-1-1 and 00-1 are selected and the switching sequence is 0-1-1/00-1/10-1. In this case, the phase *c* current does not affect the NP current, as the current is expressed by:

$$\bar{i}_0 = \left(1 - \left|v_a'\right|\right)i_a + \left(1 - \left|v_b'\right|\right)i_b. \tag{3.4}$$
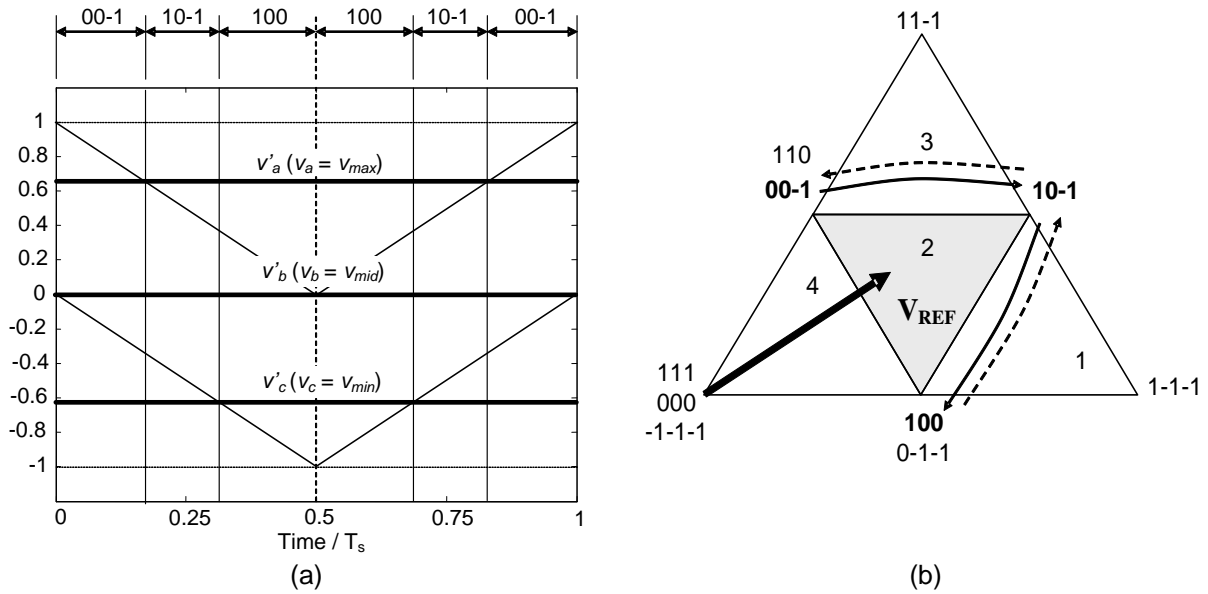
Fig.3.5. Co-relation between the CB-PWM and NTV-SVM strategy when phase *b* is clamped to 0: (a) CB-PWM switching sequence, and (b) NTV-SVM strategy.
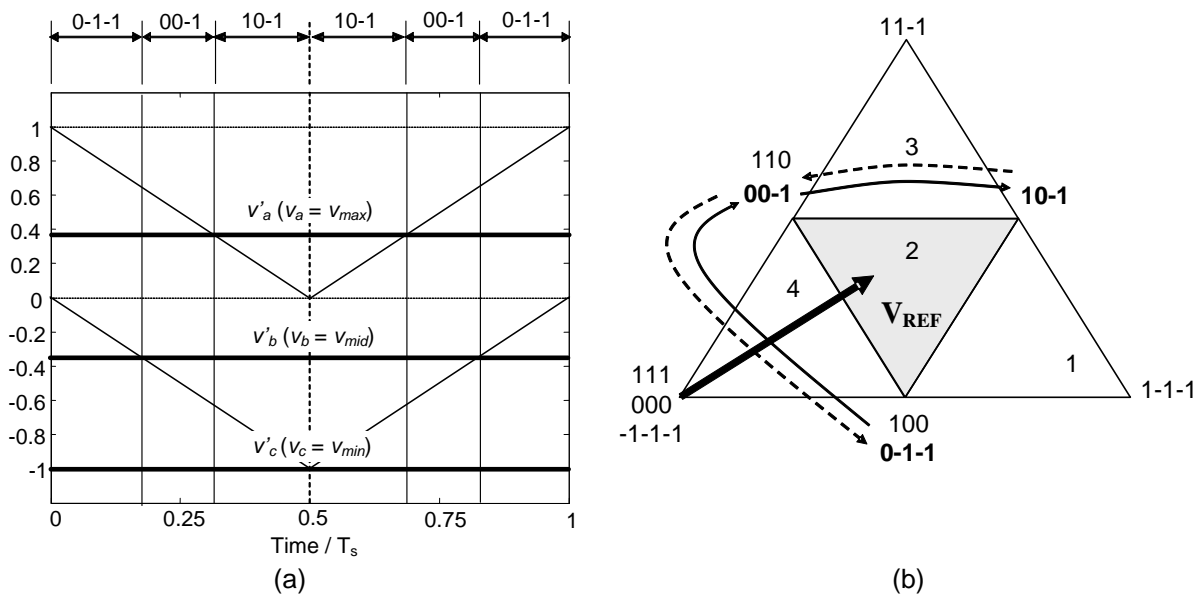
Fig.3.6. Co-relation between the CB-PWM and NTV-SVM strategy when phase *c* is clamped to -1: (a) CB-PWM switching sequence, and (b) NTV-SVM strategy.

The remaining combination to consider for Region 2 is the case when the short vectors 0-1-1 and 110 are selected. In this case, the optimal sequence of vectors is 0-1-1/10-1/110. As observed in the switching sequence, none of the converter phases is clamped. Furthermore, two converter phases switch one level at the same time. This means that the modulation signals should jump within a PWM cycle. Since

implementation of this case from a carrier-based standpoint is difficult and unpractical, a different criterion will be applied for this particular case in order to balance the voltages.

Based on the analysis of all possibilities for large modulation indices (in which the tip of the reference vector is located in one of the Regions 1, 2, or 3) and by exploring the co-relations between the modulation signals which correspond to the NTV-SVM and the CB-PWM strategy, the following conclusions can be made:

- Only a maximal modulation signal (v_{max}) can be clamped to +1. Similarly, a minimal modulation signal (v_{min}) can be clamped to -1. The median modulation signal (v_{mid}) can be clamped to 0, provided no signal escapes from the margin [+1, -1].

- If the sign of one ac-side current is not appropriate for balancing the voltage, the modulation signal of that phase should be clamped to +1 or -1 if it corresponds to v_{max} or v_{min}, respectively.

- When one output phase current has the proper direction to help balance the voltage, the corresponding modulation signal should be clamped to 0 if it is v_{mid}, but not to +1 or -1 if it is v_{max} or v_{min}, respectively.

- If the two ac-side currents corresponding to the modulation signals v_{max} and v_{min} help to balance the voltage, the ac-side current associated to v_{mid} carries a current that is not appropriate for voltage balancing. Therefore, v_{mid} should be shifted as far as possible from zero. This is usually achieved by clamping v_{max} to +1 or v_{min} to -1, for $v_{mid}>0$ or $v_{mid}\leq0$, respectively. This resolution is the only one which is determined different from the NTV SP-PWM strategy/method. Because of this, the sequences that require four switching steps in Table 3.1 are avoided.

The above-mentioned conclusions are mathematically summarized in Table 3.2, where $\varDelta v_{NP}$ is the voltage difference v_{C1}-v_{C2}. State conditions 1 and 0 indicate true and false, respectively.

Table 3.2. Actions to Help Balance the Voltage.

Sector 1 and [Sector 4]			
$\Delta v_{NP}\, i_a{>}0$	$\Delta v_{NP}\, i_c{>}0$	Action	Offset (v_{off})
0	0	b Clamped to 0	$-v_b$
0	1	a Clamped to +1 [−1]	$+1-v_a$ [$-1-v_a$]
1	0	c Clamped to −1 [+1]	$-1-v_c$ [$+1-v_c$]
1	1	For $v_b{>}0$: a Clamped to +1 [c Clamped to +1] For $v_b{\leq}0$: c Clamped to −1 [a Clamped to −1]	For $v_b{>}0$: $+1-v_a$ [$+1-v_c$] For $v_b{\leq}0$: $-1-v_c$ [$-1-v_a$]

Sector 2 and [Sector 5]			
$\Delta v_{NP}\, i_b{>}0$	$\Delta v_{NP}\, i_c{>}0$	Action	Offset (v_{off})
0	0	a Clamped to 0	$-v_a$
0	1	b Clamped to +1 [−1]	$+1-v_b$ [$-1-v_b$]
1	0	c Clamped to −1 [+1]	$-1-v_c$ [$+1-v_c$]
1	1	For $v_a{>}0$: b Clamped to +1 [c Clamped to +1] For $v_a{\leq}0$: c Clamped to −1 [b Clamped to −1]	For $v_a{>}0$: $+1-v_b$ [$+1-v_c$] For $v_a{\leq}0$: $-1-v_c$ [$-1-v_b$]

Sector 3 and [Sector 6]			
$\Delta v_{NP}\, i_b{>}0$	$\Delta v_{NP}\, i_a{>}0$	Action	Offset (v_{off})
0	0	c Clamped to 0	$-v_c$
0	1	b Clamped to +1 [−1]	$+1-v_b$ [$-1-v_b$]
1	0	a Clamped to −1 [+1]	$-1-v_a$ [$+1-v_a$]
1	1	For $v_c{>}0$: b Clamped to +1 [a Clamped to +1] For $v_c{\leq}0$: a Clamped to −1 [b Clamped to −1]	For $v_c{>}0$: $+1-v_b$ [$+1-v_a$] For $v_c{\leq}0$: $-1-v_a$ [$-1-v_b$]

If the reference vector is located within Region 4 (i.e., when the modulation index is low), a different clamping criterion is adopted. In this case, as shown in Table 3.1, only the NP voltage is considered for clamping. From the CB-PWM point of view, the amplitude of the modulation signals is small and, thus, any of the modulation signals can be clamped to the NP voltage without compromising the linear modulation range. Furthermore, under low modulation indices, clamping the modulation signals to zero requires less zero sequence voltage amplitude, i.e., v_{off} and fewer carrier crossing transitions compared to clamping them to +1 or -1. To decide which modulation

signal should be clamped to the NP, all of the three phases ($\Delta v_{NP} i_x$, $x=\{a,b,c\}$ are calculated and evaluated. The maximum calculated value specifies the modulation signal that has to be clamped to the NP. For example, if at a specific sampling instant, the product $\Delta v_{NP} i_a$ is larger than $\Delta v_{NP} i_b$ and $\Delta v_{NP} i_c$, then the modulation signal v_a is clamped to zero because phase *a* carries the best balancing current for the NP voltage balance. In this strategy, the four-step switching transition sequences are avoided and, as shown in Table 3.1, only the two-step ones are considered.

In specifying the maximum and minimum values of the modulating signals, the corresponding sector —within which the tip of the reference vector is located— is simply determined as shown in Fig.3.3. For example, if the reference vector is in Sector 1, the modulating signal v_a is the maximum and v_c is the minimum. For Sector 2, v_b is the maximum and v_c is the minimum. The different cases for the all sectors are shown in Table 3.3.

The procedure for implementing the proposed CB-PWM with the zero sequence modulation signal is summarized in the diagram of Fig.3.7. The process outlined in this section determines the required zero sequence signal that needs to be added to the sinusoidal reference waveforms of the CB-PWM strategy in order to generate the equivalent of the NTV-SVM strategy.

Table 3.3. Determination of the Sector.

v_{max}	v_{min}	Sector
v_a	v_c	1
v_b	v_c	2
v_b	v_a	3
v_c	v_a	4
v_c	v_b	5
v_a	v_b	6
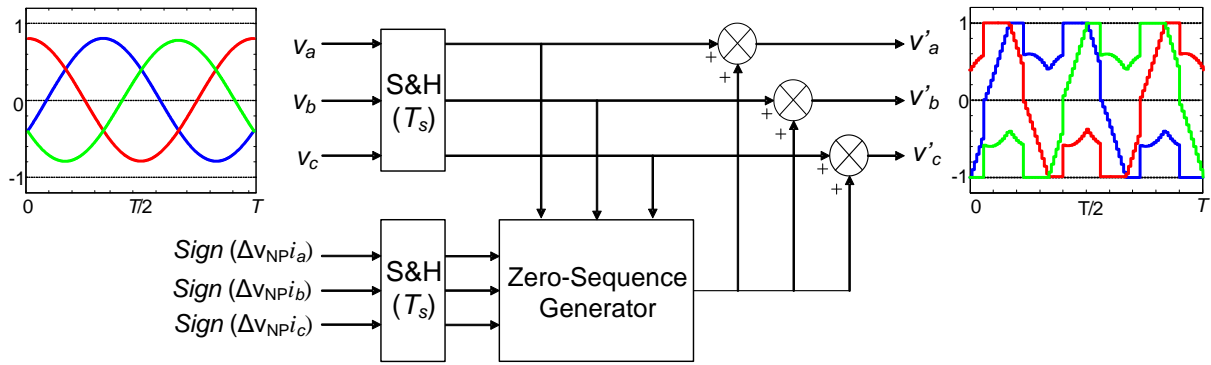
Fig.3.7. Modification of the modulation signals by adding the proposed zero-sequence signal to balance the voltage.

3.2. Simulation Results

CB-PWM waveforms and Total Harmonic Distortion analysis

The CB-PWM is initially implemented and tested by simulation using the MATLAB/SIMULINK software. The values for all these simulation examples are: V_{dc}=1,800 V and a resistive-inductive Wye-connected load with R=1 Ω and L=2 mH, respectively. The value for the dc-link capacitors is C=2,200 µF and the fundamental frequency of the ac voltage is f=50 Hz. The values of the THD and WTHD given in the figures consider the definitions D1 and D2 (Appendix D).

Fig.3.8 shows the voltage of the dc-link capacitors (v_{C1} and v_{C2}), a line-to-line voltage (v_{ab}) and the output currents (i_a, i_b, and i_c) when the converter operates under a carrier frequency of f_s=5 kHz. The low-frequency oscillation amplitude in the dc-link capacitors is largely mitigated in most of the modulation indices. Note, however, that

(a)

(b)

(c)

(d)
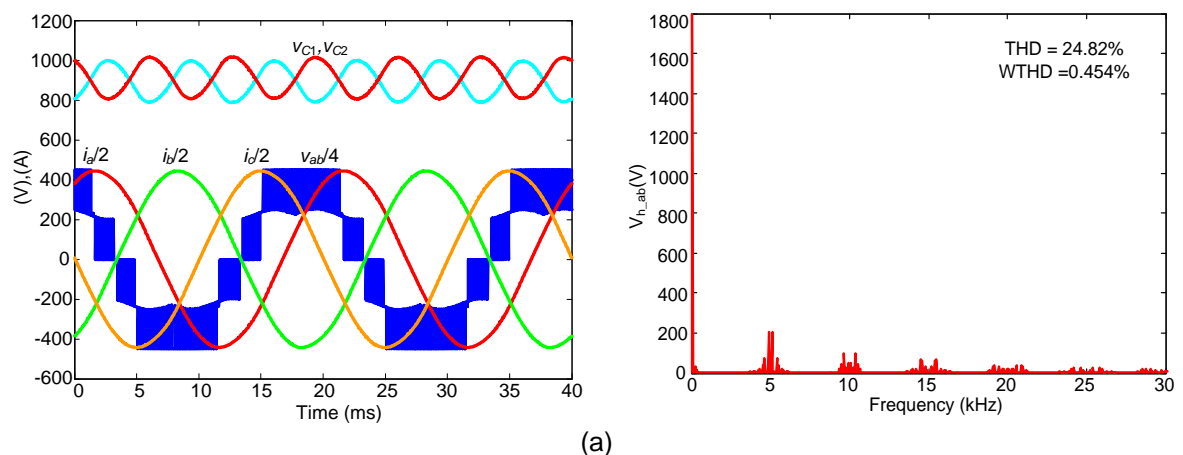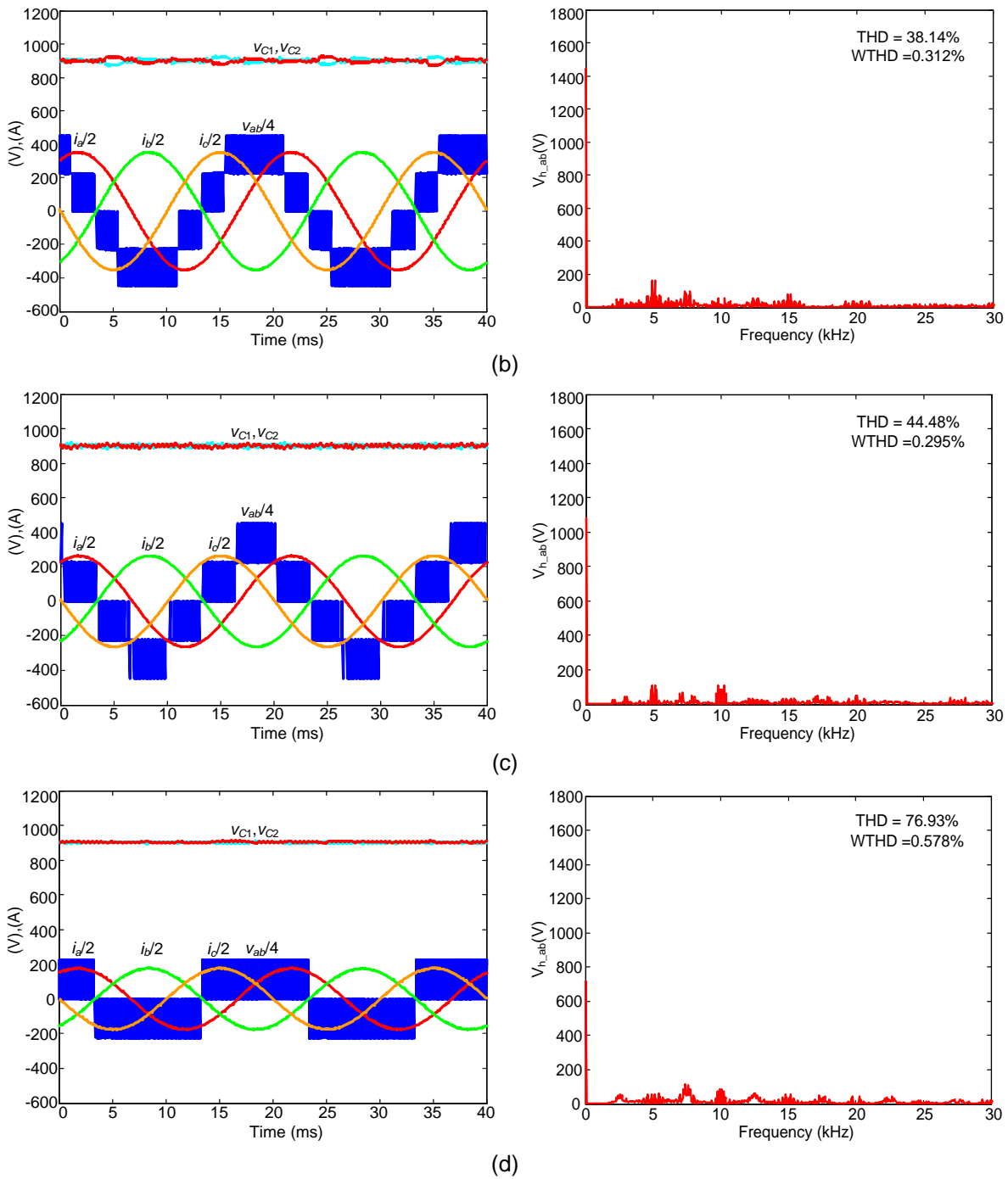
Fig.3.8. Simulation results of the proposed CB-PWM: (a) *m*=1; (b) *m*=0.8; (c) *m*=0.6; (d) *m*=0.4.

for high modulation indices, similar low-frequency oscillations appear. This is because less magnitude of the zero sequence can be applied; therefore, there is less control over the NP voltage balance. As expected, the THD value increases when the modulation index decreases. This is mostly due to the fact that the RMS value of the fundamental is divided in the definition of the THD (D1). The WTHD value performs

differently; this is because this parameter not only considers the harmonic contents of the waveforms but also their position in the spectrum.

The balancing process is shown in Fig.3.9, where the initial voltages in the dc-link capacitors are unbalanced. Observe that the voltages become equal very quickly.
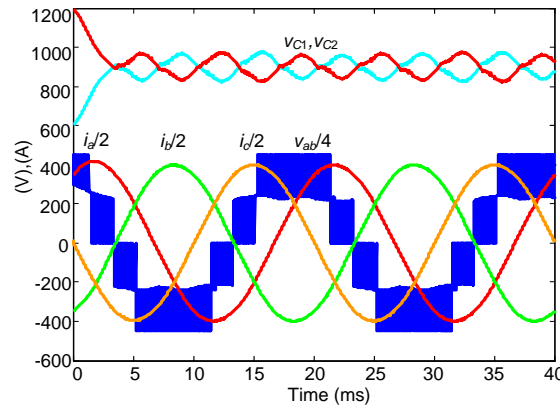
Fig.3.9. Dynamics of the voltage compensator operating on a linear load (*m*=0.9).

Loss analysis

A MATLAB/SIMULINK model of an NPC converter has been developed to calculate losses. The converter rated power is 2.8 MVA (1,700 V / 950 A, V_{dc}=2,400 V). In all simulations, the ac output currents are assumed to be steady at their rated values and the sampling frequency is f_s=5 kHz (carriers' frequency).

The IGBTs selected are the DIM1200NSM17-E000, whose maximum ratings are a forward current of 1,200 A and a direct voltage of 1,700 V. In the following analysis, the IGBT model is based on the typical curves given by the manufacturer. The main parameters used to calculate the conduction and switching losses of these IGBTs are given in Appendix C. Also, the method used to calculate the mean value of the conduction and switching losses in a power device are given and explained in the same appendix.

Fig.3.10 shows the ratio of the total losses when the converter operates using the proposed CB-PWM strategy as compared to the SPWM and NTV-SVM strategies. As Fig.3.10 (a) shows, the resulting total losses of the proposed CB-PWM strategy are smaller than those produced by the SPWM strategy for all operating conditions. The reason is that in the SPWM strategy none of the modulation signals is clamped and

consequently the switching losses are significantly higher. Fig.3.10(b) compares power losses of the proposed CB-PWM strategy to those of the NTV-SVM strategy. Observe that for some operating conditions, the ratio of the total power losses is the unity, which means they produce equal losses. However, for some other operating conditions the ratio is lower, which means that the proposed CB-PWM produces fewer losses than the original NTV-PWM. This is because, in the CB-PWM strategy, the use of the four-step transition sequences are avoided. Thus, it produces lower switching losses.
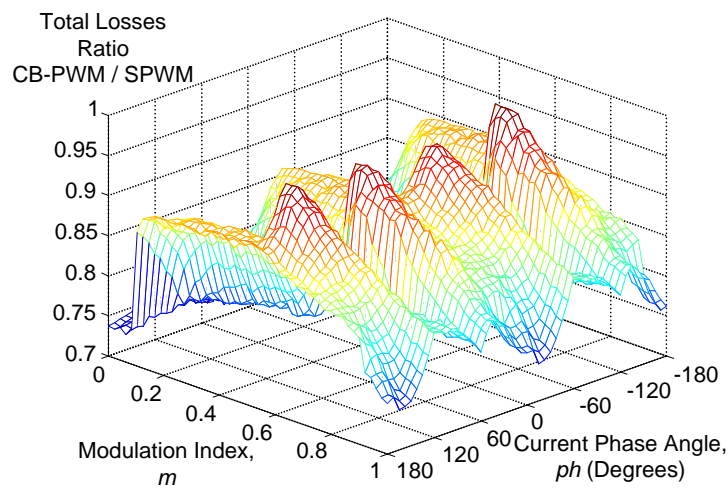
(a)
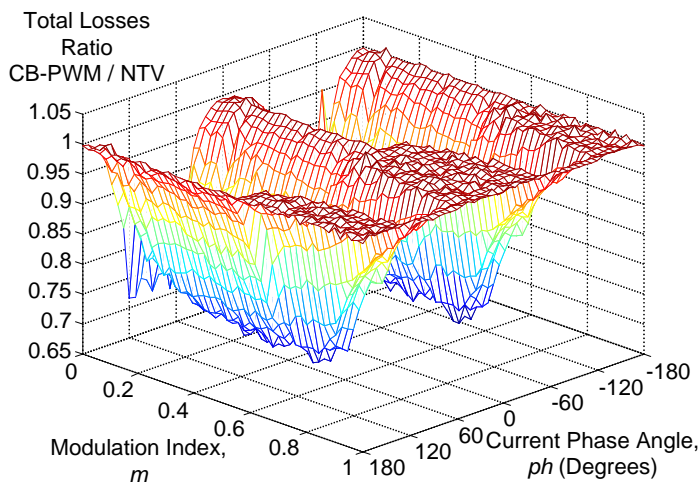
(b)

Fig.3.10 Total losses ratio of the proposed CB-PWM to those of (a) the SPWM strategy, and (b) the NTV-SVM strategy.

NP Voltage oscillations

The maximum low-frequency NP voltage amplitudes that occur under specific operating conditions of the converter are analyzed. The normalized amplitude of the ripple ($\Delta V_{NPn}/2$) is defined by (E1) and the conditions used to calculate the normalized low frequency oscillation is provided in Appendix E.

Fig.3.11 illustrates and compares the low-frequency NP voltage oscillations for both the SPWM and the proposed CB-PWM strategies. Fig.3.11(a) shows the NP voltage amplitude when the NPC converter operates based on the SPWM strategy. As

(a)

(b)
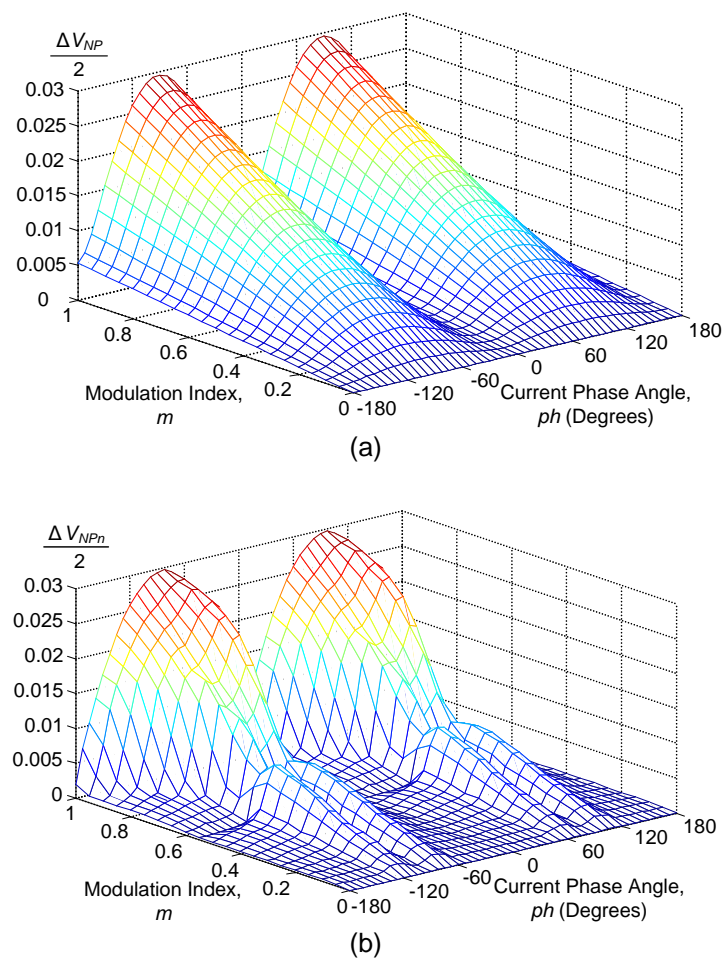
Fig.3.11. Normalized amplitude of the low-frequency NP voltage oscillations produced by: (a) the SPWM strategy, and (b) the proposed CB-PWM strategy.

shown, under any operating condition, there exist low-frequency oscillations on the NP voltage. In contrast, the proposed CB-PWM strategy obviates the oscillations for

an extensive range of operating conditions, as shown in Fig.3.11(b). As expected, these results are similar to those obtained from the NTV-SVM strategy (Celanovic and Boroyevich 2000, Pou et al. 2005). The main difference is that the proposed CB-PWM cannot fully cancel the low-frequency NP voltage oscillations when operating under low modulation indices. However, the amplitude of the oscillation is not significant, and the benefit of lowering switching losses is remarkable.

3.3. Experimental Results

The experimental evaluation of the proposed CB-PWM strategy for the three-level NPC converter in Fig.3.1 is performed using the 20-kVA scaled-down prototype presented in Section 2.4, with an averaged switching frequency of around 5 kHz. The converter is connected to a three-phase series RL load connected with R=11.5 Ω and L=12 mH to the ac side. The values of the dc-link voltage and the capacitors are V_{dc}=120 V and C=2,200 μF, respectively.

In Fig.3.12 the variables shown are a line-to-line output voltage (v_{cb}), the voltages on the dc-link capacitors (v_{C1} and v_{C2}), and the output currents (i_a, i_b, and i_c). The output frequency has been selected at 20 Hz in order to emphasize the low-frequency voltage oscillations in the dc-link capacitors. Observe that those oscillations appear to be operating under large modulation indices, which also happens when using the NTV modulation (Pou et al. 2005).

(c)
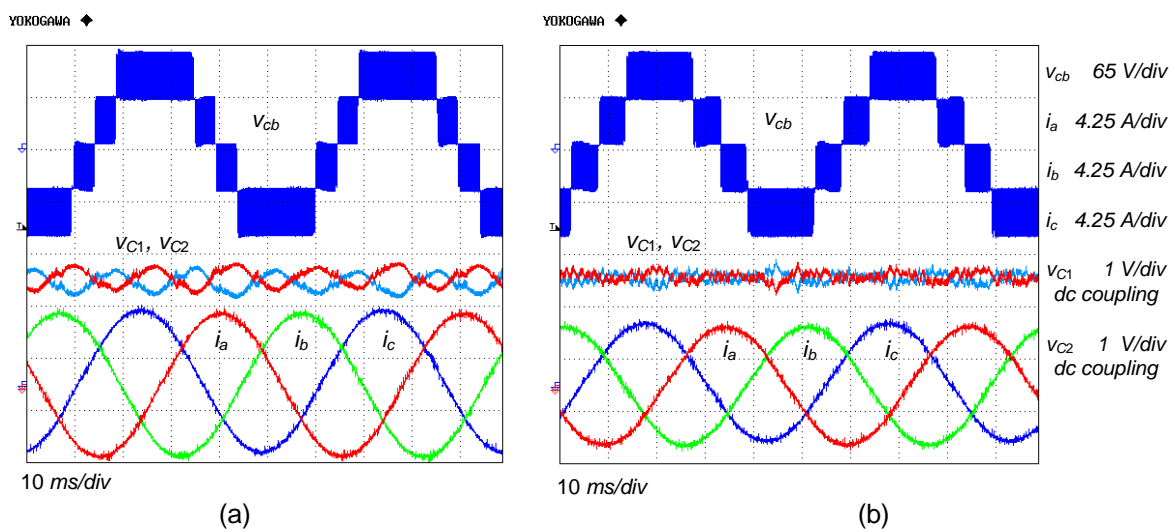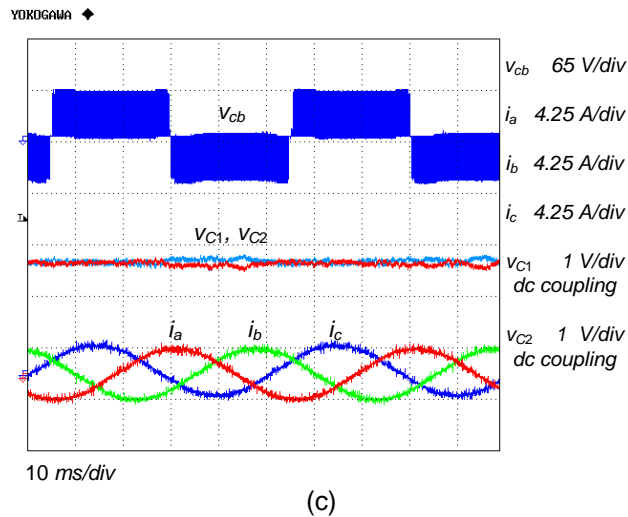
Fig.3.12. Experimental results for the proposed CB-PWM: (a) *m*=1, (b) *m*=0.7, and (c) *m*=0.4.

Fig.3.12 highlights the capability of the CB-PWM to mitigate the NP voltage oscillations, as compared with the SPWM strategy. This obviates the need for oversized NPC converter components. Fig.3.12 also proves the co-relation between the proposed strategy and the NTV-SVM strategy, since the NP voltage oscillations are mitigated in the NTV-SVM strategy as well (Pou et al. 2005, Zaragoza et al. 2009).

The effectiveness of the proposed CB-PWM strategy in balancing the voltage is shown in Fig.3.13. It shows how, after a short period of time, the capacitor voltages converge and settle at their nominal values. This shows that the proposed modulation strategy is capable of balancing the voltage fairly quickly, with no requirement for additional control effort.
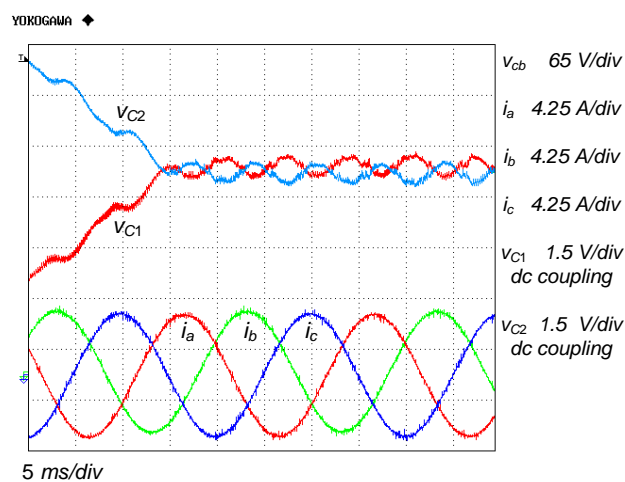
Fig.3.13. Dynamics of the voltage compensator operating over a linear load (*m*=1 and *f*=50Hz).

3.3. Conclusions of the Chapter

This chapter proposes a CB-PWM strategy in conjunction with a zero-sequence voltage injection for a three-level NPC converter. The obtained injected zero-sequence voltage is based on exploring the duality between the CB-SPWM and the NTV-SVM strategies. The proposed CB-PWM strategy is an alternative to the NTV-SVM strategy. Nevertheless, the main feature of this strategy, as compared with the NTV-SVM strategy, is its simplicity for digital implementation.

The salient features of the proposed CB-PWM strategy, as compared to the existing CB-PWM strategies, are as follows:

- It can operate at lower switching frequencies.

- It guarantees voltage balancing with no requirement for additional control effort.

- It mitigates the voltage oscillations of the NP voltage.

Simulation and experimental results show good performance of the proposed modulation strategy.

3.4. Chapter References

Bowes SR, Yen-Shin L. 1997. The relationship between space-vector modulation and regular-sampled PWM. Industrial Electronics, IEEE Transactions on 44: 670-679.

Bruckner T, Holmes DG. 2005. Optimal pulse-width modulation for three-level inverters. Power Electronics, IEEE Transactions on 20: 82-89.

Busquets-Monge S, Bordonau J, Boroyevich D, Somavilla S. 2004. The nearest three virtual space vector PWM - a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter. Power Electronics Letters, IEEE 2: 11-15.

Carpita M, Marchesoni M, Pellerin M, Moser D. 2008. Multilevel Converter for Traction Applications: Small-Scale Prototype Tests Results. Industrial Electronics, IEEE Transactions on 55: 2203-2212.

Celanovic N, Boroyevich D. 2000. A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. Power Electronics, IEEE Transactions on 15: 242-249.

Chenchen W, Yongdong L. 2008. A New Balancing Algorithm of Neutral-Point Potential in the Three-Level NPC Converters. Pages 1-5. Industry Applications Society Annual Meeting, 2008. IAS '08. IEEE.

Franquelo LG, Rodriguez J, Leon JI, Kouro S, Portillo R, Prats MAM. 2008. The age of multilevel converters arrives. Industrial Electronics Magazine, IEEE 2: 28-39.

Keliang Z, Danwei W. 2002. Relationship between space-vector modulation and three-phase carrier-based PWM: a comprehensive analysis [three-phase inverters]. Industrial Electronics, IEEE Transactions on 49: 186-196.

McMurray W. 1969. Fast response stepped-wave switching power converter circuit. US.

N. Mohan, T. Undeland, Robbins W. 2003. Power Electronics: Converters, Applications and Design

Newton C, Sumner M. 1997. Neutral point control for multi-level inverters: theory, design and operational limitations. Pages 1336-1343 vol.1332. Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE.

Pou J, Boroyevich D, Pindado R. 2002. New feedforward space-vector PWM method to obtain balanced AC output voltages in a three-level neutral-point-clamped converter. Industrial Electronics, IEEE Transactions on 49: 1026-1034.

Pou J, Pindado R, Boroyevich D, Rodriguez P. 2005. Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter. Industrial Electronics, IEEE Transactions on 52: 1582-1588.

van der Broeck HW, Skudelny HC, Stanke GV. 1988. Analysis and realization of a pulsewidth modulator based on voltage space vectors. Industry Applications, IEEE Transactions on 24: 142-150.

Zaragoza J, Pou J, Ceballos S, Robles E, Jaen C, Corbalan M. 2009. Voltage-Balance Compensator for a Carrier-Based Modulation in the Neutral-Point-Clamped Converter. Industrial Electronics, IEEE Transactions on 56: 305-314.

Chapter

4.

Carrier-Based PWM Using Two Modulation Signals per Phase

This chapter presents a novel modulation strategy for the NPC converter. This strategy overcomes one of the main problems of this type of converter, which is the low-frequency voltage oscillation that appears at the NP under some operating conditions. The proposed modulation strategy uses two modulation signals per phase, and it is the so-called double-signal PWM (DSPWM). It can completely remove the low-frequency voltage oscillations for all the operating points and for any kind of load, even unbalanced and nonlinear loads. Furthermore, this strategy can be implemented with a very simple algorithm, and hence can be processed very quickly. The algorithm is based on a carrier-based PWM. Nevertheless, it can generate the maximum output voltage amplitudes attainable under linear modulation, such as the SVM. However, the only drawback of this strategy is that the switching frequencies of the devices are one-third higher than a standard SPWM. Furthermore, it does not

provide natural voltage balancing; therefore, the modulation algorithm requires it to include a balance compensator. An optimal compensator is also presented in this chapter.

The compensator generates a feedback compensation signal that correctly modifies the three-phase modulation signals. The optimal compensation signal is calculated by a dynamic limiter according to the intrinsic limitations of the system related to the variability range of the modulation signals. It can achieve voltage balancing under all operating conditions of the converter. In addition, this compensation strategy does not increase the switching frequencies of the power devices.

The DSPWM and the optimal compensator have been verified by simulation, using the MATLAB/SIMULINK software, and also by experiment. The results show good behavior of the DSPWM and the optimal compensator. Furthermore, an analysis comparing conduction and switching losses for different modulation strategies is carried out. Finally, the multilevel converter described in Chapter 2 is used to verify the algorithms proposed in this chapter.

4.1. Double-Signal PWM (DSPWM)

4.1.1. Introduction

Although the averaged NP voltage of the NPC converter can be controlled, a low-frequency NP voltage oscillation appears under some operating conditions. This is a significant drawback of this converter, since the dc-link capacitors and the devices of the converter must be designed to stand this oscillation. Furthermore, if the modulation algorithm does not take into account this NP voltage oscillation, the output voltages will contain low-frequency distortion. The feedforward PWM (Pou et al. 2002) can completely avoid such voltage distortion at the output; however, the low-frequency NP voltage oscillation still remains.

Busquets-Monge et al. (Busquets-Monge et al. 2004), proposed an interesting modulation strategy that can cancel low-frequency voltage oscillation at the NP. The analysis is based on the use of virtual vectors in space-vector modulation.
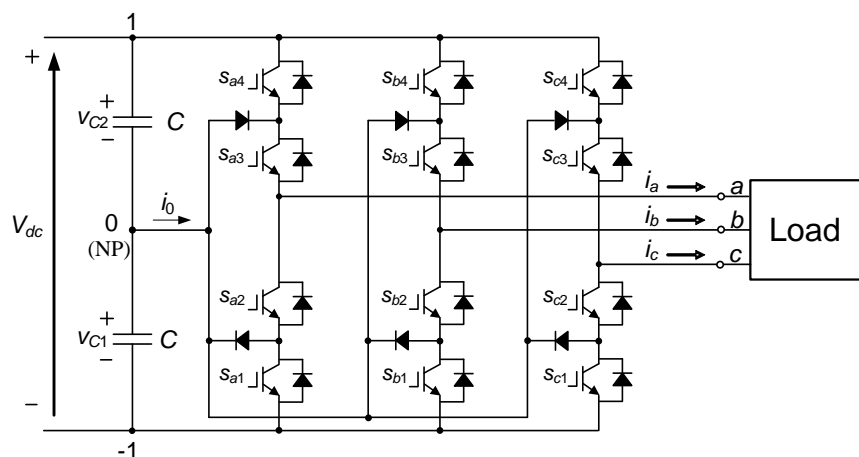
Fig.4.1. Three-level diode-clamped converter (or NPC converter).

Nevertheless, the algorithm is finally implemented using a carrier-based PWM. With this approach, however, one has to deal with angles and trigonometric functions, which complicates its application. While the algorithm can achieve an averaged NP current equal to zero, since the voltages on the capacitors are not naturally balanced, they preserve any original imbalance from the start-up of the system. Furthermore, since the voltages are not regulated, they may deviate without control.

The modulation algorithm proposed in this chapter can also enable the locally-averaged NP current to be equal to zero. However, the algorithm is based on a very simple treatment of the modulation signals, which is spectacularly easy to implement, even in a low-feature microprocessor. This strategy makes use of two carrier waveforms, just as in a standard SPWM for three-level inverters. A simple voltage-balancing compensator is proposed in this chapter that neither increases the switching frequencies of the devices nor distorts the output voltages. It is based on a proportional feedback of the voltages in the dc-link capacitors. However, the basic algorithm does not take into account the instantaneous values of the output currents and other parameters related to the operating point. Consequently, the voltage compensation dynamic is not optimal for all operating points. Consequently, an optimal compensator is also presented in this chapter that significantly improves the system's voltage balancing performance.

4.1.2. Basis of the Method

In SPWM, each phase is controlled by one modulation signal. In some approaches e. g. (Newton and Sumner 1997, Pou et al. 2005b), a zero-sequence signal is added to provide NP current control, which consequently helps to achieve voltage balance. However, the low-frequency NP voltage oscillations cannot be completely removed by means of these strategies. The modulation technique proposed here is based on the use of two modulation signals for each phase of the converter. The process for obtaining these signals is described below. First, the original modulation signals are modified to obtain SVM patterns in order to achieve the maximum range for linear operation mode, as follows:

$$\begin{cases} v_a' = v_a - v_0 \\ v_b' = v_b - v_0, \text{ and} \\ v_c' = v_c - v_0, \end{cases} \tag{4.1}$$

where $v_0 = \dfrac{\max(v_a, v_b, v_c) + \min(v_a, v_b, v_c)}{2}$.

The two modified modulation signals for each phase will be obtained from these signals, which must accomplish:

$$
\begin{cases}
v_a{}' = v_{ap} + v_{an}, \\
v_b{}' = v_{bp} + v_{bn}, \text{ and} \\
v_c{}' = v_{cp} + v_{cn},
\end{cases}
\tag{4.2}
$$

where $v_{ip} \geq 0$ and $v_{in} \leq 0$, with $i = \{a, b, c\}$. The signals with the subscript 'p' will only cross the upper carrier, $v_{carrier}^{p} \in [0, 1]$, and the signals with the subscript 'n' will only cross the lower one, $v_{carrier}^{n} [-1, 0]$. In Section (4.1.4), the process that is implemented when comparing the modulation signals with the carriers is explained. It is anticipated that the connection to the NP ("0" level) is produced when:

$$
\begin{cases}
v_{ip} > v_{carrier}^{p} \text{ and } v_{in} < v_{carrier}^{n}, \quad \text{or} \\
v_{ip} \leq v_{carrier}^{p} \text{ and } v_{in} \geq v_{carrier}^{n}.
\end{cases}
\tag{4.3}
$$

The two inner transistors of a phase leg of the converter (Fig.4.1) are in the ON state when the corresponding NP control variable $s_{i0} \in \{0, 1\}$, for $i = \{a, b, c\}$, is activated. In other words, when a variable s_{i0} takes the unity value, the subsequent output phase is connected to the NP; otherwise it takes the value of zero. When one phase leg is clamped to the NP, its output current is injected at this point. Therefore, the current i_0 can be expressed as follows:

$$
i_0 = s_{a0} i_a + s_{b0} i_b + s_{c0} i_c.
\tag{4.4}
$$

In order to preserve voltage balance, the locally-averaged NP current must be zero. Therefore, it is necessary to operate with the averaged NP current instead of the instantaneous current. The averaged NP current is obtained by using the moving average operator:

$$
\bar{x}(t) = \frac{1}{T_s} \int_{t-T_s}^{t} x(\tau) d\tau,
\tag{4.5}
$$

where T_s is the sampling or switching period. Applying this operator to (4.4), one obtains the following:

$$\bar{i}_0 = d_{a0}\bar{i}_a + d_{b0}\bar{i}_b + d_{c0}\bar{i}_c, \tag{4.6}$$

in which $d_{i0} = \bar{s}_{i0}$ for $i = \{a, b, c\}$. Assuming that the frequency of the carriers is much higher than the frequency of the modulation signals, the duty cycles can be expressed as follows:

$$d_{i0} = \left| v_{in}^{+1} - v_{ip} \right| \quad \text{where} \quad v_{in}^{+1} = v_{in} + 1. \tag{4.7}$$

Relationship (4.7) is obtained from (4.3) and by using basic trigonometry in Fig.4.2.

(a)   (b)
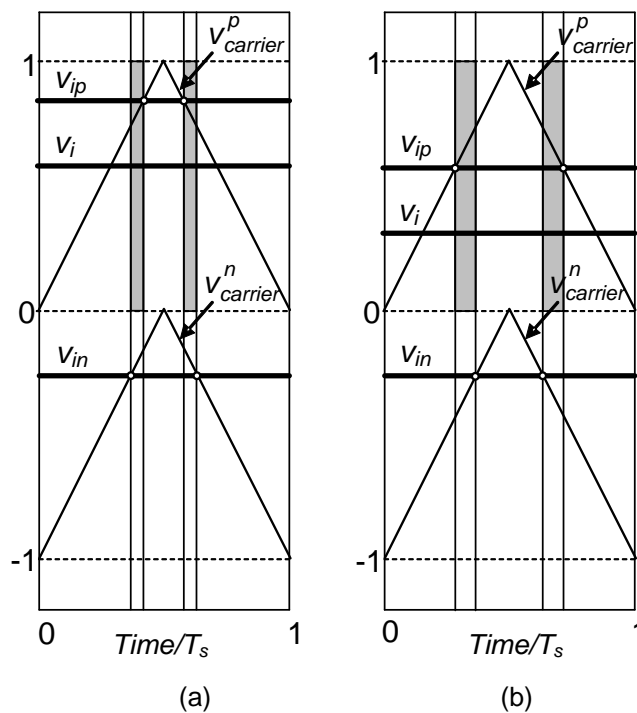
Fig.4.2. Two possible situations for the calculation of the duty cycle d_{i0}: (a) $v_{in}^{+1} < v_{ip}$, and (b)

$$v_{in}^{+1} > v_{ip}, \text{ for } v_{in}^{+1} = v_{in} + 1.$$

As a result:

$$\bar{i}_0 = \left| v_{an}^{+1} - v_{ap} \right| \bar{i}_a + \left| v_{bn}^{+1} - v_{bp} \right| \bar{i}_b + \left| v_{cn}^{+1} - v_{cp} \right| \bar{i}_c. \tag{4.8}$$

If:

$$V_{an} - V_{ap} = V_{bn} - V_{bp} = V_{cn} - V_{cp} = V_x, \quad \text{or}$$

$$v_{an}^{+1} - v_{ap} = v_{bn}^{+1} - v_{bp} = v_{cn}^{+1} - v_{cp} = 1 + v_x, \tag{4.9}$$

then the averaged NP current would be:

$$\bar{i}_0 = |1 + v_x|(\bar{i}_a + \bar{i}_b + \bar{i}_c) \tag{4.10}$$

Since the neutral of the load is open (Fig.4.1) or is just a triangle-connected load, there is not a zero-sequence of current. Subsequently, the sum of the output currents is always zero ($\bar{i}_a + \bar{i}_b + \bar{i}_c = 0$); hence, $\bar{i}_0$ becomes zero.

In conclusion, the locally-averaged voltages in the dc-link capacitors must be maintained constant, and this problem is reduced in order to find a proper value for v_x in (4.9). An infinite number of solutions can be found; however, one especially interesting solution can achieve minimum switching frequencies in the devices of the converter. This solution is found by forcing the variables v_{ip} and v_{in} to be zero for the maximum time possible, since when these signals are zero some of the transistors do not switch (the modulation signals do not cross a carrier signal). Regarding this restriction and the relationships (4.1), (4.2) and (4.9), the following solution is obtained:

$$v_x = -\frac{\max(v_a, v_b, v_c) - \min(v_a, v_b, v_c)}{2}. \tag{4.11}$$

The new modulation signals would be:

$$\begin{cases} v_{ip} = \dfrac{v_i - \min(v_a, v_b, v_c)}{2} & \text{and} \\ v_{in} = \dfrac{v_i - \max(v_a, v_b, v_c)}{2}, \end{cases} \quad \text{for} \quad i = \{a, b, c\}. \tag{4.12}$$

The algorithm can be easily implemented using the scheme shown in Fig.4.3.

Under the assumption of sinusoidal modulation signals, such that:

$$\begin{cases} v_a = (2/\sqrt{3})m\cos\omega t, \\ v_b = (2/\sqrt{3})m\cos(\omega t - 2\pi/3), \text{ and} \\ v_c = (2/\sqrt{3})m\cos(\omega t + 2\pi/3), \end{cases} \tag{4.13}$$

the solution for v_{ap} is:
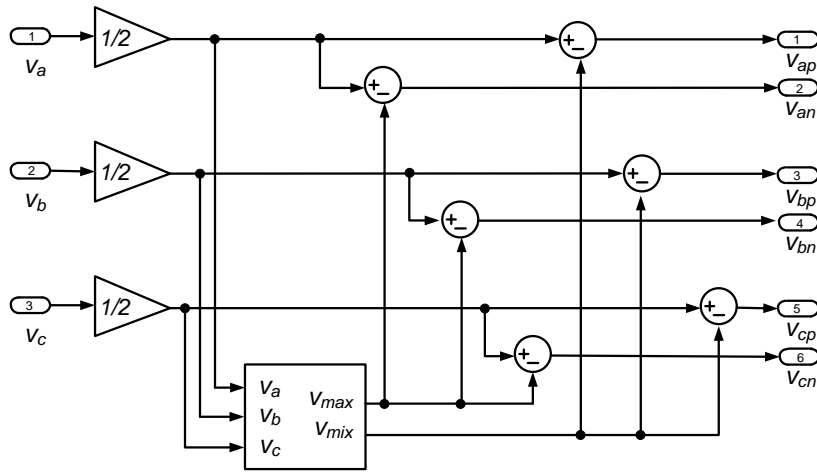
Fig.4.3. Scheme for the generation of v_{ip} and v_{in} from v_i ($i = \{a,b,c\}$.).

- for $0 \le \omega t \le 2\pi/3$, $v_{ap} = (v_a - v_c)/2 = m\cos(\omega t - \pi/6)$,

- for $2\pi/3 \le \omega t \le 4\pi/3$, $v_{ap} = 0$,   (4.14)

- for $4\pi/3 \le \omega t \le 2\pi$, $v_{ap} = (v_a - v_b)/2 = m\cos(\omega t + \pi/6)$,

and for v_{an} it is:

- for $0 \le \omega t \le \pi/3$ and $5\pi/3 \le \omega t \le 2\pi$, $v_{an} = 0$,

- for $\pi/3 \le \omega t \le \pi$, $v_{an} = (v_a - v_b)/2 = m\cos(\omega t + \pi/6)$, and   (4.15)

- for $\pi \le \omega t \le 5\pi/3$, $v_{an} = (v_a - v_c)/2 = m\cos(\omega t - \pi/6)$.

Fig.4.4 shows the waveforms for this example. Observe that the modulation index (m) is normalized to space-vector modulation: that is, $(2/\sqrt{3})m$=1.1547m is the amplitude of the original modulation signals (v_a, v_b, and v_c) according to (4.13).

The modified modulation signals for phase b have the same shape but with a $2\pi/3$ phase-shift delay, and for phase c the modulation signals have a $2\pi/3$ phase-shift advancement

Note that the modified modulation signals are within the range [-1, 1], which means that the converter would operate under linear modulation. Therefore, this example shows that the maximum modulation index achievable for linear modulation mode (amplitudes of $v_a, v_b,$ and v_c equal to 1.1547) can be achieved by this method. This maximum value is also obtained by space-vector modulation or by other carrier-

based PWM strategies that make use of a proper zero-sequence signal. However, the method proposed here has the important advantage of maintaining constant voltages in the dc-link capacitors (disregarding switching ripples).
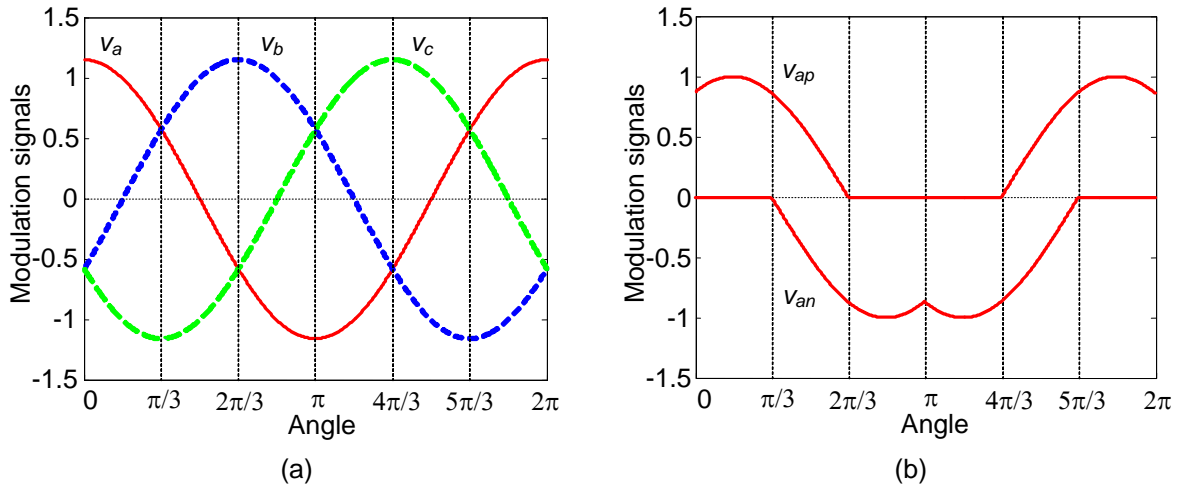
Fig.4.4. Example of sinusoidal modulation signals: (a) original signals and (b) modified signal for phase *a*.

4.1.3. Compensation for Imbalances

Using the proposed modulation technique, the locally-averaged NP current is kept to zero, and consequently the locally-averaged voltages on the dc-link capacitors are constant. However, this does not imply that these voltages are equal. In fact, in theory, if the initial voltages in the capacitors were different, this modulation strategy would tend to preserve imbalance because the locally-averaged NP current is zero. In practice, the situation is even worse since dead times, different values and behavior of the components, etc., can make the voltages drift slowly and without control. Thus, some compensation for voltage imbalances must be provided.

A control method for voltage compensation can be simply shifting the modified modulation signals in accordance with the sign of the voltage error. What makes this method inconvenient is that the signals do not preserve any interval clamped to zero when they are shifted. As a consequence, the switching frequencies of the devices increase. Furthermore, the sign of the power flux in the system needs to be known in order to provide a proper shift to the signals. The balancing strategy that will be proposed next avoids increasing the switching frequencies of the devices. Moreover, it

does not need to detect the direction of the power flux in the system. This technique is explained below.

Regarding v_{ap} and v_{an} in Fig.4.4(b), none of the signals are clamped to zero throughout the intervals $\pi/3 \le \omega t \le 2\pi/3$ and $4\pi/3 \le \omega t \le 5\pi/3$. Therefore, the modified modulation signals of phase *a* can be shifted up or down during these intervals without increasing the switching frequencies of the devices. Similarly, there are other intervals for phases *b* and *c* in which none of the associated modulation signals are clamped to zero, and therefore can be shifted. Although this strategy preserves the switching frequency of the devices when the compensator is activated, a significant drawback is the slow voltage-balancing dynamics of the system. This occurs because only the modified modulation signals associated with one phase are shifted at any time. In order to improve the balancing dynamics, the sign of the output currents should be sensed. Furthermore, relationship (4.2) must be preserved in order to avoid distortion in the output voltages during the compensation. This occurs if the offsets applied to the modified modulations signals have opposite signs. The offset applied to v_{in} is:

$$v_{i\_off} = -k_p |\Delta v_{NP}| \cdot sign(\Delta v_{NP} i_i) \cdot sign(v_{ip} - v_{in} - 1). \tag{4.16}$$

The absolute value of the voltage imbalance is multiplied by constant k_p. The term $-sign(\Delta v_{NP} \cdot i_i)$ defines a sign for the compensation. Nevertheless, the final sign of the offset depends on $sign(v_{ip} - v_{in} - 1)$ or $sign(v_{ip} - v_{in}^{+1})$, in accordance with the two possible cases shown in Fig.4.2.

4.1.4. Control Signals for the Transistors

The output level activated at each phase of the converter is defined by a comparison of the modified modulation signals with the carriers, as follows:

$$\left.\begin{array}{l} \text{If } v_{ip} > v_{carrier}^p \text{ then } x_{ip} = 1, \text{ otherwise } x_{ip} = 0 \\ \text{If } v_{in} < v_{carrier}^n \text{ then } x_{in} = 1, \text{ otherwise } x_{in} = 0 \end{array}\right\}$$

$$x_i = x_{ip} - x_{in}, \quad i \in \{a, b, c\}. \tag{4.17}$$

These variables can take three values $x_i = \{+1, 0, -1\}$., which are the possible output levels for each phase. In order to obtain the control functions of the transistors, the following relationships are needed:

$$
\begin{cases}
s_{i4} = 1 \text{ if } x_i = 1, \\
s_{i3} = 1 \text{ if } x_i = 1 \text{ or } x_i = 0, \\
s_{i2} = 1 \text{ if } x_i = 0 \text{ or } x_i = -1, \text{ and} \\
s_{i1} = 1 \text{ if } x_i = -1.
\end{cases}
\tag{4.18}
$$

If the respective above conditions are not met, then variables s_{i1}, s_{i2}, s_{i3}, and s_{i4} are correspondingly zero. These variables are associated with the ON and OFF states of the transistors ("1" and "0" mean ON and OFF, respectively), where two of them are always ON for each of the valid 27 electrical states of this converter.

4.1.5. Simulation Results

DSPWM waveforms and Total Harmonic Distortion analysis

DSPWM are initially implemented and tested by simulation using the MATLAB/SIMULINK software. The values for all these simulation examples are: V_{dc}=1,800 V and a resistive-inductive Wye-connected load with R=1 Ω and L=2 mH, respectively. The value for the dc-link capacitors is C=2,200 µF and the fundamental frequency of the ac voltage is f=50 Hz. The values of the THD and WTHD given in the figures consider the definitions D1 and D2 given in Appendix D.

Fig.4.5 shows the voltages of the dc-link capacitors (v_{C1} and v_{C2}), a line-to-line voltage (v_{ab}) and the output currents (i_a, i_b, and i_c) when the converter operates with a carrier frequency f_s=5 kHz. Note, that the voltages in the dc-link capacitors do not contain any low-frequency oscillation for all the modulation indexes. Note also, however, that the switching frequencies of the devices increase with the modulation index. This is because in DSPWM there are intervals in which the line-to-line voltages commutate among three states of the converter instead of two. The THD and WTHD values are worse compared to SPWM. However, the additional distortion is produced at high frequency (around the switching frequency and above) and therefore can be easily filtered.

Fig.4.6 shows a simulation example in which a set of second and fourth current harmonics have been added to the load currents. These harmonics are very harmful to the standard SPWM strategy, since they may introduce instability to the NP voltage, which is also a problem when operating under standard SV-PWM techniques (Pou et al. 2005a). However, when the DSPWM strategy is applied, the voltages in the dc-link capacitors do not show any negative effect and the system is always stable.

(a)

(b)

(c)

(d)
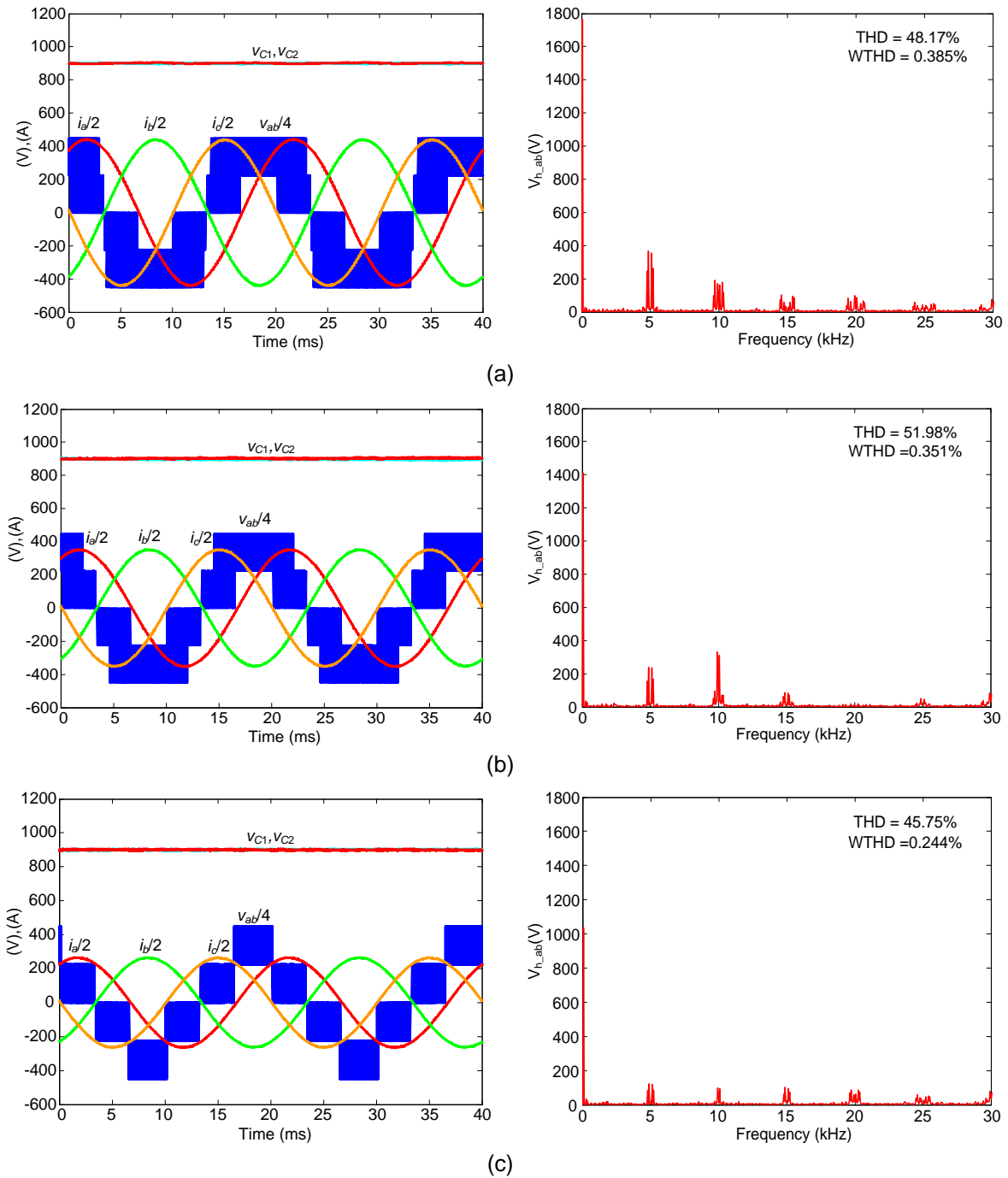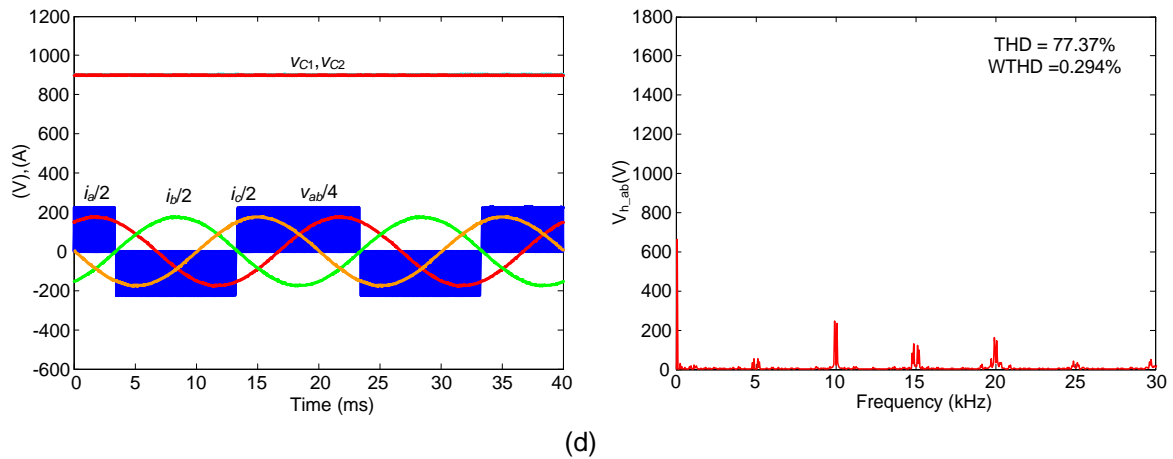
Fig.4.5. Simulation results of DSPWM: (a) *m*=1; (b) *m*=0.8; (c) *m*=0.6; (d) *m*=0.4.
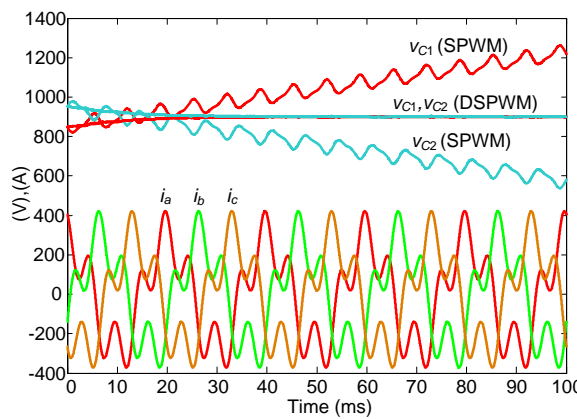
Fig.4.6. Dynamics of the SPWM and DSPWM operating over a nonlinear load.

Loss analysis

A MATLAB/SIMULINK model to calculate losses in the NPC converter has been developed. The converter rated power is 2.8 MVA (1,700 V / 950 A, V_{dc}=2,400 V). In all simulations, the ac output currents are assumed to be constant at their rated values and the sampling frequency is f_s=5 kHz (carriers' frequency).

The selected IGBTs are the DIM1200NSM17-E000, whose maximum ratings have a forward current of 1,200 A and a direct voltage of 1,700 V. In the following analysis, the model of the IGBTs is based on the typical curves given by the manufacturer. The method used to calculate the conduction and switching losses in a power device are explained in Appendix C.

Fig.4.7 shows the conduction losses obtained using SPWM and DSPWM. Since the difference between the losses obtained from the two modulation techniques is less than 1%, only one representation is given.
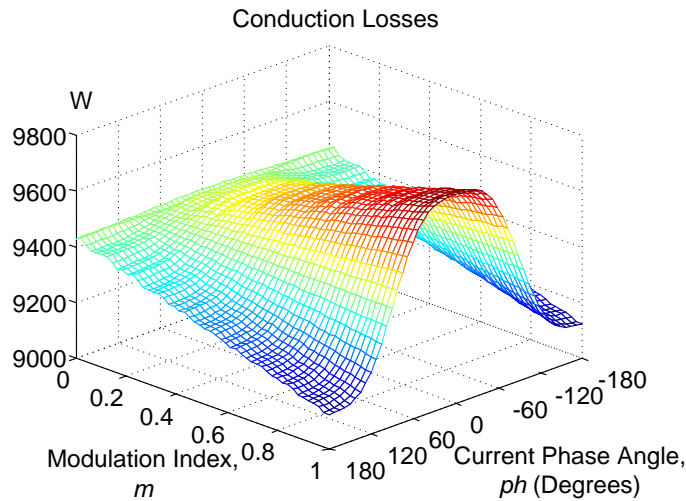
Fig.4.7. Conduction losses obtained using SPWM and DSPWM.

Fig.4.8 and Fig.4.9 show the switching losses of the SPWM and DSPWM, respectively.

Fig.4.10 shows the ratio of total losses between DSPWM and SPWM techniques. The switching losses in DSPWM are larger than in SPWM due to the higher switching frequencies. In the worst case, the maximum ratio is up by about 28%. Notice that in SPWM the maximum switching losses are obtained by operating around the unity power factor, whereas in such conditions DSPWM produces minimum losses.
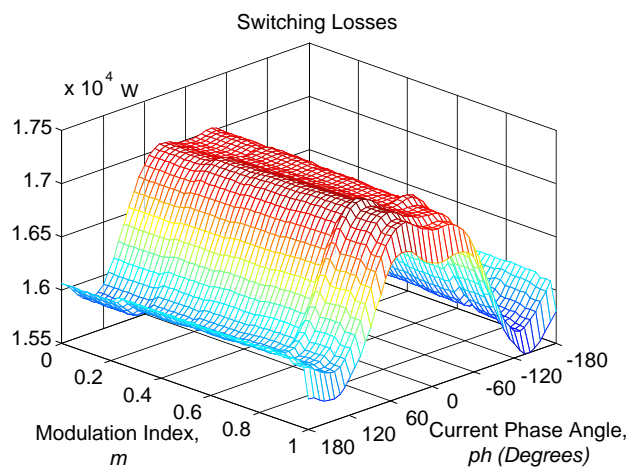
Fig.4.8. Switching losses using SPWM.
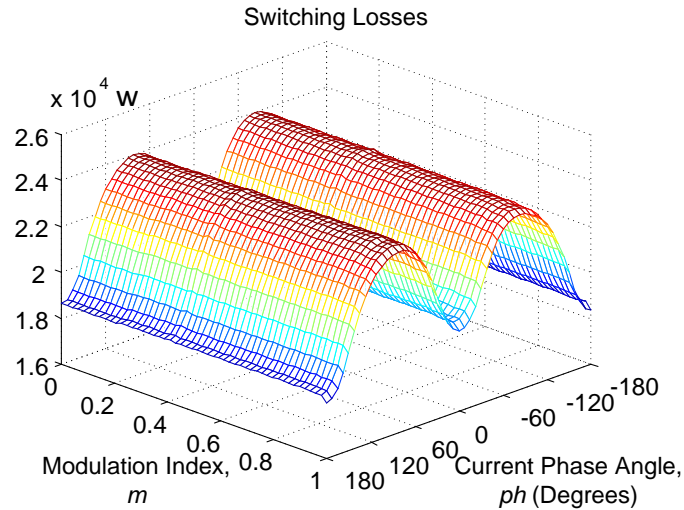
Switching Losses

Fig.4.9. Switching losses using DSPWM.
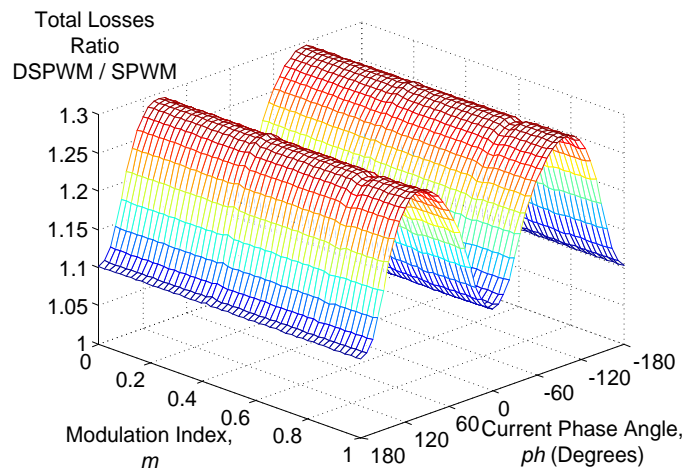
Fig.4.10. Ratio of total losses DSPWM / SPWM.

NP Voltage oscillations

The maximum low-frequency NP voltage amplitudes that occur under specific operating conditions of the converter are also analyzed with the MATLAB/SIMULINK model. The normalized amplitude of the ripple ($\Delta V_{NPn}/2$) was defined by (E1) and the conditions used to calculate the normalized low frequency oscillation were given in Appendix E. Fig.4.11 shows that there are no NP voltage oscillations using DSPWM.
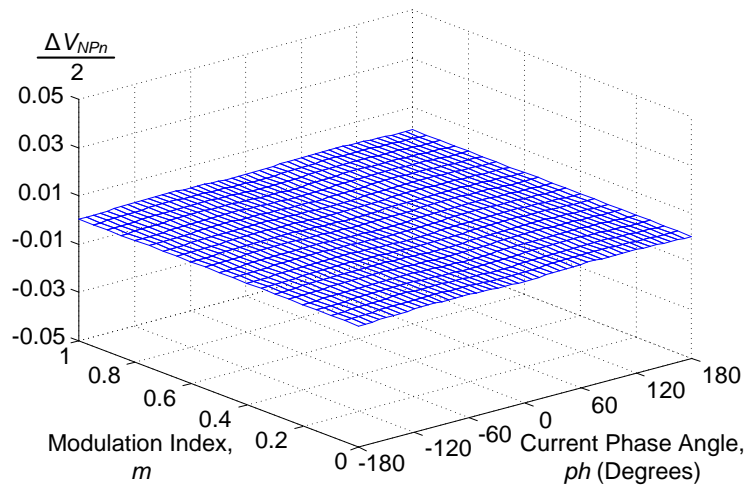
Fig.4.11. Normalized low-frequency NP voltage amplitudes in DSPWM.

4.1.6. Experimental Results

The proposed DSPWM has been verified by experiment. The values of the dc-link voltage and the capacitors are V_{dc}=120 V and C=2,200 μF, respectively. The converter operates over an R-L Wye-connected load with L=12 mH and R=11.5 Ω. The frequency of the carriers is f_s=5 kHz in all the results.

In Fig.4.12, the variables shown are a line-to-line output voltage (v_{cb}), the voltages in the dc-link capacitors (v_{C1} and v_{C2}), and the output currents (i_a, i_b, and i_c). The output frequency has been selected to be very low in this example (f=20 Hz) in order to emphasize any possible low-frequency voltage oscillations in the dc-link capacitors. Observe that there are only high-frequency voltage ripples which are related to the switching frequency. Nevertheless, the switching frequencies of the devices increase compared to SPWM, since there are intervals in which the line-to-line voltages commutate among three states of the converter instead of two. This is produced when neither of the two corresponding modified modulation signals is clamped to zero.

The balancing process is shown in Fig.4.13, where the initial voltages in the dc-link capacitors are unbalanced. Observe that the voltages become equal. However, the balancing dynamics depend on the operating point of the converter and needs readjustment of the constant k_p (4.16) for different operating conditions. Consequently, the compensation method will be improved in the following section.

(a)

(b)

(c)
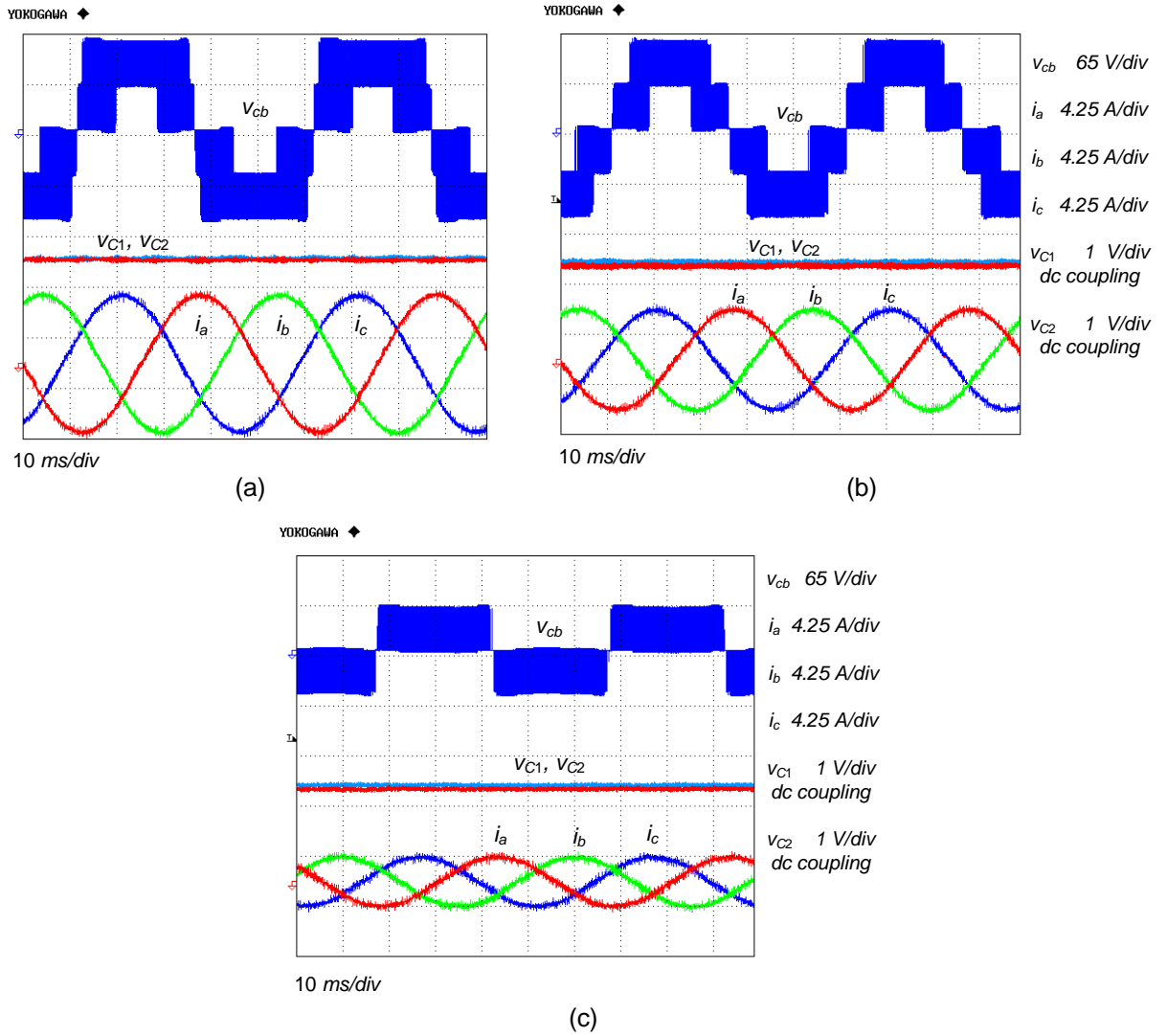
Fig.4.12. Experimental results for the proposed DSPWM: (a) m=1, (b) m=0.7, and (c) m=0.4.
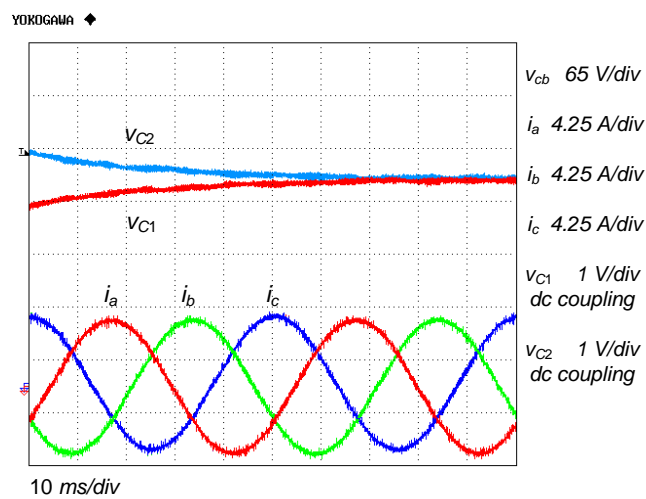
Fig.4.13. Dynamics of the voltage compensator operating on a linear load (m=0.9).

4.2. Optimal Compensator and Control Limitation in DSPWM

Several compensators able to balance the voltage in the dc-link capacitors can be applied. However, the design of a compensator is critical because it not only determines the voltage-balancing dynamic of the system, but it also may produce instability under some operating conditions.

In (Newton and Sumner 1997), a common-mode voltage is introduced into the modulation signals to control the dc-link capacitor voltages. This feature can be used to compensate for voltage imbalances. The controllers proposed in the previous Section 4.1.3, or the one used in (Busquets-Monge et al. 2008), are not optimal for all operation conditions because they do not take into account the instantaneous values of the output currents or some other parameters related to the operating point. Consequently, the voltage compensation dynamic is very slow.

In the previous section, a voltage-balance compensator was presented which not only considers voltage imbalance, but also the sign of the instantaneous output currents. A proportional-based feedback loop generates a compensation signal that is applied to the modulation signals properly without increasing the switching frequency of the power devices. However, a limiter has to be applied to the compensation signal (v_{i_off}) to avoid the opposite effect produced by overcompensation. If a static limiter is used for all the operating conditions, the output voltages may be distorted significantly, and additionally, it may cause instability in the system. The approach presented here is designed to overcome these drawbacks and the difficulty of adjusting the controller and the limiter for different operating points of the converter.

A dynamic limiter and a control loop are presented which provide the system with a fast balancing dynamic and guarantee stability under all operating conditions. The optimal compensator is applied to the modulation presented in the previous section, although it can also be adapted to other modulation strategies with similar characteristics.

The proposed optimal control generates a feedback compensation signal that correctly modifies the three-phase modulation signals. The optimal compensation signal is calculated by a dynamic limiter according to the intrinsic limitations of the

system related to the variability range of the modulation signals. It significantly improves the voltage balancing under all operating conditions of the converter. In addition, this compensation strategy preserves the property of not increasing the switching frequencies of the power devices. The algorithm is tested and verified using both simulation and experimentation.

4.2.1. Control Strategy

A proper offset must be applied to the modulation signals to achieve good voltage balancing performance. The offset is added with the opposite sign to the modulation signals of each phase (v_{ip} and v_{in}), which ensures that the values of v_a', v_b', and v_c' in (4.2) are not affected. Consequently, the output voltages are not distorted during compensation.

If the wrong sign is applied to the offset it will produce voltage imbalance. However, if the correct sign is applied but not an optimal magnitude, the following effects are observed:

- If the value of the offset is lower than required, a slow voltage-balancing dynamic on the dc-link capacitors is produced.

- If the value of the offset is higher than the optimal one, the system dynamic is slow and low-frequency voltage oscillations appear at the NP.

The control variable for voltage-balancing is the NP current i_0 (4.4). The locally-averaged value of this variable (4.8) is zero in the steady-state condition and different from zero during compensation. The current injected into the NP depends on the time during which the output phases are connected to that point and the specific values of the output currents $\{i_a, i_b, i_c\}$.

If the two dc-link capacitors have the same value (Fig.4.14), the currents i_{C1} and i_{C2} can be described by the following expressions:

$$i_{C1} = i_{Cm} - \frac{i_0}{2} \quad \text{and} \quad i_{C2} = i_{Cm} + \frac{i_0}{2}. \tag{4.19}$$

In order to produce the reference voltage value ($V_{dc}/2$), the locally-averaged currents should be:

$$\begin{cases} \bar{i}_{C2} = \bar{i}_{Cm} + \dfrac{\bar{i}_0}{2} = C\dfrac{\dfrac{V_{dc}}{2} - v_{C2}}{T_s} \quad \text{and} \\[3mm] \bar{i}_{C1} = \bar{i}_{Cm} - \dfrac{\bar{i}_0}{2} = C\dfrac{\dfrac{V_{dc}}{2} - v_{C1}}{T_s}, \end{cases} \tag{4.20}$$

where T_s is the sampling or switching period and i_{Cm} is the common current through both capacitors. If the total dc-link voltage is constant —for example, imposed by a power supply— this current is zero. Similarly, if the voltage is not absolutely constant but is controlled by a proper control loop, the average value of this current is still zero.
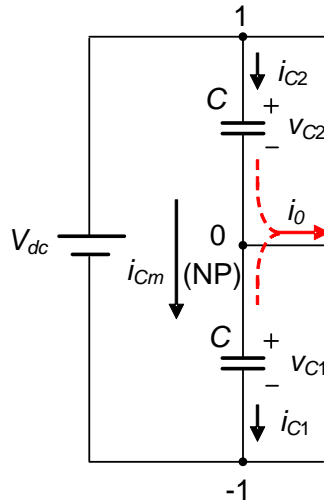
Fig.4.14. Current in the capacitors.

Consequently, by subtracting the second equation from the first one in (4.20), the reference value for the locally-averaged NP current should be defined as follows:

$$\bar{i}_0 = C\frac{v_{C1} - v_{C2}}{T_s}. \tag{4.21}$$

An example calculation of the offset needed for the modulation signals in Phase *a* (v_{a_off}) is given below. First, the duty cycle for the connection of this phase to the NP is obtained from (4.6) and (4.7):

$$d_a = \frac{-d_b\, i_b(k+1) - d_c\, i_c(k+1)}{i_a(k+1)} = \mid v_{an} - v_{ap} + 1 \mid, \tag{4.22}$$

where *k* and *k+1* represent the current sampling period and the following one, respectively. In this equation, it is assumed that the locally-averaged NP current is zero $\bar{i}_0(k+1) = 0$.

By adding an offset -v_{a_off} to the modulation signal v_{ap}, and v_{a_off} to the modulation signal v_{an}, the duty cycle d_a is changed to d_a'. Consequently, the NP current can be calculated as follows:

$$\bar{i}_0(k+1) = d_a'\, i_a(k+1) + d_b\, i_b(k+1) + d_c\, i_c(k+1), \tag{4.23}$$

where $\bar{i}_0(k+1)$ is now different from zero. The new duty cycle is:

$$d_a' = \frac{\bar{i}_0(k+1) - d_b\, i_b(k+1) - d_c\, i_c(k+1)}{i_a(k+1)}, \tag{4.24}$$

where:

$$d_a' = \mid v'_{an} - v'_{ap} + 1 \mid = \left| 2v_{a\_off} + v_{an} - v_{ap} + 1 \right|. \tag{4.25}$$

The following relationship is obtained from (4.22) and (4.24):

$$\frac{d_a'}{d_a} = \left[\frac{\bar{i}_0(k+1)}{-d_b\, i_b(k+1) - d_c\, i_c(k+1)} + 1 \right]. \tag{4.26}$$

To have a physical meaning, all duty cycles must be positive. The offset to be applied to Phase *a* is included in (4.25) and can therefore be obtained from this equation; however, it is implicit in an absolute value operator and should be isolated. Table 4.1 shows the eight possible cases, in which the sign and relative magnitude of the variables are taken into account. The sign of the variables is shown in brackets as [+] or [−]. For the sake of simplicity we used the variables *x* and *y*, which are defined as $x = v_{an} - v_{ap} + 1$ and $y = 2v_{a\_off}$.

Only two cases have to be considered: in Cases 3, 4, 7, and 8 the variable *x* is always positive, and Case 6 can also be disregarded because $x^{(+)} < y^{(-)}$ is not possible if *y* is negative.

Table 4.1. Possible cases for simplification.

$\|v_{an} + v_{a\_off} - v_{ap} + v_{a\_off} + 1\| \Rightarrow x = v_{an} - v_{ap} + 1$ and $y = 2v_{a\_off}$		
Case	**Condition**	**Solution**
1	if $[(x^{(+)}$ and $y^{(+)})$ and $(x^{(+)}>y^{(+)})]$	$\|x\|+\|y\|$
2	if $[(x^{(+)}$ and $y^{(+)})$ and $(x^{(+)}<y^{(+)})]$	$\|x\|+\|y\|$
3	if $[(x^{(-)}$ and $y^{(-)})$ and $(x^{(-)}>y^{(-)})]$	$\|x\|+\|y\|$
4	if $[(x^{(-)}$ and $y^{(-)})$ and $(x^{(-)}<y^{(-)})]$	$\|x\|+\|y\|$
5	if $[(x^{(+)}$ and $y^{(-)})$ and $(x^{(+)}>y^{(-)})]$	$\|x\|-\|y\|$
6	if $[(x^{(+)}$ and $y^{(-)})$ and $(x^{(+)}<y^{(-)})]$	$\|y\|-\|x\|$
7	if $[(x^{(-)}$ and $y^{(+)})$ and $(x^{(-)}>y^{(+)})]$	$\|x\|-\|y\|$
8	if $[(x^{(-)}$ and $y^{(+)})$ and $(x^{(-)}<y^{(+)})]$	$\|y\|-\|x\|$

Note that Cases 1 and 2 have the same mathematical solution and can therefore be treated as a single case. By taking into account the absolute value of the duty cycle, it is possible to determine the relationship between the modulation signals and the compensation according to the following expression:

$$\begin{cases} d_a{}' = \left|v_{an} - v_{ap} + 1\right| + \left|2v_{a\_off}\right| \\ d_a{}' = \left[\dfrac{\bar{i}_0(k+1)}{-d_b\,i_b(k+1) - d_c\,i_c(k+1)} + 1\right]\left|v_{an} - v_{ap} + 1\right|. \end{cases} \tag{4.27}$$

The value of v_{a_off} in Case 1 is:

$$v_{a\_off} = \frac{1}{2}\left|\frac{\bar{i}_0(k+1)\left|v_{an} - v_{ap} + 1\right|}{-d_b\,i_b(k+1) - d_c\,i_c(k+1)}\right|. \tag{4.28}$$

Case 5 is also considered. The relationship of the duty cycle with the modulation signals is:

$$d_a{}' = \left|v_{an} - v_{ap} + 1\right| - \left|2v_{a\_off}\right|, \tag{4.29}$$

and the value of v_{a_off}:

$$v_{a\_off} = -\frac{1}{2}\left|\frac{\bar{i}_0(k+1)\left|v_{an} - v_{ap} + 1\right|}{-d_b\,i_b(k+1) - d_c\,i_c(k+1)}\right|. \tag{4.30}$$

The mathematical process for the other phases is the same as the one shown for Phase *a*. Table 4.2 shows the offset for the three phases in the two possible cases. The equations define the optimal offset value because they include the most relevant variables of the operation point and the system dynamics: the output currents, the modulation index, the carrier frequency, the dc-link capacitor values, and the corresponding voltages.

Table 4.2. Possible cases per phase.

Two cases (±)	
	$v_{a\_off} = \pm \dfrac{1}{2} \left| \dfrac{\bar{i}_0(k+1)\left|v_{an} - v_{ap} + 1\right|}{-d_b\, i_b(k+1) - d_c\, i_c(k+1)} \right|$
	$v_{b\_off} = \pm \dfrac{1}{2} \left| \dfrac{\bar{i}_0(k+1)\left|v_{bn} - v_{bp} + 1\right|}{-d_a\, i_a(k+1) - d_c\, i_c(k+1)} \right|$
	$v_{c\_off} = \pm \dfrac{1}{2} \left| \dfrac{\bar{i}_0(k+1)\left|v_{cn} - v_{cp} + 1\right|}{-d_a\, i_a(k+1) - d_b\, i_b(k+1)} \right|$

In accordance with (4.16), the final sign applied to the offset of the negative modulation signal (v_{i_off}) is calculated as $-sign(\Delta v_{NP}\, i_i) \cdot sign(v_{ip} - v_{in} - 1)$. However, in this case it becomes $sign(\Delta v_{NP}\, i_i)$ because the second term is always negative.

The mathematical values obtained from the equations in Table 4.2 are not always applicable, depending on the values of the modulation signals, which must be within the carrier interval, that is $v_{carrier}^p \in [0, 1]$ and $v_{carrier}^n [-1, 0]$. Other restrictions that should be considered are described in the following section.

4.2.2. Maximum Offset and Control Limits

The magnitude and sign of v_{i_off} can be calculated either by applying the control technique proposed in this paper or by using the ones presented in Section 4.1.3 or in (Busquets-Monge et al. 2008). However, the maximum values of this offset should be limited to prevent it from producing an unbalancing effect.

By using (4.12), it is easy to demonstrate that the condition $v_{in}^{+1} \geq v_{ip}$ for $v_{in}^{+1} = v_{in} + 1$ is always met, provided that no offset is added to the signals. This situation is considered in the example shown in Fig.4.15(a); the shaded area corresponds to the time interval in which the output phase associated with the modulation signal is connected to the NP. If a negative offset is added to v_{in} (and positive to v_{ip}), the shared area is reduced, which indicates that the NP connection time decreases. However, if the offset is too large, as is the case in the example shown in Fig.4.15(b), the condition $v_{in}^{+1} \geq v_{ip}$ is not met. Consequently, the opposite effect is produced: that is, the shared area is enlarged, which indicates that the NP connection time increases. In conclusion, small offsets decrease the NP connection time and large offsets may increase it. The limiting condition is produced when $v_{in}^{+1} = v_{ip}$.
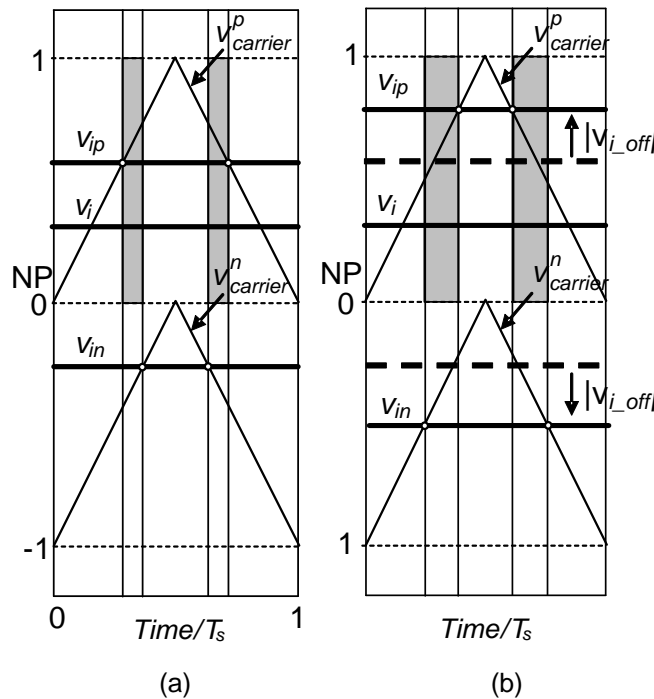
Fig.4.15. Modulation and carrier signals. (a) No compensation offset added and (b) excessive offset added.

Fig.4.16 shows the resulting upper and lower offset limits that can be applied, provided that the condition $v_{in}^{+1} \geq v_{ip}$ is met and the modulation signals are within the intervals $0 \leq v_{ip} \leq 1$ and $-1 \leq v_{in} \leq 0$. If an offset above the upper surface or below the lower surface is applied, the produced compensation effect is the opposite.

Note in Fig.4.16 that the relative phase of the output currents is represented only for the interval [0º, 120º]. The reason for this simplification is because of symmetry in the other angle intervals.

Fig.4.17 shows the average NP current produced when the maximum compensation offset is applied and sinusoidal output currents are assumed. All possible phases of the output currents and the linear modulation index (0≤m≤1) are shown. The modulation index is normalized to space-vector modulation: that is, $(2/\sqrt{3})m$ is the amplitude of the original modulation signals (v_a, v_b, and v_c) . The average NP current is normalized to the RMS output current of the converter (I_{RMS}).

The above information can be used to determine the time needed to balance the voltages in the capacitors from an initial imbalance. The voltage in a capacitor is defined by the following expression:

$$v_C = \frac{1}{C}\int_0^t i_C \, dt + V_{C0},$$ (4.31)

where v_{C0} is the initial voltage and i_C is the current through the capacitor. This current is composed of an average value and a series of ac components. However, the global voltage dynamic is defined only by the average current, since the ac currents only produce voltage oscillations. By applying (4.31) and considering only the average current, the variation in the voltage in the capacitor can be defined as follows:
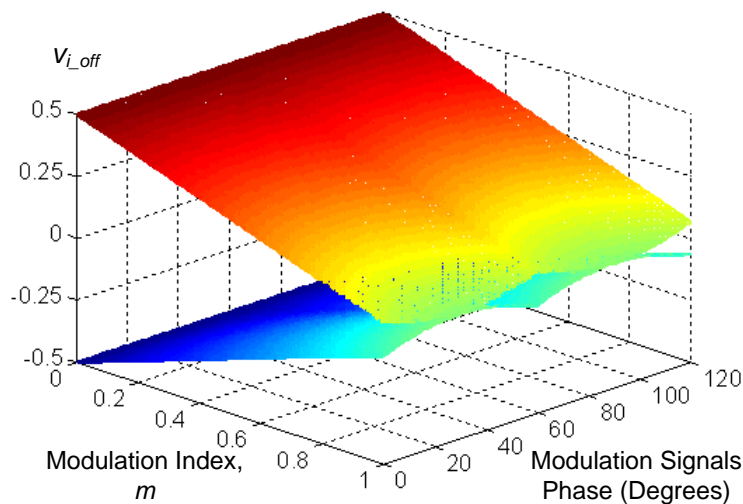
Fig.4.16. Upper and lower limiting areas for the compensation offset.
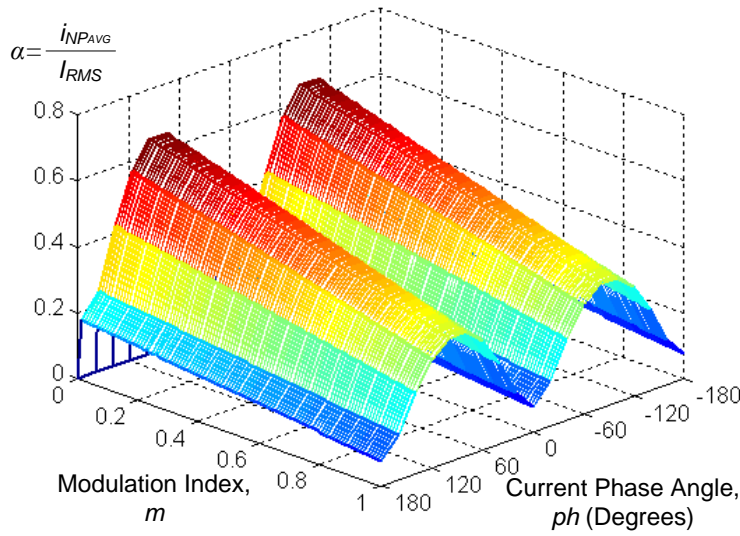
Fig.4.17. Maximum compensating NP current for sinusoidal output currents.

$$\Delta v_C = v_C - V_{C0} = \frac{I_{C_{AVG}}}{C} t .$$

(4.32)

If the two dc-link capacitors have the same value, the current through them is $i_C = i_{NP}/2$. Taking this into account, and assuming an initial voltage imbalance defined by Δv_C, the balancing time (t_B) can be calculated from (4.32) as follows:

$$t_B = \frac{2C\Delta V_C}{\alpha\, I_{RMS}} \quad \text{where} \quad \alpha = \frac{I_{NP_{AVG}}}{I_{RMS}} .$$

(4.33)

4.1.3. Simulation Results

The optimal and nonoptimal voltage-balancing control algorithms are initially implemented using the Matlab-Simulink software. The values for the simulation examples are: V_{dc} = 1,800 V and a resistive-inductive Wye-connected load with R=1 Ω and L=2 mH, respectively. The value for the dc-link capacitors is C=2,200 μF and the frequency of the triangular carriers is f_s=5 kHz in all the simulations.

Fig.4.18 shows the voltage waveforms in the dc-link capacitors. These waveforms were tested for a modulation index m=0.8 and output frequency f=50 Hz. The initial voltages in the dc-link capacitors are v_{C1}=1,100 V and v_{C2}=700 V. The waveforms labeled 'a' correspond to the proposed compensation control (Table 4.2)

used with the limiting surface shown in Fig.4.16 The waveforms 'b' and 'c' correspond to the nonoptimal compensator based on (4.16) and a static limiter adjusted to ±0.03 and ±1, respectively. Note that the balancing dynamic is much faster when the optimal compensator is used.

In Case 'c', the balancing dynamic is very slow and voltage oscillations are observed during the process. This is because offset values beyond the limiting surfaces shown in Fig.4.16 are applied, producing an unbalancing effect during some intervals.

There is no overcompensation in Case 'b' because the limiting values are lower than in Case 'c'. Consequently, the balancing dynamic is faster and no oscillations are observed. However, the dynamic is still slower than in Case 'a'. This is because the offset is limited to a constant value, whereas larger offsets could be applied at the operating point used.

In conclusion, static limiters such as the ones used in (Busquets-Monge et al. 2008, Pou et al. 2007) do not take full advantage of the balancing potential of the system. Furthermore, the limiting values should be adjusted for each specific operating point to produce a faster balancing dynamic. However, since the maximum applicable offset depends on the instantaneous phase of the modulation signals within a given period (see Fig.4.16), the results produced by a constant limiter will never be as good as those obtained when a dynamic limiter is used.

Fig.4.19 shows the balancing dynamic of the voltages in the capacitors when using the proposed compensator for the modulation indices m=1, m=0.6, and m=0.3. Since the R-L load is constant, the magnitude of the output currents depends on the modulation index. When the voltages are significantly unbalanced, the maximum compensation offset is applied according to the dynamic limiter. Note that there are some intervals in which the system is only able to produce minimal compensation (flat intervals). Nonetheless, the balancing dynamic is very good for all of the modulation indices considered.

The balancing time required to obtain equal voltages in the capacitors from an initial imbalance can be calculated by using (4.33). Table 4.3 shows the theoretical

results for the conditions used in the simulations in Fig.4.19. The two sets of results correspond exactly.
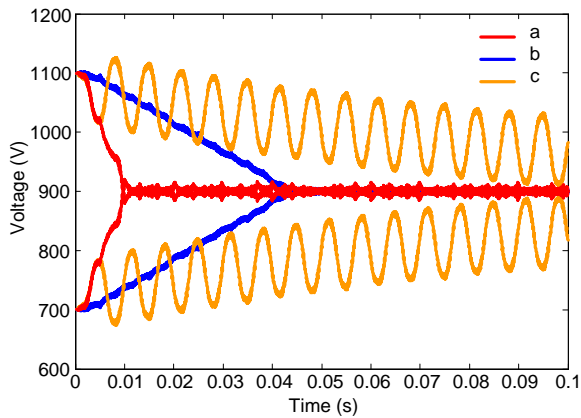
Fig.4.18. Voltage in the dc-link capacitors using the optimal (Case 'a') and the nonoptimal (Cases 'b' and 'c') compensators.
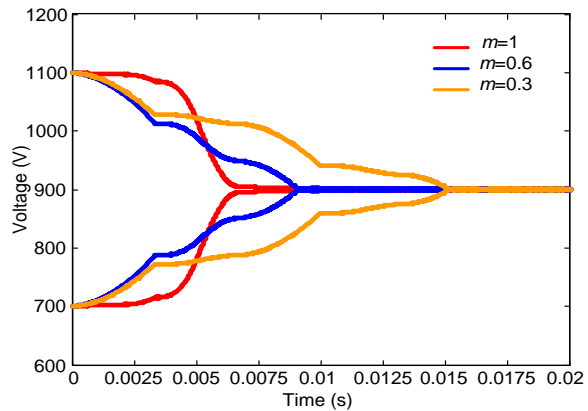
Fig.4.19. Voltage in the dc-link capacitors under different modulation indices using the optimal compensator.

Table 4.3. Calculated values for the simulation conditions in Fig.4.19.

	m=1	m=0.6	m=0.3
α	0.1837	0.2390	0.2815
I_{RMS} (A)	622.25	373.35	183.84
ph (Degrees)	32.14	32.14	32.14
t_B (s)	0.0069	0.0088	0.0150

Since high power systems usually operate at low-switching frequencies, performance of the modulation strategy with the proposed compensator is also tested in such conditions. Fig.4.20 shows some results obtained from a modulation index m=0.8 and switching frequencies of f_s=2.5 kHz and f_s=1 kHz. Note that the voltage balancing behavior is also excellent for such low-switching frequencies.

In Fig.4.21, the system is tested in zero-power factor operation mode, while the amplitude of the output currents is maintained the same. The voltage balancing dynamic using DSPWM with the optimal compensator is even better than with the previous RL load.

This is coherent with the information presented in Fig.4.17, in which the maximum compensation current is achieved for a zero-power factor. Fig.4.21 also shows the balancing dynamic using SVM, particularly the NTV modulation, in which the redundant vectors are selected to help for voltage balance (Pou et al. 2004). In this

simulation, the loading conditions are the same; that is, a zero power factor. Note that, in addition to the appearance of low-frequency voltage oscillations, the balancing dynamic is much slower under such conditions**.**
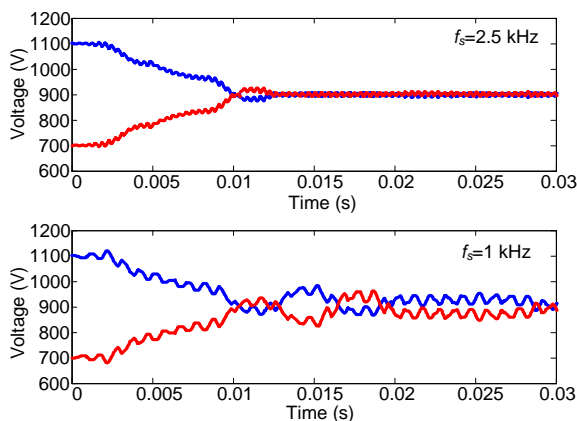
Fig.4.20. Voltage in the dc-link capacitors using the optimal compensator for a low-switching frequency operation.
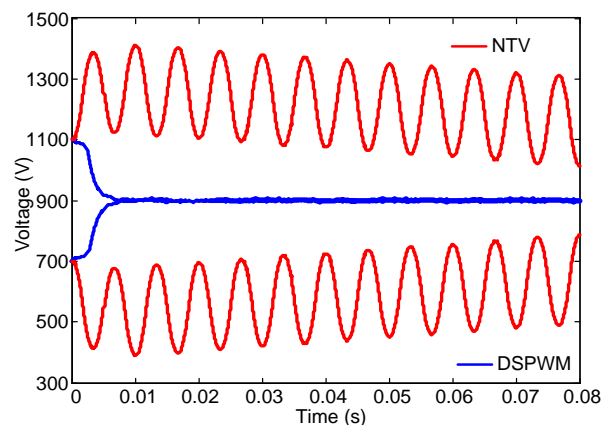
Fig.4.21. Comparison of voltage balancing dynamics operating with zero power factor for DSPWM with the optimal compensator and NTV.

4.1.4. Experimental Results

The optimal voltage-balancing compensator and the modulation technique were programmed into a TMS320F2812 DSP board. The experimental set up included the NPC converter described in Chapter 2 with the following specifications: dc-link voltage of V_{dc}=120 V, dc-link capacitors C=2,200 µF, and a Wye-connected resistance-inductance load with R=11.5 Ω and L=12 mH. The frequency of the triangular carriers was f_s=5 kHz.

The results shown in Fig.4.22 and Fig.4.23 were obtained from an output frequency f=50 Hz and a modulation index m=0.7. The waveforms represent the voltages in the dc-link capacitors, a line-to-line voltage, and the output currents.

Fig.4.22(a) and (b) show the waveforms obtained using the nonoptimal control given by (4.16) with static limiters of ±1 and ±0.03, respectively. The value of the parameter k_p is 0.1. Fig.4.23 shows the waveforms obtained using the optimal control and limiter proposed in this chapter. The results match those reported in the simulation section, which underlines the effectiveness of the proposed method.
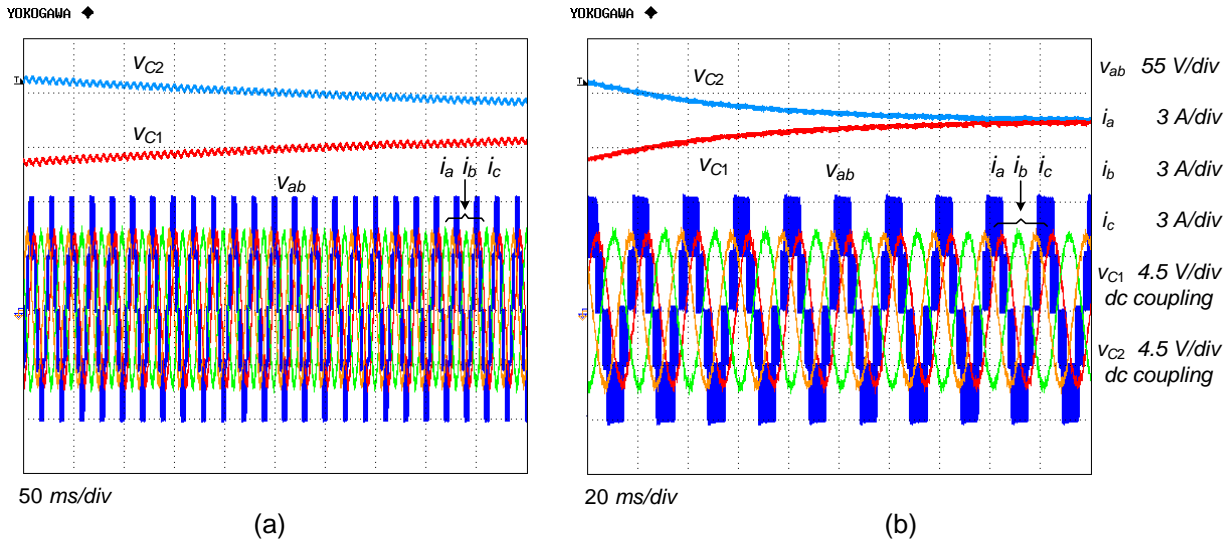
Fig.4.22. Nonoptimal compensator: (a) with a limiter of ±1, and (b) with a limiter of ±0.03.
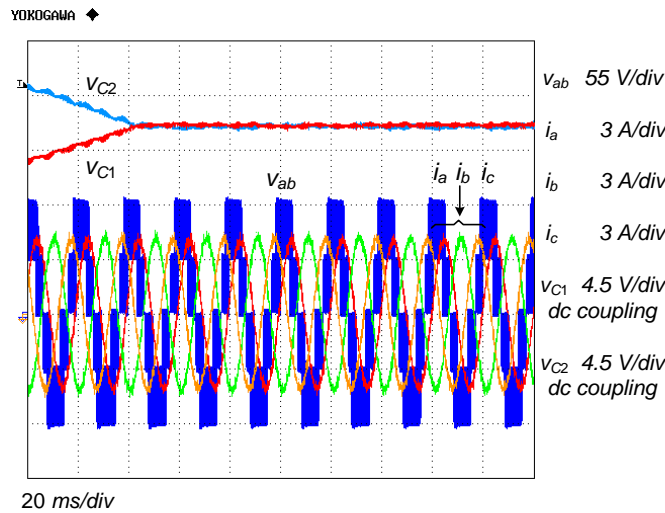
Fig.4.23. Optimal compensator.

We now consider the application of the dynamic limiter to the nonoptimal control. In this case, fast balancing dynamics can be achieved by assigning high values to parameter k_p, because maximum compensation offset is applied under large voltage imbalances. However, for small imbalances, or simply the switching ripple, high values of k_p produce an excessive compensation offset signal. Consequently, the voltage ripple in the dc-link capacitors increases and the jumps in the compensation offsets create greater distortion in the output voltages.

Fig.4.24 and Fig.4.25 show experimental results for modulation indices of m=0.8 and m=0.4, respectively, which illustrate the scenario described above. Fig.4.24(a) shows the case in which the nonoptimal control and the dynamic limiter are applied

together. The value of the parameter k_p was increased until the balancing performance was similar (k_p=0.25) to the one achieved by the proposed controller shown in Fig.4.24(b). The same value of k_p is used in Fig.4.25. Note the additional distortion produced in the line-to-line voltages when the nonoptimal controller is used, particularly in Fig.4.25(a). Consequently, assigning high values to k_p is not a good solution for improving voltage-balancing performance when the nonoptimal compensator is used. Low values of k_p would attenuate these problems but the resulting balancing performance would be poor.

(a)   (b)
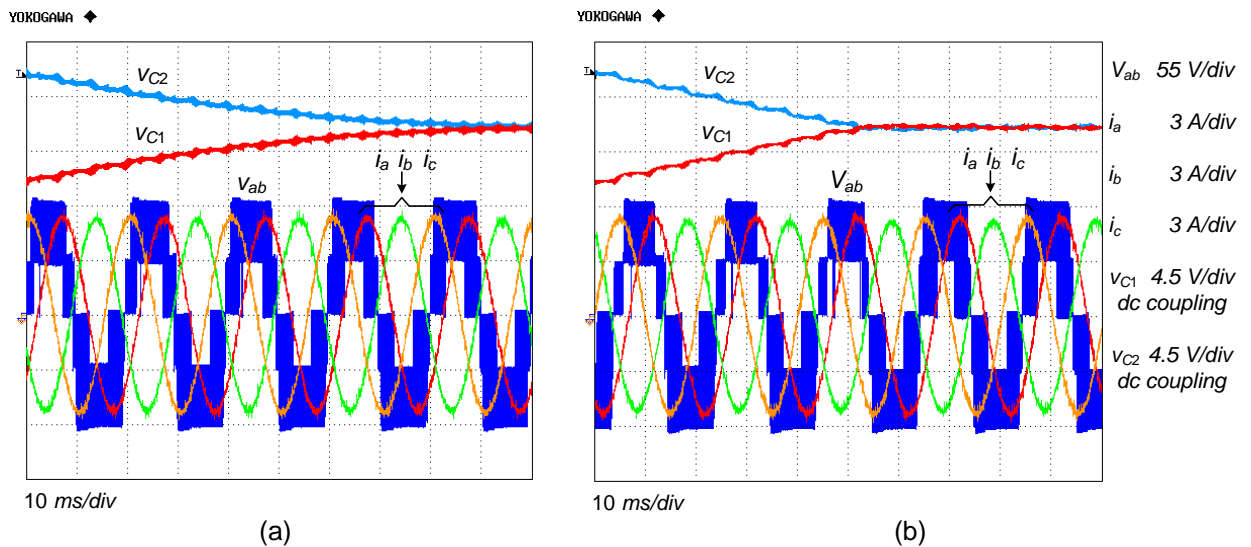
Fig.4.24. Experimental results with the dynamic limiter and a modulation index m= 0.8: (a) Nonoptimal voltage-balancing compensator, and (b) proposed compensator.

(a)   (b)
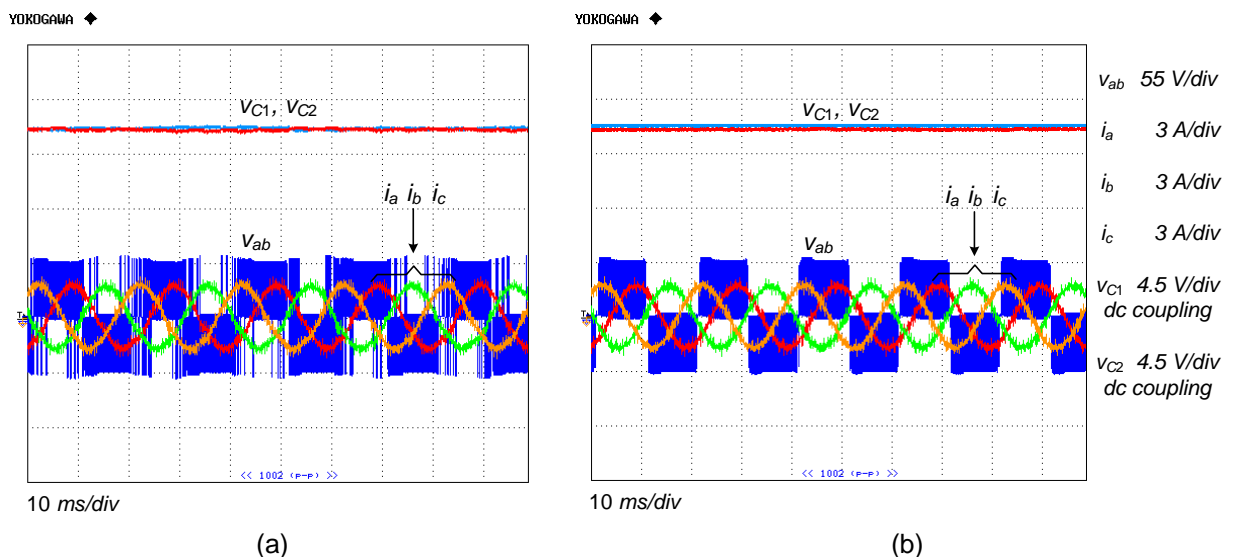
Fig.4.25. Experimental results with the dynamic limiter and a modulation index m= 0.4: (a) Nonoptimal voltage-balancing compensator, and (b) proposed compensator.

4.3. Chapter Conclusions

The DSPWM proposed in this chapter completely removes the low-frequency voltage oscillations that appear at the NP of the three-level inverter for some operating conditions. This technique is also able to attain the maximum amplitudes achievable under linear modulation, and its algorithm is very simple and can therefore be quickly processed in real time. Furthermore, unbalanced and nonlinear loads no longer produce additional low-frequency voltage oscillations or instability to the NP. The only drawback of this strategy is that the switching frequencies of the devices are one-third higher than a standard SPWM for any modulation index under linear operation mode.

Although the voltages on the dc-link capacitors do not show any low-frequency oscillation, the proposed modulation method does not provide natural voltage balance. Therefore, a voltage compensator is needed. A first attempt to achieve capacitor voltage balance based on a proportional feedback is presented. The method is able to preserve constant switching frequencies on the devices and introduces no distortion in the output voltages. Nevertheless, for optimal balancing performance, the constant parameter k_p of the compensator needs to be readjusted depending on the operating conditions of the converter. Furthermore, if excessive compensation is applied to this system, the resulting balancing dynamic is slower and instability may be produced. Thus, a second compensator able to overcome these drawbacks is presented. The approach consists in adjusting a proper offset to the modulation signals and produces optimal balancing results for all converter operating conditions. This solution also determines the dynamic compensation limits, which ensures that overcompensation cannot be produced.

Both the dynamic limiter and optimal controller approaches can be applied to the modulation techniques DSPWM and (Busquets-Monge et al. 2004).

The optimal compensator presented here guarantees maximum balancing without decreasing the quality of the output voltage waveforms. The proposed algorithm presents a number of advantages: most importantly, it does not require any parameter adjustment and it operates optimally under all of the system's operating conditions. In addition, stability is always guaranteed.

The DSPWM and the optimal compensator proposed in this chapter provide a definitive solution to the voltage-balancing problem in NPC converters by preventing low-frequency voltage oscillation at the NP and compensating for any initial imbalance between the voltages on the dc-link capacitors in a very short time.

The main drawbacks of the DSPWM strategy are that the switching frequencies are increased compared to other modulation techniques, and that the output voltage spectra are worse. However, the additional distortion is produced at high frequency (around the switching frequency and above) and therefore can be easily filtered.

This DSPWM with the optimal compensator will help to extend the use of the NPC converter to lower-power applications. One reason for this is that the modulation algorithm can be straightforwardly implemented in a very simple microprocessor. Furthermore, since there is no longer low-frequency voltage oscillation at the NP, the values of the dc-link capacitors can be significantly reduced. An interesting application could be the use of MOSFETs for the synthesis of the NPC converter operating at about 600 V in the dc bus. Since the NP voltage never oscillates, the devices would only have to support half of the dc-link voltage.

The proposed modulation strategy with the optimal compensator is very promising in applications such as active filtering, in which the current harmonics are not at fundamental frequency. Under such conditions, other modulation schemes, such as NTV modulation, may produce instability in the system when operating with certain current harmonics (Pou et al. 2005a). Another application field of the proposed strategy can be static reactive compensation (STATCOM), where NTV produces high NP voltage oscillation amplitudes because the converter operates at nearly a zero power factor.

4.4. Chapter References

Busquets-Monge S, Bordonau J, Boroyevich D, Somavilla S. 2004. The nearest three virtual space vector PWM - a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter. Power Electronics Letters, IEEE 2: 11-15.

Busquets-Monge S, Ortega JD, Bordonau J, Beristain JA, Rocabert J. 2008. Closed-Loop Control of a Three-Phase Neutral-Point-Clamped Inverter Using an Optimized Virtual-Vector-Based Pulsewidth Modulation. Industrial Electronics, IEEE Transactions on 55: 2061-2071.

Celanovic N, Boroyevich D. 2000. A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. Power Electronics, IEEE Transactions on 15: 242-249.

Liu HL, Choi NS, Cho GH. 1991. DSP based space vector PWM for three-level inverter with DC-link voltage balancing. Pages 197-203 vol.191. Industrial Electronics, Control and Instrumentation, 1991. Proceedings. IECON '91., 1991 International Conference on.

Nabae A, Takahashi I, Akagi H. 1981. A New Neutral-Point-Clamped PWM Inverter. Industry Applications, IEEE Transactions on IA-17: 518-523.

Newton C, Sumner M. 1997. Neutral point control for multi-level inverters: theory, design and operational limitations. Pages 1336-1343 vol.1332. Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE.

Pou J, Boroyevich D, Pindado R. 2002. New feedforward space-vector PWM method to obtain balanced AC output voltages in a three-level neutral-point-clamped converter. Industrial Electronics, IEEE Transactions on 49: 1026-1034.

—. 2005a. Effects of imbalances and nonlinear loads on the voltage balance of a neutral-point-clamped inverter. Power Electronics, IEEE Transactions on 20: 123-131.

Pou J, Pindado R, Boroyevich D, Rodriguez P. 2004. Limits of the neutral-point balance in back-to-back-connected three-level converters. Power Electronics, IEEE Transactions on 19: 722-731.

Pou J, Rodriguez P, Zaragoza J, Sala V, Jaen C, Boroyevich D. 2005b. Enhancement of Carrier-Based Modulation Strategies for Multilevel Converters. Pages 2534-2539. Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th.

Pou J, Zaragoza J, Rodriguez P, Ceballos S, Sala VM, Burgos RP, Boroyevich D. 2007. Fast-Processing Modulation Strategy for the Neutral-Point-Clamped Converter With Total Elimination of Low-Frequency Voltage Oscillations in the Neutral Point. Industrial Electronics, IEEE Transactions on 54: 2288-2294.

Sun-Kyoung L, Jun-Ha K, Kwanghee N. 1999. A DC-link voltage balancing algorithm for 3-level converter using the zero sequence current. Pages 1083-1088 vol.1082. Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE.

Tallam RM, Naik R, Nondahl TA. 2005. A carrier-based PWM scheme for neutral-point voltage balancing in three-level inverters. Industry Applications, IEEE Transactions on 41: 1734-1743.

Chapter 5.

Carrier-Based Hybrid PWM

This chapter presents a hybrid modulation technique for the three-level NPC converter. A modulation strategy, based on two modulation signals per phase, was presented previously in Chapter 4. This strategy completely removes the low-frequency voltage oscillations that appear at the NP in some operating conditions. However, a major drawback is that it significantly increases the switching losses of the converter. The proposal in this chapter combines such a modulation strategy with SPWM. The main characteristic of this hybrid pulse-width modulation (HPWM) is the reduction in switching losses at the cost of some low-frequency voltage oscillations at the NP. The amplitude of these oscillations can be controlled by varying the combination of the two strategies. The performance of the hybrid modulation is analyzed and compared with the original strategies. Power losses and oscillation amplitudes on the dc-link capacitors are evaluated. Experimental results show how the hybrid modulation performs by balancing the dc-link capacitors.

A tracking method is also proposed in this chapter in order to achieve the maximum reduction of the voltage oscillation amplitudes in HPWM. This method

defines the best intervals in which SPWM should be used. Consequently, the low-frequency NP voltage oscillation is further minimized. Some simulation results are presented to show good performance of the proposed strategy and are compared with the non-tracking method.

The maximum amplitude of the NP voltage oscillations can be regulated thanks to a controller, which defines the exact degree of mixture between the two modulation strategies. The use of the proposed controller limits the maximum amplitude of the NP voltage oscillations; hence, the power devices and the dc-link capacitors of the converter can be designed for these maximum voltage specifications. Some simulation and experimental results are presented.

5.1. Hybrid PWM based on SPWM and DSPWM

The HPWM proposed in this chapter combines DSPWM with SPWM. The main characteristic of HPWM is the reduction in switching losses, at the cost of some low-frequency voltage oscillations at the NP. The amplitude of these oscillations can be controlled by varying the combination of the two strategies. Furthermore, HPWM is implemented using a simple algorithm, and hence it can be processed very quickly.
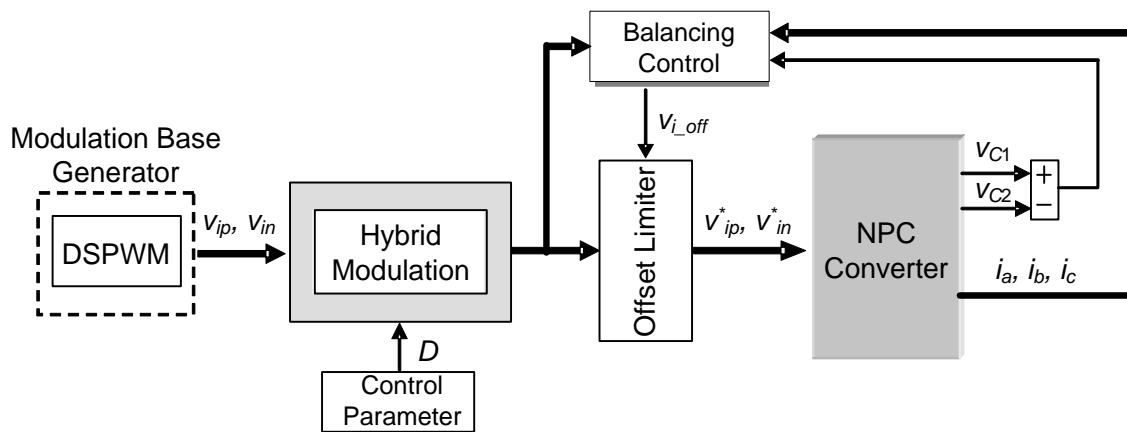
Fig.5.1. Scheme of HPWM.

Fig.5.1 shows the general structure of the system, including the HPWM block, which is responsible for generating new modulation signals. The balancing control block is based on (Zaragoza, Pou et al. 2009), described in Chapter 4, which provides a proper offset to facilitate voltage balance between the dc-link capacitors. Other balancing strategies can be found in the literature (Busquets-Monge, Somavilla et al. 2007; Pou, Zaragoza et al. 2007; Busquets-Monge, Ortega et al. 2008).

5.1.1. Basis of the Method

Fig.5.2 shows modulation signals for DSPWM and SPWM. Note that, in order to achieve the same range as DSPWM in the linear operation mode, the SPWM signals include the zero sequence obtained from the SVM patterns (4.1). In this example, one of the DSPWM modulation signals coincides with the SPWM signal for the intervals $0 \leq \omega t \leq \pi/3$, $2\pi/3 \leq \omega t \leq 4\pi/3$ and $5\pi/3 \leq \omega t \leq 2\pi$. In these intervals, the other DSPWM modulation signal is clamped to zero. Consequently, the switching patterns

of the switches are the same as those obtained with SPWM. Therefore, the switching patterns differ only for the duration of the other intervals $\pi/3 \le \omega t \le 2\pi/3$ and $4\pi/3 \le \omega t \le 5\pi/3$. HPWM is based on clamping one modulation signal for some time during the uncommon intervals. This brings DSPWM closer to SPWM. As the modulation signals are clamped to zero for some additional time, this leads to the switching frequency of the transistors being reduced. Thus, their switching losses also decrease. The exact combination is defined by a sharing variable *D*, which can take values within the interval [0, 1]. If the parameter *D* takes the extreme values zero or unity, the HPWM becomes DSPWM or SPWM, respectively.

Fig.5.3 shows that when the modulation signal from SPWM crosses zero, the absolute value of the DSPWM modulation signals is exactly half the modulation index (*m*/2), *m* being the amplitude of the modulation signals. This fact is used to determine the extension of the common interval directly from the instantaneous values of the modulation signals obtained from DSPWM. The variable *x* used for this is:

$$x = D\frac{m}{2}. \tag{5.1}$$

The modulation signals are compared with the value of *x* to determine the additional intervals in which these signals need to be clamped in order to extend SPWM patterns further. Fig.5.3 shows an example in which D=0.5; one of the modulation signals is clamped to zero during 50% of the uncommon intervals (SPWM is applied). This is performed by applying the following conditions:

$$\begin{cases} \text{if } (v_{ip} \le x) \text{ then } v_{i\_off\_HPWM} = v_{ip} \text{ else } v_{i\_off\_HPWM} = 0 \quad \text{and} \\ \text{if } (-v_{in} \le x) \text{ then } v_{i\_off\_HPWM} = -v_{in} \text{ else } v_{i\_off\_HPWM} = 0, \end{cases} \tag{5.2}$$

in which $v_{i\_off\_HPWM}$ for *i*= {*a*, *b*, *c*} is the offset that should be applied to the DSPWM signals of phase *i* to extend their zero clamping. In order to fulfill (4.2) and avoid low-frequency distortion of the output voltages, any modification applied to a modulation signal (for example, v_{in}) should have the sign opposite to the other signal (v_{ip}). This principle is observed by using the following relationships:

$$\begin{cases} v_{ip\_HPWM} = v_{ip} - v_{i\_off\_HPWM} & \text{and} \\ v_{in\_HPWM} = v_{in} + v_{i\_off\_HPWM}. \end{cases} \tag{5.3}$$
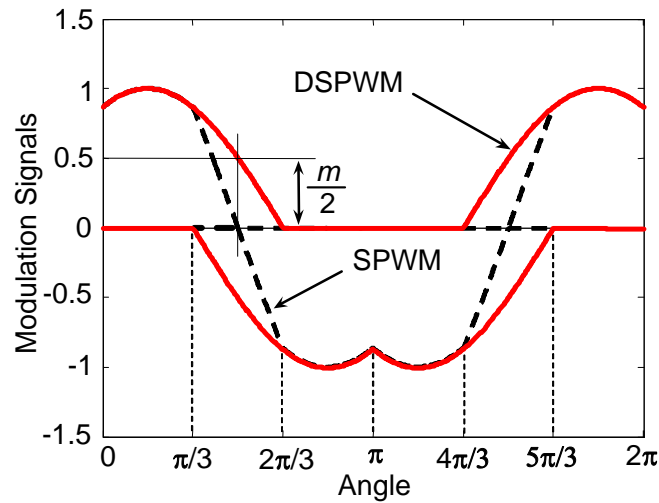
Fig.5.2. Modulation signals for the DSPWM and SPWM techniques.
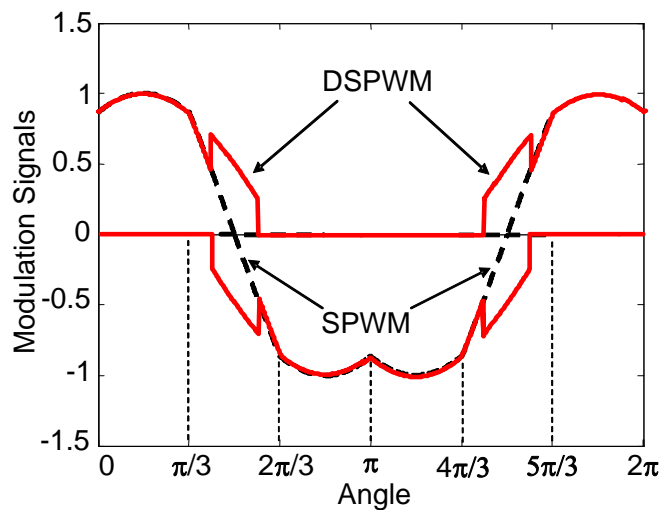
Fig.5.3. Modulation signals for the HPWM.

This modification of the modulation signals is applied to the waveforms in Fig.5.3. In this figure, during $\pi/3 \le \omega t \le 2\pi/3$ and $4\pi/3 \le \omega t \le 5\pi/3$, the modulation signals of HPWM match the waveforms of DSPWM for some intervals and SPWM for others. During the intervals in which the HPWM signals coincide with SPWM, one modulation signal matches it while the other is clamped to zero. This produces the same switching patterns for the transistors as for SPWM.

5.1.2. Simulation Results

HPWM waveforms and Total Harmonic Distortion analysis

The HPWM is initially implemented and tested by simulation using the MATLAB/SIMULINK software. The values for all these simulation examples are: V_{dc}=1,800 V and a resistive-inductive Wye-connected load with R=1 Ω and L=2 mH, respectively. The value for the dc-link capacitors is C=2,200 µF and the fundamental frequency of the ac voltage is f=50 Hz. The values of the THD and WTHD given in the figures consider the definitions given in Appendix D.

Fig.5.4 shows the voltages of the dc-link capacitors (v_{C1} and v_{C2}), a line-to-line voltage (v_{ab}) and the output currents (i_a, i_b, and i_c) when the converter operates with a carrier frequency f_s=5 kHz. Note that, for all the modulation indexes, the voltages in the dc-link capacitors do not contain any low-frequency oscillation. Note also, however, that the switching frequencies of the devices increase with the modulation index. This is because, in DSPWM, there are intervals in which the line-to-line voltages commutate among three states of the converter instead of two. The THD and WTHD values are worse when compared to SPWM. However, the additional distortion is produced at high frequency (around the switching frequency and above) and therefore can be easily filtered.

The quality of the output voltage waveforms from HPWM is evaluated. The THD and WTHD (or DF1) are the parameters used for the quantification.

Fig.5.5 shows THD values of the line-to-line output voltages for *D* ranging from zero to unity. In such analyses, the calculated values of the THD are practically independent of the frequency-modulation ratio (m_f=f_s/f_m). Note that the THD decreases when *D* approaches the unity value (SPWM). WTHD values are shown in Fig.5.6. This parameter considers the harmonic order (*n*) with respect to the fundamental frequency, so that low-order harmonics weigh more in the calculated value. Consequently, the WTHD values are strongly dependent on m_f. In this evaluation, the modulation signals are sampled at the carrier frequency rate. A discrete controller is assumed to make the analysis more realistic. Thus, the curves

show some steps. As expected, the WTHD values are lower when the parameter *D* takes values closer to unity and when m_f increases.
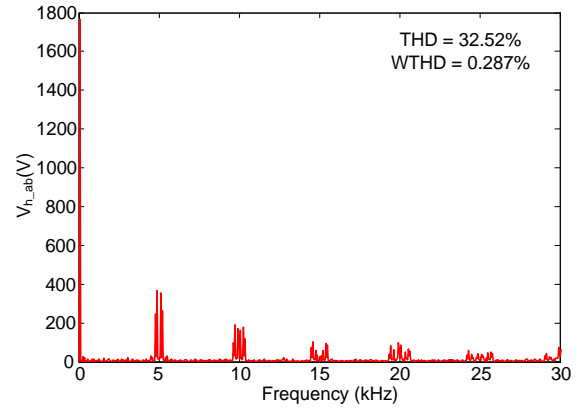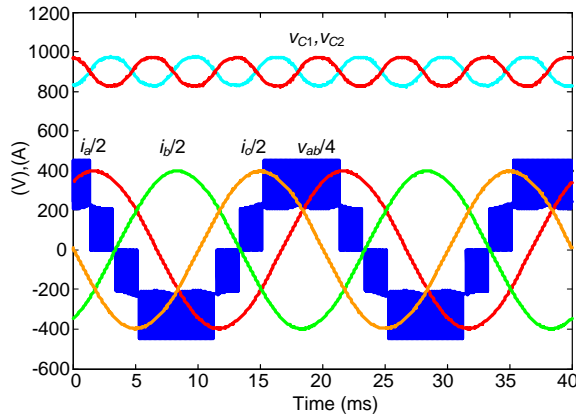
(a)
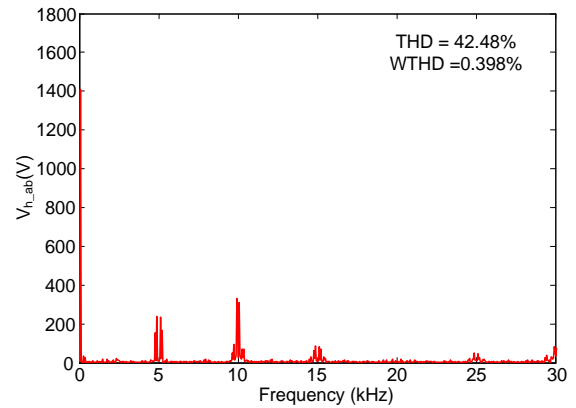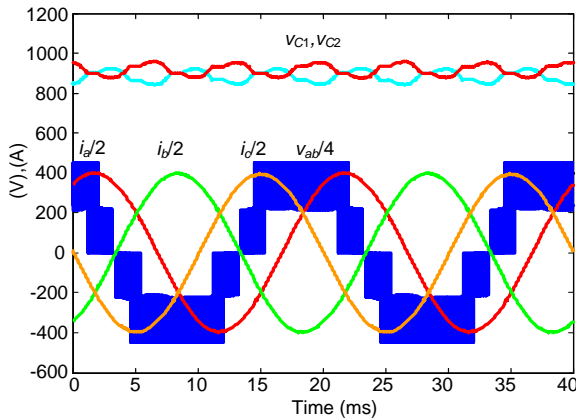
(b)
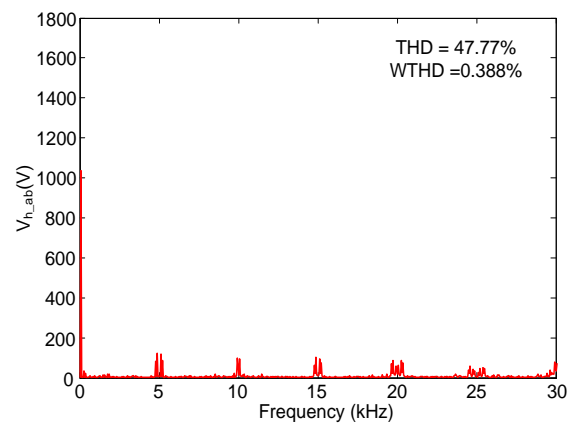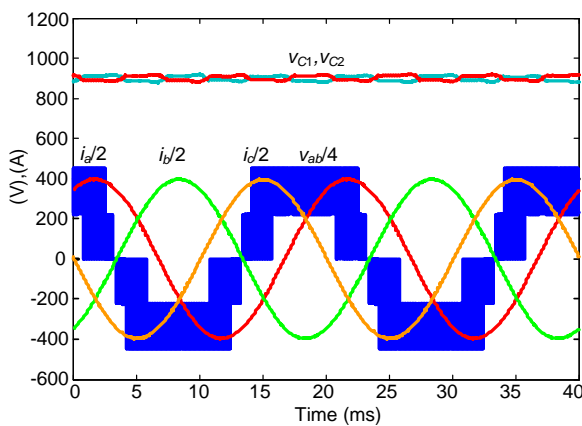
(c)
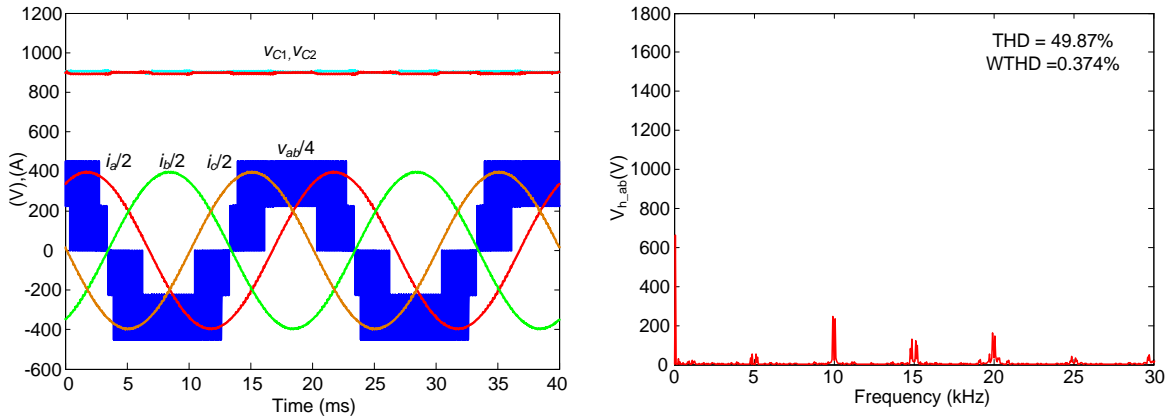
(d)
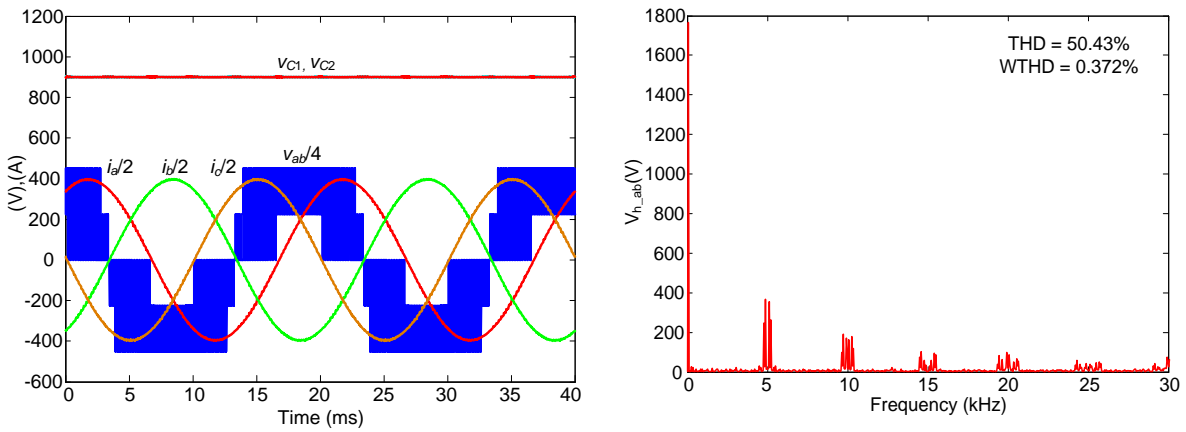
(e)

Fig.5.4. Simulation results of HPWM: (a) *D*=1; (b) *D*=0.75; (c) *D*=0.5; (d) *D*=0.25; (e) *D*=0.
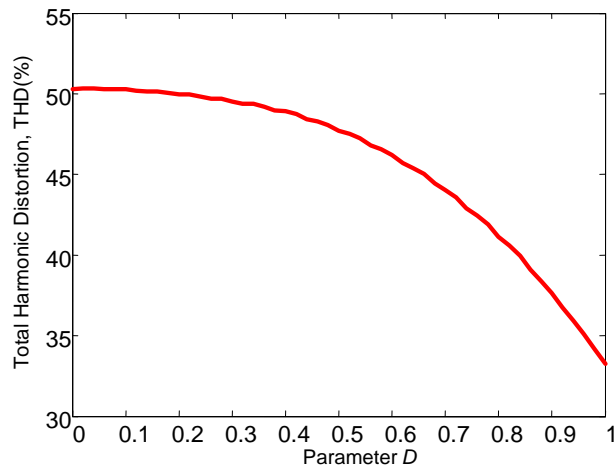
Fig.5.5. THD values of the HPWM.
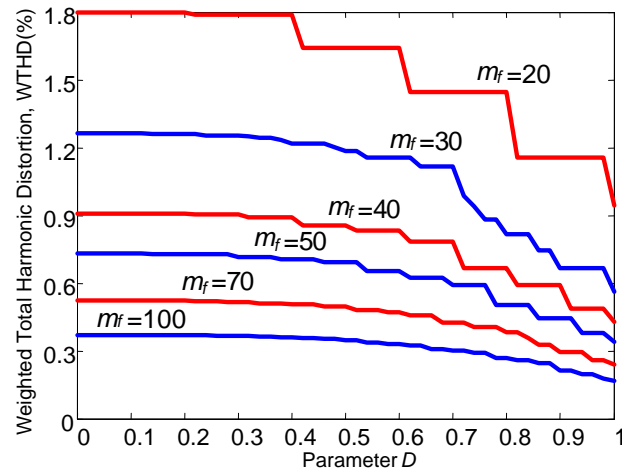
Fig.5.6. WTHD values of the HPWM.

Loss analysis

The MATLAB/SIMULINK model of an NPC converter has been used to calculate losses. The converter rated power is 2.8 MVA (1,700 V / 950 A, V_{dc}=2,400 V). In all simulations, the ac output currents are assumed to be constant at their rated values and the sampling frequency is f_s=5 kHz (carriers' frequency).

The IGBTs selected are the DIM1200NSM17-E000, whose maximum ratings are a forward current of 1,200 A and a direct voltage of 1,700 V. In the following analysis, the model of the IGBTs is based on the typical curves given by the manufacturer. The method used to calculate the conduction and switching losses in the converter is explained in Appendix C.

Fig.5.7 shows the conduction losses obtained using SPWM, DSPWM and HPWM with *D*= 0.5. Since the difference between the losses obtained in the three modulation techniques is less than 1%, only one representation is given.

Fig.5.8 and Fig.5.9 show the switching losses obtained in this example for SPWM and DSPWM, respectively. These modulation strategies are obtained by imposing the parameter *D* on extreme values (unity and zero, respectively).

The switching losses in DSPWM take higher values than in SPWM. Moreover, in SPWM the maximum switching losses are obtained by operating around the unity power factor, whereas in DSPWM they are the minimum.
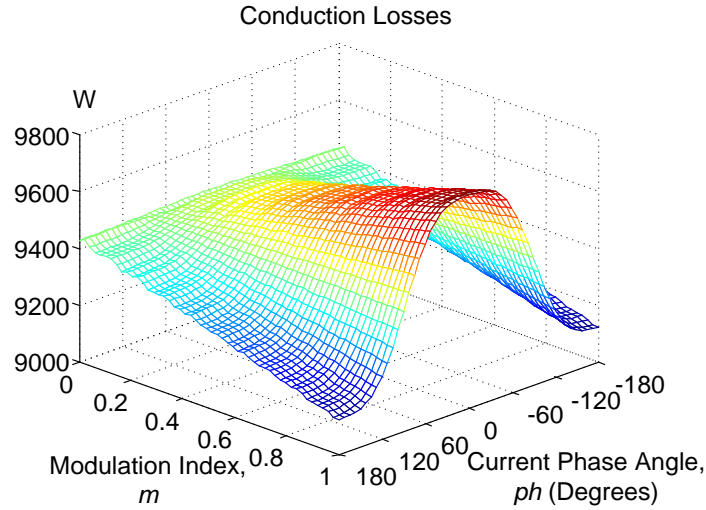
Fig.5.7. Conduction losses obtained using SPWM, DSPWM, and HPWM with *D*=0.5.
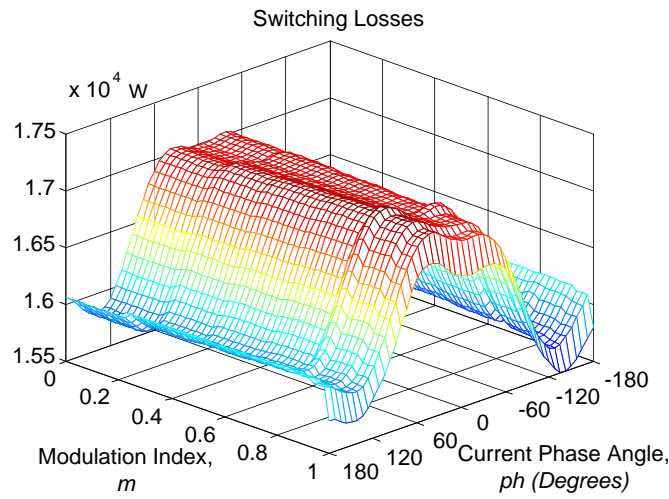
Fig.5.8. Switching losses using SPWM (*D*=1).
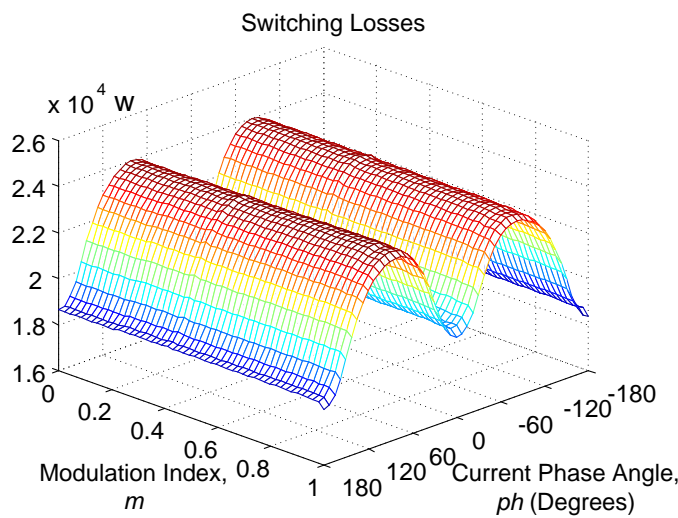
Fig.5.9. Switching losses using DSPWM (*D*=0).

Fig.5.10 shows the switching losses of HPWM with a 50% combination (*D*=0.5). These losses take values between SPWM and DSPWM, as expected.

Fig.5.11 shows the ratio of total losses between DSPWM and SPWM techniques. In the worst case, the maximum ratio is up by about 28%.

Fig.5.12 illustrates the same ratio for *D*=0.5. In this case, the maximum losses are about 16% higher for HPWM and the minimum value is about 4%. As total losses show very little dependence on the value of the modulation index, this variable can be omitted from the representations. Fig.5.13 summarizes the total loss ratio for different combinations using the parameter *D*.
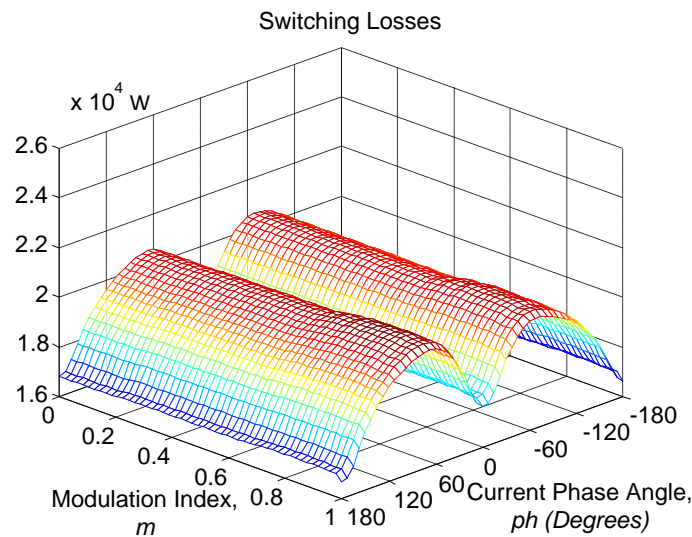
Fig.5.10. Switching losses using HPWM for *D*=0.5.
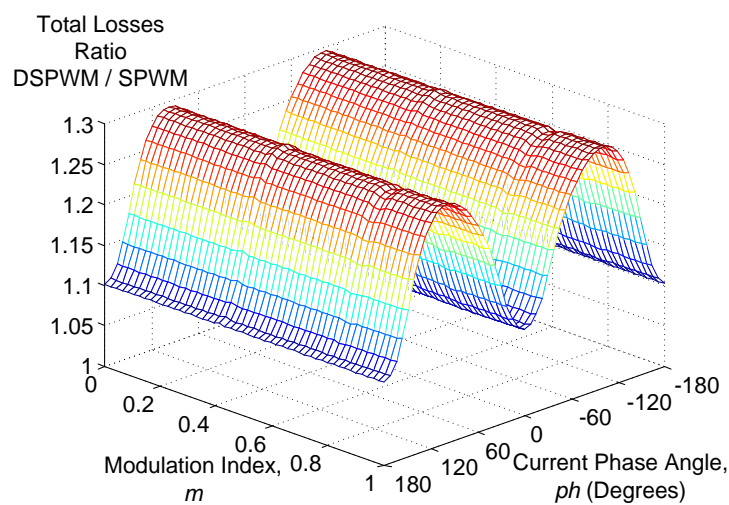
Fig.5.11. Ratio of total losses DSPWM / SPWM.
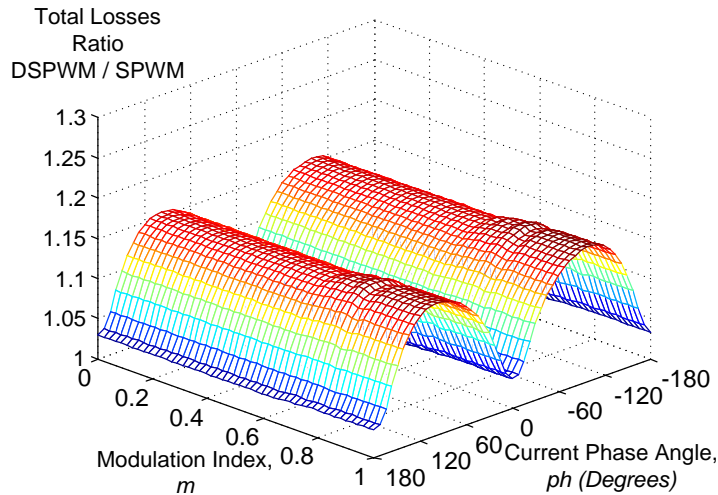
Fig.5.12. Ratio of total losses HPWM / SPWM for *D*=0.5
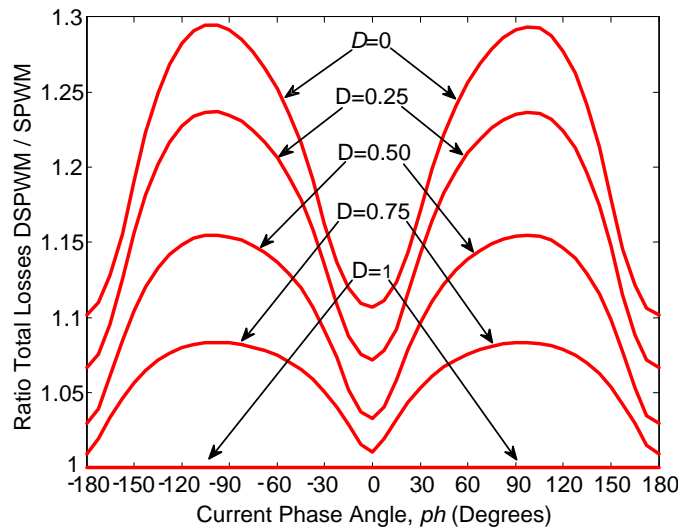
Fig.5.13. Ratio of total losses HPWM / SPWM for different *D* values

As expected, the loss reduction depends on how long the modulation signals are clamped to the zero value. Furthermore, the total losses ratio takes the minimum value for the unity-power-factor operation mode.

NP Voltage oscillations

The maximum low-frequency NP voltage amplitudes that occur under specific operating conditions of the converter are analyzed. The normalized amplitude of the ripple ($\Delta V_{NPn}/2$) is defined in Appendix E.

Fig.5.14 shows the low-frequency NP voltage amplitudes under SPWM, including the zero sequence from SVM given in (4.1). Again, the output currents are

assumed to be sinusoidal and all possible phase angles related to the output voltage fundamentals are analyzed. Switching-frequency voltage ripples are not considered in this study, as they are less significant than the low-frequency voltage oscillations. This analysis is thus independent of the switching frequency.

Fig.5.15 shows the amplitude of the NP voltage oscillations under HPWM for *D*= 0.5. These amplitudes are much lower than SPWM amplitudes for all operating conditions, especially for power factors that are far from unity.

Fig.5.16 illustrates such a reduction. It shows the ratio of low-frequency NP voltage amplitudes between SPWM and HPWM for different values of *D*.
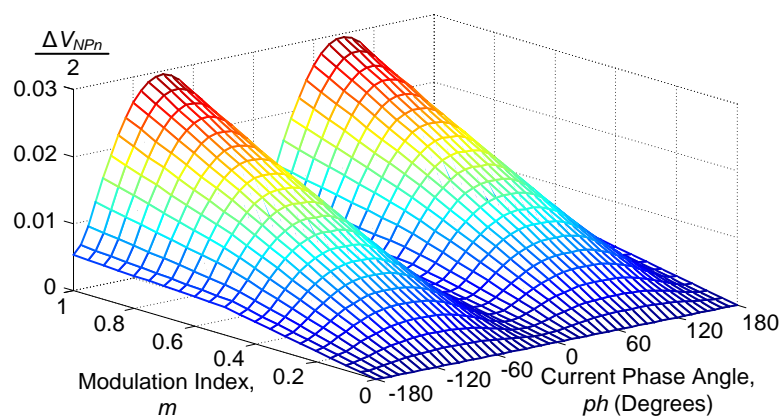
Fig.5.14. Normalized low-frequency NP voltage amplitudes in SPWM.
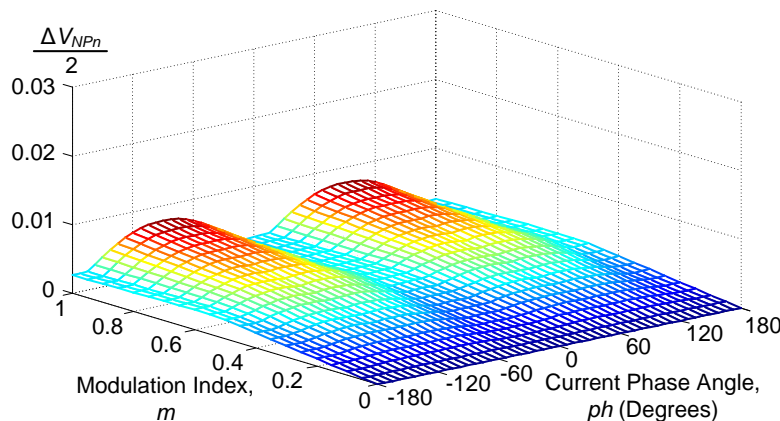
Fig.5.15. Normalized low-frequency NP voltage amplitudes in HPWM with *D*=0.5.

A closed-loop control can be designed to calculate the value of the variable *D*, in order to limit the maximum amplitude of the NP voltage oscillations. The converter should normally operate under SPWM unless the NP voltage oscillation tends to be larger than a predefined maximum value. In such a case, the controller should

provide a proper value of *D* to regulate the oscillation amplitude to that maximum value.
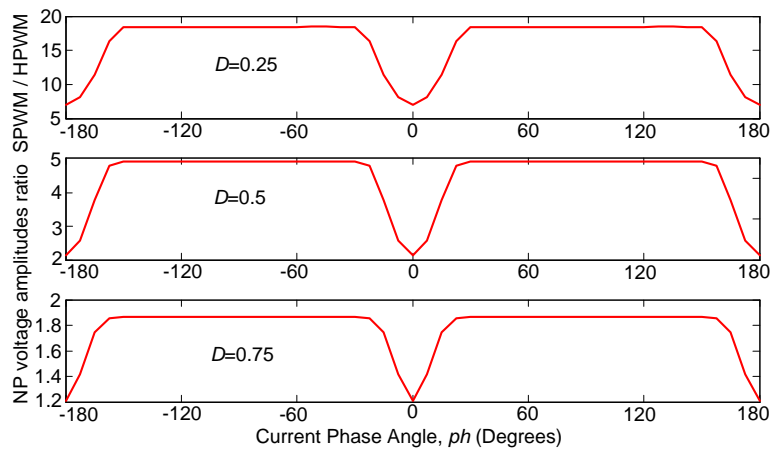
Fig.5.16. Normalized low-frequency NP voltage amplitudes in SPWM.

5.1.3. Experimental Results

Experimental validation of HPWM was performed under the following conditions: a dc-link voltage of V_{dc} =115 V, dc-link capacitors of *C*=2,200 µF and a Wye-connected resistive-inductance load with *R*=11.5 Ω and *L*=12 mH. The HPWM technique was programmed on a DSP board, TMS320F2812. The frequency used for the triangular carriers was f_s=5 kHz.

The results shown from Fig.5.17(a) to Fig.5.17(e) were obtained with an output frequency *f*=10 Hz and a modulation index *m*= 0.9. The waveforms illustrated in these figures are the voltages in the dc-link capacitors, a line-to-line voltage, and the output currents.

In Fig.5.17(a), the waveforms correspond to the use of the proposed HPWM technique. In this case, the factor *D* is defined as unity, which means 100% of SPWM and 0% of DSPWM. Note that there is a significant low-frequency voltage oscillation.

In Fig.5.17(b), the waveforms were obtained using HPWM with a factor *D*= 0.75 (75% SPWM and 25% DSPWM). This figure shows significant amplitude of the voltage oscillations in the dc-link capacitors (about 75% with respect to SPWM). There are short intervals in which the line-to-line voltages commutate among three levels.

In Fig.5.17(c), the parameter D is defined as 0.5, which means 50% of SPWM and 50% of DSPWM. In this case, the amplitude of the oscillations is reduced further than in the previous case (Fig.5.17(a)). Two zones can be distinguished in these voltage waveforms. One corresponds to the application of DSPWM, in which the voltages remain constant. The other corresponds to SPWM. In this case, the voltages tend to oscillate. In addition, there are intervals in which the line-to-line voltages commutate among three levels. In such intervals, the switching frequencies of the power devices increase.

In this example, the use of HPWM with a factor D=0.5 implies a reduction of about 50% in the amplitude of the oscillations. This attenuation value can be verified using the curves in Fig.5.16.

In Fig.5.17(d), the waveforms were obtained using HPWM with a factor D= 0.25 (25% SPWM and 75% DSPWM). This figure shows a significant reduction in the amplitude of the voltage oscillations in the dc-link capacitors (about 75% with respect to SPWM). There are longer intervals in which the line-to-line voltages commutate among three levels.

In Fig.5.17(e), the parameter D is defined as zero. This figure shows a complete absence of low-frequency voltage oscillations.

(a)   (b)

(c)

(d)

(e)
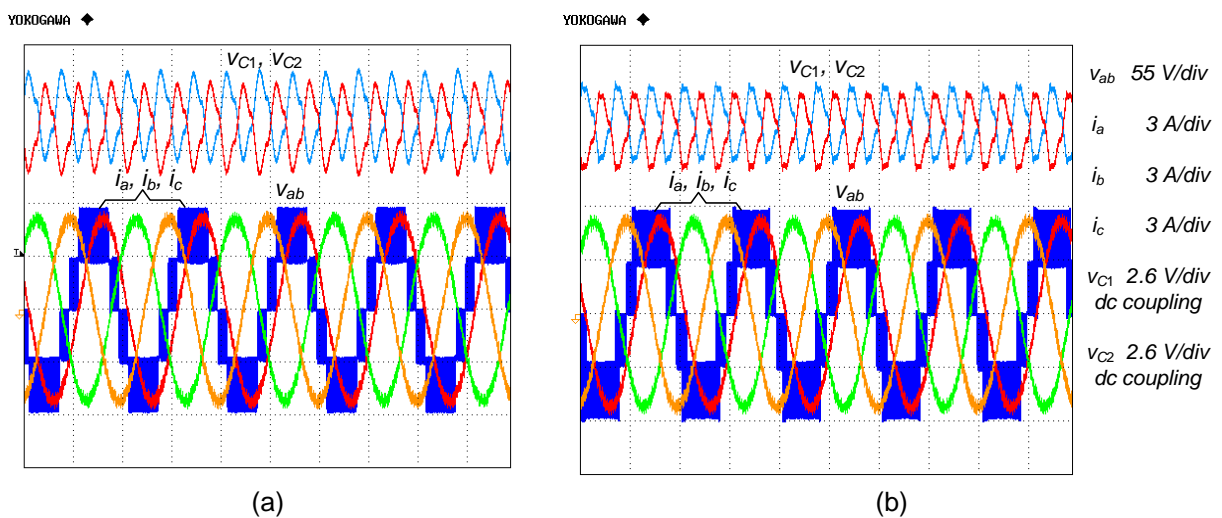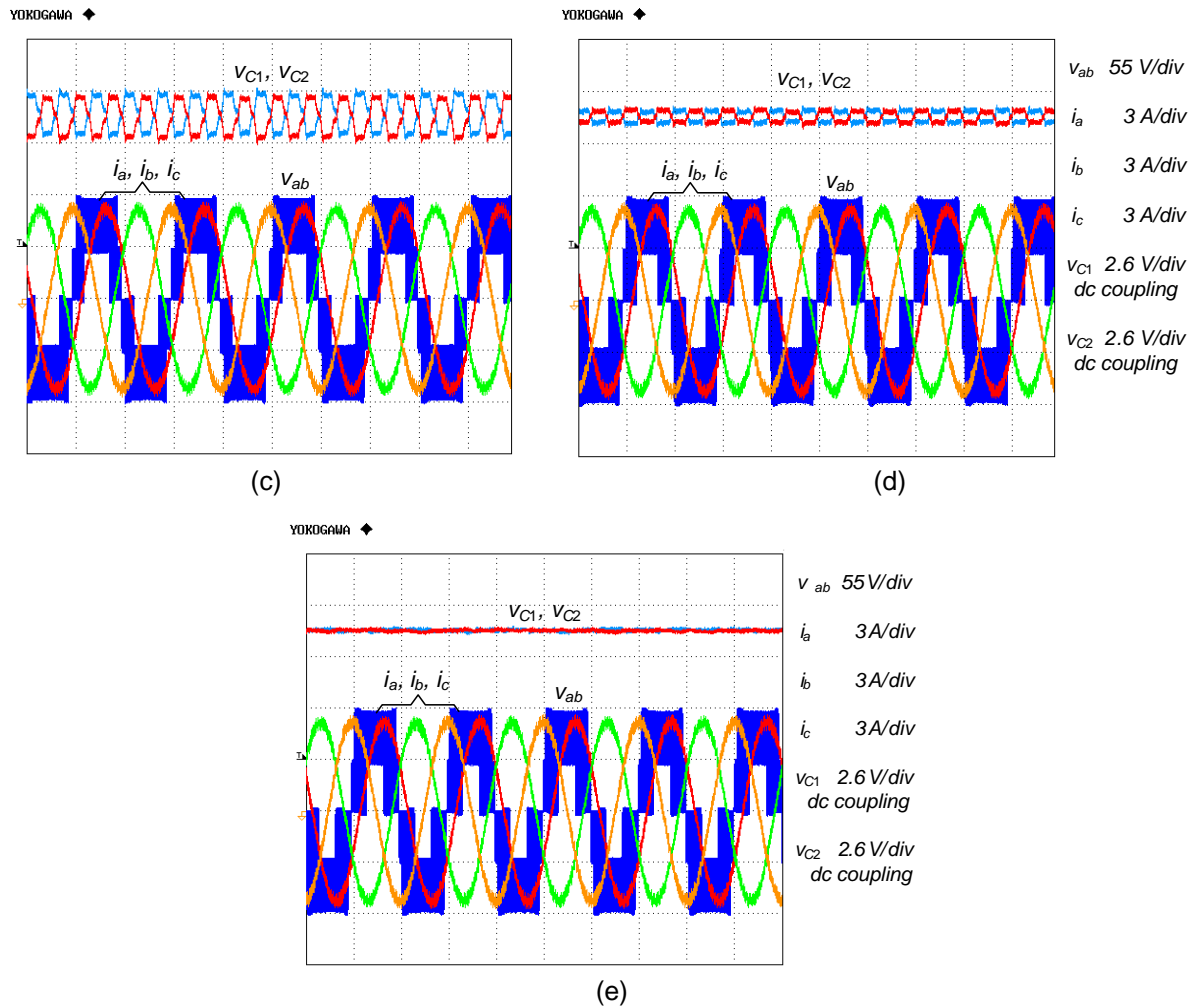
Fig.5.17. Experimental results of HPWM: (a) *D*=1; (b) *D*=0.75; (c) *D*=0.5; (d) *D*=0.25; (e) *D*=0.

Fig.5.18 shows power losses in this prototype for different values of the parameter *D.* As expected, the power losses decrease when *D* increases. However, the power reduction is very small. This is because in this low-power laboratory prototype, the switching losses represent only about 15% of the total losses. In a practical high-power system, such as the one assumed in the simulation results, switching losses are usually higher than conduction losses. Therefore, saving switching losses becomes important for improving the efficiency of the system.

Fig.5.18 also presents the simulation results of the power losses in this prototype. Since the simulation results are very close to the experimental ones, validity of the simulation model is corroborated.
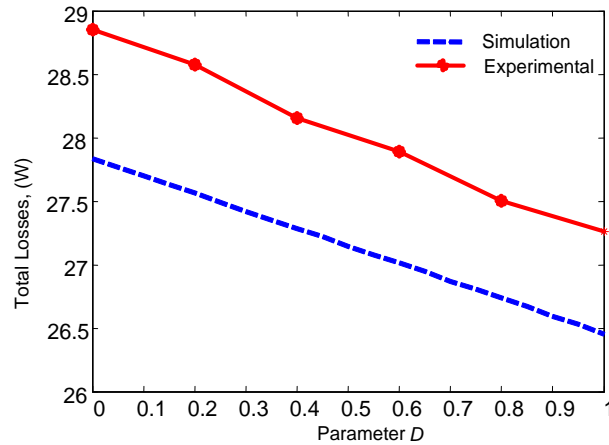
Fig.5.18. Power losses from the low-power prototype.

5.2. Tracking Method in the Hybrid Modulation.

Once the value of parameter *D* is defined, the best interval for using SPWM has to be determined. The goal of the tracking method proposed in this section is to try to make the NP voltage oscillations as small as possible. This is achieved if the clamping is produced where the absolute values of the NP current under SPWM are as minimal as possible. Some simulation results are presented to show the good performance of the proposed tracking method. Those results are compared with the ones obtained from the non-tracking method.

5.2.1. Tracking Method for NP Voltage Oscillation Minimization

In the proposed tracking method, the extension of the clamping intervals is achieved through a pulsed signal whose frequency is six times the output fundamental frequency. The pulse width of this waveform defines the exact combination (parameter *D*), and its relative position (parameter *ψ*) determines the tracking interval of the modulation signals. Some examples are represented in Fig.5.19. Observe that when the pulse signal is in high level, SPWM is applied; otherwise, the modulation signals follow DSPWM patterns. Note that if a pulse is activated during the intervals in which one of the modulation signals is already clamped, no change occurs because the modulation signals are exactly the same for both basic strategies, SPWM and DSPWM.

During the intervals in which the modulation signals are clamped further, SPWM is applied. Therefore, a low-frequency oscillation in the NP voltage will appear. The amplitude of this oscillation depends on the NP current values.

According to Chapter 4, equation (4.6), the locally-averaged NP current can be determined as follows:

$$\bar{i}_0 = \left(1 + v_{an} - v_{ap}\right)\bar{i}_a + \left(1 + v_{bn} - v_{bp}\right)\bar{i}_b + \left(1 + v_{cn} - v_{cp}\right)\bar{i}_c . \tag{5.4}$$

In the case that SPWM were applied continuously, this current would be expressed as:

$$\bar{i}'_0 = \left(1 + v'_{an} - v'_{ap}\right)\bar{i}_a + \left(1 + v'_{bn} - v'_{bp}\right)\bar{i}_b + \left(1 + v'_{cn} - v'_{cp}\right)\bar{i}_c , \tag{5.5}$$

(a)

(b)
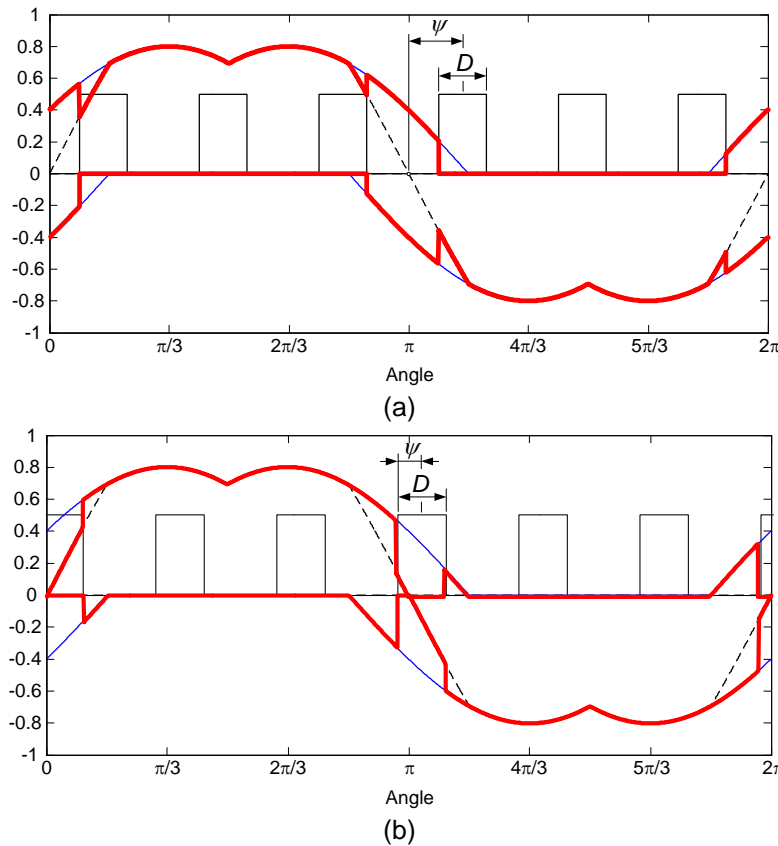
Fig.5.19. Clamping intervals defined from the parameters D and ψ.

in which v'_{in} and v'_{ip} for $i = \{a, b, c\}$ are the modulation signals under the assumption of SPWM.

If the system operates with HPWM, the locally-averaged NP current is obtained from the general expression (5.4). However, the current values are exactly the same as those calculated from (5.5) for the intervals in which SPWM is applied:

$$\bar{i}_{0 \ (Intervals\,of\,SPWM)} = \bar{i}_0'. \tag{5.6}$$

The tracking method is based on calculating on-line $\bar{i}_0'$ from (5.5) and determining the instants in which this current crosses zero. During those intervals, SPWM can be applied because the NP current takes low values and hence produces small NP voltage imbalances. Therefore, every time that $\bar{i}_0'$ crosses zero, the position parameter for the clamping interval (ψ) is updated, so that the pulse center of the clamping control coincides with this zero crossing instant. This is illustrated in Fig.5.20.

Fig.5.21 shows the main blocks of the tracking algorithm. The Pulse Position Block defines the correct position of the six pulses within a modulation period. This block shifts the position of the pulses according to the value of the parameter ψ. Such pulses are originally synchronized with the modulation signals and shifted properly after the Pulse Position Block.

For the calculation of ψ the locally-averaged NP current (assuming SPWM), the parameter D, and the modulation signals are needed.
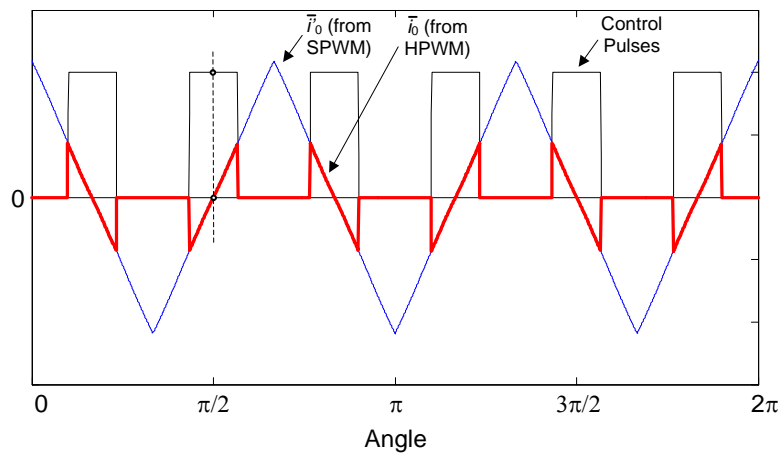
Fig.5.20. Tracking example.

The Hybrid Modulation Block multiplexes the input modulation signals SPWM and DSPWM, so that it switches from one to another, producing the HPWM.
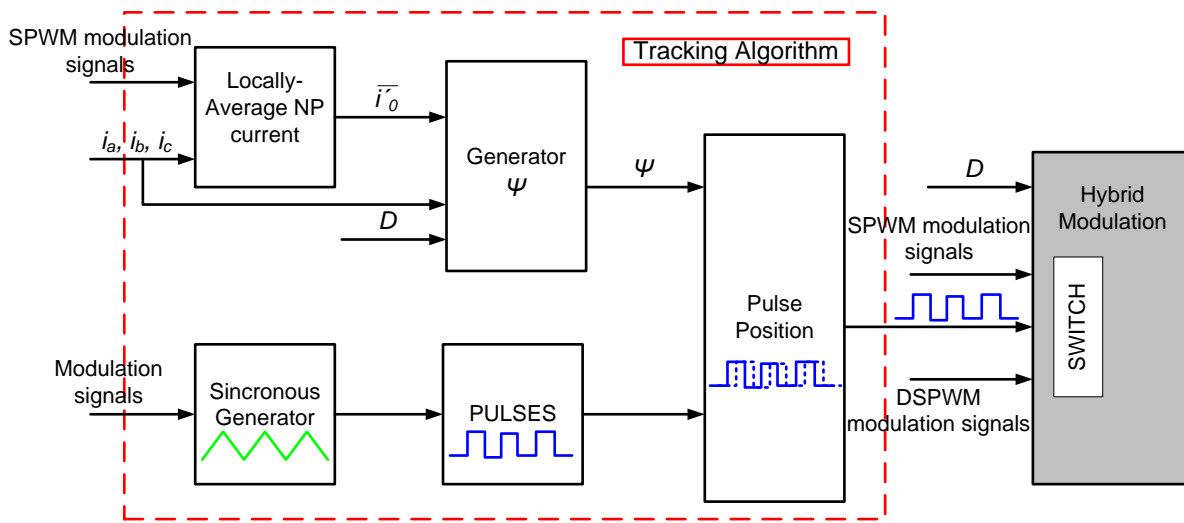
Fig.5.21.Tracking algorithm.

5.2.2. Simulation Results

The proposed tracking method is implemented and tested by simulation using the MATLAB/SIMULINK software. The values for all these simulation examples are: V_{dc}=1,800 V and a resistive-inductive Wye-connected load with R=1 Ω and L=2 mH, respectively. The value for the dc-link capacitors is C=2,200 μF and the fundamental frequency of the ac voltage is f=50 Hz.

The voltage amplitudes in the dc-link capacitors, using both the non-tracking and the tracking methods, are shown in Fig.5.22. The exact combination of the modulation signals in this figure is 50% (D=0.5) in both cases. In the upper one, the basic HPWM is applied (non-tracking method), which is equivalent to defining ψ=0.5. For the lower one, the proposed tracking method for achieving the minimum amplitude for the dc-link capacitors is used. In that case, the parameter ψ is determined as explained in the previous Section and self-adjusted to ψ=0.85. The additional attenuation, clearly shown in this example, is obtained thanks to the tracking method. The last representation of Fig.5.22 shows the parameter ψ. One can observe that the dynamic of this parameter is very fast in finding out the best value for minimizing the low frequency voltage oscillations.

Fig.5.23. illustrates how the voltage oscillations in the capacitors are minimized for different loads (R). This figure shows that when $\bar{i}'_0$ crosses zero, the position parameter for the clamping interval (ψ) is updated. One can observe that the pulse center of the clamping control coincides very quickly with this zero crossing instant.
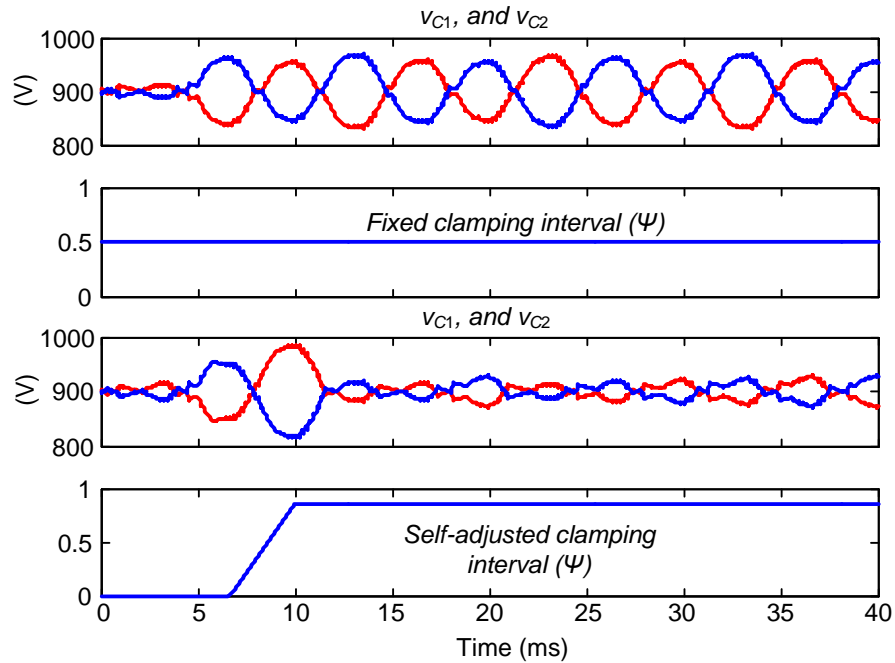
Fig.5.22. Voltage amplitudes in the dc-link capacitors using both the non-tracking and the tracking methods.
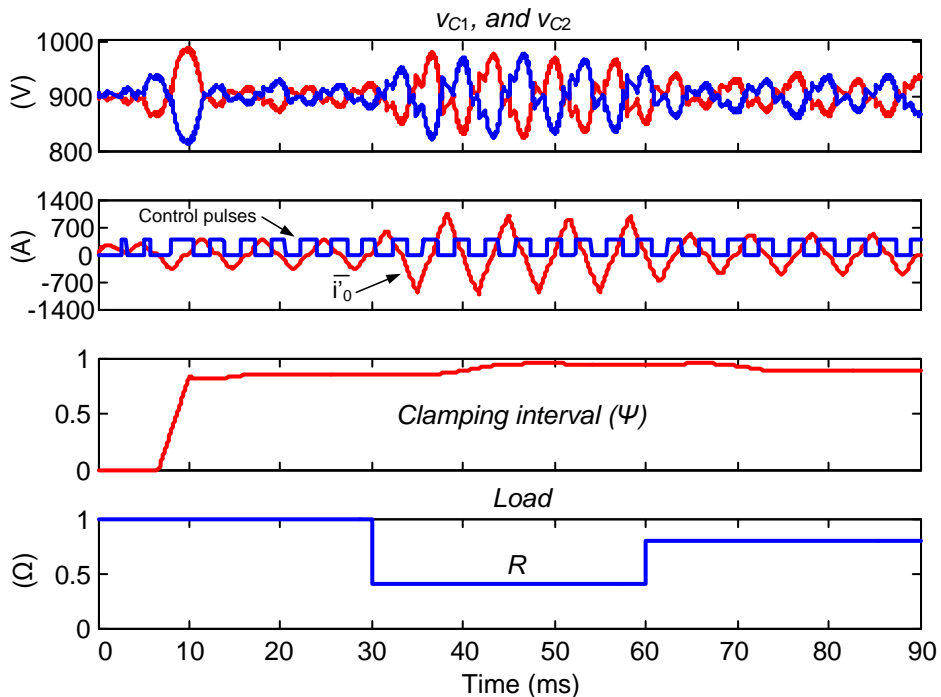
Fig.5.23. Tracking method under different loads.

5.3. Control Loop for the NP Voltage Oscillation Amplitude

So far, the parameter *D* was given. In this section, the value of this parameter will be determined by a control loop. A drawback of the HPWM, which is common in many modulation strategies, is that the amplitude of the NP voltage oscillations depends on the operation point of the converter. The amplitude of these oscillations increases while operating with deep modulation indices and low power factors. The use of the proposed controller guarantees that a defined value for the maximum amplitude of the NP voltage oscillations is not exceeded. Hence, the power devices and the dc-link capacitors of the converter can be designed with consideration toward this maximum voltage specification.

Fig.5.24 shows the general structure of the system, which includes the control loop for the regulation and limitation of the amplitude of the NP voltage oscillations.

The block called Hybrid Modulation is responsible for the generation of the new modulation signals from the DSPWM, which are modified by a mixture parameter (*D*). The Oscillation Voltage Control block corresponds to the proposed controller. It is able to regulate the amplitude of the NP voltage oscillations when they tend to be larger than the predefined maximum limit.
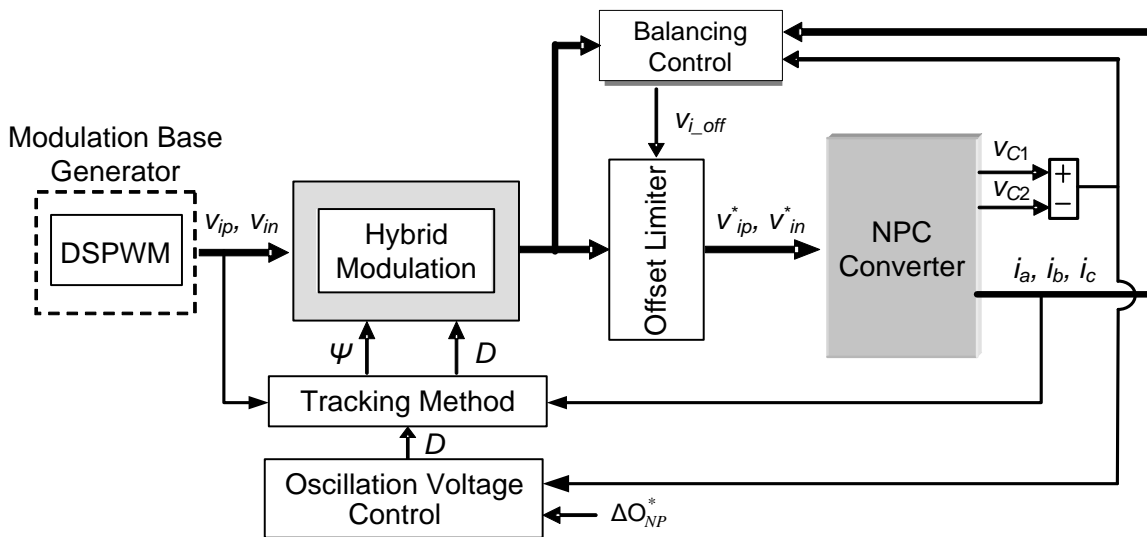
Fig.5.24. System Structure.

The Balancing Control block is the optimal compensator proposed in Chapter 4, Section 4.2, and provides a proper offset to help balance the voltage between the dc-

link capacitors. The block Modulation Base Generator, which generates DSPWM patterns, and the Offset Limiter are blocks already presented in Chapter 4.

The proposed strategy for limiting the maximum NP voltage oscillations is implemented in the Oscillation Voltage Control block. The inputs of this block are the maximum amplitude reference (ΔO_{NP}^*) and the difference of the capacitor voltages.

5.3.1. Amplitude Control Strategy of the Neutral-Point Voltage Oscillations

The proposed controller is used to modify the parameter D of the HPWM strategy online. Consequently, the HPWM becomes adaptive, and it can be adjusted for controlling the NP voltage amplitude.

Fig.5.25, shows the different blocks used in the proposed control strategy. Firstly, the value of the instantaneous oscillations around the NP is obtained, as follows:

$$\Delta O_{NP} = \frac{v_{C1} - v_{C2}}{2} \, . \tag{5.7}$$

This variable is filtered by a moving-average operator with a window width equal to the period of the triangular carriers (T_s):

$$\overline{\Delta O_{NP}} = \frac{1}{T_s} \int_{t-T_s}^{t} \Delta O_{NP}(\tau) d\tau \, . \tag{5.8}$$

Once $\overline{\Delta O_{NP}}$ is filtered, the amplitude of the NP voltage oscillations is continuously calculated every third of the output period ($T/3$), as follows:

$$\Delta O'_{NP} = \frac{\overline{\Delta O_{NP\max}} - \overline{\Delta O_{NP\min}}}{2} \, . \tag{5.9}$$

Finally, the error between this variable and the maximum amplitude reference is calculated as follows:

$$\varepsilon = \Delta O_{NP}^* - \Delta O'_{NP} \tag{5.10}$$

This error is provided to a particular PI-based controller. Fig.5.25 also shows a block which is called Protection Algorithm. It is activated when the oscillation tends to go beyond the defined limit specified by the dc bus. Then, the control parameter D must be zero in order to minimize the oscillations and to keep this under their

security limit. This is basically achieved by resetting the integrator of the controller. The PI regulator will be activated in the next oscillation cycle unless the operating conditions change and the NP voltage amplitude becomes lower than the maximum limit.
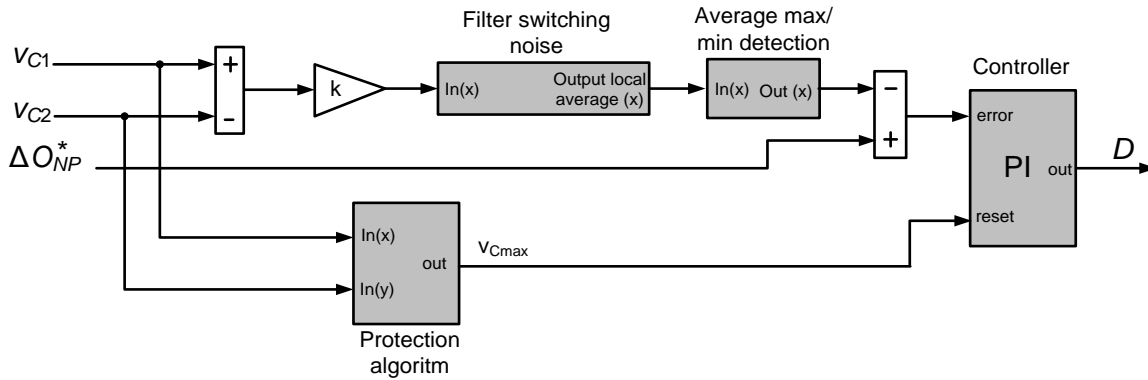
Fig.5.25. Control strategy.

The proposed control strategy has the property of minimizing the switching frequencies of the power devices. This is because the modulation waveforms are practically not modified. On the other hand, the dynamic of this controller is slower than that of other control strategies (Zaragoza et al. 2008). However, that produces more switching losses than the strategy proposed here.

5.3.2. Simulation Results

The structure shown in Fig.5.24 was implemented by Matlab-Simulink software. The values for the simulation examples are: V_{dc}=1,800 V and a resistive-inductive Wye-connected load with R=1 Ω and L=2 mH, respectively. The value for the dc-link capacitors is C= 2,200 µF and the frequency of the triangular carriers is f_s=5 kHz in all the simulations.

Fig.5.26 shows the voltage waveforms in the dc-link capacitors when operating with an output frequency (modulation frequency) f_m=50 Hz. It shows the control response for different amplitude references.

Fig.5.27 shows the converter operating under the same conditions but the load resistor value has been changed to R=0.5 Ω in order to produce NP voltage oscillations that would go beyond a specified limit. However, the limit of 960 V has

been imposed to protect the system. The results show that the control parameter *D* is clamped to zero when the capacitor voltage amplitudes tend to be higher than the specified limit. This drastic reduction in parameter *D* activates DSPWM; hence, the voltage amplitudes are immediately reduced.

Once the protection algorithm block has been activated, the voltage amplitudes of the oscillations go back again towards the maximum reference value.
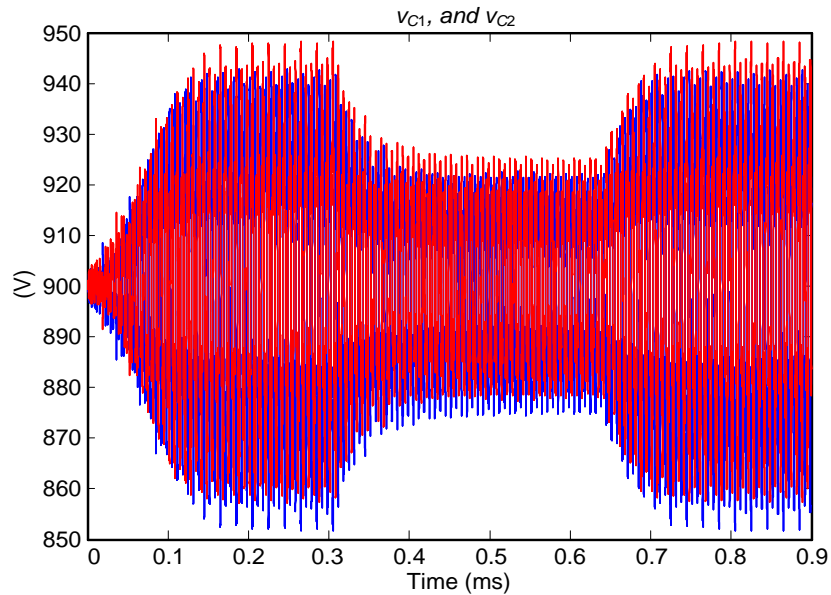
Fig.5.26. Simulation results for different NP voltage amplitude reference values.
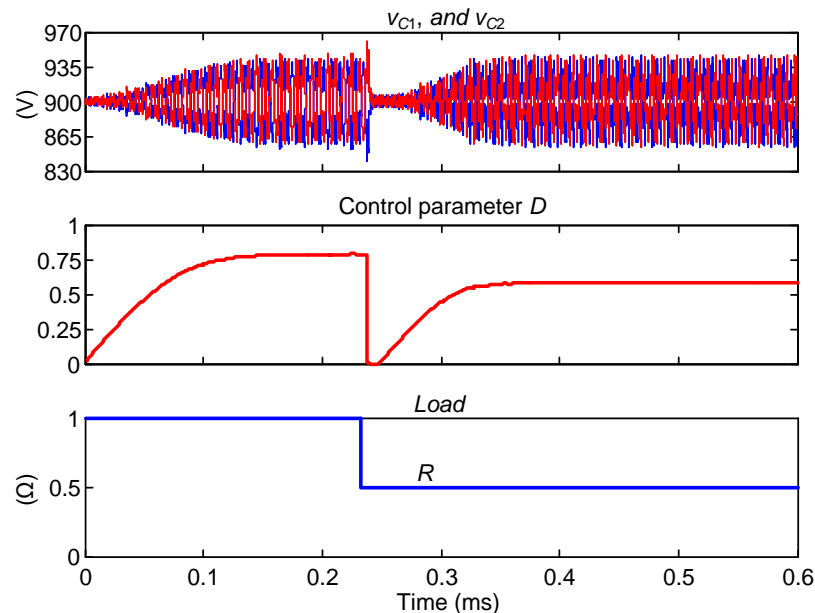
Fig.5.27. Protection algorithm verification.

5.4. Chapter Conclusions

The DSPWM strategy proposed in Chapter 4 can completely eliminate low-frequency oscillation in the NP voltage, but it produces high switching frequencies in power devices. On the other hand, the well known SPWM generates lower switching losses, but some low-frequency oscillations may appear in the NP voltage. Such oscillations can take significant amplitudes under some operating conditions. The proposed HPWM is a compromise solution between DSPWM and SPWM. It can be modified online by varying just one controlling parameter (D). Thus, for $D=0$ the technique becomes DSPWM, for $D=1$ it becomes SPWM, and for $0<D<1$ it is a combination of the two techniques (HPWM). However, it is very important to define the best intervals in which SPWM can be applied in order to achieve the maximum attenuation of the voltage oscillations.

In this chapter, a versatile means has been proposed for modifying the clamping intervals of the modulation signals (application of SPWM). A tracking strategy has also been presented for minimizing the amplitude of the voltage oscillation for a specific combination (D value). The results shown in this chapter demonstrate that the modified HPWM can achieve far better results than basic HPWM.

Furthermore, the amplitudes of the NP voltage oscillations can be regulated and limited by the control strategy proposed in this chapter. The control loop for the hybrid modulation is designed so that the maximum amplitude of the low-frequency NP voltage oscillations can be limited to a given value. Therefore, the maximum voltage is defined and limited to what the power devices of the converter and the dc-link capacitors can stand. This is a very important feature for the design of the converter. Furthermore, the switching frequency of the power devices is reduced and the quality of the output voltage spectra improved compared to DSPWM.

The use of HPWM has some interest for some practical applications. Regarding NP voltage oscillations, SPWM seems to be acceptable for operating under or close to unity power factors. However, if the converter has to operate at other power factors, either temporarily or continuously, the HPWM proposed in this paper is able to attenuate such NP voltage amplitudes significantly thanks to both the proper

selection of the parameter *D* and the determination of the optimal intervals in applying DSPWM and SPWM*.* Some practical examples in which the converter does not operate at unity power factor are motor drives, static compensators (STATCOM), wind turbine systems, etc. In those cases, HPWM leads to a significant reduction in the maximum voltages applied to the capacitors and the power devices, at the expense of a slight decrease in the efficiency of the converter. This represents a reduction in the values of the dc-link capacitors. Furthermore, HPWM can be used to regulate and limit the maximum NP voltage amplitudes to a defined value, which would help size the components and power devices of the converter.

In summary, the HPWM, when applied together with the tracking method and voltage oscillation amplitude control, is able to achieve a compromise between the amplitude of the NP voltage oscillations and the power losses of the converter.

5.5. Chapter References

Busquets-Monge S, Bordonau J, Boroyevich D, Somavilla S. 2004. The nearest three virtual space vector PWM - a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter. Power Electronics Letters, IEEE 2: 11-15.

Busquets-Monge S, Somavilla S, Bordonau J, Boroyevich D. 2007. Capacitor Voltage Balance for the Neutral-Point- Clamped Converter using the Virtual Space Vector Concept With Optimized Spectral Performance. Power Electronics, IEEE Transactions on 22: 1128-1135.

Busquets-Monge S, Ortega JD, Bordonau J, Beristain JA, Rocabert J. 2008. Closed-Loop Control of a Three-Phase Neutral-Point-Clamped Inverter Using an Optimized Virtual-Vector-Based Pulsewidth Modulation. Industrial Electronics, IEEE Transactions on 55: 2061-2071.

Celanovic N, Boroyevich D. 2000. A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. Power Electronics, IEEE Transactions on 15: 242-249.

—. 2001. A fast space-vector modulation algorithm for multilevel three-phase converters. Industry Applications, IEEE Transactions on 37: 637-641.

Pou J, Boroyevich D, Pindado R. 2005a. Effects of imbalances and nonlinear loads on the voltage balance of a neutral-point-clamped inverter. Power Electronics, IEEE Transactions on 20: 123-131.

Pou J, Pindado R, Boroyevich D, Rodriguez P. 2005b. Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter. Industrial Electronics, IEEE Transactions on 52: 1582-1588.

Pou J, Zaragoza J, Rodriguez P, Ceballos S, Sala VM, Burgos RP, Boroyevich D. 2007. Fast-Processing Modulation Strategy for the Neutral-Point-Clamped Converter With Total Elimination of Low-Frequency Voltage Oscillations in the Neutral Point. Industrial Electronics, IEEE Transactions on 54: 2288-2294.

Zaragoza J, Pou J, Ceballos S, Robles E, Jaen C, Corbalan M. 2009. Voltage-Balance Compensator for a Carrier-Based Modulation in the Neutral-Point-Clamped Converter. Industrial Electronics, IEEE Transactions on 56: 305-314.

Zaragoza J, Pou J, Arias A, Ceballos S, Robles E, Ibanez P, Gabiola I. 2008. Amplitude control of the neutral-point voltage oscillations in the three-level converter. Pages 2473-2477. Power Electronics Specialists Conference, 2008. PESC 2008. IEEE.

<div style="text-align: right">

**Chapter
6.**

</div>

Modeling and Control of a Grid-Connected NPC Converter

In general, two large-signal models of the converter can be obtained; a switched model and an averaged model. The switched model contains discrete variables that define the state of the switches of the converter. The model can be simplified by assuming ideal switches. This model is not described in this chapter but can be found in Appendix B; nevertheless, it has been used to generate simulation results (voltage and current waveforms, and for the calculation of THD values).

The second model (averaged model) is obtained directly from the switched model and it is implemented by using duty cycles instead of switching functions. This model is originally a large-signal model; however, if the system is nonlinear, the model is usually linearized around an operating point. Averaged models are continuous models since they do not contain switching functions but averaged variables. An averaged model is presented in this chapter and it is used to design the control loops.

This chapter also presents a grid–side control strategy based on Voltage Oriented Control (VOC). It makes use of a coordinate transformation in a synchronous rotating *dq* reference frame. This strategy shows high dynamic and static performance via internal current control loops that depend on the quality of the current control strategy (Kazmierkowski and Malesani 1998, Malinowski M Sc Mariusz 2001).

There are many control techniques that can be applied to multilevel converters (Espinoza et al. 2005, Pou J. et al. 2005). Some of them are based on state-space models of the converter, such as the linear-quadratic-regulator (LQR) presented in (Fukuda et al. 1999, Pou J. et al. 2005), which is based on d-q coordinates. Other controllers use standard PI regulators. One of the main drawbacks of using linear controllers is that their parameters are usually adjusted for a specific operating point, and taking into account the nonlinear behavior of the system, the results are not optimal for other operating conditions. The controller proposed in this work is based on PI regulators; where a zero-pole cancelation strategy for tuning the parameters of the PI is used. However, taking into account that the system is nonlinear, a fuzzy supervisor is proposed which takes care of adjusting the PI parameters during transitory processes. The main objective is to improve the response of the system under load changes. Furthermore, simulation and experimental results show better behavior of the system when the fuzzy supervisor is applied in order to adjust the PI parameters of the controller.

6.1. Model of a Grid-Connected Multilevel Converter

6.1.1. Large-Signal Model of the System

Fig.6.1 shows the diagram of the multilevel system to be modeled. Conventional signs of voltages and currents are also indicated. Note that, in this chapter, the dc-link voltage is not provided by a dc source, but it is a variable to be regulated. Therefore, it is represented in lowercase (v_{dc}) because it is time dependent.
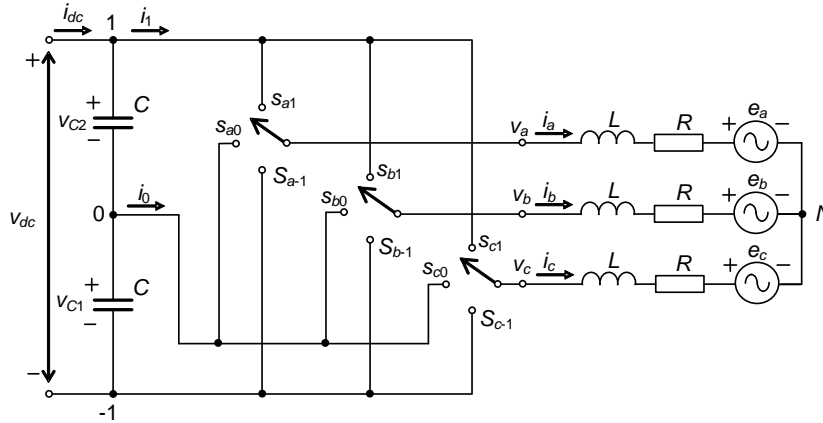
Fig.6.1. Grid-connected NPC converter.

The output voltages in Fig.6.1, which refer to the middle dc-link potential ("0"), can be expressed as:

$$L\frac{di_a}{dt} = v_{a0} - Ri_a - e_a - v_{N0},$$

$$L\frac{di_b}{dt} = v_{b0} - Ri_b - e_b - v_{N0}, \quad and \qquad (6.1)$$

$$L\frac{di_c}{dt} = v_{c0} - Ri_c - e_c - v_{N0}.$$

If the Park transformation is applied to (6.1), the following equations are obtained:

$$\frac{di_d}{dt} = \frac{1}{L}v_d - \frac{R}{L}i_d + \omega\,i_q - \frac{1}{L}e_d,$$

$$\frac{di_q}{dt} = \frac{1}{L}v_q - \frac{R}{L}i_q - \omega\,i_d - \frac{1}{L}e_q, \quad and \qquad (6.2)$$

$$\frac{di_o}{dt} = \frac{1}{L}v_o - \frac{R}{L}i_o - \frac{1}{L}e_o - \frac{\sqrt{3}}{L}v_{N0},$$

where ω is the angular frequency of the grid. Considering a balanced system, the zero-sequence current is $i_o = \dfrac{i_a + i_b + i_c}{\sqrt{3}} = 0$; hence, the last equation in (6.1) can be neglected.

In (6.2), the variables have been translated into *d-q* coordinates, and they should be understood as averaged variables. The *d-q* rotating axes can be synchronized to make the *q* component of the voltage grid zero ($e_q = 0$); the other component is $e_d = E_{RMS}$, which is the value of the line-to-line RMS voltage. Therefore the ac side of the system can be expressed as:

$$\frac{di_d}{dt} = \frac{1}{L} v_d - \frac{R}{L} i_d + \omega\, i_q - \frac{1}{L} E_{RMS}, \quad and$$
$$\frac{di_q}{dt} = \frac{1}{L} v_q - \frac{R}{L} i_q - \omega\, i_d. \tag{6.3}$$

The behavior of the dc-link voltage can be modeled by:

$$\frac{dv_{C2}}{dt} = \frac{i_{dc} - i_1}{C}, \quad and$$
$$\frac{dv_{C1}}{dt} = \frac{i_{dc} - i_1 - i_0}{C}. \tag{6.4}$$

In order to avoid switching functions, the equation of the dc side (6.4) can be related to the ac side (6.3) by the power-balance relationship. Taking into account that the *d-q* transformation is power conservative:

$$p_{ac} = v_a\, i_a + v_b\, i_b + v_c\, i_c = v_d\, i_d + v_q\, i_q, \tag{6.5}$$

and assuming efficiency of 100%, the instantaneous power at the dc side is:

$$p_{dc} = \left(v_{C1} + v_{C2}\right) i_1 + v_{C1}\, i_0. \tag{6.6}$$

Making both power values equal, current i_1 is:

$$i_1 = \frac{v_d\, i_d + v_q\, i_q - v_{C1}\, i_0}{v_{C1} + v_{C2}}, \tag{6.7}$$

and substituting this current into (6.4):

$$\frac{dv_{C2}}{dt} = \frac{i_{dc}}{C} - \frac{v_d\ i_d + v_q\ i_q - v_{C1}\ i_0}{C(v_{C1} + v_{C2})}\ and$$

$$\frac{dv_{C1}}{dt} = \frac{i_{dc}}{C} - \frac{v_d\ i_d + v_q\ i_q + v_{C2}\ i_0}{C(v_{C1} + v_{C2})}. \tag{6.8}$$

The large-signal model of the system is defined by (6.3) and (6.8).

Since the modulation algorithm will balance the NP voltage, the control stage must only regulate the total dc-link voltage and the ac currents. Therefore, the model can be simplified by assuming balanced voltage in the capacitors ($v_{C1}=v_{C2}=v_{dc}/2$). Summing term by term in (6.8):

$$\frac{dv_{dc}}{dt} = 2\frac{i_{dc}}{C} - 2\frac{v_d\ i_d + v_q\ i_q}{Cv_{dc}}. \tag{6.9}$$

6.1.2. Averaged-Signal Model of the System

The equations of the large-signal model, (6.3) and (6.8), describe the behavior of the converter. However, the variables will contain switching frequency ripple. In order to eliminate such ripple, averaged variables are assumed, according to the local averaging operator:

$$\overline{x}_{(t)} = \frac{1}{T_s} \int_{t-T_s}^{t} x_{(\tau)}\ d\tau. \tag{6.10}$$

As a result of applying this linear operator to the model of the system, all components of the variables related to switching frequency disappear. The variables of the model are assumed henceforth to be averaged variables. Equation (6.9) becomes:

$$\frac{d\overline{v_{dc}}}{dt} \approx 2\frac{\overline{i_{dc}}}{C} - 2\frac{\overline{v_d i_d} + \overline{v_q i_q}}{C\overline{v_{dc}}}. \tag{6.11}$$

Note that (6.11) is nonlinear; therefore, it should be linearized to obtain a useful model for the control.

The variables assumed to be controlled are the reactive current component and the dc-link voltage:

$$\overline{i_q} = i_q^* \quad \text{and} \quad \overline{v_{dc}} = v_{dc}^*, \tag{6.12}$$

where i_q^* and v_{dc}^* denote the reference values.

The transformed ac voltages of the converter (v_d, v_q) are the control variables. Thus, the system is simplified into a two-input-two-output three-order system.

In steady-state conditions, the subscript "*op*" is added to the variables to identify the operating point:

$$\overline{i_{q\_op}} = i_q^* \quad \text{and} \quad \overline{v_{dc\_op}} = v_{dc}^* \tag{6.13}$$

The remaining steady-state variables are found by imposing zero into the dynamic of the system; in other words, they are obtained by making the derivatives of the variables equal zero, as follows:

$$\frac{d\overline{i_{d\_op}}}{dt} = -\frac{R}{L}\overline{i_{d\_op}} + \frac{1}{L}\overline{v_{d\_op}} + \omega\, i_q^* - \frac{1}{L}E_{RMS} = 0 \quad and$$

$$\frac{d\overline{i_{q\_op}}}{dt} = -\frac{R}{L}i_q^* + \frac{1}{L}\overline{v_{q\_op}} - \omega\,\overline{i_{d\_op}} = 0 \tag{6.14a}$$

$$\frac{d\overline{v_{dc\_op}}}{dt} = 2\frac{\overline{i_{dc\_op}}}{C} - 2\frac{\overline{v_{d\_op}}\,\overline{i_{d\_op}} + \overline{v_{q\_op}}\,i_q^*}{Cv_{dc}^*} = 0. \tag{6.14b}$$

The solution for the steady-state values:

$$\overline{i_{d\_op}} = \sqrt{\left(\frac{E_{RMS}}{2R}\right)^2 + \frac{V_{dc}^*}{R}i_{dc\_op} - i_q^{*2}} - \frac{E_{RMS}}{2R}, \tag{6.15a}$$

$$\overline{v_{d\_op}} = E_{RMS} + R\,\overline{i_{d\_op}} - \omega L i_q^* \quad \text{and} \tag{6.15b}$$

$$\overline{v_{q\_op}} = Ri_q^* + \omega L\,\overline{i_{d\_op}}. \tag{6.15c}$$

The model is linearized by applying Taylor's Series around the operating point and by disregarding high-order terms. This is acceptable if variations around the operating point are assumed to be small; therefore, the equations of the small-signal model can be given as (Ceballos Salvador 2008, Pou Josep 2002):

$$\frac{d\tilde{i}_d}{dt} = -\frac{R}{L}\tilde{i}_d + \frac{1}{L}\tilde{v}_d + \omega\tilde{i}_q - \frac{1}{L}\tilde{E}_{RMS},$$ (6.16a)

$$\frac{d\tilde{i}_q}{dt} = -\frac{R}{L}\tilde{i}_q + \frac{1}{L}\tilde{v}_q - \omega\tilde{i}_d \quad \text{and}$$ (6.16b)

$$\frac{d\tilde{v}_{dc}}{dt} = -\frac{2\overline{v_{d\_op}}}{Cv_{dc}^*}\tilde{i}_d - \frac{2\overline{v_{q\_op}}}{Cv_{dc}^*}\tilde{i}_q + \frac{2(\overline{v_{d\_op}i_{d\_op}} + \overline{v_{q\_op}i_q^*})}{C(v_{dc}^*)^2}\tilde{v}_{dc} - \frac{2\overline{i_{d\_op}}}{Cv_{dc}^*}\tilde{v}_d$$

$$-\frac{2i_q^*}{Cv_{dc}^*}\tilde{v}_q + \frac{2}{C}\tilde{i}_{dc}.$$ (6.16c)

6.2. Control of the Grid-Connected Converter Working as a Rectifier

6.2.1. Control of the Multilevel Converter Using Standard PI's

The objective of this section is to describe a process for tuning the parameters of standard PI's in order to control the total dc-link voltage and the ac currents (i_d and i_q). This tuning technique is called zero-pole cancelation (Ceballos S. et al. 2006.).

In this study, a resistor is connected to the dc bus and no additional current is injected into the dc link (Fig.6.2). Therefore, the converter will operate as a rectifier, transferring energy from the ac side to the dc side. In this case, the dc current is:

$$i_{dc} = -\frac{v_{dc}}{R_{load}}.$$ (6.17)
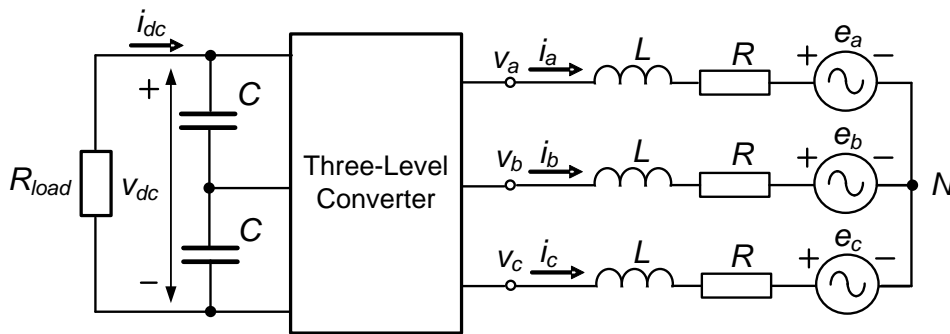
Fig.6.2. Grid-connected converter operating as a rectifier.

A control diagram for the three-level-based system can be obtained from (6.3). This equation can also be expressed as follows:

$$v_d = \Delta v_d - \omega L i_q + E_{RMS} \quad \text{and} \quad v_q = \Delta v_q + \omega L i_d, \tag{6.18}$$

in which $\Delta v_d = L\dfrac{di_d}{dt} + R i_d$ and $\Delta v_q = L\dfrac{di_q}{dt} + R i_q$.

The VOC diagram is pictured in Fig.6.3, in which the blocks that contain ωL have the objective of decoupling influences between both current control loops (Bong-Hwan et al. 1999). Nevertheless, due to sensing errors and filtering delays, some practical influences between the loops still remain after decoupling the channels.

The control structure in Fig.6.3 has two loops:

1. An external voltage loop, which is responsible for the dc-link voltage regulation.

2. An internal current loop, which adjusts the values of the ac currents (i_d and i_q). This current loop has a relatively faster dynamic than the voltage loop.

The external loop generates the current references from the dc-link voltage error ($v_{dc}^* - v_{dc}$). The inner loop provides the components of the reference vector (v_d and v_q) to the modulator.
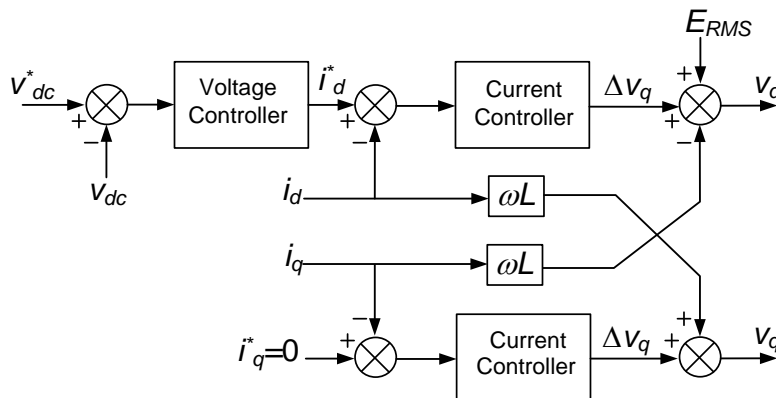
Fig.6.3. Decoupled PI controller.

The small-signal model of the converter (6.16) can be used for the design of the voltage and current controllers, which are based on proportional and integral (PI)

actuations. The parameters of the controllers can be calculated by classical design methods.

6.2.1.1 Tuning of the PI Controllers

The design process of the controller is based on the zero-pole cancellation methodology (Ceballos S. et al. 2006., Malinowski M. and Steffen 2004, Malinowski M. et al. 2009). This strategy allows easy calculation of the PI parameters.

Fig.6.4 shows the model and the VOC of the grid-connected converter. In this representation, the modulator and the converter are assumed to perform very fast so that the control variables (v_d and v_q) provided by the control stage are directly applied to the ac side of the system.

Observe that the coupled terms *($\omega L i_d$* and *$\omega L i_q$)* and the grid voltage (E_{RMS}) that appear in the system model in Fig.6.4 are compensated in the control stage as feedforward terms. Consequently, the voltages provided by the current PI regulators (Δv_d and Δv_q) are the only variables that are eventually applied to the transfer functions of the system ($1/(Ls+R)$ being s the laplace variable).

Firstly, the controllers of the current loop are adjusted using (6.19). From that equation, the diagram in Fig.6.5 is obtained. Equation (6.19) describes the PI function for both the current and voltage control loop:

$$G_C(s) = k_p + \frac{k_i}{s} = \frac{1 + \dfrac{k_p}{k_i} s}{\dfrac{1}{k_i} s} \ . \tag{6.19}$$

The applied control strategy is based on canceling the pole of the system by the zero of the controller. The following equation shows the open loop of the current loop.

$$G_{OL}(s) = \frac{k_i}{R} \frac{1 + \dfrac{k_p}{k_i} s}{s} \cdot \frac{1}{\dfrac{L}{R} s + 1} \ . \tag{6.20}$$

To achieve such zero-pole cancellation, the following condition has to be fulfilled:

$$\frac{k_p}{k_i} = \frac{L}{R} \ . \tag{6.21}$$
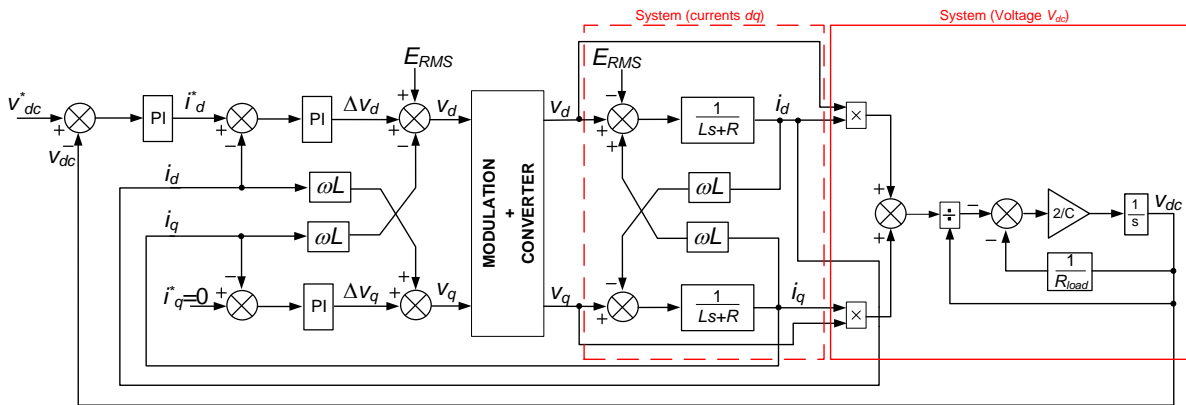
Fig.6.4. Model and control of the grid-connected converter.
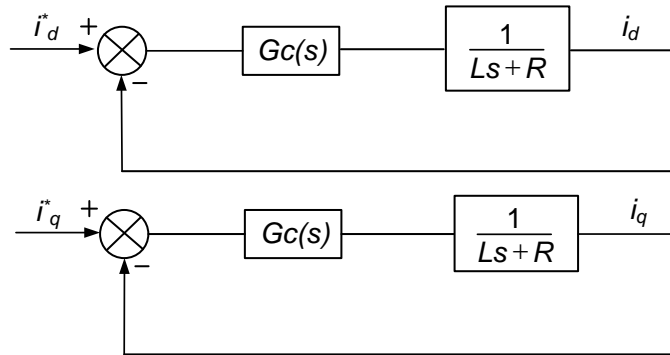
Fig.6.5. Current control loop.

Hence, the control loops in Fig.6.5 become as shown in Fig.6.6.
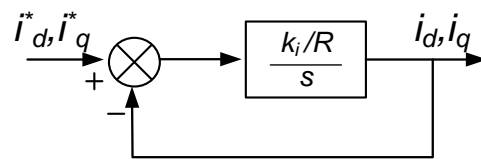
Fig.6.6. Current control loop with zero-pole cancelation.

Therefore, the following closed-loop transfer function becomes a first order system:

$$G_{CL}(s) = \frac{i_d(s)}{i_d^*(s)} = \frac{i_q(s)}{i_q^*(s)} = \frac{1}{\dfrac{R}{k_i}s + 1} \ . \tag{6.22}$$

Equation (6.21) is used to calculate the parameters of the controller. Another equation is needed to solve both k_p and k_i. The time constant of the closed-loop

transfer function (6.22) is $\tau = R/k_i$. The response time is defined at 2% of its final value when a step input is applied. This corresponds to 4τ in a first order system:

$$T_r = 4\tau = \frac{4R}{k_i} \Rightarrow k_i = \frac{4R}{T_r}. \tag{6.23}$$

The values of the constants k_p and k_i can be found once the response time T_r is defined. This time value should be high enough to provide a fast dynamic to the system, but not so high that it causes overmodulation in the converter.

The PI parameters of the current controllers can be calculated using (6.21) and (6.23). For this, it is necessary to know the values of both the inductors (L) that connect the converter to the network, and the resistors (R) associated with losses.

On the other hand, the performance of the dc voltage loop is nonlinear. Therefore, the linearized equation on the dc side (2.16c) has to be used. This equation is transformed into a Lapace representation, as follows.

$$\tilde{v}_{dc}(s) = \left[\frac{\dfrac{2R_{load}\overline{v_{d\_op}}}{V_{dc}^*}}{2aR_{load} - 2 - R_{load}Cs} \right] \left[\tilde{i}_d(s) + \frac{\overline{i_{d\_op}}}{v_{d\_op}}\tilde{v}_d(s) + \frac{\overline{v_{q\_op}}}{v_{d\_op}}\tilde{i}_q(s) - \frac{Cv_{dc}^*}{2v_{d\_op}}\tilde{v}_{dc}(0) \right], \tag{6.24}$$

in which $a = \dfrac{\overline{v_{d\_op}}\,\overline{i_{d\_op}}}{v_{dc}^{*\,2}}$

The diagram representing the linearized voltage control loop is shown in Fig.6.7. The terms denoted in Fig.6.7 by the superscript [1] are considered disturbances. The controller can eliminate their effect on the dc link voltage in the steady state due to the integral actuation; therefore, they are not considered.

The transfer function $G_2(s)$ is represented as follows:

$$G_2(s) = \frac{\dfrac{R_{load}\overline{v_{d\_op}}}{v_{dc}^*(aR_{load} - 1)}}{1 - \dfrac{R_{load}Cs}{2(aR_{load} - 1)}}, \tag{6.25}$$
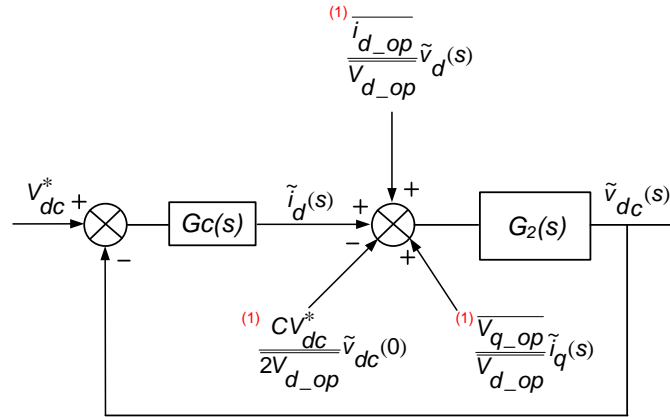
Fig.6.7. Voltage control loop.

The relationship for obtaining a zero-pole cancelation is:

$$\frac{k_p}{k_i} = -\frac{R_{load}C}{2(aR_{load}-1)}. \tag{6.26}$$

Therefore, the following closed-loop transfer function becomes a first order system:

$$G_{CL}(s) = \frac{v_{dc}^*(s)}{\tilde{v}_{dc}(s)} = \frac{1}{\frac{1}{k_i\,cte}s+1}, \tag{6.27}$$

where $cte = \dfrac{R_{load}\overline{V_{d\_op}}}{v_{dc}^*(aR_{load}-1)}$.

To calculate the parameters k_i and k_p a second equation is needed. It is obtained by imposing a response time (T_r) in a way similar to that done in the current loops.

$$T_r = 4\tau = \frac{4}{k_i\,cte} \Rightarrow k_i = \frac{4}{T_r\,cte}, and$$

$$k_p = -\frac{R_{load}C}{2(aR_{load}-1)}\frac{4}{cte\,T_r}. \tag{6.28}$$

All the variables of the voltage controller have to be known. As a design requirement, the current loop should be about ten times faster than the voltage loop so that the voltage and the current controllers can be tuned independently.

Some simulation and experimental results are presented in Section 6.3. As it will be observed, the dynamic of the VOC may be too slow for some transitory processes.

Although, it could be improved by imposing smaller time constants in the design, this will deteriorate the steady-state performance of the system. This is due to the fact that imposing smaller time constants means having high bandwidth control loops, which makes the system too sensitive to noise and ripple.

In order to improve the VOC response in transitory processes, the parameters of the controller can be changed only during the transitory processes and return back to the original values in the steady state. In this research, the tuning of the controllers during the transitory processes is made by a fuzzy supervisor, which is explained in the following section.

6.2.2. Control of the Multilevel Converter Using a Fuzzy Supervisor

A fuzzy-based strategy is proposed in this section. The VOC loops are the same; however, the parameters are changed on-line by the fuzzy supervisor. It measures the variables to be supervised and modifies the parameters of both control loops; the current and the voltage loops. This supervisor should improve the response of the system under loading changes. Fig.6.8 shows the control structure propose where the external loop generates the current references from the dc-link voltage error ($v_{dc}^* - v_{dc}$) and the inner loop provides the components of the reference vector (v_d^* and v_q^*) to the modulator. The PI controllers are tuned using the zero-pole cancelation strategy presented in the previous section. The fuzzy supervisor cancels both the zero and the pole and, thus, keeps the property.
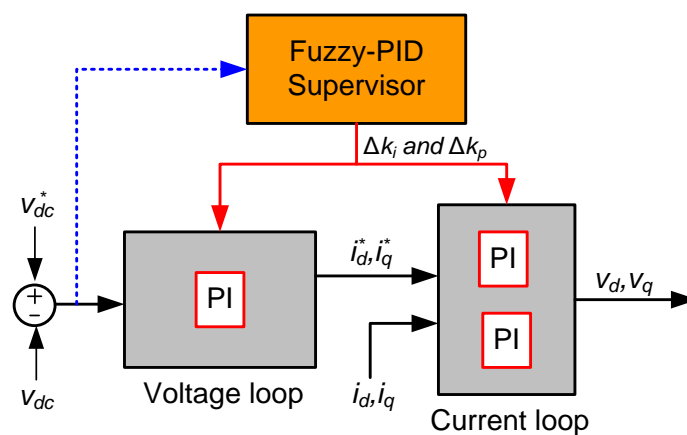
Fig.6.8. Control structure.

6.2.2.1 The fuzzy Supervisor Strategy

The PID-Fuzzy supervisor is based on (Wing-Chi et al. 1996). This structure uses two input variables and one output variable. The input variables are the proportional and derivative signals in a conventional PD controller. As the output signal goes through an integrator, the resulting characteristic is similar to a PID controller.

The PID-Fuzzy is suited to the zero order Takagi-Sugeno fuzzy architecture (Takagi and M. 1985), which is biunivocally described by a set of IF-THEN rules such as:

$$\text{IF} \quad x_1 \text{ is } \tilde{x}_{1i} \quad \text{AND ... AND } x_n \text{ is } \tilde{x}_{ni} \quad \text{THEN } u_i = C_i, \tag{6.29}$$

where $x_1, \ldots x_n$ are the physical inputs to the fuzzy supervisor. The rule antecedents (part IF of the rule) $\tilde{x}_{1i}, \ldots \tilde{x}_{ni}$ are variables described by means of membership functions, which are in charge of locally and gradually mapping the corresponding physical variables into the [0 1] interval. The rule consequents (part THEN of the rule) are defined as singletons (i.e $u_i = C_i$, where C_i is the degree of change of the PI parameters). The inference result of each rule consists of the logic-product of factor ω_i and C_i. The factor ω_i is obtained by applying the *min* operation to the $\mu_e(e_o)$ and $\mu_{ce}(ce_o)$, as follows:

$$\omega_i = \min\{\mu_e(e_o), \mu_{ce}(ce)\}, \tag{6.30}$$

in which the variables e_o and ce_o are the singleton inputs, e being the *dc* voltage error (noted as $e = v_{dc}^* - v_{dc}$) and *ce* its derivative.

Finally, the crisp output of the TSK supervisor *u* is given by the method of center of gravity which can be found as:

$$u = \sum_{i=1}^{N} \omega_i C_i \bigg/ \sum_{i=1}^{N} \omega_i . \tag{6.31}$$

where *N* is the maximum number of effective rule. In this case, *N*=4.

This kind of rules will be used to adapt the coefficients of all the PI controllers. It can be noted in Fig.6.9 that the integral action will restore the value of the PI coefficient u_i, in accordance with:

$$u_i = k(n) = k(n-1) + \Delta k(n).$$ (6.32)

On the other hand, the fuzzy computation is carried out in a normalized domain as shown in Fig.6.9 where $\beta_e^{-1}, \beta_{ce}^{-1}$ and $\eta_1,...,\eta_4$ stand for the input and output normalization coefficients, respectively.
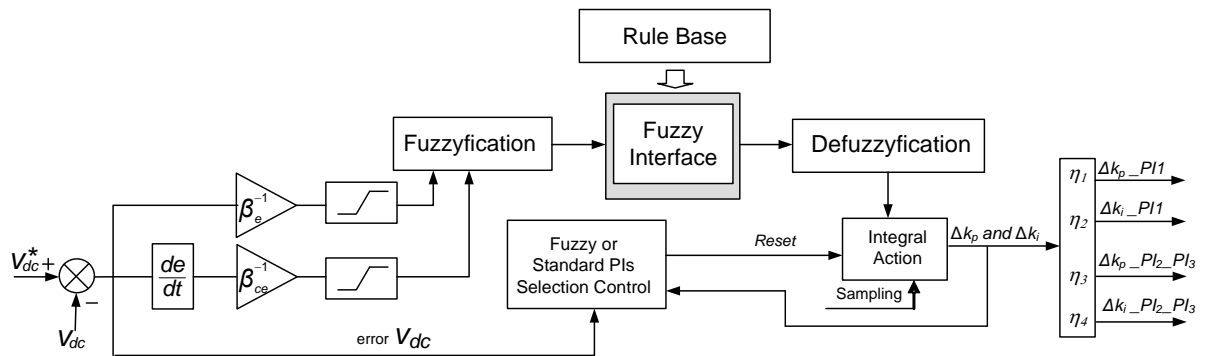
Fig.6.9. Control Structure based with Fuzzy-PID.

The membership functions, the rule base, as well as the normalization coefficients are deduced on a trial and error basis, the control policy being to keep the closed-loop poles of the system on the left-hand-side of the real axis, as shown in the example in Fig.6.10.

As a result, the adjustment of each PI coefficient is carried out by a Fuzzy supervisor of 25 rules, where antecedents are labeled as NB, NS, Z, PS, PB, where P means "Positive", N "Negative", Z "Zero", S "small" and B "Big". The rule base is summarized in Table 6.1, whereas the membership functions corresponding to the labels NB, NS, Z, PS, PB are depicted in Fig.6.11

The parameters of the PI controllers, k_p and k_i, are incremented proportionally. As a result, the pole-zero cancellation and the time constant ratios of the voltage and current loops are preserved. Therefore, the performance of the system is like a first-order system for the whole operating range of the fuzzy supervisor (Fig.6.10). The increments of the values k_p and k_i are limited by the fuzzy supervisor to a maximum which, at the operating point, is five times the values for both the current and voltage

loops. Since these parameters are limited, stability of the system is guaranteed for the particular values that have been selected in the Simulation Section. Fig.6.12 shows the resulting input-output surface.
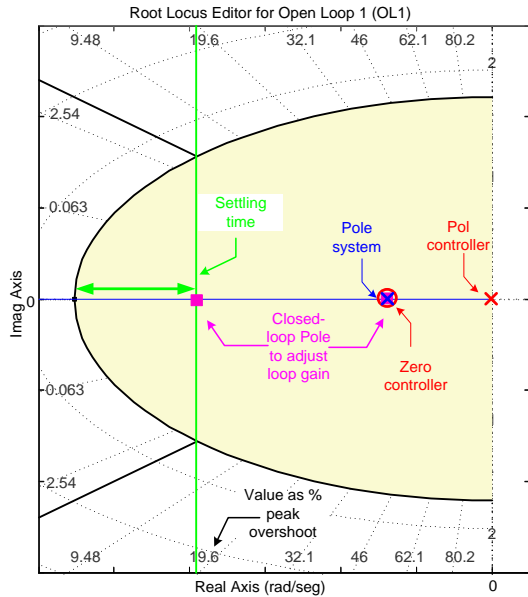
Fig.6.10. Example of the zero-pole cancelation strategy.
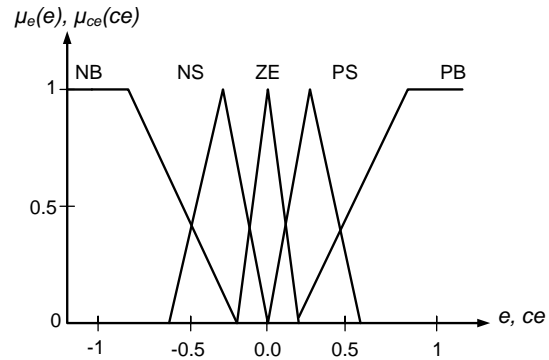
Fig.6.11. Membership functions for *e* and *ce*.

Table 6.1. Rule table of the fuzzy supervisor.

e_o\ ce_o	NB	NS	Z	PS	PB
PB	1	0.65	-0.2	-0.65	-1
PS	0.45	0.3	-0.1	-0.3	-0.45
Z	0.2	0.2	0	-0.1	-0.2
NS	-0.45	-0.3	0.1	0.3	0.45
NB	-1	-0.65	0.2	0.65	1
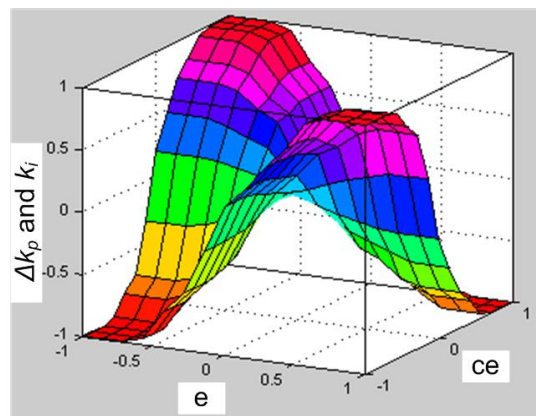
Fig.6.12. Resulting input-output supervisor surface.

6.3. Simulation and Experimental Results

The control algorithm operates with the standard PIs structure and NTV modulation, which are programmed and tested by Matlab-Simulink. Furthermore, some experimental results are obtained using the 20-kVA prototype presented in Section 2.4. The values used for the simulations and experiments were: line-to-neutral grid voltage 230 V, coupling inductors L=6 mH, R=0.1 Ω, sampling frequency f_s=5 kHz. The system operates at v_{dc}^* =750 V and output resistor R_{load}=35 Ω.

Table 6.2 shows the values selected for the input and output variables of the fuzzy controller, and Table 6.3 indicates the initial values of the constants k_p and k_i.

Table 6.2. Parameters of the Fuzzy Controller.

β_e^{-1}	β_{ce}^{-1}	η_1	η_2	η_3	η_4
10	7	0.033	1.739	0.6	10

Table 6.3. Parameters of the PI's Controller.

	PI_1	PI_2	PI_3
k_p	0.0837	1.5	1.5
k_i	4.3477	25	25

Fig.6.13 and Fig.6.14 show the transitory process of connecting the resistor to the dc output (the dc-link voltage and two output currents). The results show both standard PI and Fuzzy control strategy behavior. Notice that the simulation results match the experimental ones.

(a)   (b)
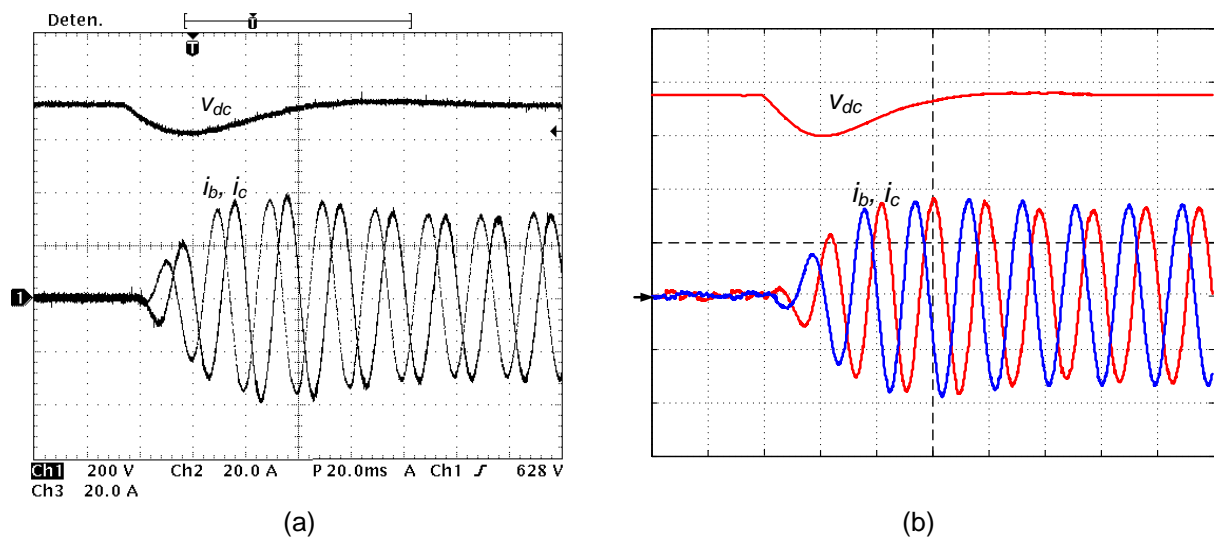
Fig.6.13. Dynamics of the dc voltage and two currents using VOC: (a) experimental results, and (b) simulation results.

(a)   (b)
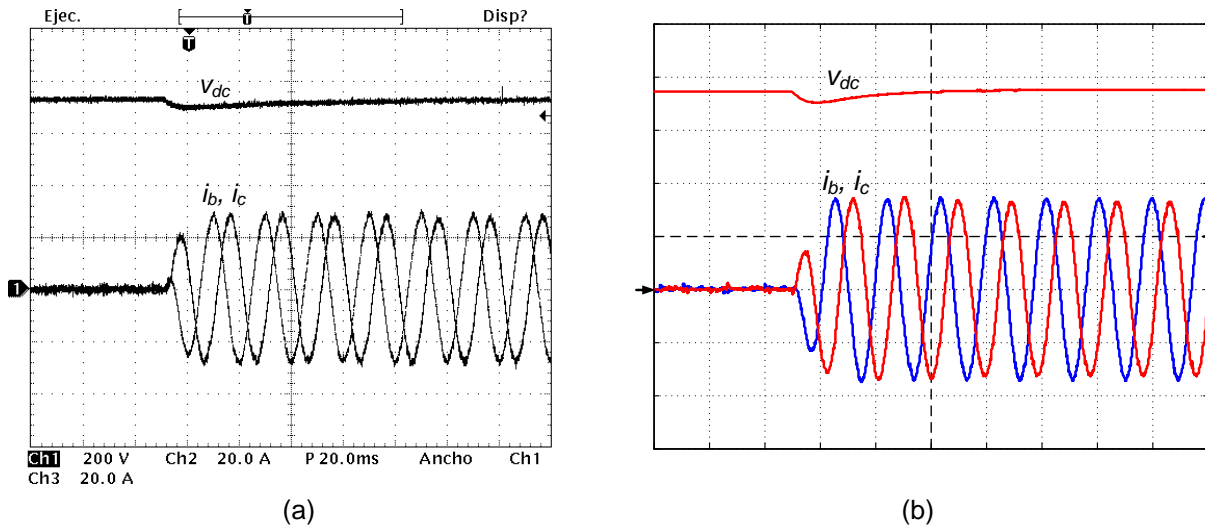
Fig.6.14. Dynamics of the dc voltage and two currents using VOC with a Fuzzy supervisor: (a) experimental results, and (b) simulation results.

Fig.6.15 shows a line-to-line output voltage, the total dc-link voltage, and two output currents in the steady-state condition. The converter operates with practically a unity-power factor.

(a)   (b)
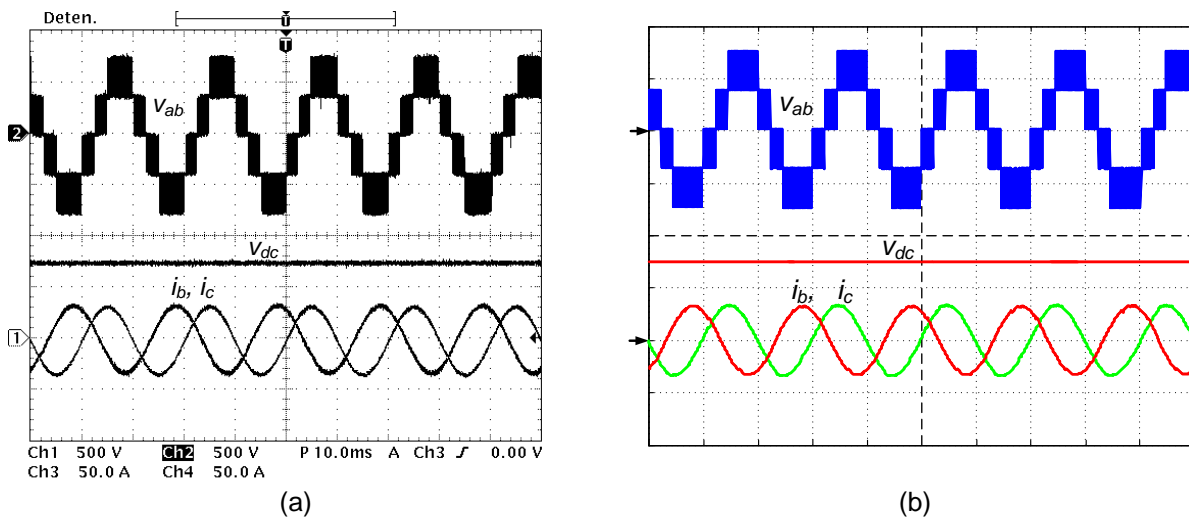
Fig.6.15. Results under steady-state conditions: (a) experimental results, and (b) simulation results.

6.4. Chapter Conclusions

In this work, a VOC scheme has been studied. It is based on three PI control loops, one for the regulation of the total dc-link voltage, and the other two for the *d* and *q* components of the ac currents. The PIs have been tuned using the pole-zero

cancellation method. In order to speed up the response of the system, a fuzzy supervisor is included. This supervisor changes the PI parameters when the loading conditions of the system change. The parameters k_p and k_i are modified proportionally in order to guaranty stability of the system.

The standard PI control structure is tested by simulation and experiment. The results show significant improvement when the controller includes the fuzzy supervisor under steep loading changes.

This control technique can be applied to other systems to improve dynamic response with guaranteed stability.

6.5. Chapter References

Bong-Hwan K, Jang-Hyoun Y, Jee-Woo L. 1999. A line-voltage-sensorless synchronous rectifier. Power Electronics, IEEE Transactions on 14: 966-972.

Ceballos S. 2008. Mejora en la Fiabilidad y en el Control de Tensión del Punto Neutro en Convertidores de Fijación por Diodos de Tres NivelesEscuela Técnica Superior de Ingniería de Bilbao, Bilbao.

Ceballos S, Gabiola I, Robles E, Zaragoza J, Martín JL. 2006. Development and Experimental analysis of a 20 kW 3-level converter. Paper presented at Proc. Conference for Power Electronics, Intelligent Motion and Power Quality PCIM'06.

Espinoza JE, Espinoza JR, Moran LA. 2005. A systematic controller-design approach for neutral-point-clamped three-level inverters. Industrial Electronics, IEEE Transactions on 52: 1589-1599.

Fukuda S, Matsumoto Y, Sagawa A. 1999. Optimal-regulator-based control of NPC boost rectifiers for unity power factor and reduced neutral-point-potential variations. Industrial Electronics, IEEE Transactions on 46: 527-534.

Kazmierkowski MP, Malesani L. 1998. Current control techniques for three-phase voltage-source PWM converters: a survey. Industrial Electronics, IEEE Transactions on 45: 691-703.

Malinowski M, Steffen S. 2004. Simple Control Scheme of Three-Level PWM Converter Connecting Wind Turbine with Grid. International Conference on Renewable Energy and Power Quality (ICREPQ'04).

Malinowski M, Stynski S, Kolomyjski W, Kazmierkowski MP. 2009. Control of Three-Level PWM Converter Applied to Variable-Speed-Type Turbines. Industrial Electronics, IEEE Transactions on 56: 69-77.

Malinowski MSM. 2001. Sensorless Control Strategies for hree - Phase PWM RectifiersWarsaw University of Technology, Warsaw, Poland.

Pou J. 2002. Modulation and Control of Three-Phase PWM Multilevel ConvertersUniversitat Politècnica de Catalunya, Terrassa.

Pou J, Rodriguez P, Pindado R, Boroyevich D, Candela I. 2005. Simplified linear-quadratic regulator applied to a three-level converter. Pages 10 pp.-P.10. Power Electronics and Applications, 2005 European Conference on.

Takagi T, M. S. 1985. Fuzzy Identification of systems and its applications to modelling and control. IEEE Trans. on Systems Man and Cybernetics 15: 116-132.

Wing-Chi S, Tse CK, Yim-Shu L. 1996. Development of a fuzzy logic controller for DC/DC converters: design, computer simulation, and experimental evaluation. Power Electronics, IEEE Transactions on 11: 24-32.

Chapter 7.

Wind-Turbine Control Application

Wind generation is an application field where multilevel converters are starting to be used nowadays and are expected to be further applied in the near future as the size of wind turbines grows. This chapter is focused on the control of a variable-speed wind energy conversion system (WECS) based on a permanent-magnet synchronous generator (PMSG). Different control tuning strategies for field oriented control (FOC) are studied and compared. The aerodynamics of the wind turbine (WT) and a PMSG have been modeled. The control strategy used in this research is composed of three regulators, which may be based on either linear or nonlinear controllers. In this analysis, proportional-integral (PI) linear controllers have been used. Two different tuning strategies are analyzed and compared. The main goal is to enhance the overall performance by achieving low sensitivity to disturbances and minimal overshoot under variable operating conditions. Finally, the results have been verified by an experimental WECS laboratory prototype.

7.1. Wind Generation

7.1.1 Wind Turbine Configurations

Wind is a natural energy resource that is starting to play an important role in electrical generation, a role that is expected to continue to grow in the near future. The use of the variable-speed WTs instead of their constant-speed counterparts is becoming more and more common for several reasons, including a more efficient collection of wind energy, the reduction of stress in the mechanical structure, and the reduction of acoustic noise due to blade movement. Fig.7.1 shows two of the main WT structures; the configuration in Fig.7.1(a) is based on a double-fed induction generator (DFIG), and the one in Fig.7.1(b) is based on a permanent-magnet synchronous generator (PMSG). These structures use two back-to-back connected power converters (Baroudi et al. 2007, Camblong et al. 2006a, Pena et al. 2001, Portillo et al. 2006, Rabelo and Hofmann 2001, Schiemenz and Stiebler 2001). In this configuration, one converter controls the WT speed, while the other takes care of shaping the currents injected into the electrical grid. Therefore, the active and reactive power can be controlled independently.

(a)

(b)
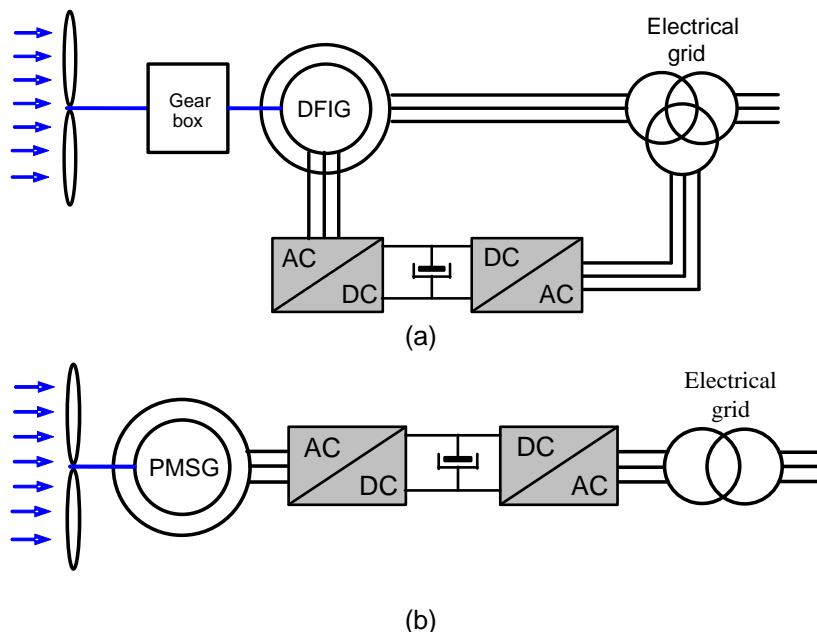
Fig.7.1. Variable-speed WT systems: (a) double-fed induction generator and (b) permanent-magnet synchronous generator.

The converters used in the DFIG have to process only about 30% of the total power generated. However, the converters in the PMSG are sized to process 100% of the generator rated power. Because of this, the PMSG configuration can achieve a harmonic current and reactive power control of higher VA ratings. This is an important advantage for fulfilling grid-connection regulations.

Another advantage of the multipolar PMSG configuration is that it may not require a gearbox. This implies both an increase in system efficiency as well as fewer maintenance requirements. Additionally, PMSG drives can achieve very high torque at low speeds, do not experience significant losses in the rotor, produce less noise, and do not require external excitation (Binder and Schneider 2005, Mohamed Y. A. R. I. 2007, Yang and Zhong 2007, Zhong et al. 1999). For all of these reasons, it is expected that the PMSG will be used extensively in the future. This chapter is devoted to studying PMSG control with the aim of improving its performance as a WECS.

7.1.2 Ac-dc-ac Power Electronic Topologies

The back-to-back-connected converters based on two-level configurations shown in Fig.7.2 are widely used in variable-speed WT systems. However, this type of converter has some limitations, such as:
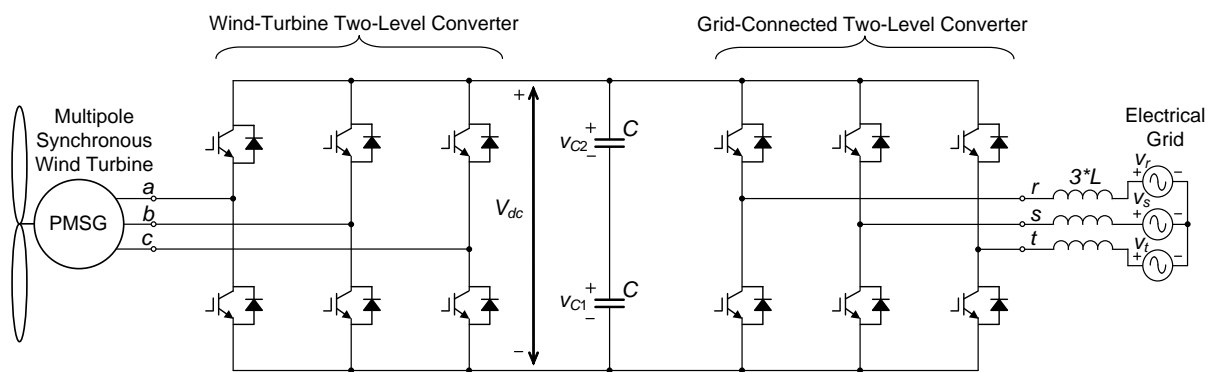
Fig.7.2. Back-to-back-connected conventional two-level converters.

-   The maximum voltage that the transistors have to withstand is the total dc-link voltage (V_{dc}). This leads to power limitations.

- Low quality output voltage spectra. This implies large values of the reactive components to filter the output currents (L or LCL filters) (Bueno 2005, Liserre et al. 2003). The switching frequencies could be pushed up, but it would increase switching losses.

For high power systems, such as the new generation of wind turbines (P>5 MW), the output currents can be increased by paralleling legs through inductors (Pou et al. 2009). However, another way to increase the output power is pushing the output voltages up by using multilevel converter topologies.

Since the rated power of wind generators is expected to grow further in the near future, multilevel converters are of special interest in this application. Among the various multilevel topologies, the most widely used nowadays is the three-level NPC converter. Fig.7.3 shows a back-to-back connection of two NPC converters.
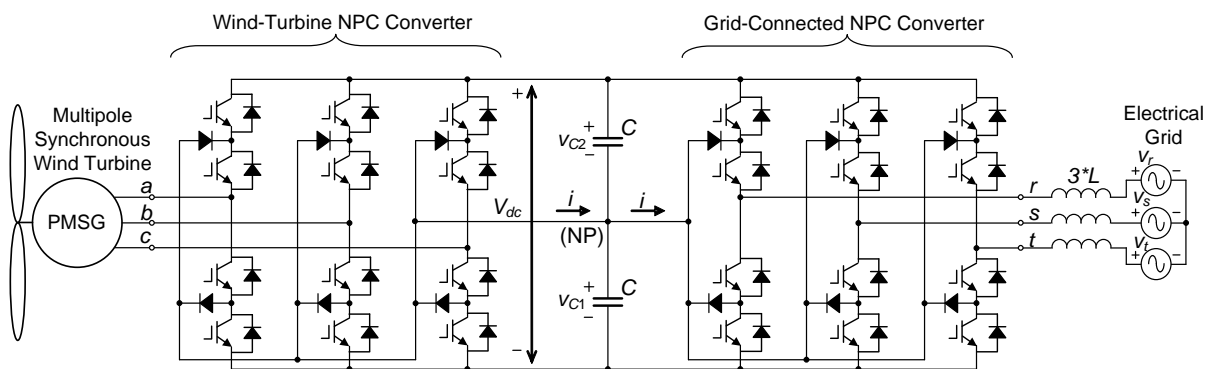
Fig.7.3. Back-to-back-connected NPC converters.

As was previously explained in Chapter 2, the NPC topology improves the main drawbacks of the two-level configuration, that is, the transistors have to withstand only half of the total dc-link voltage ($V_{dc}/2$) and the output voltage spectra have better quality (Zhe et al. 2009).

On the other hand, the main concern of the NPC converter is voltage-balance in the dc-link capacitors. However, in the back-to-back configuration both converters can contribute to the NP voltage balance (Pou et al. 2004). Under balanced grid voltages, the NP voltage balance is not a problem since both converters operate at nearly unity power factor.

A critical situation appears when there is a grid voltage sag. In such a case, according to the grid code regulations, the grid-connected converter has to provide reactive power to the grid and therefore it introduces NP currents which unbalance the NP voltage. If the converter connected to the generator cannot provide enough NP current for voltage-balance compensation (it will be dealing with low currents because low active power is transmitted), significant NP voltage oscillations will be produced.

The use of the hybrid modulation proposed in Chapter 5 can help to handle this situation. The hybrid modulation could be applied to the grid-connected converter while some of the modulations shown in Chapter 3 could be used in the converter connected to the wind generator.

Since the modulation strategy is responsible for controlling the NP voltage balance, the overall control of the system does not have to perform such a task. Therefore, regardless of dealing with two-level or multilevel converters, the control strategy can be the same. Because of this, and the fact that the experimental setup using three-level converters was not ready to perform some tests, the results of the control study performed in this chapter were obtained using two-level converters.

7.1.3 Control Strategies

Higher energy efficiency is obtained in WTs operated under configurations that allow rotor variable speed. For such purposes, different control strategies can be implemented, such as direct torque control (DTC) (Casadei et al. 2002, Zhong et al. 1999) and field-oriented control (FOC) (Casadei et al. 2002, Murray et al. 2008).

In this work, the FOC scheme using PI controllers is implemented to achieve variable speed in a WECS. The PI controller is a linear regulator that is easily tuned and usually provides good results. Consequently, this controller is widely used today in different industrial applications (Jul-Ki et al. 2006, Kristiansson and Lennartson 2006, Murray et al. 2008, Teodorescu and Blaabjerg 2004). PI controllers are normally adjusted for a specific operating point of the system under control. This fact provides satisfactory results if the system can be considered a linear system.

However, for nonlinear systems, the designed PI controllers may not be optimal for other operating conditions. For this reason, nonlinear controllers are used in some applications (Billy Muhando et al. 2007, Cadenas and Rivera 2009, Camblong et al. 2006b, López et al. 2008, Mohamed Amal Z. et al. 2001).

In a WT system, the electrical and mechanical parts are mostly linear. However, the aerodynamics of the blades are highly nonlinear; hence, the system behaves globally as a nonlinear system. Additionally, the WT is expected to operate under a wide range of wind speeds, which makes the control design more difficult. For all of these reasons, different strategies for tuning linear PI controllers have been studied in this chapter with the aim of minimizing the negative effects of the nonlinear parts of the WECS.

7.2. Wind Energy Conversion System Modeling

7.2.1 Wind Turbine Modeling

Wind energy is transformed both into mechanical energy through the WT blades and, ultimately, into electrical energy through the generator. The mechanical power (P_m), is given by the following equation:

$$P_m = \frac{1}{2}\rho A C_p(\lambda,\beta)v_{wind}^3 ,$$

(7.1)

where ρ is the air density (Kg/m^3), which normally takes values in the range [1.22,1.3], A is the area swept out by the turbine blades (m^2), and v_{wind} is the wind speed (m/s). The power coefficient (C_p) of a wind turbine is a measurement of how efficiently the WT converts the wind energy into mechanical energy. This coefficient depends on two parameters: β, which is the blade pitch angle and λ, which is called the tip speed ratio and is defined as follows:

$$\lambda = \frac{\Omega R_b}{v_{wind}} ,$$

(7.2)

where Ω is the angular shaft speed (rad/s) and R_b is the blade radius (m).

The power coefficient $C_p(\lambda,\beta)$ is nonlinear (Heier 1998, Monroy and Alvarez-Icaza 2006, Tafticht et al. 2006), and it depends on the blades' aerodynamic design and operating conditions. In (Heier 1998), the following relation is proposed to approximate the rotor power coefficient

$$C_p(\lambda,\beta) = c_1\left(\frac{c_2}{\lambda_i} - c_3\beta - c_4\right)e^{-\frac{c_5}{\lambda_i}} + c_6\lambda \ , \tag{7.3}$$

with $\dfrac{1}{\lambda_i} = \dfrac{1}{\lambda + 0.08\beta} - \dfrac{0.035}{\beta^3 + 1}.$

The coefficients c_1 through c_6 depend on the shape of the blade and its aerodynamic performance.

Equations (7.2) and (7.3) are used to implement the WT model, and the mechanical torque (T_m) is calculated as follows:

$$T_m = \frac{P_m}{\Omega} \ . \tag{7.4}$$

Fig.7.4 shows a three-dimensional representation of the power coefficient $C_p(\lambda,\beta)$. This surface was obtained using the following coefficient values: $c_1 = 0.5176$, $c_2 = 116$, $c_3 = 0.4$, $c_4 = 5$, $c_5 = 21$ and $c_6 = 0.0068$ (Heier 1998, Monroy and Alvarez-Icaza 2006, Tafticht et al. 2006).

Fig.7.5 shows C_p curves for constant values of β. Notice that the maximum power coefficient ($C_{pmax} = 0.48$) is achieved for $\beta = 0^o$ and $\lambda = 8.1$.
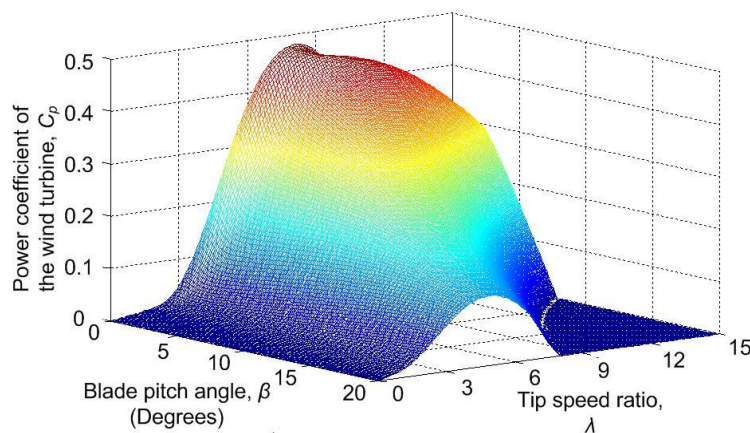
Fig.7.4. Representation of the power coefficient C_p.
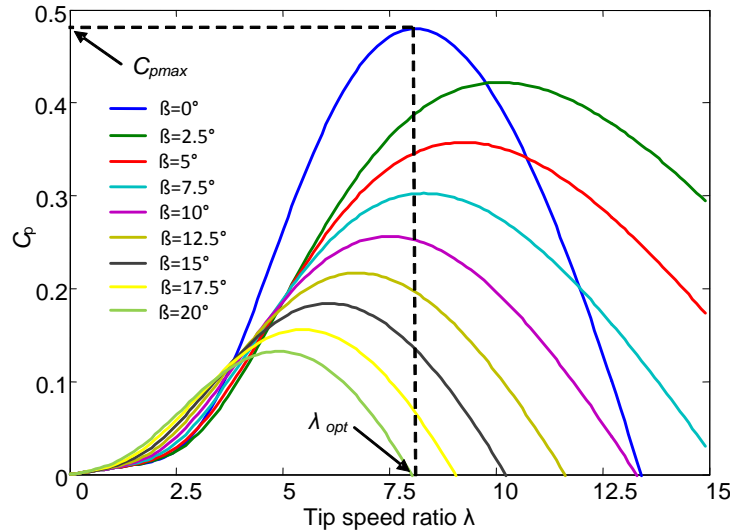
Fig.7.5. Power coefficient C_p for constant values of β.

7.3. Variable-Speed Wind Turbine Systems

7.3.1. Variable Speed Control Reference

Operating with a constant pitch angle $\beta = 0^o$, the maximum coefficient $C_p = C_{pmax} = 0.48$ is achieved for a λ value of $\lambda_{opt} = 8.1$ (see Fig.7.5). Thus, the optimal angular speed is given by:

$$\Omega_{opt} = \frac{\lambda_{opt} v_{wind}}{R_b} \, , \tag{7.5}$$

and the maximum mechanical power by:

$$P_{m\_max} = \frac{1}{2} \rho A C_{pmax} v_{wind}^3 . \tag{7.6}$$

Fig.7.6 shows the typical three regions of control for a WT (Camblong 2008, Fernando D. et al. 2007). In Region 1, the pitch angle is kept constant at $\beta = 0^o$, and the speed reference provided to the controller is the optimal one ($\Omega^* = \Omega_{opt}$). Therefore, maximum mechanical power (P_{m_max}) is obtained from the wind. This interval starts with a minimum wind speed V_{min}. The WT does not operate for wind speeds below that

minimum because the captured wind energy is not large enough to compensate for the losses and operation costs.
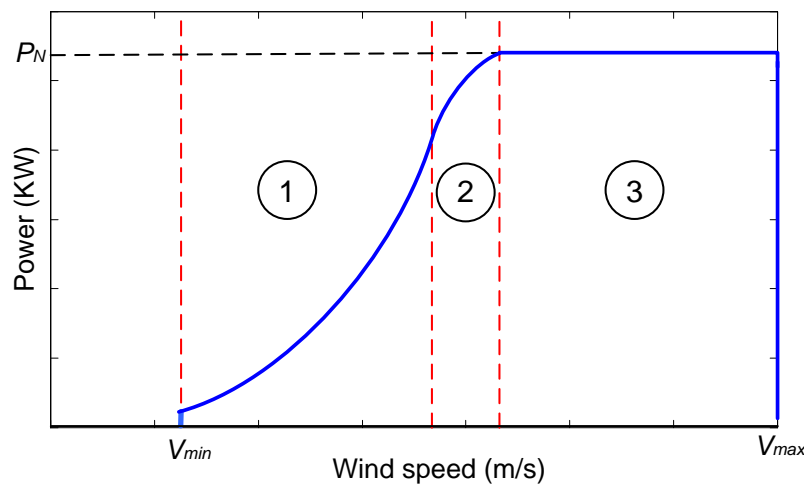
Fig.7.6. Control regions for the WT.

In this study, the control strategy is focused on Region 1, that is, a variable speed and fixed pitch angle regime (Fernando D. et al. 2007). This control strategy is commonly used in commercial WTs, especially when operating under low and medium wind speeds.

Region 2 is a transition interval between the optimum power curve of Region 1 and the constant power line of Region 3. In this region, the rotor speed is limited in order to both maintain acoustic noise emission below an admissible level and to keep centrifugal forces below the values tolerated by the rotor.

Finally, in Region 3, constant speed is maintained at the rated value by controlling the blade pitch angle (Fernando D. et al. 2007, Jauch et al. 2007). In such conditions, the generated power is the rated value (P_N). When the wind speed is very high and above a maximum value (V_{max}), the WT has to be stopped to avoid overloading the mechanical structure.

7.3.2. PMSG Modeling

The PMSG can be modeled by the following equations, represented in the rotating *dq* reference frame:

$$v_d = R_s i_d + L_d \frac{d}{dt} i_d - \omega_e L_q i_q \quad \text{and} \tag{7.7}$$

$$v_q = R_s i_q + L_q \frac{d}{dt} i_q + \omega_e L_d i_d + \omega_e \Psi_m, \tag{7.8}$$

where v_d and v_q are the stator voltages (V), i_d and i_q are the stator currents (A), R_s is the stator resistance (Ω), L_d and L_q are the machine inductances (H), ω_e is the electrical speed (rad/s), and Ψ_m is the magnetic flux (Wb). The main parameters of this machine are given in Appendix F.

The electrical torque (T_e) is obtained from the following expression:

$$T_e = \frac{3}{2} p \left[\Psi_m i_q + \left(L_d - L_q \right) i_d i_q \right], \tag{7.9}$$

where p is the pair of poles. The machine's rotor dynamics are described by:

$$T_m + T_e = B \omega_r + J \frac{d\omega_r}{dt}, \tag{7.10}$$

where B is the rotational friction (kg·m^2/s), J is the rotational inertia (kg·m^2), ω_r the rotational speed (rad/s), and T_m is the torque produced by the wind (N·m). Note that the electrical torque T_e takes negative values because the machine operates as a generator.

Fig.7.7 shows the PMSG electrical and mechanical model. Note that (7.9) has been simplified in this scheme by assuming the term $(L_d\text{-}L_q)i_d i_q$ to be negligible for two reasons; L_d and L_q are quite similar (L_d=L_q=L), and the d reference current is usually zero (i^*_d=0).
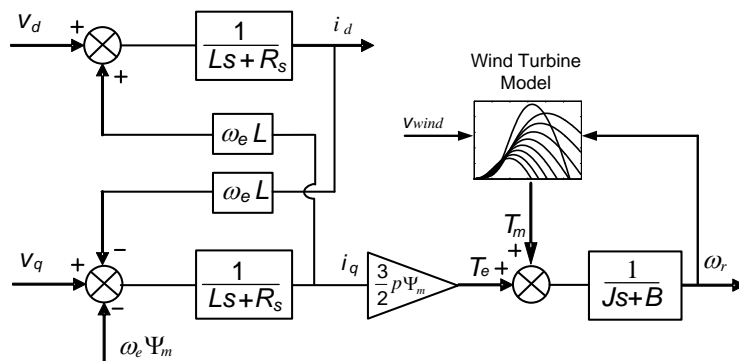
Fig.7.7 Electrical and mechanical model of the PMSG.

7.4. Field-Oriented Control Strategy

For operation in Region 1 (Fig.7.6), the rotor speed needs to be maintained at the optimal speed (Ω_{opt}). The FOC diagram and the model of a WT-connected converter are shown in Fig.7.8. The FOC has the following control loops:

1. An external mechanical loop, which is responsible for speed regulation.

2. Two current loops, which adjust the generator currents (i_d and i_q).
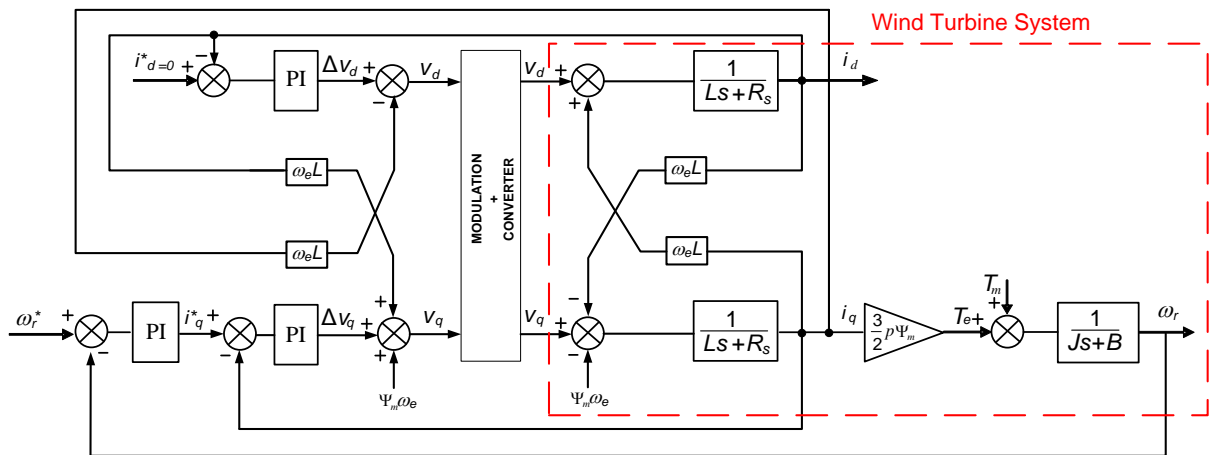
Fig.7.8. Model and control of the wind turbine system.

Observe in Fig.7.8 that the coupled terms *($\omega_e L i_d$ and $\omega_e L i_q$)* and the magnetic flux on the *q* axis (*$\Psi_m \omega_e$*) of the machine model are compensated in the control stage as feedforward terms. Consequently, the voltages provided by the current PI regulators (Δv_d and Δv_q) are the only variables that are eventually applied to the transfer functions of the system ($1/(Ls+R_s)$).

After compensating the known terms, the resulting block diagram of the FOC is shown in Fig.7.9, and a general scheme of the whole system is shown in Fig.7.10.

The optimal speed calculated according to the operating point (Section 7.3.1) is provided as a reference to the external speed loop ($\omega_r^* = \Omega_{opt}$), which generates the quadrature current reference (i_q^*). The outputs of the current loops are the power converter's voltage demands (v_d and v_q).
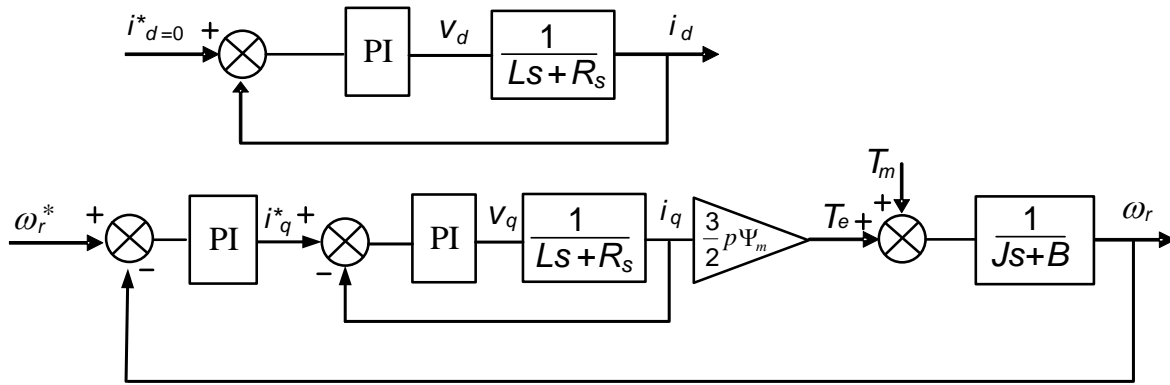
Fig.7.9. Current and speed control loops after compensating the known terms.
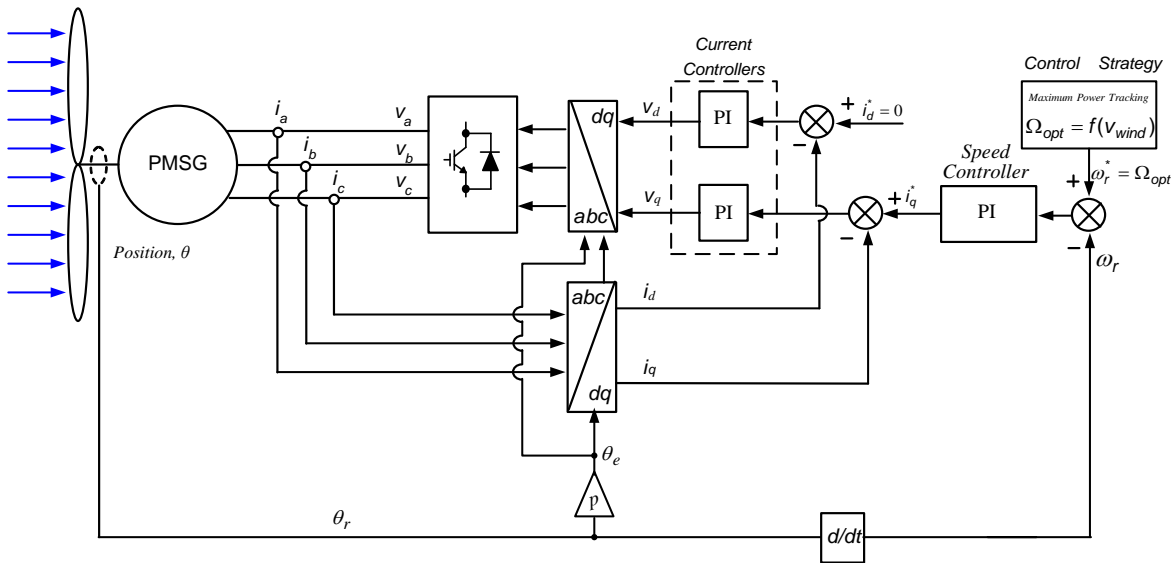
Fig.7.10. Simplified FOC scheme applied to the WT system.

The current loops are not critical because the current dynamic is relatively fast. The regulators are usually implemented by standard PIs. However, the external loop dynamics are slower and, additionally, the mechanical speed reference provided changes continuously because it depends on wind speed. For these reasons, this critical control loop will be the main issue of this research.

7.4.1. Tuning the PIs

After decoupling the current loops, the electrical and mechanical plants can be simplified to first-order transfer functions as follows:

$$G_1(s) = \frac{1}{Ls + R_s} ,$$

(7.11)

$$G_2(s) = \frac{1}{Js + B} \quad (7.12)$$

The PI controller is mathematically represented by:

$$G_C(s) = k_p + \frac{k_i}{s} = k_i \frac{1 + \frac{k_p}{k_i}s}{s} \quad . \quad (7.13)$$

The closed-loop transfer functions are as follows:

$$G_{1\_cl}(s) = \frac{\frac{k_{i1}}{L}(\frac{k_{p1}}{k_{i1}}s + 1)}{s^2 + s(\frac{k_{p1} + R_s}{L}) + \frac{k_{i1}}{L}} \quad , \quad (7.14)$$

$$G_{2\_cl}(s) = \frac{\frac{k_{i2}}{J}(\frac{k_{p2}}{k_{i2}}s + 1)}{s^2 + s(\frac{k_{p2} + B}{J}) + \frac{k_{i2}}{J}} \quad . \quad (7.15)$$

To improve the control bandwidth, a pre-filter $G_{f(s)}$ is included in the control loops (Fig.7.11). This pre-filter is designed to cancel out the zero of the closed-loop transfer functions by the following expression:

$$G_f(s) = \frac{1}{\frac{k_p}{k_i}s + 1} \quad . \quad (7.16)$$

Two methods shall be used to determine the parameters of the speed controller. The first method is carried out by defining a rise time (T_r) and a damping factor (D_f). Henceforth in this chapter, this tuning method will be called the imposed damping factor (IDF) strategy.
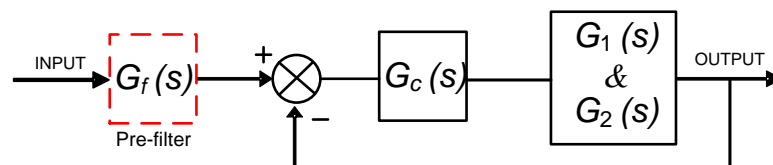
Fig.7.11. Control configuration.

Fig.7.12 shows the root locus of the mechanical system and the controller under the IDF tuning strategy. Using this strategy, the complex poles of the controller are placed at the intersection of the predefined damping factor and the settling time lines (Fig.7.12(a)). In this example, T_r and D_f are defined as 0.5 seconds and 0.707, respectively (this will result in an overshoot of less than 4.33%).
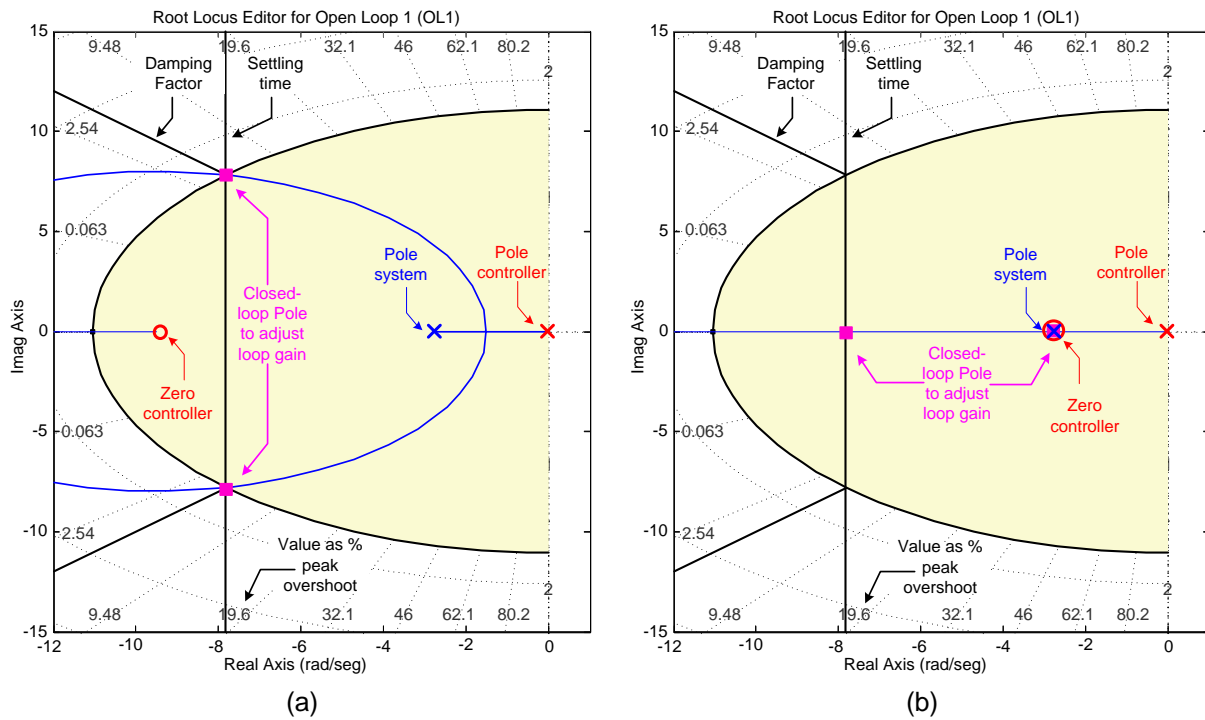
Fig.7.12.Root-locus of the speed controller: (a) IDF (D_f=0.707) and (b) ZPC tuning strategies.

The second tuning strategy (Fig.7.12(b)) is based on canceling the pole of the system by the zero of the controller. Using this zero-pole cancelation (ZPC) strategy, the same rising time is selected in order to make the two tuning strategies comparable.

The method of tuning the control parameters is not relevant because the outer mechanical loop response is much slower than that of the inner current loops. Therefore, the current loops can be tuned by either of the two methods. In this work, the parameters k_{p2} and k_{i2} of the current loops are determined by the IDF method, including pre-filters. All of the PI parameter values used in the simulation and experimental results are given in Appendix F.

Fig.7.13 shows a step response of the mechanical plant with a settling time at 98% in the specified time (T_r=0.5 s). In Fig.7.13(a), the IDF tuning strategy with and without

a pre-filter has been applied. The results show that, with a pre-filter, unlike the case without a pre-filter, a negligible overshoot is obtained. In Fig.7.13(b), the ZPC tuning strategy is applied and, as expected, the output shows a first-order response.
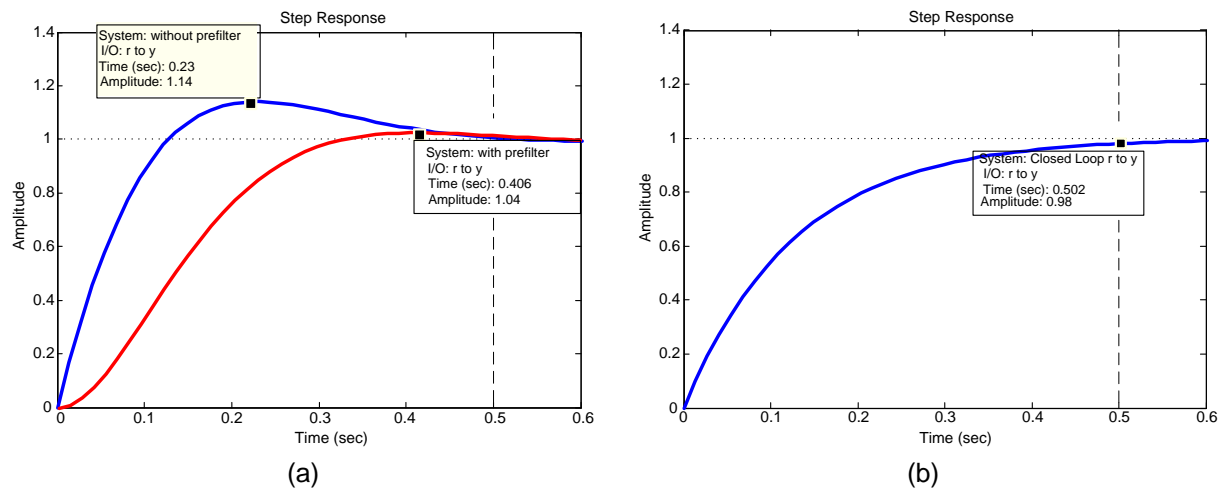
Fig.7.13. Step response with a settling time of T_r=0.5 s: (a) IDF strategy with and without pre-filter and (b) ZPC strategy.

Fig.7.14 illustrates the response of the system under a torque disturbance (torque step). A similar analysis was performed in (Robles et al. 2008); however, in that case, the pre-filter was not considered. Note that the IDF tuning strategy (D_f=0.707) provides a faster response than the ZPC method. Nevertheless, this strategy requires more control actuation (mechanical torque).

Minimizing torque disturbance effects is important in controlling the speed of the WT because torque disturbances are continuously produced due to wind speed changes.

Fig.7.15 shows the simulation results of the complete WECS model obtained with the wind model based on the block developed by RISØ National Laboratory (Florin Iov et al. March 2004), which is based on Kaimal spectra. The wind speed is calculated as an average value of the fixed-point wind speed over the whole rotor, and it takes the tower shadow and the rotational turbulences into account.

Fig.7.15 also shows the energy increment ratio obtained using the IDF strategy (with pre-filter) compared to the ZPC strategy, given by:

$$\Delta\boldsymbol{\varepsilon}(\%) = \frac{\boldsymbol{\varepsilon}_{IDF} - \boldsymbol{\varepsilon}_{ZPC}}{\boldsymbol{\varepsilon}_{ZPC}}100. \tag{7.17}$$
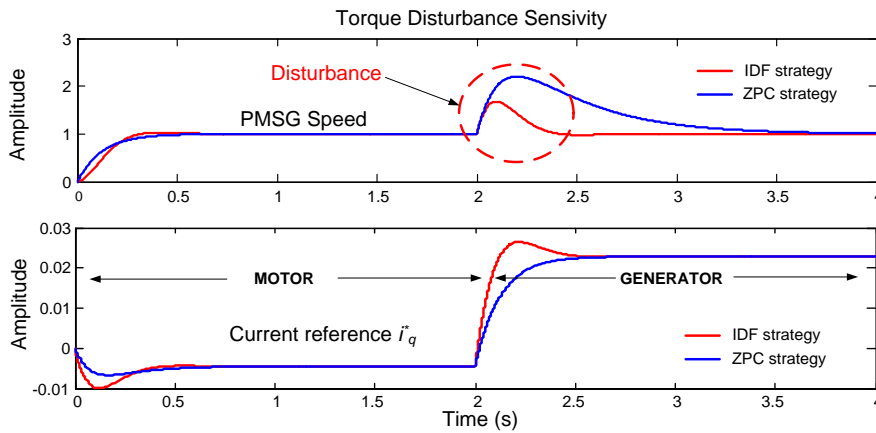
Fig.7.14. Disturbance load effect.
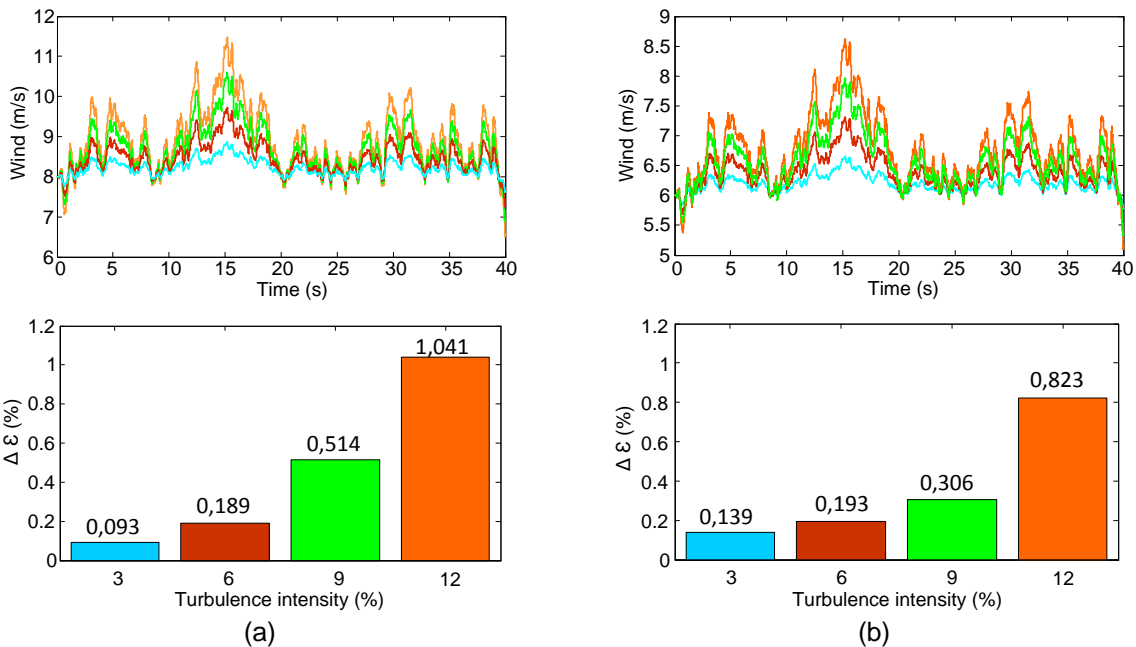
Fig.7.15. Energy increment ratio (%): (a) average wind of 8 m/s and (b) 6 m/s.

In Fig.7.15(a), the average wind speed is 8 m/s, and four turbulence intensities are tested: 12%, 9%, 6%, and 3%. Note that the energy increment ratio ($\Delta\varepsilon$) is larger when using the IDF method than it is when using the ZPC method. Furthermore, this increment is even more significant during large turbulences.

Similar results are shown in Fig.7.15(b) for an average wind speed of 6 m/s. The same turbulence intensities were used.

7.4.2. Experimental Results

7.4.2.1 System Description

The control tuning strategies have been developed and tested using a dSPACE 1103. This hardware provides flexible implementation in MATLAB/SIMULINK of the WT model emulator control strategy. A control panel has been developed using the ControlDesk software (Fig.7.16). This software provides an easily handled interface between the dSPACE 1103 and the Simulink blocks. This screen not only represents the different signals from the WECS, but it also allows for changing the operating parameters of the system online.
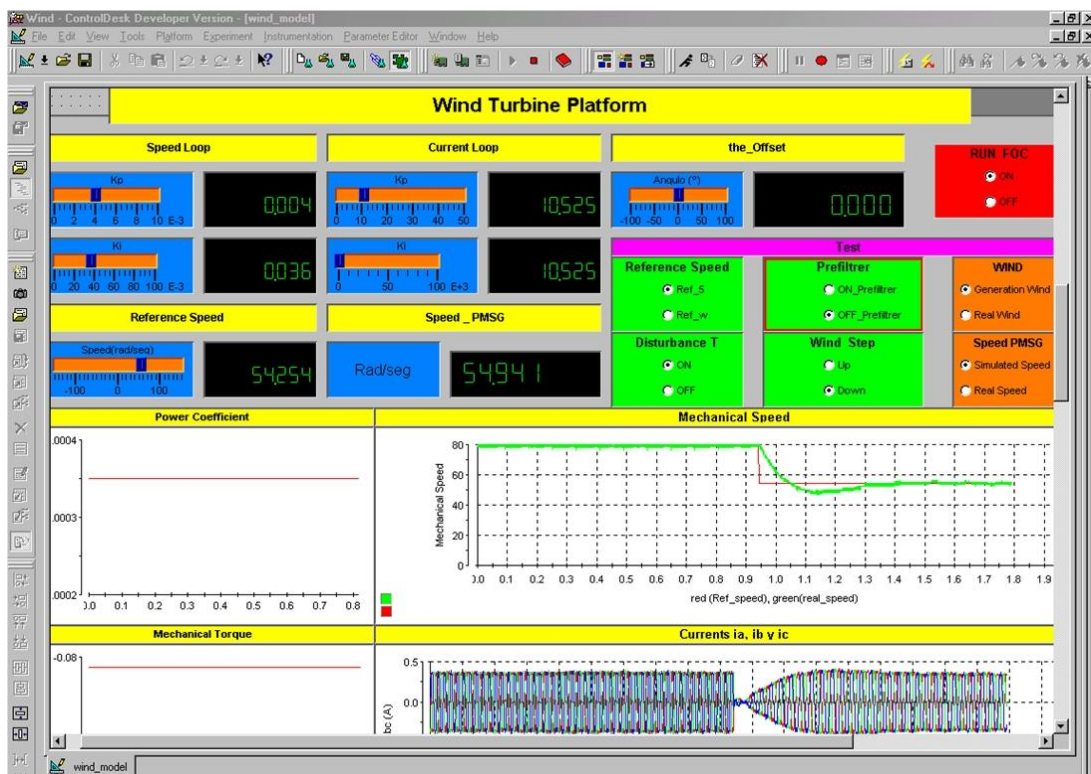
Fig.7.16 Developed ControlDesk screen.

The experimental platform of the WECS is shown in Fig.7.17. The main data of this platform is given in Appendix F. A dc motor is used to emulate the mechanical power coming from the wind according to the WT model described in Section 7.2.1. A low-power PMSG is controlled by a three-phase inverter. A power supply provides the inverter's dc-link voltage. Some resistors are connected to the dc bus to dissipate the

energy produced in the system. Two main tasks are given to the dSPACE: (i) to provide the torque reference from the WT emulator and (ii) to control the PMSG by providing the PWM signals for the inverter. Fig.7.18 shows this experimental setup.
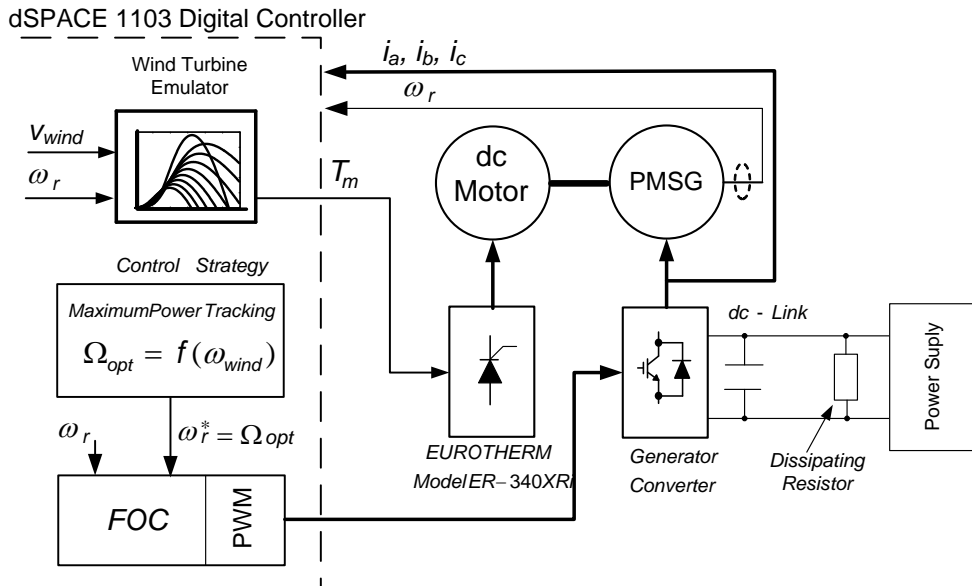
Fig.7.17. Block diagram of the experimental platform.
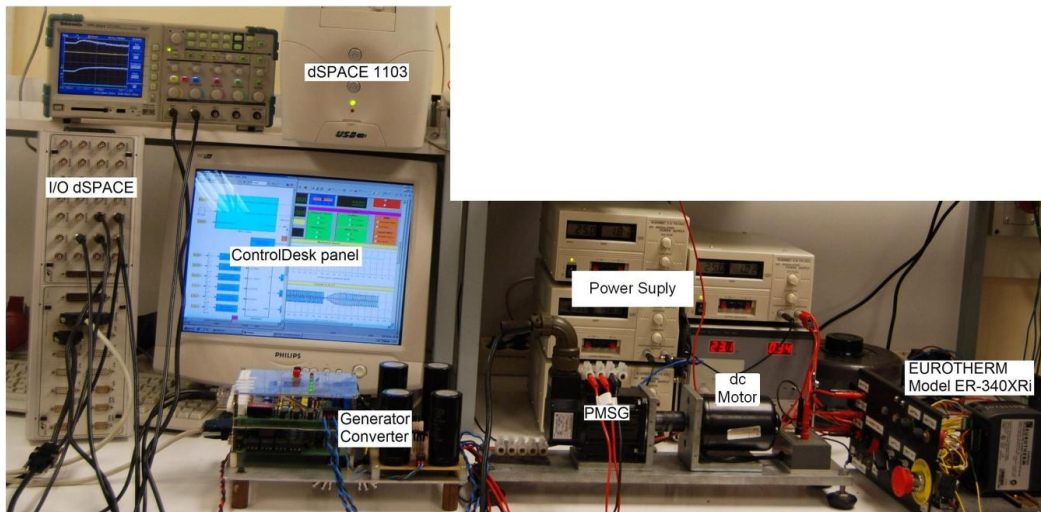
Fig.7.18. View of the experimental setup.

7.4.2.2 Experimental Results

Some experimental results were obtained using the different tuning strategies studied in this work. Fig.7.19 and Fig.7.20 show some results using the PMSG operating as a motor. These figures show the rotational speed (ω_r) and the reference current (i^*_q) under a reference speed step of 25 rad/s. This test verifies the previous

results obtained by simulation. Furthermore, it confirms that the values of the different parameters were obtained correctly from previous tests (mechanical and electrical coefficients such as J, B, R_s and L).

Fig.7.19(a) shows the results using the IDF method (D_f=0.707) for tuning the controllers. The speed shows a significant overshoot (ω_{r_IDF}) when a pre-filter is not included in the control loop. On the other hand, a better response is obtained when a pre-filter is used ($\omega_{r\_IDF\_pre-filter}$). Furthermore, the control energy required without the pre-filter ($i^*_{q\_IDF}$) is larger than with the pre-filter ($i^*_{q\_IDF\_pre-filter}$). As a consequence, the currents i_a, i_b and i_c in Fig.7.19(b) show a smoother dynamic when using a pre-filter than when not using a pre-filter.

Fig.7.20 shows the results obtained using the ZPC strategy. As expected, the system performs with a first-order behavior.

A second test is performed that makes the PMSG work as a generator. In this test, the system operates at an optimum speed reference given in (7.5), and some mechanical torque disturbances from the wind model are added. Fig.7.21 shows a comparison between two strategies for tuning the speed controller: IDF (including a pre-filter) and ZPC. The results show that the generator speed is significantly disturbed when using the ZPC strategy. Therefore, it is less efficient at controlling the PMSG speed during wind disturbances.

(a)   (b)
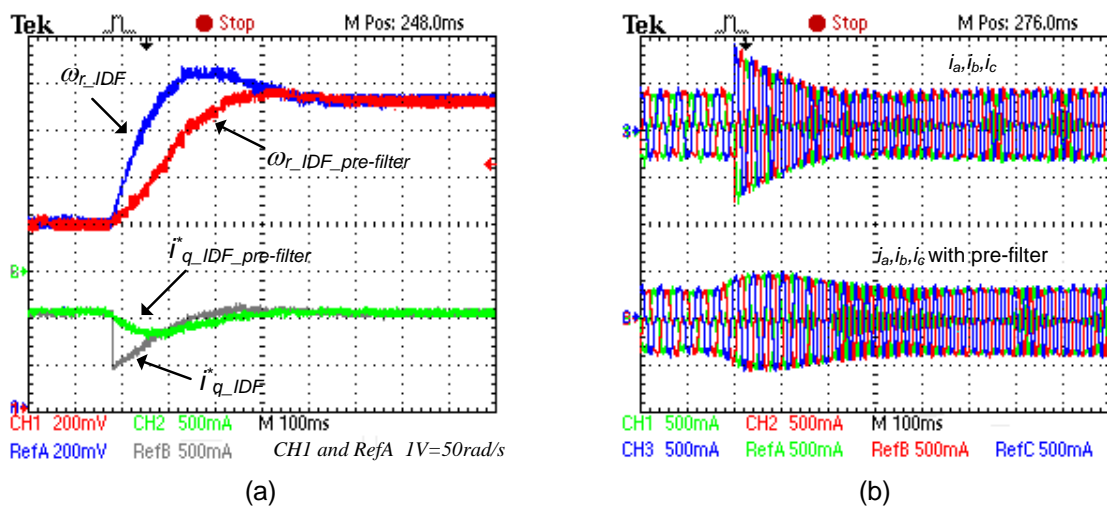
Fig.7.19. Step response with and without a pre-filter using the IDF: (a) mechanical speed and reference current and (b) PMSG currents.

(a)   (b)
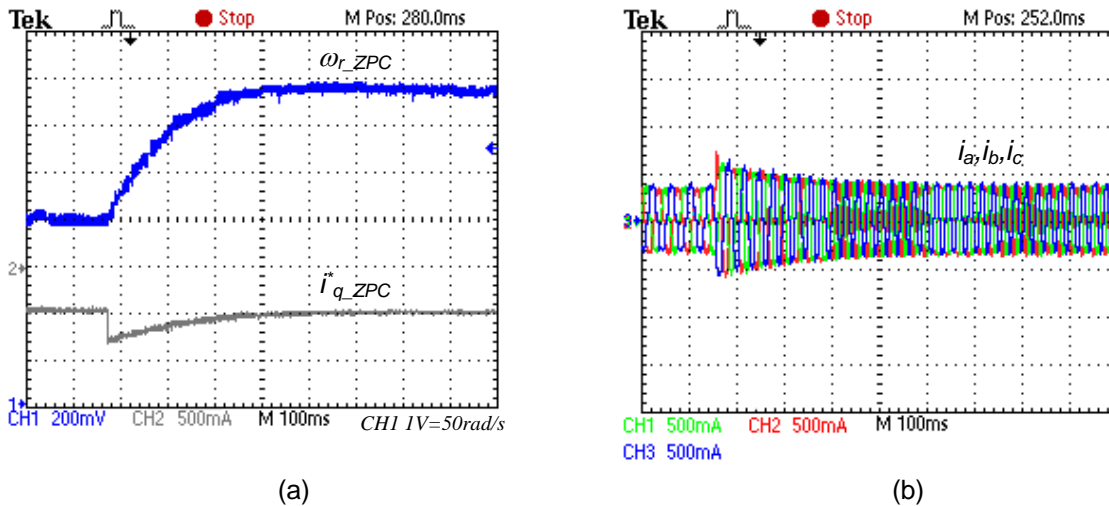
Fig.7.20. Step response using the ZPC strategy: (a) mechanical speed and reference current, and (b) PMSG currents.
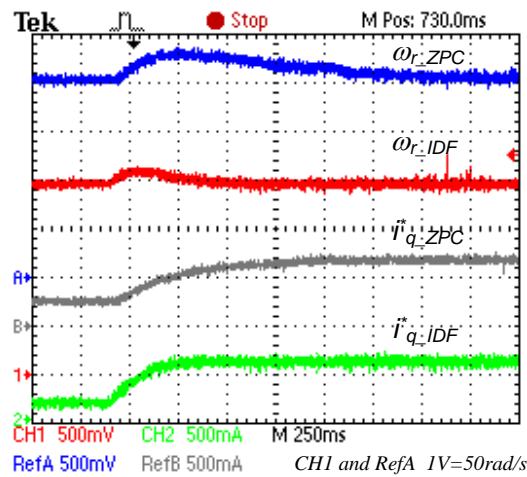
Fig.7.21.Disturbance load effect.

A third test is performed that also makes the PMSG operate as a generator. In this test, a wind step is applied, which implies a mechanical torque step. However, in this case, the wind speed reference also changes according to (7.5). Fig.7.22 shows a comparison between the two tuning strategies, IDF and ZPC. The results show that the generator speed response is significantly better when using the IDF strategy. The ZPC strategy produces a high overshoot and slower dynamics with respect to the desirable response shown in Fig.7.20.

Fig.7.23 shows several experimental results from the WECS using the wind model (Florin Iov et al. March 2004).
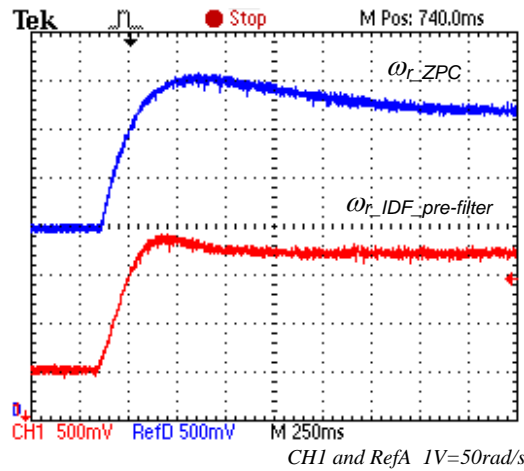
Fig.7.22.PMSG speed response when a wind step is applied.
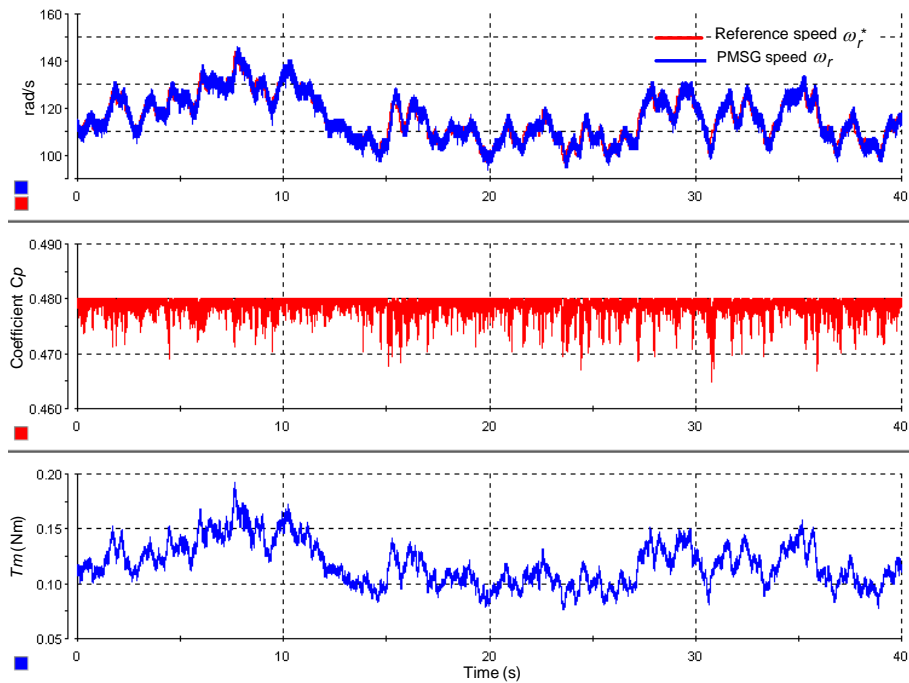
Fig.7.23. Experimental results shown in the ControlDesk panel.

The variables shown in Fig.7.23 are the reference and real rotor speeds (ω_r^* and ω_r, respectively), the performance coefficient (C_p), and the mechanical torque (T_m). The values used in the wind model are an average wind speed of 5 m/s and turbulence intensity of 12%.

These results show good performance of the WECS when the controller is tuned using the IDF strategy (with pre-filter). Furthermore, the C_p coefficient is, most of the time, close to the optimal value of 0.48 despite the large rotational turbulence.

7.5. Chapter Conclusions

In this work, a PMSG-based WECS has been modeled with WT aerodynamics included. An FOC of the WT is implemented, and two different tuning strategies of the PIs are analyzed and compared. The tuning strategies are IDP, with and without pre-filter, and ZPC. Simulation results from the studied methods have been tested under speed reference changes and disturbances. A WECS platform was built to verify the simulation results experimentally.

In summary, the IDF tuning method with a pre-filter has shown better performance during wind speed disturbances, because not only is the speed overshot lower, but the time response is also faster. As a consequence, greater energy is captured from the wind, and it is produced with a lower power coefficient ripple. This is a remarkable feature, considering both that the energy will be finally injected into the electrical grid and that it will require steady production.

7.6. Chapter References

Baroudi JA, Dinavahi V, Knight AM. 2007. A review of power converter topologies for wind generators. Renewable Energy 32: 2369-2385.

Billy Muhando E, Senjyu T, Urasaki N, Yona A, Kinjo H, Funabashi T. 2007. Gain scheduling control of variable speed WTG under widely varying turbulence loading. Renewable Energy 32: 2407-2423.

Binder A, Schneider T. 2005. Permanent magnet synchronous generators for regenerative energy conversion - a survey. Pages 10 pp.-P.10. Power Electronics and Applications, 2005 European Conference on.

Bueno EJ. 2005. Optimización del comportamiento de un convertidor de tres niveles NPC conectado a la red elèctricaUniversidad de Alcalá, Alcalá de Henares.

Cadenas E, Rivera W. 2009. Short term wind speed forecasting in La Venta, Oaxaca, México, using artificial neural networks. Renewable Energy 34: 274-278.

Camblong H. 2008. Digital robust control of a variable speed pitch regulated wind turbine for above rated wind speeds. Control Engineering Practice 16: 946-958.

Camblong H, Tapia G, Rodriguez M. 2006a. Robust digital control of a wind turbine for rated-speed and variable-power operation regime. Control Theory and Applications, IEE Proceedings - 153: 81-91.

Camblong H, Lescher F, Guillaud X, Vechiu I. 2006b. Comparison of Three Wind Turbine Controller Synthesis Methodologies. Pages 1908-1913. Industrial Technology, 2006. ICIT 2006. IEEE International Conference on.

Casadei D, Profumo F, Serra G, Tani A. 2002. FOC and DTC: two viable schemes for induction motors torque control. Power Electronics, IEEE Transactions on 17: 779-787.

Fernando D., Hernán De Battista, J. R. 2007. Wind turbine control systems (Principles, Modelling and Gain Scheduling Design).

Florin Iov, Anca Daniela Hansen, Poul Sørensen, Blaabjerg F. March 2004. Wind Turbine Blockset in Matlab/Simulink (General Overview and Description of the Models). Aalborg University: Institute of Energy Technology. Report no.

Heier S. 1998. Grid integration of wind energy conversion systems.

Jauch C, Islam SM, Sørensen P, Bak Jensen B. 2007. Design of a wind turbine pitch angle controller for power system stabilisation. Renewable Energy 32: 2334-2349.

Jul-Ki S, Jong-Kun L, Dong-Choon L. 2006. Sensorless speed control of nonsalient permanent-magnet synchronous motor using rotor-position-tracking PI controller. Industrial Electronics, IEEE Transactions on 53: 399-405.

Kristiansson B, Lennartson B. 2006. Robust tuning of PI and PID controllers: using derivative action despite sensor noise. Control Systems Magazine, IEEE 26: 55-69.

Liserre M, Dell'Aquila A, Blaabjerg F. 2003. Genetic algorithm based design of the active damping for a LCL-filter three-phase active rectifier. Pages 234-240 vol.231. Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE.

López P, Velo R, Maseda F. 2008. Effect of direction on wind speed estimation in complex terrain using neural networks. Renewable Energy 33: 2266-2272.

Mohamed AZ, Eskander MN, Ghali FA. 2001. Fuzzy logic control based maximum power tracking of a wind energy system. Renewable Energy 23: 235-245.

Mohamed YARI. 2007. Design and Implementation of a Robust Current-Control Scheme for a PMSM Vector Drive With a Simple Adaptive Disturbance Observer. Industrial Electronics, IEEE Transactions on 54: 1981-1988.

Monroy A, Alvarez-Icaza L. 2006. Real-time identification of wind turbine rotor power coefficient. Pages 3690-3695. Decision and Control, 2006 45th IEEE Conference on.

Murray A, Palma M, Husain A. 2008. Performance Comparison of Permanent Magnet Synchronous Motors and Controlled Induction Motors in Washing Machine Applications Using Sensorless Field Oriented Control. Pages 1-6. Industry Applications Society Annual Meeting, 2008. IAS '08. IEEE.

Pena R, Cardenas R, Blasco R, Asher G, Clare J. 2001. A cage induction generator using back to back PWM converters for variable speed grid connected wind energy system. Pages 1376-1381 vol.1372. Industrial Electronics Society, 2001. IECON '01. The 27th Annual Conference of the IEEE.

Portillo RC, Prats MM, Leon JI, Sanchez JA, Carrasco JM, Galvan E, Franquelo LG. 2006. Modeling Strategy for Back-to-Back Three-Level Converters Applied to High-Power Wind Turbines. Industrial Electronics, IEEE Transactions on 53: 1483-1491.

Pou J, Pindado R, Boroyevich D, Rodriguez P. 2004. Limits of the neutral-point balance in back-to-back-connected three-level converters. Power Electronics, IEEE Transactions on 19: 722-731.

Pou J, Zaragoza J, Capella G, Gabiola I, Ceballos S, Robles E. 2009. Current balancing strategy in parallel-connected legs of power inverters. Pages 1-9. Power Electronics and Applications, 2009. EPE '09. 13th European Conference on.

Rabelo B, Hofmann W. 2001. Optimal active and reactive power control with the doubly-fed induction generator in the MW-class wind-turbines. Pages 53-58 vol.51. Power Electronics and Drive Systems, 2001. Proceedings., 2001 4th IEEE International Conference on.

Robles E, Ceballos S, Pou J, Arias A, Martin JL, Ibanez P. 2008. Permanent-magnet wind turbines control tuning and torque estimation improvements. Pages 742-745. Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on.

Schiemenz I, Stiebler M. 2001. Control of a permanent magnet synchronous generator used in a variable speed wind energy system. Pages 872-877. Electric Machines and Drives Conference, 2001. IEMDC 2001. IEEE International.

Taftiicht T, Agbossou K, Cheriti A, Doumbia ML. 2006. Output Power Maximization of a Permanent Magnet Synchronous Generator Based Stand-alone Wind Turbine. Pages 2412-2416. Industrial Electronics, 2006 IEEE International Symposium on.

Teodorescu R, Blaabjerg F. 2004. Flexible control of small wind turbines with grid failure detection operating in stand-alone and grid-connected mode. Power Electronics, IEEE Transactions on 19: 1323-1332.

Yang SS, Zhong YS. 2007. Robust speed tracking of permanent magnet synchronous motor servo systems by equivalent disturbance attenuation. Control Theory & Applications, IET 1: 595-603.

Zhe C, Guerrero JM, Blaabjerg F. 2009. A Review of the State of the Art of Power Electronics for Wind Turbines. Power Electronics, IEEE Transactions on 24: 1859-1875.

Zhong L, Rahman MF, Hu WY, Lim KW, Rahman MA. 1999. A direct torque controller for permanent magnet synchronous motor drives. Energy Conversion, IEEE Transactions on 14: 637-642.

Chapter 8.

Conclusions and Future Research

This chapter is dedicated to reviewing the final conclusions of the thesis, to showing its main contributions, and to proposing some future research work. Furthermore, the publications and patents derived from this thesis are also shown in this chapter.

8.1. Conclusions

This thesis studies and proposes new modulation strategies based on CB-PWM for the NPC converter. All these modulation strategies have their counterparts based on SVM. Fig.8.1 shows a classification of the main modulation strategies which includes both SVM and CB-PWM; the proposed modulation strategies are also included.

The NTV based on CB-PWM proposed in this thesis has practically the same features as the SV-PWM-based NTV. However, the CB-PWM strategy has some advantages over its SVM counterpart, such as its simplified scheme for practical implementation and some reduction of switching losses.
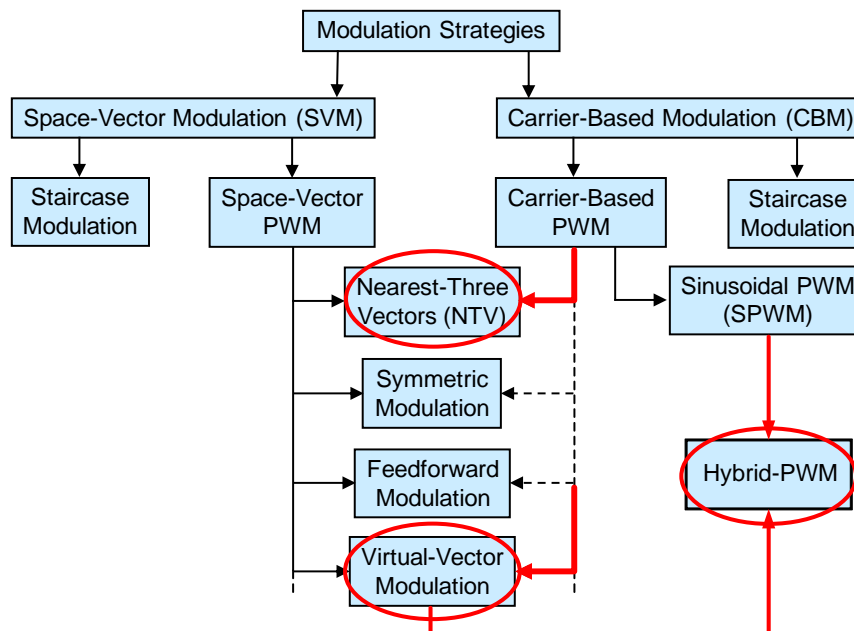
Fig.8.1. Space vector modulation strategies.

The virtual-vector modulation is able to completely overcome one of the main drawbacks in NPC converters: the low-frequency NP voltage oscillations that could appear for some operation points. However, implementation of this algorithm from an SVM standpoint is not simple and, additionally, some voltage balance control should be provided since the system has no natural voltage balance.

The proposed carrier-based DSPWM can be implemented by a simple and very fast processing algorithm that makes it ideal for real-time implementation.

Furthermore, the optimal control and the limiter proposed in this thesis solve the voltage balance problem. The proposed solution is a step forward for the virtual-vector modulation.

On the other hand, from a standpoint of switching losses, both the virtual-vector modulation and the DSPWM are worse than other modulation strategies. It seems that solving the NP voltage balance issue leads to a significant increase in the switching losses of power devices. In fact, a new modulation is proposed that represents a compromise solution between switching losses and NP voltage oscillation amplitudes. The HPWM is able to find a balance between both aspects. Furthermore, a parameter that defines the mixture ratio between SPWM and DSPWM is defined (*D*) and a tracking method for determining the optimal clamping intervals are presented (Ψ). The two strategies are combined into a control loop to limit the maximum amplitude of the NP voltage ripple. This is a very interesting feature from a practical point of view, since the maximum voltage applied to the capacitors and to the power devices is limited to a defined value.

Nowadays, the use of two back-to-back-connected NPC converters is becoming a realistic solution in WECS. The main advantage of using this configuration is an increase in WT rated power. In this application, when there is a voltage sag in the grid voltages, the grid-connected converter is required to provide reactive currents. As a consequence, an unbalancing current is introduced into the NP, producing significant NP voltage oscillations. With the use of the modulation strategies proposed in this dissertation, the NP voltage oscillations can be limited or even eliminated. In order to achieve the best performance, different possibilities can be chosen for implementing the proposed modulation strategies in the two NPC converters of a back-to-back configuration.

The NPC converters of a back-to-back configuration can be controlled independently. The main control strategies used in industrial applications are the FOC and the VOC schemes for the wind turbine converter and the grid-connected converter, respectively. In this thesis, some control improvements have been made regarding the dynamic performance of the system and tuning methodologies.

Standard PI controllers may be used in nonlinear systems, such as in WT applications. However, the dynamic performance of the system can be improved significantly by using a nonlinear controller. The fuzzy supervisor proposed in this thesis dynamically adjusts the PI parameters in order to improve the performance of a grid-connected converter under load changes and in rectifier mode. On the turbine side, the use of a good strategy for tuning a standard PI could significantly improve system behavior.

8.2. Main Contributions

The research work of this thesis has focused on meeting the objectives given in Chapter 1. A review of the main contributions is given in the following.

- <u>Development of a CB-PWM strategy as an alternative to the NTV-SVM strategy</u>.

The proposed NTV modulation implemented under CB-PWM is an alternative to the NTV-SVM strategy. The main feature of this strategy, as compared with the NTV-SVM strategy, is its simplicity for digital implementation.

This research shows by simulation and experimental results a good dynamic for balancing the voltage in dc-link capacitors. What's more, this modulation mitigates the low-frequency oscillations at the NP. This has been possible thanks to a zero-sequence voltage injection.

The main difference between the proposed CB-PWM and the NTV-SVM strategies is that CB-PWM cannot fully cancel the low-frequency NP voltage oscillations when operating under low modulation indices. However, the amplitude of the oscillation is not significant, and the benefit of lower switching losses under low modulation indices is remarkable. Lower switching losses occur because, with the CB-PWM strategy, four-step transition sequences are avoided.

- <u>Completely removing low-frequency voltage oscillations in an NPC converter</u>.

The developed DSPWM is able to attain the maximum amplitudes achievable under linear modulation, and its algorithm is very simple and can therefore be quickly

processed in real time. The only drawback of this strategy is that, for any modulation index in linear operation mode, the switching frequencies of the devices are one-third higher than with a standard SPWM. This algorithm has been tested through simulation and experimental results, followed by an accurate analysis of the total losses.

This modulation strategy could be of interest in applications such as active filtering, in which the current harmonics are not at fundamental frequency. In such an application, other modulation schemes could produce instability in the system when operating with certain current harmonics.

- Development of an optimal compensator and a limiter to DPWM.

One shortcoming of the DSPWM is that it does not provide natural voltage balancing; therefore, the modulation algorithm requires the inclusion of a balance compensator.

The optimal compensator developed in this dissertation guarantees a maximum balancing dynamic without decreasing the quality of the output voltage waveforms. The proposed algorithm presents a number of advantages: most importantly, it does not require any parameter adjustment and it operates optimally under all of the operating conditions of the system. In addition, stability is always guaranteed.

Together with the optimal compensator, a dynamic limiter has also been developed. This limitation is necessary because the maximum compensation value depends on the instantaneous values of the modulation signals. If the compensation signal went beyond the maximum dynamic value, an opposite balancing effect would be produced. Both contributions, the optimal compensator and the dynamic limiter, could be extended to converters with more than three levels.

- Development of an HPWM strategy able to regulate the low-frequency NP voltage oscillation amplitude and minimize switching losses.

The HPWM is a compromise solution between DSPWM and SPWM. This strategy has the capability of modifying online the degree of mixture between both modulations (SPWM and DSPWM). The main characteristic of this hybrid modulation is the reduction in switching losses of the power devices, though at the cost of having

some low-frequency voltage oscillations at the NP. This strategy has been tested by simulation and experiment.

A control loop for the hybrid modulation has also been designed so that the maximum amplitude of the low-frequency NP voltage oscillation amplitudes can be limited to a given value. Therefore, the maximum voltage that the power devices of the converter and the dc-link capacitors have to stand is defined and limited.

Furthermore, a tracking method is also developed in order to further reduce the voltage oscillation amplitudes in HPWM.

- <u>Improvement of the grid-side control</u>.

On the grid side, a VOC technique with PI controllers has been implemented in order to control the total dc-link voltage of a grid-connected NPC converter under load changes. The well known zero-pole cancelation strategy for tuning the parameters of the PI is used. However, taking into account that the system is nonlinear, a fuzzy supervisor has been developed in order to adjust the PI parameters during transitory processes. The use of this supervisor significantly improves the dynamic of the system under load changes when the converter is working as a rectifier.

- <u>Improvement of the generator-side control</u>.

The FOC technique with PI controllers has been implemented on the generator side NPC converter of a variable-speed WT based on a PMSG. The main contribution from using the FOC technique has been the evaluation of different tuning strategies for improving system performance during different wind disturbances. The compared tuning strategies are the IDF, with and without a pre-filter, and the ZPC technique. A small-scale WECS laboratory prototype has been used in order to analyze and obtain some experimental results.

8.3. Publications and Patents Derived from the Thesis

This section presents the publications and patents resulting from the research work of the thesis.

<u>Publications related to Chapter 3</u>:

A) Publications indexed in Journal Citation Reports

- Pou J, Zaragoza J, Ceballos S, Saeedifard M, Borojevic D. 2010. A Carrier-Based PWM Strategy With Zero-Sequence Voltage Injection for a Three-Level Neutral-Point-Clamped Converter. Power Electronics, IEEE Transactions on PP: 1-1(This article has been accepted for publication in a future issue of this journal). *Impact Factor* (2010) =3.176

B) International Conferences

- Pou J, Rodriguez P, Zaragoza J, Sala V, Jaen C, Boroyevich D. 2005. Enhancement of Carrier-Based Modulation Strategies for Multilevel Converters. Pages 2534-2539. Power Electronics Specialists Conference, 2005. PESC '05. IEEE 36th.

Publications related to Chapter 4:

A) Publications indexed in Journal Citation Reports

- Pou J, Zaragoza J, Rodriguez P, Ceballos S, Sala VM, Burgos RP, Boroyevich D. 2007. Fast-Processing Modulation Strategy for the Neutral-Point-Clamped Converter With Total Elimination of Low-Frequency Voltage Oscillations in the Neutral Point. Industrial Electronics, IEEE Transactions on 54: 2288-2294. *Impact Factor* (2007) = 2.216.

- Zaragoza J, Pou J, Ceballos S, Robles E, Jaen C, Corbalan M. 2009. Voltage-Balance Compensator for a Carrier-Based Modulation in the Neutral-Point-Clamped Converter. Industrial Electronics, IEEE Transactions on 56: 305-314. *Impact Factor* (2009) = 4.678

B) International Conferences

- Pou J, Rodriguez P, Sala V, Zaragoza J, Burgos R, Boroyevich D. 2005. Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of the low-frequency voltage oscillations in the neutral point. Pages 6 pp. Industrial Electronics Society, 2005. IECON 2005. 31st Annual Conference of IEEE.

- <u>Zaragoza J</u>, Pou J, Ceballos S, Robles E, Jaen C. 2007. Optimal Voltage-Balancing Compensator in the Modulation of a Neutral-Point-Clamped Converter. Pages 719-724. Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on.

C) Patents

- <u>Zaragoza J</u>, Pou J, Ceballos S, Ibáñez P, Hernández C.J. 16-Marzo-2007. Compensador de equilibrado de las tensiones de los condensadores del bus de continua en un convertidor de potencia de tres niveles in Cataluña UPC, ed. P200700739. Spain.

<u>Publications related to Chapter 5</u>:

A) Publications indexed in Journal Citation Reports

- <u>Zaragoza J</u>, Pou J, Ceballos S, Robles E, Ibáñez P, Villate JL. 2009. A Comprehensive Study of a Hybrid Modulation Technique for the Neutral-Point-Clamped Converter. Industrial Electronics, IEEE Transactions on 56: 294-304. *Impact Factor* (2009) = 4.678.

B) Publications not indexed in Journal Citation Reports

- <u>Zaragoza J</u>, Pou J, Ceballos S, Villate JL, Gabiola I. 2007. Hybrid modulation technique for the neutral-point-clamped converter. Przeglad Elektrotechniczny 83: 48-53.

C) International Conferences

- <u>Zaragoza J</u>, Pou J, Ceballos S, Villate JL, Gabiola I. 2007. Hybrid Modulation Technique for the Neutral-Point-Clamped Converter. Pages 1-6. Compatibility in Power Electronics, 2007. CPE '07.

- <u>Zaragoza J</u>, Pou J, Arias A, Ceballos S, Robles E, Ibáñez P, Gabiola I. 2008. Amplitude control of the neutral-point voltage oscillations in the three-level converter. Pages 2473-2477. Power Electronics Specialists Conference, 2008. PESC 2008. IEEE.

- <u>Zaragoza J</u>, Pou J, Ceballos S, Arias A, Ibáñez P. 2008. Tracking method for the hybrid modulation to minimize neutral-point voltage oscillations in the three-level converter. Pages 1095-1098. Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on.

D) Patents

- <u>Zaragoza J</u>, Pou J, Ibáñez P, Robles E, Antxustegi IG. 24-Mayo-2007. Modulador adaptativo híbrido para un convertidor de tres niveles in Robotiker-Tecnalia, ed. P200701425. Spain.

Publications related to Chapter 6:

A) International Conferences

- <u>Zaragoza J</u>, Pou J, Ceballos S, Robles E, Ibáñez P, Guinjoan F. 2006. Control Structure with Fuzzy Supervision of PI Parameters in a Multilevel Converter Application. Pages 1271-1276. Industrial Electronics, 2006 IEEE International Symposium on.

Publications related to Chapter 7:

A) Publications indexed in Journal Citation Reports

- <u>Zaragoza J</u>, Pou J, Arias A, Spiteri C, Robles E, Ceballos S. 2011. Study and experimental verification of control tuning strategies in a variable speed wind energy conversion system. Renewable Energy 36: 1421-1430. *Impact Factor* (2010) = 2.554.

Publications related to Chapter 8:

A) International Conferences

- <u>Zaragoza J</u>, Staines CS, Arias A, Pou J, Robles E, Ceballos S. 2010. Comparison of speed control strategies for maximum power tracking in a wind energy conversion system. Pages 961-966. MELECON 2010 - 2010 15th IEEE Mediterranean Electrotechnical Conference.

8.4. Future Research

- <u>Improving the control loop used in the HPWM.</u>

An interesting contribution related to the HPWM is the tracking method and the control loop. Thanks to those, the maximum amplitude of the low-frequency NP voltage oscillations are controlled and limited. However, the present control loop provides a slow voltage balancing dynamic. Consequently, the DSPWM is fully applied because the HPWM is not able to keep the oscillations within the defined values. This leads to an increase in the switching losses of the power devices. In order to improve the performance of the converter, this control loop could be improved upon by using a predictive controller.

- <u>Limits of the NP voltage balance control in a back-to-back configuration.</u>

When connecting two NPC converters back-to-back, the two converters can contribute to NP voltage balance. However, under some operating conditions, the low-frequency NP voltage ripple may still be too large. In those cases, the use of the DSPWM will avoid the unbalancing problem but will produce too many switching losses. The HPWM provides a compromise solution for limiting the NP voltage amplitudes. Future study will be focused not only on how the HPWM is applied to a specific converter, but it will also consider the whole system, i.e. the two back-to-back-connected converters. Therefore, different modulation strategies may be considered for each converter, depending on the operating conditions.

- <u>Improving maximum power tracking in a wind energy conversion system using a nonlinear controller</u>.

In Chapter 7, some linear control tuning strategies for the PI's controllers have been shown and compared. However, the aerodynamics of the blades are highly nonlinear; hence, the use of a nonlinear controller will improve the performance of the WECS. For this reason the immediate future research will focus on nonlinear controllers such as fuzzy or sliding techniques.

Currently, a basic fuzzy controller which obtains good dynamic performance has already been implemented. This fuzzy controller replaces the standard PI used in the speed loop.

This preliminary work has already been published, but it can be further analyzed and improved upon. Although this study has not been included in the previous chapters, some simulation results are shown in the following.

<u>Reference publication</u>:

Zaragoza J, Staines CS, Arias A, Pou J, Robles E, Ceballos S. 2010. Comparison of speed control strategies for maximum power tracking in a wind energy conversion system. Pages 961-966. MELECON 2010 - 2010 15th IEEE Mediterranean Electrotechnical Conference.

Fig.8.2 and Fig.8.3 show the variation of the performance coefficient (C_p), the optimal and real rotor speeds (ω^*_r and ω_r, respectively), and the mechanical torque (T_m), for a PI-based control and a fuzzy control, respectively. In Fig.8.2, a high torque disturbance has been added to the mechanical torque. This disturbance produces a high overshoot in speed and a decrease in the C_p coefficient. Furthermore, this coefficient also decreases due to rotational turbulences. Unlike in Fig.8.2, these unwanted responses are not observed in Fig.8.3, where the fuzzy controller is operating.

As expected, the fuzzy controller operates better under varying wind conditions. Moreover, the results show that the fuzzy controller achieves better transient responses during both large and small disturbances.

The results show that the proposed control structure based on two PI regulators and a fuzzy controller provides an optimal control solution for PMSG wind turbines. However, further improvements can be made on the fuzzy controller design. In addition, some experimental results could be obtained from an actual low-power wind turbine system.

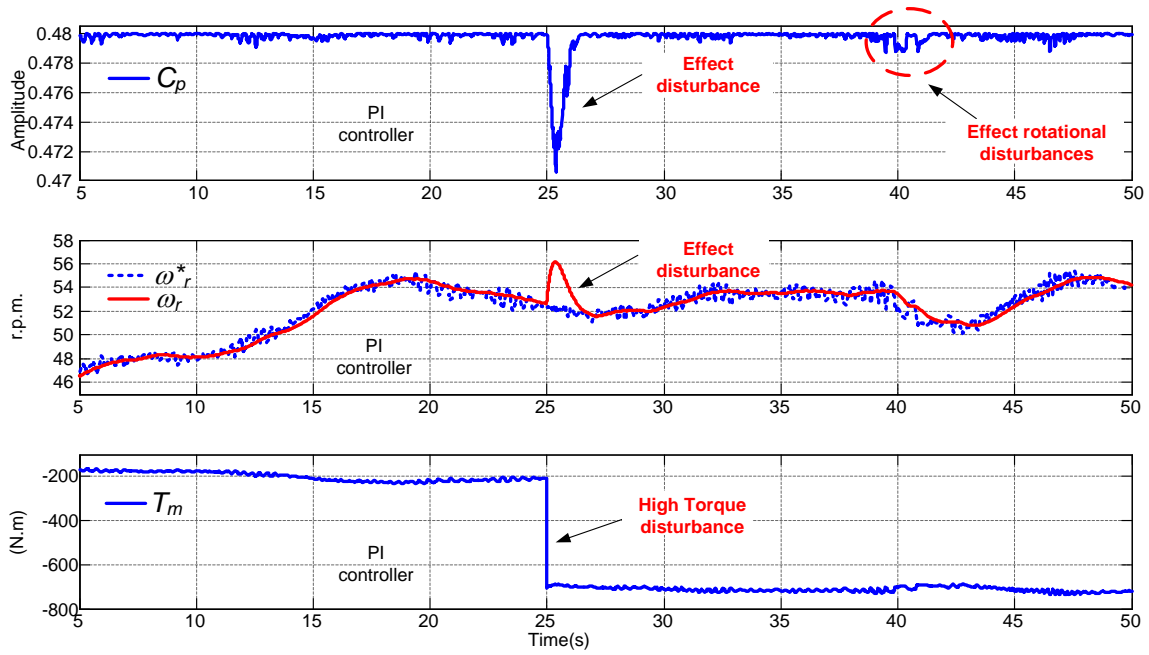Fig.8.2. PI controller performance. (a) power coefficient, C_p; (b) rotor speed, ω_r; and (c) mechanical torque, T_m.
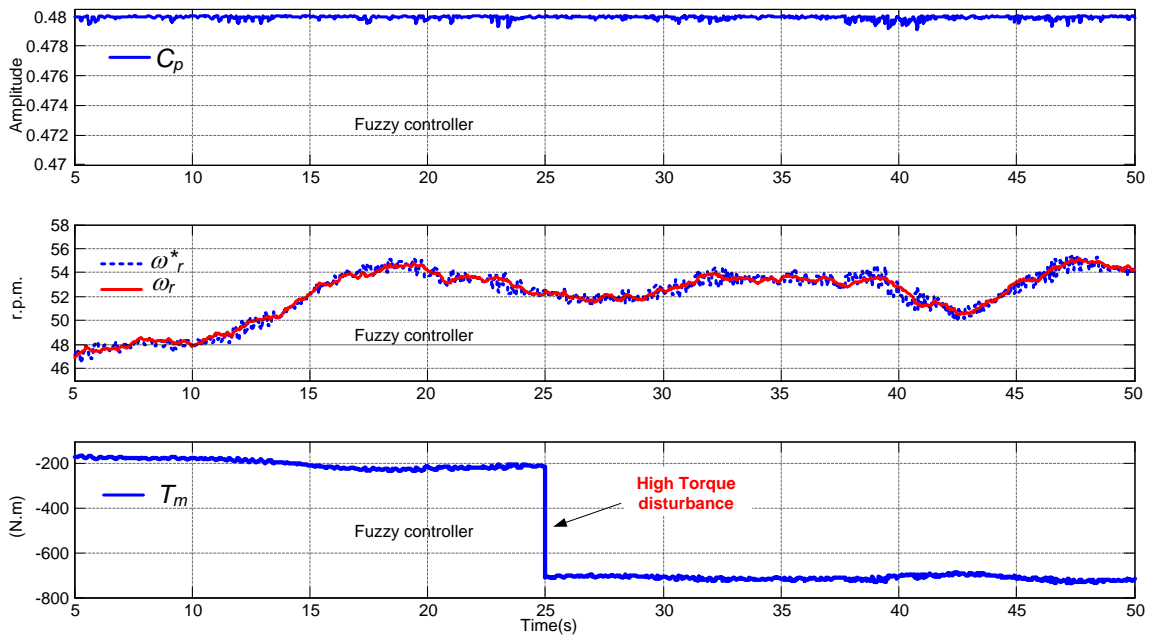
Fig.8.3. Fuzzy controller performance. (a) power coefficient, C_p; (b) rotor speed, ω_r; and (c) mechanical torque, T_m.

Appendices

Appendices A, B, C, D, E and F

These appendices describe and show the models, equations and parameters used in this thesis that have not been included in the chapters and that are considered complementary information. The contents are the following:

-   Appendix A. Switching states in an NPC converter.

-   Appendix B. Switched model of an NPC converter.

-   Appendix C. Power losses calculation.

-   Appendix D. Harmonic distortion calculation.

-   Appendix E. Normalized voltage amplitudes on the NP of an NPC converter.

-   Appendix F. Parameters of the PMSG and the controllers.

Appendix A

A.1. Switch Status in an NPC Converter

In order to be able to generate three voltage levels at the output of an NPC converter, two voltage sources are needed. In practice, the converter will have a single dc bus with two series-connected capacitors that provide a third voltage level, i.e. the NP voltage.

Fig.A.1 shows a leg of an NPC converter. It is assumed that the capacitors share the dc-bus voltage evenly ($v_{C1}=v_{C2}=V_{dc}/2$). The control signal of each IGBT can take two states, $s_{ai}=\{0,1\}$ for $i=\{1,2,3,4\}$; therefore, considering the four IGBTs of the leg, there are $2^4 = 16$ possible combinations. At most, three output voltage levels can be obtained ($V_{dc}/2$, -$V_{dc}/2$ and 0).
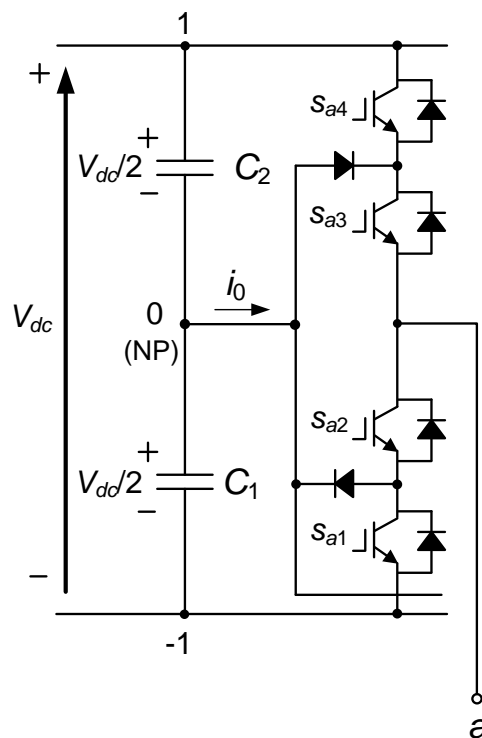

Fig.A.1. An NPC converter leg.

Indeed, only six possible states are allowed. The other states produce short-circuits, or one IGBT has to stand the whole dc-bus voltage. Fig.A.2 shows the feasible states.

Three main states define the levels $V_{dc}/2$, $-V_{dc}/2$ and 0. Fig.A.2(a) Fig.A.2(b) and Fig.A.2(c) show these states, respectively.

The other three valid states for the leg produce undefined output voltages that depend on the output current direction. Fig.A.2(d), Fig.A.2(e) and Fig.A.2 show those states.

Table A1 shows the possible states of the switches.

Table A1.Possible states of the switches.

State	S_4	S_3	S_2	S_1	V_{a0}
1	0	0	0	0	$-V_{dc}/2$ o $V_{dc}/2$
2	0	0	0	1	$-V_{dc}/2$ o $V_{dc}/2$
3	0	0	1	0	$-V_{dc}/2$ o $V_{dc}/2$
4	0	0	1	1	$-V_{dc}/2$
5	0	1	0	0	0 o $V_{dc}/2$
6	0	1	0	1	$-V_{dc}/2$ o $V_{dc}/2$
7	0	1	1	0	0
8	0	1	1	1	Short-circuit C_1
9	1	0	0	0	$-V_{dc}/2$ o $V_{dc}/2$
10	1	0	0	1	$-V_{dc}/2$ o $V_{dc}/2$
11	1	0	1	0	$-V_{dc}/2$ o $V_{dc}/2$
12	1	0	1	1	$-V_{dc}/2$
13	1	1	0	0	$V_{dc}/2$
14	1	1	0	1	$V_{dc}/2$
15	1	1	1	0	Short-circuit C_2
16	1	1	1	1	Short-circuit dc bus

Fig.A.3 shows a summary of feasible sates. Fig.A.4 shows the feasible sates and transitions.

(a) (b) (c)

(d)

(e)

(f)
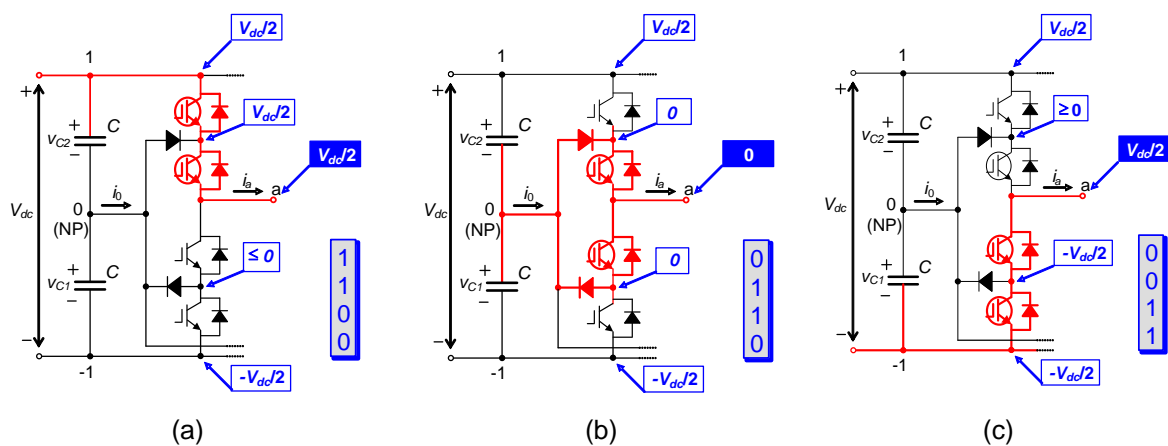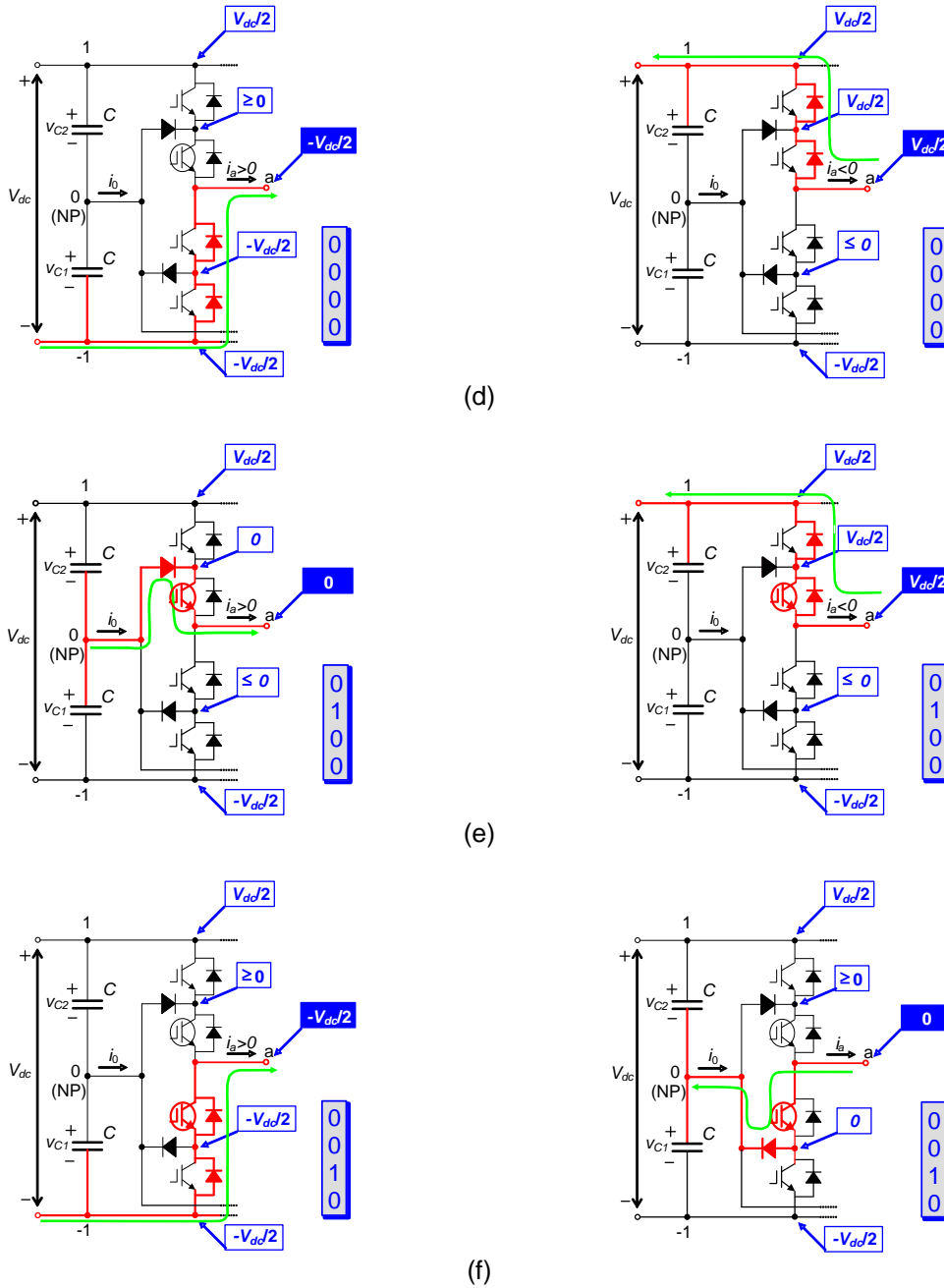
Fig.A.2. Switching states of the IGBTs: (a) high level, (b) middle level, (c) low level, (e) stopped level and (f) available for transitions levels.

Fig.A.5 shows the turning-off and turning-on sequences. Notice, that in all the cases, one switch has to be turned <u>off</u> and then the following one should be activated. It is a standard dead-time time. Furthermore, the transitions from the higher output voltage level to the lower one and vice versa have to go through the neutral-point connection.

Fig.A.3. Summary of feasible states.

Fig.A.4. Feasible states and transitions.
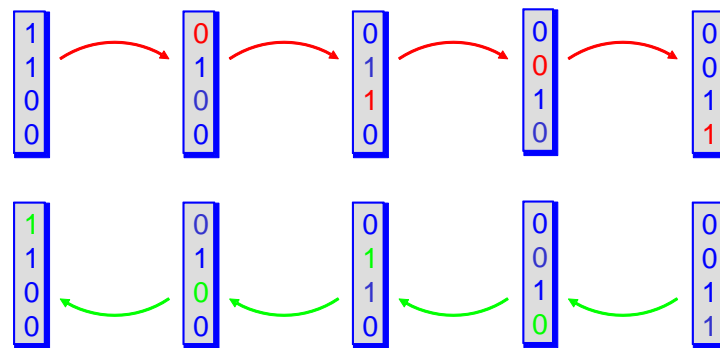
Fig.A.5. Sequence in both directions.

Appendix B

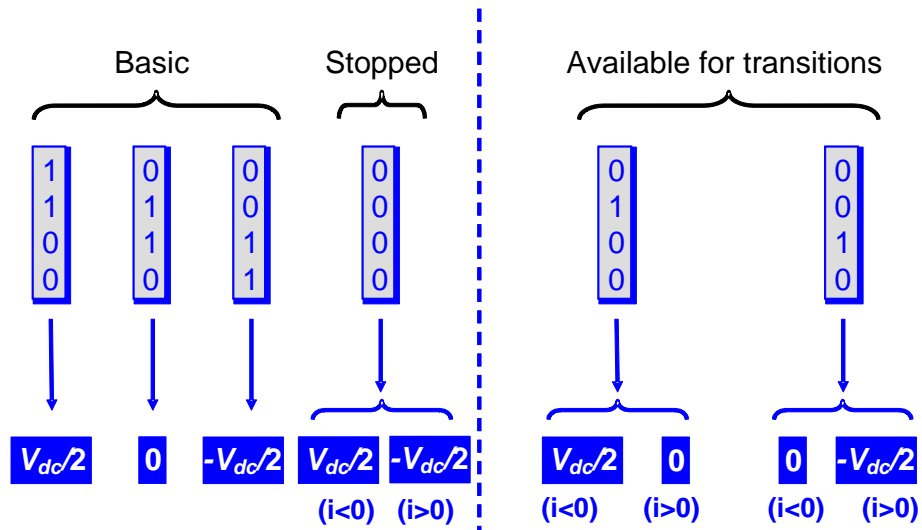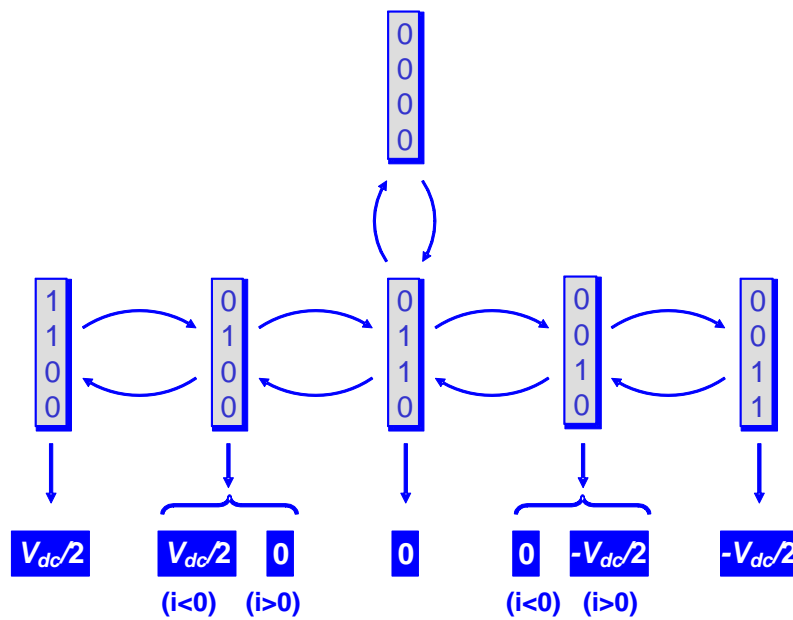## B.1. Switching Model of an NPC Converter

The equations of the switching model of an NPC converter are presented in this appendix. The model was used in this thesis to obtain simulation results from the converter. The model considers ideal switches; i.e. no voltage drops in the on state (R_{ON}=0, V_{F0}=0), open circuit in the off state (R_{OFF}=∞), and all the commutation times are assumed to be worthless.

Fig.B.1 shows the diagram of the multilevel system to be modeled. Conventional signs of voltages and currents are also indicated.

Fig.B.1.Grid-connected NPC converter.

The output voltages in Fig.B.1 referring to the middle dc-link potential ("0") can be expressed as:

$$v_{a0} = L\frac{di_a}{dt} + Ri_a + e_a + v_{N0},$$

$$v_{b0} = L\frac{di_b}{dt} + Ri_b + e_b + v_{N0}, \quad and \tag{B.1}$$

$$v_{c0} = L\frac{di_c}{dt} + Ri_c + e_c + v_{N0}.$$

Summing up the three equations in B.1, the following equation is obtained:

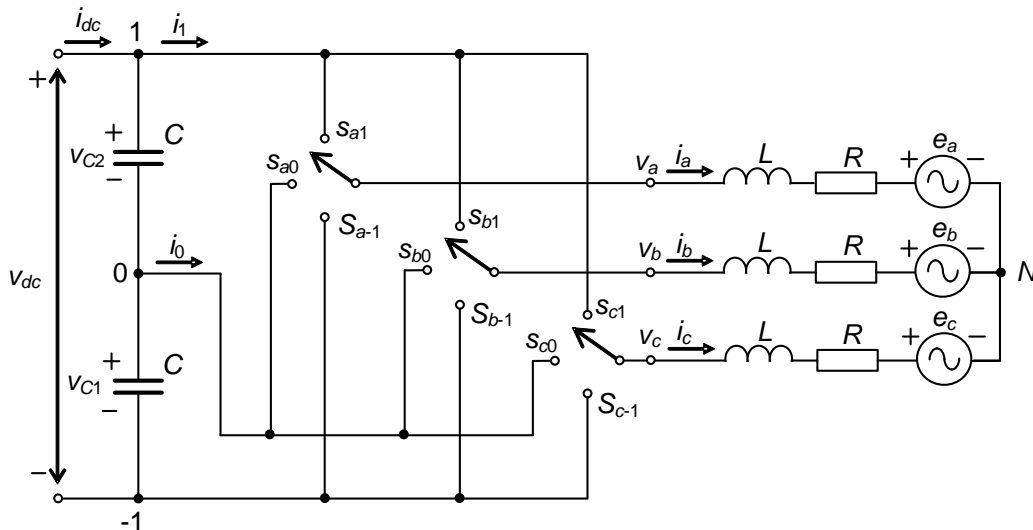$$v_{a0} + v_{b0} + v_{c0} = L\frac{d\left(i_a + i_b + i_c\right)}{dt} + R\left(i_a + i_b + i_c\right) + e_a + e_b + e_c + 3v_{N0}, \qquad \text{(B.2)}$$

where, assuming that there is no zero-sequence current (e.i., $i_a + i_b + i_c = 0$):

$$v_{N0} = \frac{v_{a0} + v_{b0} + v_{c0} - \left(e_a + e_b + e_c\right)}{3}. \qquad \text{(B.3)}$$

The dc-link voltage dynamics are modeled by:

$$\frac{dv_{C2}}{dt} = \frac{i_{dc} - i_1}{C}, \quad and$$
$$\frac{dv_{C1}}{dt} = \frac{i_{dc} - i_1 - i_0}{C}. \qquad \text{(B.4)}$$

In order to include the switching functions of the transistors, (B.4) can be represented by:

$$v_{a0} = S_{a1}\,v_{C2} - S_{a-1}\,v_{C1},$$
$$v_{b0} = S_{b1}\,v_{C2} - S_{b-1}\,v_{C1}, \quad and \qquad \text{(B.5)}$$
$$v_{c0} = S_{c1}\,v_{C2} - S_{c-1}\,v_{C1}.$$

$$i_1 = S_{a1}\,i_a + S_{b1}\,i_b + S_{c1}\,i_c, \quad and \qquad \text{(B.6)}$$
$$i_0 = S_{a0}\,i_a + S_{b0}\,i_b + S_{c0}\,i_c.$$

Appendix C

C.1. Power Losses

There are four types of losses in power electronic converters:

- Conduction losses

- Switching losses

- Snubber losses

- Off-state losses

The last category is usually omitted, as these losses are insignificant. Snubber losses can be important in some kinds of power devices, such as gate turn-off (GTO) thyristors. However, snubbers are not usually required in converters made for other devices, such as IGBTs. Thus, only conduction and switching losses will be considered in this work.

New high-power devices can switch faster. Since switching losses are directly related to the switching frequency, these losses are usually greatest in PWM power converters.

A Matlab-Simulink model of an NPC converter has been developed in this thesis to calculate power losses. The following simulation conditions are assumed when estimating and comparing power losses: the converter rated power is 2.8 MVA (1,700 V / 950 A, V_{dc}=2,400 V), the ac output currents are constant at their rated values, and the sampling frequency is f_s=5 kHz (carriers' frequency).

The IGBTs selected are the DIM1200NSM17-E000, whose maximum ratings are a forward current of 1,200 A and a direct voltage of 1,700 V. In the following analysis, the model of the IGBTs is based on the typical curves given by the manufacturer. Table C1 and Table C2 show the main parameters used to calculate the conduction and switching losses of these IGBTs.

A. Conduction Losses

The conduction losses of the transistors are obtained from linearization of the static characteristics of the power switches. The model of the switches in the on-state is represented by a voltage source and a series resistor. Consequently, the mean value of the conduction losses in a power device can be approximated by the following equation:

$$P_{cl} = \frac{1}{T} \int_0^T (V_{F0} + R_{on}\, i_F)\, i_F\, dt, \tag{C1}$$

in which V_{F0} is the threshold voltage, R_{on} the dynamic resistance of the model, i_F is the forward current in the device, and T is the period of the fundamental frequency. The specific values used for V_{F0} and R_{on} are given in Table C1.

The values were obtained drawing a straight line tangent to the characteristic curves of the device while taking into account the current magnitude in a 2.8-MW converter. The resistance R_{on} corresponds to the inverse slope of this line and V_{F0} to the voltage for which $i_F=0$ in this linearized model.

Table C1. Parameters of the IGBTs for calculating conduction losses.

		Transistor	Diode
Conduction Losses	Drop-on voltage, V_{F0} (V)	0.8	1
	Dynamic on resistor, R_{on} (Ω)	0.001	0.0007

B. Switching Losses

These losses are generated during the turn-on and turn-off switching processes of the power devices. In such processes, the voltages and currents can take significant values simultaneously. Therefore, their product (instantaneous power) can reach high values. Fortunately, these processes only last for short periods, although they are repeated several times within a second. For this reason, they are directly related to the switching frequency.

In this thesis, switching losses are calculated using the characteristics of the energy losses from the data sheet of the power devices. These curves are approximated by a second order equation, given in Table C2. The specific range of current values in this application was taken into account in the approximation.

The expression used to calculate the mean value of the switching losses is:

$$P_{sl} = \frac{1}{n}\sum_{j=1}^{n}\left[E_{on_j}\left(i_F, v_{offs}\right) + E_{off_j}\left(i_F, v_{offs}\right)\right], \tag{C2}$$

where *n* is the number of transitions in an output voltage period (*T*), and E_{on} and E_{off} are the energy dissipated during the turn-on and turn-off processes, respectively. These values depend on the voltage in the off-state (v_{offs}) and the current in the on-state (i_F) through the power devices. The curves provided in the data sheets usually show energy versus current for a specific constant voltage. The dependence of energy on voltage is assumed to be proportional (Table C2).

Table C2. Parameters of the IGBTs for calculating switching losses.

		Transistor	**Diode**
Switching Losses	**Turn-on energy, E_{on} (mJ)**	$10^{-6}\left(\dfrac{V_{offs}}{900}\right)\left(-0.0482\,|i_F|^2+390\,|i_F|+71.4286\right)$	0
	Turn-off energy, E_{off} (mJ)	$10^{-6}\left(\dfrac{V_{offs}}{900}\right)\left(0.0253\,|i_F|^2+318.75\,|i_F|+595.2381\right)$	$10^{-6}\left(\dfrac{V_{offs}}{900}\right)\left(-0.2\,|i_F|^2+490.2\,|i_F|+16190.5\right)$

Appendix D

D.1. Harmonic Distortion

The quality of output voltage waveforms are evaluated using two parameters: the total harmonic distortion (THD) and the weighted total harmonic distortion (WTHD), also called distortion factor (DF1). Unlike the THD, the WTHD considers the frequency of the harmonics so that the low-frequency harmonics weigh more. The parameters are defined as follows:

$$THD(\%) = 100\sqrt{\dfrac{\sum\limits_{n=2}^{\infty} V_{n,RMS}^2}{V_{1,RMS}^2}} = 100\sqrt{\left(\dfrac{V_{RMS}}{V_{1,RMS}}\right)^2 - 1} \tag{D1}$$

$$\text{and } WTHD(\%) = 100\sqrt{\dfrac{\sum\limits_{n=2}^{\infty}\left(\dfrac{V_{n,RMS}}{n}\right)^2}{V_{1,RMS}^2}}. \tag{D2}$$

Appendix E

E.1. Normalized NP Voltage Ripple

In order to evaluate the low-frequency NP voltage amplitudes that occur under the specific operating conditions of the NPC converter, the following normalized parameter ($\Delta V_{NPn}/2$) has been used in this thesis:

$$\frac{\Delta V_{NPn}}{2} = \frac{\Delta V_{NP}/2}{I_{RMS}/f\,C}, \tag{E1}$$

in which I_{RMS} is the RMS value of the output currents, f is the output frequency, and C is the value of a single dc-link capacitor. Observe that it is a nondimensional parameter; therefore, the results presented using this parameter have a more general meaning, since they provide more information than when using dimensional variables.

Appendix F

F.1. Parameters of the PMSG and Controllers

The main data of the PMSG are given in Table F1. This Table shows the main values of the PMSG and the total inertia and friction, taking into account the complete drive systems (the PMSG and the dc driving motor).

Table F1 shows the parameters of the speed and current controllers used in the simulations in Chapter 7. These values have also been used in the controller of the DSPACE, despite the fact that the FOC is processed by a discrete-time DSP. The DSPACE platform is able to process continuous controllers since it automatically transforms them into discrete controllers.

Table F1. Parameters of the machine.

Parameter name	Value
P_N (W)	200
ω_N (rpm)	3000
T_m (Nm)	0.63
Rated voltage (V)	200
Pole pairs (ρ)	4
L (mH)	8.45
R_s (Ω)	2.5
[1]J (kg m^2)	2.98E-4
[1]B (kg m^2/s)	8.29E-4

[1]*Taking into account the assembly of the PMSG and the dc motor*

Table F2. Parameters of the controllers.

Current loop PI	Value
[2]k_{i2}	10.525
[2]k_{p2}	10.52
Speed loop PI	**Value**
[2]k_{i1}	36.41E-3
[2]k_{p1}	4E-3
[3]k_{i1}	6.6E-3
[3]k_{p1}	2.376E-3

[2]*IDF tuning strategy*

[3]*ZPC tuning strategy*