



5.8 Diaphragm Uniaxial Optical Accelerometer

Optical accelerometers are based on the BESOI (*Bond and Etch back Silicon On Insulator*) wafers, supplied by *Shin-Etsu* with (100) orientation, 4' diameter and total thickness of $450 \pm 25 \mu\text{m}$. The thickness of the buried silicon oxide layer is $2 \mu\text{m}$ and the upper silicon layer is $15 \mu\text{m}$ thick, with a dispersion of less than $0.5 \mu\text{m}$ in the wafer and less than $1 \mu\text{m}$ between the wafers of the same set. This accurate control on the silicon thickness allows controlling the beam thickness, responsible of the appropriate working range of the accelerometer. Although the price of these wafers is much higher as compared to standard wafers, the buried silicon oxide layer permits defining complex mechanical structures in a relatively simple manner.

First steps on the fabrication head towards aligning the bridge with the future waveguides (table 5.13). With that objective, a thin silicon oxide layer is deposited on the entire wafer and, after the first photolithographic step, it is removed by RIE from the regions where waveguides have to be defined. Remaining silicon oxide acts as a mask during the wet silicon etching, which has been done with TMAH due to the fact that its selectivity against SiO_2 is much higher and, it is CMOS compatible, that is, wafers can still be treated as non-contaminated after this process (This would not be so if KOH was used, since K^+ ions could contaminate furnaces or reactors). Silicon etching has been fixed at a depth of $3.8 \mu\text{m}$. Thus, the diaphragm will be aligned with the center of the waveguide. As can be seen in table 5.13, etching has been done where waveguides should be located, but its initial thickness remains unchanged at the diaphragm zone.

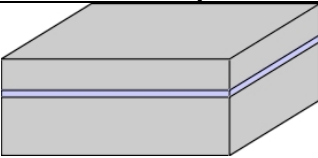
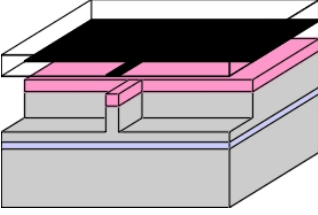
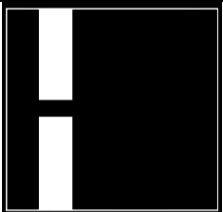
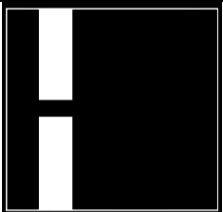
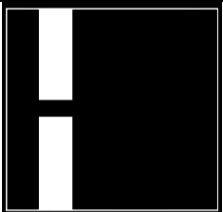
<p style="text-align: center;">First Steps</p> 	<p>BESOI substrate. Double-side polished, 4' diameter, $450 \mu\text{m}$ thick. $2 \mu\text{m}$ buried SiO_2. $15 \mu\text{m}$ upper silicon layer</p>			
	<p>CNM-135 M1 mask: Definition of the diaphragm structure</p> <table border="1" style="width: 100%;"> <tr> <td data-bbox="646 1792 869 2002" rowspan="2">  </td> <td data-bbox="869 1792 1369 1899"> <p>Mask: Width: $290 \mu\text{m}$ Distance: $40 \mu\text{m}$</p> </td> </tr> <tr> <td data-bbox="869 1899 1369 2002"> <p>Step: Positive photoresist $2 \mu\text{m}$ thick Wet TMAH silicon etching: $3.8 \mu\text{m}$</p> </td> </tr> </table>		<p>Mask: Width: $290 \mu\text{m}$ Distance: $40 \mu\text{m}$</p>	<p>Step: Positive photoresist $2 \mu\text{m}$ thick Wet TMAH silicon etching: $3.8 \mu\text{m}$</p>
	<p>Mask: Width: $290 \mu\text{m}$ Distance: $40 \mu\text{m}$</p>			
	<p>Step: Positive photoresist $2 \mu\text{m}$ thick Wet TMAH silicon etching: $3.8 \mu\text{m}$</p>			

Table 5.13: Diaphragm definition on the uniaxial diaphragm optical accelerometer.



Secondly, ARROW-A waveguides are defined following the steps described in section 5.3.1. However, the thermal silicon oxide causes excessive mechanical stresses on the back of the wafer and it is completely removed from this side. Afterwards a new thin silicon oxide layer of $0.1\mu\text{m}$ is grown. It will be the mask during the anisotropic etch (table 5.14). This small oxidation does not cause significant changes on the components side of the wafer due to the fact that there still are $2\mu\text{m}$ silicon oxide and the growth in a furnace is not linear, but has a logarithmic behavior. The silicon nitride that acts as the 1st cladding in an ARROW-A waveguide is also used as a mask for the KOH etching. However, in order to reduce mechanical stresses on the back, it has been Boron-implanted. After the deposition of the core, a $3.5\mu\text{m}$ RIE etching is performed in order to define the rib ARROW structure, obtaining input and output waveguides of 14 and $50\mu\text{m}$, respectively. Finally, $2\mu\text{m}$ PECVD silicon oxide is deposited for passivation

ARROW-A waveguides			
	2nd cladding: $2\mu\text{m}$ wet thermal silicon dioxide. $n=1.46$ Removed from back by wet etching. $0.1\mu\text{m}$ re-growth		
	1st cladding: $0.38\mu\text{m}$ LPCVD silicon nitride. $n=2.00$ Boron implantation at the back.		
	Core: $4\mu\text{m}$ PECVD silicon oxide. $n=1.48$		
	CNM-135 M2: Rib definition		
	<table border="1"> <tr> <td rowspan="2"> </td> <td> Mask: Width: $14/50\mu\text{m}$ Distance: $40\mu\text{m}$ </td> </tr> <tr> <td> Step: Positive photoresist. $2\mu\text{m}$ thick $3.5\mu\text{m}$ SiO_2 RIE etching with CHF_3 </td> </tr> </table>		Mask: Width: $14/50\mu\text{m}$ Distance: $40\mu\text{m}$
	Mask: Width: $14/50\mu\text{m}$ Distance: $40\mu\text{m}$		
	Step: Positive photoresist. $2\mu\text{m}$ thick $3.5\mu\text{m}$ SiO_2 RIE etching with CHF_3		
	Wafer after rib definition		
	Passivation: $2\mu\text{m}$ PECVD silicon oxide. $n=1.46$		

Table 5.14: Wafer status during the waveguide fabrication steps.



The following steps, shown in table 5.15, is the complete removal of all the ARROW layers except in the zone where the rib has been defined. Concretely, the third mask has been designed so as to leave the ARROW structure only at 100µm in distance from the rib. This has been done for preventing the accelerometer from suffering the so-called bimetal effect, that is, bending of the structures due to the different expansion coefficient of two or more adjacent layers. Thus, it is essential to remove all silicon oxide and silicon nitride in the region where the mechanical structure has to be defined.

Layer thicknesses to be etched are significantly thick. This force using a material able to stand such a long etching time: first attempts with thick photoresist did not provide with satisfactory results and it was decided to use aluminium as mask. The main advantage of this material is the capability of this layer to resist the deep etching required. However, deposition of a metal on the wafer causes to be treated as a contaminated wafer, being forbidden to be processed in the CMOS line afterwards.

Unnecessary layer removal			
	<p>CNM-135 M3: Stress-free regions</p> <table border="1" style="width: 100%;"> <tr> <td data-bbox="643 1151 866 1368"> </td> <td data-bbox="866 1151 1370 1368"> <p>Mask: Width: 250µm Distance: 120µm</p> <p>Step: 2µm sputtered aluminium 2µm positive photoresist</p> </td> </tr> </table>		<p>Mask: Width: 250µm Distance: 120µm</p> <p>Step: 2µm sputtered aluminium 2µm positive photoresist</p>
	<p>Mask: Width: 250µm Distance: 120µm</p> <p>Step: 2µm sputtered aluminium 2µm positive photoresist</p>		

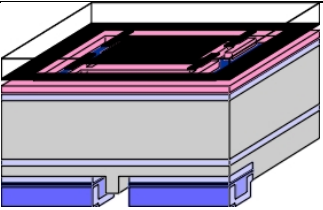
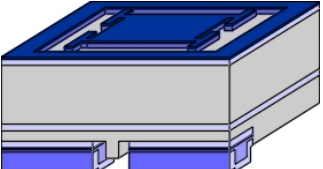
Table 5.15: Removal of unnecessary layers and final appearance of the sensing region where it can be observed the thinner input waveguide (bottom) the zone where the diaphragm will be defined and the output waveguide (top).

Once the optical part has been successfully defined, the next issue is the definition of the mechanical part, that is, the wafer micromechanization. It has been done in two steps, firstly, an anisotropic etching has been produced at the back of the wafer so as to define the three dimensional structure. Once this point has been fulfilled,



a second etching, being in this case RIE etching, has been used in order to free the structure.

Micromechanization starts by the deposition of a photoresist on the back of the wafer and etch by RIE both the silicon nitride and the silicon oxide in order to open the windows where anisotropic etching will be done. However, before doing the etching, the next photolithographic step, this time in the front side, is done (table 5.16). This step has been done at this time because of the fact that after KOH etching wafers are extremely fragile and would not be possible to do any further photolithographic process. Photoresist used at the front side is 6 μm thick because it is needed to cover high steps and stand harsh silicon RIE etching (15 μm). Anisotropic etching is done in KOH. As compared to TMAH, the former has a higher selectivity on etching (100) and (111) planes (which provides with a better accuracy on obtaining the expected geometry) and a minor lateral etching (which allows defining smaller convex corner compensation structures). Moreover, due to the KOH selectivity, either in the (111) and silicon oxide etching speed, the etching is automatically stops at (111) planes and/or when the buried silicon oxide layer is reached.

Micromechanization (back side)	
	<p>CNM-135 M4: Seismic mass</p> <p>Mask: Square 2500x2500μm "T" convex corner compensation. 1200μm</p> <p>Steps: Positive photoresist 2μm thick 0.38μm RIE Si₃N₄ etching with SF₆+He 2μm RIE SiO₂ etching with CHF₃</p>
	<p>Wafer after the etching the protection layers at the back side</p>



	CNM-135 M5: Diaphragm	
		Mask: As defined in chapter 4
Wafer after the silicon anisotropic etching		Thick positive photoresist (6 μm)

Table 5.16: Anisotropic steps that allow defining the three-dimensional structure of the diaphragm optical accelerometer.

For convex corner protection, in chapter 3 it was shown that experimental KOH etching results obtained at CNM required a length of 1300 μm in order to fully protect the corners. During the design of the seismic mass of the accelerometers, corners were 100 μm subcompensated. This was done so as to cause a small rounding at the corners, trying to avoid salient formation at the bottom of the seismic mass (as shown in fig. 5.28) that could cause malfunctions on the correct behavior of the device. However, its removal could be simply done by overetching the wafers, which would not cause significant variations on the device working range.

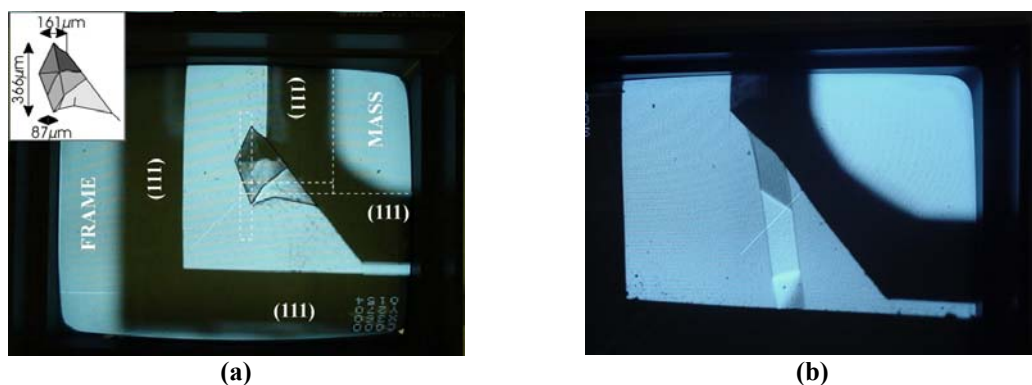


Fig. 5.28: Salient obtained after Convex corner subcompensation etching (a) which has been completely removed after wafer overetching (b).

Layers that still remain in the backside after the steps shown in table 5.16, that is, Si_3N_4 and SiO_2 , are removed, by dry and wet etching, respectively, so as to prepare that side for anodic bonding. Then, the accelerometer micromechanization ends with a RIE etching on the front side.