Universitat Autònoma de Barcelona

A nanoscale study of MOSFETs reliability and Resistive Switching in RRAM devices

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A nanoscale study of MOSFETs reliability and Resistive Switching in RRAM devices

A dissertation submitted by
Qian Wu
in fulfillment of the requirements for the Degree of
Doctor of Philosophy in Electronic and Telecommunication Engineering

Supervised by Dr. **Marc Porti i Pujal**
Bellaterra, November 2016

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Certifies

That the dissertation:

A nanoscale study of MOSFETs reliability and Resistive Switching in RRAM devices

submitted by Qian Wu to the School of Engineering in fulfillment of the requirements for the Degree of Doctor in the Electronic and Telecommunication Engineering Program, has been performed under his supervision.

Dr. Marc Porti
Bellaterra, November of 2016

To my family

Acknowledgement

The four years' doctoral study is a significant and unforgettable experience for me. Many kind-hearted people give me a great amount of help, professional advice and encouragement. Thus, here I would like to express my sincere appreciation to them.

First of all, I would like to show my sincere thanks to my supervisor Dr. Marc Porti who gives me invaluable guidance and constant support throughout the whole PhD period.

Secondly, I express my sincere gratitude to all the members in group Reliability of Electron Device and Circuits (REDEC) with the leadership of Prof. Montserrat Nafria. In particular, I would like to thank Dr. Albin Bayerl who helps me a lot especially at the beginning of doctoral study, patiently training me kinds of experimental skills. I appreciate Dr. Sergi Claramunt for the inspiring discussions and generosity of useful suggestions. I also thank Dr. Mario Lanza for his kindness, advices and help.

Thirdly, my greatest thanks go to the China Scholarship Council (CSC) for the financial support during the doctoral period.

Last but not least, I give the deepest gratitude to my family, especially my brother Dr. Jun Wan. Without their encouragement, support and love, I would not persist in neither the study of PhD, nor the completion of this thesis.

Contents

Publications related to this thesis

Compendium of publications included in this thesis

1) Q. Wu, A. Bayerl, M. Porti, J. Martin-Martinez, M. Lanza, R. Rodriguez, V. Velayudhan, M. Nafria, X. Aymerich, M.B. Gonzalez, and E. Simoen, "A Conductive AFM Nanoscale Analysis of NBTI and Channel Hot-carriers Degradation in MOSFETs," IEEE Transactions on Electron Devices, vol. 61, pp. 3118-3124, 2014.

2) Q. Wu, M. Porti, A. Bayerl, J. Martin-Martinez, R. Rodriguez, M. Nafria, X. Aymerich, and E. Simoen, "Channel Hot-carriers Degradation of Strained MOSFETs: A Device Level and Nanoscale Combined Approach," Journal of Vacuum Science & Technology B, vol. 33, pp. 022202, 2015.

3) Q. Wu, S. Claramunt, M. Porti, M. Nafria and X. Aymerich, "Evaluation of ultra-thin structures composed of graphene and high-k dielectrics for resistive switching memory applications," International Journal of Nanotechnology, vol. 13, pp. 634-641, 2016.

Annex S. Claramunt, Q. Wu, M. Maestro, M. Porti, M. B. Gonzalez, J. Martin-Martinez, F. Campabadal and M. Nafria, "Non-homogeneous conduction of conductive filaments in Ni/HfO_2/Si resistive switching structures observed with CAFM," Microelectronic Engineering, vol.147, pp.335-338, 2015.

Other publications

- V. Iglesias, Q. Wu, M. Porti, M. Nafria, G. Bersuker, and A. Cordes, "Monitoring defects in III-V materials: A nanoscale CAFM study," Microelectronic Engineering, vol. 147, pp. 31-36, 2015.

- M. Porti, V. Iglesias, Q. Wu, C. Couso, S. Claramunt, M. Nafria, A. Cordes and G. Bersuker, "CAFM experimental considerations and measurement methodology for in-line monitoring and quantitative analysis of III-V materials defects," IEEE Transactions on Nanotechnology, vol. 15, pp. 986-992, 2016.

Contributions to conferences

- Q. Wu, M. Porti, A. Bayerl, J. Martin-Martinez, R. Rodriguez, M. Nafria, X. Aymerich, and E. Simoen, "CHC degradation of strained MOSFETs: a device level and nanoscale combined approach," 18th Workshop on Dielectrics in Microelectronics (WODIM), June 9th-11th, 2014, Kinsale Co Cork, Ireland.

- Q. Wu, M. Porti, A. Bayerl, J. Martin-Martinez, R. Rodriguez, M. Nafria, X. Aymerich, and E. Simoen, "CAFM Study of Negative Bias Temperature Instability and Channel Hot-carriers Degradation in Strained and Non-strained MOSFETs," Trends in Nanotechnology International Conference (TNT2014), October 27th-31st, 2014, Barcelona, Spain.

- Q. Wu, M. Porti, J. Martin-Martinez, R. Rodriguez, M. Nafria, and X. Aymerich, "A Conductive AFM study of NBTI and Channel Hot-carriers degradation in MOSFETs at nanoscale," AFM Beyond Imaging. Nanoscale Characterization of Functional Materials (AFM2015), January 19th, 2015, Barcelona, Spain.

- Q. Wu, M. Porti, A. Bayerl, J. Martin-Martinez, R. Rodriguez, M. Nafria, X. Aymerich, and E. Simoen, "Impact of NBTI and CHC Stress on the Nanoscale Electrical Properties of strained and non-strained MOSFETs," 10th Spanish Conference on Electron Devices (CDE), February 11th-13th, 2015, Aranjuez, Spain.

- S. Claramunt, Q. Wu, M. Porti, N. Mestres, M. Nafria, and X. Aymerich, "Im-

provement of the transfer process of CVD graphene," 3rd edition of the largest European Event in Nanoscience & Nanotechnology (ImagineNano), March 10th-13th, 2015, Bilbao, Spain.

- V. Iglesias, M. Porti, C. Couso, Q. Wu, S. Claramunt, E. Miranda, N. Domingo, M. Nafria, G. Bersuker, and A. Cordes, "Threading Dislocations in III-V Semiconductors: Analysis of Electrical Conduction," 2015 IEEE International Reliability Physics Symposium (IRPS), April 19th-23rd, 2015, Hyatt Regency Monterey, CA, USA.

- V. Iglesias, Q. Wu, M. Porti, M. Nafria, G. Bersuker, and A. Cordes, "Monitoring defects in III-V materials: A nanoscale CAFM study," 19th Conference on Insulating Films on Semiconductors (INFOS), June 29th-July 2nd, 2015, Udine, Italy.

- S. Claramunt, Qian Wu, M. Maestro, M. Porti, M.B. Gonzalez, J. Martin-Martinez, F. Campabadal and M. Nafria, "Non-homogeneous conduction of conductive filaments in Ni/HfO_2/Si resistive switching structures observed with CAFM," 19th Conference on Insulating Films on Semiconductors (INFOS), June 29th-July 2nd, 2015, Udine, Italy.

- Q. Wu, S. Claramunt, M. Porti, M. Nafria and X. Aymerich, "Evaluation of ultra-thin structures composed of graphene and high-k dielectrics for resistive switching memory applications," Trends in Nanotechnology International Conference (TNT2015), September 7th-11th, 2015, Toulouse, France.

- Q. Wu, J. Martin-Martinez, M. Porti, R. Rodriguez, M. Nafria and X. Aymerich, "CAFM analysis of the Temperature Dependence of Random Telegraph Noise in SiON gate dielectrics," 19th Workshop on Dielectrics in Microelectronics (WODIM), June 27th-June 30th, 2016, Catania, Italy.

Presentation

Since the beginning of the new century, people on every continent of this planet not only have witnessed but also have integrated in the unprecedented flourishing of electronics technologies. Firmly followed by Moore's Law, electronic devices with enhanced performance have brought us smartphones, high performance computers, 4G networks, autopilot cars, powerful Artificial Intelligence (AI), Virtual Reality (VR) technologies, electronic payment, non-offline social network, etc., all over the world, which have tremendously changed our lifestyles comparing to some decades ago. However, simultaneously, electronic devices with faster chips, larger memories, less energy consumption, greater reliability, smaller size and higher levels of integration are continuously required. All these great challenges are creating new problems and introducing new topics of study at the same time to the micro- and nanoelectronics industry and academia, leading the research community to face both hardship and opportunities.

In the case of MOSFETs, reliability issues associated to gate stacks are considered to be increasingly important due to the continuous scaling. The persistent increase of the electric fields in nanoscale devices can trigger different aging mechanisms. Therefore, it is necessary to go forward in the understanding of how these mechanisms affect the performance of gate dielectrics in the updated technologies. Channel Hot-Carriers (CHC) degradation, Bias Temperature Instabilities (BTI) and Time-Dependent Dielectric Breakdown (TDDB) have been identified as the most relevant degradation mechanisms in MOSFETs. BTI and CHC aging involve the generation of defects at the gate oxide/Si interface and/or oxide bulk, so that several device parameters (threshold voltage and carrier mobility in the channel) shift during the device operation. Consequently, the circuit performance could be harshly affected. The BTI and CHC aging has been extensively analyzed at device level. However,

details on the spatial distribution of damage after an electrical stress can only be revealed using other high resolution characterization techniques.

Although the Dielectric Breakdown of gate oxides corresponds to the irreversible loss of the dielectric properties and has been treated as an important reliability problem in CMOS technology, it has been demonstrated that the formation of a conductive filament connecting both electrodes in a MIS/MIM structure could be reversible if a sufficient current limit is set when it is triggered. This reversible phenomenon exhibiting two conductivity states is known as Resistive Switching (RS) phenomenon and has powerful applications for memory devices. Recently, Resistive Random Access Memory (RRAM) devices based on RS have emerged due to their scalability, non-volatility and high performance. However, the adequate understanding of the physics of the RS mechanisms is still lack. Moreover, graphene, which has attracted great attention of researchers since 2004, could also be used in devices for RRAM applications. However, the variation of switching parameters during cycling in one device and from device to device, and reliability issues related to graphene based memories still need investigation. Since the physical mechanisms associated to the conductive filaments formation have been found to have a nanometric origin, again, standard techniques are not enough, and high spatial resolution techniques are required to evaluate their properties.

Since 1986, with the invention of the first Atomic Force Microscope (AFM), AFM based techniques have turned into very important tools for nanoscale characterization. Among them, especially when studying the electrical properties and reliability of gate dielectrics, the Conductive Atomic Force Microscope (CAFM) has been the most used until now. This technique is capable to obtain simultaneously and independently topographical and electrical information at the nanoscale, achieving lateral resolutions of less than 10 nm. Taking advantage of the resolution of this technique, the general goal of the research presented in this thesis is to analyze at the nanoscale the impact of degradation mechanisms as NBTI and CHC in MOSFETs and the resistive switching phenomenon in Metal/Insulator/Semiconductor (MIS) and Metal/Graphene/Insulator/Semiconductor (MGIS) structures. For this purpose, CAFM has been the main technique used in this thesis. This manuscript is organized as follows:

Chapter 1 will be devoted to introduce the state of the art and the general concepts

which are necessary for understanding the results presented in this thesis. It will be started with the basic concepts of MOSFET and its scaling. Then, different failure mechanisms affecting the gate stack will be described. RS, graphene properties and how this material could be introduced in graphene-based MIM/MIS devices for memory applications will also be explained. Finally, both, the standard and nanoscale characterization techniques used in this thesis will be briefly introduced.

In Chapter 2, more details about Atomic Force Microscope (AFM) and related techniques will be described. First, basic concepts of AFM will be presented. Then, Conductive Atomic Force Microscope (CAFM) and some improvements introduced to enhance the conductivity measurements will be explained. As the AFM resolution and reliability of the measurements highly depend on the tip properties, several most common AFM probes have been compared and studied.

In Chapter 3, different electrical stresses (NBTI and CHC) were applied to ultra-thin SiON based MOSFETs at device level and their impact on the nanoscale gate oxide properties has been investigated before and after the electrical stress with CAFM. The impact of NBTI and CHC degradation has been studied on both strained and unstrained MOSFETs with different channel lengths. Moreover, leaky sites at different temperatures on as-grown SiON layers have been analyzed with CAFM.

Finally, in Chapter 4, resistive switching phenomenon in MIS structures for RRAM applications has been analyzed at both device level and nanoscale. First, the local properties of conductive filaments in MIS devices left in the HRS and LRS have been studied with CAFM. Then, the variability and electrical properties of MIS devices when an interfacial layer of graphene is intercalated between the top electrode and the gate dielectric have also been investigated at both device level and nanoscale.

Chapter 1

Introduction

In this chapter, the fundamental concepts which are necessary for understanding the rest of the manuscript will be introduced. It will start with the basic concepts of MOSFETs, which are present almost in every electronic set. Afterwards, the downscaling of the electronic devices as well as the challenges related to the continuous shrinking of the devices' dimensions will be introduced. Alternative materials have been one approach to reduce the leakage current through the traditional gate dielectric (SiO_2); however other reliability issues should still be faced. Some of the most important failure mechanisms associated to gate dielectrics of MOSFETs will be presented, such as Dielectric Breakdown (BD), Negative Bias Temperature Instability (NBTI), Channel Hot Carrier (CHC) and Random Telegraph Noise (RTN). Since strain techniques have been as well a useful approach to enhance the carrier mobility of MOSFETs, which have been used in the devices analyzed in Chapter 3; there will be a brief introduction about them. Resistive switching for memory applications and the impact of graphene on RRAM devices will be analyzed in Chapter 4. Therefore, this issue will be also introduced in this chapter. Finally, since all the analyses presented in this thesis have been obtained at device level and mainly, at nanoscale, different characterization techniques will be presented, such as the standard characterization for global electrical properties of MOSFETs and memory devices, and the Conductive Atomic Force Microscope (CAFM) for nanoscale investigations.

1.1 MOSFET and its Scaling

1.1.1 The Basic Concepts of MOSFETs

The metal-oxide-semiconductor field-effect transistor (MOSFET) is one of the most common and important device in the silicon-based integrated circuits. The fundamental part of the MOSFET is the capacitive MOS structure (Fig.1.1a) with the top contact (gate, G) of metal or polysilicon, a thin layer of gate oxide and the bottom electrode made of semiconductor. The dielectric layer traditionally was silicon dioxide. However, it has been replaced by silicon oxynitride (SiON) and high-k dielectric materials to continue device scaling [1] (see Section 1.1.2). The bottom electrode is also referred as bulk, substrate or body and it can be either n-type or a p-type leading to a p-type or an n-type MOSFET, respectively.

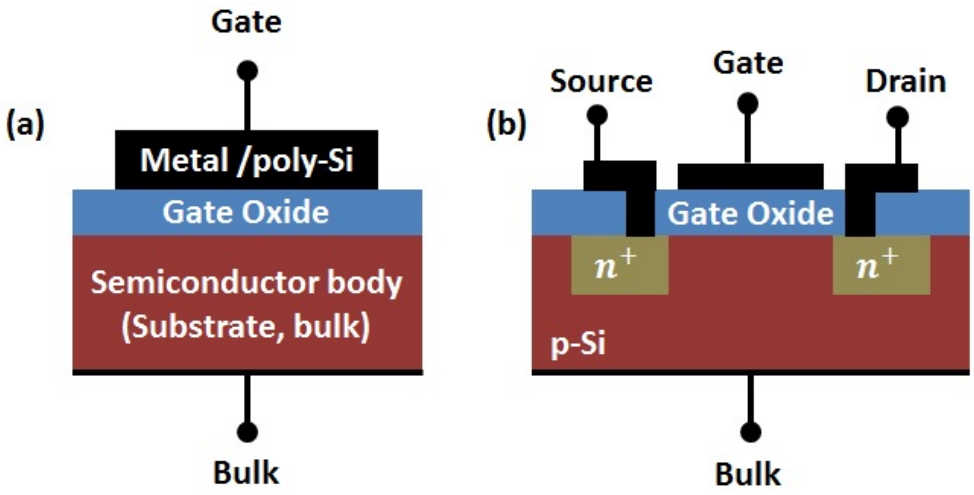


Fig. 1.1. Schematic of a (a) MOS structure and (b) MOSFET with a p-type substrate.

There are three different operation modes of a MOS capacitor, depending on the voltages applied between the gate and bulk. Fig.1.2 shows the energy-band diagrams of an ideal MOS capacitor with a p-type semiconductor at different gate voltages, V_G.

(a) When a negative bias ($V_G < 0$ V) is applied, the Fermi level of metal increases and the semiconductor bands bend upwards at the oxide/semiconductor interface. Consequently, the valence energy, E_V, is closer to Fermi energy, E_F,

at the interface than in the bulk, leading to a higher concentration of holes at or near the surface. This mode is called accumulation (Fig.1.2a).

(b) When a positive bias (V_G > 0 V) is applied to the gate contact, the Fermi level of metal decreases leading to the semiconductor bands bending downwards. Therefore, the hole concentration near the interface decreases and a space charge region of fixed and ionized ions is formed. This mode is called depletion (Fig.1.2b).

(c) When a positive bias ($V_G \gg 0$ V) is applied high enough, the energy band bends down further. The electrons are attracted to the oxide/semiconductor interface forming what is called a channel, which means that such interface behaves like n-type semiconductor. This mode is called inversion (Fig.1.2c). The minimum gate voltage to create the channel is called threshold voltage, V_{th}.

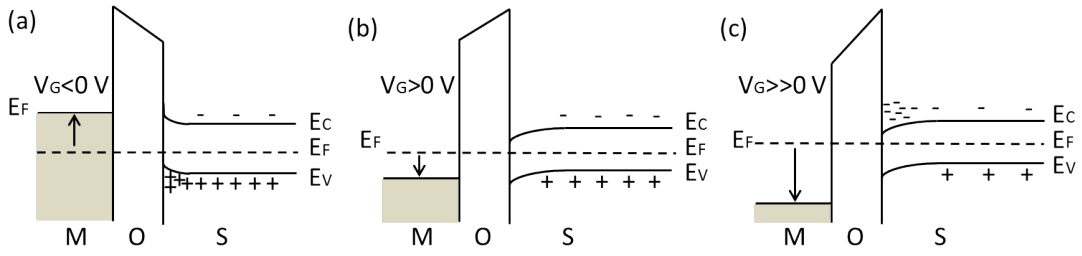


Fig. 1.2. Energy-band diagrams of an ideal MOS capacitor with a p-type semiconductor at different V_G, showing (a) accumulation, (b) depletion and (c) inversion conditions.

It is important to emphasize that we have discussed the ideal MOS structure. In this case, the work function for semiconductor and metal is assumed to be equal, that is, $\phi s = \phi m$, and the capacitance C_{ox} of the MOS capacitor is given by:

$$C_{ox} = \frac{Ak\varepsilon_0}{t_{ox}} \tag{1.1}$$

Here, A is the area of the capacitor, ε_0 represents the permittivity of vacuum, k represents the relative permittivity of the dielectric and t_{ox} is the oxide thickness. For real MOS capacitors, there are undesirable charges within the oxide and at the oxide/semiconductor interface and moreover, ϕs is probably different from ϕm. Therefore, it is necessary to apply a suitable voltage to the gate to achieve the flat-band condition, which is defined as the situation in which there is no internal

potential difference across a MOS structure.

The MOSFET is a four-terminal device (Fig.1.1b) which consists of a MOS structure and two additional contacts (source, S and drain, D). In a MOSFET with a p-type substrate, the source and drain regions are n-type doped and are separated by the body region called channel.

Depending on the voltages applied to the terminals, the operation of a MOSFET can be separated into three different modes: 1) cut-off or weak inversion region, 2) triode mode or linear region, 3) active mode or saturation region [2]:

• If $V_{GS} < V_{th}$, the transistor is turned off since the inversion channel is not created. Ideally, the current between drain and source should be zero even when a V_{DS} is applied. When the transistor is being used as a turned-off switch, there is a weak-inversion current, sometimes called subthreshold leakage. This is known as cut-off or weak inversion region (Fig.1.3).

• If $V_{GS} > V_{th}$, and $V_{DS} < (V_{GS} - V_{th})$, the transistor is turned on, and the voltage exceeding the threshold determines an accumulation of mobile charge on the channel. The current from drain and source, I_{DS}, is modeled as:

$$I_D = \mu C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{1.2}$$

Where μ is the carrier mobility, W is the channel width, L is the channel length and C_{ox} is the gate oxide capacitance per unit area. This is known as ohmic mode or linear mode (Fig.1.3).

• If $V_{GS} > V_{th}$, and $V_{DS} < (V_{GS} - V_{th})$, the channel is pinched off at the drain end, and I_{DS} saturates. That is, I_{DS} becomes, in first approximation, independent of the drain voltage. I_{DS} is modeled as:

$$I_{sat} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \tag{1.3}$$

This is known as saturation mode(Fig.1.3).

Finally, another important parameter that characterizes the small signal response

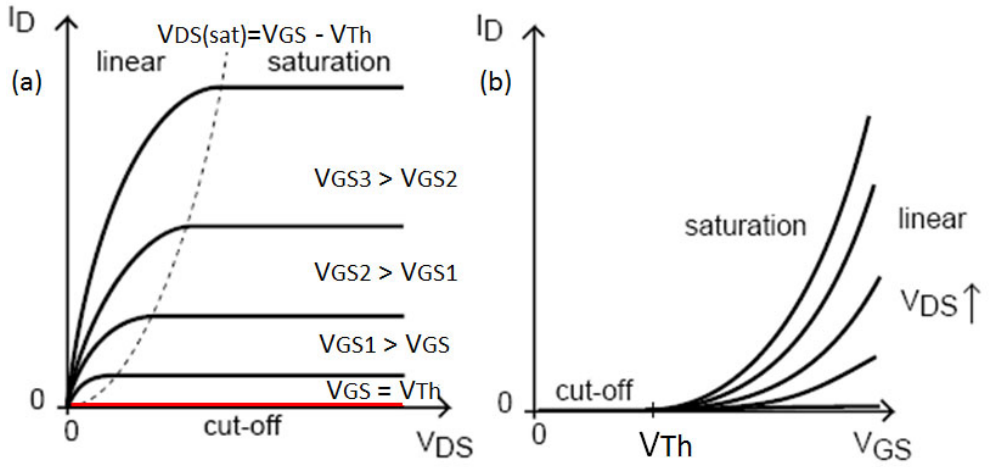


Fig. 1.3. Typical I_D-V_{DS} (a) and I_D-V_{GS} (b) curves of an n-channel MOSFET which illustrate the three operation regions of a transistor.

of the transistor is the transconductance, g_{msat}, defined as:

$$g_{msat} = \frac{\partial I_{Dsat}}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \tag{1.4}$$

Large saturation current and transconductance are required for fast signal response. This can be achieved by increasing the oxide capacitance according to Eq.1.3 and Eq.1.4. However, shrinking dimensions of MOSFETs will cause other problems which affect the operating performance. How to improve operating performance while transistors have been shrinking will be discussed in following sections.

1.1.2 MOSFET Scaling

For the last decades, the microelectronic industry has benefited enormously from the MOSFET scaling which is required to increase integration density and speed, as well as storage capacitive for memories. The number of transistors integrated in a single chip has followed an exponential increase which is known as Moore's law (Fig.1.4). The simplest scaling concept of MOSFET is constant-field scaling which was presented by Dennard et al. at International Electron Device Meeting (IEDM), 1972 [3]. The basic principle is to scale the device voltages and dimensions (both in horizontal and vertical direction) by the same factor, k (k>1), while

increasing the substrate doping concentration to keep the electrical field in the device constant. However, highly doped channel results in carrier mobility degradation and short channel effect (SCE) [4]. Moreover, as device dimensions enter into the sub-micron dimensions, two-dimensional effects (such as drain induced barrier lowering (DIBL) [5, 6]) become increasingly important, which require the redefinition of scaling rules. During the 80's, a new strategy was born: the generalized scaled theory [7]. The main advantage of this approach is that the parameters do not all have to be scaled by one factor. The generalized scaling allows electric field to scale up by α while the device dimensions scale down by k. But the main problem associated with these scaling rules is related to an increment of the power density.

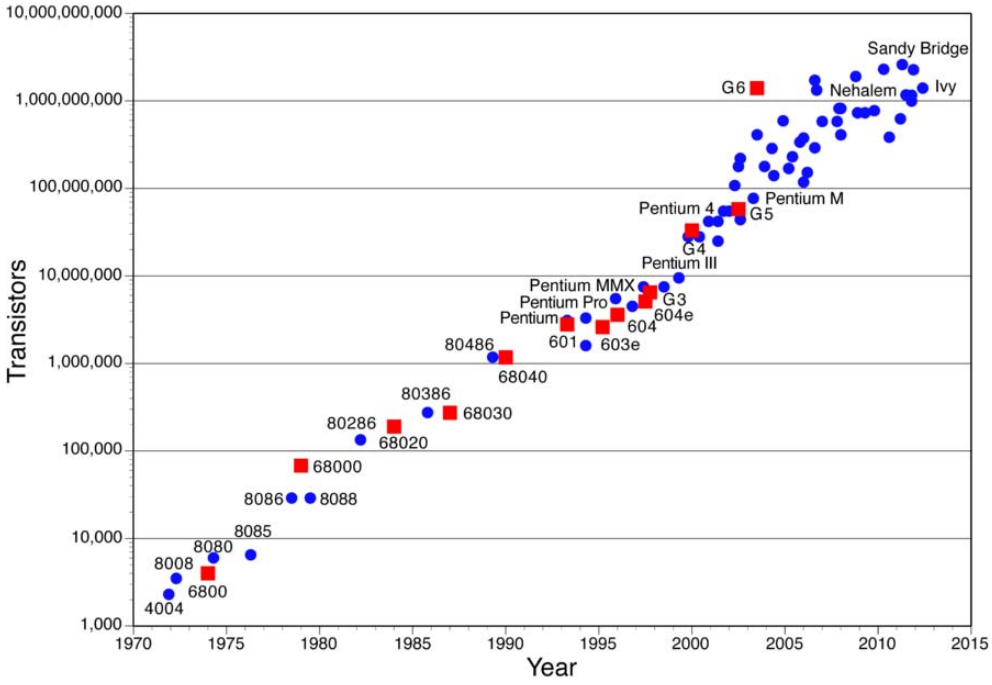


Fig. 1.4. Moore's law which shows the number of transistors against years of introduction [8].

Numerous attempts have been done to solve these problems. From 1998, the International Technology Roadmap for Semiconductors (ITRS) has been outlined possible solutions for the challenges that microelectronic industry must face, and highlighted the specific areas that need urgent research. Some of the solutions to overcome the problems associated to the continuous scaling down were to prompt a replacement to conventional MOSFETs, for example, use alternative gate dielectrics to suppress gate leakage [9–11]. The alternative can be introduction of

nitride into the SiO_2 or other dielectric materials which have a higher dielectric permittivity [12–14]. However, the leakage from the source to drain (punch-through) was still a challenge in short devices. A direct method to eliminate the punch-through was to use depleted-substrate devices, realized as ultra-thin body Silicon on Insulator (SOI) devices [15]. In the 90nm technology node and beyond, strain engineering was widely accepted as a promising technique to improve CMOS performance [16–18]. Intel firstly fabricated chips with strain engineering in early 2003 [19]. The carrier mobility in these transistors was enhanced meanwhile the power consumption was reduced. Moreover, semiconductors with high mobility, such as Ge and III-V materials have also been studied to improve the device performance [20]. Some of these issues will be discussed in details in the next sections of this chapter.

Paying attention to the gate stack of the transistors, the scaling down of the MOSFET affects the vertical dimension as the gate oxide thickness, t_{ox}, which has also been scaled down. However, continuous thinning down of the thickness of the gate oxide raises severe problems, being the two most important:

- *Gate leakage*: As the downscaling of the oxide thickness, the gate leakage current increases exponentially due to quantum tunneling effects [21, 22]. According to the tunneling theory [23], an important parameter that determines the magnitude of the tunneling probability is the width of the potential barrier. In MOSFETs, the element that plays the role of a potential barrier is the gate dielectric. Therefore, when the oxide thickness decreases, the width of the energy barrier is reduced facilitating electrons tunneling through the insulator layer [24–26]: tunneling current increases more and more becoming the dominant source of device leakage. Examples of experimental and simulated leakage currents are shown versus the gate voltage for various oxide thicknesses in Fig.1.5. As an example, through SiO_2 layers, the leakage current at 1.5 nm reaches 10 A/cm^2 at a gate voltage of 1 V, while it is 1x10^{-12} A/cm^2 at 3.5 nm thick dielectric layers.

- *Reliability*: The reliability of SiO_2 layers (and other materials) has been extensively studied over years and it becomes even more critical as the gate oxide thickness continues shrinking. In general, the reliability can be associated with the capability to maintain the insulator properties as long as possible,

providing a correct operation in devices. Therefore, the loss of reliability can be understood as an increment of probability that the failure happens in a shorter time than usual. This issue will be further studied in Section 1.3.

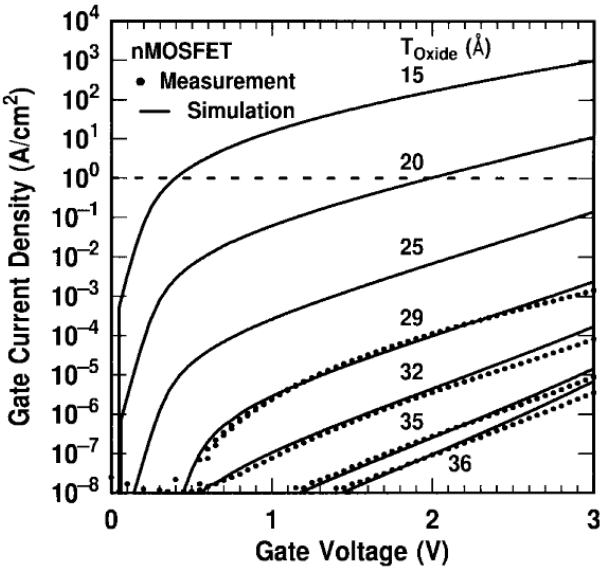


Fig. 1.5. Experimental (dot lines) and simulated (solid lines) gate leakage current versus gate voltage for different oxide thickness [27].

1.2 Alternative Gate Dielectrics

As mentioned before, numerous attempts have been used to improve the oxide quality and reduce the gate leakage. Several successful approaches used in advanced CMOS technology were the introduction of nitride into the SiO_2, leading to the formation of silicon oxynitrides (SiO_xN_y) [12, 13, 28]. Since nitrogen slows down the thermal growth rate, improves the interface uniformity, and offers protection against boron and other impurity penetration through the gate dielectric, the thickness of gate dielectrics can be reduced below 2nm. Furthermore, oxynitrides enhance reliability characteristics and make the oxide less sensitive to hot electrons which may create defects in the dielectrics and induce degradation.

To obtain the same capacitance in a MOSFET (see Eq. 1.1), the use of alternative dielectric materials with higher dielectric constant would allows the fabrication of devices with a thicker gate dielectric than those based on SiO_2. This reduces

leakage current significantly. In this case, the alternative gate dielectrics would be converted to the SiO_2 Equivalent Oxide Thickness (EOT) by the relationship:

$$EOT_{film} = \frac{k_{SiO_2}}{k_{film}} t_{film} \tag{1.5}$$

Here, K_{SiO_2} represents the permittivity of SiO_2 (3.9), K_{film} and t_{film} represents the permittivity and thickness of alternative gate dielectrics. Depending on the concentration of N, silicon oxynitrides may have a larger dielectric constant. However, too much nitrogen near the silicon interface may reduce the carrier mobilitydegrade device performance. Thus, other alternative materials with high dielectric constant, so called high-k materials such as Ta_2O_5 [29], TiO_2 [30], $SrTiO_3$ [31] began to be investigated.

Unfortunately, the replacement of SiO_2 by high-k dielectrics was not straightforward. These materials should fulfill requirements in order to be compatible with the well-known silicon technology and to meet the specific properties required for ultra-short channel MOSFET devices [32, 33]. Several important requirements are as following:

- *Thermodynamic stability*: Oxygen diffusion may cause an uncontrolled interfacial layer in contact with silicon, leading to an increment of EOT. Furthermore, other most likely reactions are the formation of metal oxides and silisides, leading to stack degradation.

- *High band gap*: The dielectric should have a sufficiently high band gap in order to achieve the acceptable low leakage.

- *Low defects density*: Low density of intrinsic defects at the Si/dielectric interface and in the bulk is also required in order not to reduce the carrier mobility.

- *Gate compatibility*: A depletion region at the interface with the traditional polysilicon gate electrode has been observed [9], which can be reduced by a metallic gate.

- *Process compatibility*: The deposition process for the dielectric must be compatible with current or expected CMOS processing, cost and speed. Possible deposition methods are: sputter deposition, Chemical Vapor Deposition

(CVD), Atomic Layer Deposition (ALD), and Molecular Beam Epitaxy (MBE). However, MBE has poor throughput, expensive cost and requires enormous maintenance, sputter deposition is not easy to meet the uniformity target, so CVD and ALD has shown to be attractive deposition technique.

Even though none of alternative materials have been found to fulfill all these requirements, HfO_2 has turned out to be the most promising candidate for replacing SiO_2 [34–36]. A Hf-based Dielectric was integrated in products of the 45 nm technology node by chipmaker Intel at 2007 [37]. Other companies such as AMD/Global Foundries and Samsung followed in 2010 with the introduction of Hf-based dielectrics in products of the 32 nm technology generation [38]. Later in 2012, a 22 nm generation logic technology was proposed for high performance CPU products [39] and Intel developed a true 14 nm technology with industry-leading performance, power, density and cost per transistor in 2014 [40] with high-k based gate dielectrics. However, despite all the technological advances described in this section, there are still variability and reliability issues that must be faced. In next section, those related to the gate stack will be considered.

1.3 Reliability Concerns: Failure Mechanisms in Oxides

As explained in Section 1.2, although alternative dielectrics can reduce the gate leakage, these materials also suffer reliability issues can affect the functionality of the circuits of which the device is part. Some of them were already known for SiO_2 technology [1]. Moreover, additional failure mechanisms have appeared [41]. The insulating properties of the gate oxide can be affected not only by the individual defects in as-grown dielectrics, but also by the failure mechanisms associated to an electrical stress. Therefore, it is necessary to go forward to the understanding of these mechanisms. This section will be dedicated to review some of the most and common important failure mechanisms [Dielectric breakdown (BD), the Negative Bias Temperature Instability (NBTI), Channel Hot Carriers (CHC) and Random Telegraph Noise (RTN)] since they have been analyzed in the rest of chapters and form the main part of this thesis.

1.3.1 Dielectric Breakdown and Resistive Switching

It's widely accepted that gate leakage through the gate oxide leads to the generation of defects during the stress, which can cause larger leakage current [42]. When the density of defects is high enough leading to the creation of a defect-related conduction path between the two electrodes of the MOS structure, dielectric breakdown is triggered. After that, the oxide loses its dielectric properties and a sudden increment of tunneling current through the MOS structure can be observed [43–45]. Degraeve et al. [46] proposed a percolation approach to model the formation of conduction path by sphere where the defect radius is the only parameter of the model (Fig.1.6). Stathis also presented a similar approach though using a fixed cubic lattice [47] and considered the effect of different spatial distributions of defects in the oxide as a function of the distance from the interfaces [48].

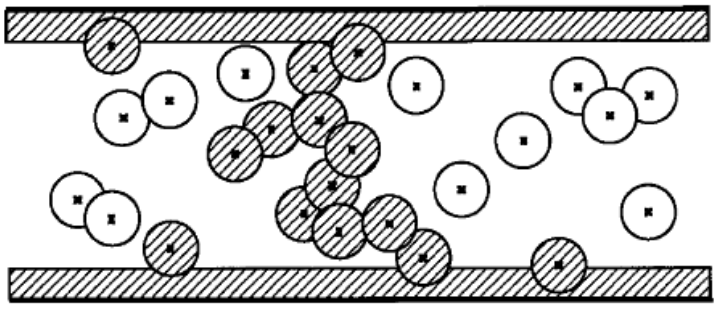


Fig. 1.6. Schematic illustration of the percolation model for intrinsic oxide breakdown simulation. A breakdown path is indicated by the shaded spheres [46].

Traditionally, the dielectric breakdown was observed as a complete loss of the dielectric insulation properties (hard breakdown, HBD) for oxides thicker than 10 nm. However, as the oxide thickness decreases below 7 nm, high-field stressing causes the increment of gate oxide leakage through tunneling assisted by the traps generated during the stress, which is referred as Stress Induced Leakage current (SILC) [49]. With further reduction of the oxide thickness, two more breakdown modes appeared: Soft Breakdown (SBD) [50] and Progressive Breakdown (PBD) [51]. The different BD modes can be distinguished by time scale of the BD triggering and the post-BD current level as observed in Fig.1.7.

Although the dielectric breakdown corresponds to the irreversible loss of the dielectric properties and has been treated as an important reliability problem in CMOS

technology, it has been demonstrated that the dielectric breakdown could be reversible if a sufficient current limit is set when it is triggered [52, 53]. The reversible phenomenon exhibiting two conductivity states is known Resistive Switching (RS) phenomenon and has powerful applications for memory devices. Typically, the change of resistance is non-volatile, resulting that the resistance state can be maintained for a long time following the removal of externally applied electrical field. The two resistance states are denominated Low Resistive State (LRS) and High Resistive State (HRS).

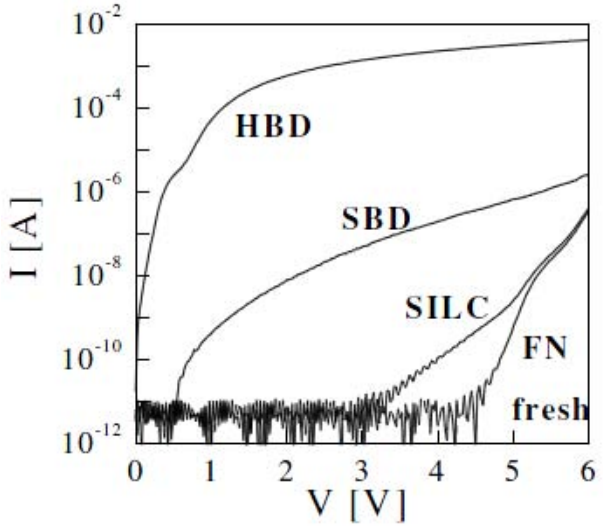


Fig. 1.7. Typical I-V characteristics measured in a MOS structure with a 4.35 nm thick oxide, showing different degradation and breakdown modes. The characteristic corresponding to the as-grown oxide is labelled as FN fresh [42].

Research on RS backs to early 1960's [54–56], but it becomes widely investigated since it is one of the best solutions to overcome the several technical limits of memory technology [57]. Among next generation of non-volatile memory (NVM), Resistive Random Access Memory (ReRAM) technology based on RS phenomenon is standing out for its simple structure, high switching speed, high scalability, low power and good compatibility with the standard CMOS process [58]. The resistive switching phenomenon has been observed in a wide variety of oxides, such as HfO_2 [59–64], TiO_2 [65–68], NiO [69, 70], and Cu_2O[71]. Three types of switching behavior can be classified: unipolar, bipolar and threshold switching, respectively. Typical I-V curves for the three kinds of RS are shown in Fig.1.8. Unipolar (Fig.1.8a) and bipolar (Fig.1.8b and c) switching exhibit at least two stable states without an applied bias, and these are therefore suitable for non-volatile mem-

ory applications. Threshold switching (Fig.1.8d) can also have multiple states in response to an applied bias; however, there is only one stable state when the external voltage is zero, resulting that the volatile switching phenomenon.

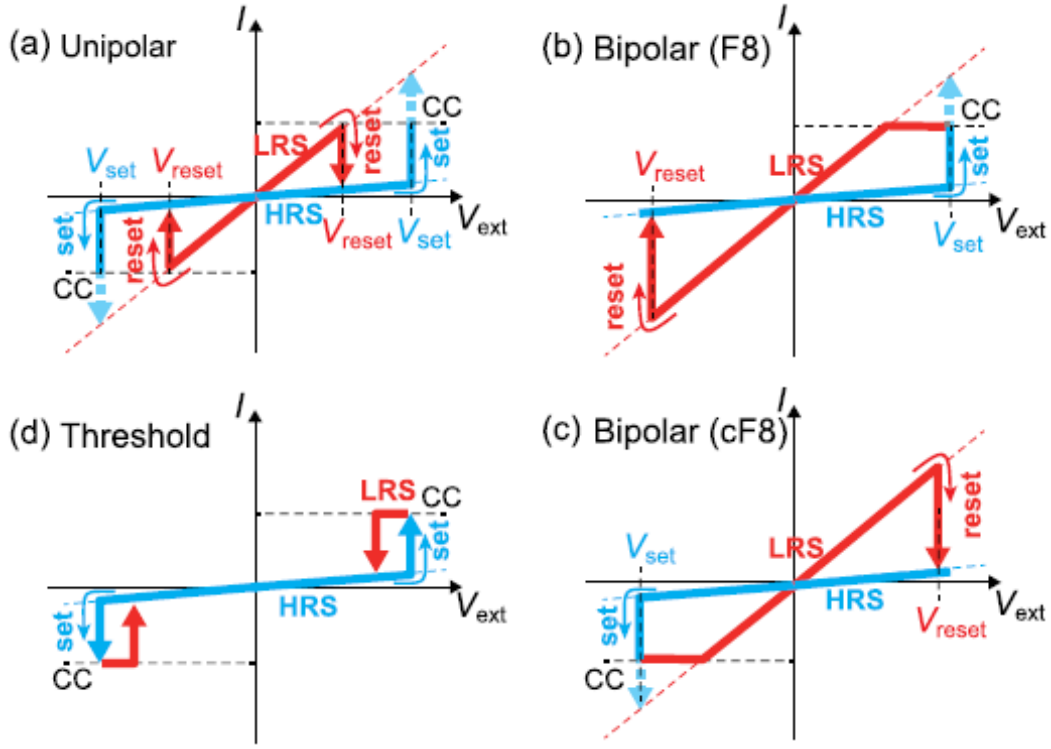


Fig. 1.8. Typical I-V curves of (a) unipolar switching, (b) figure-of-eight (F8) bipolar switching, (c) counter-figure-of-eight (cF8) bipolar switching with the set and reset occurring at a different polarity compared with the F8 case and (d) threshold switching with the LRS maintained only when a bias is applied [72].

In unipolar resistive switching (Fig.1.8a), the switching from HRS to LRS occurs at the same voltage polarity as the switching from LRS to HRS. Usually a fresh memory cell is in an initial highly resistive state and needs an external high voltage to change it into LRS. This process is called “forming” and the voltage at which the conductive filament is formed is named forming voltage, $V_{Forming}$. During the forming process, it is important to limit the flowing current, thus protecting the oxide against a complete dielectric breakdown. After the forming process, the switching from LRS to HRS is called “reset” and happens at a voltage, V_{RESET}, and switching from HRS to LRS is called “set” process and happens at a voltage, V_{SET}, larger than the reset voltage. In the set process, the current is also limited by the current compliance. The set and reset switching processes are repeatable for many times. In the case of bipolar resistive switching, writing and erasing occur under different

polarities. That is, the set to a LRS occurs at one voltage polarity and the reset to the HRS on reversed voltage polarity. Fig.1.8b show a typical bipolar RS cycles in which reset (set) process occurs with a negative (positive) bias. It is referred as "figure-of-eight (F8)" bipolar switching since the corresponding curve follows the pattern of writing the number "8". Fig.1.8c shows a counter-figure-of-eight (cF8) bipolar switching with the set and reset occurring at a different polarity compared with the F8 case.

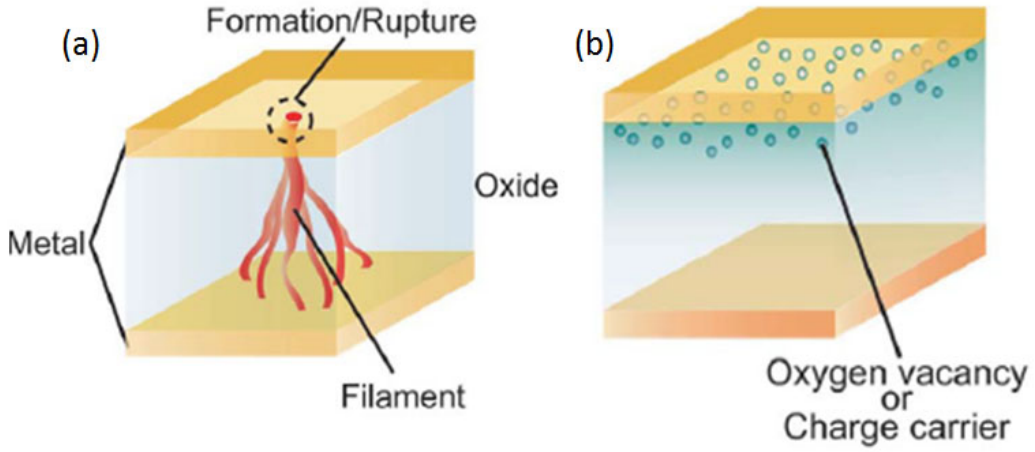


Fig. 1.9. Proposed models for resistive switching classified according to either (a) a filamentary conducting path, or (b) an interface-type conducting path [73].

In addition to the classification of the switching behavior, physical mechanisms that lead to the creation of the two conduction states are also used to categorize the RS [73, 74]. One mechanism is associated to a filamentary conductive path, in which the RS originates from the formation and rupture of conductive filaments (CFs) in the insulator (Fig.1.9a) [63, 75–82]. In the second mechanism, the RS takes place at the interface between the metal electrode and the oxide (Fig.1.9b). It has been mainly related to electrochemical migration of oxygen vacancies [83–91], trapping of charge carriers (hole or electron) [76, 92–95]. Whatever the mechanism responsible of the RS, the metal electrodes play a crucial role in the performance of the memory device [96]. Therefore, the election of the convenient material is a challenge, and novel materials like graphene have been proposed for the new generation of NVM based in MIM/MIS memories. In any case, RRAM technology is still in its infancy and great challenges must be faced. Despite considerable advances in fundamental research, the knowledge of the underlying physics behind the electrical phenomena of RRAM technology is still lacking. Fundamental rela-

tionships among the electrical transition phenomena, device parameters (including programming/erasing voltage and speed, ON-OFF currents ratio, retention time, reprogramming ability and cyclability) and materials properties should be explored. Recently graphene has been studied intensively because of its outstanding physical properties, which will be introduced in details in Section 1.5. In this thesis, the electrical properties and variability of MIS structures with and without graphene as interfacial layer between the top electrode and dielectric will be studied in Chapter 4.

1.3.2 Bias Temperature Instability

Another severe device degradation mechanism in ultra-scaled MOSFETs is the Bias Temperature Instability (BTI). BTI happens when a given voltage is applied to the gate while keeping the other terminals grounded. It is known that the transistor parameters degrade under these conditions, and this phenomenon is even more pronounced at elevated temperature [97, 98]. Depending on the polarity of the voltage applied to the gate, BTI is classified into two categories, Positive Bias Temperature Instability (PBTI) with $V_G > 0$ V and Negative Bias Temperature Instability (NBTI) with $V_G < 0$ V which will be considered in this thesis.

It is widely accepted that the physical phenomenon responsible for NBTI is related to the generation and/or activation of interface states and positive trapped charges in the oxide mainly in p-channel MOS devices under negative gate bias. NBTI was firstly reported by Miura and Matukura [99] and further characterized by researchers at Bell Laboratories [100, 101], Fairchild Semiconductor [102], and RCA Laboratories [103]. In the early studies, it was outlined that similar amounts of positive charge and interface state generation occur for both n- and p-type silicon substrate [102, 104]. However since the charge in the interface states on which threshold voltage, ΔV_{th}, depends, is greater for p-FETs, in this case the positive oxide charge and positive interface charge are additives [105]. This is one main reason why NBTI is of greater practical concern for p-FET devices compared to n-FET. NBTI causes a reduction in the absolute drain current (I_{Dsat}) and transconductance (g_m), and an increment of the threshold voltage (V_{th}), which can be described

as:

$$\Delta V_{th} = \frac{q\left(\Delta N_{if} + \Delta N_f\right)}{C_{ox}} \tag{1.6}$$

Where q is the electron charge, C_{ox} is oxide capacitance, ΔN_{it} is the density of charged interface states and ΔN_f is the density of fixed charge.

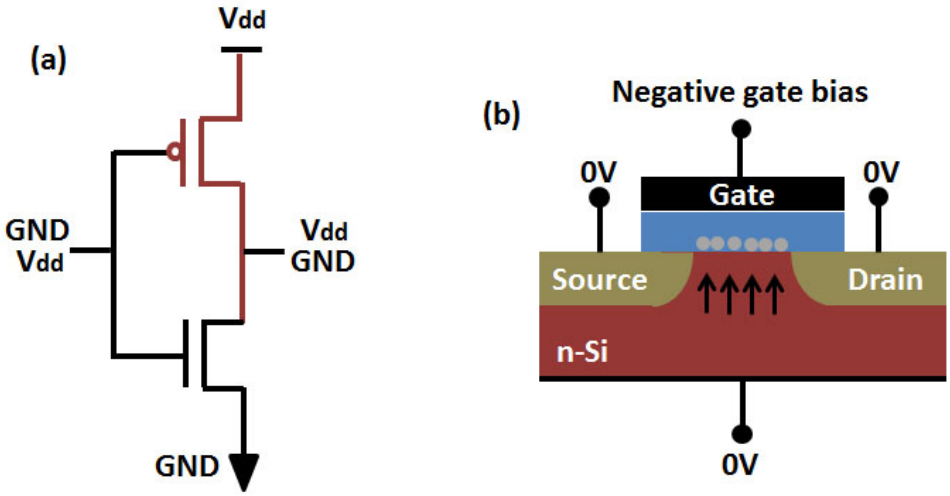


Fig. 1.10. (a) Bias conditions during circuit operation of a CMOS inverter. With input at ground, output is high and the p-MOS device (top) is under uniform negative gate bias with respect to its substrate, (b) schematic of a cross-section of a NBTI stressed p-channel MOSFET.

For the analyses of NBTI, a negative bias is applied to the gate of the sample (either a capacitor or transistor structure), with interruptions at desired intervals for device characterization. During the stress all other terminals (substrate, source, and drain) are grounded. In this way, the bias condition represents the homogenous damage of the whole active region. Fig.1.10 shows the bias condition during circuit operation of a CMOS inverter (a) and a schematic of the cross-section of a p-MOSFET under NBTI stress.

Different studies have tried to explain the physical origin of NBTI. Although little or no clear consensus has been reached until now, the reaction-diffusion model seems to be the most accepted theory to explain the experimental and theoretical aspects of NBTI. According to Reaction Diffusion model (RD model (Fig.1.11)) [106, 107], silicon hydrogen bonds (Si-H) break during the negative stress at the Si-SiO_2 interface. Therefore hydrogen is released and forms hydrogen ion (H^+) which diffuses into the oxide and returns back to the interface when the stress is

removed, indicating that the NBTI degradation can be recovered. It is worth noting that the magnitude of N_{it} is equal to the number of released hydrogen atoms at any given time. The released hydrogen atoms interferes with carriers and as a result, decreases I_D and shifts V_{th}. Thinner oxides have brought the poly-silicon gate closer the Si/SiO_2 interface. Since hydrogen diffusion through poly-silicon is faster than that in oxide, scaling of gate oxides has increased NBTI susceptibilities.

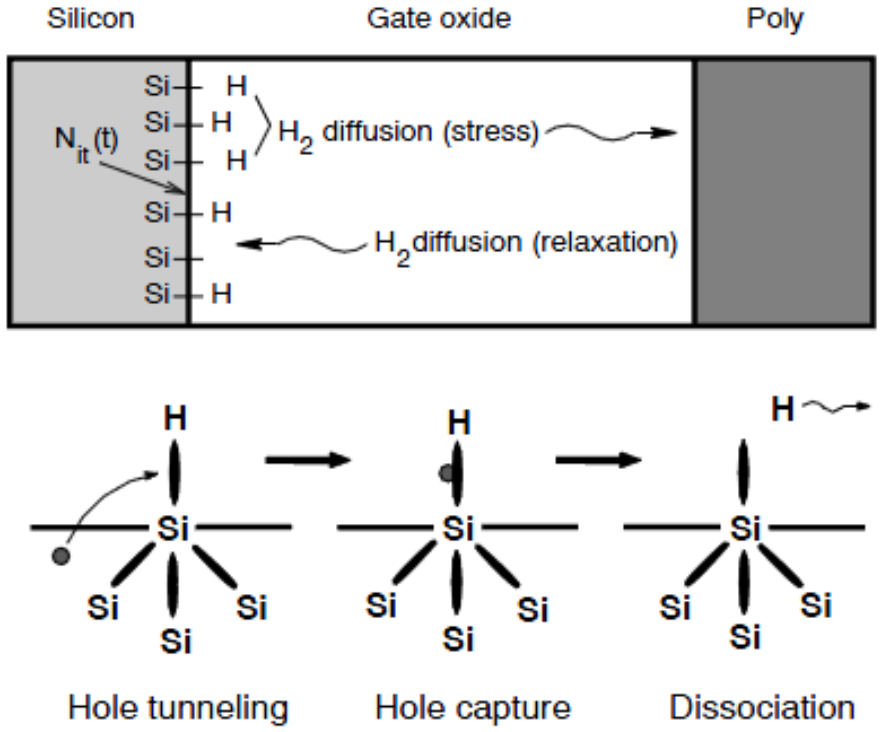


Fig. 1.11. Schematics of RD model, which indicates possible mechanism of breaking interfacial Si-H bonds by interaction with inversion-layer holes [106].

Once NBTI stress is removed from the device, the V_{th} degradation can be partially recovered, indicating a permanent and a recoverable component of the NBTI effects. This recovery can be very fast and should be taken into account as it is difficult to estimate the real damage generated in the device during the stress [108–110]. Due to the relaxation phenomena, NBTI degradation and device lifetime depend strongly on the measurement procedure and equipment [111–113]. As an example in Fig.1.12, it can be seen that if the delay between stress and measurement is short (0.4s) the lifetime is 1000s. If it is a long delay (100s), the lifetime increases until 7000s due to the relaxation effect [112]. Therefore, it is necessary to reduce as much as possible the time between the end of the stress and the characterization of the damaged device.

With the downscaling of MOSFETs, $\Delta V_t h$ should be proportionally reduced according to Eq.1.1and Eq.1.6. However, NBTI has been identified to be one of the most relevant degradation mechanisms due to several effects [114]: 1) the high operating voltage has not scaled as rapidly as gate oxide thickness, resulting in higher fields which enhance the NBTI; 2), device threshold voltage scaling has not kept pace with operating voltage, which results in larger percentage degradation of drive current for the same ΔV_{th}; and 3) the addition of nitrogen into the gate dielectric for gate leakage reduction and control of boron penetration has had the side effect of increasing NBTI. In this thesis, the electrical properties of MOSFETs with SiON as gate dielectrics after NBTI stress has been studied.

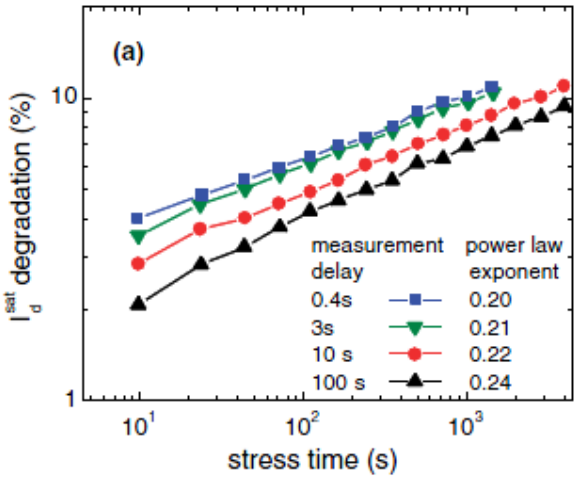


Fig. 1.12. NBTI degradation versus stress time for various delays between stress interruption and measurement.

1.3.3 Channel Hot-Carriers

In a MOSFET, hot carrier degradation occurs when the applied gate voltage V_G is higher than the threshold voltage $V_t h$ ($V_G > V_t h$), and when simultaneously, a voltage to drain above its saturation voltage is applied ($V_D > V_{Dsat}$), while the other terminals are grounded. With this configuration, the drain-source voltage (V_{DS}) leads to a strong lateral electrical field [115]. In this situation, charge carriers (electrons or holes) can gain a considerable amount of energy in the high electric field (hot carriers) to generate e^--h^+ pairs. Hence, the name *hot carriers* means energetic carriers. It is worth noting that the most damaging CHC conditions are:

V_G = V_D for pMOS (independently of the channel length) and V_G = V_D/2 and V_G = V_D for long and short channel nMOS transistors, respectively [116].

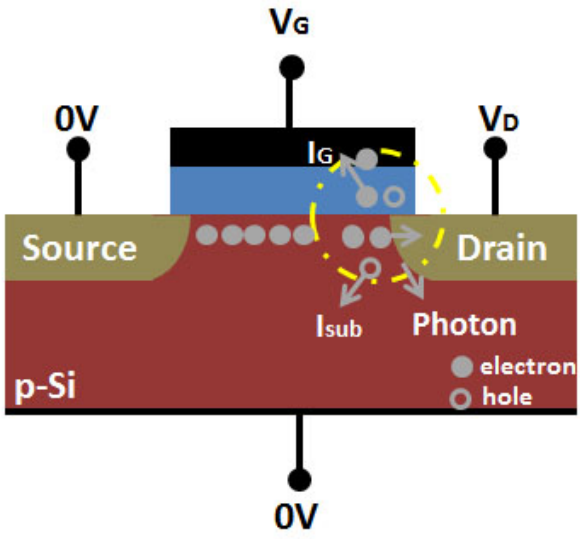


Fig. 1.13. Typical channel hot-carrier stress condition and the resulting high-field region of the drain in an nMOS transistor.

The majority of the hot carriers continues toward the drain, but a small number of them gain enough energy to generate electrons and holes by impact ionization. Considering an nMOSFET (Fig.1.13), the vast majority of the generated holes is collected by the substrate as substrate current (I_{sub}), while the generated electrons enhance the drain current ($I_D \approx I_S + I_{sub}$, where I_S is the source current). Isub can be recognized as the product of the source current (I_S) and the probability of the impact ionization. In this way, I_{sub} is the easiest way to measure and model hot-carrier current in a MOSFET [117]. Photon emission that takes place during hot-carrier generation in the drain is also an indication of the intensity of hot-carrier generation [118]. Some of the hot carriers gain so much energy that can surmount the energy barrier at the Si/SiO_2 interface and be injected into the oxide (N_{ot}), producing a small gate current (I_G) and generating interface traps (D_{it}). N_{ot} and D_{it} cause the change of threshold voltage and mobility degradation [119]. These modifications may ultimately affect the proper functioning of the integrated circuit itself.

It has to be noted, that the impact ionization mainly occurs in the pinch-off area (yellow circle in Fig.1.13) of the channel and hence the degradation essentially is

localized near the drain, which makes the hot carrier degradation a non-uniform degradation mechanism. In fact, some studies [116, 120] divided the transistor degradation in two components: on one hand the damage produced by the electrical field applied between gate and grounded terminals, and on the other hand, the CHC degradation located close to drain. In this case, the CHC degradation is a non-uniform degradation mechanism in contrast to NBTI degradation. In the last decades, BTI became more detrimental than the Channel Hot Carriers (CHC) degradation [1]. Nevertheless, for the recent technology nodes, CHC degradation has acquired a renewed relevance, because supply voltage reduction is slowing down, increasing in this way in the lateral electric fields in the devices. The impact of CHC degradation on the nanoscale properties of MOSFET gate dielectrics will be studied in details in Chapter 3.

1.3.4 Random Telegraph Noise

In MOSFETs, especially those ultra-scaled, drain current (I_D) or gate current (I_G) can exhibit fluctuations between two or more discrete current levels, which are random. These fluctuations look like a random telegraph signal (RTS) and is called Random Telegraph Noise (RTN).

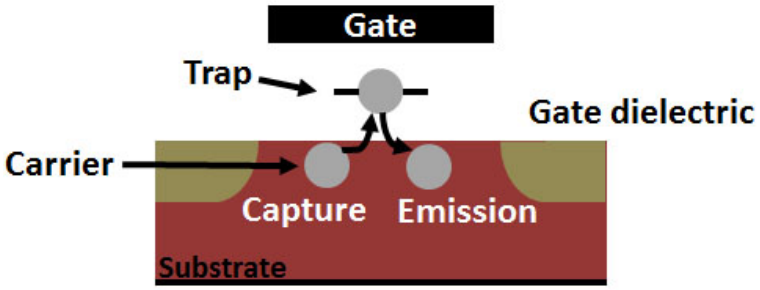


Fig. 1.14. Schematic of RTN behavior which is caused by single trap at gate dielectric.

Random Telegraph Noise (RTN) observed in MOSFETs is associated to the capture and emission of carriers at single traps in the gate dielectric (Fig.1.14), which is a random process. As an example, Fig.1.15a shows the typical RTN behavior of the gate current in time domain with two discrete states (capture and emission) referred as on and off, or up and down, in a MOS structure with a 5.6 nm thick SiO_2 gate dielectric when a bias of 6 V is applied to the gate. The value of on (τ_{on}) and

off (τ_{off}) time is known to show an exponential distribution and the power spectral density (PSD) of RTN is described as following:

$$S(f) = \frac{4A^2}{\left(\bar{\tau}_{on} + \bar{\tau}_{off}\right)\left[\left(\frac{1}{\bar{\tau}_{on}} + \frac{1}{\bar{\tau}_{off}}\right)^2 + (2\pi f)^2\right]} \tag{1.7}$$

where A is the amplitude of RTN and $\bar{\tau}_{on}$ and $\bar{\tau}_{off}$ are the average of τ_{on} and τ_{off}, respectively. Fig.1.15b shows the PSD corresponding to the data shown in Fig.1.15a, and the inset shows the frequency histogram with a clear exponential behavior of τ_{on}.

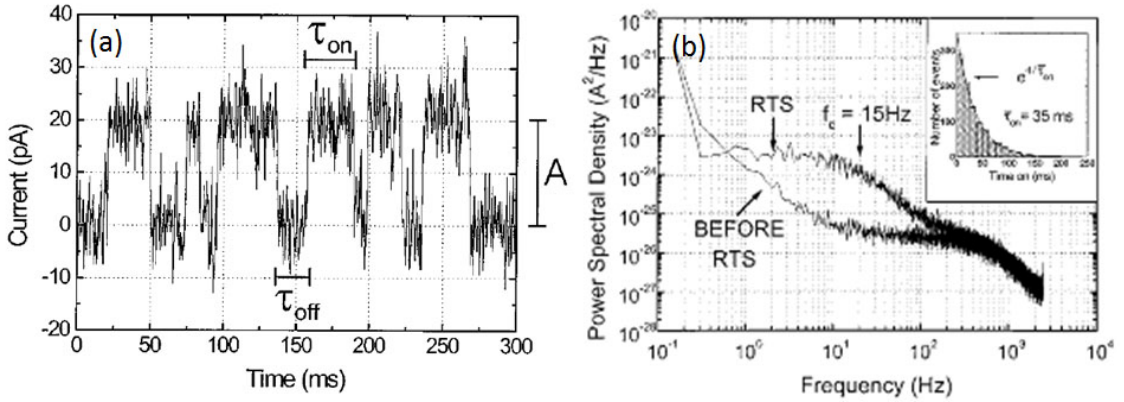


Fig. 1.15. (a) Typical two-state RTN behavior with amplitude of 20 pA during a 6 V stress in a MOS structure and (b) its PSD immediately before and during the RTS. The inset shows the frequency histogram with a clear exponential behavior [121].

The discrete switching of current in semiconductors backs to 1950s [122]. However, the RTN behavior in MOSFETs and the identification of its cause, namely, charge trapping/detrapping in/from interface and bulk traps at the gate oxide, have been reported from 1984 [123]. Since the RTN parameters depend on the kind and characteristics of the defects, in the past, researchers were interested in RTN just to investigate the fundamental characteristics of traps at gate dielectrics. However, low priority on RTN as a reliability issue was given until 2000s [124]. In 2006, it was firstly reported that RTN became a reliability issue in high-capacity flash memories [125]. Later, the 2009 International technology roadmap for semiconductors (ITRS), for the first time, mentioned that an attention is needed to be paid to RTN for static random access memory (SRAM) scaling because its acceptable noise margins are becoming narrower due to increasing V_{th} variability including RTN, as well mentioned in 2011 ITRS [36].

In ultra-scaled MOSFETs, there has been an enhancement of the impact of the current [126–128] and threshold voltage fluctuation (ΔV_{th}) in MOSFETs performance due to RTN [124, 129, 130], which can be approximately expressed as:

$$\Delta V_{th} = \frac{q}{L_{eff} W_{eff} C_{ox}} \tag{1.8}$$

where q is the elementary charge, L_{eff} is the effective channel length, W_{eff} is the effective channel width and C_{ox} is the gate capacitance per unit area [131]. This equation indicates that the RTN impact increases with the downscaling of gate dielectrics. Actually, the V_{th} variation of RTN for the 25 nm generation reached 70 mV [132]. Moreover, it has been experimentally proved that RTN and recoverable BTI are due to the same single defects [133], which makes the analyses of both RTN and BTI crucial for assessing time-dependent V_{th} variability and failure [130, 134–136]. In [135], it is demonstrated that RTN amplitude and time-dependent BTI-induced variability is further aggravated by interface state generation during operation in low doped pFETs.

In 2014, Intel commercially released Tri-gate transistors on the 22 nm technology [39]. However, variability such as NBTI and RTN will be likely to remain as the reliability challenges even in the age of the multi-gate transistor.

Since the RTN behavior can be one of the most important phenomena affecting the performance of MOS devices, and it is related to the behavior of single traps, CAFM is a powerful technique to study the trapping/detrapping defects at the gate dielectric. In this thesis, RTN in the gate current of an as-grown SiON based structure will be preliminary analyzed at different temperatures with CAFM.

1.4 Strain Techniques for Advanced Devices

As explained in Section 1.2, using alternative dielectrics is one way to reduce the high leakage currents. However, there are still many challenges that have held back the performance of the devices with alternative dielectrics. One of the main challenges is large carrier mobility degradation [137]. In this respect, new channel materials (as those based on Ge and/or III-V semiconductors [20]) and/or promis-

ing methods as strain engineering have found an important acceptance to improve MOSFETs characteristics. With the 90 nm technology node, strain techniques have been introduced to efficiently increase the transistor carrier mobility and drive current [138–143].

Strain impact on the intrinsic mobility was firstly investigated in the 1950's [144, 145], and the concept of enhancing mobility with strain gained interest again in the 1990's [146]. In the following years many different technologies to introduce strain into the channel of a MOSFET have been developed. Fig.1.16 shows the schematic of strain technologies currently in use. Among different technologies, global (substrate) strain techniques and process (local) strain techniques are considered to be one of the most promising for improving device performance [147, 148]. The strain is introduced across the entire substrate in global techniques. However, in local strain techniques, the strain is inserted locally at certain places.

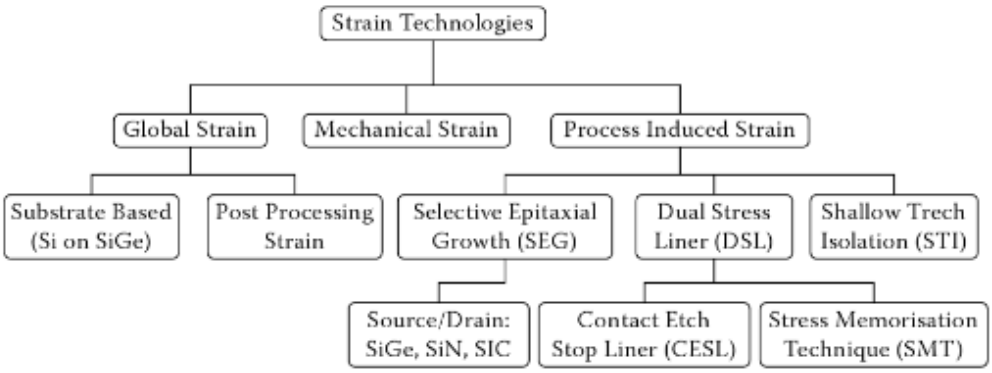


Fig. 1.16. Schematic of strain technologies for mobility enhancement currently in use [149].

One method of local strain techniques consists in the selective growth of a local epitaxial film in the source and drain regions of a transistor [147]. In nMOSFETs, SiC, which has a smaller lattice than Si substrate, is epitaxial grown at S/D regions to achieve uniaxial tensile stress (Fig.1.17a), and in pMOSFETs, epitaxial growth of SiGe, which has a larger lattice constant than Si substrate, is used to create uniaxial compressive stress (Fig.1.17b). In this thesis, strained SiGe S/D pMOSFETs will be studied.

The growth of strained SiGe in the S/D areas, with a substitutional Ge concentration (between 20% and 35%) leads to an improvement of the drive current in short channel transistors [138]. This improvement is attributed firstly, to the presence of

uniaxial compressive stress in the silicon channel, which favorably alters the band structure, enhancing the hole mobility and secondly, to the presence of the highly activated SiGe Source/Drain regions, which provides a reduced resistivity and series resistance[150]. There are several most essential parameters as recess depth, Ge concentration, recess shape and gate length, which affect the amount of stress present in the channel. In Fig.1.18a, it shows that a deeper recess depth of the source drain areas will create a higher channel stress. The stress variations with recess depth will be important for depths lower than 60 nm. Furthermore, one of the most essential parameters for the increase of the channel stress is the amount of substitutional Ge in the strained S/D regions. It's also important to know that the compressive stress decreases as the gate length increases, especially for the gate length shorter than 1 μm (Fig.1.18b).

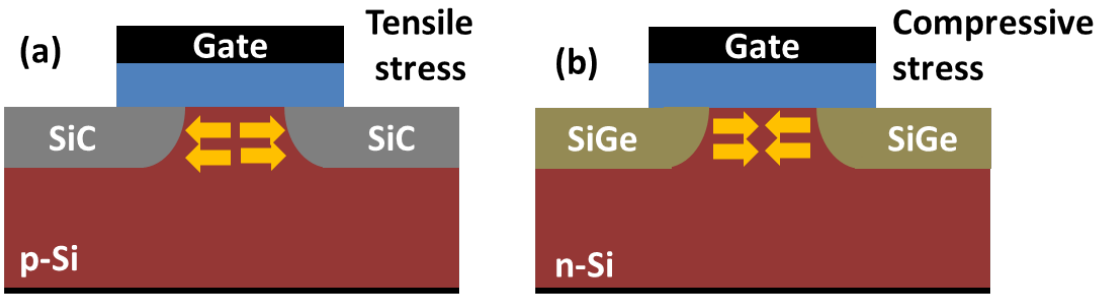


Fig. 1.17. Schematic of transistors of nMOS (a) and pMOS (b) with induced mechanical stress.

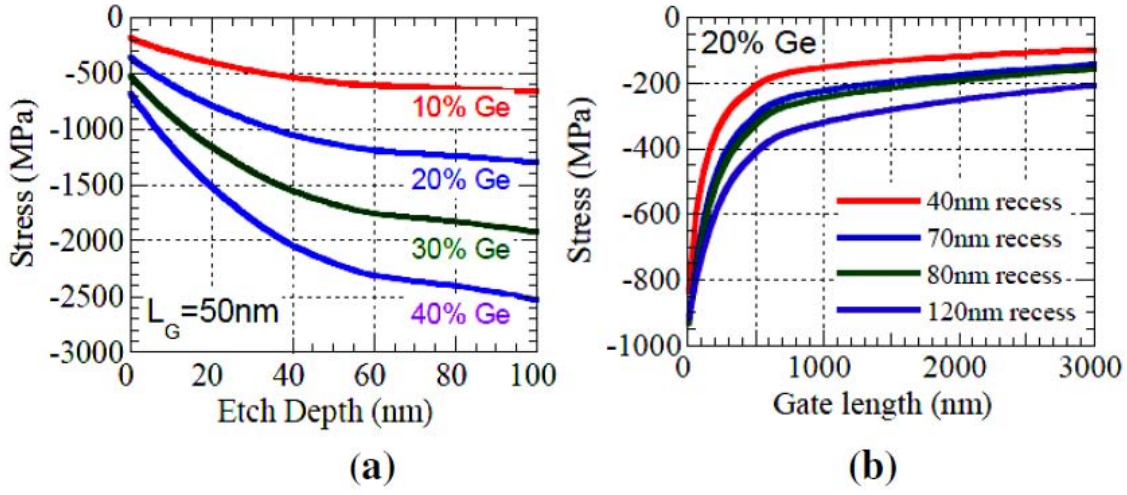


Fig. 1.18. Simulated channel stress dependence on the substitutional Ge content and recess depth (a) and gate length dependence (b) for SiGe pMOSFETs [151].

However, one concern is the possible presence of extended defects at the SiGe/Si interface. As a consequence, the Channel Hot-Carrier (CHC) degradation and Bias temperature instability (BTI) can be enlarged [152]. These failure mechanisms of p-MOSFETs with epitaxial grown SiGe will be analyzed in Chapter 3.

1.5 Graphene-based Devices for Memory Applications

Conventional memory scaling is expected to reach physical limits in the near future. A number of alternatives to present Flash memories are being extensively investigated by introducing new materials and/or other new device concepts, which could operate under physical principles very different from those of conventional floating gate based memories [153]. Candidates for equivalent scaling can be based on new materials as ferroelectric random access memory (FeRRAM), magnetoresistive RAM, phase-change RAM and Resistive Random Access Memory (RRAM) [73, 74] (see Section 1.3.1). In the case of RRAM devices, the so called 2D materials may revolutionize the information technology industry. Since the isolation for the first time of graphene in 2004 [154], researchers have found new kind of 2D analogues, like the insulators graphene oxide (GO) [155] and hexagonal boron nitride (hBN) [156], or the semiconductors dichalcogenides, like MoS_2 [157] or WS_2 [158]. Recently, more exotic 2D materials are appearing, like the silicene [159], germanene [160] or phosphorene [161].

Graphene, which is a one-atom-thick planar sheet of sp2-bonded carbon atoms arranged in a honeycomb crystal lattice, has attracted great attention of researchers since 2004 [154, 162–165]. The interesting properties of graphene make it an ideal candidate for electronic device applications; for example, field effect transistors [166–170], energy storage cells [171–173], micro-nano electromechanical systems [174] or spintronic devices [175–177]. Some of the most relevant properties of graphene, which have been demonstrated, are high mobility [178–180], high thermal conductivity [181], high current density [154, 182] and transparency [183]. The minimum conductance of macroscopic graphene at the Dirac point, where no carriers are nominally present, is still too high to result in a significant ON and OFF

current (I_{on}/I_{off}) ratio sufficient for logic applications [184]. However, graphene is still promising for flexible electronics, analogic electronics and/or memory applications.

Method	Crystallite size(μm)	Sample size (mm)	Charge carrier mobility (at ambient temperature) ($cm^2V^{-1}s^{-1}$)	Applications
Mechanical exfoliation	>1000	>1	>2×10^5 and >10^6 (at low temperature)	Research
Chemical exfoliation	$\leq$0.1	Infinite as a layer of overlapping flakes	100 (for a layer of overlapping flakes)	Coatings, paint/ink, composites, transparent conductive layers, energy storage, bioapplications
Chemical exfoliation via graphene oxide	$\sim$100	Infinite as a layer of overlapping flakes	1 (for a layer of overlapping flakes)	Coatings, paint/ink, composites, transparent conductive layers, energy storage, bioapplications
CVD	1000	$\sim$ 1000	10000	Photonics, nanoelectronics, transparent conductive layers, sensors, bioapplications
SiC	50	100	10000	High-frequency transistors and other electronic devices

Tab. 1.1. Properties of graphene obtained by different methods [185].

The properties of graphene, especially Graphene Single Layer (GSL) for high performance electronic devices, depend very much on the quality of the material, type of defects, substrate, and so forth, which are strongly affected by the production method. Tab.1.1 shows a summary of the different methods to synthetize graphene [185]. With the method of Chemical exfoliation with and without oxidizing the graphite pellets, monolayer graphene flakes can be obtained for application such as coating, paint/ink. Through SiC method, which is based on the growth of graphene on SiC, the quality of such graphene can be very high, with crystallites approaching hundreds of micrometers in size for high-frequency transistors and

other electronic devices. However, two main drawbacks of this method are the high cost of the SiC wafers and the high temperatures used, which are not directly compatible with silicon electronics technology. Among the different methods used to synthesize graphene, Chemical Vapor Deposition (CVD) has shown to be one of the most common approaches to obtain GSL on Cu and/or Ni, which can then be transferred to other substrates for many applications [167–170]. The obtained GSL has smooth surface interrupted by wrinkles which are a consequence of the variable grain structure of the metal catalyst film and differences in the thermal expansion coefficients of metal and graphene. Moreover, during the transference process, the wrinkles may increase and affect the performance of the graphene based structure. In Chapter 4, the transference process of GSL obtained by CVD.

In the field of memory devices, graphene could offer great advantages over the current state-of-the-art memories and other upcoming technologies [186–190]. In [187] it was demonstrated that the use of graphene as gate electrode in a non-volatile Flash memory device increases its retention time. The excellent properties of graphene and the fact that the RS phenomenon depends on the electrode characteristics make the inclusion of graphene a very promising alternative as electrode in capacitive structures for memory applications in RRAM technology. Recently, some works have included graphene as interfacial layer between the metal oxide and top electrode (i.e. MGIS or MGIM structures) [191–195]. In [192], it was demonstrated that graphene provide a larger charge trapping state density revealed by the larger memory window, enhanced memory endurance due to the pure electrons storage, and enhanced retention. Also, the graphene-based memory showed a faster program speed compared to Si nanoparticle memory, which highlight that such memory structures have potential in next-generation non-volatile memory devices. In [195], a significant improvement of the on state resistance retention was observed. This is related to an effective oxygen reservoir effect of the graphene inserted layers, which stabilizes oxygen species released during set operation. Mechanisms about the origin of oxygen storage are still unclear but two main hypotheses emerge: Oxygen insertion between graphene layers or at the graphene-oxide interface and graphene oxidation. This comparative study demonstrates the benefits of graphene intercalation in RRAM memories with a significant improvement on the retention effect.

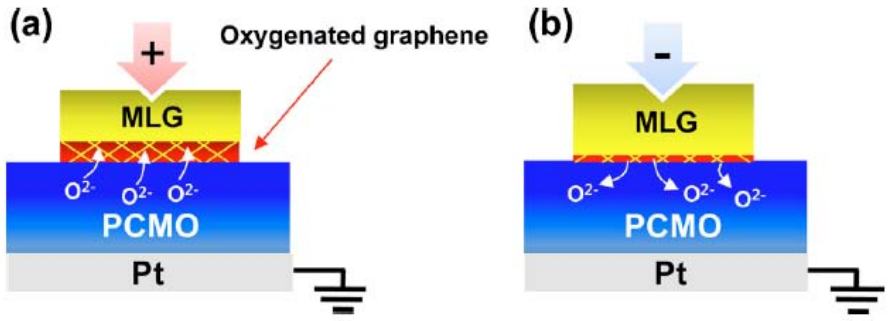


Fig. 1.19. Schematic illustrations of resistive switching in MLG (Multi-Layer Graphene)/PCMO/Pt device: (a) HRS and (b) LRS.

Recent works have even explored the inclusion of graphene as top electrode in RS based devices [196–199]. In [196], graphene/$Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO)/metal structures exhibited an interfacial reaction, attributed to the formation-dissolution of an oxygenated graphene layer at the graphene/PCMO interface (see Fig.1.19). Moreover, the lower work function of graphene as compared to noble metals reduces the SET and RESET voltages, as demonstrated in [199], where Pt/NiO/graphene RRAM nanocapacitors were fabricated and compared to Pt/NiO/Nb-doped devices. Other works [197], used graphene as a SET electrode in a three-dimensional (3D) RRAM arrays, and demonstrated ultra-high-density, low power consumption, and high storage potential for graphene devices.

With continuous enhancement in the device fabrication techniques, the performance, stability and reliability of the graphene based memories have advanced significantly towards practical information storage applications. However, great challenges still persist against the commercially viable devices. The underlying switching and conduction mechanism in graphene-based memories has yet to be clearly understood and a solid interpretation of the physics behind the interesting electrical phenomena is still lacking [185]. Nevertheless, it is crucial to elucidate the exact role of a graphene electrode in a RRAM structure in order to be able to fabricate fully 2D devices. In this thesis, the transference process of GSL grown by CVD onto Si substrates has been improved and the electrical properties and variability of graphene-based devices will be analyzed, and moreover, graphene based structures for RRAM applications will be analyzed at both device level and nanoscale with CAFM.

1.6 Characterization Techniques

In order to get information of the electrical properties and failure mechanisms of micro- and nanoelectronic devices, electrical tests are applied to test structures. In this section, the characterization techniques which are used to perform these analyses are introduced.

1.6.1 Standard Characterization Techniques

By standard characterization techniques, the electrical tests normally used consist in the application of voltages or the injection of currents (called electrical stresses) through test structures (generally MOS capacitors or transistors [200]), and the measurement of the evolution of their electrical properties. The test structures are placed in a probe station (Fig.1.20a), which is used to connect each electrode of the device to the instrumentation such as a Semiconductor Parameter Analyzer (SPA, Fig.1.20b).

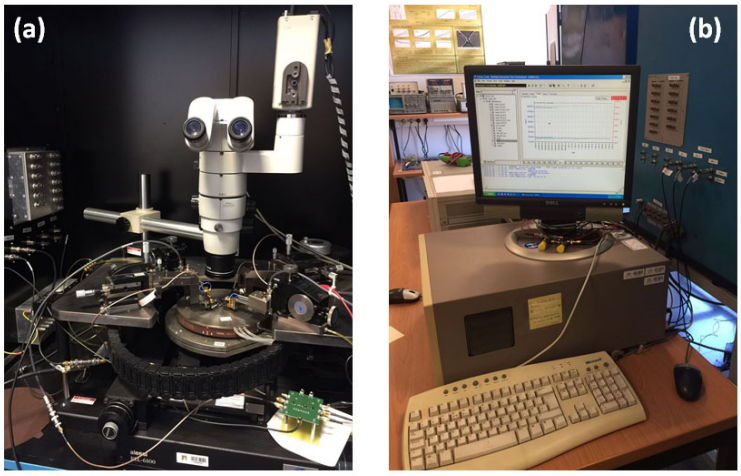


Fig. 1.20. Images of the probe station (a) and Semiconductor Parameter Analyzer, SPA, and connected computer (b) used in this thesis.

Since degradation times are very large in normal operation conditions, during the electrical test, higher voltages are applied in order to accelerate the degradation in reasonable times. The most common tests which will be used in this thesis are briefly described below:

- *Ramped Voltage Stress* (RVS): In this test, a ramped voltage is applied to the gate of the test structure. I-V curves can be plotted to see the electrical properties of the device.

- *Constant Voltage Stress* This test consists in the application of a constant voltage to the gate electrode over time. As a consequence, the current versus time can be plotted.

For its straightforward principle of RVS, it is widely used to study the dielectric breakdown. Moreover, with the application of a Current Limit (CL) during the ramped voltage, RS phenomenon can be analyzed through the measurements of I-V curves in MIS/MIM devices. Fig.1.21 shows typical I-V curves obtained in NiO devices [201]. The first voltage ramp is applied until the breakdown (formation of the conductive filament) happens (while the current is limited to I_{comp}, to set the device to LRS. Then another ramped voltage is applied to reset it back to HRS. The voltage for the set and reset is referred as SET and RESET voltage, V_{SET} and V_{RESET}, respectively, as mentioned in Section 1.3.1.

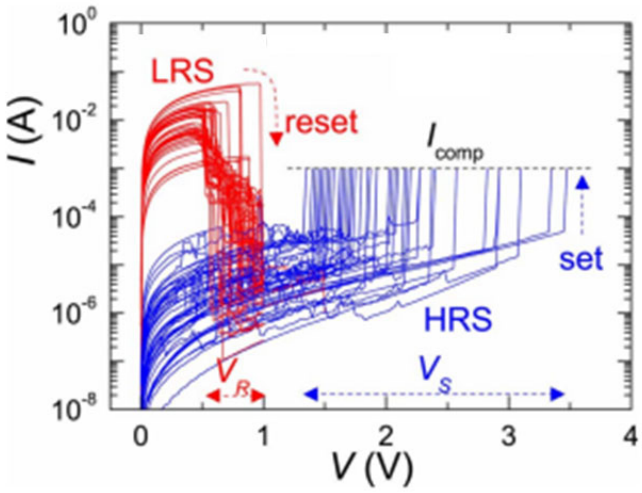


Fig. 1.21. Typical I-V curves of RS observed in NiO capacitors [201].

On the other hand, Ramped voltage tests are also used to measure the main electrical characteristics of the MOSFETs like I_{DS}-V_G, I_{DS}-V_{DS}, I_G-V_G and I_{sub}-V_G curves and determine the electrical characteristics of the MOSFETs. CVS is also used to stress the device when failure mechanisms as NBTI and CHC are studied. After that, I_{DS}-V_G, and I_{DS}-V_{DS} curves are measured again. These tests also allow

to measure the time to breakdown (t_{BD}), and the time evolution of the electrical properties of the oxide before breakdown.

These tests are usually applied to the whole active area of the device and are referred as standard characterization techniques. Standard characterization techniques can provide only averaged information of the electrical properties of the oxide. However, degradation and the failure mechanisms that affect the gate oxide of MOSFETs and the CF associated to RS in MIS/MIM devices are phenomena that have been found to have a nanometric origin, since they are related to the generation of defects and/or the formation of conductive paths in the gate oxide. Therefore, the correlation between structural defects with their impact on the electrical performance of devices as measured by the conventional electrical measurement techniques (C-V, I-V), is not possible if standard characterization techniques are only used. These considerations strongly suggest that there is a need to be able to locate single defects in dielectric layers and directly assess their impact on the electrical properties of these layers. In this respect, alternative techniques with a nanoscale resolution are required if these phenomena want to be studied in detail. In next section, these characterization techniques will be briefly introduced.

1.6.2 Nanoscale Characterization Techniques

Since the middle of the 80's, with the invention of the Scanning Tunneling Microscope (STM), a new family of microscopes, the Scanning Probe Microscopy (SPM) based techniques, have turned into very important tools for nanoscale characterization. A SPM is based on an extremely sharp tip, which scans over the surface of a materia, while measures its topographical and electrical properties with nanometer resolution. SPMs are able to obtain a sub-nanometric lateral and vertical resolution and three-dimensional quantitative information of the investigated surface. Several SPM instruments has been developed over the past decades, which can sense topography, current, contact potential, resistance, force, temperature, magnetic field, capacitance and so on.

The first STM was developed in 1981 at IBM Zurich Research Laboratory by Binning and Rohrer [202] (Nobel Prize in Physics in 1986) with the ability to view the atomic lattice of a sample surface. Although the STM provides sub-angstrom

resolution in all three dimensions, it is limited to conductive and semi-conductive samples and requires ultrahigh vacuum environments. The STM is based on the detection of the tunneling current (nA) that flows between the tip and a sample when the separation between them is of just few nanometers and the sample is polarized. The current (which depends on the tip-sample distance) is measured and is used to evaluate the topographical properties of the surface atoms. However, since tunneling current depends not only on the tip-sample distance but also on the electrical properties of the structure, electrical and topographical information cannot be simultaneously and independently measured. All these limitations led to the invention in 1986 of the first Atomic Force Microscope (AFM) [203]. With AFM based techniques, topographical and electrical information on both insulators and conductors can be collected, simultaneously and independently, without specific environment. Depending on the measured electrical magnitude, different AFM based techniques have been developed. One of the most powerful to study micro- and nanoelectronic devices (and gate oxides) is the Conductive Atomic Force Microscope (CAFM) [204], which allows measuring the current that flows between tip and sample (see Chapter 2).

Since the mid-1990s, CAFM has been used to study the electrical properties of gate oxides [205–208]. In the first studies, CAFM was used to evaluate the dielectric strength of SiO_2 gate oxides [209], local variations of the gate oxide thickness with high resolution [210], the influence of electrical stress [211–213] and irradiation [214] on the oxide degradation. Since 2000s, the CAFM has been used to analyze high-k materials [215–217]. Some works studied the electrical homogeneity of HfO_2 and $HfAlO_x$ films on silicon [218, 219] and the impact of high-k polycrystallization on the topographical and electrical properties of such material [220]. Afterwards, different materials were investigated, for example Al_2O_3 [221], Pr_2O_3 [222], ZrO_2 [223], Ta_2O_5 [224], $SrTiO_3$ [225]). Some works have also investigated the degradation of high-k dielectrics based gate stacks. For example, in [226] it was demonstrated that the bimodal BD distributions measured in polycrystalline high-k dielectrics can be attributed to the different electrical properties of grains and grain boundaries. In [227] the SILC in ALD grown ultrathin Al_2O_3 films has been investigated using C-AFM, showing great difference of SILC and degradation of thick films, with respect to thin films.

Recently, CAFM has been used to investigate RS phenomenon in memory devices due to the local characteristics of the CF [64, 80–82, 228–231], and oxygen vacancy defects [90, 91, 232]. As an example in [65] it was revealed that the amount of conductive spots in the LRS is larger and show lager current than in the HRS, confirming again the capability of CAFM to analyze the resistive switching phenomenon at nanoscale. At this respect, CAFM can be used for helping to understand the switching and conduction mechanisms.

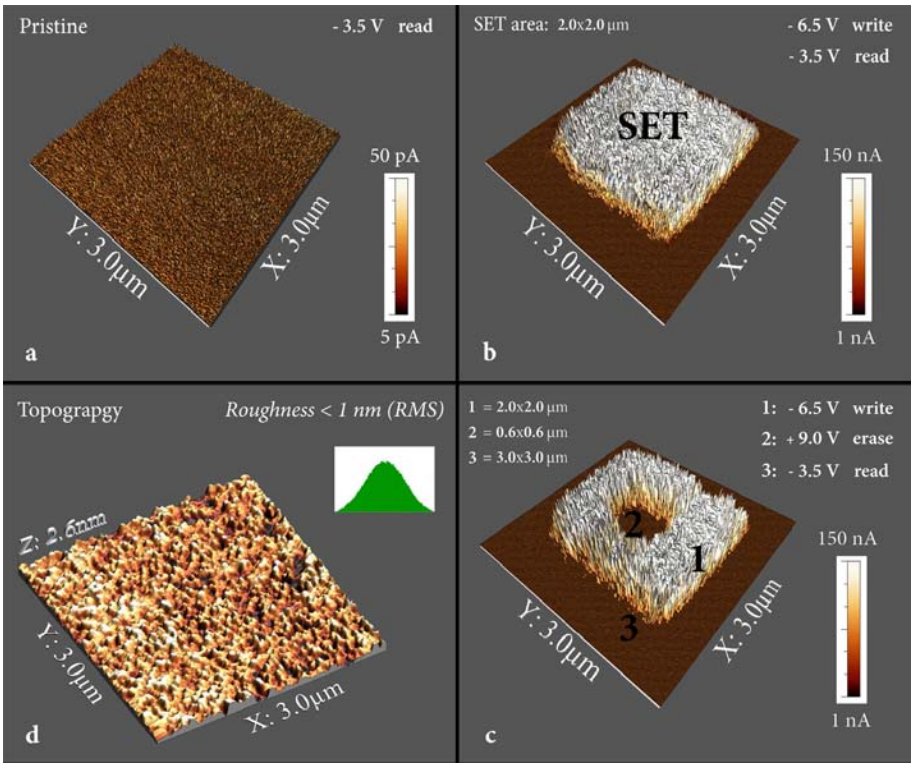


Fig. 1.22. Current images of TiO_{2x}/Au film (a) prior to any process, (b) LRS after applying -6.5 V on the back electrode in an area of 2 $\times$ 2 μm^2 and (c) HRS after applying 9 V on the back electrode in an area of 0.6 $\times$ 0.6 μm^2 inside the initially LRS region, (d) topographic image of the sample surface during resistive switching operation [90].

Some works have used the tip of the CAFM not only to characterize the CF, but also to induce the set and reset processes by applying RVS with the tip directly on the bare surface of the insulator, and then measure the CFs characteristics [230]. This method permits not only the in situ observation of the CF in each state, but also to analyze the evolution of the electrical properties of single CFs depending on the applied bias. Other methods have induced the set, reset and read operations by scanning the surface with CL [64, 90, 233, 234]. Current maps have shown a top view of CF through the insulator and information about the CF such as size,

maximum current and volume can be evaluated. For example, Bousoulas et al. [90] presented the bipolar switching behavior in a TiO_{2-x}/Au film with CAFM (Fig.1.22). Fig.1.22a shows the current map of a pristine device, in which only noise level of current can be observed. After applying -6.5 V on the back electrode in an area of 2 $\times$ 2 μm^2, the area was set to be in the LRS and the large current indicating the formation/annihilation of oxygen vacancy-based filaments can be observed in Fig.1.22b. Next, 9 V was applied in an area of 0.6 $\times$ 0.6 μm^2 inside the initially LRS region, and current in this area was lower than outside (LRS area), which suggests that this area was reset to be in the HRS (Fig.1.22c). Finally, Fig.1.22d shows the topography of this film with the RMS less than 1 nm.

To sum up with this section, it has been demonstrated that CAFM is a powerful technique to investigate at nanoscale the electrical properties, reliability and variability of materials for nanoelectronics applications, as SiON, high-k dielectrics, graphene and so on. In this thesis, the CAFM has been used to study the degradation in the gate stack of on strained and unstrained MOSFETs. Different kind of degradation mechanisms including NBTI, CHC and RTN will be considered. RS in MIS structures with and without graphene layers will be investigated with CAFM as well.

Chapter 2

Atomic Force Microscope, related techniques and experimental considerations

As introduced in Chapter 1, AFM is one of the most powerful tools for the characterization of materials and devices at the nanoscale, especially when their electrical properties need to be analyzed. In this chapter, AFM and those techniques used in this thesis, such as Conductive Atomic Force Microscope (CAFM), will be described. As the AFM resolution and reliability of the measurements highly depends on the tip properties, details about probes will be introduced. In particular, the impact of the tip-sample resistance is analyzed. Finally, since AFM measurements at different temperatures will be performed in this thesis, the setup calibration will be discussed in this chapter as well.

2.1 Atomic Force Microscope

The AFM (Fig.2.1a) is based on the measurement of the interaction forces that appear between the tip and the sample when the distance between both is in the nanometric range. Since the tip is located at the end of a flexible cantilever, any force applied to the tip causes a deflection of the cantilever, Δx, which is propor-

tional to the force according to the Hooke's law, F= -kΔx (where k is the spring constant of the cantilever). This deflection can be sensed commonly by a system based on a laser beam which can shine onto and reflect off the back of the cantilever into a segmented photodiode to measure the tip motion (Fig.2.1b). By detecting the difference in the photodiode detector output voltages when the cantilever is deflected, changes in the cantilever deflection or oscillation amplitude are determined which give the user information about the position of the sample under the tip. A piezoelectric tube is used to control the scan of the tip over the surface (X and Y direction) to obtain the topography maps. Moreover, by applying the required voltage to the piezoelectric tube, an electronic feedback continuously corrects the Z-axis tip position during the scan to maintain constant the tip-to-sample distance and the force applied to the tip. Typically, the resolution of an AFM can be 2-10 nm in x and y direction and 0.1 nm in z direction. Finally, taking into account that an AFM works at the nanoscale, a mechanical anti-vibration system is necessary to avoid the AFM from external vibrations.

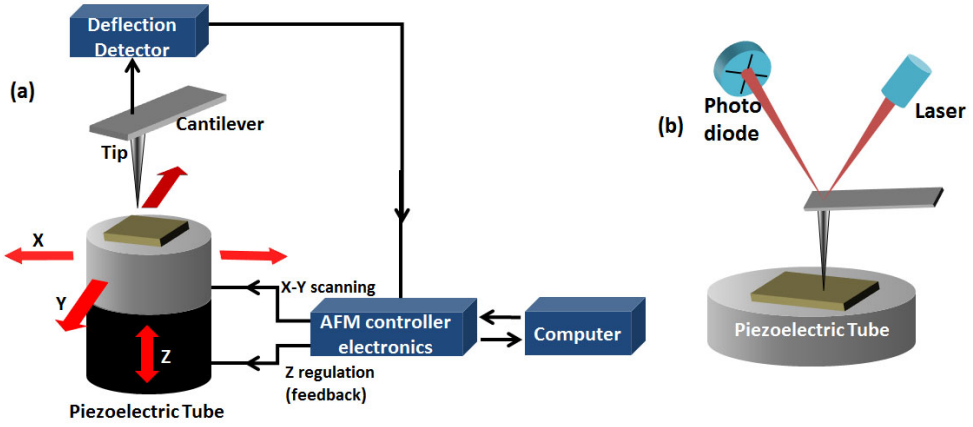


Fig. 2.1. Schematic of a conventional Atomic Force Microscope (a) and the optical deflection detector (b).

2.2 Operation Modes

Typically, depending on the distance between tip and sample and therefore, the forces applied to the tip during the scan, AFM can be operated in three modes (Fig.2.2):

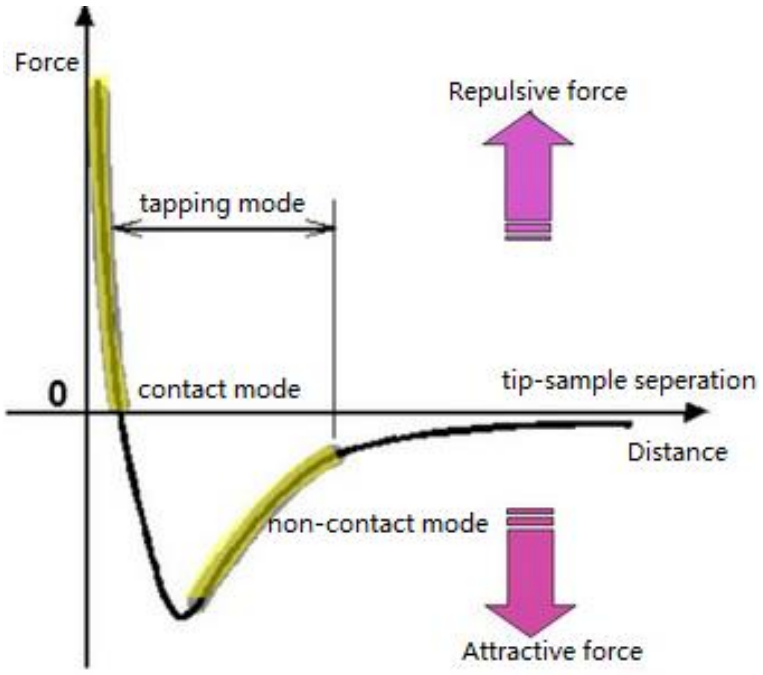


Fig. 2.2. Interatomic force versus distance between AFM tip and sample surface.

- *Contact mode*: The atoms at the end of the tip are close enough to the sample surface (at a distance of 1-3 $\mathring{A}$) [235], and the interaction force is in repulsive regime as shown in Fig.2.2. As the tip is in permanent contact during the entire scan, it wears out fast, which is one of the main drawbacks of this operation mode. However, the vertical resolution obtained in this mode is higher than in non-contact mode [236].

- *Non-contact mode*: The interaction force is in attractive regime (Fig.2.2) [237], keeping the tip close enough to the sample surface, but without being in contact. Since the attractive forces (mainly Van der Waals' forces) applied to the tip are substantially weak, the tip must be given a small oscillation so that these small forces can be detected by measuring the change in amplitude, phase, or frequency of the oscillating of cantilever. From this information, topographic images can be obtained. In this mode, the absence of repulsive forces permits the imaging of "soft" samples to provide topography with little or no contact between the tip and the sample.

- *Tapping mode*:This mode is an intermediate operation mode between contact mode and non-contact mode, which overcomes problems such as friction and adhesion, and offers a very high resolution. In this mode, the cantilever is os-

cillated at or near its natural resonant frequency (Fig.2.3)[237] and the tip vibrates towards the sample until it begins to lightly tap the surface. During tapping mode operation, the oscillation amplitude is kept constant through a feedback loop and the force on the sample can be automatically maintained at very low detectible level. When the tip passes over an obstacle on the surface, its vibration amplitude decreases. On the other hand, when it passes over a depression, its vibration amplitude increases. This change in the oscillation amplitude is detected by the optical system and fed back to the controller (which compares the measured value with the set reference value) and adjusts the tip-sample separation to maintain the amplitude, and thereby the force constant.

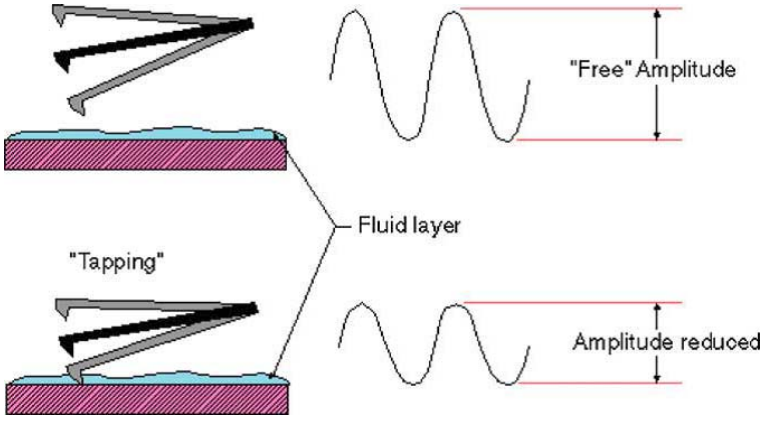


Fig. 2.3. Schematic of tapping mode.

2.3 Conductive Atomic Force Microscope (CAFM) and Resiscope

2.3.1 Conductive Atomic Force Microscope (CAFM)

Since this thesis is focused on the electrical characterization and reliability of gate oxides of MOSFETs and MIS structures for memory applications, CAFM (Conductive AFM), which can perform simultaneously topography and electrical conductivity measurements, has been used. A CAFM is an AFM based technique with three additional elements comparing to conventional AFM: 1) a conductive tip, 2)

a voltage source and 3) a very low noise preamplifier (Fig.2.4). With this setup, when a voltage is applied between the tip and the sample, current through it can be measured.

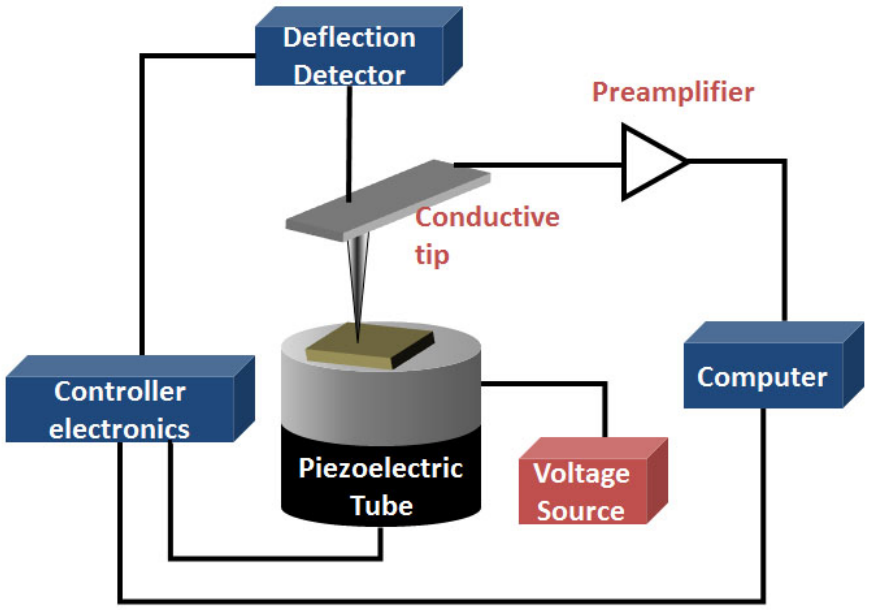


Fig. 2.4. Schematic of a CAFM.

CAFM is used to obtain electrical information through the measurement of current maps in a given area simultaneously with the topographical images by applying a constant voltage between the tip and the sample. This provides the possibility to correlate directly topography with electrical information from the measurement of topographical and current maps, which represent the electrical conduction for each point at a given bias voltage. Besides, CAFM provides the option of spectroscopic analysis as well in a given position of the sample when the tip is fixed on it. Different types of spectroscopic tests can be performed, of which, the two most commonly used types are: ramped voltage tests (RVT) and constant voltage tests (CVT). In RVT, I-V curves can be obtained to analyze the different conduction mechanisms at a given site, and in CVT, I-t curves can be obtained to analyze, for example, the time evolution of the electrical properties of the sample.

2.3.2 Resiscope

Although CAFM is a powerful technique to study the electrical properties of gate oxides, its current dynamic range is limited typically by the preamplifier to 3-4 orders of magnitude, from 1 pA to 10 nA. Different solutions have been developed to overcome this limitation, as the connection of a Semiconductor Parameter Analyzer to the tip [238], or the development of a logarithmic preamplifier [239]. Nowadays, however, other commercial solutions are available, as the use of the module Resiscope, manufactured by Scientec [240]. In this case, Resiscope allows the current to be measured from pA to mA in a single test. Fig.2.5 shows the schematics of a Resiscope connected with an AFM [241]. A DC voltage is applied between the sample and a conductive AFM tip when the tip is scanning in contact mode, and simultaneously to the topography, the Resiscope measure the sample resistance or current through the High Performance Amplifier (HPA) in a wider current dynamic range. In this thesis, standard CAFM and a Resiscope were used for the electrical measurements at the nanoscale. Resiscope was especially suitable for RRAM measurements, because the current difference between the HRS and LRS can be of several orders of magnitude.

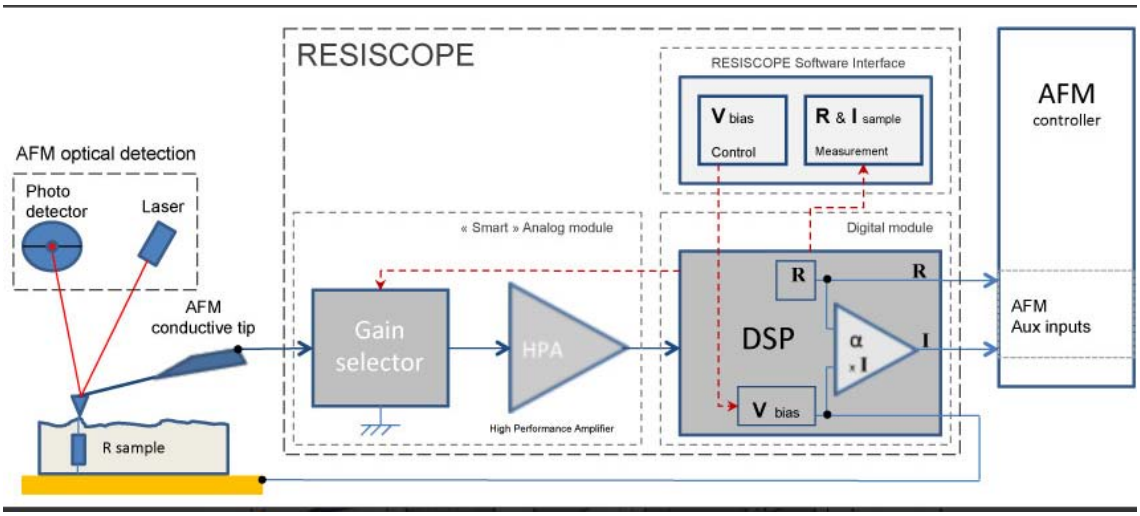


Fig. 2.5. Schematic of working principle of a Resiscope connected with an AFM.

2.4 AFM Probes

The electrical and mechanical characteristics of the tips are critical to obtain reliable results when investigating samples with an AFM, as on them depend the lateral resolution of both the topographical and current maps. As mentioned in Section 2.2, the tip is located at the end of a cantilever. Both the tip and cantilever can show different shapes, dimensions or composition, depending on the final use as operation mode, environmental conditions and analyzed sample.

2.4.1 Basic Concepts of CAFM Tips

AFM tips are modeled as a cone with a semi-sphere at its apex (Fig.2.6a) [242, 243]. The curvature radius, R, is defined as the radius of the semi-sphere located at the apex and determines the limit to detect structures with lateral dimensions (lateral resolution) in the order of the tip diameter (Fig.2.6b) [243]. Therefore, the tip radius, R, defines the resolution of the tip. On the other hand, the half cone angle, θ (Fig.2.6a), indicates the ability to image steep side-walls (Fig.2.6c) [243]. Therefore, the quality of an AFM image strongly depends on the shape and size of the tip, since it is a convolution between the real topography and the tip geometry. To get high resolution images, small curvature radius and half-cone angles are required.

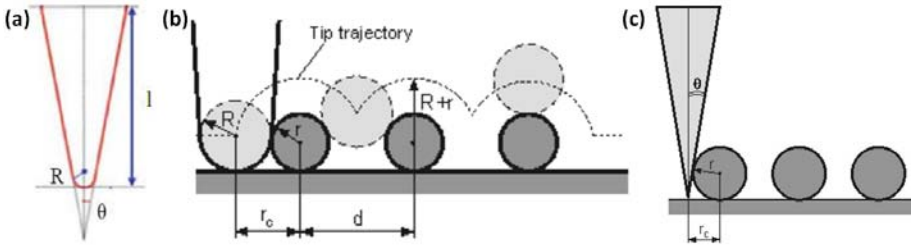


Fig. 2.6. (a) Geometrical cross-section of a tip, with a finite length l, half-cone angle θ, and spherical apex radius R. (b) Influence of the curvature radius to detect structures. A smaller tip radius leads to a better AFM resolution. (c) Influence of the half-cone angle to image steep side-walls. Smaller θ leads to a better definition of top side walls.

Another important issue which should be taken into account is that the fabrication materials (including coating layers, if any) can determine the properties of tips.

According to different AFM applications, different materials are required. For example, in CAFM experiments, conductive tips are required. Fig.2.7 [244] illustrates SEM images of different kind of tips used in this thesis: a) PtIr coated Si tips (with a nominal radius < 20 nm), b) diamond coated Si tips (with a nominal radius of 150 nm), c) bulk Pt tips (with a nominal radius of 20 nm) and d) silicon tips (with a nominal radius of 10 nm), which can only be used for topographical measurements.

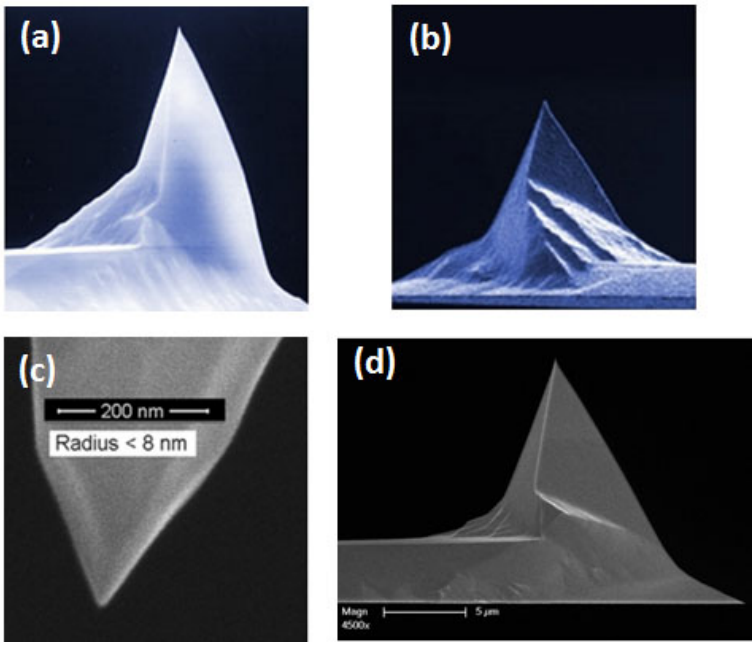


Fig. 2.7. SEM images of a) PtIr coated Si tips, b) diamond coated Si tips, c) bulk Pt tips and d) silicon tips.

2.4.2 Analysis of the Tip-Sample System Resistance

Regarding the CAFM measurements, tip material must be very resistant from a mechanical point of view, and conductive. However, the tip-sample contact generally exhibits certain parasitic resistances, which can affect measurements especially when conductive samples (of low resistances) are studied (for example, graphene layers). In this case, the resistances involved in the tip-sample system and their variations as the measurement proceeds (due to tip wear out) should be estimated.

When the tip contacts the surface, a widely used common model that includes most of the resistances that come into play in the tip-sample system considers of the following components: the sample resistance to be measured, R_{sample}, the parasitic

tip resistance, R_{tip} [245], a contact resistance between the tip and sample, $R_{contact}$, and the resistance between the sample and back contact, R_{back}. R_{tip}, R_{back} and $R_{contact}$ should be avoided or, at least, somehow controlled and/or kept constant to avoid variations in the same set of experiments. R_{back} could be considered very small and constant, since the contact of the sample with the sample holder can be assumed not to vary. However, R_{tip} and $R_{contact}$ cannot and will be discussed in the next sections.

Contact Resistance

The contact resistance between the tip and the sample, $R_{contact}$, cannot be measured and isolated from the others because it depends on many parameters that the user is not able to monitor precisely. In particular, $R_{contact}$ is influenced by the materials itself (sample specific resistance, airborne contaminations, insulating layers), the applied voltage, the force applied between the tip and sample, the presence of a water meniscus and tip characteristics itself (as the size of the contact area, which depends on the tip radius, thickness of the coating, etc). $R_{contact}$ could be estimated by measuring I-V curves on a reference sample (like a gold layer) with a known resistance. However, this procedure is not effective since $R_{contact}$ can change from one sample (reference sample) to another (the sample of interest).

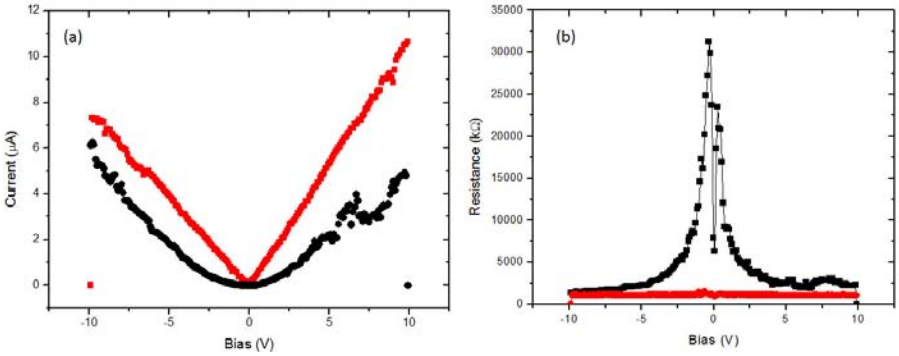


Fig. 2.8. Example of two I-V curves (a) and the corresponding resistance (b) measured with the Resiscope and a Pt coated tip on a gold contact in series with a 1 MΩ resistance. Only the red one shows a perfect ohmic contact.

However, $R_{contact}$ can be minimized by applying high pushing force to the tip (to move it closer/deeper against the sample surface) leading to a larger contact area and making the tip-sample contact more of an ohmic or Schottky-type (depending

on the materials), although it leads to a fast tip wear out (and its eventual breakdown). If the pushing force is not sufficient, the tip-sample contact may remain only partially ohmic/Schottky and a tunneling current component may also be present. As an example, Fig.2.8 shows an example of two I-V curves (a) and the corresponding resistance (b) measured with the Resiscope and a Pt coated tip on a gold contact in series with a 1 MΩ resistance. Note that meanwhile the red curve shows a nearly perfect ohmic contact, the black one doesn't, probably due to some organic contamination, bad contact, etc.

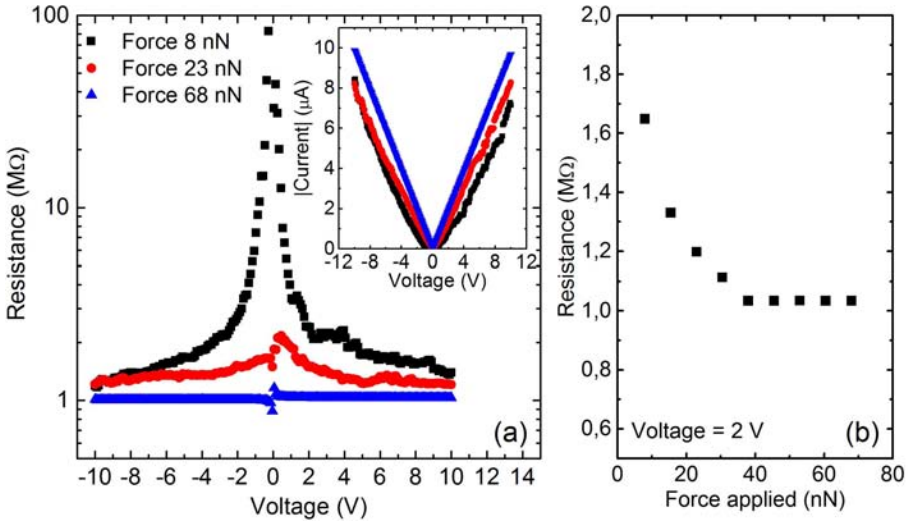


Fig. 2.9. (a) Example of R-V curves measured with the Resiscope and a Pt coated tip over a gold contact, in series with a 1 MΩ resistance, by applying different contact forces. The inset shows the I-V curves from which the R-V curves were extracted. (b) Resistance measured when different forces are applied to the tip (selected by the user) at 2 V.

Fig.2.9a shows another example of three R-V curves (the inset shows the I-V data used to obtain the R-V curves) measured using AFM and the Resiscope with a Pt bulk tip on a gold layer in series with a 1 MΩ resistance. The I-V measurements were performed by applying different set points, which is proportional to the applied force (from 8 to 68 nN). In this case, since R_{tip} is $\leq$ 5 KΩ, R_{tip} can be neglected and, therefore, the effect of $R_{contact}$ + R_{sample} is measured. Note that while applied high forces lead to a nearly perfect ohmic contact in this case (because tip and sample are metals), with an overall resistance of 1 MΩ (as expected), the measured resistance (which corresponds to the contact resistance) at lower forces is much higher, especially at low voltages. $R_{contact}$ is reduced with increasing the force applied to the sample as shown in Fig.2.9b. In this case, the current

was measured at 2 V on the same sample by applying different forces. From the measured current, $R_{contact}$ + R_{sample} is plotted in Fig.2.9b versus the applied force.

To conclude, the contact resistance is very sensitive to experimental conditions. To minimize variations of the contact resistance and contact area, the tip should be engaged by applying high force between the tip and sample and keeping it constant. In the case shown in Fig.2.9, this is achieved when forces above 40 nN are applied.

Tip Resistance

The current measured by CAFM cannot only depend on the contact resistance, but also on the tip resistance. Tip resistance, Rtip, can change as the measurements proceed, that is, as the tip wears out. When standard tips for CAFM measurements (such as doped diamond and metallic coated Si tips) are used, tip wear out can lead to changes in its resistance affecting the experiments [246].

Fig.2.10 shows some examples of I-V curves obtained at random position of the sample at, first, 150°C, second, 100°C and third, 50°C. Note that, as the temperature decreases, the conductivity of the analyzed spots is reduced. However, this tendency could also be observed when the same experiment was performed but, this time, increasing the temperature (that is, first at 50°C, second at 100°C and third at 150°C). From these results it can be concluded that the conductivity reduction observed as temperature changes (increasing or decreasing) cannot be only related to the temperature itself but to other factors as tip conductivity wear out: tip wear out can affect to the conductivity measurements even more than the temperature itself. A possible solution to this problem would be assessing the change of the tip resistance as the experiment proceeds by measuring it on a conductive reference sample. However, since various sources of parasitic resistances, such as $R_{contact}$, cannot be measured and isolated from each other, this procedure to estimate and correct the tip wear-out, although feasible, would not provide all the parasitic resistance contributions. Therefore, we propose using more durable tips such as bulk metallic tips. Since the reduction of tip conductivity is mostly related to a mechanical wear-out of the tip coating (in standard CAFM tips), this effect is minimized when bulk conductive tips, such as Pt tips, are used. Experiments

performed with Pt tips (with a force constant of 8 N/m, in order to get a good and stable mechanical contact with the sample) have shown that very large areas can be scanned without changing significantly their conductivity.

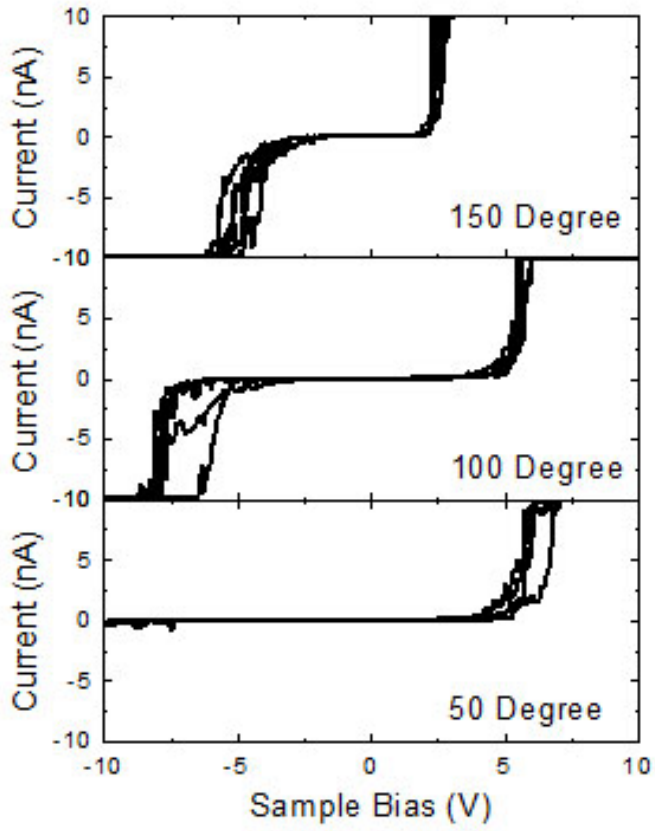


Fig. 2.10. Example of I-V curves obtained at different temperatures and random positions of the sample.

2.5 Calibration of the Temperature Controller

The measurement of the electrical properties of a given gate oxide at different temperatures can also provide additional information. As an example, in Section 3.3, the conduction through SiON-based samples at different temperatures is studied. However, a calibration of the system that controls the temperature must be firstly performed. In this thesis, and before the experiments shown in Section 3.3, the temperature controller was firstly checked and calibrated to make sure about which is the real temperature applied to the sample.

In our case, a Lakeshore 331 Temperature Controller is used to heat the sample plate. Fig.2.11 shows the optical image of the sample plate used in this thesis with a sample holder and a conductive tap over it. The conductive tap usually is made by copper, silver and carbon to stick the sample on the sample holder. Since the top surface of the sample is far away of being in contact with the sample plate, the real temperature of the sample surface, T_{Cu-S}, will be probably different from the temperature set in the controller by the user, T_{set}. Therefore, before measurements, the system was calibrated in order to obtain which temperature the user must set in the controller, T_{set}, to heat the sample at a temperature, T_{Cu-S} of interest.

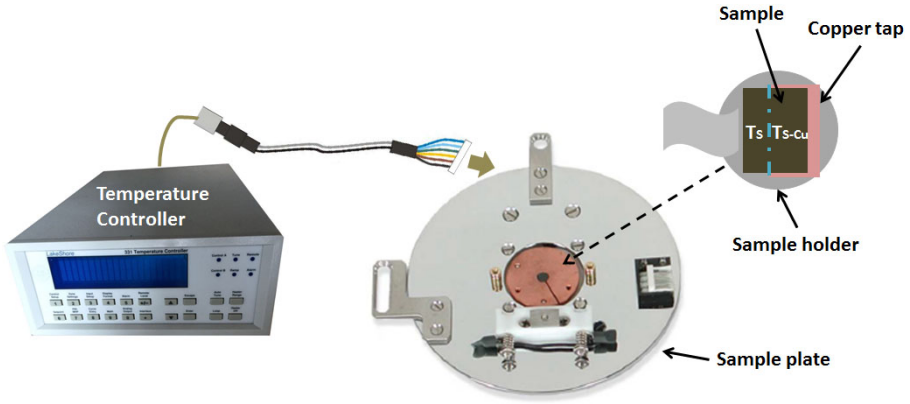


Fig. 2.11. Optical image of the sample plate used in this thesis and a sample holder with a conductive tap over it.

To do so, an infrared camera was used to measure the temperature of the sample surface comparing with the temperature set in the controller. The sample was stuck to the sample holder by a copper tap (Fig.2.11). The calibration was done in air and using four different temperatures. For each temperature set in the controller, the temperature of the sample surface was measured by the infrared camera. Two different samples were used. Sample 1 consists of a 6 nm thick HfO_2 gate oxide over silicon substrate, and sample 2 consists of a stack of III-V semiconductors. The measured temperatures are shown in Table 2.1. T_{set} represents the temperature set in the controller by the user, T_{Cu} represents the temperature of the copper surface and T_{Cu-S} and T_S represents the average temperature of the part of sample surface which is over the copper and not, respectively (Fig.2.11). In Fig.2.12, the measured temperature on the sample surface when it is in contact with the copper tap for both samples is plotted versus T_{set} (symbols).

°C	Sample 1				Sample 2			
T_{set}	71.7	95.5	142.6	191.9	70	95.7	143.8	195
T_{Cu}	69.6	93.5	143.1	191.6	69.1	95.1	143.3	196.4
T_{Cu-S}	55.6	79.2	120.8	156.6	53.8	76.4	117.9	160
T_S	50.8	67.2	102.4	138.5	48.7	67.3	101.7	139

Tab. 2.1. Temperatures measured by infrared camera on Sample 1 and Sample 2. T_{set} represents the temperature set in the controller by the user, T_{Cu} represents the temperature of the copper surface, T_{Cu-S} and T_S represents the average temperature of the part of sample surface which is over the copper and not, respectively.

Table 2.1 shows that the temperature on the copper tap is generally the same as the one that has been set, demonstrating that the used copper tap has a good thermal conductivity. Note also that since the thermal conductivity (which strongly depends on materials) of the samples is lower than that of copper, the temperatures of samples, T_{Cu-S}, are lower than the temperature of copper surface. Moreover, when the sample is not fully over the copper tap, the temperature of the surface, T_S, is even lower. As an example, Fig.2.13a and b show the optical image of the set up and corresponding infrared image after heating 5 min Sample 2 with a temperature of 200°C. Through Fig.2.13b, it is obviously observed two level of temperature over the sample: the higher one, T_{Cu-S}, on the Cu tap, and the lower one, T_S, on the part of the sample not in contact with the Cu tap. Therefore, it is important that the measuring part of sample should be over conductive tap during the CAFM measurements. Finally, as the temperature increases, the difference between T_S and T_{Cu-S} increases.

Note also that the differences observed between the two samples are small. The plot of T_{Cu-S} versus T_{set} shown in Fig.2.12 has been used to determine the dependence of both parameters, finding a linear behavior in the form of:

$$T_{Cu-S} = aT_{set} + b \tag{2.1}$$

where in Sample 1, a_1 is 0.8389, b_1 is -2.175°C and r_1 is 0.99806; in Sample 2, a_2 is 0.8497, b_2 is -5.150°C and r_2 is 0.9999. The r is quite approaching to 1, which indicates it fit the linear behavior. Moreover, the two parameters are similar which means that this behavior does not too much depend, at least on the samples used in this thesis.

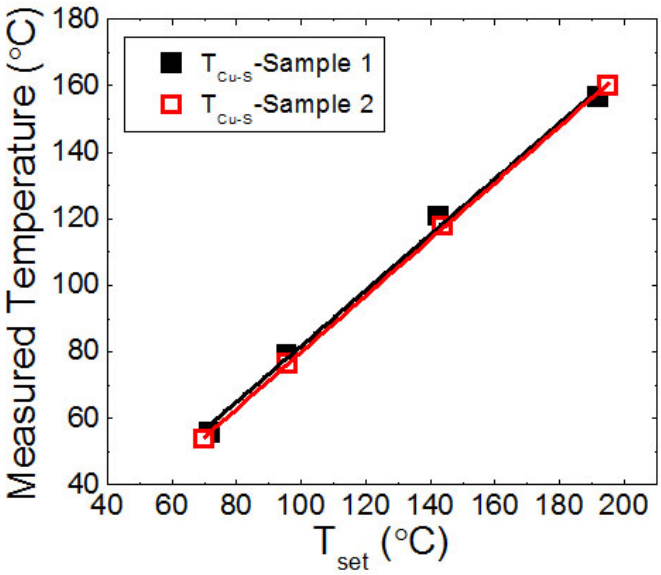


Fig. 2.12. T_{Cu-S} of Sample 1 (black, solid) and Sample 2 (red, open) and their linear fittings are plotted versus T_{set}.

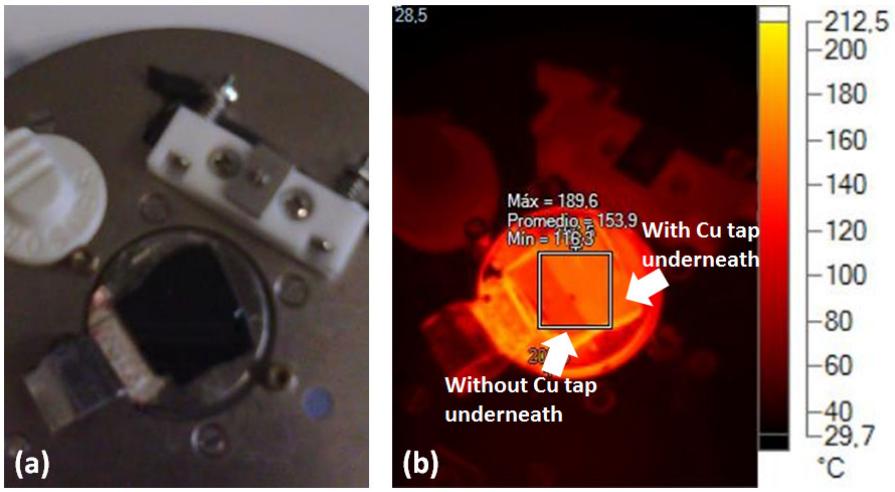


Fig. 2.13. Optical (a) and corresponding infrared (b) images of a sample on the sample plate with a temperature setting of 200°C, in (b), sample with (left) and without (right) Cu tap underneath show different color which indicates two levels of temperature.

So, to conclude, we have demonstrated that, although the sample plate reaches the T set by the user, the top surface of the sample doesn't. We observed that it is very important that the whole sample must be stuck over the copper tap to set a good thermal conduction. In this case, a linear relationship between T_{Cu-S} and T_{set} has been found, which does not too much depend on the samples that have been used in this calibration process.

Chapter 3

Negative Bias Temperature Instability, Channel Hot-Carriers, and Random Telegraph Noise Degradation in Strained and Unstrained MOSFETs

In Chapter 1 it was introduced that electrical stresses can trigger different aging mechanisms (as BTI and CHC degradation), which affect the electrical properties of CMOS devices. Moreover, the impact of Random Telegraph Noise (RTN) on device performance is becoming essential as the voltage supply is continuously decreasing, being especially critical for those devices working near/under the sub-threshold region [247]. Considering the electric field distribution in the device during BTI and CHC stresses, the oxide damage is expected to be uniformly distributed over the gate oxide area for BTI aging, whereas it should be mostly located close to the drain for CHC degradation. The CHC non-uniform aging has been experimentally evidenced by the different measured values of the drain current when the roles of source and drain are interchanged during device tests [120]. Moreover, when strain is introduced in MOSFETs to improve the channel carrier mobility, they are more sensitive to CHC and NBTI degradation than unstrained

ones [152]. Note that, in all the cases mentioned before, NBTI, CHC, and RTN impact on the device performance is related to defects that are already present in the device or that have been generated during the stress. However, most of the studies until now have been performed at device level, that is, measuring I-V data of the whole device. Since defect generation is a very local phenomenon that takes place in nanoscale areas, high resolution techniques as Conductive Atomic Force Microscopy (CAFM) can be very useful to investigate how different stresses and RTN affect the electrical properties of gate stacks. Working on a bare gate oxide without top electrode, the conductive tip of CAFM plays the role of the gate electrode, defining a MOS capacitor with an area that corresponds to the contact region between the tip and the sample [209]. Because this area is very small (it has been experimentally estimated to be $\sim$100 nm^2 [209]), the technique opens the possibility to perform a nanoscale electrical characterization of the gate stack properties with a resolution of $\sim$10 nm. Some studies on the gate oxide aging under electrical stress have been already performed, but most of them use the AFM tip as the gate electrode for stressing and aging monitoring [209, 248–252]. Nonetheless, due to experimental limitations, few works have combined device level stresses and nanoscale characterization to analyse the impact of such stresses on the nanoscale gate oxide properties [253–256]. The combination of both analyses is especially difficult because once the device is stressed and its electrical properties are analysed, the structure under investigation must be reprocessed to expose the gate oxide to the CAFM tip. Therefore, many experimental difficulties may appear. In this sense, the studied structures should allow an easy gate electrode removal and should have the proper dimensions for the scanning of the whole gate area of the device. Such experimental difficulties are especially remarkable in the case of MOSFETs. As a consequence, the few studies performed in this direction have been focused on MOS capacitors and, therefore, these works are restricted to stresses that are uniform over the gate active area [255] such as BTI. In this chapter (**PUBLICATION 1-2**), the electrical properties of unstrained and strained MOSFETs after NBTI and CHC stresses have been studied by combining device level and nanoscale tests with CAFM. This chapter will be also devoted to study leaky spots and their electrical properties on as-grown (before any electrical stress) MOSFETs at the nanoscale with CAFM and at different temperatures (T), which will be related to RTN phenomenology.

3.1 A Nanoscale Analysis of NBTI and CHC Degradation in MOSFETs

In this section, the impact of differnt electrical stress on device level and nannoscale electrical properties of the unstrained MOSFET gate dielectric has been studied. Using a Conductive Atomic Force Microscope (CAFM), the gate oxide has been analysed after bias temperature instability (BTI) and channel hot-carrier (CHC) stresses. The CAFM explicitly shows that while the degradation induced along the channel by a negative BTI stress is homogeneous, after a CHC stress different degradation levels can be distinguished, being higher close to source and drain (**PUBLICATION 1**).

3.1.1 Experimental

In this section, pMOSFETs (L = 1 μm and W = 0.5 μm) with a 1.4 nm thick SiON layer as gate dielectric have been analysed. The gate electrode consisted of a 60 nm thick layer of polysilicon and a 40 nm thick layer of NiSi (Fig.3.1a). Some devices were subjected to NBTI stress by applying -2.6 V at the gate, and others were subjected to CHC stress by applying -2.6 V at the drain and gate, while the other terminals were grounded. In both cases, the stress time was 200 s. Other transistors, acting as a reference, were not stressed. The stresses and device level characterization was performed by a semiconductor parameter analyser (SPA), Keithley 4200. In the case of CHC stress, the voltage configuration (V_G = V_D) is the most damaging stress condition for p-MOSFETs [116, 257] because it provokes a larger hole injection into the oxide [116]. A current compliance of 1 mA was fixed during the stress.

Once the device level stress (NBTI or CHC) was applied, and the device aging characterized, the polysilicon and NiSi layers on top of the gate dielectric were removed for the CAFM analyses (Fig.3.1b). This removal was carried out using a very selective wet etch, allowing exposure of the upper surface of the gate dielectric to the CAFM tip. During the etching, the device was immersed in an 85% phosphoric acid solution, at a temperature of 125°C, for 90s [258]. After the etch-

ing, the gate oxide was scanned with the AFM tip with the purpose of investigating its morphology and comparing it to other results in literature [259]. Fig.3.2a shows a typical 3D topography map obtained for a MOSFET. Note that the gate region can be easily distinguished and measured between the two spacers. However, the presence of such sidewall spacers limits the possibility of measuring at the extreme edges of the channel (< 0.1 or > 0.9 μm) because they impede the CAFM tip (which has a conical shape) contacting the gate area (Fig.3.2a). Fig.3.2b shows a 2D topographical map of a MOSFET after etching [260] and Fig.3.2c shows a topographical profile of a MOSFET where it can be observed that roughness is in this range of < 0.2 nm and that variations on the oxide thickness are actually very small and randomly located along the channel. That roughness is comparable with values reported in [254]. This value demonstrates that the gate oxide is not affected by the removal of the top electrode. In addition, it is important to note that although the etching process could somehow affect the gate dielectric, because all samples were subjected to the same etching, similar effects should be observed in all the studied MOSFETs (fresh and stressed).

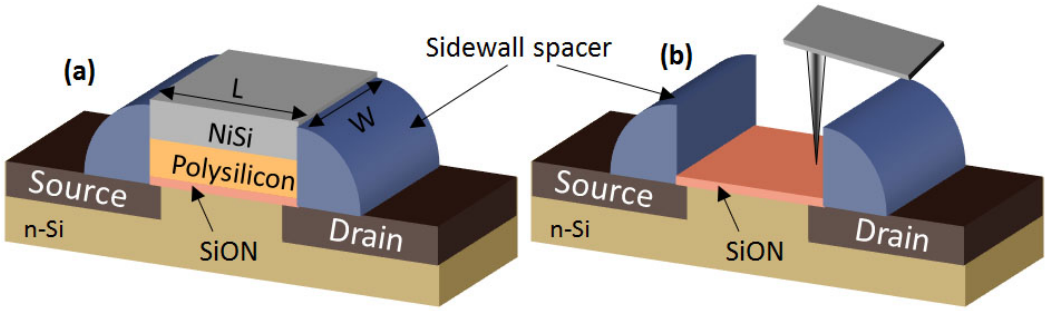


Fig. 3.1. Schematics of p-MOSFETs before (a) and after (b) removal of the top gate electrode.

The nanoscale electrical properties of the dielectric were studied by scanning the bare gate area with the CAFM tip (Fig.3.2). PtIr-coated Si tips with a nominal tip radius of 20 nm were used. When the structure is polarized, current can flow through the gate, and the electrical properties of nanometre sized regions of the dielectric can be evaluated. To avoid anodic oxidation [205, 206], we positively polarized the tip (substrate injection of negative charge carriers) and carried out the CAFM measurements in dry nitrogen ambient, keeping the humidity level inside the AFM chamber below 0.5%. It should be mentioned that maximum currents of 10 nA can be measured due to the saturation of the electronics of the setup. An important

point that should be emphasized is that when performing conductivity measurements with CAFM, the currents measured with this technique are very sensitive to several experimental factors. These factors are related to the contact area between the tip and the sample and the resistivity of the tip, which can vary from tip to tip and even during the measurements due to the tip wear out or the average thickness fluctuations between samples. Therefore, the comparison of absolute values of the currents measured in different samples may not be really meaningful unless, for example, the same tip and experimental conditions were used, so only relative variations in the same sample are fully reliable. Consequently, in this section, we will focus on the conductivity variations along the channel for a given sample.

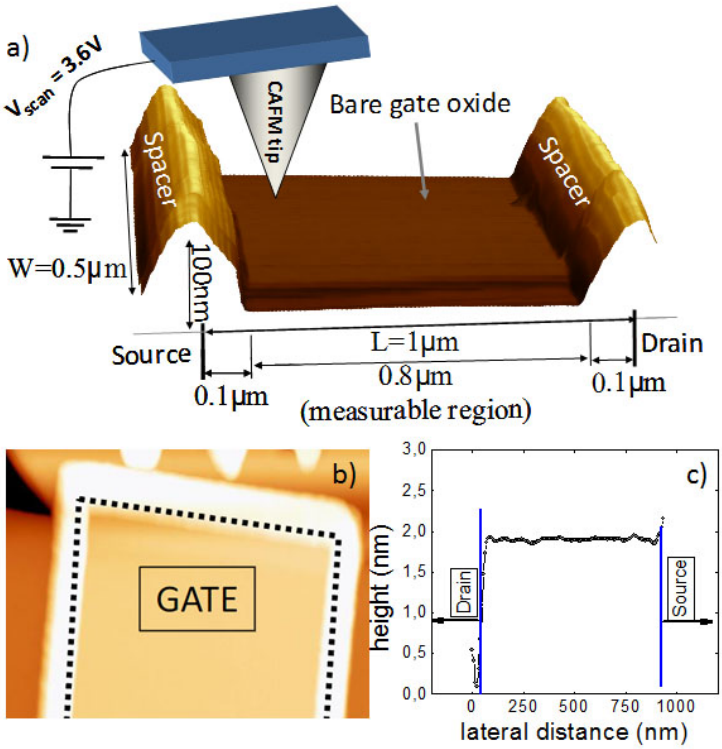


Fig. 3.2. (a) Schematics and AFM 3D topographic image of a p-MOSFET after the removal of the gate electrode. The dimensions of the area under study and the applied polarization voltage are indicated. (b) Example of a 2D topographic map of a MOSFET after etching. (c) A topographical profile of a MOSFET where it can be observed that roughness is in this range of < 0.2 nm. These variations on the oxide thickness are very small and randomly located along the channel.

3.1.2 Electrical Characterization at Device Level

The device level electrical properties of MOSFETs were studied from the measurements of I_D-V_D, I_D-V_G, and I_G-V_G curves before and after NBTI and CHC stresses. Fig.3.3a-c shows typical I_D-V_D, I_D-V_G, and I_G-V_G characteristics obtained before (continuous line) and after a NBTI (open symbols) and CHC (solid symbols) stress. Note that after the stress, I_D is smaller and I_G increases (being this reduction/increment larger in the case of CHC stressed device). The characterization after the stress revealed a threshold voltage shift of 25 mV for NBTI stress and 125 mV for CHC stress with respect to non-stressed devices. The threshold voltage was estimated from the maximum slope of the I_D-V_G curves. In addition, a decrease of 4% for NBTI stress and 19% for CHC stress in the drain current at V_D = -1.2 V and an increase of 4% for NBTI stress and 227% for CHC stress in the gate current at V_G = -1 V was observed. The breakdown voltage, V_{BD}, was also determined from the I_G-V_G characteristics obtained after the application of ramped voltage stresses to the gate of some MOSFETs (Fig.3.3c). Fig.3.3d shows the Weibull plot of the voltage to breakdown (V_{BD}). The voltage to get a 63% probability of BD occurrence [V_{BD} (63%)] was determined to be 3.8 V.

3.1.3 Electrical Characterization at the Nanoscale

Several devices before and after the electrical stress (NBTI and CHC) have been studied at the nanoscale with the CAFM. Four unstressed, five NBTI- and nine CHC-stressed MOSFETs have been measured. Fig.3.4a-c shows, respectively, examples of typical current maps (on the same current scale, 25 pA) obtained on reference (non-stressed), NBTI- and CHC-stressed MOSFETs, where the gate area that could be measured with the CAFM tip has been delimited by a dotted line. In all cases, current images were obtained by applying +3.6 V to the tip (substrate grounded). This voltage is high enough to be able to measure current above the noise level of the setup, but low enough to avoid the breakdown of the gate stack (see Section 3.1.1). Although this voltage could induce an additional stress to the gate oxide, the differences observed between the three images of Fig.3.4 should be attributed to the device level stress and not to the AFM scan, because all devices (reference, NBTI- and CHC-stressed MOSFETs) were scanned under the same

conditions.

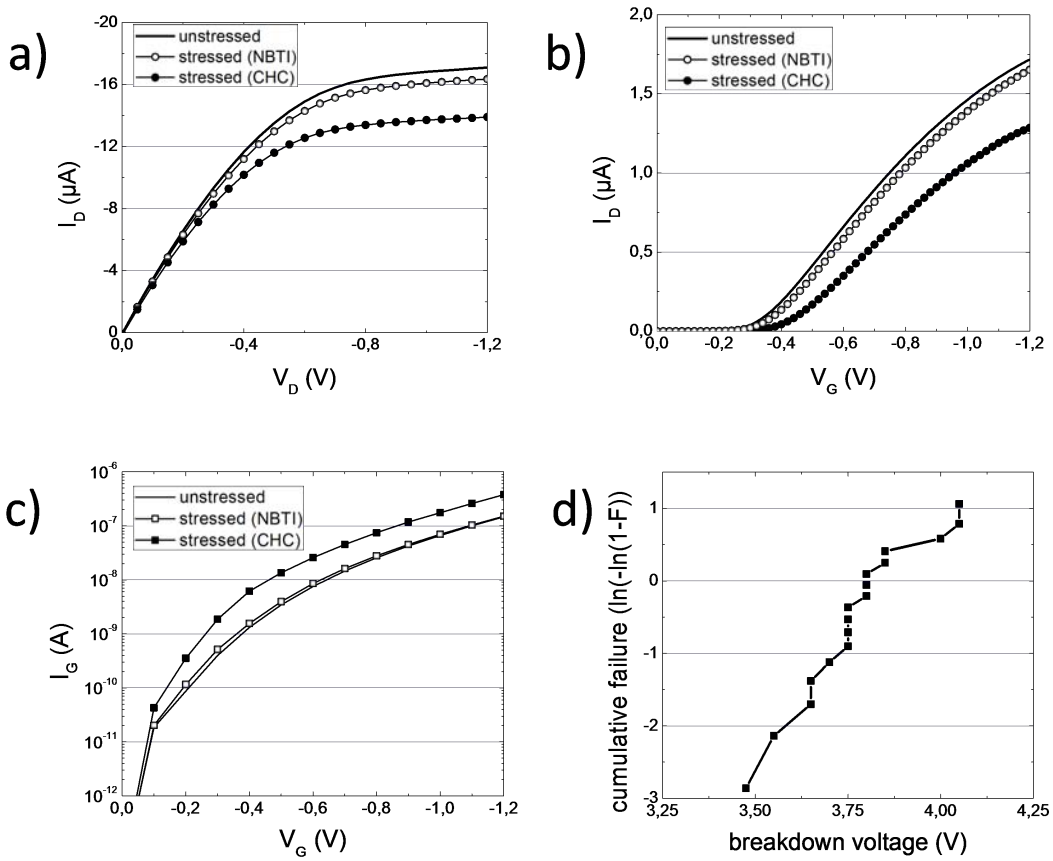


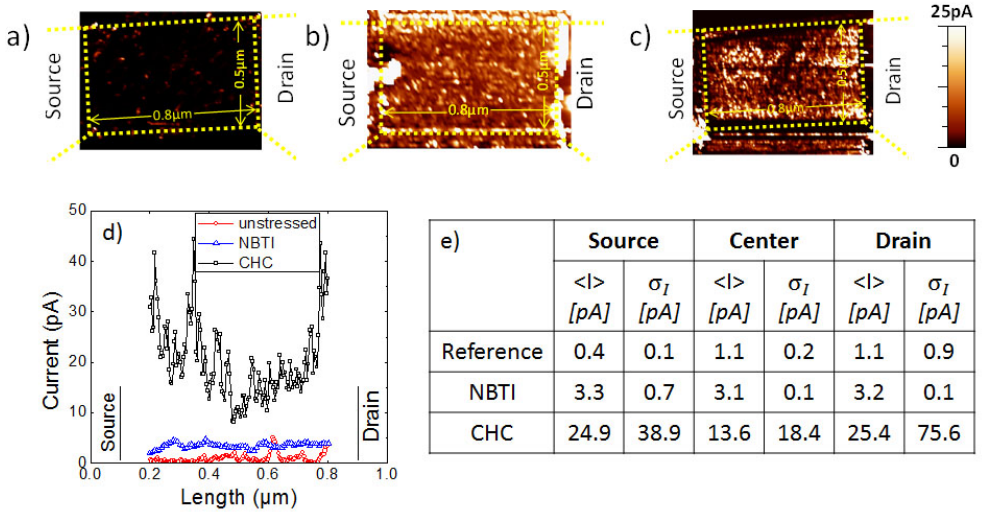
Fig. 3.3. Typical I_D-V_D (a) I_D-V_G (b) and I_G-V_G (c) characteristics of a MOSFET recorded before (continuous line) and after NBTI (open symbols) and CHC (full symbols) stress. (d) Breakdown statistics from which V_{BD} (63%) was estimated.

In the unstressed samples (Fig.3.4a), currents corresponding to the noise level of the setup ($\sim$pA) are measured, which indicates that the conductivity of the fresh sample could be even smaller. However, in all the stressed (NBTI and CHC) MOSFETs, brighter areas, representing larger currents (which correspond to leaky sites in the dielectric) were observed. The comparison of the images in Fig.3.4a (non-stressed sample) with the images in Fig.3.4b (NBTI stressed sample) and Fig.3.4c (CHC stressed sample) allows the conclusion that: 1) the number of leaky sites in the stressed MOSFETs is considerably larger than in non-stressed devices and 2) the distribution of leaky sites over the gate region can change after applying the stress.

The images shown in Fig.3.4a-c have been quantitatively evaluated in Fig.3.4d and e. Fig.3.4d shows the averaged current profiles obtained with the CAFM tip at

different positions along the channel for the non-stressed (circles) and NBTI (triangles) and CHC (squares) stressed MOSFETs. Since the comparison of the current absolute value between samples is not completely meaningful, we will focus on variations within the same sample only. In the unstressed sample, the current is close to the noise level of the CAFM and homogeneously distributed along the channel. The stressed MOSFETs (triangles and squares) always show larger currents than the non-stressed device. In this case, the difference is so large that it can be easily detected. However, a difference between NBTI- and CHC-stressed MOSFETs can be observed: the former always shows a homogeneous distribution of the current along the channel, whereas in CHC-stressed MOSFETs larger gate currents can be measured in the regions close to the junctions. The table in Fig.3.4e, which shows the RMS value, σ_I , and average current, <I>, measured in a W $\times$ 0.05 μm^2 region in Fig.3.4a-c, located close to the source, close to the drain, and at the centre of the channel of the three MOSFETs, further supports these observations. Note that in the CHC-stressed MOSFET, the current close to the source and drain is higher than in the centre of the channel and also shows a higher dispersion. However, in unstressed and NBTI-stressed MOSFETs, the current distributions are more homogeneous, although a larger dispersion was measured after the NBTI stress.

The characteristics and spatial distribution of the leaky sites has been analysed in more detail from the current images. Randomly located leaky spots are measured on the fresh oxide, which can be assigned to currents through native defects (see Section 3.3) and/or local thinning of the dielectric [261]. On the previously stressed dielectrics, however, the number of leaky sites is larger, and they are more conductive. In this case, these spots can be considered to be related to the defects generated during the stress. In addition, because the current through the leaky spots does not reach the CAFM maximum current and the device level measurements did not show a post-BD behaviour in the gate current, they cannot be BD spots. Consequently, the current measured with the CAFM through the stressed oxides can be assumed to be indicative of the degradation induced during the NBTI or CHC stress. Therefore, the current images in Fig.3.4b and c lead to the conclusion that in the case of CHC-stressed MOSFETs, the degradation in the gate is specifically concentrated close to source and drain regions.



e)	Source		Center		Drain	
	<I> [pA]	σ_I [pA]	<I> [pA]	σ_I [pA]	<I> [pA]	σ_I [pA]
Reference	0.4	0.1	1.1	0.2	1.1	0.9
NBTI	3.3	0.7	3.1	0.1	3.2	0.1
CHC	24.9	38.9	13.6	18.4	25.4	75.6

Fig. 3.4. Typical current images obtained at a gate voltage of 3.6 V in non-stressed (a), NBTI (b) and CHC (c) stressed MOSFETs. (d) Average current measured with the CAFM tip along the channel for the non-stressed (circles), NBTI (triangles), and CHC (squares) stressed MOSFETs. (e) Table indicating the average and dispersion of the current measured in W $\times$ 0.05 μm^2 regions taken in (a-c), close to the source, drain, and at the centre of the channel. (b) to (e) clearly show the effect of the degradation induced by the previous NBTI and CHC stress, where larger currents (brighter areas) are evident for stressed devices. These brighter areas are non-uniformly distributed after CHC stress.

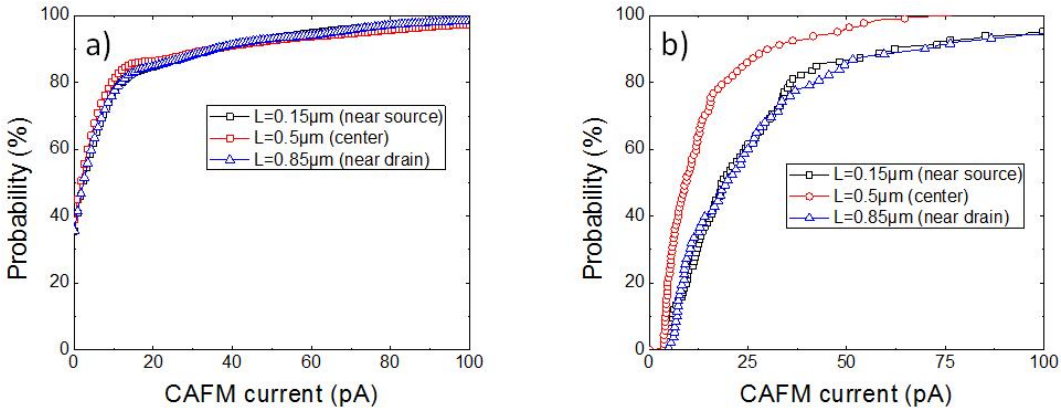


Fig. 3.5. Cumulative distributions of the current measured with the CAFM in 0.05 μm^2 regions centred close to the source (L= 0.15 μm) and drain (L = 0.85 μm) and in the centre of the channel (L = 0.5 μm), for (a) NBTI- and (b) CHC-stressed MOSFETs.

To accurately analyse the distributions of the generated defects along the channel, the cumulative distribution of currents measured in 0.05 μm^2 regions centred at channel distances L = 0.15 and 0.85 μm (i.e., close to source and drain respectively), and L = 0.5 μm (in the centre of the channel) are represented in Fig.3.5a for NBTI, and in Fig.3.5b for CHC-stressed MOSFETs. Note that in the case of the NBTI-stressed devices (Fig.3.5a), similar cumulative distributions are found in the three regions. On the other hand, after the CHC stress (Fig.3.5b), lower currents are measured in the centre, whereas larger currents are shown in the distributions measured close to the junctions. The current distributions at the extremes of the channel do not show remarkable differences between them, which indicates that a similar degradation effect is produced close to the source and drain areas. To explain this result, it should be considered that the NBTI degradation measured by CAFM is mainly due to the permanent NBTI component (several days passed between the electrical stress and the CAFM characterization). Therefore, Fig.3.5b suggests that the CHC stress and the permanent NBTI could have a similar origin, as suggested in [262], where both mechanisms were associated to the creation of interface states.

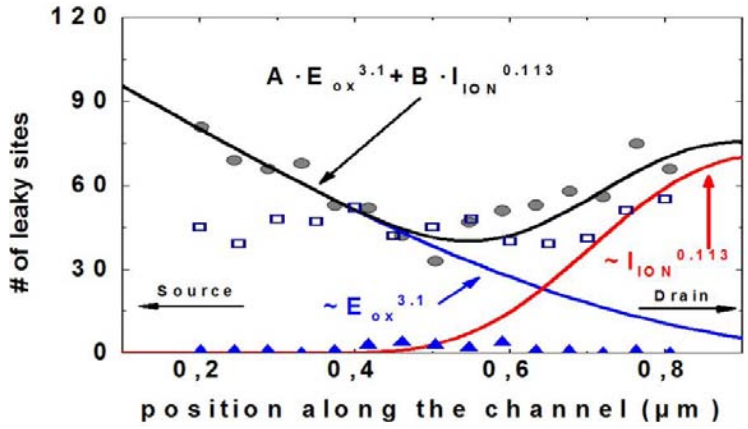


Fig. 3.6. Average number of leaky sites (CAFM current >10 pA) obtained at different positions along the channel in fresh (triangles), NBTI (squares) and CHC (circles) stressed devices, obtained from 20 current profiles registered along the channel width in the current images in Fig. 3.4. Lines correspond to the fitting of the number of leaky sites to A·E_{ox}^{γ} (blue) and B·I_{ion}^{α} (red) and their sum (black).

The number of leaky sites on reference and stressed samples has also been analysed, as determined from 20 current profiles along the channel width, extracted from the current maps of Fig.3.4. For each kind of sample (reference, NBTI- and CHC-stressed MOSFET), the profiles were obtained on the same device (Fig.3.4).

Fig.3.6 shows the average number of leaky sites that show currents larger than 10 pA versus their position along the channel. Squares and circles correspond, respectively, to NBTI- and CHC-stressed MOSFETs, while triangles show the data corresponding to the unstressed transistor. Clearly, the number of leaky sites is larger in stressed (both NBTI and CHC) MOSFETs. In addition, in the CHC-stressed MOSFET, leaky sites are mostly located close to the junctions, whereas in the NBTI stressed and fresh oxides the spots are uniformly distributed along the channel.

3.1.4 Simulation

In order to explain the experimental distribution of leaky sites observed with CAFM (circles in Fig.3.6), TCAD simulations of a p-MOSFET under the same CHC stress bias experimentally applied in Section 3.1.1 have been performed and analyzed. In particular, the potential distribution (Fig.3.7a) and the impact ionization, I_{ion}, (Fig.3.7b) at the CHC stress conditions have been obtained. The dashed rectangle in Fig.3.7a indicates the region that corresponds to the gate oxide. As expected, the potential distribution in the oxide is clearly not uniform along the channel direction. The voltage drop at the gate oxide (V_{ox}) is especially large close to the source because of the different bias applied to the gate and source terminals (-2.6 and 0 V, respectively). In contrast, V_{ox} is small close to the drain because the same voltage is applied at gate and drain terminals during the CHC stress. Consequently, the vertical electric field, which leads to the NBTI degradation, is more intense close to the source, and decreases along the channel direction from source to drain [258, 263]. The impact ionization (Fig.3.7b) reaches the maximum at a position close to the drain, where the carriers are more energetic. Hence, this position is more susceptible for the hot carrier degradation [258]. Note that the TCAD simulation allows investigating the two degradation sources during the CHC stress: 1) the high-vertical electric field close to the source and 2) the impact ionization close to the drain. Therefore, the leaky sites of Fig.3.5 located near the drain should be related to the traps created by impact ionization (I_{ion}) caused by hot carriers [116]. On the other hand, those leaky sites located close to the source should have been created by the high-electric field applied to the oxide (E_{ox}) during the CHC stress, which can induce NBTI damage as well [257]. In this case, due to the long time

elapsed between the CHC stress and the CAFM characterization (some days), the measured degradation can be related only to the permanent (or slow component) of BTI.

Therefore, the damage induced in the oxide seems to be caused by the combination of E_{ox} and I_{ion} effects. In addition, as shown in Fig.3.5b, both aging mechanisms generate a similar effect, at least from the CAFM currents point of view. These observations suggest that their contribution to the number of leaky sites could be additive. This hypothesis can be confirmed by fitting the leaky sites profile in Fig.3.5. The experimental profile is well reproduced, assuming the contribution of both mechanisms. Blue/red lines show the fit of the data to a potential law on E_{ox}/I_{ion}, that is, to $\sim {E_{ox}}^{\gamma}$ and to $\sim {I_{ion}}^{\alpha}$. For the fits, the values of E_{ox} and Iion of Fig.3.7a and b have been considered. From these fits (Fig.3.5, exponents of γ = 3.10 and α = 0.113 have been obtained [258]. The extracted γ value is consistent with exponents given in the literature for the permanent component of BTI, which ranges between 3 and 5 [264]. The black line shows that the number of leaky sites can be fitted by the sum of the two exponential laws. Then, the leaky sites profile in Fig.3.5 can be explained by the combination of permanent damage caused by NBTI in the region close to the source, and hot-carrier injection close to the drain. In addition, it confirms the degradation scheme proposed from conventional characterization techniques [116, 120], where the CHC degradation is divided in two different stress components: 1) a CHC aging component located at the drain side (pinch-off region) and 2) a BTI-component distributed between the source and the pinch-off region [116, 120]. The CAFM results show, additionally, that, at the nanoscale, from a gate oxide current point of view, the generated defects, though created by different degradation mechanisms, are not significantly different.

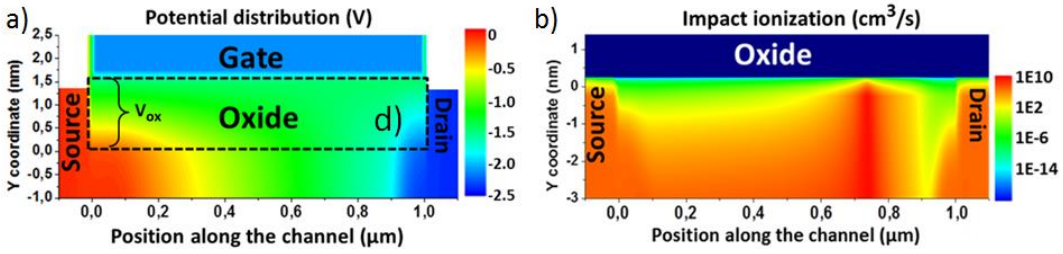


Fig. 3.7. TCAD simulation of the potential distribution (a) and impact ionization (b) for a p-MOSFET at the stress conditions used to obtain the E_{ox} and I_{ion} profiles along the channel.

To conclude Section 3.1 (**PUBLICATION 1**), a Conductive Atomic Force Microscope has been used to investigate the impact of a NBTI and CHC stress on the nanoscale electrical properties of the MOSFET gate dielectric. The high-lateral resolution of the microscope has allowed investigation of the differences of the degradation induced along the channel. The analysis has been performed by considering that the defects generated by electrical stress assist in the process of tunnelling through the gate when the tip-sample system is biased. After the stress, a larger number of leaky sites and larger currents are measured, suggesting a larger degradation in stressed devices. However, the degradation of the gate oxide area after the NBTI stress is found to be homogeneous, while in the case of a CHC-stressed MOSFET the regions close to the source and drain show a larger degradation than in the centre of the channel. This fact is indicative of the non-uniformity of the CHC stress. The TCAD simulations of the parameters involved in the CHC stress (oxide voltage drop and impact ionization) suggest that the generated defects close to source and drain can be attributed to NBTI and CHC degradation, respectively. However, although the aging mechanisms are different, from the gate oxide conductivity point of view, the generated defects have similar characteristics.

3.2 Impact of NBTI and CHC Degradation in Strained MOSFETs

In Chapter 1, it was introduced that strained MOSFETs have been proposed to enhance the channel carrier mobility. However, one concern is the possible presence of defects at the SiGe/Si interface and the larger sensitivity of strained MOSFETs to electrical stresses as channel-hot-carrier (CHC) degradation and bias temperature instability [152]. In this section (**PUBLICATION 2**), p-MOSFETs with epitaxial grown SiGe at the source (S) and drain (D) regions have been subjected to electrical stresses (Chanel hot-carrier and NBTI stresses) and their electrical characteristics have been analysed and compared to identical devices without strained channels. In particular, the impact of the stress on the drain current, I_D (measured at device level), and on the gate current, I_G, at different regions of the channel (measured at the nanoscale with CAFM) has been studied on devices with different channel lengths.

3.2.1 Experimental

p-MOSFETs as those analysed in Section 3.1 that is, with a 1.4 nm thick SiON layer as gate dielectric and 60 nm polysilicon/40 nm NiSi stack as gate electrode have been studied. In strained devices, the SiGe at S/D regions were selectively deposited with a 15% Ge content (Fig.3.8a). These devices were compared to identical p-MOSFETs without strained silicon (reference devices, Fig.3.8b). Transistors with different channel lengths (L = 0.13, 0.5, 1, and 3 μm) and 1 μm width were considered. Some samples were subjected to CHC stress by applying V_G = V_D = -2.6 V, some samples were subjected to NBTI stress by applying -2.6 V at the gate for 200 s keeping the other terminals grounded (**PUBLICATION 1**) and some others were not stressed (fresh samples). Although strain can result in lower external resistance leading to higher internal bias for the same external voltages (compared to unstrained devices), since the goal of the work is to perform a reliability comparison between the two technologies, NBTI and CHC degradation was induced at the same voltages. Using the same biases allow evaluating which technology suffers from larger degradation when operating under the same conditions.

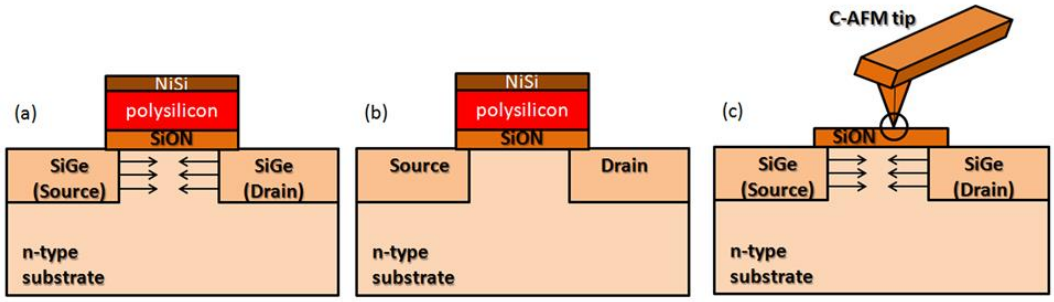


Fig. 3.8. Schematics of strained (a) and unstrained (b) p-MOSFETs measured at device level (c). Experimental configuration when the strained devices are studied with CAFM.

Before and after the NBTI and CHC stress, device level measurements were performed (to get the I_D-V_G, I_D-V_D characteristics), and the device aging was characterized. After the device level analysis, the polysilicon and NiSi layers on top of the gate dielectric were removed with a very selective wet etching as mentioned in Section 3.1.1 to expose the gate dielectric and make it accessible to nanoscale electrical measurements with the CAFM tip (Fig.3.8c). The same configuration was used as described in Section 3.1.1.

3.2.2 Device Level Analyses

In this section, the impact of an electrical stress on the current along the channel, that is, the drain current, I_D, of strained MOSFETs is going to be analysed. Since the CAFM configuration used in this thesis can only measure the gate current through the dielectric, the effect of the strain and the stress on I_D is going to be studied at device level with a semiconductor parameter analyser, Keithley 4200, and a probe station. In particular, the electrical characteristics of fresh (before any electrical stress), NBTI and CHC stressed devices have been compared on strained and unstrained MOSFETs with different channel lengths.

CHC Degradation in Strained MOSFETs

In this section, the impact of a CHC stress is analysed. Fig.3.9 shows typical I_D-V_G (a, d, and g), I_D-V_D (b, e, and h), and transconductance (g_m) (c, f, and i) characteristics of MOSFETs with a 0.13 μm (a-c), 1 μm (d-f), and 3 μm (g-i) channel length. In all plots, solid symbols correspond to strained devices and open symbols to unstrained transistors. Squares and circles correspond to fresh (unstressed) and CHC stressed devices, respectively. The I_D-V_G characteristics were measured at V_{DS} = -50 mV and the I_D-V_D curves at V_{GS} = -0.6 V. First, the effect of the strain on the electrical characteristics of fresh devices (squares in Fig.3.9) is compared. A clear increase of the drain current, I_D, is observed in strained transistors, which is attributed to an increment of the carrier mobility due to the channel strain [138]. This increase of μ is confirmed in Fig.3.9c, f, and i, which shows the transconductance (g_m) as a function of V_G for the different channel lengths MOSFETs. A larger g_m is observed in strained (solid) transistors, which indicates a higher mobility in these devices for all lengths. However, when comparing short and long channel devices, the I_D increase is much larger in short channel devices (see Tab.3.1, which shows the percentage increment of I_D, at V_D = -0.6 V, in strained MOSFETs compared to unstrained devices for different lengths, called from now on α_D). This effect could be related to the fact that the induced strain is not uniformly distributed. Near source and drain regions, the induced strain is larger and decreases as we move to the centre of the channel. As a consequence, the total strain in the channel depends on the channel length. For shorter devices, the source and drain

regions are closer, and, therefore, the strained gate region (compared to the total gate area) is larger, leading to an enlargement of the average mobility and, thus, a higher I_D [19].

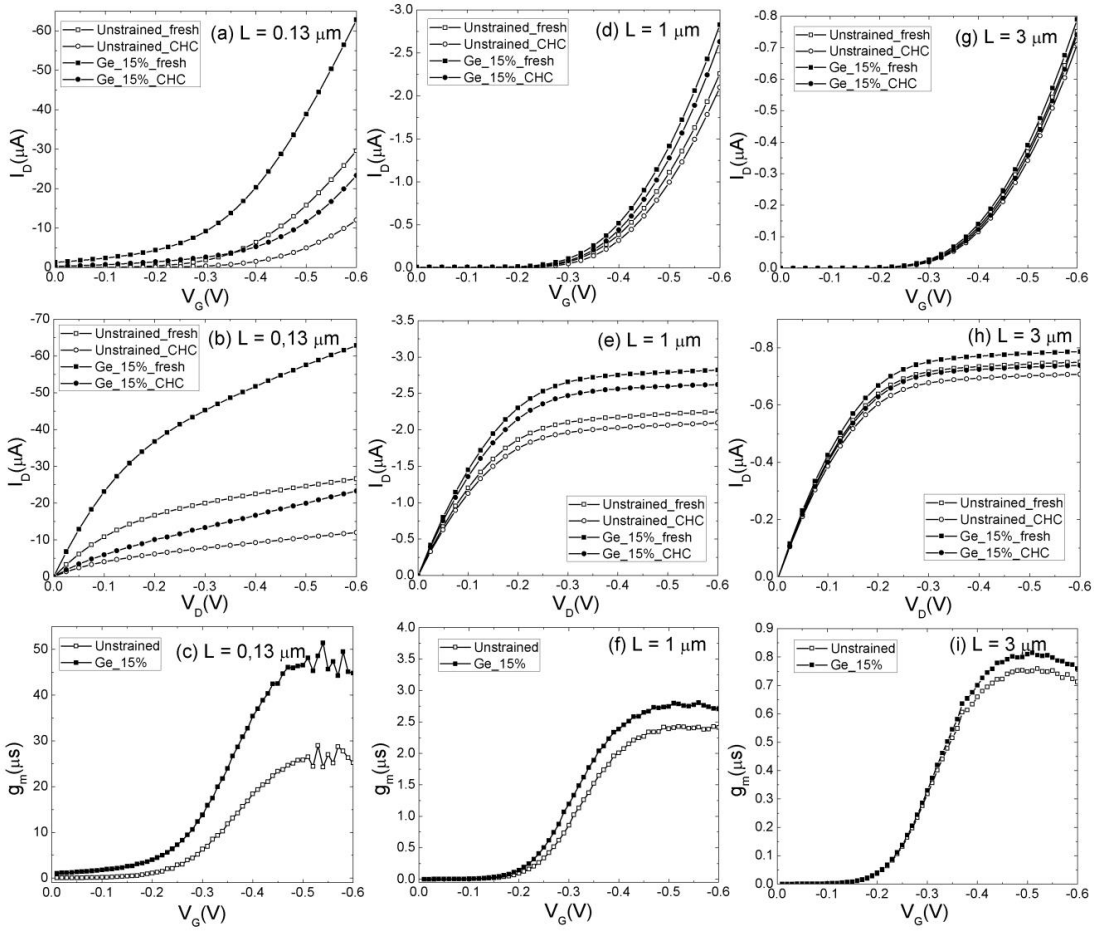


Fig. 3.9. I_D-V_G (a, d, and g), I_D-V_D (b, e, and h), and g_m-V_G (c, f, and i) curves of fresh (squares) and CHC (circles) stressed MOSFETs with strained (solid symbols) and unstrained (open symbols) channels. Channel lengths are 0.13 μm (a-c), 1 μm (d-f), and 3 μm (g-i).

	L=0.13 μm (%)	L=1 μm (%)	L=3 μm (%)
α_D	111.57	25.42	4.94
β_D	18.59	11.74	8.89

Tab. 3.1. α_D is the percentage increment of I_D in fresh strained MOSFETs compared to fresh unstrained devices for different L. β_D indicates how large is the I_D reduction (and, therefore, the CHC stress effect) in strained MOSFETs compared to unstrained devices (in percentage) for a given L.

The impact of CHC stress on both kinds of MOSFETs (strained and unstrained)

was also studied. Note that, after the stress (Fig.3.9, circles), I_D is reduced in both, strained (solid symbols) and unstrained devices (open symbols). Tab.3.2 shows the I_D reduction ($I_{D,red}$) at V_D = -0.6 V, in percentage, for the different MOSFETs. Note that the reduction depends on L and on the strain in the channel. In particular, $I_{D,red}$ is larger in strained devices (for a given L) [152], demonstrating that strained MOSFETs are more sensitive to a CHC electrical stress. When different lengths are compared, we can observe that the stress impact in short channel devices is larger, as expected, since higher electrical fields were applied along the channel. To eliminate the effect of the different stress conditions so that the strain effect is only considered, Tab.3.1 shows, for a given L (and, therefore, for the same stress conditions), how large is the I_D reduction in strained MOSFETs compared to unstrained devices (in percentage, β_D), defined as:

$$\beta_D = \frac{I_{D,red,strain} - I_{D,red,non-strain}}{I_{D,red,non-strain}} \times 100\% \tag{3.1}$$

	Unstrained devices			Strained devices		
L(Channel length)	0.13 μm	1 μm	3 μm	0.13 μm	1 μm	3 μm
$I_{D,red}$	55.37%	6.82%	6.05%	68.02%	7.73%	6.64%

Tab. 3.2. I_D reduction after CHC stress, $I_{D,red}$, in percentage, in CHC stressed MOSFETs compared to fresh devices for different lengths and substrates.

Note that in short channel devices, β_D is larger, indicating that, for the same electric field, strained MOSFETs with short channel lengths are more sensitive to a CHC stress than those with large L. This can be explained again by considering that strain affects a larger portion of the global gate area of the device. So, from this analysis, we can conclude that the drain current (I_D) measured in strained devices, although larger, is more susceptible to be affected by CHC stress: a larger decrease than in unstrained MOSFETs is observed, especially in short channel transistors.

The I_G-V_G curves have also been measured (Fig.3.10) for different channel lengths by applying a RVS to the gate while other terminals were grounded. Although there is negligible difference of I_G between strained and unstrained pMOSFETs before stress [265], it can be observed in Fig.3.10 that after CHC stress I_G is larger in strained devices (circles) than in unstrained devices (squares) with channel lengths

L = 0.13 μm (a), 1 μm (b) and 3 μm (c). These data will be considered again in Section 3.2.3, where I_G will be measured with CAFM.

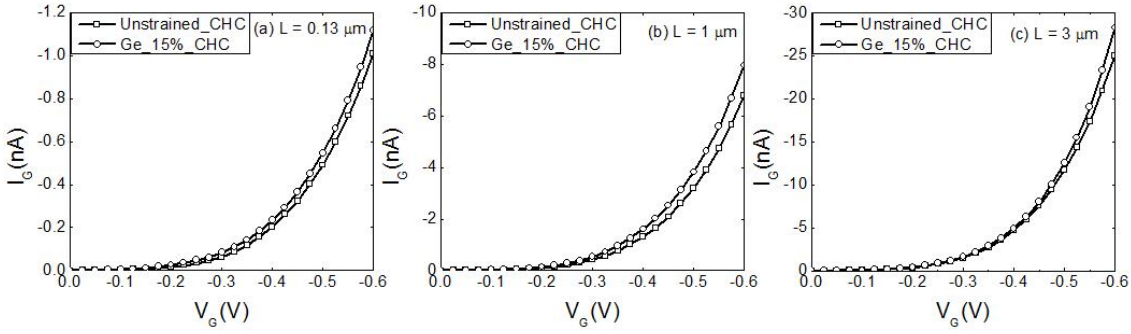


Fig. 3.10. I_G-V_G curves of unstrained (squares) and strained (circles) MOSFETs with a channel length of 0.13 μm (a), 1 μm (b) and 3 μm (c) after NBTI stress.

NBTI Degradation in Strained MOSFETs

Next, the impact of NBTI stress on the current along the channel (I_D) of both kinds of MOSFETs (strained and unstrained) was also studied. Fig.3.11 shows typical I_D-V_G (a, c, and e) and I_D-V_D (b, d, and f) characteristics of MOSFETs with a 0.5 μm (a and b), 1 μm (c and d), and 3 μm (e and f) channel length. In all plots, solid symbols correspond to strained devices and open symbols to unstrained transistors. Squares, and circles correspond to fresh (unstressed) and NBTI stressed devices, respectively. The I_D-V_G characteristics were measured at V_{DS} = -50 mV and the I_D-V_D curves at V_{GS} = -0.6 V. It is observed that there is a clear increase of drain current, I_D, in strained transistors (solid symbols in Fig.3.11), which indicates a higher mobility as mentioned above.

After a NBTI stress, a decrease of I_D is observed in both strained (solid symbols) and unstrained (open symbols) devices. Tab.3.3 shows the I_D reduction ($I_{D,red}$) at V_D = -0.6 V, in percentage, for the different MOSFETs. $I_{D,red}$ is slightly larger in strained devices (for a given L), demonstrating that strained MOSFETs are a bit more sensitive to a NBTI electrical stress. NBTI leads to a further degradation of drain current in these MOSFETs [266]. Note, however, that there isn't any significant reduction of I_D for different Ls in unstrained devices, but it slightly depends on L in strained ones. Since unstrained devices are homogenous in the entire channel, the impact of NBTI (which is also homogenous) is more or less same

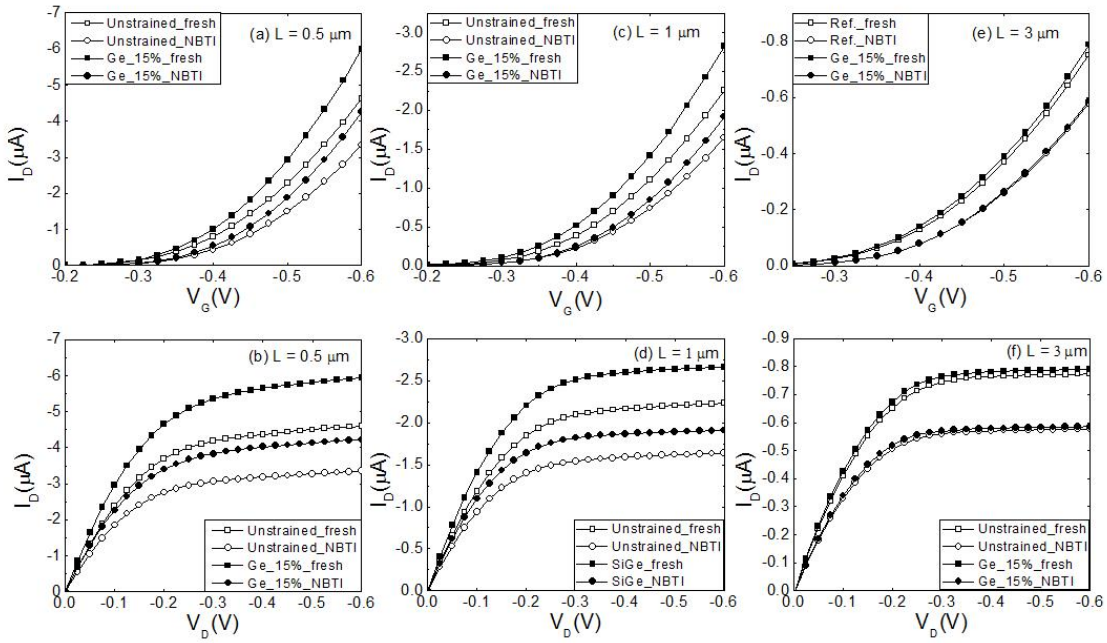


Fig. 3.11. I_D-V_G (a, c, and e) and I_D-V_D (b, d, and f) curves of fresh (squares) and NBTI (circles) stressed MOSFETs with strained (solid symbols) and unstrained (open symbols) channels. Channel length is 0.5 μm (a and b), 1 μm (c and d), and 3 μm (e and f).

for different lengths. However, since it has been demonstrated that strained areas are slightly more sensitive to NBTI than unstrained ones, this effect makes strained short channel devices a bit more sensitive to NBTI (as shown in Tab.3.3, $I_{D,red}$) than long channel ones. This is because the strained gate region is larger (in percentage) in devices with short channel.

	$I_{D,red}(\%)$		
	Unstrained	Strained	$\beta_D(\%)$
0.5 μm	26.99	29.12	7.89
1 μm	26.62	28.31	6.34
3 μm	25.48	25.90	1.35

Tab. 3.3. I_D reduction after NBTI stress, $I_{D,red}$, in percentage, in NBTI stressed MOSFETs compared to fresh devices for different lengths and substrates. β_D indicates how large is the I_D reduction (and, therefore, the NBTI stress effect) in strained MOSFETs compared to unstrained devices (in percentage) for a given L.

Note that in NBTI stresses, β_D, defined as in Eq.3.1, is also larger in shorter channel devices as expected and demonstrating again that strained devices with short L are more sensitive to this kind of stress. However, the differences between short and long devices (see β_D in Tab.3.1and 3.3) are smaller in NBTI stresses than in

CHC stressed devices. This is because CHC stress basically affects S/D regions where strain is induced and therefore those regions are more sensitive to an electrical stress, consequently in CHC stresses the differences between strained and unstrained devices should be larger. In NBTI stresses, however, since all the gate area is homogeneously affected, the weight of the degradation at S/D regions is smaller than in CHC stresses, especially when L is large.

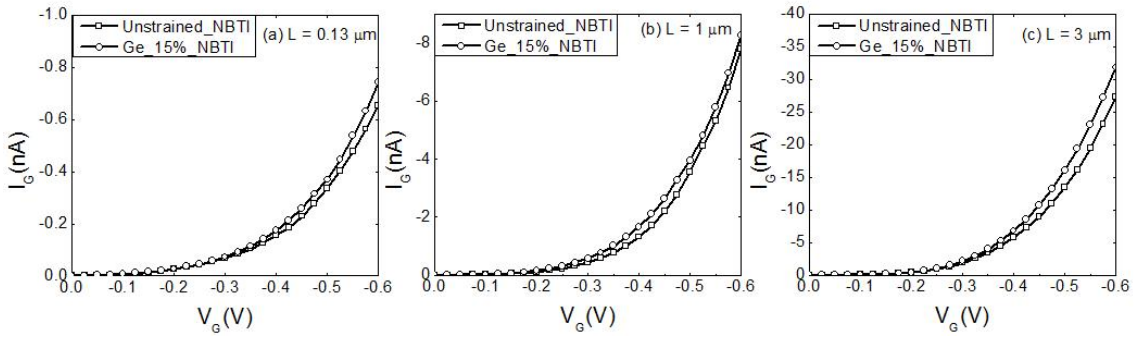


Fig. 3.12. I_G-V_G curves of unstrained (squares) and strained (circles) MOSFETs with a channel length of 0.13 μm (a), 1 μm (b) and 3 μm (c) after NBTI stress

Typical I_G-V_G curves (Fig.3.12) were also measured in strained (circles) and unstrained (squares) devices with L = 0.13 μm (a), 1 μm (b) and 3 μm (c) after NBTI stresses. It is observed that I_G is slightly larger in strained devices than unstrained ones. These data will be also used in Section 3.2.3, where the I_G is measured with a CAFM tip.

3.2.3 Nanoscale Analyses

In this section, a nanoscale analysis of the gate oxide properties of strained and unstrained MOSFETs before and after an electrical stress (with different lengths) has been performed with CAFM. The gate current (I_G) has been measured with the CAFM tip on fresh and stressed transistors and it has been considered as an indicative magnitude of the degradation induced by the stress [258].

CHC Degradation in Strained MOSFETs

First, the effect of a CHC stress was studied on strained and unstrained MOSFETs. Fig.3.13a and b show typical current images obtained at V_G = -4 V on the gate area of a fresh unstrained (a) and strained (b) MOSFET (with L = 3 μm in this case). Note that before CHC stress (Fig.3.10a and b) no currents are detected in the image. In both maps, only the instrumental noise from the CAFM preamplifier can be observed. Fig.3.13 also shows the current maps of the gate area measured at -4 V on unstrained (c and e) and strained (d and f) MOSFETs after a CHC stress at device level, with L = 3 μm (c and d), and L = 0.13 μm (e and f). Note that, after the stress, brighter areas which correspond to regions with a higher conductivity that were not present in fresh devices at the same voltage are measured. These higher conductive regions are indicative of the degradation induced by the stress.

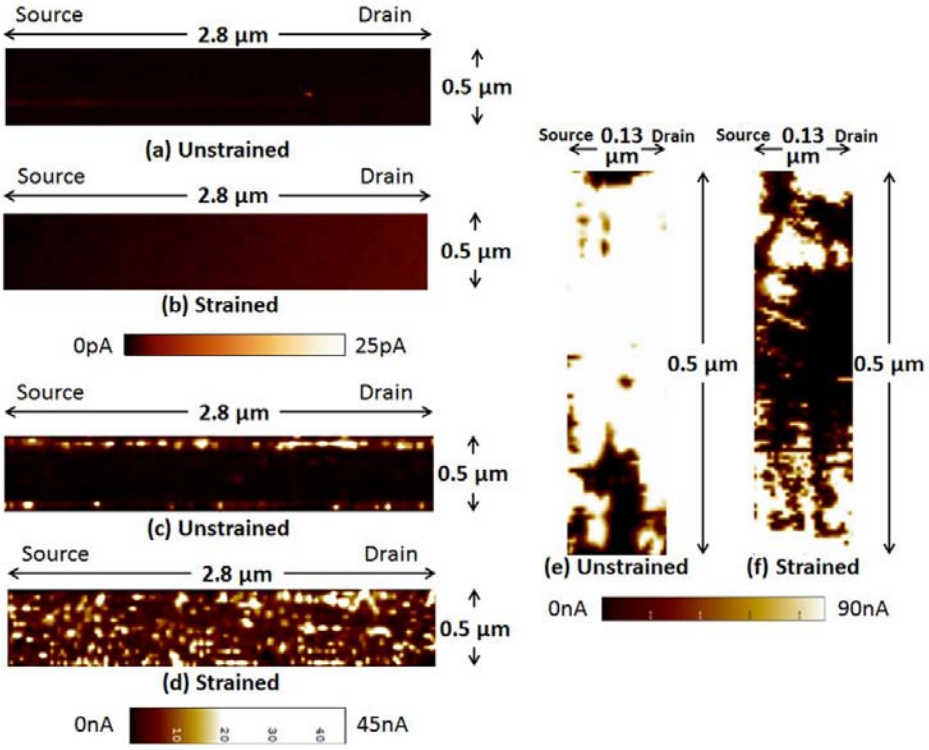


Fig. 3.13. Current images obtained at a gate voltage of -4 V in fresh (a and b) and CHC stressed (c-f) MOSFETs with channel length 3 μm (a-d) and 0.13 μm (e and f). Note that (a), (c), and (e) corresponds to unstrained devices and (b), (d), and (f) corresponds to strained devices.

In the 0.13 μm channel length MOSFET, the measured currents reach the maxi-

mum measurable value (100 mA), indicating that breakdown (BD) could have been triggered during the CAFM scan probably due to the large degradation induced by the CHC stress. Although breakdown was not triggered during the device level measurements (see Fig.3.9), the stress could have damaged the gate oxide in such a way that when voltage was applied to the tip, breakdown could have been triggered. Even in the case that BD was not induced by the CAFM scan, currents are very large, which are indicative of a larger degradation. However, since I_G reaches the maximum allowed current by the setup, no quantitative analysis is possible in these short channel devices.

Contrarily, in the 3 μm channel length MOSFET (Fig.3.10c and d), the leaky sites show lower currents, clearly indicating that BD was not induced in this case. The same kind of behaviour is observed in devices with L = 1 μm channel length (Fig.3.14, which shows a current map measured in a strained MOSFET with channel length of 1 μm after a CHC stress). The leaky sites can be related to trap assisted tunnelling through the defects generated during the stress. Therefore, these sites can be used to analyse the impact of the CHC degradation on the electrical properties of the gate oxide area. Note that the number of leaky sites in strained samples is considerably larger than in unstrained transistors, which indicates a larger CHC damage in strained devices. These results are consistent with the device level measurements. Moreover, thanks to the possibility of this technique to analyse very small areas along the channel, the CAFM images also give us the possibility to study the impact of the stress in different regions of the channel. A quantitative analysis of the current images obtained in different MOSFETs (L = 1 μm) is summarized in Tab.3.4. This table shows the average gate current $<I_G>$ measured on six devices (L = 1 μm) in a 0.25 μm^2 region close to the S, D and in the centre of the channel (C), obtained from current images as those shown in Fig.3.14. Note that, in both kind of transistors (unstrained and strained), (1) regions close to S and D show larger currents, demonstrating the non-uniform degradation of CHC stress, as previously observed in Section 3.1.3 (Tab.3.4), and (2) I_G currents are larger in strained devices, suggesting that strained MOSFETs are more sensitive to the stress which is confirmed at device level in Fig.3.10. However, other experimental considerations could also have an effect on the measured current. To quantitatively compare the impact of the CHC stress in different regions of the channel between strained and unstrained devices, the β_G parameter was

calculated (Tab.3.4):

$$\beta_G = \frac{I_{G,strain} - I_{G,non-strain}}{I_{G,non-strain}} \times 100\% \tag{3.2}$$

which corresponds to the increment of the gate current in strained devices compared to unstrained ones. Note that β_G, which is indicative of the impact of the stress, is larger close to S and D. Therefore, these results demonstrate that, besides the non-uniformity of the CHC stress itself (observed in unstrained devices), in strained devices, source and drain are more sensitive to the stress than unstrained MOSFETs especially close to S/D, where the device was strained. Because of this higher susceptibility, the generation of defects in these areas is favoured (compared to unstrained devices) and is detected by measuring a larger number of leaky sites and higher currents with the tip of the CAFM.

	I_G (nA)		
	Unstrained	Strained	$\beta_G(\%)$
Source	2.67	10.54	294
Channel	1.43	4.92	244
Drain	2.01	9.51	373

Tab. 3.4. Average I_G and β_G values obtained with CAFM close to S/D and in the centre of the channel (C) for 1 μm strained and unstrained devices.

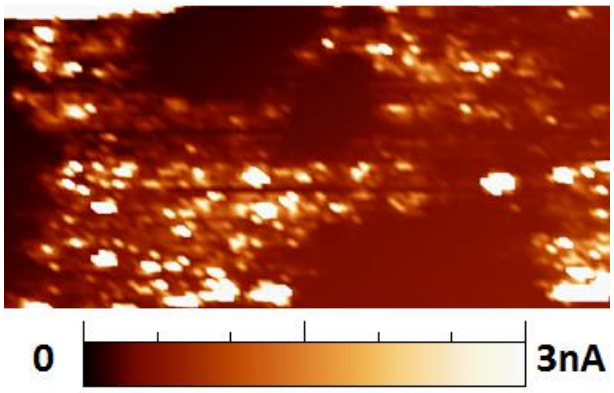


Fig. 3.14. Current map (0.8 $\times$ 0.4 μm^2) of a MOSFET with the channel length of L = 1 μm after a CHC stress applied at device level.

NBTI Degradation in Strained MOSFETs

In this section, the impact of NBTI at nanoscale on strained devices will be studied and compared to unstrained ones. First, the gate oxide electrical properties of strained devices with channel length of 1 μm before and after different electrical stress have been studied. Fig.3.15 shows current images (at the same scale) obtained at V_G = 3.6 V on the gate area (480 nm $\times$ 950 nm) of (a) fresh and (b) NBTI stressed strained MOSFETs with the channel length of 1 μm. Note that in the fresh samples (Fig.3.15a), current is very low, however, in the NBTI stressed device (Fig.3.15b), brighter areas, which correspond to larger current associated to the defects in the oxide, were observed. Similarly to the conclusion obtained in unstrained devices (see Section 3.1.2), the number of leaky sites (associated to the defects in the oxide) in the stressed strained MOSFETs is considerably larger than in the non-stressed strained devices.

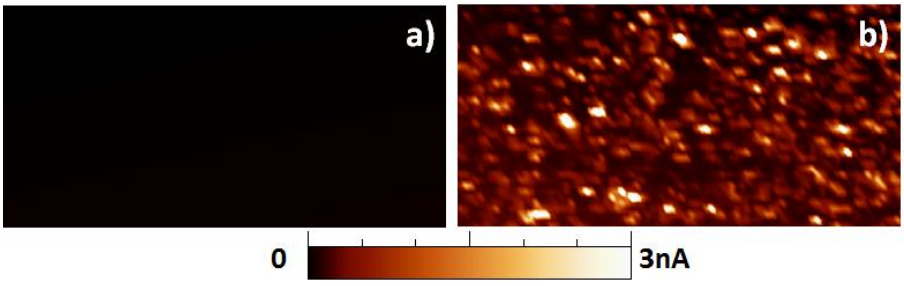


Fig. 3.15. Current images obtained at a gate voltage of 3.6 V in (a) non-stressed and (b) NBTI-stressed MOSFETs (480 nm $\times$ 950 nm).

To quantitatively analyse the information in Fig.3.15a and b, Tab.3.5 shows the average current, <I>, measured in a W $\times$ 0.05 μm^2 region in Fig.3.15, close to the source, drain and at the centre of the channel of the fresh (reference) and stressed devices. Note that in the fresh device, currents are close to the noise level while in the stressed one the conduction is larger (Fig.3.15a). Moreover, in non-stressed MOSFETs the current is distributed quite homogeneously, while in NBTI-stressed MOSFETs, it seems to be a bit higher close to S/D region, further supporting the data of Tab.3.3 (although further analysis should be performed), where it was shown that although NBTI stress is homogenous, strained areas are more sensitive to the stress, leading to higher I_G/lower I_D in these regions (S/D).

Comparing to unstrained devices (see Section 3.1.3) in Fig.3.4, the average cur-

rent is larger in strained transistors which indicates a higher defected degradation, as shown at device level in Fig.3.12. However, the difference observed with CAFM is much higher. Therefore, these results suggest that the measured currents at different devices have probably been affected by other experimental considerations.

<I>	Source	Center	Drain
Reference [pA]	2.14	1.97	2.55
NBTI [nA]	0.27	0.25	0.33

Tab. 3.5. Average current measured in W $\times$ 0.05 μm^2 regions taken in Fig.3.15, close to the source, drain, and at the centre of the channel.

To conclude this Section 3.2, the impact of a CHC an NBTI stress on strained MOSFETs has been investigated and compared to unstrained devices by combining device level and nanometre scale characterization techniques. The nanoscale resolution of the CAFM has allowed investigating the spatial distribution of the damage after the stress. The results show that, with the introduction of strain, the channel mobility increases in both long and short channel devices, being the increment larger in short devices. However, the transistors subjected to local strain are more sensitive to CHC and NBTI degradation, leading to a higher reduction of I_D and higher I_G in both CHC- and NBTI-stressed devices. This effect could be related to a higher defect generation in strained devices, especially at the channel close to source and drain after CHC stress, since a larger increase of the gate current was detected with CAFM in these regions compared to unstrained devices.

3.3 CAFM Analysis of Temperature Dependence of RTN in SiON Gate Dielectrics

As introduced in Chapter 1, Random Telegraph Noise (RTN) in gate dielectrics of MOSFETs is becoming an increasingly important issue in a context of future nanoelectronics, where low voltage operation of devices and circuits will be mandatory. However, suitable tools to study RTN, associated to single defects present in the gate oxide, are required. In this section, RTN has been analyzed at the nanoscale with CAFM at different temperatures (T) on gate stacks. The nanoscale resolution of the CAFM has allowed investigating individual leaky sites of as-grown

layers. Switching between different conduction states have been measured during constant voltage tests in the form of Random Telegraph Noise, which have been related to the trapping/detrapping of single charges in defects present in the dielectric. The number of activated defects has been observed to be dependent on the Temperature and randomly distributed in the gate area.

3.3.1 Experimental

The samples are consisted of MOS structures with a 1.4 nm thick SiON layer as gate dielectric. The layers on top of the gate dielectric were removed as previously explained in Section 3.1.1. After the etching, constant voltage scans to measure current maps and localized Constant Voltage Tests (CVT) to measure I-t curves have been applied to investigate the spatial distribution of the weak spots and their conductivity time evolution. Different temperatures have been used for this analysis as 25, 50 and 75°C. Since the purpose is the evaluation of the electrical properties of as-grown weak spots, the voltage applied during the voltage scans and CVTs was low enough to avoid any oxide degradation.

3.3.2 Temperature Dependence of RTN in SiON Dielectrics

First, leaky sites have been analysed from current images. Fig.3.16 shows 3 current maps measured at 1V at (a) 25°C, (b) 50°C and (c) 75°C on different areas of the same MOSFET. At this voltage, no degradation is induced [258], so the leaky sites which measured in the images correspond to as-grown weak spots. Note that the number and current through the leaky sites increase with temperature, T. CVT on the weak spots have also been measured, showing a time dependent conductivity in the form of RTN (Fig.3.16d). The time and frequency parameters of the RTN in Fig.3.16d have been obtained. The time in which the signal is high, τ_{up}, (Fig.3.17a) and in which it is low τ_{down} (Fig.3.17b), can be correctly fitted by an exponential distribution with time constants of 290 ms and 280 ms, respectively. The Power Spectral Density (PSD) of the current (Fig.3.17c) shows a Lorentzian behavior with a corner frequency, f_c, of 1.12 Hz. The exponential distribution of τ_{up} and τ_{down} and the Lorentzian spectrum suggests that the transitions between

the two states occur randomly. Therefore, the observed RTN can be explained by the change of the oxide conductivity when electrons are trapped/detrapped in/from traps conveniently located to modulate the conductivity of the dielectric.

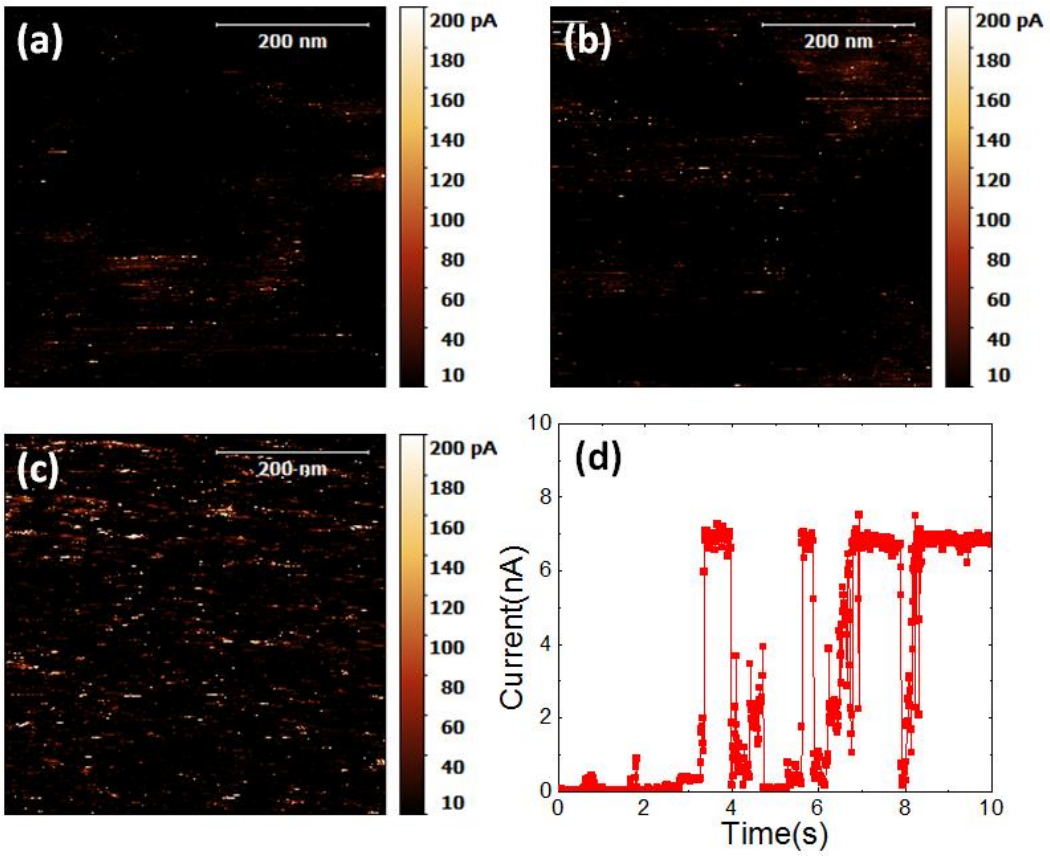


Fig. 3.16. Current maps (at 1 V) measured at (a) 25°C, (b) 50°C and (c) 75°C. Time evolution of the current measured at 25°C and 3 V on a leaky site (d). A two level RTN with amplitude of 7 nA is observed.

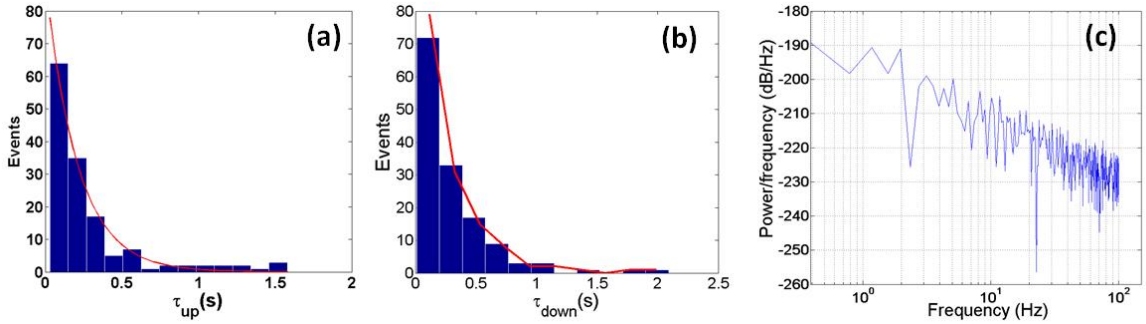


Fig. 3.17. Distribution of τ_{up} (a) and τ_{down} (b), (c) shows power spectral density (PSD) measured for the RTN obtained at 25°C and 3 V of Fig.3.16d. A Lorentzian behavior with a corner frequency of 1.12 Hz has been found.

The nature of the weak spots detected in the current maps could be due to different factors, as oxide thinning. However, CVT have been applied to different leaky sites. The observation of RTN on some of the leaky spots suggests that the current measured at these sites could be also related to the presence of defects, which can be charged/discharged, leading to the switch of conductivity observed in Fig.3.16d. Therefore, the current spots detected in the current maps of Fig.3.16 could be also related to defects that have been activated. This assumption is further supported by the fact that (i) the distribution of currents measured at the leaky sites of the current maps show an exponential behavior (Fig.3.18), as the $\Delta I = I_{up} - I_{down}$ measured in RTN signals during CVT [267] and (ii), the number of spots increases with T, showing a dependence of the activated defects with T as expected: higher T leads to the activation of a larger number of defects.

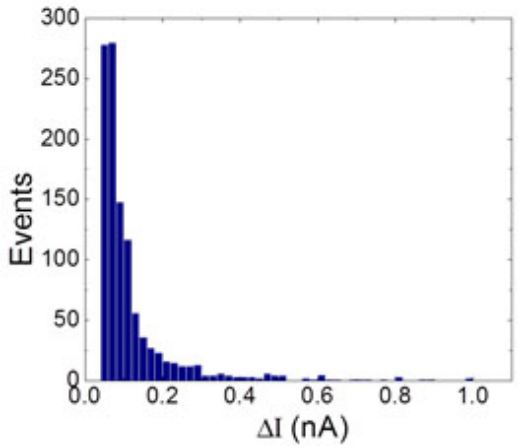


Fig. 3.18. Distribution of $\Delta I = I_{up} - I_{down}$ of the weak spots measured in the current image of Fig.3.16c.

Assuming this hypothesis, that is, the fact that the leaky sites measured in the current maps correspond to defects that have been activated, the current spots have been studied in more detail from current images. Fig.3.19a shows the cumulative distribution function of the number of weak spots versus their conductivity. Note that, as expected, for higher temperatures, higher currents are also measured.

Finally, the spatial distribution of the weak spots in the dielectric has also been evaluated. For this analysis, first, the distance between each leaky spot of the current image measured at 75°C from the rest in the same current map has been measured. Then, the number of times (Y-axis) that a given interval of distances

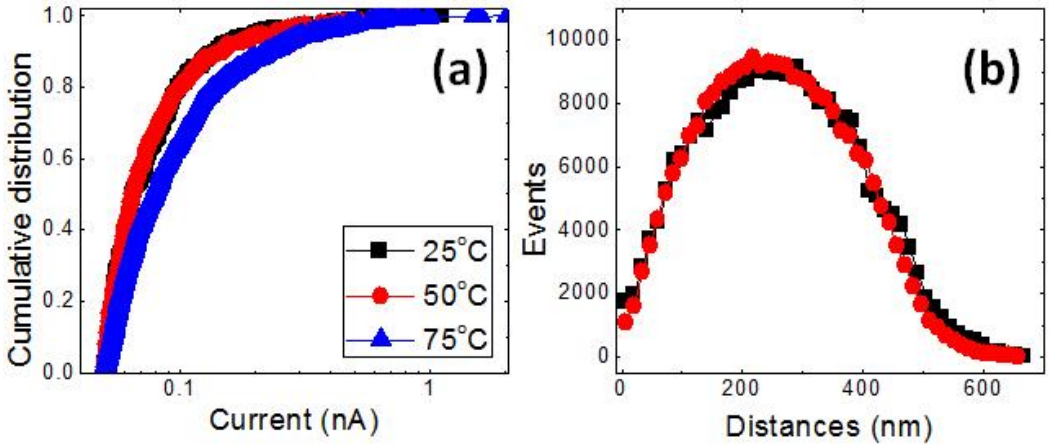


Fig. 3.19. (a) Cumulative distribution of the leaky spots detected in the current maps of Fig.3.16 vs. their conductivity, for different temperatures, (b) Distribution of all the possible distances between the leaky spots of Fig.3.16c (black squares) and when the same number of spots (red circles) are randomly distributed in an area of 500 $\times$ 500 nm^2.

(X-axis) is repeated when considering all the weak spots in the current map of Fig.3.16c is plotted in Fig.3.19b (squares). Note that this distribution of distances is very similar to that obtained when the same number of spots of Fig.3.16c is randomly placed (circles) in an area of 500 $\times$ 500 nm^2 (the area of the current map). These results demonstrate that the distribution of weak spots is random and, therefore, any correlation between their positions can be stablished.

To conclude this section, a CAFM has been used to study individual leaky spots at the nanoscale and at different temperatures on as-grown SiON layers. Switching between different conduction states have been measured in the form of Random Telegraph Noise during Constant Voltage Tests, which has been related to the trapping/detrapping of single charges in the defects present in the dielectric. The measurement of current maps at different T suggests that the detected leaky sites correspond to defects, whose activation depends on T and that are randomly distributed in the gate area. This section, therefore, demonstrates that the CAFM allows the analysis not only of failure mechanism associated to an electrical stress, but also the electrical characteristics of single defects present in as-grown dielectrics.

Chapter 4

Resistive Switching in MIS/MGIS Structures

In Chapter 1, it was introduced that Resistive Random Access Memory (RRAM) is a promising alternative for future memory devices, owing to its scalability, non-volatility and high performance. RRAM devices, which are based on Resistive Switching (RS) phenomenon, usually are two terminal devices, such as Metal-Insulator-Metal (MIM) or Metal-Insulator-Semiconductor (MIS) structures. These structures can be easily fabricated using standard microfabrication techniques [268, 269]. In these structures, it is possible to electrically form and partially break a Conductive Filament (CF) through the insulator material leading to the low and high resistive state (LRS and HRS), respectively. Although some prototypes of memory cells based on the RRAMs have been presented [270–272], some issues have to be resolved. For example, the physical phenomenon of formation of CF is still needed to be clarified, as well as its dependency on the electrode material [96]. In this chapter, on one hand, CFs in MIS structures showing RS will be analyzed at the nanoscale by means of Conductive Atomic Force Microscope (CAFM) (**ANNEX**). On the other hand, since novel materials such as graphene has already been used to improve the RRAM devices [107, 174, 193], the electrical properties of MIS structures with an interfacial layer of graphene between the dielectric and the metal electrode (MGIS structures) will be studied at device level (**PUBLICATION 3**) and at nanoscale with CAFM and will be compared with MIS structures without graphene. In this respect, the fabrication of the MGIS structures

will also be discussed.

4.1 Observation of Conductive Filaments in Ni/HfO_2/Si Structures with CAFM

For the analyses of RS at the nanoscale, CAFM is a useful technique not only to characterize the electrical properties of the CF, but also to switch the resistance of the dielectric material by using the conductive tip as the top electrode of the structure [273, 274]. So it is possible to create and analyze the CFs locally with a relatively simple setup with CAFM. However, since the switching characteristics are strongly dependent on the electrode material [96], the properties of the CF formed using the CAFM tip as a top electrode could differ from the ones generated in conventional MIS or MIM structures. To overcome this limitation, in this section, a CF is formed in Ni/HfO_2/Si capacitors. Afterwards, the Ni electrode is removed and the CF properties analyzed at the nanoscale with the CAFM tip. The objective is to give further insight into the RS mechanisms responsible for the formation and partial dissolution of CFs.

4.1.1 Samples and Experimental Setup

The samples used to investigative the RS phenomenon consisted of 5×5 μm^2 Ni/HfO_2/Si structures, with a 20 nm thick HfO_2 layer as dielectric. The structure and size was carefully chosen so that the whole active area of the device could be fully analyzed by CAFM. Fig.4.1a shows a schematic of the cross-section of the sample. These samples were fabricated at the IMB-CNM (Institute of Microelectronics of Barcelona, Centre Nacional de Microelectr∂nica).

Firstly, the CF was created at device level with a HP-4155B Semiconductor Parameter Analyzer (SPA), with a current limit of 10^{-4} A. The voltage was applied to the Ni top electrode, while the Si substrate was grounded. To reach a stable state of the CF, five set and reset cycles were applied. Some samples were left at the high resistance state (HRS) while some others were left at the low resistance state

(LRS). Fig.4.2 shows the last I-V curves recorded after the set (LRS, left) and reset (HRS, right) processes in two different samples. In total, 10 samples were studied.

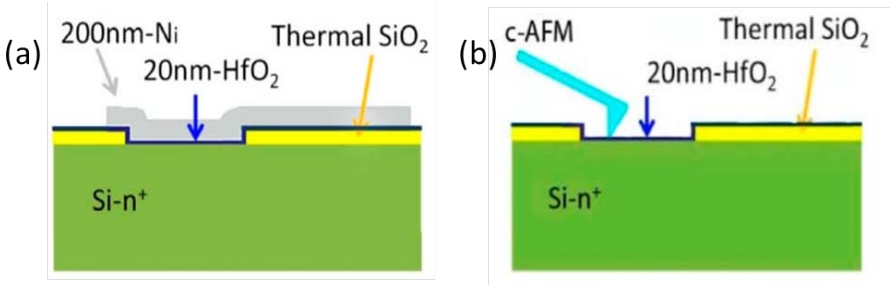


Fig. 4.1. (a) Schematic cross-section of the studied Ni/HfO_2/Si structures. (b) After Ni electrode removal, the whole active area of the device was exposed to the CAFM tip.

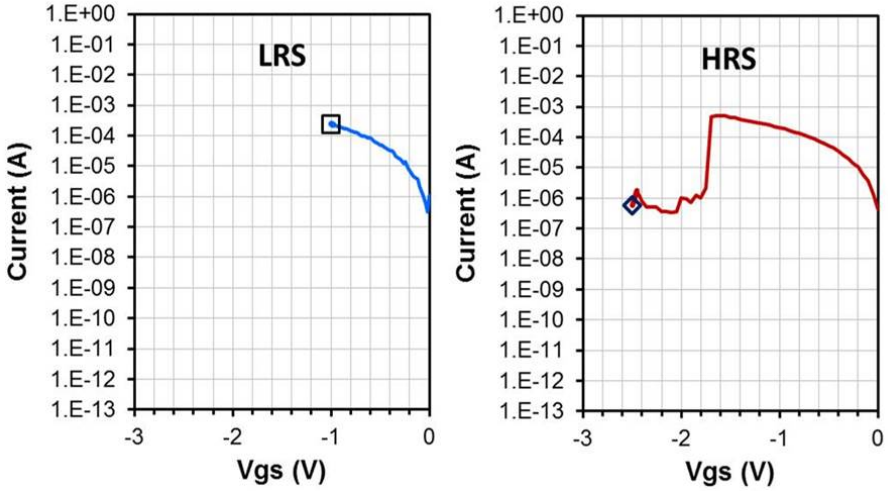


Fig. 4.2. Last I-V curves of two of the studied samples that were left at the LRS (left) and HRS (right). The measurements have been obtained at device level with the Semiconductor Parameter Analyzer (SPA).

After the forming of the CF and the device level analyses, the Ni electrode of the MIS structures was etched by means of H_2O:HNO_3 = 4 : 1 for 10.5 minutes so that the HfO_2 surface was exposed and could be analyzed with the CAFM tip (Fig.4.1b). A conductive Pt bulk tip with 20 nm nominal radius was used in order to study the device at the nanoscale. These tips are mechanically more stable than the metal-coated ones, permitting us to measure more maps without losing the topographical resolution and the conductivity during the experiments, a critical issue in measuring this type of systems. In any case, when small conductivity and/or resolution losses were observed, the tip was changed, so that the results are not affected by the tip properties. The whole active area was scanned at -4 V (injection from the

substrate). Note that although this voltage seems to be too large compared to the voltages applied at device level (see Fig.4.2), it must be taken into account that due to the resistance of the tip (see Section 2.4.2), not all the voltage is applied to the sample. Therefore, a direct comparison between the voltages applied at device level and those applied with the CAFM tip cannot be performed. In any case, by applying -4 V with the CAFM, the CF properties were not modified. For comparison, pristine samples and samples in which no current limit was established during electroforming have also been studied and compared to those left at the LRS and HRS.

4.1.2 Analyses of the CFs with CAFM

First, CAFM analysis of pristine samples was performed in order to study any possible effects of the etching of the top electrode on the HfO_2 layer. Fig.4.3 shows the topographical (a) and current (c) images of a pristine MIS device, after the etching of top electrode. It is observed that the surface of oxide layer is very uniform and no current is detected, which indicates that the etching process had a negligible effect on the properties of HfO_2 layer. Next, samples which underwent hard breakdown (applied voltage without current limit at device level) were studied. Fig.4.3b and d show the topography and current map respectively of a device in which a BD was triggered without any current limit. In this case, after the etching of the top electrode, the topographical image showed an uncontrolled growth of a large structure covering the entire device surface, a consequence of the large energy dissipation caused by the irreversible dielectric breakdown of the oxide layer. It can be observed in Fig.4.3d that large current appears in different regions of the device.

In the case of the devices where RS was observed, the topography and current images are significantly different. To show this point, Fig.4.4a and b present typical 2D topographical and current images, respectively, of a device after the formation of the CF that was left at the HRS. Qualitatively similar results were obtained in the LRS samples shown in Fig.4.4e and f. Interestingly, in the entire device surface only a hillock is detected, that corresponds to the sole conductive area found in the current image (Fig.4.4b and f). As can be observed in Fig.4.4c, which cor-

responds to the 3D topographical image of the hillock observed in Fig.4.4a, the hillock has an irregular shape but presents well defined edges, demonstrating that the CF formation is local. In addition, the surface around the hillock is unaffected, as the homogeneity of the pristine samples (see Fig.4.3a). This indicates that in our experimental conditions, one or several CFs are concentrated in the spot revealed by the topographical images. This is shown in Fig.4.4d, which corresponds to the topographical image (Fig.4.4a) of the CF overlapping the current image (red color, Fig.4.4b). This hillock is probably the result of the electrochemical and thermochemical reactions responsible for the CF formation and dissolution processes [275]. However, further analysis is needed to elucidate the physical origin of these morphological modifications.

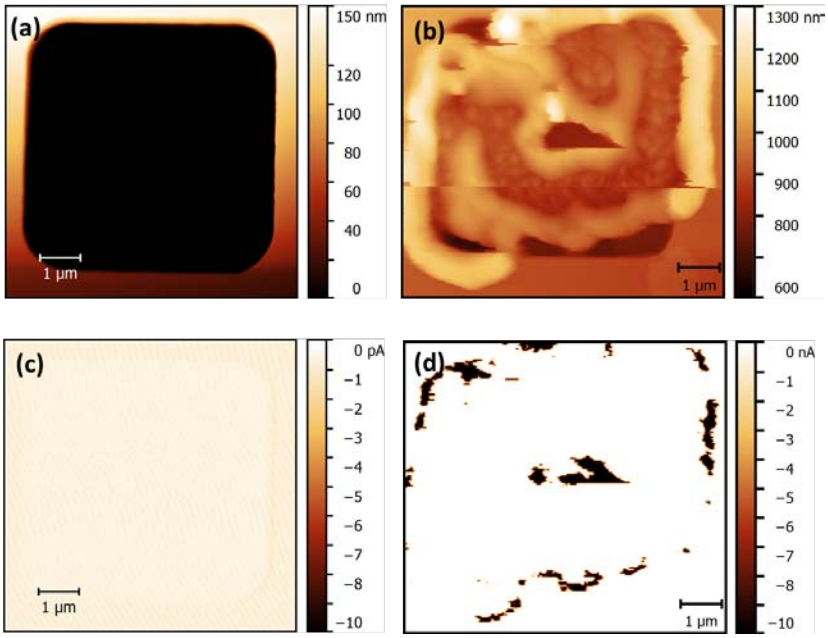


Fig. 4.3. (a) and (c) show the topographical and current images of the pristine device after the etching of the top electrode, Ni. A very flat surface with only noise level current is observed. (b) and (d) show topographical and current images of a device after electroforming without current limit. A large morphological modification and large current in the device area are measured.

After the analysis of several devices we observed that the position of the CF is random. Measurements show that the CF characteristics are qualitatively similar between devices, independently of the device state (i.e. LRS or HRS). We found that in Fig.4.4c the spot areas are around 0.5 μm^2 with an estimated hillock height of around 100 nm. However, though a statistically representative analysis has not been carried out, the measurements seem to indicate that the LRS spots present

smaller sizes than the HRS spots (Fig.4.4a and e).

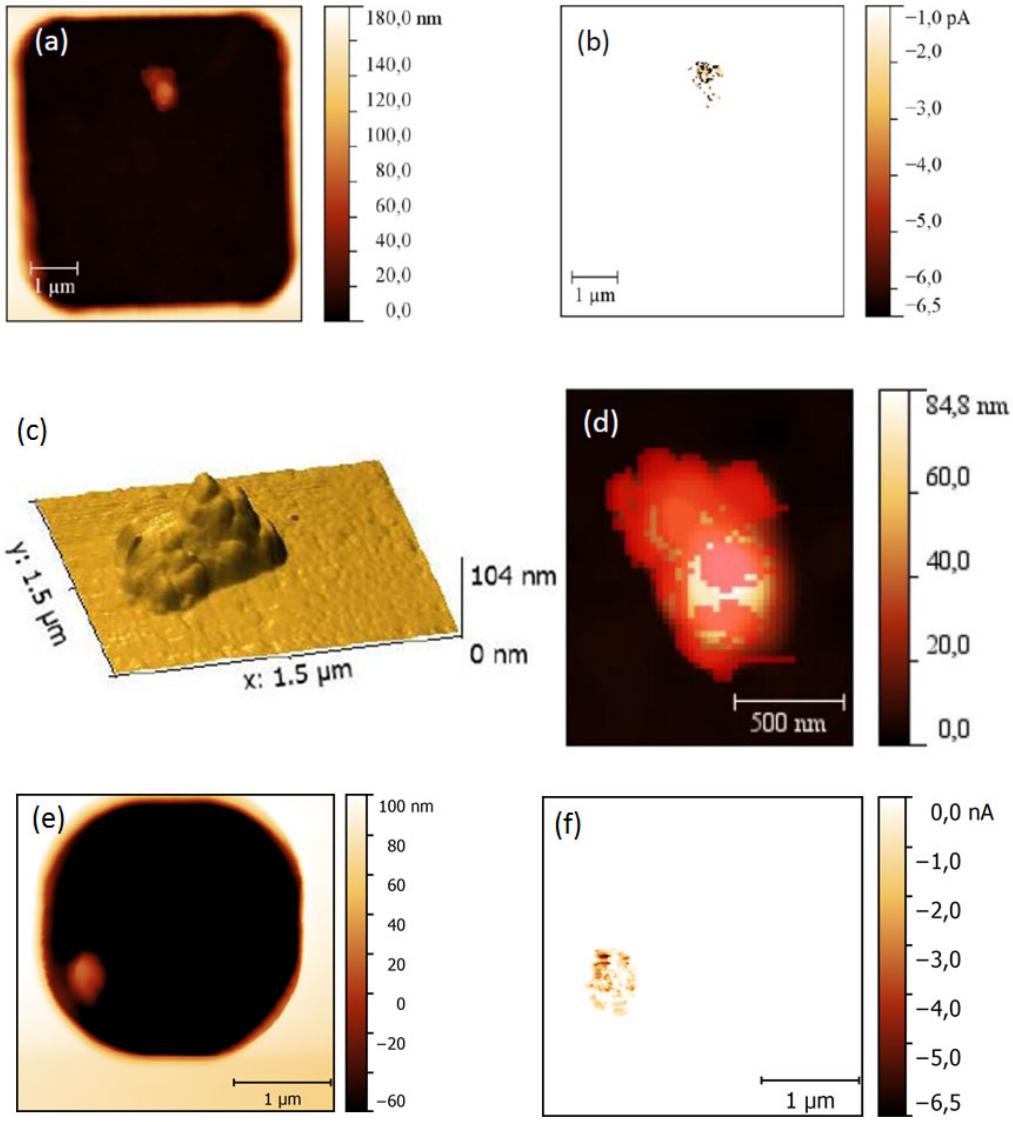


Fig. 4.4. (a) Topographical and (b) current images of a sample at the HRS state measured at -4 V. In both images, a unique spot is clearly visible in the device area. (c) Representation in 3D of the hillock. (d) Topographical image of the spot overlapping the current image (red colour), indicating that surface modifications and current increase are correlated. (e) Topographical and (f) current images of a sample at the LRS state measured at -2 V.

Interestingly, as can be seen in Fig.4.5, the local conductive measurements of spots corresponding to LRS (a) and HRS (b) show that the current through the CF is not spatially homogeneous. Although in most of the spot area currents of pA are detected, there are small regions with currents in the range of nA in both LRS and HRS. Moreover, in the LRS spots, the portion of the CF area with higher currents is

larger than in the HRS, which would explain the larger LRS conductivity observed at device level (Fig.4.2). This inhomogeneous conduction is compatible with a tree-shaped CF [275]. As sketched in Fig.4.5c, some branches would span all along the dielectric thickness, connecting the two electrodes, whereas some others would end within the dielectric. Then, when scanning with the tip, larger currents would be measured in the first case ($\sim$ nA currents) whereas lower currents would be observed in the second case ($\sim$ pA currents). The number of electrode-connecting branches would be larger for the LRS case, in accordance with the observed size of the high-current area of the CF.

To conclude Section 4.1 (**ANNEX**), the CAFM characterization of CFs in Ni/HfO_2/Si RS structures has shown that, independently on the device state (LRS or HRS), the CFs are formed in a unique spot that can be detected as a hillock in the topography image after the removal of the Ni electrode. Local electrical analysis of the HRS and LRS spots reveals a non-uniform conduction, with some regions in the spots with significantly higher conductivity. This behavior is in agreement (although not a definite conclusion) with the tree-shaped model of CF formation.

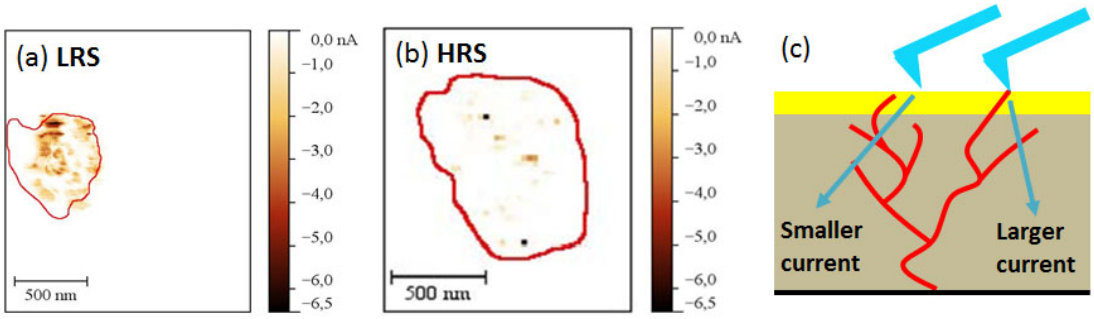


Fig. 4.5. Current images of representative spots corresponding to (a) LRS and (b) HRS measured on different samples. The red line marks the edges of the regions where current is measured. (c) Schematic representation of the tree-shaped model of the CFs. The higher current measured with CAFM goes through the branches that end near the dielectric surface, whereas the others are responsible for the lower conductivity measured in the rest of the spot.

4.2 Impact of Current Limit on the Electrical Properties of Conductive Filaments in MIS structures

In this section, the electrical characteristics of CFs created with different CLs are analyzed at device level and at the nanoscale with the CAFM. For this analysis, two different structures were studied. In one of them, the CF was created during a forming process with a CL of 5 μA (Fig.4.6a), and in the other, the CL was 150 μA (Fig.4.6b). At device level, several RS cycles were applied at each device and finally they were left in the HRS. Fig.4.6 shows I-V curves measured in both devices where the forming and set processes were obtained with a CL of 5 μA (a) and 150 μA (b), respectively. The continuous lines correspond to the last I-V curves registered in the capacitors, whereas the discontinuous lines correspond to previous I-V curves before the final reset. Although more devices should be studied to obtain enough statistical data, it can be observed that the CL impacts on the global current flowing through the CF. In the case shown in Fig.4.6, with the CL of 150 μA, the current measured in the HRS is about one order of magnitude larger than that with a CL of 5 μA. However, in the LRS this impact is not clear. Since the variability of the current in the LRS is shown to be larger than that of HRS (Fig.4.6), it is difficult to conclude with the reduced number of analyzed structures whether with higher CL, the current measured in LRS is larger or not. Therefore, in the preliminary analysis shown in this section, we will pay attention to structures left in the HRS.

After the device level analysis, the top electrode of the two devices was etched and the gate oxide was scanned with the CAFM. Topography and current maps were measured on the two samples (Fig.4.7). Fig.4.7 presents the topographical (a and b) and corresponding current (c and d) images of the devices left in the HRS with the CL of 5 μA (a and c) and 150 μA (b and d). The current images were obtained with -1.5 V applied to the substrate. Regarding the topographical images, although the area of the capacitor is 25 μm^2, after the removal of the top electrode, only topographical changes associated to the CF with a much smaller area are detected, suggesting that the filament formation is localized as explained in Section 4.1.2. As can be seen in Fig.4.7a, a maximum height of around 30-60 nm with a base below in the size of about 0.2 μm^2 is detected. In Fig.4.7b, the

size is about 2.5 μm^2. It can be observed that the detected structure is larger with higher CL, at least, in these two devices.

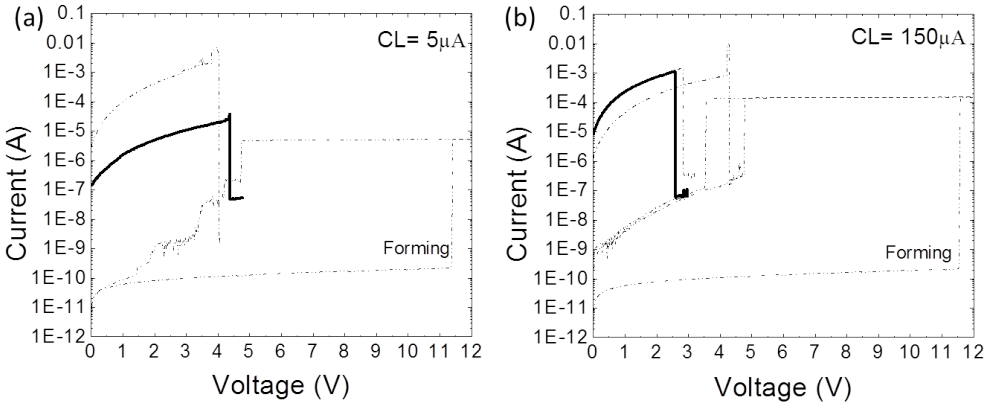


Fig. 4.6. I-V curves corresponding to devices left in the HRS at which the CF was created with a CL of 5 μA (a) and 150 μA (b). The continuous lines correspond to the last I-V curves registered in the capacitors, whereas the discontinuous lines correspond to previous I-V curves before the final reset.

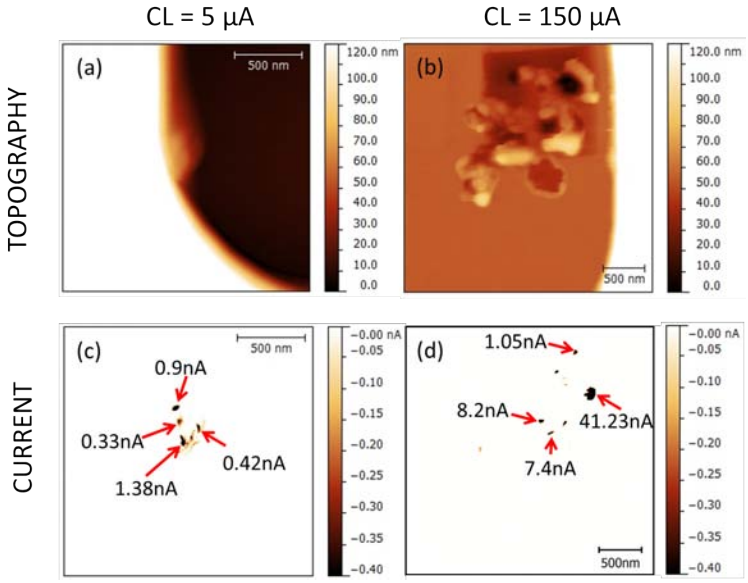


Fig. 4.7. Topographical (a and b) and current (c and d) images of devices left in HRS with a CL of 5 μA (a and c) and 150 μA (b and d).

Not only the area affected by the forming has been analyzed and compared with different CLs, but also their conduction from current maps. The current images shown in Fig.4.7c and d corroborate the behavior that only affected regions in topographical maps are conductive. The maximum current values of some spots

detected in the images (indicated by arrows) are shown in Fig.4.7c and d, which indicate a larger conductivity in the capacitors with higher CL. Moreover, the total current flowing through the CFs has been roughly estimated from these current images and compared to the current measured at device level. This comparison has been possible thanks to the use of the Resiscope module [241], which allows the measurement of currents with the CAFM tip in the range of 1 pA - 1 mA. To estimate the current flowing through the whole CF detected in the current image, the sum of all the currents registered in the map (inside the CF) was calculated. The global current of Fig.4.7c is -10.34 nA, while the global current of Fig.4.7d is -172.06 nA, about one order of magnitude larger in the case of a higher CL. Therefore a similar tendency as that shown at device level is observed. In the HRS, the global current measured at device level when the CL was 5 μA, was about one order of magnitude smaller than with 150 μA (Fig.4.6). Note also that a direct comparison between the absolute values of the current measured at device level and at nanoscale is not possible due to experimental considerations that can affect the value of the current measured with the CAFM tip (as the contact area, the ambient conditions, and the tip resistance...).

To conclude this section, the use of a CAFM and a Resiscope module has been used to preliminary evaluate at the nanoscale the impact of the CL on the HRS conduction. We have seen that the different level of current observed at device level when different CLs are used can be attributed not only to an increase (for high CLs) of the affected area but also to the conductivity through the different conductive spots observed in the current map.

4.3 MIS structures with Interfacial Graphene for RRAM Applications

In Chapter 1, it has been introduced that graphene is a very promising material as an interfacial layer between the metal oxide and top electrode (i.e. MGIS or MGIM structures) for memory applications in RRAM technology. It seems to provide a better control of the formation of the CF, as the graphene layer avoids interfacial interactions [107], preventing the migration of metal atoms into the insulator or

acting as an oxygen barrier (avoiding the oxidation of the metal electrode) [193]. In Section 4.3.1, first, the fabrication of graphene-based structures (i.g. MGIS structure) will be described. Then, in Section 4.3.1, the electrical properties and variability of these structures will be analyzed at device level and at nanoscale with CAFM and compared to devices without graphene. Their feasibility for RRAM applications is also evaluated.

4.3.1 Fabrication of Graphene-based Structures

Recently, chemical vapor deposition (CVD) has been one of the most common approaches to grow graphene on both nickel [276] and copper films [277]. In particular, the process to grow graphene flakes on copper has been useful for monolayer formation because of low carbon solubility in copper [277]. One of the characteristics of CVD-grown graphene flakes is that they can be transferred to other substrates by using a very ingenious process [278]. This method helps the study of the interaction between graphene and different materials, and allow to transferring graphene to substrate typically used an micro/nano-electronics for the fabrication of electronic devices as graphene field effect transistors and/or graphene-based MIS capacitors [187, 279–281].

In this section, typical transfer process of graphene onto such substrates will be presented. Moreover, some improvements for the process will be demonstrated. Nanoscale and atomic scale techniques (SEM, TEM and AFM) are used to study the quality of the transference on different substrates. Moreover, it is also demonstrated from Raman spectroscopy that the graphene sheets grown by CVD used in this thesis were mainly monolayers. Finally, the fabrication process of graphene-based devices such as MGIS structure for memory applications is presented.

As-grown Graphene on Copper Films

The as-grown graphene over a copper substrate used in this thesis was obtained from Graphenea. It is important to check the quality of the as-grown graphene layer before the transference and fabrication process. The morphology of as-grown graphene on a copper substrate was investigated with SEM. Fig.4.8a shows the

typical SEM image of as-grown graphene single layer on Cu, in which a network of long and dark lines (red arrow) and some dark islands (yellow arrow) can be distinguished. These features correspond to typical graphene wrinkles and multilayer graphene, respectively, as discerned in [282]. The wrinkles are known to be formed due to the high compressive strain originated from the cooling down after the CVD growth process [283, 284].

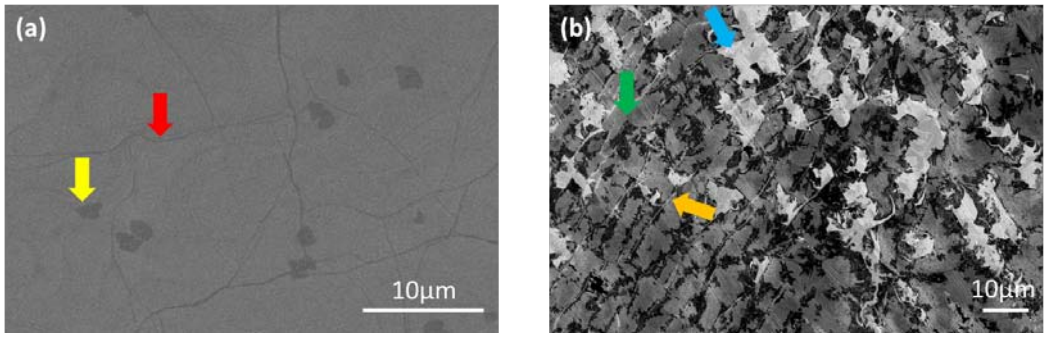


Fig. 4.8. SEM images of graphene single layer over copper (a) in good condition with graphene wrinkles (red arrow) and multilayer graphene islands (yellow arrow), (b) in bad condition with broken area (blue arrow), green flakes (green arrow) and oxidation due to the long time kept in air atmosphere (orange arrow).

Fig.4.8b shows the SEM image of a sample (as-grown graphene single layer on Cu) kept in air atmosphere for several months. It is clearly observed that the graphene layer is in bad condition comparing with Fig.4.8a. In Fig.4.8b, it can be observed some dark islands, which correspond to graphene flakes (green arrow), large light areas, which correspond to bare copper surface (blue arrow), and bright spots, which correspond to oxidation (orange arrow) due to the long time kept in air atmosphere [285, 286]. In this case, the graphene single layer is really bad and not recommended for further fabrication process, indicating that graphene on Cu substrate must be carefully protected and selected for the device fabrication. Once the as-grown graphene single layer has been checked, it can be transferred to the substrate of interest for further process, which will be discussed in the next sections.

Improvement in Transfer Process of CVD Graphene

Nowadays, various methods have been carried out to separate the graphene layer from copper films and transfer it onto a given substrate. The most common pro-

cess used in laboratory scale is as following (Fig.4.9). First, a PMMA layer is spin coated over the graphene/copper surface (a). Next, the copper is etched away by a solution of $FeCl_3$ [287] (b). Then, the PMMA /Graphene stack is transferred to a container with water or HCl in order to clean the bottom surface (c). After that, it can be transferred over the objective substrates by fishing it with the target substrate (d). Finally, the PMMA layer is removed with acetone, (e), as a dissolving agent to uncover the graphene layer which will be ready for further treatment (f).

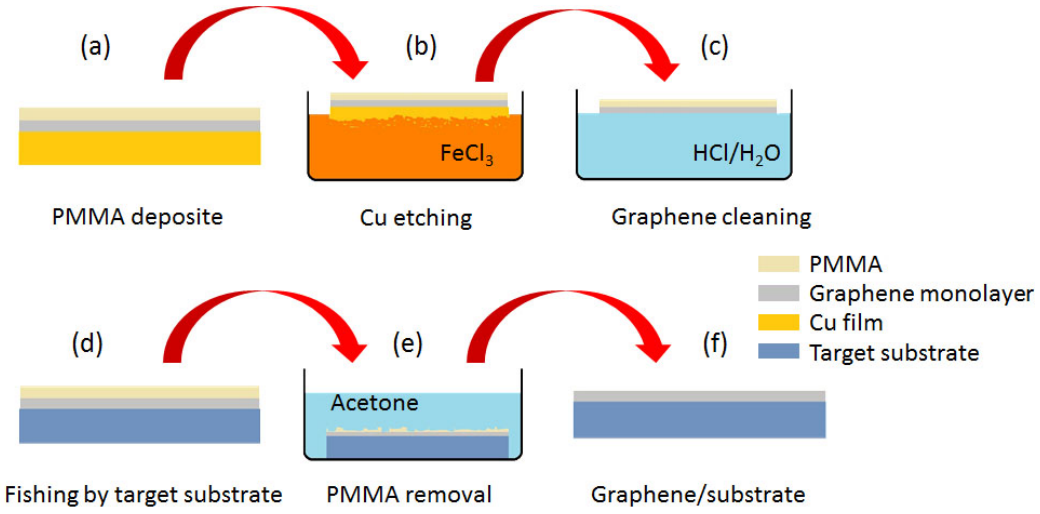


Fig. 4.9. Schematic of typical transference process of CVD graphene.

In order to analyze this transfer process and the quality of the transferred graphene, a silicon wafer with a 300 nm SiO_2 layer above was initially used as substrate since graphene single layers can be easily distinguished on this substrate even with an optical microscope. Fig.4.10a shows an example of the optical image of the sample surface after graphene transference, where the final step of Fig.4.9 was performed with acetone. The brighter areas (red arrow) correspond to non-dissolved PMMA, the dark blue areas (yellow arrow) correspond to graphene single layer and the light blue areas (green arrow), which are referred as holes and clean areas, correspond to the surface of SiO_2. Fig.4.10b shows a SEM image of the same graphene single layer where the holes are detected. Although it is possible to make a good transfer with this typical process, we detected that is not reproducible, mainly due to two critical issues: 1) The existence of holes, as seen in Fig.4.10a and b, may indicate that the graphene layer is not in intimate contact with the substrate surface [278]. This may be a result of the wrinkles formed by the PMMA layer shown in Fig.4.11, 2) Moreover, acetone is not efficient enough to eliminate the PMMA,

especially in zones where the graphene is wrinkled and the concentration of PMMA is higher (Fig.4.10). Note that the most prominent features in the Raman spectra of monolayer graphene are the so-called G band appearing at 1582 cm^{-1} (graphite) and the 2D (G') band at around 2700 cm^{-1} [288]. However, in Fig.4.10c which corresponds to the Raman spectra of the sample shown in Fig.4.11a and b, the intensity of both G and 2D bands is very low. Moreover, peaks are observed from 2750 to 3100 cm^{-1} with high intensity which indicates the existence of PMMA [289, 290].

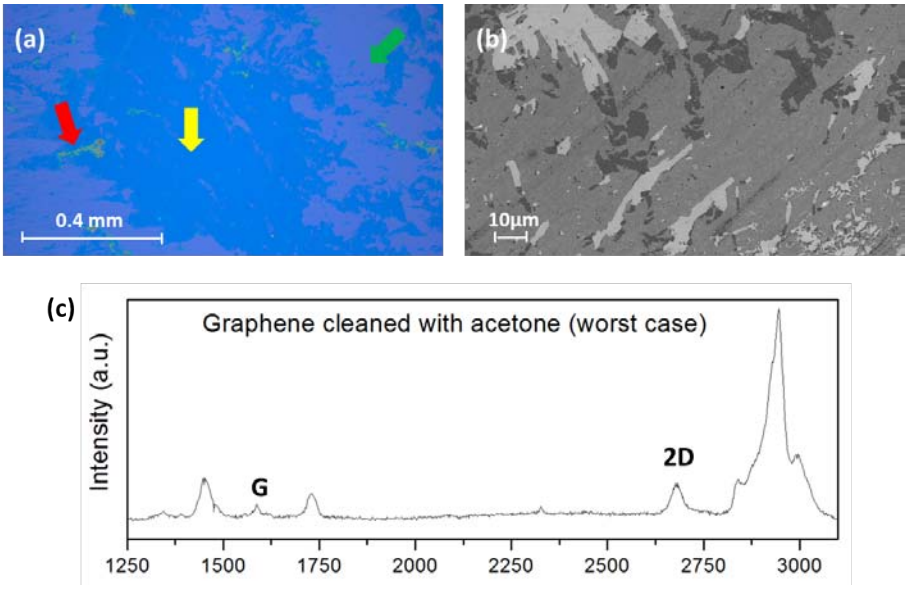


Fig. 4.10. (a) Optical image of bad graphene transference over SiO_2/Si substrate where acetone was used for the PMMA removal. The brighter areas correspond to non-dissolved PMMA. (b) SEM image of the same GSL where holes are detected. (c) Raman spectrum of the worst case scenario found on layers cleaned with acetone where PMMA is detected.

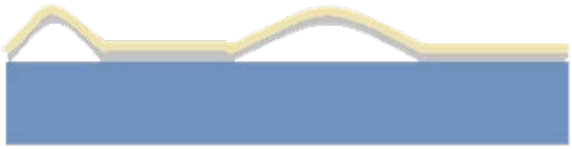


Fig. 4.11. Schematic of PMMA wrinkles over the substrate.

In order to reduce the imact of these two issues on the transference process, a heating treatment was added before the removal of the PMMA. After PMMA/graphene stack was transferred to the target substrate, the system is heated at 70°C for a few minutes to dry the stack and then heated at 150°C for 4-6 hours to relax the

PMMA. It is important to know that before the transference to the target substrate, it is better to clean the target substrate with the solution, H_2SO_4 : H_2O_2 = 1 : 1, as the substrates used in this thesis are oxides/Si stacks.

After the heating, PMMA was removed in acetic acid instead of acetone [291]. These additional processes assure the good transference of almost all the graphene single layer. Fig.4.12 shows an example of the optical (a) and SEM (b) images of the graphene single layer transferred by the improved process. It is observed that almost no holes are detected in graphene surfaces as high as 1 cm^2, which indicates that the relaxation of the PMMA layer allows a good contact between the graphene single layer and the substrate surface. Moreover, the cleaning with acetic acid seems to achieve two objectives: 1) The slower reaction with the PMMA decrease the possibility of the stripping of graphene single layer from the substrate, lowering the formation of holes, and 2) the results indicate that acetic acid is more efficient eliminating the PMMA than acetone, as no PMMA residues can be detected by Raman spectroscopy and both G and 2D bands can be observed (Fig.4.12c).

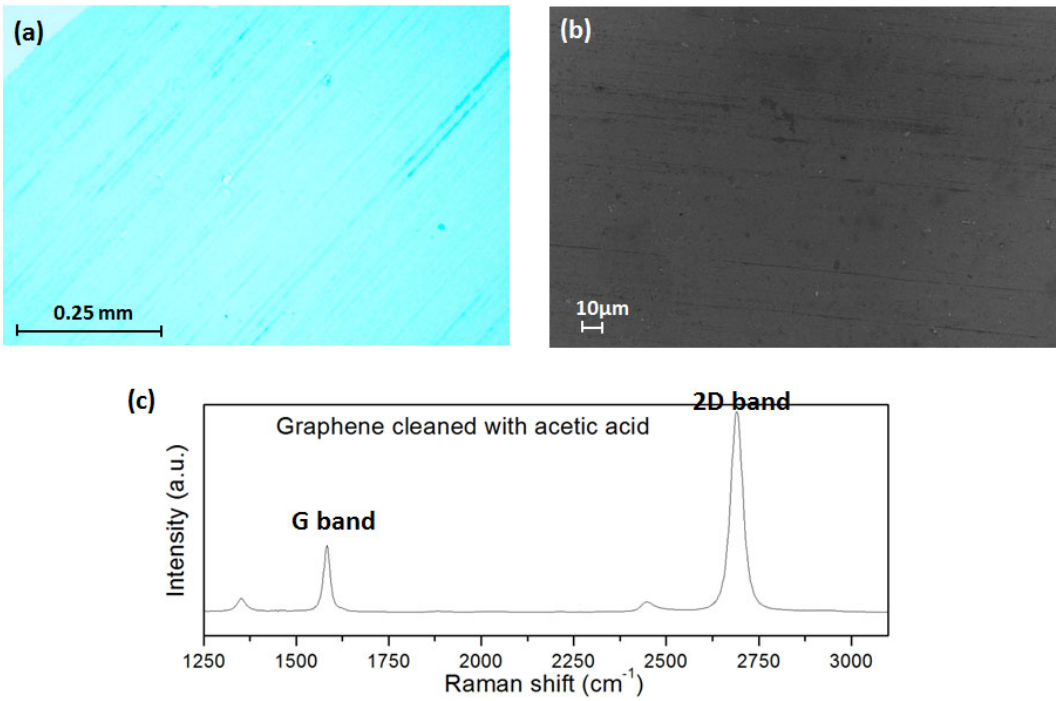


Fig. 4.12. (a) Optical image, (b) SEM image and (c) Raman spectrum of a GSL transferred using the improved method.

With the improved transference process, graphene single layers have been trans-

ferred on different substrates for the fabrication of MGIS devices. The fabrication process will be discussed in the next sections.

Fabrication of Graphene-based MGIS Structures

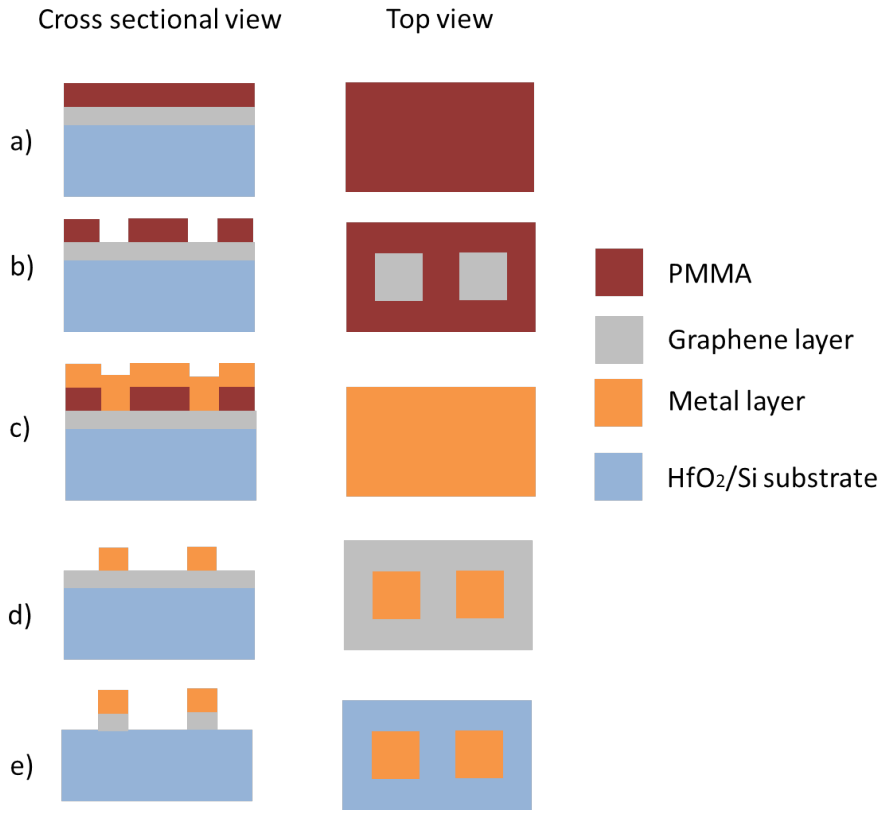


Fig. 4.13. Fabrication process of MGIS devices.

For the fabrication of MIS devices with and without graphene, the target substrate used in this thesis consisted of a 6.6 nm thick HfO_2 layer deposited by atomic layer deposition (ALD) on a p-Si substrate at 200°C. As shown in Fig.4.13, after the transference process of graphene, the sample should be covered with PMMA by spinning (Fig.4.13a). Then, the active areas of the device are defined with laser photolithography (MicroWriter ML^{TM}) and etched with methyl-isobutyl-ketone (Fig.4.13b). Next, a 1 μm thick Au/Ti layer was deposited on the substrates with different sizes (from 20x20 μm^2 to 80x80 μm^2) (Fig.4.13c). After that, the PMMA was removed with acetone and only metallic layer remained on those areas which related to the electrical contacts (Fig.4.13d). Finally, the samples were etched by O_2 plasma using a Reactive Ion Etcher (RIE) 2000 CE from South Bay Technol-

ogy inc. in order to eliminate the graphene material which is not underneath the metal electrodes (Fig.4.13e). Identical structures but without graphene, that is, Au/Ti/HfO_2/Si structures (MIS structures) were also fabricated as references.

4.3.2 Analyses of MGIS Structures for RRAM applications

At Device Level

After the devices were fabricated, they were electrically measured with a Semiconductor Parameter Analyzer (SPA) (**PUBLICATION 3**). Current limited (CL) Ramped Voltage Stresses (RVS) were applied (CL=0.1 A or 0.1 mA), in order to control the CF forming process and evaluate their feasibility as Resistive Switching (RS) based memory devices. Fig.4.14 illustrates the schematics of the device level measurements of MIS (a) and MGIS (b) devices. All the measurements were performed at room temperature.

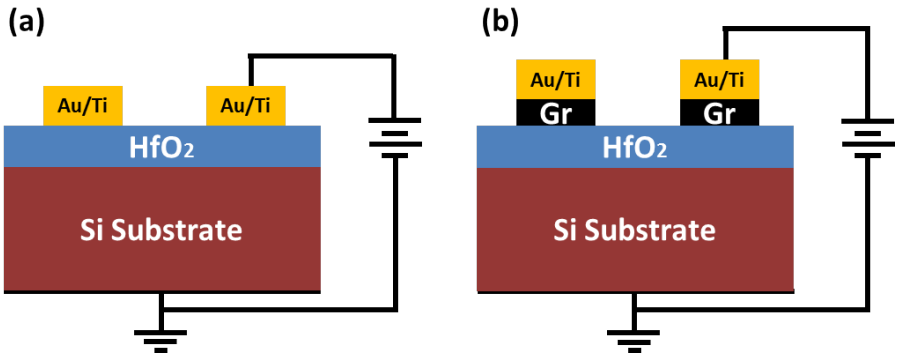


Fig. 4.14. Schematic illustration of the final MIS (a) and MGIS (b) structures measured at device level.

First of all, the impact of the graphene layer on the electrical conduction and subsequent forming process of the MIS and MGIS devices was investigated from the measurement of I-V curves with a CL = 0.1 A or 0.1 mA. Fig.4.15 shows a set of I-V characteristics measured on different MIS (a) and MGIS (b) devices. Only one curve (green) is shown for the case of CL = 0.1 mA since qualitatively equivalent behaviors are observed for the two CLs. Fig.4.15c corresponds to the Weibull plot of the forming voltage, V_F for the case of CL = 0.1 A obtained on samples with (circles) and without (squares) graphene. Note that V_F of MIS devices is around

3 V. Moreover, very little variability is observed between devices neither on V_F (Fig.4.15c) nor in the tunneling conduction before the forming (Fig.4.15a), which means that the HfO_2 layer is very homogeneous along the wafer. However, in the case of MGIS devices, larger deviations in both, the currents measured before the forming (Fig.4.15b) and V_F (Fig.4.15c) are observed. Although the V_F varies ranging from 2 V to 5.5 V, the I-V curves and Weibull distribution of the MGIS devices can be classified into three differentiated groups (Fig.4.15b and c). In Group 1 (G1, black in Fig.4.15b and c) the I-V curves have similar shape to those of the MIS devices, but with higher currents and smaller V_F. In this case, the graphene layer underneath the metal electrode could have been somehow damaged and/or broken during the transference process or the metal deposition, allowing the direct contact between the metal electrode and the HfO_2, thus leading to such large level of current. Group 3 (G3, blue lines in Fig.4.15a and c), however, shows an erratic and much smaller conductivity and higher V_F than MIS devices. This behavior could be related to other kind of gross defects such as undesired multiple layers, wrinkles or remaining polymer residues from the transference process affecting the conduction through the device. Finally, the Group 2 (G2, red in Fig.4.15b and c) concentrates the higher number of devices. In this region, the I-V curves show a lower conductivity and higher V_F, although with a still high variability compared to MIS structures. In these capacitors, a good quality graphene layer seems to have been successfully transferred on top of the oxide, leading to a reduction of the tunneling conduction and an increase of the V_F. However, minor imperfections of the graphene layer or the fabrication process [169] can be the origin of the observed device-to-device variability.

The electrical properties of the MIS and MGIS devices after the forming have been also analyzed. After forming with CL = 0.1 A, I-V curves measured on both the MIS and MGIS devices show the typical irreversible post-breakdown conduction of MIS capacitors, so that RS was not observed. For MIS devices, no reset phenomena was detected even in the case of the smaller CL = 0.1 mA, meaning that the CF formation is in reality irreversible. Since in the analyzed devices the HfO_2 layer is amorphous and RS tends to be observed through the Grain Boundaries of polycrystalline oxides [292], this is actually an expected result after the forming. However, the behavior of the MGIS devices where a CL = 0.1 mA was used is different. While those devices in Group 1 (Fig.4.15b) do not show RS (probably

due to the defects, imperfections of the graphene and/or the fabrication process), some of those in Groups 2 and 3 showed RS after the forming. Fig.4.16a shows an example of two cycles of resistive-switching obtained on the same MGIS device. Note that after the forming (with a CL = 0.1 mA), the device was reset from the LRS to the HRS (RESET1, without any current limit) by applying a RVS with the same polarity (unipolar RS). SET2 and RESET2 correspond to the I-V curves of the second cycle. Therefore, since RS is only observed when graphene is intercalated between the HfO_2 and top electrode, graphene seems to control the formation of the conductive filament (CF), thus avoiding destructive microstructural damage and allowing the observation of RS. Fig.4.16b shows I-V curves of forming processes and their corresponding RESET obtained on different MGIS devices (each color corresponds to one device). Note that the variation of V_F and V_{RESET} among different devices is quiet large, which could be related again to the intrinsic defects of the CVD graphene layer.

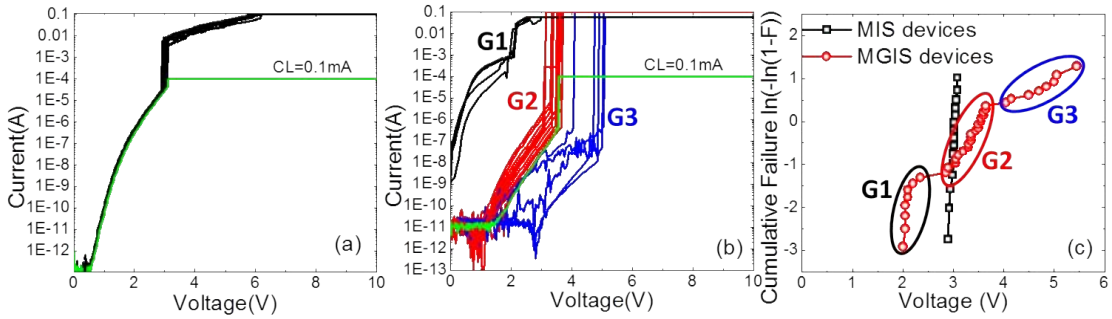


Fig. 4.15. Typical I-V characteristics measured on MIS (a) and MGIS (b) devices for CL = 0.1 A (black, red and blue) and 0.1 mA (green). Only one curve is shown for the case of CL = 0.1 mA because results are equivalent for both cases. (c) shows cumulative distribution of the V_F of both samples, where the three groups of I-V curves measured in MGIS devices in (b) (G1, black, G2, red and G3, blue) can also be observed (c).

The device-to-device variability of the first V_{RESET} and V_F could be observed clearly in the cumulative distribution in Fig.4.17a (solid and open symbols respectively), which could be related to intrinsic defects of the graphene layer. However, when several cycles are sequentially measured on the same device, cycle-to-cycle variability of V_{RESET} (Fig.4.17b, solid symbols) is comparable to that observed between devices. Nevertheless, V_{SET} variability (Fig.4.17b, open symbols) is quite large. This, together with the fact that only few devices showed several RS cycles, allowed us to conclude that when comparing forming, set and reset voltages, V_{SET}

is the less stable and controllable parameter. So the most difficult issue for the observation of RS in the fabricated MGIS devices is to control the set voltage without inducing irreversible CFs.

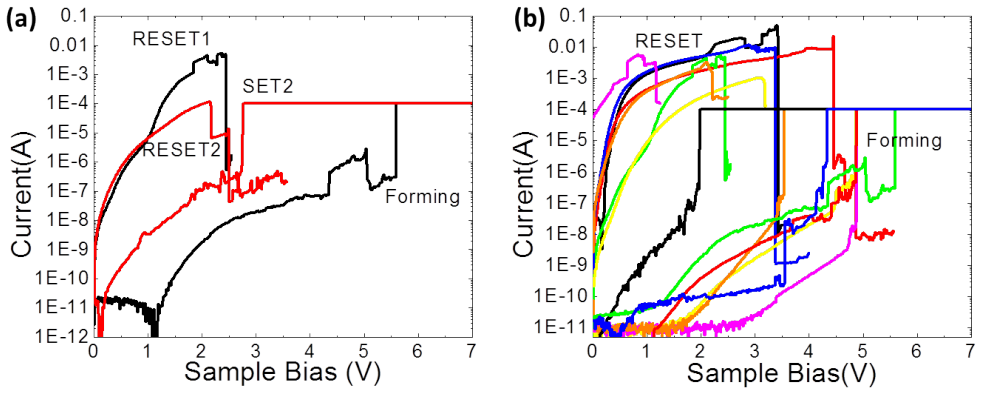


Fig. 4.16. (a) Example of two RS cycles measured on the same MGIS device, (b) Forming process and corresponding reset process obtained on several MGIS devices. Note that one color corresponds to one device.

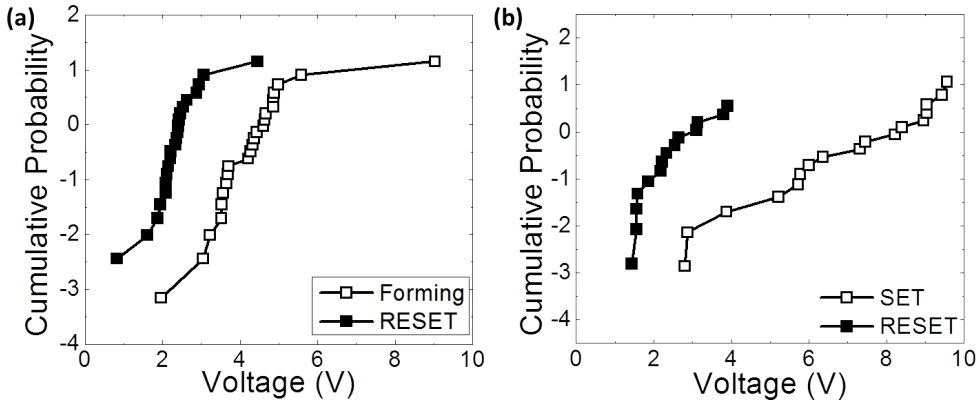


Fig. 4.17. (a) V_F (open symbols) and the first V_{RESET} (solid symbols) of different devices. (b) V_{SET} (open symbols) and V_{RESET} (solid symbols) for several cycles in one device.

Regarding the process of formation of conductive paths we identify two different phenomena. In the MIS structures, the Ti metal electrode favors the diffusion of oxygen atoms owing to ease of Ti to react with oxygen [293] (Fig.4.18a). Because of the size (quite large) of the electrode and the small thickness of the oxide, this process becomes irreversible. With the intercalation of a graphene layer (MGIS structure) the contact between the Ti and the HfO_2 is avoided, thus preventing the generation of oxygen vacancies. Moreover, the relatively high forming voltages and

the non-polar phenomenology indicate that the conduction paths may occur owing to diffusion of Ti atoms (Fig.4.18b), that could diffuse through structural defects of the CVD graphene layer, for example grain boundaries. Therefore, intercalating a graphene layer avoids the irreversibility of the CF formation that occurs in the MIS structures. In spite of that, topographic defects on the graphene layer can degrade its electronic properties, increasing the variability between devices.

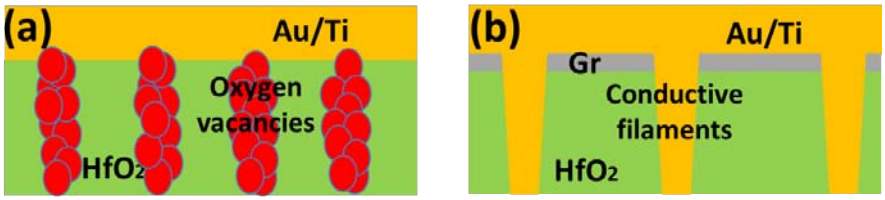


Fig. 4.18. Schematic illustration of the formation of conductive filament based on (a) oxygen vacancies in MIS devices, (b) diffusion of Ti atoms in MGIS devices.

At the Nanoscale

The role of the graphene layer on the formation of the CF in devices with graphene as interfacial layer was also investigated at the nanoscale with CAFM. To perform this study, structures as those shown in Fig.4.19a, that is, without top electrode, were used (GIS structures). Identical structures without graphene were also considered as reference (IS structures, Fig.4.19b). Remember that during the CAFM measurements, the tip will act as a top (metallic) electrode, so that we will still talk about MIS and MGIS structures. In both structures, RVS (without CL) were applied at different sites until the CF was formed.

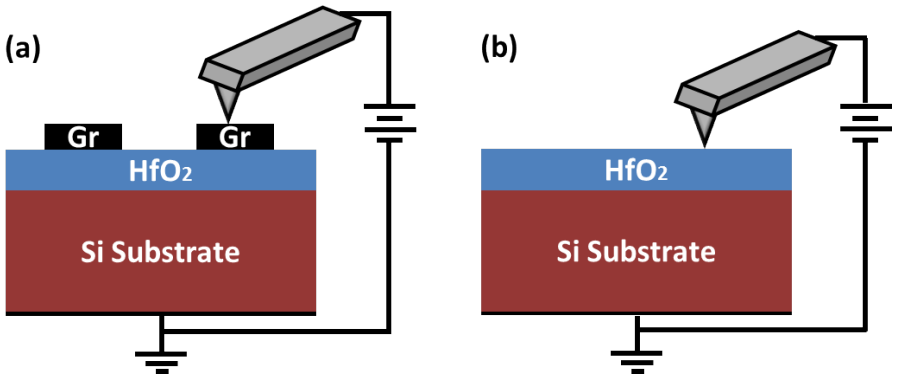


Fig. 4.19. Scheme illustrating the experimental configuration of nanoscale, the CAFM tip plays the role of the top electrode.

Examples of I-V curves measured with the CAFM in MIS (open symbols) and MGIS (solid symbols) structures are shown in Fig.4.20. On each sample, two I-V curves were measured. The first one led to the formation of the CF, while the second one measured the post-forming conduction. Note that the currents measured with CAFM (Fig.4.20) are smaller (at a given voltage) compared to those registered at device level (Fig.4.16a). This is because the area through which current is collected with the CAFM is smaller. While at device level the current is measured through the whole gate area of the device (80x80 μm^2), in CAFM experiments only the current through the contact area between the tip and the sample is registered. This contact area is much smaller ($\sim$300 nm^2 on oxides), leading to lower currents. The area through which current can flow would also explain the higher currents measured with AFM in MGIS structures (compared to MIS structures): although the physical contact area of the CAFM tip with the surface is similar in both cases, the conduction area in the MGIS devices is larger because graphene is not an insulator. In both structures (MIS and MGIS), the second I-V curve measured at the same site shows a higher conductivity, demonstrating that the CF was actually formed.

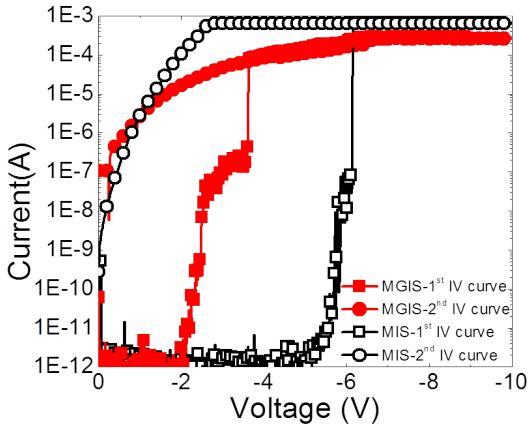


Fig. 4.20. Forming and the next I-V curve measured on MIS (black, open symbols) and MGIS (red, solid symbols) structures measured with CAFM. The maximum current measurable by the setup is 1 mA.

After the formation of the CF, topographical and current maps of the areas where the CFs were created were measured with the CAFM. Fig.4.21 shows topographic (b and e) and current (c and f) images obtained with the CAFM at a gate voltage of 0.1 V on the gate area of a MIS (a, b and c) and MGIS (d, e, and f) structure

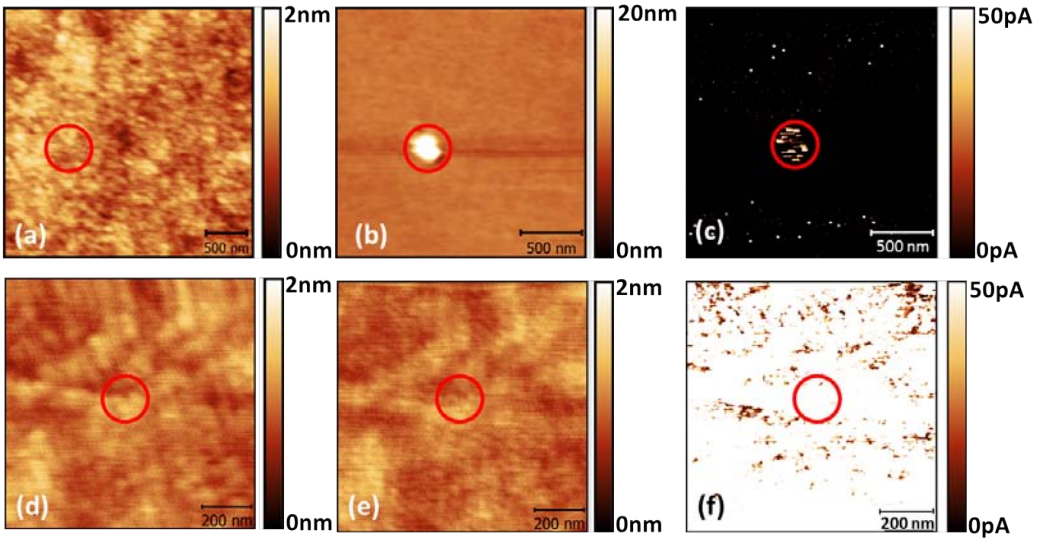


Fig. 4.21. Forming and the next I-V curve measured on MIS (black, open symbols) and MGIS (red, solid symbols) structures measured with CAFM. The maximum current measurable by the setup is 1 mA.

(recall that in this case, the top electrode was the tip) where the I-V curves were measured inside the circles. For comparison, Fig.4.21a and4.21d correspond to topographical images obtained before the RVS were applied. In the MIS structure, at the site where the CF was created, a hillock in the topography (Fig.4.21b), not measured before the RVS (Fig.4.21a), was observed (6 nm high), indicating that the oxide has been seriously damaged [294]. Moreover, higher currents (120 pA at 0.1 V) than in the rest of the oxide are also registered at the same site, as expected, since a conductive path was created between the two electrodes. In this case, the CF formation has been irreversible and uncontrolled and has completely destroyed the oxide, leading to hillocks that could be related to Dielectric Breakdown Induced Epitaxy (DBIE) [295], (damage induced in the oxide microstructure due to thermo-chemical effects) and/or to charge trapping at the conductive filaments [294]. In MGIS devices, however, no significant changes were observed in the topographical images measured before and after the CF formation (Fig.4.21d and 4.21e). Note that the current image (Fig.4.21f) measured in the MGIS structure shows larger currents than those registered in the MIS device in all the analyzed area (because of the larger conduction area, as suggested to explain the current differences between MIS and MGIS structures in Fig.4.20). Therefore, current images in Fig.4.21c and 4.21f are not directly comparable. Despite that, note

that in Fig.4.21f (MGIS structure), no spot with remarkable larger currents is measured, suggesting that CF cannot be distinguished from the background current. Therefore, these results further demonstrate that graphene somehow protects the structure during the CF formation, avoiding catastrophic damage and allowing the observation of RS (Fig. 4.16).

To conclude this section, the fabrication of MGIS devices has been demonstrated. Moreover, the transference process of CVD graphene single layer has been improved. Besides, the variability of the CF forming and their RS properties of capacitive structures with thin HfO_2 layers as dielectric and graphene as interfacial layer between the dielectric and the top electrode (MGIS devices) have been analyzed (at device level and at the nanoscale, with CAFM) and compared to identical devices without graphene (MIS devices). Due to the graphene quality and/or transfer process, the device-to-device variability of the MGIS structures, especially that of the set voltage, is large when compared to standard MIS capacitors. However, the intercalation of the graphene layer prevents the microstructural irreversible damage of the HfO_2 layer resulting in non-polar resistive switching, which was not detected in devices without graphene. This observation suggests the potential use of the MGIS structures as RRAM devices. Further work should be performed both on the improvement of the quality of graphene layer and deeper study of the RS phenomenon.

Chapter 5

Conclusions

The progressive scaling of CMOS technologies has allowed improving the performance of present integrated circuits (IC) and memory devices. This scaling has been possible thanks to the introduction of new materials and/or processes (high-k dielectrics, metal electrodes, strained channels, III-V alloys as channel materials...) in the MOSFET and/or the modification of its architecture like multi-gate FET, FinFET, gate-all-around MOSFET etc... However, as semiconductor technology scaling reaches a sub-nanometer regime, several reliability problems, which were second order effects in the past, become increasingly important with each technological node. For example, in the high-k based devices, the aging mechanisms in traditional SiO_2 based transistors such as the effects of Bias Temperature Instabilities (BTI), channel hot carrier (CHC) and dielectric breakdown (BD) are even more harmful, and additional mechanisms appear, which must be understood in order to correctly determine the device lifetime and minimize their effects. On the other hand, regarding memory devices, the reversibility of the Conductive Filament (CF) formation in MIS/MIM structures has demonstrated to be very promising for future non-volatile memory applications, as those based on Resistive Random Access Memory (RRAM) technology, which is based on the Resistive Switching (RS) phenomenon. However, many technological issues are still open, as those related to the electrodes, since the RS mechanism is strongly influenced by the electrode properties. Due to its special properties, the use of graphene as electrode in RRAM devices could offer great advantages. However, the graphene-based devices still suffer from reliability and variability issues. Since all the aging mechanisms afore-

mentioned and the CF formation are phenomena that take place at the nanometer scale, the application of Atomic Force Microscope (AFM) based techniques such as Conductive AFM (CAFM) to the analysis of these topics naturally appears.

This thesis has contributed in the field of the reliability and electrical properties of MOSFETs and RRAM devices. CAFM has been used to investigate the effects of aging mechanisms (as NBTI and CHC) in the gate stack of unstrained and strained MOSFETs. The leaky spots and their electrical properties on as-grown MOS structures have also been studied at different temperatures with CAFM. On the other hand, conductive filaments (CFs) in MIS structures and the electrical properties of MIS devices with an interfacial layer of graphene between the dielectric and the metal electrode (MGIS structures) have been studied at device level and at nanoscale with CAFM.

The impact of Negative Bias Temperature Instabilities (NBTI) and channel hot carrier (CHC) stresses on the gate electrical properties of SiON based MOSFETs has been investigated by combining standard device-level characterization techniques and CAFM. The main results can be summarized in the following points:

- The high lateral resolution of CAFM has allowed investigating the differences of the degradation induced along the channel.

- Comparing non-stressed with NBTI and CHC stressed MOSFETs, a larger number of leaky sites and larger currents are measured along the channel after the stress, which suggests a larger degradation in stressed devices.

- The effect on the gate oxide after NBTI stress is homogeneous, while in the case of CHC-stressed MOSFETs the regions close to the source and drain show a larger degradation than in the center of the channel, indicating the non-uniformity of the CHC stress.

- TCAD simulations of the parameters involved in the CHC stress (oxide voltage drop and impact ionization) suggest that the generated defects close to source and drain can be attributed to NBTI and CHC degradation, respectively. However, although the aging mechanisms are different, from the gate oxide conductivity point of view, the generated defects have similar characteristics.

The electrical characteristics of locally strained MOSFETs (at the source and drain regions) before and after NBTI and CHC stresses have also been analyzed and compared to identical devices without strained channels. In particular, the impact of the stress on the drain current, I_D (measured at device level), and on the gate current, I_G, at different regions of the channel (measured at the nanoscale with CAFM) has been studied on devices with different channel lengths. The main results are:

- When comparing with non-strained MOSFETs, the channel mobility of strained MOSFETs increases in both long and short channel devices. In particular, the increment is larger in short channel devices.

- However, the transistors subjected to local strain are more sensitive to CHC and NBTI degradation, leading to a higher reduction of I_D and higher I_G in both CHC- and NBTI-stressed devices. Moreover, strained MOSFETs with short channel lengths are more sensitive to a CHC stress than those with large channel lengths.

- After CHC stress, this effect could be related to a higher defect generation in strained devices, especially at the channel close to source and drain, since a larger increase of the gate current was detected with CAFM in these regions compared to unstrained devices.

CAFM has also been used to study leaky spots at different temperatures (T) on as-grown SiON layers. The main results can be concluded as following:

- Switching between different conduction states has been measured during constant voltage tests in the form of RTN, which has been related to the trapping/detrapping of single charges in defects present in the dielectric.

- The measurement of current maps at different T suggests that the detected leaky sites correspond to defects, whose activation depends on T and that are randomly distributed in the gate area.

- Therefore, these results demonstrate that the CAFM allows the analysis not only of failure mechanism associated to an electrical stress, but also the electrical characteristics (and their dependence on T) of single defects present in

as-grown dielectrics.

Conductive Filaments (CFs) in MIS (Ni/HfO_2/Si) structures for RRAM applications have been observed and analyzed with CAFM when the device has been left in the Low Resistive State (LRS) and High Resistive State (HRS). The impacts of Current Limit (CL) in these structures have also been investigated. The main results are the following:

- Independently on the device state (LRS or HRS), the CFs are formed in a unique spot that can be detected as a hillock in the topography image after the removal of the Ni electrode.

- Local electrical analysis of the HRS and LRS spots reveals a non-uniform conduction, with some regions in the spots with significantly higher conductivity. Moreover, in the LRS spots, the portion of the CF area with higher currents is larger than in the HRS, which would explain the larger LRS conductivity observed at device level.

- This behavior is compatible (although not a definitive conclusion) with the tree-shaped model of CF formation: some branches of the CF would span all along the dielectric thickness, connecting the two electrodes, whereas some others would end within the dielectric. Then, when scanning with the CAFM tip, larger currents would be measured in the first case whereas lower currents would be observed in the second case.

- When a higher CL is used during the forming process, not only the affected area but also the conductivity of the different CFs is shown to be larger at nanoscale. Therefore, the higher current measured at device level with high CLs can be attributed not only to an increase of the affected area but also to the current through the different CFs.

Finally, MIS (Au/Ti/HfO_2/Si) structures with graphene as the interfacial graphene layer between the top electrode and dielectric (MGIS devices) in for RRAM applications have been fabricated and investigated. The electrical properties and variability of these structures have been analyzed at device level and at nanoscale with CAFM and compared to devices without graphene. The results are:

- Regarding the fabrication of MGIS devices, the transference process of CVD-grown graphene from copper to the gate dielectric has been improved by two following steps. First, before the removal of PMMA, the sample is heated to relax the PMMA. Moreover, instead of acetone, acetic acid was used to remove the PMMA. The relaxation of the PMMA layer allows a good contact between the graphene single layer and the substrate surface. The cleaning with acetic acid seems to decrease the possibility of the stripping of graphene single layer from the substrate, lowering the formation of holes, and it seems to be more efficient eliminating the PMMA than acetone.

- When comparing to standard MIS capacitors, the device-to-device variability of the structures with graphene as interfacial layer (MGIS devices), especially that of the set voltage, is larger due to the graphene quality and/or transfer process.

- However, the intercalation of the graphene layer prevents the microstructural irreversible damage of the HfO_2 layer, resulting in non-polar resistive switching, which was not detected in devices without graphene. This observation suggests the potential use of the MGIS structures as RRAM devices.

To conclude, this thesis has shown that CAFM is a very useful tool to study the reliability of MOSFETs and resistive switching phenomenon in RRAM applications. The nanometer resolution of CAFM has allowed to investigated not only the details of the impact of the failure mechanisms on gate oxides, but also the electrical characteristics of single defects present in as-grown dielectrics. Moreover, the CAFM has also been used to study the nanoscale morphological and electrical properties of the CFs present in MIS and MGIS devices for RRAM applications.

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PUBLICATIONS 1-3

A Conductive AFM Nanoscale Analysis of NBTI and Channel Hot-Carrier Degradation in MOSFETs

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***Abstract*— This paper addresses the impact of different electrical stresses on nanoscale electrical properties of the MOSFET gate dielectric. Using a conductive atomic force microscope (CAFM) for the first time, the gate oxide has been analyzed after bias temperature instability (BTI) and channel hot-carrier (CHC) stresses. The CAFM explicitly shows that while the degradation induced along the channel by a negative BTI stress is homogeneous, after a CHC stress different degradation levels can be distinguished, being higher close to source and drain.**

***Index Terms*— Atomic force microscopy (AFM), channel hot-carrier (CHC) degradation, MOSFET, negative bias temperature instability (NBTI).**

I. Introduction

THE unstoppable development of the semiconductor industry requires the continuous increase of the computing power of most electronic devices [1]. As a consequence, electron devices, like the MOSFET, have experienced a spectacular reduction in their physical size in the last years.

This has presented a challenge for the reliability researchers, mainly due to the persistent increase of the electric fields in nanoscaled devices, which can trigger different aging mechanisms. Channel hot-carriers (CHC) degradation, bias temperature instabilities (BTI), and time-dependent dielectric breakdown (TDDB) have been identified as the most relevant degradation mechanisms in MOSFETs [1]. In the last decades, BTI has become more detrimental than the CHC degradation [2]. Nevertheless, for the recent technology nodes, CHC degradation has acquired a renewed relevance because the supply voltage reduction is slowing down, thus increasing the lateral electric field in the device. The BTI and CHC aging involve the generation of defects at the gate oxide/Si interface and/or oxide bulk. These defects modify several device parameters (threshold voltage and carrier mobility in the channel) during the device operation, which could affect the circuit performance [3].

The bias temperature instability is the result of the application of a negative/positive voltage [negative BTI (NBTI)/positive BTI, respectively] to the gate terminal, with its effects enhanced at high temperatures. On the other hand, CHC is basically caused during the MOSFETs ON-state, when the transistors are subjected to a gate voltage (V_G) larger than the threshold voltage and, simultaneously, to a drain voltage (V_D) larger than the saturation drain voltage. This voltage configuration produces a maximum electric field located close to the drain region, which provokes the injection into the gate oxide near the drain of high-energetic electrons and holes (hot-carriers) created by impact ionization. Considering the electric field distribution in the device during BTI and CHC stresses, the oxide damage is expected to be uniformly distributed over the gate oxide area for BTI aging, whereas it should be mostly located close to the drain for CHC degradation. The CHC nonuniform aging has been experimentally evidenced by the different measured values of the drain current when the roles of source and drain are interchanged during device test [4]. However, details on the spatial distribution of damage after applying an electrical stress can only be revealed using other high-resolution characterization techniques. In this sense, conductive atomic force microscopy (CAFM) is recognized as a very effective technique to provide valuable information about the nanoscale electrical properties [5]–[7] and failure mechanisms (as TDDB) [8]–[12] associated with the MOSFET gate dielectric. Working on a bare gate oxide, the conductive tip of CAFM plays the role of the gate electrode, defining a MOS capacitor with an area that corresponds to the contact region between the tip and the sample [12]. Because this area is very small (it has been experimentally estimated to be $\sim$100 nm^2 [12]), the technique opens the possibility to perform a nanoscale electrical characterization with a resolution of $\sim$10 nm. Some studies based on the gate oxide aging under electrical stress have been already performed, but most of them use the AFM tip as the gate electrode for stress and age monitoring [12]. Nonetheless, due to experimental limitations, few works have combined device level stresses and nanoscale characterization to analyze the impact of such stresses on

Manuscript received July 23, 2013; revised March 26, 2014, May 15, 2014, and July 9, 2014; accepted July 16, 2014. Date of current version August 19, 2014. This work was supported in part by the Spanish Ministerio de Ciencia e Innovación under Grant TEC2010-16126 and Grant GICSERV5-NGG120 and in part by the Generalitat de Catalunya under Grant 2009SGR-793. The review of this paper was arranged by Editor E. Rosenbaum.

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Digital Object Identifier 10.1109/TED.2014.2341315

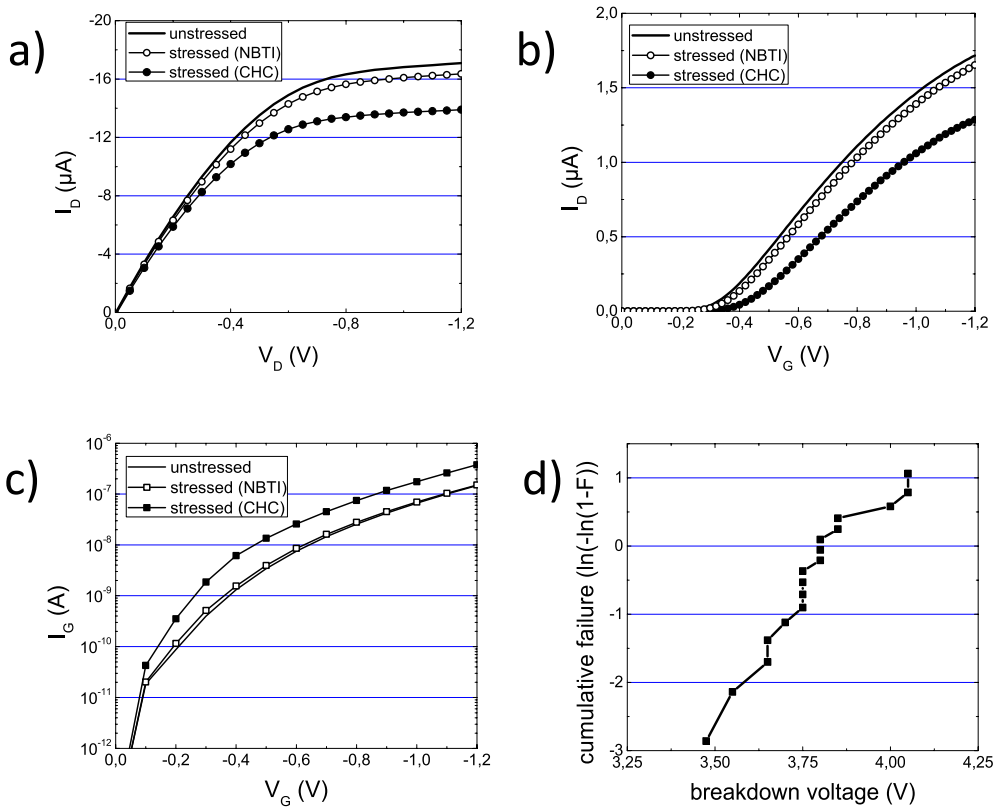


Fig. 1. Typical (a) I_D–V_D, (b) I_D–V_G, and (c) I_G–V_G characteristics of a MOSFET recorded before (continuous line) and after NBTI (open symbols) and CHC (full symbols) stress. (d) Breakdown statistics from which V_{BD} (63%) was estimated.

the nanoscale gate oxide properties [13]. The combination of both analyses is specially difficult because once the device is stressed and its electrical properties are analyzed, the structure under investigation must be deprocessed to expose the gate oxide to the CAFM tip. Therefore, many experimental difficulties may appear. In this sense, the studied structures should allow an easy gate electrode removal and should have the proper dimensions for the scanning of the whole gate area of the device. Such experimental difficulties are specially remarkable in the case of MOSFETs. As a consequence, the few studies performed in this direction have been focussed on MOS capacitors and, therefore, these works are restricted to stresses that are uniform over the gate active area [13] such as BTI. In this paper, the nanoscale electrical properties of the gate oxide of MOSFETs after homogeneous (BTI) and nonhomogeneous (CHC) device level stresses have been studied with CAFM. Because with the CAFM tip very small areas can be analyzed, the measurement of the bare oxide electrical properties enables evaluation of the degradation induced in the different regions of the gate oxide along the channel.

II. Experiment

The pMOSFETs ($L = 1\ \mu$m and $W = 0.5\ \mu$m) with a 1.4-nm-thick SiON layer as gate dielectric have been analyzed. The gate electrode consisted of a 60-nm-thick layer of polysilicon and a 40-nm-thick layer of NiSi. Some devices were subjected to NBTI stress by applying -2.6 V at the gate, and others were subjected to CHC stress by applying -2.6 V at the drain and gate, while the other terminals were grounded. In both cases, the stress time was 200 s. Other transistors, acting as a reference, were not stressed. In the case of CHC stress, the voltage configuration ($V_G = V_D$) is the most damaging stress condition for pMOSFETs [14], [15] because it provokes a larger hole injection into the oxide [15]. A current compliance of 1 mA was fixed during the stress. Fig. 1(a)–(c) shows typical I_D–V_D, I_D–V_G, and I_G–V_G characteristics obtained before (continuous line) and after a NBTI (open symbols) and CHC (solid symbols) stress. The poststressed characterization revealed a threshold voltage shift of 25/125 mV with respect to nonstressed devices. In addition, a decrease of 4/19% in the drain current at $V_D = -1.2$ V and an increase of 4/227% in the gate current at $V_G = -1$ V was observed for NBTI and CHC stressed devices. The breakdown voltage was also estimated from the I_G–V_G characteristics obtained after applying ramped voltage stresses to the gate of some MOSFETs [Fig. 1(c)]. The V_{BD}(63%), that is, the voltage for a 63% probability of BD occurrence, was estimated to be 3.8 V.

Once the device level stress (NBTI or CHC) was applied, and the device aging characterized, the polysilicon and NiSi layers on top of the gate dielectric were removed. This removal was carried out using a very selective wet etch, allowing exposure of the upper surface of the gate dielectric to the CAFM tip. During the etching, the device was immersed in an 85% phosphoric acid solution, at a temperature of 125 °C, for 90 s. After the etching, the gate oxide was scanned with the AFM tip with the purpose of investigating its morphology. Fig. 2 shows a typical 3-D topography map obtained for a

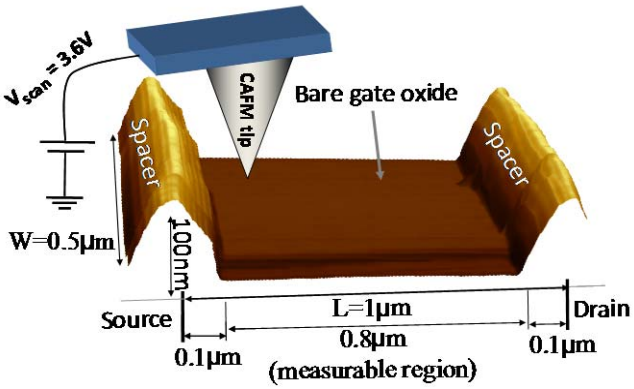


Fig. 2. AFM 3-D topographic image of a pMOSFET after the removal of the gate electrode, showing a very flat surface (RMS < 0.2 nm) between the two spacers. Placing the CAFM tip on the gate oxide region, the conduction through the oxide can be studied with nanometer lateral resolution. The dimensions of the area under study and the applied polarization voltage are indicated.

MOSFET. Note that the gate region can be easily distinguished and measured between the two spacers. However, the presence of such sidewall spacers limits the possibility of measuring at the extreme edges of the channel (<0.1 or >0.9 μm) because they impede the CAFM tip (which has a conical shape) contacting the gate area (Fig. 2). The roughness of the exposed dielectric was determined to be below 0.2 nm, which is comparable with values reported in [16]. This value demonstrates that the gate oxide is not affected by the removal of the top electrode.

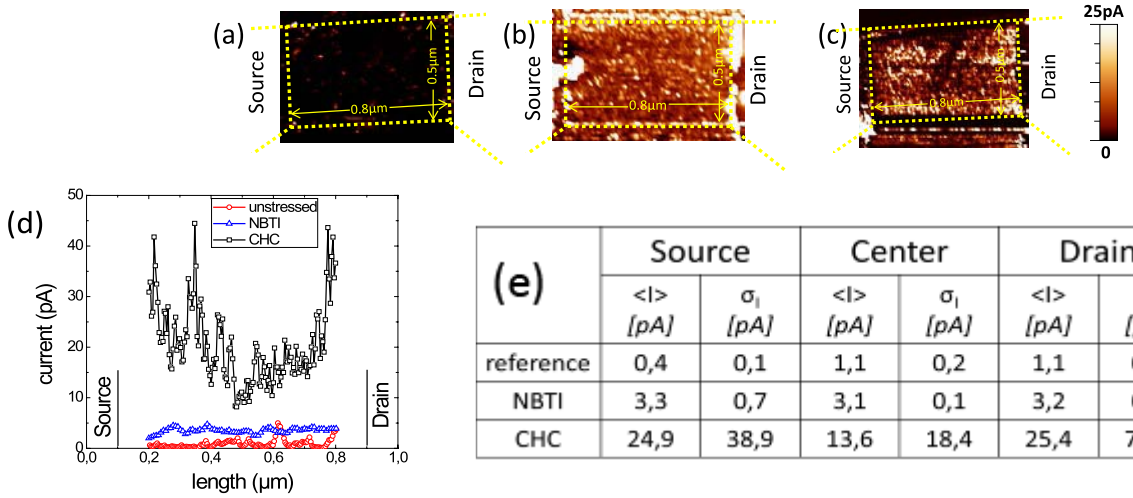
The nanoscale electrical properties of the dielectric were studied by scanning the bare gate area with the CAFM tip (Fig. 2). In this paper, PtIr-coated Si tips with a nominal tip radius of 20 nm were used. When the structure is polarized, current can flow through the gate, and the electrical properties of nanometer sized regions of the dielectric can be evaluated. To avoid anodic oxidation [17], [18], we positively polarized the tip (substrate injection of negative charge carriers) and carried out the CAFM measurements in dry nitrogen ambient, keeping the humidity level inside the AFM chamber below 0.5%. It should be mentioned that maximum currents of 10 nA can be measured due to the saturation of the electronics of the setup. An important point that must be emphasized when performing conductivity measurements with CAFM, is that the currents measured with this technique are very sensitive to several experimental factors. These factors are related to the contact area between the tip and the sample and the resistivity of the tip, which can vary from tip to tip and even during the measurements due to the tip wear out or the average thickness fluctuations between samples. Therefore, the comparison of absolute values of the currents measured in different samples may not be really meaningful and only relative variations in the same sample are reliable. Consequently, in this paper, we will focus on the conductivity variations along the channel for a given sample.

III. Results and Discussion

The gate oxide electrical properties of several devices before and after the electrical stress have been studied at the nanoscale with the CAFM. Four unstressed, five NBTI stressed, and nine CHC-stressed MOSFETs have been measured. Fig. 3(a)–(c) shows, respectively, examples of typical current maps (on the same current scale, 25 pA) obtained on reference (nonstressed), NBTI-, and CHC-stressed MOSFETs [19], where the measurable gate area has been delimited by a dotted line. In all cases, current images were obtained by applying +3.6 V to the tip (substrate grounded). This voltage is high enough to be able to measure current above the noise level of the setup, but low enough to avoid the breakdown of the gate-stack (see Section II). Although this voltage could induce an additional stress to the gate oxide, the differences observed between the three images of Fig. 3 should be attributed to the device level stress and not to the AFM scan, because all devices (reference, NBTI-, and CHC-stressed MOSFETs) were scanned at the same voltage. In addition, it is important to note that although the etching process could somehow affect the gate dielectric, because all samples were subjected to the same etching, similar effects should be observed in the studied MOSFETs and, if different, they should be randomly observed in the different set of samples.

In the unstressed samples, [Fig. 3(a)], currents corresponding to the noise level of the setup are measured, which indicates that the conductivity of the fresh sample could be even smaller. However, in all the stressed (NBTI and CHC) MOSFETs, brighter areas, representing larger currents (which correspond to leaky sites in the dielectric) were observed. The comparison of the images in Fig. 3(a) (nonstressed sample) with the images in Fig. 3(b) (NBTI stressed sample) and Fig. 3(c) (CHC stressed sample) allows the conclusion that: 1) the number of leaky sites in the stressed MOSFETs is considerably larger than in nonstressed devices and 2) the distribution of leaky sites over the gate region can change after applying the stress.

The information obtained in Fig. 3(a)–(c) has been quantitatively evaluated in Fig. 3(d) and (e). Fig. 3(d) shows the averaged current profiles obtained with the CAFM tip at different positions along the channel for the nonstressed (circles) and NBTI (triangles) and CHC (squares) stressed MOSFETs. It should be remarked that absolute comparisons between samples are not meaningful. Therefore, we will focus on variations within the same sample only. In the unstressed sample, the current is close to the noise level of the CAFM and homogeneously distributed along the channel. The stressed MOSFETs (triangles and squares) always show larger currents than the nonstressed device. In this case, the difference is so large that it can be easily detected. However, a difference between NBTI- and CHC-stressed MOSFETs can be observed: the former always shows a homogeneous distribution of the current along the channel, whereas in CHC-stressed MOSFETs larger gate currents can be measured in the regions close to the junctions. The table in Fig. 3(e), which shows the rms value, σ_I, and average current, $\langle I \rangle$, measured in a $W \times 0.05$ μm^2 region in Fig. 3(d), located close to the source, close to the drain, and at the center of the channel of the three MOSFETs, further supports these observations. Note that in the CHC-stressed MOSFET, the current close to the source



(e)	Source		Center		Drain	
	<I> [pA]	σ_I [pA]	<I> [pA]	σ_I [pA]	<I> [pA]	σ_I [pA]
reference	0,4	0,1	1,1	0,2	1,1	0,9
NBTI	3,3	0,7	3,1	0,1	3,2	0,1
CHC	24,9	38,9	13,6	18,4	25,4	75,6

Fig. 3. Typical current images obtained at a gate voltage of 3.6 V in (a) nonstressed, (b) NBTI-, and (c) CHC-stressed MOSFETs. (d) Average current measured with the CAFM tip along the channel for the nonstressed (circles), NBTI (triangles), and CHC (squares) stressed MOSFETs. (e) Table indicating the average and dispersion of the current measured in $W \times 0.05\ \mu m^2$ regions taken in (d), close to the source, drain, and at the center of the channel. In (b)–(e), the effect of the degradation induced by the previous NBTI and CHC stress, where larger currents (brighter areas) are evident for stressed devices. These brighter areas are nonuniformly distributed after CHC stress.

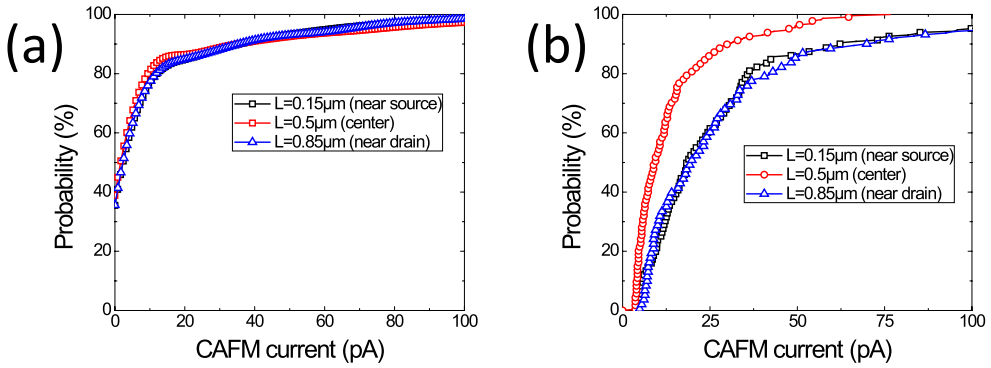


Fig. 4. Cumulative distributions of the current measured with the CAFM in 0.05 μm^2 regions centered close to the source ($L = 0.15\ \mu m$) and drain ($L = 0.85\ \mu m$) and in the center of the channel ($L = 0.5\ \mu m$), for (a) NBTI- and (b) CHC-stressed MOSFETs.

and drain is higher than in the center of the channel and also shows a higher dispersion. However, in unstressed and NBTI-stressed MOSFETs, the current distributions are more homogeneous, although a larger dispersion was measured after the NBTI stress.

The spatial distribution of the leaky sites has been analyzed in more detail from the current images. Randomly located leaky spots are measured on the fresh oxide, which can be assigned to currents through native defects and/or local thinning of the dielectric [6]. On the previously stressed dielectrics, however, the number of leaky sites is larger, and they are more conductive. In this case, these spots can be considered to be related to the defects generated during the stress. In addition, because the current through the leaky spots does not reach the CAFM maximum current and the device level measurements did not show a post-BD behavior in the gate current, they cannot be BD spots. Consequently, the current measured with the CAFM through the stressed oxides can be assumed to be indicative of the degradation induced during the NBTI or CHC stress. Therefore, the current images in Fig. 3(b) and (c) lead to the conclusion that in the case of CHC-stressed MOSFETs, the degradation in the gate is specifically concentrated close to source and drain regions.

To accurately analyze the distributions of the generated defects along the channel, the cumulative distribution of currents measured in 0.05-μm^2 regions centered at channel distances $L = 0.15$ and $0.85\ \mu m$ (i.e., close to source and drain respectively), and $L = 0.5\ \mu m$ (in the center of the channel) are represented in Fig. 4(a) for NBTI, and in Fig. 4(b) for CHC-stressed MOSFETs. Note that in the case of the NBTI-stressed devices [Fig. 4(a)], similar cumulative distributions are found in the three regions. On the other hand, after the CHC stress [Fig. 4(b)], lower currents are measured in the center, whereas larger currents are shown in the distributions measured close to the junctions. The current distributions at the extremes of the channel do not show remarkable differences between them, which indicates that a similar degradation effect is produced close to the source and drain areas. To explain this result, it should be considered that the NBTI degradation measured by CAFM is mainly due to the

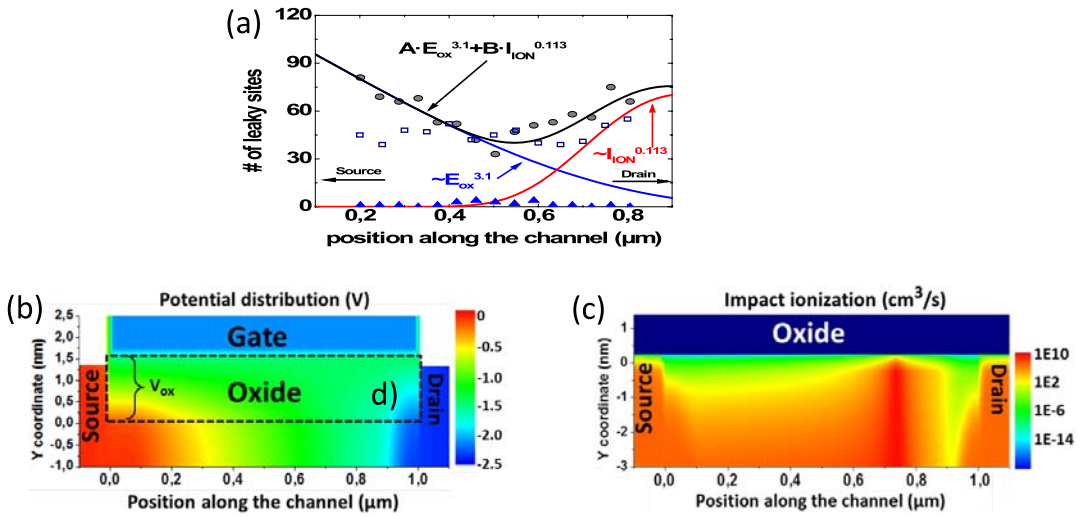


Fig. 5. (a) Average number of leaky sites (CAFM current >10 pA) obtained at different positions along the channel in fresh (triangles), NBTI (squares), and CHC (circles) stressed devices, obtained from 20 current profiles registered along the channel width in the current images in Fig. 3. Lines correspond to the fitting of the number of leaky sites to $A \cdot E_{ox}^{\gamma}$ (blue) and $B \cdot I_{ion}^{\alpha}$ (red) and their sum (black). (b) TCAD simulation of the potential distribution and (c) impact ionization for a pMOSFET at the stress conditions used to obtain the E_{ox} and I_{ion} profiles along the channel.

permanent NBTI component (several days passed between the electrical stress and the CAFM characterization). Therefore, Fig. 4(b) suggests that the CHC stress and the permanent NBTI could have a similar origin, as suggested in [19], where both mechanisms were associated to the creation of interface states.

The number of leaky sites on reference and stressed samples has also been analyzed, as determined from 20 current profiles along the channel width, extracted from the current maps of Fig. 3. For each kind of sample (reference, NBTI- and CHC-stressed MOSFET), the profiles were obtained on the same device (Fig. 3). Fig. 5(a) shows the average number of leaky sites that show currents larger than 10 pA versus their position along the channel. Squares and circles correspond, respectively, to NBTI- and CHC-stressed MOSFETs, while triangles show the data corresponding to the unstressed transistor. Clearly, the number of leaky sites is larger in stressed (both NBTI and CHC) MOSFETs. In addition, in the CHC-stressed MOSFET, leaky sites are mostly located close to the junctions, whereas in the NBTI stressed and fresh oxides the spots are uniformly distributed across the channel.

The TCAD simulations of a pMOSFET under CHC stress bias have been performed to explain the experimental distribution of leaky sites observed with CAFM [circles in Fig. 5(a)]. In particular, the potential distribution [Fig. 5(b)] and the impact ionization, I_{ion}, [Fig. 5(c)] at the CHC stress conditions have been obtained. The dashed rectangle in Fig. 5(b) indicates the region that corresponds to the gate oxide. As expected, the potential distribution in the oxide is clearly not uniform along the channel direction. The voltage drop at the gate oxide (V_{ox}) is especially large close to the source because of the different bias applied to the gate and source terminals (−2.6 and 0 V, respectively). In contrast, V_{ox} is small close to the drain because the same voltage is applied at gate and drain terminals during the CHC stress. Consequently, the vertical electric field, which leads to the NBTI degradation, is more intense close to the source, and decreases along the channel direction from source to drain [20], [21]. The impact ionization [Fig. 5(c)] reaches the maximum at a position close to the drain, where the carriers are more energetic. Hence, this position is more susceptible for the hot carrier degradation [20]. Then, the TCAD simulation allows investigation of the two degradation sources during the CHC stress: 1) the high-vertical electric field and 2) the impact ionization. Therefore, the leaky sites of Fig. 5(a) located near the drain should be related to the traps created by impact ionization (I_{ion}) caused by hot-carriers [15]. On the other hand, those leaky sites located close to the source should have been created by the high-electric field applied to the oxide (E_{ox}) during the CHC stress, which can induce NBTI damage as well [14]. In the last case, due to the long time elapsed between the CHC stress and the CAFM characterization (some days), the measured degradation can be related only to the permanent (or slow component) of BTI. Consequently, the damage produced in the oxide seems to be caused by the combination of E_{OX} and I_{ion} effects. In addition, as shown in Fig. 4(b), both aging mechanisms generate a similar effect, at least from the CAFM currents point of view. These observations suggest that their contribution to the number of leaky sites could be additive. This hypothesis can be confirmed by fitting the leaky sites profile in Fig. 5(a). The experimental profile is well reproduced, assuming the contribution of both mechanisms. Blue/red lines show the fit of the data to a potential law on E_{OX}/I_{ion}, that is, to $\sim E_{ox}^{\gamma}$ and to $\sim I_{ion}^{\alpha}$. For the fits, the values of E_{ox} and I_{ion} of Fig. 5(b) and (c) have been considered. From these fits [Fig. 5(a)], exponents of $\gamma = 3.10$ and $\alpha = 0.113$ have been obtained [20]. The extracted γ value is consistent with exponents given in the literature for the permanent component of BTI, which ranges between 3 and 5 [22]. The black line shows that the number of leaky sites can be fitted by the sum of the two exponential laws. Then, the leaky sites profile in Fig. 5(a) can be explained by the combination of permanent damage caused by NBTI in the

region close to the source, and hot-carrier injection close to the drain. In addition, it confirms the degradation scheme proposed from conventional characterization techniques [4], [15], where the CHC degradation is divided in two different stress components: 1) a CHC aging component located at the drain side (pinchoff region) and 2) a BTI-component distributed between the source and the pinchoff region [4], [15]. The CAFM results show, additionally, that, at the nanoscale, from a gate oxide current point of view, the generated defects are not significantly different, though created by different aging mechanisms.

IV. Conclusion

In this paper, a conductive atomic force microscope has been used to investigate the impact of a NBTI and CHC stress on the nanoscale electrical properties of the MOSFET gate dielectric. The high-lateral resolution of the microscope has allowed investigation of the differences of the degradation induced along the channel. The analysis has been performed by considering that the defects generated by electrical stress assist in the process of tunneling through the gate when the tip-sample system is biased. After the stress, a larger number of leaky sites and larger currents are measured, suggesting a larger degradation in stressed devices. However, the degradation of the gate oxide area after the NBTI stress is found to be homogeneous, while in the case of a CHC-stressed MOSFET the regions close to the source and drain show a larger degradation than in the center of the channel. This fact is indicative of the nonuniformity of the CHC stress. The TCAD simulations of the parameters involved in the CHC stress (oxide voltage drop and impact ionization) suggest that the generated defects close to source and drain can be attributed to NBTI and CHC degradation, respectively. However, although the aging mechanisms are different, from the gate oxide conductivity point of view, the created defects are not significantly different.

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Javier Martin-Martínez, photograph and biography not available at the time of publication.

Mario Lanza, photograph and biography not available at the time of publication.

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Channel-hot-carrier degradation of strained MOSFETs: A device level and nanoscale combined approach

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Citation: Journal of Vacuum Science & Technology B **33**, 022202 (2015); doi: 10.1116/1.4913950
View online: http://dx.doi.org/10.1116/1.4913950
View Table of Contents: http://scitation.aip.org/content/avs/journal/jvstb/33/2?ver=pdfcov
Published by the AVS: Science & Technology of Materials, Interfaces, and Processing

Channel-hot-carrier degradation of strained MOSFETs: A device level and nanoscale combined approach

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(Received 30 September 2014; accepted 20 February 2015; published 4 March 2015)

Strained MOSFETs with SiGe at the source/drain regions and different channel lengths have been studied at the nanoscale with a conductive atomic force microscope (CAFM) and at device level, before and after channel-hot-carrier (CHC) stress. The results show that although strained devices have a larger mobility, they are more sensitive to CHC stress. This effect has been observed to be larger in short channel devices. The higher susceptibility of strained MOSFETs to the stress has been related to a larger density of defects close to the diffusions, as suggested by CAFM data. [http://dx.doi.org/10.1116/1.4913950]

I. INTRODUCTION

With the introduction of alternative materials in CMOS technology, some challenges such as large carrier mobility (μ) in the channel must be confronted.[1] In this respect, strain techniques have been presented as an alternative, which can increase the channel mobility[2] and, to a lesser degree, can lead to lower external resistance (making the internal bias of the strained device higher for the same external voltages).[3] Recently, different techniques to introduce strain into the channel of a MOSFET have been developed and can be classified into two main categories:[4] global strain techniques and local strain techniques. In global techniques, the strain is introduced across the entire substrate; however, in local strain techniques, the strain is inserted locally at certain regions. One method of introducing local strain consists in the selective growth of a local epitaxial film in the source and drain regions of a transistor. In n-MOSFETs, a $Si_{1-x}C_x$ layer is epitaxially grown in source/drain (S/D) regions to achieve tensile stress and in p-MOSFETs selective epitaxial growth of SiGe is used to create uniaxial compressive stress.[5] The implementation of strained SiGe in the S/D areas, with a given Ge concentration, leads to an improvement of the drive current in short channel transistors.[2] This improvement is attributed first to the presence of uniaxial compressive stress in the silicon channel, which favorably alters the band structure, enhancing the hole mobility and second to the presence of the highly activated SiGe source/drain regions, which provides a reduced resistivity and series resistance.[6] However, one concern is the possible presence of defects at the SiGe/Si interface and the larger sensitivity of strained MOSFETs to electrical stresses as channel-hot-carrier (CHC) degradation and bias temperature instability.[7]

Since defect generation is a very local phenomenon that takes place in nanoscale areas, high resolution techniques as conductive atomic force microscopy (CAFM) can be very useful to investigate how strain affects the electrical properties of gate stacks. Actually, CAFM has been extensively used to investigate the MOS structures that are subjected to different fabrication processes, as high temperature annealings, which can induce the high-k polycrystallization.[8,9] CAFM has also been used to study the electrical properties of gate dielectrics (SiO_2) and high-k materials.[10–13] In particular, in a recent investigation,[14] it was demonstrated that CAFM is able to study separately the impact of CHC stress on the different regions of the channel of MOSFETs. However, in that case, nonstrained substrates were investigated only. In this work, p-MOSFETs with epitaxially grown SiGe at S/D regions have been subjected to CHC stress and their electrical characteristics have been compared to reference devices without strained channels. In particular, the impact of the stress on the drain current, I_D (measured at device level), and on the gate current, I_G, at different regions of the channel (measured at the nanoscale with CAFM) has been studied on devices with different channel lengths.

II. EXPERIMENT

In this work, p-MOS transistors with a 1.4 nm thick SiON layer as gate dielectric and 60 nm polysilicon/40 nm NiSi stack as gate electrode have been studied. In strained devices, the SiGe at S/D regions were selectively deposited with a 15% Ge content [Fig. 1(a)]. These devices were compared to identical p-MOSFETs without strained silicon [reference devices, Fig. 1(b)]. Transistors with different channel lengths ($L = 0.13$, 0.5, 1, and 3 μm) and 1 μm width were considered. Some samples were subjected to CHC stress by applying $V_G = V_D = -2.6$ V for 200 s keeping the other terminals grounded[15] and some other samples were not stressed (fresh samples). Although strain can result in lower external resistance leading to higher internal bias for the same external voltages (compared to nonstrained devices), since the focus of the work is to perform a reliability comparison between both technologies, CHC degradation was induced at the same voltages. Using the same biases allow to evaluate which technology suffers from larger degradation when operation under the same conditions.

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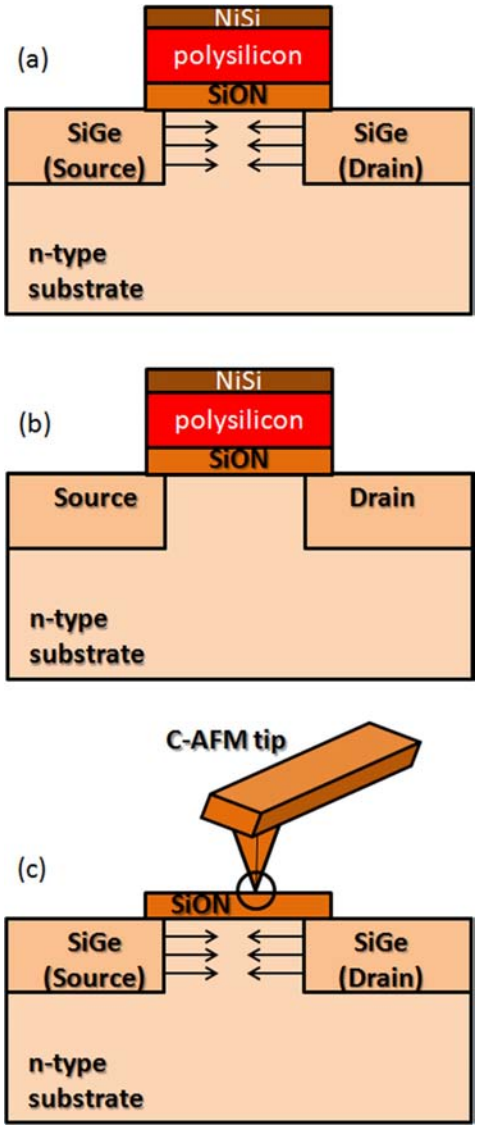

FIG. 1. (Color online) Schematics of strained (a) and unstrained (b) pMOSFETs measured at device level (c). Experimental configuration when the strained devices are studied with CAFM.

Before and after the CHC stress, device level measurements were performed (to get the I_D–V_G, I_D–V_D characteristics), and the device aging was characterized. After the device level analysis, the polysilicon and NiSi layers on top of the gate dielectric were removed with a very selective wet etch to expose the gate dielectric and make it accessible to nanoscale electrical measurements with the CAFM tip [Fig. 1(c)]. The etching consisted of immersing of the sample in a solution of phosphoric acid, 85%, at 125 °C, during 90 s.[14] After the etching, the gate oxide was scanned with the AFM tip to investigate its morphology and electrical properties. When the structure is polarized, current can flow through the gate and the electrical properties of nanometer sized regions of the dielectric can be evaluated. Due to the saturation of the electronics of the CAFM setup, maximum currents of 10 nA can be measured. In this work, PtIr coated Si tips with a nominal tip radius of 20 nm were used.

III. DEVICE LEVEL MEASUREMENT

Since CAFM can only measure the gate current through the dielectric, the device level analysis will allow to investigate the effect of the strain and the stress on the current along the channel, that is, the drain current, I_D. In this section, the electrical characteristics of fresh (before any electrical stress) and CHC stressed devices have been compared on strained and nonstrained MOSFETs at device level. Several channel lengths were also studied. Figure 2 shows typical I_D–V_G [(a), (d), and (g)], I_D–V_D [(b), (e), and (h)], and transconductance (g_m) [(c), (f), and (i)] characteristics of MOSFETs with a 0.13 μm [(a)–(c)], 1 μm [(d)–(f)], and 3 μm [(g)–(i)] channel length. In all plots, solid symbols correspond to strained devices and open symbols to unstrained transistors. Squares and circles correspond to fresh (unstressed) and CHC stressed devices, respectively. The I_D–V_G characteristics were measured at $V_{DS} = -50$ mV and the I_D–V_D curves at $V_{GS} = -0.6$ V.

First, the effect of the strain on the electrical characteristics of fresh devices (squares in Fig. 2) is compared. A clear increase of the drain current, I_D, is observed in strained transistors, which is attributed to an increment of the carrier mobility due to the channel strain.[2] This increase of μ is confirmed in Figs. 2(c), 2(f), and 2(i), which shows the transconductance (g_m) as a function of V_G for the different channel length MOSFETs. A larger g_m is observed in strained (solid) transistors, which indicates a higher mobility in these devices for all lengths. However, when comparing short and long channel devices, the I_D increase is much larger in short channel devices (see Table I, which shows the percentage increment of I_D, at $V_D = -0.6$ V, in strained MOSFETs compared to nonstrained devices for different lengths, called from now on α_D). This effect could be related to the fact that the induced strain is not uniformly distributed. Near source and drain regions, the induced strain is larger and decreases as we move to the center of the channel. As a consequence, the total strain in the channel depends on the channel length. For shorter devices, the source and drain regions are closer, and, therefore, the strained gate region (compared to the total gate area) is larger, leading to an enlargement of the average mobility and, thus, a higher I_D.[16]

The impact of a CHC stress on both kinds of MOSFETs (strained and nonstrained) was also studied. Note that, after the stress (Fig. 2, circles), I_D is reduced in both, strained (solid symbols) and nonstrained devices (open symbols). Table II shows the I_D reduction ($I_{D,red}$) at $V_D = -0.6$ V, in percentage, for the different MOSFETs. Note that the reduction depends on L and on the strain in the channel. In particular, $I_{D,red}$ is larger in strained devices (for a given L),[7] demonstrating that strained MOSFETs are more sensitive to a CHC electrical stress. When different lengths are compared, we can observe that the stress impact in short channel devices is larger, as expected, since higher electrical fields were applied along the channel. To eliminate the effect of the different stress conditions so that the strain effect is only considered, Table I shows, for a given L (and, therefore, for the same stress conditions), how large is the I_D reduction in

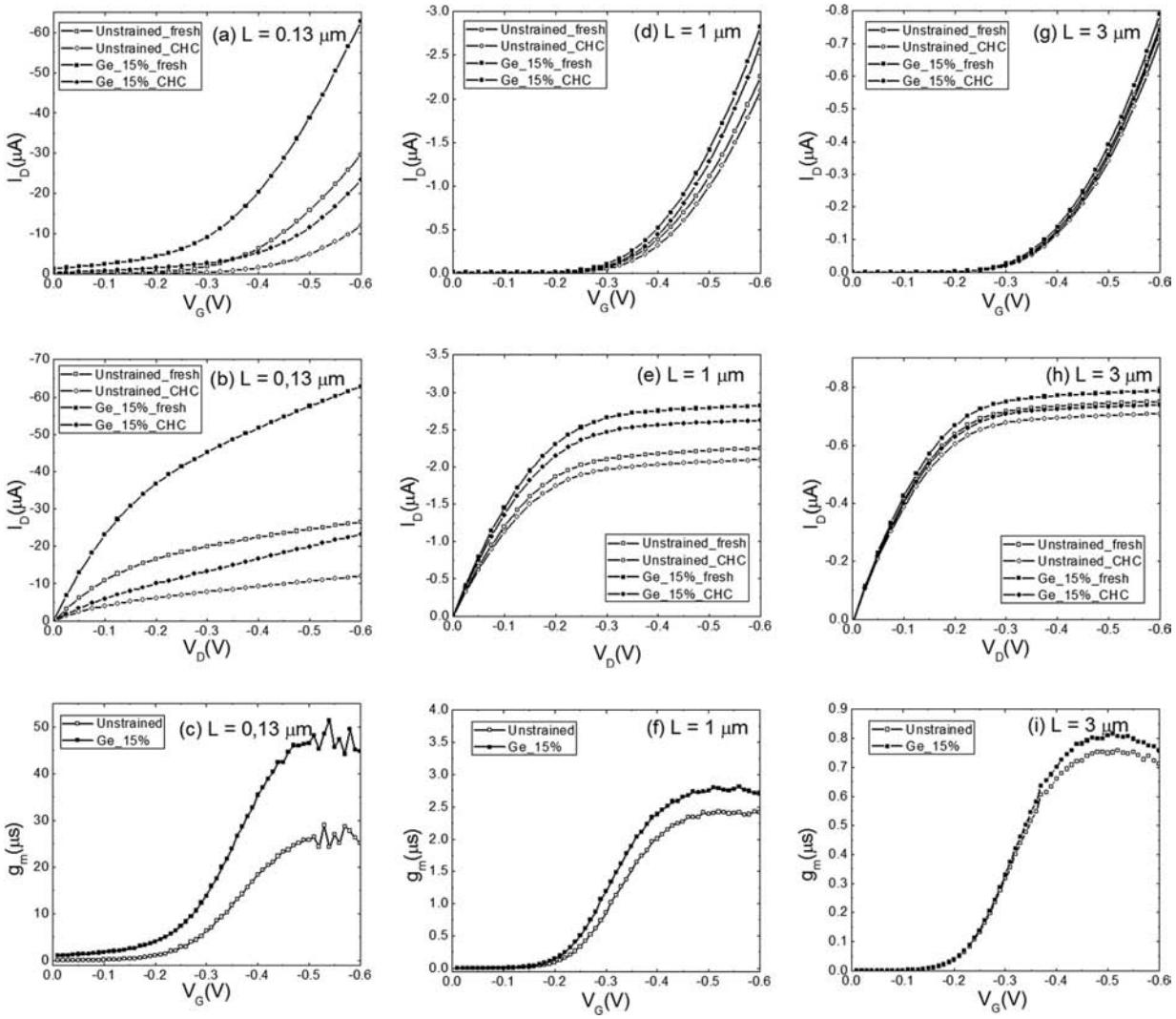

FIG. 2. I_D–V_G [(a), (d), and (g)], I_D–V_D [(b), (e), and (h)], and g_m–V_G [(c), (f), and (i)] curves of fresh (squares) and CHC (circles) stressed MOSFETs with strained (solid symbols) and unstrained (open symbols) channels. Channel length is 0.13 μm [(a)–(c)], 1 μm [(d)–(f)], and 3 μm [(g)–(i)].

strained MOSFETs compared to nonstrained devices (in percentage, β_D), defined as

$$\beta_D = (I_{D,red,\,strain} - I_{D,red,\,non\text{-}strain}) / I_{D,red,\,non\text{-}strain} \times 100. \quad (1)$$

Note that in short channel devices, β_D is larger, indicating that, for the same electric field, strained MOSFETs with short channel lengths are more sensitive to a CHC stress than those with large L. This can be explained again by considering that strain affects a larger portion of the global gate area of the device. So, from this analysis, we can conclude that the drain current (I_D) measured in strained devices, although larger, is more susceptible to be affected by CHC stress: a larger decrease than in nonstrained MOSFETs is observed, especially in short channel transistors.

TABLE I. α_D is the percentage increment of I_D in strained MOSFETs compared to nonstrained devices for different L. β_D indicates how large is the I_D reduction (and, therefore, the stress effect) in strained MOSFETs compared to nonstrained devices (in percentage) for a given L.

	L = 0.13 μm (%)	L = 1 μm (%)	L = 3 μm (%)
α_D	111.57	25.42	4.94
β_D	18.59	11.74	8.89

IV. NANOSCALE MEASUREMENT

In this section, a nanoscale analysis of the gate oxide properties of strained and unstrained MOSFETs (with different lengths) has been performed with CAFM. The gate current (I_G) has been measured with the CAFM tip on fresh and

TABLE II. I_D reduction after stress, $I_{D,red}$, in percentage, in CHC stressed MOSFETs compared to fresh devices for different lengths and substrates.

	Unstrained devices			Strained devices		
L (channel length)	0.13 μm	1 μm	3 μm	0.13 μm	1 μm	3 μm
$I_{D,red}$	55.37%	6.82%	6.05%	68.02%	7.73%	6.64%

stressed transistors and it has been considered as an indicative magnitude of the degradation induced by the stress.[14] Figures 3(a) and 3(b) show typical current images obtained at $V_G = -4$ V on the gate area of a fresh unstrained (a) and strained (b) MOSFET (with $L = 3\ \mu$m in this case). Note that before the stress [Figs. 3(a) and 3(b)] no currents are detected in the image. In both maps, only the instrumental noise from the CAFM preamplifier can be observed. Figure 3 also shows the current maps of the gate area measured at −4 V on nonstrained [(c) and (e)] and strained [(d) and (f)] MOSFETs after a CHC stress, with $L = 3\ \mu$m [(c) and (d)], and $L = 0.13\ \mu$m [(e) and (f)]. Note that, after the stress, brighter areas, which correspond to regions with a higher conductivity and were not present in fresh devices at the same voltage, are measured. This is indicative of the induced degradation by the stress in the device.

In the 0.13 μm channel length MOSFET, the measured currents reach the maximum measurable value, indicating that breakdown (BD) could have been triggered during the CAFM scan probably due to the large degradation induced by the CHC stress. Although breakdown was not triggered during the device level measurements (see Fig. 2), the stress could have damaged the gate oxide in such a way that when voltage was applied to the tip, breakdown could have been triggered. Even in the case that BD was not induced by the CAFM scan, currents are very large, which are indicative of a larger degradation. However, since I_G reaches the maximum allowed current by the setup, no quantitative analysis is possible in these short channel devices.

Contrarily, in the 3 μm channel length MOSFET [Figs. 3(c) and 3(d)], the leaky sites show lower currents, clearly indicating that BD was not induced in this case. The same kind of behavior is observed in devices with $L = 1\ \mu$m channel length (not shown). The leaky sites can be related to trap assisted tunneling through the defects generated during the stress. Therefore, these sites can be used to analyze the impact of the CHC degradation on the electrical properties of the gate oxide area. Note that the number of leaky sites in strained samples is considerably larger than in unstrained transistors, which indicates a larger CHC damage in strained devices. These results are consistent with the device level measurements. Moreover, thanks to the possibility of this technique to analyze very small areas along the channel, the CAFM images, also give us the possibility to study the impact of the stress in different regions of the channel. A quantitative analysis of the current images obtained in different MOSFETs ($L = 1\ \mu$m) is summarized in Table III. This table shows the average gate current $\langle I_G \rangle$ measured on six devices ($L = 1\ \mu$m) in a 0.25 μm^2 region close to the S, D and in the center of the channel (C), obtained from current images as those shown in Fig. 3. Note that, in both kind of transistors (unstrained and strained), regions close to S and D show larger currents, demonstrating the nonuniform degradation of CHC stress, as previously observed in Ref. 14 (Table III). To quantitatively compare the impact of the CHC stress in different regions of the channel between strained and nonstrained devices, the β_G parameter was calculated (Table III)

$$\beta_G = (I_{G,\text{increase, strain}} - I_{G,\text{increase, nonstrain}}) / I_{G,\text{increase, nonstrain}} \times 100, \quad (2)$$

which corresponds to the increment of the gate current in strained devices compared to nonstrained ones. Note that β_G, which is indicative of the impact of the stress, is larger close to S and D. Therefore, these results demonstrate that, besides the nonuniformity of the CHC stress itself, in strained devices, source and drain are more sensitive to the stress than nonstrained MOSFETs. Because of this higher susceptibility, the generation of defects in these areas is favored (compared to unstrained devices) and is detected by measuring a larger number of leaky sites and higher currents with the tip of the CAFM.

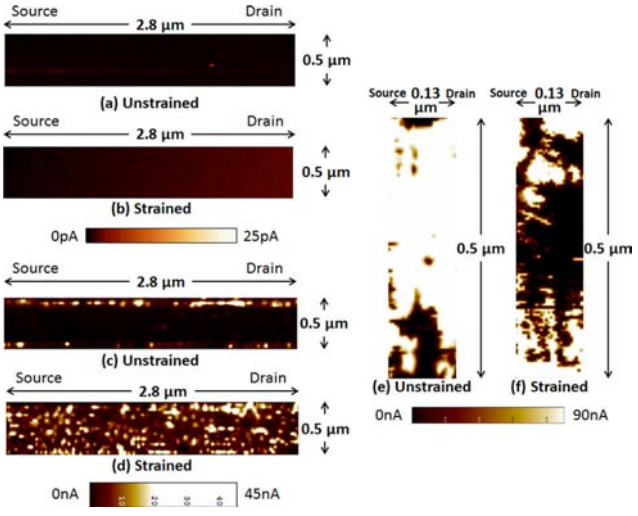

FIG. 3. (Color online) Current images obtained at a gate voltage of −4 V in fresh [(a) and (b)] and CHC stressed [(c)–(f)] MOSFETs with channel length 3 μm [(a)–(d)] and 0.13 μm [(e) and (f)]. Note that (a), (c), and (e) corresponds to unstrained devices and (b), (d), and (f) corresponds to strained devices.

V. CONCLUSIONS

In this work, the impact of a CHC stress on strained MOSFETs has been investigated and compared to unstrained devices by combining device level and nanometer scale characterization techniques. The nanoscale resolution of the CAFM has allowed investigating the spatial distribution of the damage after the stress. The results show that, with the introduction of strain, the channel mobility increases in both

TABLE III. Average I_G and β_G values obtained with CAFM close to S/D and in the center of the channel (C) for 1 μm strained and unstrained devices.

	$\langle I_G$ (nA)$\rangle$		
	Unstrained	Strained	β_G (%)
Source	2.67	10.54	294
Channel	1.43	4.92	244
Drain	2.01	9.51	373

long and short channel devices, being the increment larger in short devices. However, the transistors subjected to local strain are more sensitive to CHC degradation, leading to a higher reduction of I_D after the stress. This reduction could be related to a higher defect generation in strained devices, especially at the channel regions close to source and drain, since a larger increase of the gate current was detected with CAFM in these regions compared to nonstrained devices.

ACKNOWLEDGMENTS

This work has been partially supported by the Spanish MINECO and ERDF (TEC2013-45638-C3-1-R) and the Generalitat de Catalunya (2014 SGR-384). Qian Wu is financially supported by China Scholarship Council (CSC) with No. 201408390030.

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Evaluation of ultra-thin structures composed of graphene and high-k dielectrics for resistive switching memory applications

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Abstract: In this work, metal-insulator-semiconductor (MIS) structures with graphene as interfacial layer between the HfO_2 dielectric and the top electrode are evaluated as resistive random access memory (RRAM) devices. The graphene acts as a barrier between the metal electrode and the HfO_2 layer, hindering the diffusion of O atoms and protecting the structure from a destructive microstructural damage. The results show that when graphene is present, resistive switching (RS) can be measured probably owing to the controlled diffusion of the metal atoms from the electrode. We show also that the quality of graphene layer plays an important role on the behaviour of the described structures.

Keywords: resistive random access memory; RRAM; grapheme; resistive switching; high-k dielectrics.

Reference to this paper should be made as follows: Wu, Q., Claramunt, S., Porti, M., Nafría, M. and Aymerich, X. (2016) 'Evaluation of ultra-thin structures composed of graphene and high-k dielectrics for resistive switching memory applications', *Int. J. Nanotechnol.*, Vol. 13, Nos. 8/9, pp.634–641.

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This paper is a revised and expanded version of a paper entitled ‘Evaluation of ultra-thin structures composed of graphene and high-k dielectrics for resistive switching memory applications’ presented at *Trends in Nanotechnology*, Toulouse, France, 07–11 September, 2015.

1 Introduction

Nowadays the electronics industry is reaching a point that, in order to keep up with the Moore’s law, the introduction of novel materials and thinking about new kinds of architectures are necessary. This is especially important in memory applications, as the present non-volatile memory technology soon will have to be replaced by an alternative owing to physical constraints. So, new device concepts based in different physical principles from those of conventional floating gate based memories [1,2] have to be elucidated. Recently, a very attractive type of memory has been proposed, the resistive random access memory (RRAM) [3]. This type of memory, based on the resistive switching (RS) phenomenon, has emerged owing to its scalability, non-volatility and high performance. In this technology, a two terminal device is fabricated, usually formed by a metal-insulator-metal (MIM) or metal-insulator-semiconductor (MIS) device. By applying the correct voltage to the structure, it is possible to switch between two different conductivity states, named low resistance state (LRS) and high resistance state (HRS). Usually, this change in conduction is due to the formation and destruction of conductive

filaments (CF) [4–9]. These CF can be due to oxygen vacancies or to the diffusion of metallic atoms from the electrode material.

Although some prototypes of memory cells based in the RRAMs have been presented [10], some issues have to be resolved. For example, the physical phenomenon of formation of CF is still needed to be clarified, as also its dependency on the electrode material [11]. Because of that, the RRAM devices still suffer from severe variability between devices and between cycles [12], hindering their use in commercial applications. To solve this problem some authors have proposed the use of novel materials like graphene for improving the RRAM device. Graphene was first isolated by Novoselov et al. [13] and thanks to its incredible physical properties has been studied as a component in multiple applications, from field effect transistors [14] to micro-nano electromechanical systems [15]. In the case of the RRAMs, some authors have proposed the intercalation of a graphene monolayer between the top electrode and the insulator of a MIM or MIS structure. In Misra et al. [16], it is demonstrated that graphene can avoid interfacial interactions and diffusion of the metal gate into the underlying dielectric, avoiding its contamination and the fast degradation of the device reliability. In the case of RRAM devices based on HfO_x [17], the interfacial graphene layer acts as an oxygen barrier preventing oxygen ions from further migrating deep into the metal electrode. Independently of the case, the intercalation of the graphene layer helps to control the formation of CF.

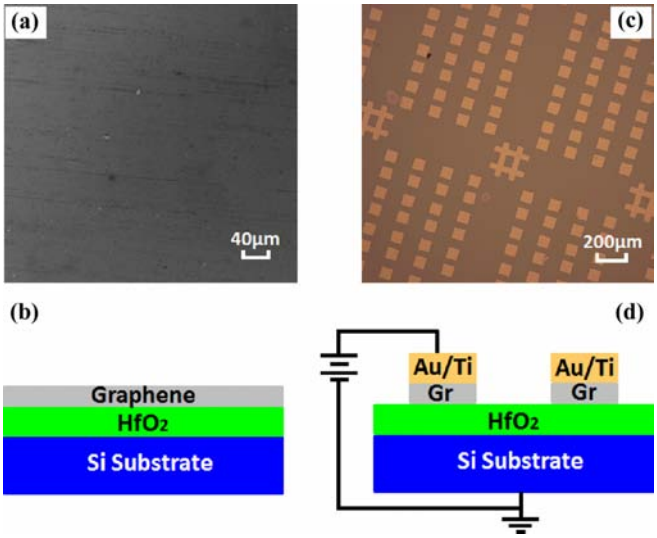
In this work, we evaluate ultra-thin RRAM structures composed of a MIS type structure (Au + Ti/HfO_2/Si) or MGIS (Au + Ti/G/HfO_2/Si), being the insulator layer as thin as 6 nm. We observe that the MIS structures always suffer an irreversible breakdown so that it is impossible to reset the device owing to the damage induced in the dielectric. On the other hand, some of the MGIS structures show RS behaviour. We propose that the graphene layer inhibits the oxygen diffusion that happens due the interaction of the electrode and the HfO_2 and favours the formation of CF owing to the diffusion of metal atoms through the grain boundaries of the graphene layer and later through the insulator layer.

2 Experimental

Ultra-thin HfO_2 based MIS structures with intercalated graphene between the high-k dielectric and the top electrode (from now on MGIS structures) were fabricated. First, a HfO_2 layer with a thickness of 6 nm was deposited by atomic layer deposition (ALD) on a p-Si substrate. The CVD single-layer graphene grown over a Cu foil was obtained from Graphenea, and then transferred onto the HfO_2/Si substrates [18] (Figure 1(a) and (b)). As we can see in Figure 1(a), the transferred graphene layer is continuous, with no observable defects. Then, 80×80 μm^2 Au/Ti electrodes were evaporated over the substrates to generate the electrical contacts. Finally, the samples were etched by O_2 plasma using a reactive ion etcher (RIE) 2000 CE from South Bay Technology inc. to eliminate the graphene material that is not underneath the metal electrodes. Figure 1(c) and (d) show the optical image of the final configuration of the electrodes and the schematic of the final MGIS structures, respectively. Samples without intercalated graphene (from now on MIS devices) were also prepared as references. The resulting structures were electrically measured with a Keithley 4200 Semiconductor Parameter Analyser. Some devices were stressed using a ramped voltage stress (RVS) until

irreversible breakdown (with a CL of 0.1 A), while in others, RVS with a CL of 0.1 mA were applied to observe the resistive switching (RS) phenomenon. In both cases, the role of the graphene interfacial layer was investigated. All the measurements were performed at room temperature.

Figure 1 (a) Representative field effect scanning electron microscopy (FESEM) image of a transferred graphene layer. (b) Schematic illustration of the Gr/HfO_2Si stack. (c) Optical image of the final configuration of the electrodes. (d) Schematic illustration of the final devices (see online version for colours)

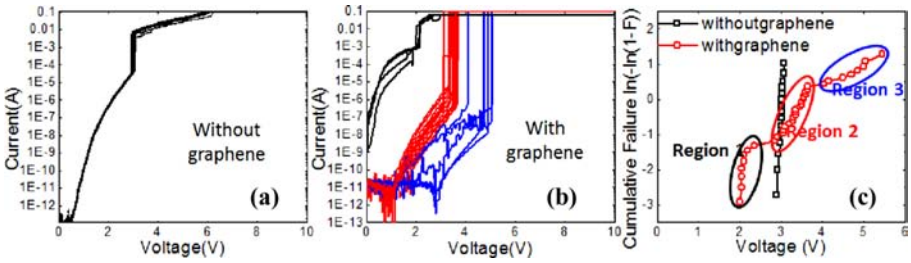


3 Results and discussion

First of all, the impact of the graphene layer on the voltage needed to trigger irreversible dielectric breakdown (V_{BD}, by applying RVS with a high CL of 0.1 A) was investigated. Figure 2 shows several I–V curves measured on MIS (a) and MGIS (b) devices. Figure 2(c) corresponds to the Weibull plot of V_{BD} obtained on samples with (squares) and without (circles) graphene. Note that V_{BD} of MIS devices is around 3 V. Moreover, very little variability is observed between devices neither on V_{BD} (Figure 2(c)) nor in the pre-breakdown conductivity (Figure 2(a)), which means that the HfO_2 layer is very homogeneous. However, in the case of the samples with graphene, large variability in V_{BD} (Figure 2(c)) and the pre-BD conductivity (Figure 2(b)) is measured. Although the V_{BD} varies ranging from 2 V to 5.5 V, the Weibull distribution of the MGIS devices can be divided into three differentiated regions (Figure 2(b) and (c)). In Region 1 (black in Figure 2(b) and (c)) the I–V curves have similar shape to those of the MIS structures, but with higher currents and smaller V_{BD}. In this case the graphene layer underneath the metal electrode could have been somehow damaged and/or broken during the transfer process or the metal deposit, allowing the direct contact between the metal electrode and the HfO_2, thus leading to a similar behaviour of the MIS structures. The Region 2 (red in Figure 2(b) and (c)) concentrates the higher number of devices. In this region,

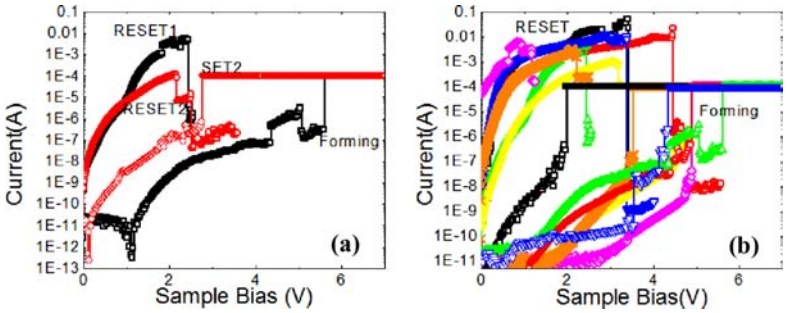
the I–V curves show a lower conductivity and higher V_{BD}, although a larger variability compared to MIS structures is measured, indicating a different forming phenomenon. In this case, the graphene layer is probably in good conditions and separate successfully the electrode from the oxide. Finally, in the Region 3 (blue lines in Figure 2(a) and (c)), a higher voltage is needed for the breakdown and the device-to-device variability increases. These results could be owing to other kind of defects of the graphene layer such as undesired layers, wrinkles or remaining polymer residues from the transfer process. Such defects changes the electrical properties of the graphene layer hindering the vertical current flow.

Figure 2 Typical I–V curves measured on samples without (a) and with (b) graphene. The I–V curves measured on MGIS devices can be divided into three regions (region 1, black, region 2 red and region 3 blue). Cumulative distribution of the V_{BD} of both samples, where the three regions can be observed again in MGIS devices (see online version for colours)



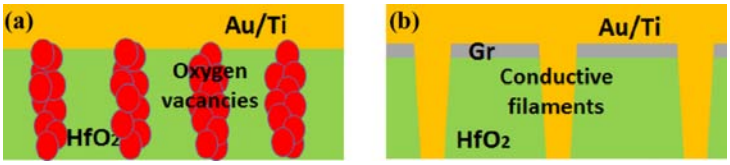
The electrical properties of MIS and MGIS devices when RVS with a current limit of 0.1 mA is applied were also been investigated. In MIS devices, no reset phenomenon was detected, meaning that this 'forming' process is in reality an irreversible breakdown and that RS cannot be observed in these structures. Regarding the devices with graphene, it is possible to reset the structure from the LRS to the HRS, being the observed RS unipolar. Figure 3(a) shows an example of two cycles of resistive-switching curves obtained on the same MGIS device. I–V curves of forming processes and their corresponding RESET obtained on different MGIS devices are also shown in Figure 3(b). Note that the variation of V_{Forming} and V_{RESET} among different devices is quiet large, which could be related again to the natural defects of the CVD graphene layer.

Figure 3 (a) Two I–V cycles of RS measured on MGIS devices. (b) Forming processes and corresponding reset voltages obtained on several MGIS devices (see online version for colours)



Regarding the process of formation of conductive paths we identify two different phenomena. In the MIS structures, the Ti metal electrode favours the diffusion of oxygen atoms owing to ease of Ti to react with oxygen [19] (Figure 4(a)). Because the size (very large) of the electrode and the small thickness of the oxide, this process becomes irreversible (breakdown). With the intercalation of a graphene layer (MGIS structure) the contact between the Ti and the HfO_2 is avoided, thus preventing the generation of oxygen vacancies. Moreover, the relatively high forming voltages and the non-polar phenomenology indicate that the conduction paths may occur owing to diffusion of Ti atoms (Figure 4(b)), that could diffuse through structural defects of the CVD graphene layer, for example grain boundaries. Therefore, intercalating a graphene layer avoids the irreversible BD that occurs in the MIS structures. In spite of that, topographic defects on the graphene layer can degrade its electronic properties, increasing the variability between devices. Probably with an improvement of the transfer process this variability could be reduced.

Figure 4 (a) Schematic illustration of the formation of conductive filament based on oxygen vacancies on samples without graphene. (b) Schematic illustration of the formation of conductive filaments based on diffusion of Ti atoms in samples with graphene (see online version for colours)



4 Conclusions

In summary, MIS structures composed of ultra-thin HfO_2 and graphene as interfacial layer between the top electrode and the dielectric were evaluated for their use in RS-based memory applications. The devices without graphene show irreversible breakdown, not allowing the measurement of RS. However, the intercalation of graphene prevents the irreversible breakdown and favours the diffusion of Ti atoms as a CF formation process, resulting in non-polar resistive switching. Owing to the quality of graphene layer, the variability of graphene devices is still far from that of the well-known MIS structures. In spite of that, we have demonstrated that the use of intercalated graphene opens the door to the fabrication of ultra-thin resistive memories. Further work should be performed both on the improvement of the quality of graphene layer and deeper study of the RS phenomenon.

Acknowledgements

This work has been partially supported by Spanish MINECO and ERDF (TEC2013-45638-C3-1-R), the Generalitat de Catalunya (2014SGR-384). Qian Wu acknowledges support from the Chinese Scholarship Council (No. 201408390030).

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ANNEX

Microelectronic Engineering 147 (2015) 335–338

Contents lists available at ScienceDirect

Microelectronic Engineering

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Non-homogeneous conduction of conductive filaments in Ni/HfO_2/Si resistive switching structures observed with CAFM

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ARTICLE INFO

Article history:
Received 23 February 2015
Received in revised form 7 April 2015
Accepted 10 April 2015
Available online 28 April 2015

Keywords:
Resistive switching
CAFM
Metal–insulator–semiconductor (MIS)

ABSTRACT

Conductive filaments (CFs) in Ni/HfO_2/Si resistive switching structures are analysed at the nanoscale by means of Conductive Atomic Force Microscopy (CAFM). Differences in the CF conductivity are measured depending on the resistive state of the device. Moreover, for both resistance states, non-homogeneous conduction across the CF area is observed, in agreement with a tree-shaped CF.

1. Introduction

Resistive random access memories (RRAM) based on metal–insulator–metal (MIM) or metal–insulator–semiconductor (MIS) structures have emerged as promising candidates for substituting the present non-volatile memory technology [1]. In these structures, it is possible to electrically form and partially break a conductive filament (CF) through the insulator material, so that the dielectric resistance is changed. Then ON or OFF states are achieved, depending on the dielectric conductivity. This phenomenon is known as Resistive switching (RS). Moreover, the MIM (or MIS) structure can be easily fabricated using standard microfabrication techniques [2,3], opening the door to fully operational RRAM devices based on these structures [4,5]. In spite of that, before their integration at commercial level, the complex RS mechanism must be well understood [6]. Its analysis is complicated since the CF has a localised nature so that high spatial resolution techniques are required to evaluate their properties. For example, by combining Focused Ion Beam (FIB) and Transmission Electron Microscopy (TEM) it has been possible to observe the formation and dissolution of a CF in real time [7]. Another alternative is the use of Conductive Atomic Force Microscopy (CAFM) to switch the resistance of the dielectric material by using the conductive tip as the top electrode of the stack structure [8,9]. With this technique, it is possible to create and analyse the CFs locally with a relatively simple setup. However, since the switching characteristics are strongly dependent on the electrode material [10], the properties of the CF formed using the CAFM tip as a top electrode could differ from the ones generated in conventional MIS or MIM structures. To overcome this limitation, in this work, a CF is formed in Ni/HfO_2/Si capacitors. Afterwards, the Ni electrode is removed and the CF properties analysed at the nanoscale with the CAFM tip. The objective is to give further insight into the RS mechanisms responsible for the formation and partial dissolution of CFs in these MIS structures.

2. Materials and methods

A schematic cross-section of the studied Ni/HfO_2/Si capacitors [11] is shown in Fig. 1(a). The area of the devices is $5 \times 5\ \mu m^2$. The structure and size was carefully chosen so that the whole active area of the device could be fully analysed by CAFM.

The methodology used consisted in first, creating the CF at device level with a HP-4155B semiconductor parameter analyser, using a current limit of 10^{-4} A. The voltage was applied to the Ni top electrode, while the Si substrate was grounded. To reach a stable state of the CF, five set and reset cycles were applied. Some samples were left at the high resistance state (HRS) while some others at the low resistance state (LRS). Fig. 2 shows the last *I–V* curves recorded after the set (left) and reset (right) processes in two different samples. In total, 10 samples were studied. After that, the Ni electrode of the MIS structures was etched off by means of (H_2O:HNO_3) (4:1) so as the HfO_2 surface was exposed and could be analysed with the tip of the CAFM (Fig 1b). A conductive Pt bulk tip

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http://dx.doi.org/10.1016/j.mee.2015.04.112
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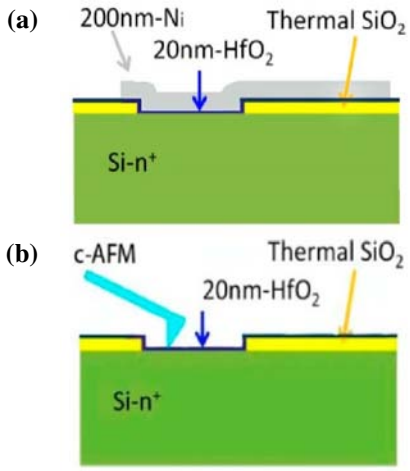

Fig. 1. (a) Schematic cross-section of the studied Ni/HfO_2/Si structures. (b) After Ni electrode removal, the whole active area of the device was scanned at constant voltage with the CAFM tip.

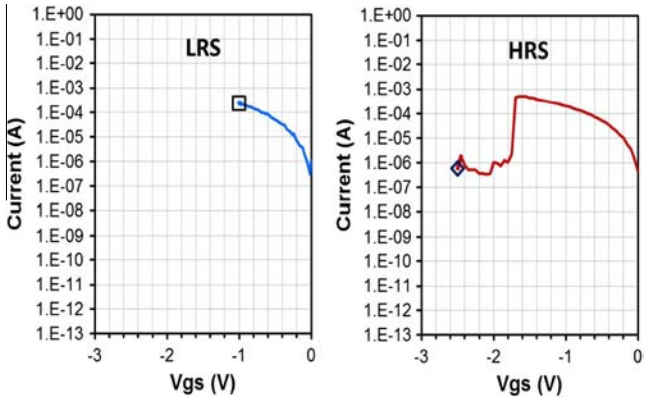

Fig. 2. Last *I–V* curves of two of the studied samples that were left at the LR (left) and HR (right) states. The measurements have been obtained at device level with the semiconductor parameter analyser.

with 20 nm nominal radius was used in order to study the device at the nanoscale. These tips are mechanically more stable than the metal-coated ones, permitting us to measure more maps without losing the topographical resolution and the conductivity during the experiments, a critical issue in measuring this type of systems. In any case, when small conductivity and/or resolution losses were observed, the tip was changed, so that the results are not affected by the tip properties. The whole active area was scanned at −4 V (injection from the substrate), so that the CF properties were not modified. For comparison, pristine samples and samples in which no current limit was established during electroforming have also been studied.

3. Results and discussion

First, CAFM analysis of pristine samples was performed in order to study any possible effects of the etching of the top electrode on the HfO_2 layer (Fig. 3(a)). We found the oxide layer surface to be very uniform and no current was detected, meaning that the etching process had a negligible effect on the HfO_2 layer properties. Next, samples that underwent hard breakdown (i.e. without current limit) were studied (Fig. 3(b)). In this case after Ni etching the topographical analysis showed an uncontrolled growth of a

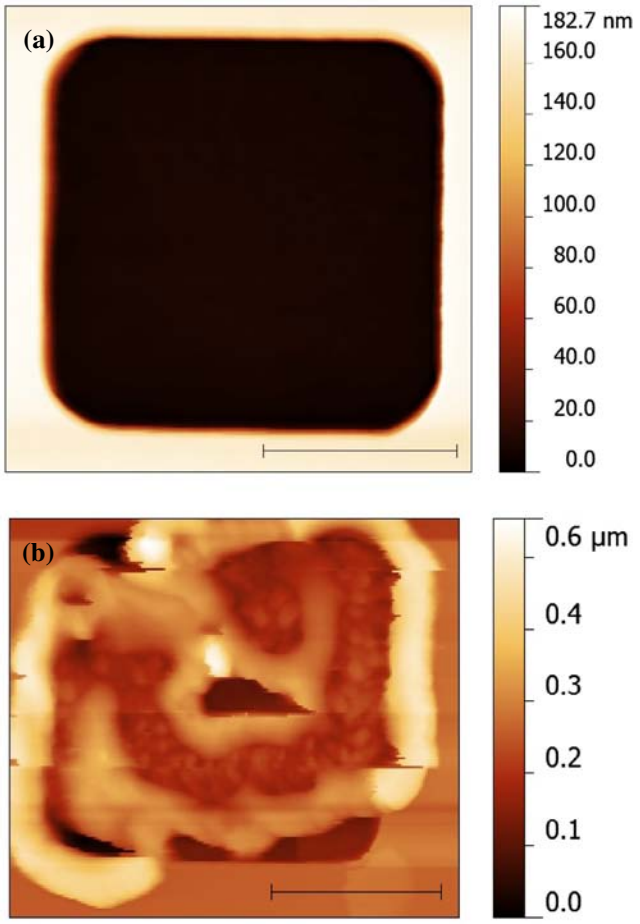

Fig. 3. (a) Topographical image of the pristine device after the etching of the Ni top electrode. A very flat surface is observed. (b) Topographical image of a device after electroforming without current limit. A large morphological modification is measured. In both images the horizontal scale bar is 3 µm.

large structure covering the entire device surface, a consequence of the large energy dissipation caused by the irreversible dielectric breakdown of the oxide layer.

The topography and current images measured on the rest of samples are significantly different. To show this point, Fig. 4(a) and (b) present typical 2D topographical and current images, respectively, of a device after the formation of the CF that was left at the HR state. Qualitatively similar results were obtained in the LRS samples. Interestingly, in the entire device surface only a hillock is detected, that corresponds to the sole conductive area found in the current image (Fig. 4(b) and (d)). As can be seen in Fig. 4(c), which corresponds to the 3D topographical image of the hillock observed in Fig. 4(a), the hillock has an irregular shape but presents well defined edges, demonstrating that the CF formation is local. In addition, the surface around the hillock is unaffected, and with the homogeneity of the pristine samples (see Fig. 3(a)). This indicates that in our experimental conditions, one or several CFs are concentrated in the spot revealed by CAFM. This hillock is probably the result of the electrochemical and thermochemical reactions responsible for the CF formation and dissolution processes [12]. However, further analysis, which is out of the scope of this work, is needed to elucidate the physical origin of these morphological modifications.

After the analysis of several devices we observed that the position of the CF is random. Measurements show that the CF characteristics are qualitatively similar between devices, independently of the device state (i.e. LRS or HRS). We found that the spot areas

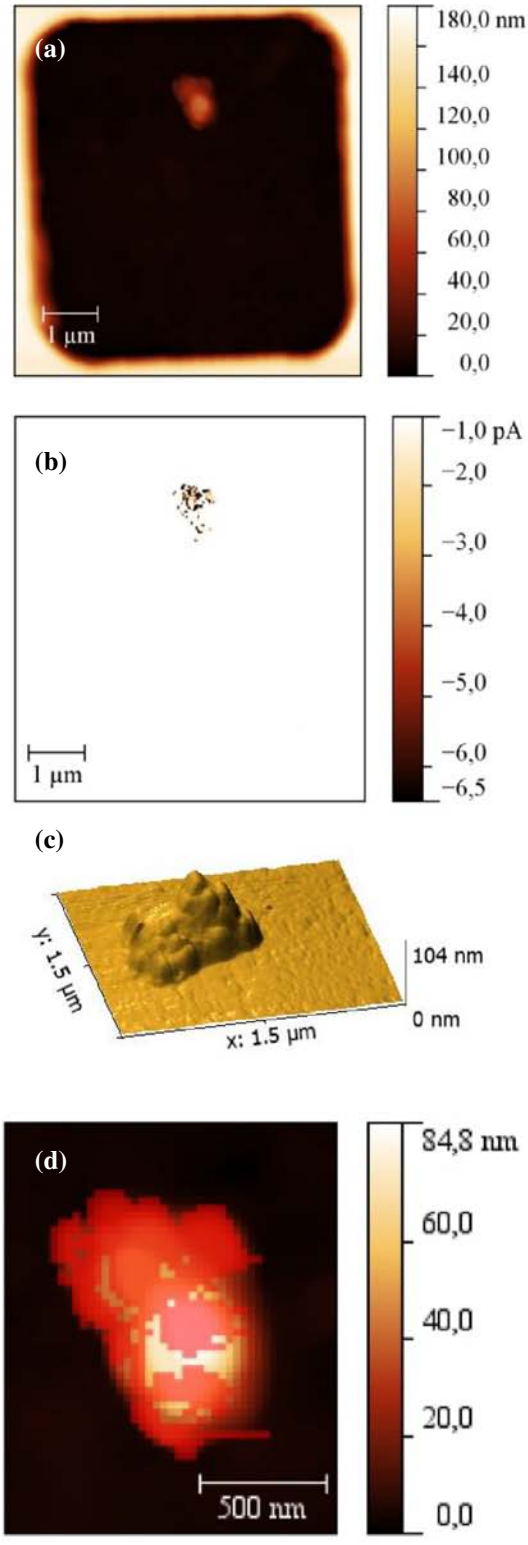

Fig. 4. (a) Topographical and (b) current images of a sample at the HRS state measured at −4 V. In both images, a unique spot is clearly visible in the device area. (c) Representation in 3D of the hillock. (d) Topographical image of the spot overlapping the current image (red colour), indicating that surface modifications and current increase are correlated. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

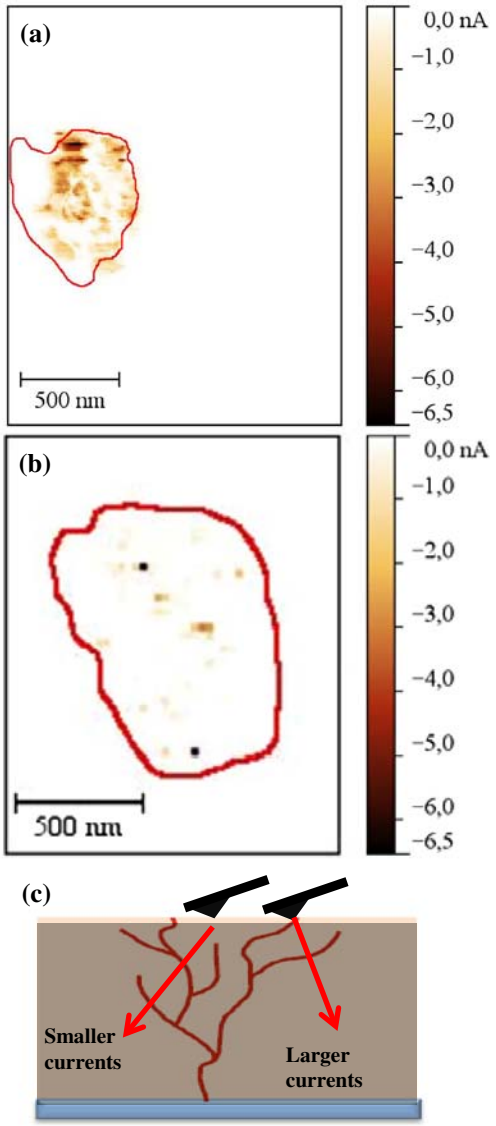

Fig. 5. Current images of representative spots corresponding to (a) LR and (b) HR states measured on different samples. The red line marks the edges of the regions where current is measured. (c) Schematic representation of the tree-shaped model of the CFs. The higher current measured with CAFM goes through the branches that end near the dielectric surface, whereas the others are responsible for the lower conductivity measured in the rest of the spot. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

are around 0.5 μm^2 with an estimated hillock height of around 100 nm. However, though a statistically representative analysis has not been carried out, the measurements seem to indicate that the LRS spots present smaller sizes (around 0.5×) than the HRS spots (Fig. 5).

Interestingly, as can be seen in Fig. 5, the local conductive measurements of spots corresponding to LRS (a) and HRS (b) show that the current through the CF is not spatially homogeneous. Although in most of the spot area currents of pA are detected, there are small regions with currents in the range of nA. Moreover, in the LRS spots, the portion of the CF area with higher currents is larger than in the HRS, which would explain the larger LRS conductivity observed at device level (Fig. 2). This inhomogeneous conduction is compatible with a tree-shaped CF [12]. As sketched in Fig. 5(c), some branches would span all along the dielectric thickness, connecting the two electrodes, whereas some others would end within the dielectric. Then, when scanning with the tip, larger currents would be measured in the first case (nA currents) whereas lower currents would be observed in the second case (pA currents). The

number of electrode-connecting branches would be larger for the LRS case, in accordance with the observed size of the high-current area of the CF.

4. Conclusions

The CAFM characterisation of CFs in Ni/HfO_2/Si RS structures is presented. We have shown that, independently of the device state (LRS or HRS) the CFs are formed in a unique spot that can be detected as a hillock in the topography image after the removal of the Ni electrode. Local electrical analysis of the HRS and LRS spots reveals a non-uniform conduction, with some regions in the spots with significantly higher conductivity. This behaviour is in agreement with the tree-shaped model of CF formation.

Acknowledgments

This work has been partially supported by the Spanish MINECO and ERDF (TEC2013-45638-C3-1-R and TEC2011-27292-C02-02) and the Generalitat de Catalunya (2014SGR-384). Qian Wu acknowledges support from the Chinese Scholarship Council (No. 201408390030).

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