Sigma-Delta Control of Charge Trapping in Heterogeneous Devices

Dissertation presented in partial fulfillment of the requirements for the degree of Doctor in Electronic Engineering

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Septiembre 2019

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Acknowledgments

I would like to express my sincere gratitude to everyone who has contributed to the realization of this thesis.

Firstly, I would like to thank my thesis director, Manuel Domínguez Pumar, for the continuous support and guidance, for his patience and knowledge. His door was always open for me and he has been there to help me throughout this journey of my PhD. I appreciate all his contributions to make my PhD experience productive and stimulating. I would also like to thank Joan Pons for his patience and consistent support in numerous ways over the years. My sincere thanks to Prof. Lluís Pradell and Prof. Luis Castañer for providing me the opportunity to work at UPC.

My profound gratitude to all my colleagues and friends who made my stay at UPC enriching, pleasant, and enjoyable. I am grateful to: Teresa Atienza for her help and support; Gema López for always helping me; Guillermo Gerling, Sergi Gorreta, Lukasz Kowalski for sharing good moments and interesting conversations; Guillermo Martínez, Bremnen for fabricating the devices for my work; Miguel García, Pablo Ortega for their help during the experiments; Santi Pérez and Manuel for nice conversations over coffee; Julio, Roselena, Zaira, Mohamed Saad, Chen Jin for spending good time together.

I am indebted to all my dear friends for always being helpful and spending their precious time with me. David and Dani: I am grateful to have you two as my friends. I truly appreciate your unconditional love, support, and care that you show towards me. Thanks for always having my back no matter what. Angie: Muchas gracias por su amable apoyo y esfuerzo para hacerme una mejor persona. Te estoy agradecido. Anand: Thanks for being a great friend, flatmate and for your support. Joan and Jose: Thanks for all the good times we spent together. A very special thanks to Sudheer, Mahesh, Sagar, Chenna Krishna, Shajahan, EC, Maneesh, Kartheek, Gopi, Devendar, Shravan, Shailesh, Prakash, Madhu, Subbu, Mohit, Sridhar for all the love and support.

Finally, I would like to say heartfelt thanks to my family: my sister and my parents for their love and support all my life.

Abstract

Dielectric charging represents a major reliability issue in a variety of semiconductor devices. The accumulation of charge in dielectric layers of a device often alters its performance, affecting its circuital features and even reducing its effective lifetime. Although several contributions have been made in order to mitigate the undesired effects of charge trapping on circuit performance, dielectric charge trapping still remains an open reliability issue in several applications.

The research work underlying this Thesis mainly focuses on the design, analysis and experimental validation of control strategies to compensate dielectric charging in heterogeneous devices. These control methods are based on the application of specifically designed voltage waveforms that produce complementary effects on the charge dynamics. Using sigma-delta loops, these controls allow to set and maintain, within some limits, the net trapped charge in the dielectric to desired levels that can be changed with time. This allows mitigating long-term reliability issues such as capacitance-voltage (C-V) shifts in MOS and MIM capacitors. Additionally, the bit streams generated by the control loops provide real-time information on the evolution of the trapped charge.

The proposed controls also allow compensating the effects of the charge trapping due to external disturbances such as radiation. This has been demonstrated experimentally with MOS capacitors subjected to various types of ionizing radiation (X-rays and gamma rays) while a charge control is being applied. This approach opens up the possibility of establishing techniques for active compensation of radiation-induced charge in MOS structures as well as a new strategy for radiation sensing.

A modeling strategy to characterize the dynamics of the dielectric charge in MOS capacitors is also presented. The diffusive nature of the charge trapping phenomena allows their behavioral characterization using Diffusive Representation tools. The experiments carried out demonstrate a very good matching between the predictions of the model and the experimental results obtained. The time variations in the charge dynamics due to changes in the voltages applied and/or due to external disturbances have been also investigated and modeled.

Moreover, the charge dynamics of MOS capacitors under sigma-delta control is analyzed using the tools of Sliding Mode Controllers for an infinite sampling frequency approximation. A phenomenological analytical model is obtained which allows to predict and analyze the sequence of control signals. This model has been successfully validated with experimental data.

Finally, the above control strategies are extended to other devices such as eMIM capacitors and

perovskite solar cells. Preliminary results including open loop and closed loop control experiments are presented. These results demonstrate that the application of the controls allows to set and stabilize both the C-V characteristic of an eMIM capacitor and the current-voltage characteristic (J-V) of a perovskite solar cell.

Resumen

La carga atrapada en dieléctricos suele implicar un problema importante de fiabilidad en muchos dispositivos semiconductores. La acumulación de dicha carga, normalmente provocada por las tensiones aplicadas durante el uso del dispositivo, suele alterar el rendimiento de éste con el tiempo, afectar sus prestaciones a nivel de circuital e, incluso, reducir su vida útil. Aunque durante años se han realizado muchos trabajos para mitigar sus efectos no deseados, sobre todo a nivel circuital, la carga atrapada en dieléctricos sigue siendo un problema abierto que frena la aplicabilidad práctica de algunos dispositivos.

El trabajo de investigación realizado en esta Tesis se centra principalmente en el diseño, análisis y validación experimental de estrategias de control para compensar la carga atrapada en dieléctricos de diversos tipos de dispositivos, incluyendo condensadores MOS, condensadores MIM fabricados con nanotecnología y dispositivos basados en perovskitas. Los controles propuestos se basan en utilizar formas de onda de tensión, específicamente diseñadas, que producen efectos complementarios en la dinámica de la carga. Mediante el uso de lazos sigma-delta, estos controles permiten establecer y mantener, dentro de unos límites, la carga neta atrapada en el dieléctrico a valores prefijados, que pueden cambiarse con el tiempo. Esto permite mitigar problemas de fiabilidad a largo plazo como por ejemplo las derivas de la curva capacidad-tensión (C-V) en condensadores MOS y MIM. Adicionalmente, las tramas de bits generadas por los lazos de control proporcionan información en tiempo real sobre la evolución de la carga.

Los controles propuestos permiten también compensar los efectos de la carga atrapada en dieléctricos debida a perturbaciones externas como la radiación. Esto se ha demostrado experimentalmente con condesadores MOS sometidos a diversos tipos de radiación ionizante (rayos X y gamma) mientras se les aplicaba un control de carga. Este resultado abre la posibilidad tanto de establecer técnicas de compensación activa de carga inducida por radiación en estructuras MOS, como una nueva estrategia de sensado de radiación.

Se presenta también una estrategia de modelado para caracterizar la dinámica de la carga dieléctrica en condensadores MOS. La naturaleza difusiva de los fenómenos de captura y eliminación de carga en dieléctricos permite caracterizar dichos fenómenos empleando herramientas de Representación Difusiva. Los experimentos realizados demuestran una muy buena correspondencia entre las predicciones del modelo y los resultados experimentales obtenidos. Se muestra también como las variaciones temporales de los modelos son debidas a cambios en las formas de onda de

actuación del dispositivo y/o a perturbaciones externas.

Además, la dinámica de carga en condensadores MOS bajo control sigma-delta se analiza utilizando herramientas de control en modo deslizante (SMC), considerando la aproximación de frecuencia de muestreo infinita. Con ello se obtiene un modelo analítico simplificado que permite predecir y analizar con éxito la secuencia de señales de control. Este modelo se ha validado satisfactoriamente con datos experimentales.

Finalmente, las estrategias de control anteriores se han extendido a otros dispositivos susceptibles de sufrir efectos de carga atrapada que pueden afectar su fiabilidad. Así, se han llevado a cabo experimentos preliminares cuyos resultados demuestran que la aplicación de controles de carga permite controlar y estabilizar la característica C-V de un condensador eMIM y la característica corriente-tensión (J-V) de una célula solar basada en perovskitas.

What can be asserted without evidence can
also be dismissed without evidence.

Christopher Hitchens

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Chapter 1

Introduction

1.1 Framework

The reliability of dielectric materials has always been one of the major concerns in the commercialization of microelectronic technologies [1, 2, 3]. A great deal of success in the evolution of modern microelectronics industry has been attributed to the excellent dielectric properties of silicon dioxide (SiO_2). Silicon dioxide can be formed by thermal oxidation, and has characteristics of good dielectric strength, low defect density, large band gap and provides a thermodynamically stable interface, making it the most commonly used insulator in IC technology. A lot of investigation and investments have been made over decades in research, development and manufacture of highly reliable oxides. This has been evident from its successful and diverse applications not only in the field of semiconductor devices but also in metallurgy [4], material science [5], and geology [6], to name a few. However, in most of the applications involving the gate and passivation oxide layers (MOS devices, for example), operating the devices under high stress conditions [7, 8, 9] or in radiation environment [10, 11] over a period of time could degrade the electrical properties of the oxide layer leading to critical device failures.

A thorough and detailed analysis of surface properties of the oxides has been carried out to gain the knowledge about such instabilities. Primarily, the origin of such instabilities corresponds to defects in the dielectric layer and at the interface between the dielectric and the electrode/semiconductor [12, 13, 14]. When a bias voltage is applied across the gate oxide, these defects act as traps for electrons and holes. This trapping of charge carriers in the dielectric and at the interface is an important issue that controls the performance of the devices. Gaining insight about the properties of these defects contributes to the development of models related to the long term reliability of MOS devices. Significant practical and theoretical knowledge concerning the reliability issues have been accumulated in the past decades to address the challenges and to meet lifetime specifications for commercial applications [15, 16, 17].

When the devices are under operating conditions, the dielectric films undergo electrical stress and charge carrier injection. With the applications of high fields, trapping of charge carriers takes

place at defects and affects device parameters such as operating voltage, gate leakage current, mobility etc. In general, the measurement of shift in threshold voltage, V_T, serves as an indirect estimation for the amount of charge trapped in the dielectric. It has been observed in most of the MOS devices that a negative gate bias stress would result in a negative shift of V_T due to an increase in the amount of positively-charged oxide traps. Similarly, applying a positive gate bias voltage would cause a V_T shift in positive direction possibly due to electron trapping in the oxide. Accumulation of large amounts of charge would cause a large V_T shift, resulting in potential device failure.

The mechanisms of electron and hole trapping in dielectrics are important for understanding and improving the performance of devices in applications such as photovoltaics, electronics. Especially, charge trapping phenomena in SiO_2 gate dielectrics has been studied extensively in the past [18, 19, 20]. However, aggressive scaling of device dimensions and need for high power electronics has raised concerns over the use of conventional SiO_2 in the device architecture. So, many studies investigated the effects of charge trapping in alternative (high-k) dielectric materials [21, 22] to improve the reliability of devices. It has been reported that employing high-k materials with a high injection barrier and low concentration of interface states may overcome the dielectric charging [23]. Most of the strategies to mitigate the instabilities in the operating characteristics of MOS devices related to charge trapping involves the reduction of defect denisities by improving the fabrication processing control and annealing procedures [24, 25, 26, 27].

On the other hand, electrostatic MEMS also suffer from the effects of dielectric charging. The net charge accumulated in dielectric layers has a significant impact on the behavior of such devices resulting in undesirable effects such as shifts of the capacitance-voltage (CV) characteristic and even permanent stiction of movable mechanical parts. Several techniques proposed for mitigating this undesirable phenomena focus on either improving the design of the device or implementing intelligent bipolar voltage waveforms for actuation in open loop. However, these strategies have not been able to completely solve the charge trapping issue in long term.

In order to reduce the effects of dielectric charge trapping, charge control strategies have been proposed and implemented in [28, 29]. Under predefined limits, these controls allow to set and maintain a previously given amount of net dielectric charge, thus mitigating long-term reliability issues such as CV shifts or V_T drifts. In these controls, the charge being continuously leaked out of the dielectric is compensated in average by applying an adequate sequence of bipolar voltages. The theoretical validation of these control methods has been carried out employing the numerical simulation and matching it with experimental results in case of MEMS [30].

Another challenging reliability issue for the microelectronic devices operating in aerospace systems is their exposure to various forms of radiation. The radiation effects include the buildup of oxide and interface trap charge, leading to the changes in threshold voltage. Following the exposure to ionizing radiation, MOS structures typically exhibit a negative shift in oxide-charge-induced threshold voltage component, V_{ot} that could potentially persist for hours to years. Figure 1.1 shows typical radiation-induced oxide charge buildup characteristics with respect to gate bias for an MOS capacitor [31]. This component is the predominant and most commonly observed form of radiation

damage in MOS devices. Hence in this work, effort towards compensating this oxide positive charge trapping has been made by implementing a charge compensation strategy.

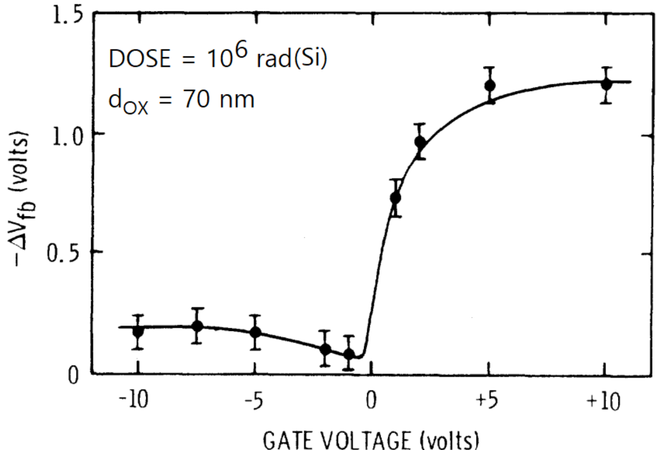

Figure 1.1: Radiation-induced flatband voltage shift of an MOS capacitor vs gate bias during irradiation [31].

The characterization of charge trapping mechanisms in the bulk oxide and at the oxide-semiconductor interface is of crucial importance in mitigating the effects of dielectric charging. Modeling the charge dynamics at different actuation voltages allows to describe the evolution of dielectric charge contributions. Thus, characterization of charge dynamics as a function of the voltages applied is of great relevance for the active operation of MOS based devices, especially while operating in environments affected by external factors such as ionizing radiation. The charging/discharging phenomena has been identified as a diffusion like process and has been widely studied and analyzed in case of MEMS [32, 33, 34, 35, 36].

The characterization of the charge trapping dynamics in MOS devices has been extensively studied in literature [37]. Trap distributions are obtained from impedance spectra for different voltages in [38, 39]. Other works analyze the charging dynamics as the result of the application of a voltage (or temperature) stress, while observing discharging currents or shifts in the threshold voltage. In these methods, the stress factor is instantaneously changed and changes in drain currents or threshold voltage shifts are monitored and fitted. Models with one or two time constants, as well as, more generally, stretched exponentials have been used to this purpose. In stretched exponentials the charge transient is characterized by the function $exp(-(t/\tau)^{\beta})$, with $\beta \in (0,1)$. This model has been linked to Gaussian distributions in the energy barriers found in charge trapping and detrapping [40]. However, in all these cases the analysis of the time evolution of systems under arbitrary excitation becomes difficult because it is necessary to take into account the distributed nature of the processes involved. In this Thesis, the dynamics of trapped charge in MOS capacitors is characterized by obtaining the state-space model using Diffusive Representation (DR) and the

behavior of the device under control has been predicted using a specific analytical model, derived from the Sliding Mode Control (SMC) theory.

DR is a mathematical tool that allows the description of any physical phenomena based on diffusion using state-space models of arbitrary order in the frequency domain. The key idea behind DR is to decompose long range time series on a continuous family of purely damped exponentials [41, 42]. Additionally, SMC is a non-linear control technique which employs a discontinuous feedback signal to drive the system state trajectory onto a predetermined sliding surface [43, 44] for all subsequent time. The theory of SMC has recently been applied for the prediction of the closed-loop dynamics of wind sensors [45, 46] that have been thermally characterized. In this Thesis, DR technique is employed to describe the charge dynamics of a system using an arbitrary order state-space model. The behavioural models obtained with DR are used in the analysis and prediction of the closed-loop control of charge trapping, using the tools of SMC.

Furthermore, in this Thesis, the charge trapping issue has been explored in other devices such as perovsite solar cells and electrosprayed nanoparticle MIM (eMIM) capacitors. Perovskite based devices are considered promising materials in photovoltaic technology due to their high efficiency, and low fabrication costs. However, the photovoltaic performance of organic-inorganic perovskites have been severely affected by the charge traps by deactivating the photoexcited species [47]. In [48, 49, 50], it has been established that charge traps have significant impact on the degradation of metal halide perovskites by monitoring trapped electronfree hole recombination kinetics. Many works in the literature suggests the possibility of improving the perovskite stability by encapsulation and varying the fabrication process or the chemical composition of the materials [51, 52, 53, 54]. However, currently the maximum stability is established in 6 months, far from the 25 years required to compete commercially against conventional Silicon based solar cells. The work carried in this Thesis intend to tackle the issue of charge trapping by means of an external control circuit.

In case of energy storage applications, it has been recently demonstrated that MIM capacitors with SiO_2 nanoparticles [55, 56] have been projected as future of high density energy storage elements. The recent advances in functional nanostructures along with their intrinsic advantage of large surface area to volume ratio has resulted in widespread use of supercapacitors as potential energy storage devices. Since the overall performance of the supercapacitor devices strongly depends on the properties and the structure of the component materials, characterization of different dielectric materials has become one of the most important aspects to be investigated to improve the energy storage performance. In this Thesis, the effects of bias voltage on charge distribution in eMIM dielectric layer has been investigated with an aim to improve the energy storage ability of the devices.

1.2 Objectives

With regard to the above discussion, the main objective of this Thesis is to contribute to the improvement of the reliability and/or operating lifetime of MOS capacitors by designing and analyzing effective strategies for dielectric charge control. This Thesis implements the closed loop

control techniques to control and maintain the net amount of charge in dielectric layer of these devices. Further a model is developed to analyze the dynamics of the oxide trapped charge with different actuation voltages and in also with external disturbances. The secondary objective is to extend the control strategies to other devices such as eMIM capacitors and perovskite devices.

The specific objectives for the research work are as following:

- *Dielectric charge control*: Implement the charge control method based on sigma-delta loop by continuous monitoring and keeping constant the net trapped charge in the dielectric. This has been achieved by periodically sampling the horizontal displacement of the capacitance-voltage (CV) characteristic curve of the device and applying the adequate voltage waveforms to maintain it at a desired position. In particular, the main focus has been on the analysis and compensation of dielectric charging in MOS capacitors.
- *Compensation of radiation-induced charge*: Compensating the ionizing radiation (X-ray and Gamma radiation) induced charge accumulation in the dielectric layer to improve the radiation response of MOS capacitors made of SiO_2 and Al_2O_3 dielectrics. In particular, since trapping of net positive charge dominates other effects such as electron trapping and interface trap buildup, our aim in this Thesis is to control the oxide trapped charge.
- *Characterization of trapped charge dynamics*: Characterization of the trapped charge dynamics in the dielectric of a MOS capacitor to obtain the dynamic model of the device using DR theory. Validation of the model predictions using the experiments under arbitrary voltage excitations.

  The main objective is to derive behavioral models, considering MOS capacitor as a 'black box', thus capturing the dynamical behavior of the device without interpreting the results in terms of physical phenomena.
- *Sliding mode analysis of the charge dynamics*: Analyze and predict the closed loop charge dynamics, operating under sigma-delta control, using the tools of SMC for an infinite sampling frequency approximation.
- *Charge control applied to other semiconductor devices*: Employ the proposed closed loop control strategies to investigate the charge control capability in eMIM capacitors and perovskite solar cells.

1.3 Document Organization

The rest of this document is organized as follows:

- Chapter 2 describes the background of this Thesis. In this chapter, the contributions regarding the issues in literature related to charge trapping in heterogeneous semiconductor devices have been discussed. The significance of mathematical tools which are used to analyze and model the charge dynamics is also discussed.

- Chapter 3 introduces and demonstrates the effectiveness of closed loop control technique based on sigma-delta modulation in controlling the dielectric charge in a MOS capacitor. An analytical model is developed to characterize and predict the effects of oxide trapped charge on device capacitance. A second order sigma-delta control strategy is also presented and the advantages over the first order control are discussed.
- Chapter 4 discusses the radiation-induced effects of ionizing radiation on the operation of MOS capacitors. It demonstrates the effectiveness of the proposed control method in improving the radiation response of the device. This provides a potential control technique to improve the reliability of MOS-related devices working in hardness environments.
- Chapter 5 presents a modeling strategy, based on DR to characterize the dynamics of the charge trapped in the dielectric of MOS capacitors. It also introduces the SMC technique to analyze the charge dynamics when the device is being controlled by a sigma-delta control. The predictions made using these models are validated with the experimental measurements.
- Chapter 6 demonstrates the effectiveness of the control schemes in avoiding the drifts in the device characteristics. This chapter also discusses the experiments comprising open loop stress and closed loop control to study and understand the charge dynamics in case of eMIM capacitors and perovskite devices.
- Chapter 7 draws the main conclusions derived from the results of the Thesis work. It also includes a future work section, which highlights potential research lines outlined from this work.

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Chapter 2

Thesis Background

This chapter provides the background details of the research work carried out in this thesis. It focuses on elucidating the idea of the research topic undertaken and the methodologies employed along the main topics related to the research work. Accordingly, Section 2.1 reviews the main issues related to dielectric charge trapping in heterogeneous devices such as MOS devices, organic field effect transistors (organic FETs or OFETs), MEMS, and perovskite devices. Section 2.1.3 discusses about the effects of ionizing radiation and the radiation response of MOS systems. Finally, Section 2.2 reviews the significance of mathematical tools such as Diffusive Representation and Sliding Mode Control in the modeling and analysis of charge trapping dynamics in MOS capacitor devices.

2.1 Dielectric Charging

2.1.1 Dielectric Charging in Semiconductor Devices

Traps, in general, refer to anomalous defects in a crystal lattice, which create energy levels into the bandgap of the structure where the charge carriers can be trapped, either temporarily or permanently. Charge trapping in a dielectric occurs when the charge carriers tunnel into the dielectric layer (from an adjacent metal or semiconductor layer) under voltage stress and get trapped, thereby screening the applied voltage [1]. Depending on the positions of these energy levels, these traps or defect states can be categorized as shallow levels and deep levels. Shallow traps correspond to defects with energy levels close to band edges (either conduction band or valence band) and are thermally ionized at room temperature. On the other hand, deep-level traps are the ones whose energy levels lie near the middle of the bandgap and, therefore, the energy required to remove the charge carrier from the trap to the valence or conduction band is larger than the characteristic thermal energy, given by kT, where k is the Boltzmann constant and T is temperature. Under the influence of an electric field, these charge carriers begin to migrate through the oxide where some of them get trapped in shallow traps and deep traps. These give rise to undesirable effects such as:

- a shift in the threshold (or operating) voltage of the device.
- a reduction in the carrier mobility by scattering the carriers.
- instability of operating characteristics leading to eventual device failure.

A large number of semiconductor devices such as MOS capacitors, MOSFETs, OFETs, thin film transistors, MEMS etc. suffer from reliability issues, where trapping and detrapping of charge carriers in their dielectric layers generate typically stress-induced leakage currents and bias-induced threshold voltage shifts. Instabilities in the characteristics of MOS transistors have been extensively investigated [2, 3, 4]. In MOSFETs, oxide defects have been responsible for random telegraph and $1/f$ noise [5] due to their random exchange of charge with the substrate. Also, bias temperature instability (BTI) degradation has been a critical reliability concern for CMOS circuits and devcies [6, 7]. The impact of time-dependent degradation of device electrical properties due to BTIs have been studied [8, 9] at circuit level. The earlier investigations [10] show that MOSFETs are most severely affected due to negative BTI (NBTI) compared to positive BTI (PBTI), see Figure 2.1. However, in modern nanometer technologies, PBTI poses a serious degradation problem in pMOS transistors [11, 12]. In addition, process variations in fabrication of these devices lead to threshold voltage variability.The combined effects of threhold voltage variability and device degradation leads to time-dependent variations in the transistor characteristics at device and circuit levels [13, 14].

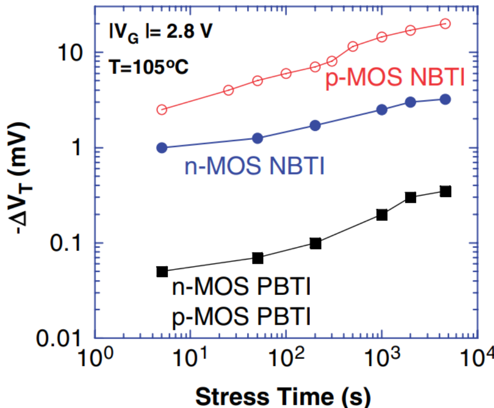

Figure 2.1: Threshold voltage shifts for p- and n-MOSFETs for positive and negative gate bias [10].

In case of organic FETs [15, 16], with the application of gate bias stress, a decrement in the source-drain current has been observed, which corresponds to a shift of the threshold voltage. The most commonly accepted mechanism associated with this voltage shift is accumulation of charge in the dielectric layer and/or at the interface between semiconductor/metal and dielectric. Nonetheless, it has been reported that charge trapping on the dielectric surface could be semiconductor-independent and depends on electrochemical reactions taking place under positive and negative bias

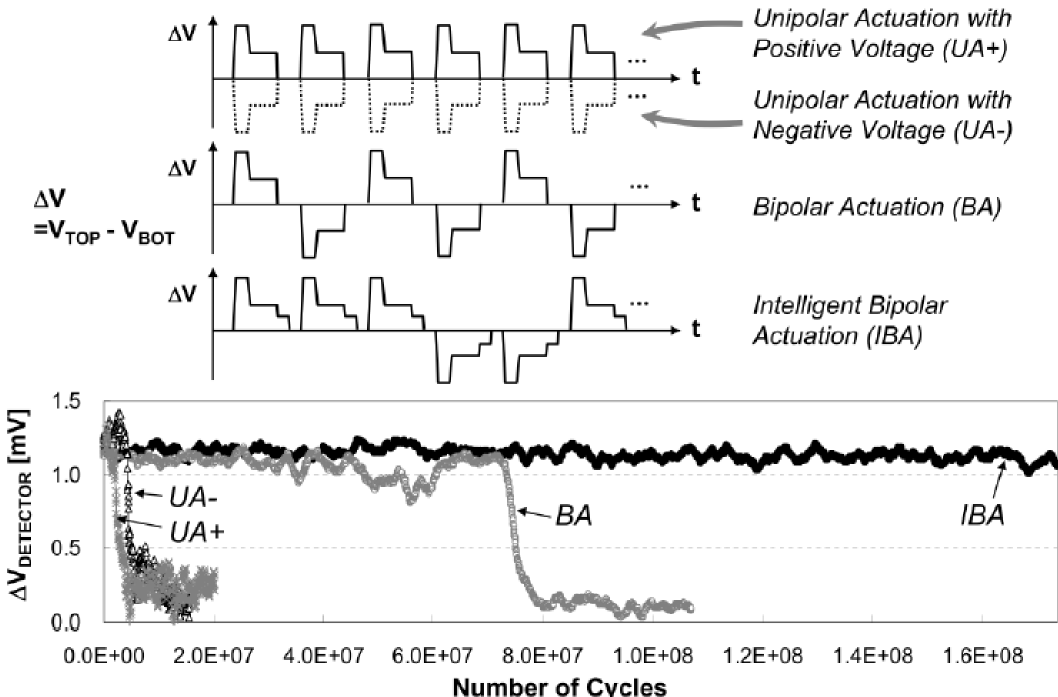

Figure 2.2: Comparison of measured lifetimes between for different methods: positive and negative unipolar actuation, bipolar actuation and IBA [22].

stresses [17]. Thus, charge induced by gate bias stress [18, 19] imposes rudimentary impediment to the commercial applications of organic semiconductors.

In microelectromechanical systems (MEMS) devices that operate electrostatically, accumulation of parasitic charge in the dielectric layer also poses serious reliability problems, preventing their use in many commercial applications [20, 21, 22, 23]. Effects such as the shift in the capacitance-voltage (CV) characteristic and even permanent stiction of movable mechanical parts to actuation electrodes in case of varactors and RF switches [24, 25, 26] or changes of the resonant frequency in oscillators [27, 28, 29] are induced by trapped charge in the dielectric. Although the effects of charging on MEMS performance have been extensively studied, obtaining mitigation strategies is still an open challenge. For example, open loop [30, 31] and closed loop [22, 32] control strategies have been proposed as a promising way to reduce the long-term effects of dielectric charging. Figure 2.2 shows the device lifetimes comparison when a MEMS switch is actuated with four different methods: positive and negative unipolar actuation, bipolar actuation and intelligent bipolar actuaton (IBA) [22].

On the other hand, perovskite based photovoltaic cells suffer from degradation effects affecting

their long-term stability. Most of the research aimed at improving the stability of the perovskite focus on varying the manufacturing process and/or the materials used. However, many recent works published have linked the degradation of perovskites to the presence of trapped charge in the layers [33, 34, 35, 36]. In particular, it has been pointed out that the presence of trapped charge in grain boundaries, either positive or negative, triggers the degradation in perovskite materials. This trapped charge is due to ionic vacancies, which are able to move through the prevoskite and also affect the interfaces with the electron and hole transport layers. Depending on the species involved, ionic vacancies can exhibit dynamics with different activation energies and time constants [37, 38]. Typical effects of perovskite cells such as current-voltage curve (J-V) hysteresis or their behaviour at different time scales have been explained recently by combining coupled ionic and electronic charging effects [39].

In order to pacify the issues of dielectric charge trapping, closed loop control techniques based on sigma-delta modulation have been proposed [40, 41, 42]. These techniques involve bipolar actuation waveforms, $BIT0/BIT1$, and indirect charge sensing from quasi-differential capacitance measurements. In this case, control loops always try to compensate any deviations from the desired target charge in the dielectric by generating an adequate sequence of actuation waveforms, thus maintaining the charge at desired level. These strategies serve as effective ways of compensating the effects of charge trapping, even in the presence of external disturbances.

Since charge trapping phenomena plays a significant role in the operating characteristics of various electronic devices, a better insight into the charging mechanisms is necessary to obtain good analytical models that describe the influence of charge accumulation on the device behavior. Nonetheless, despite the advances in modeling, the dielectric charging issue is still an open challenge limiting the use of some semiconductor devices in a large set of commercial applications.

2.1.2 Charge Trapping in MOS Devices

Charge trapping in gate oxide layers has been widely identified as one of the key factors affecting the reliability of many MOS-related devices [43]. In earlier times, during the fabrication process, it is more likely that charged mobile ions such as Na^+, K^+ get incorporated into the oxide layer of the structure that led to deterioration of the device characteristics [44]. Extensive works have been carried out to show the impact of this charge migration on the instability issues resulting in the failure of MOS devices [45, 46]. However, with the recent advancements in fabrication processes, the effects of these ionic contaminations have been significantly reduced.

One of the key elements that enables the improvement of integrated circuits (ICs) performance is the gate dielectric material used and its electrical properties. Traditionally, silicon dioxide (SiO_2) has been the primary choice as a gate insulator since it can be thermally grown and can form a very stable interface with the silicon substrate. MOS devices with SiO_2 as the gate dielectric have been thoroughly studied and relatively well understood in the past decades. SiO_2 has a main advantage of being made from Si by thermal oxidation and forming an excellent interface with Si, while other semiconductors such as Ge, GaAs, GaN form a poor native oxide.

However, with phenomenal downscaling of the MOS devices to smaller physical dimensions

in order to improve the device performance, so does the gate oxide thickness, leading to a severe leakage current across the dielectric. As the requirement for new dielectric materials has become evident and with the evolution of new technology, many new materials have been studied. In this regard, alternate materials with high dielectric constant (high-k) gate dielectrics such as Al_2O_3, HfO_2, ZrO_2, TiO_2, Ta_2O_5 [47, 48, 49] have been actively investigated with an aim to replace the traditional SiO_2 as the oxide layer. Regardless, it is crucial to ensure that the electrical interface between the chosen dielectric and the semiconductor needs to have less pronounced defect states. At the same time, the chosen oxide must create a large band offsets with the adjacent semiconductor (typically $> 1eV$) in order to restrict the conduction of electrons or holes by Schottky emission to the bands of the oxide [50]. Figure 2.3 shows the inverse relation of dielectric values with the bandgap of various oxides [51].

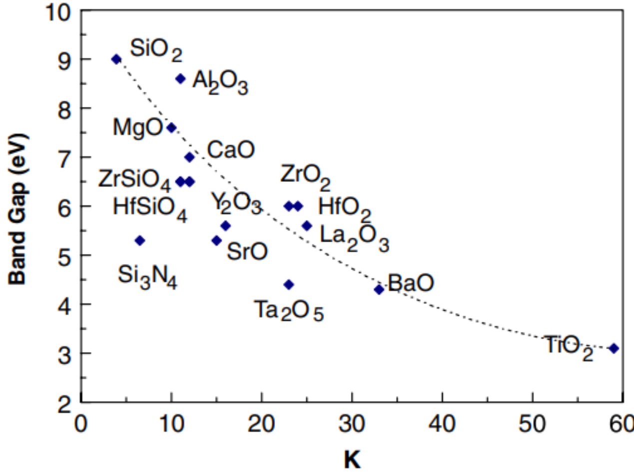

Figure 2.3: Dielectric constant versus band gap for different gate oxides [51].

Except for few materials such as Al_2O_3, ZrO_2, Y_2O_3, most of the high-k dielectrics have smaller band gap and smaller conduction and valence band offsets, limiting their incorporation into commercial ICs.

On the other hand, the presence of oxide network defects introduce energy levels into the bandgaps of oxide layer, thus acting as charge traps for electrons and holes [2, 52], while the defects located near the oxide-semiconductor interface introduce energy levels in the silicon, acting as interface traps. The physical mechanisms responsible for such charge trapping are rather complex and, for a given device type, mainly dependent on the fabrication process, the temperature, ionizing radiation, and the applied stress [53, 54, 55, 56, 57, 58, 59, 60].

It has been identified that the buildup of the densities of these oxide trap and interface trap charges when bias is applied at elevated temperatures leads to a degradation phenomena known as Bias Temperature Instability (BTI) [61, 62, 63]. The resulting phenomena manifests as a shift in

threshold voltage and a decrease of carrier mobility which could possibly influence the long term reliability leading to circuit failures [64]. Several studies have been undertaken [65, 66] to understand the nature of these instabilities related to gate oxide traps and their properties. Numerous models have been developed to analyze the effects of oxide traps on the behavior of MOS structures.

In order to investigate and gain the insight about charge injection mechanisms in the MOS devices, MOS capacitors have been extensively used as a two-terminal test structures. Ease of fabrication, simplicity of analysis, and simple structure allows it to serve as the most powerful tool for investigating the electrical properties of the MOS structure. Figure 2.4 shows the cross-section of an MOS structure.

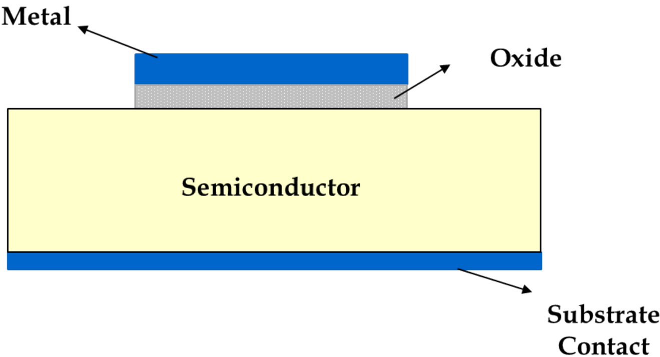

Figure 2.4: The metal-oxide-semiconductor structure.

Extensive measurements on MOS capacitors reveal a lot of information regarding the oxide quality. The oxide layer can be inadventently contaminated with some defects during oxide growth or processing steps resulting in different types of charges and traps. The reliability and performance of the devices strongly depend on these charges in the bulk oxide and at the oxide-semiconductor interface. Thus maintaining the quality and realiability of gate oxides has become one of the most challenging tasks. The details about the origin and properties of these charges have been discussed in Chapter 3. The non-uniform distribution of these charges within the oxide layer would also affect the device characteristics [67, 68].

The amounts of bulk oxide traps and interface traps increase with the levels of voltage stress applied to the gate oxides. To illustrate the effects of bias voltages on the charge traps and on CV shift, the case of a SiO_2/Si structure is considered. When a large positive bias voltage is applied at the gate electrode, electrons are injected from the semiconductor into the traps of the oxide layer. This trapping of electrons in SiO_2 results in a linear shift in the CV characteristic in positive direction with the applied bias until dielectric breakdown occurs. Whereas the application of negative bias causes the release of trapped electrons from the oxide layer and results in negative shifts in the CV curves. However, the charge injection mechanism is complex and it depends not only on the applied voltages, but also on the previous bias history.

In case of Al_2O_3/Si [69, 70], with the application of a small negative gate bias, electrons from the gate electrode gets injected into the oxide, causing a positive voltage shift. The electron trapping near Si/Al_2O_3 interface is more efficient, which implies that more energy is needed to trap electrons at negative bias compared to positive bias. The trapped electrons near the interface (due to positive bias) are more easily released compared to those away from the interface (due to negative bias) and hence positive voltage shift caused by the negative biases decay slowly than those due to the positive biases. However, when a large negative bias is applied, current through the oxide increases exponentially, which results in the release of trapped electrons causing negative voltage shifts. In short, the threshold voltage instability in MOS devices is caused by a voltage dependent charge exchange between the gate electrode and the semiconductor.

Alternative gate dielectrics with good electrical characteristics have been widely investigated for MOS applications. High-k dielectric materials have larger charge storage capacity compared to SiO_2, allowing them to have physically thicker gate oxide while maintaining lower electrical thickness. Among the high-k dielectrics, HfO_2 seems to be promising due to its relatively large bandgap, good thermal stability, and high dielectric constant. However, unlike SiO_2 films, high-k dielectrics tend to exhibit significant charge trapping. The charge trapping properties of ultrathin HfO_2 MOS capacitors during constant bias stress have been investigated in [71]. The influence of bias voltage, substrate type, annealing temperature, and gate electrode on trapping of charge has been discussed. Moreover, a model has been developed [72] to predict the threshold voltage shift due to charge trapping, at different stress voltages and temperatures over decades of stress time, for Al_2O_3 and HfO_2 based MOS devices. However, forming a chemically stable interface between HfO_2 and Si remains a challenge.

On the other hand, different types of semiconductor substrates other than silicon have been explored. For example, silicon carbide (SiC) has a wide bandgap and high thermal conducitivity, making it a strong contender for use in high-power MOS devices. Recently, group III-V compound semiconductor based ($GaAs, InGaAs$) MOS devices have been projected as active replacements to silicon devices for high-performance digital applications [73, 74] due to their high mobility. It has been reported in [75] that $Al_2O_3/\beta - Ga_2O_3$ MOS capacitors trap predominantly negative charge during positive voltage stress due to electron trapping in Al_2O_3 and the trapping increases with increasing stress bias. However, the poor electrical characteristics of oxide-semiconductor interface results in higher interface trap density and oxide traps [76, 77, 78].

Interestingly, the property of charge trapping in MOS devices has been exploited to use them predominantly as chemical or gas sensing elements [79, 80, 81, 82, 83] by virtue of their high sensitivity and selectivity, especially at high temperatures. It has been first reported in [84, 85] that semiconductor field effect devices could be made gas sensitive by incorporating catalytically active elements such as platinum, iridium, palladium as metal electrodes. These structures operate by exploiting the drifts in the device parameters such as threshold voltage shift [86] or field-effect mobility [87] upon exposure to chemical species, allowing them to detect the chemical elements.

For example, in [88, 89], sensors based on platinum metal MOS capacitor have been used to detect the saturated hydrocarbons by sensing the changes in the flatband voltage of the capacitor.

Similarly, the changes in the threshold voltage of a silicon MOSFET with a palladium (Pd) metal electrode in [90] have been attributed to a decrement in the electronic work function of the Pd due to adsorption of hydrogen at the $Pd - SiO_2$ interface. In [91], the sensing response of a PdMOS (Pd gate metal-oxide-semiconductor) transistor has been improved by eliminating the hydrogen-induced drift issues. In recent years, field-effect transistors have been used as gas sensors to detect NO_2 by sensing the threshold voltage shifts due to gate bias induced electron trapping [92, 93]. Also, the time response of the gas sensors have been improved by compensating the charges induced by the target gases [94].

2.1.3 Ionizing Radiation on MOS Devices

Microelectronic devices are fundamental components in space exploration systems. Exposure of these electronic systems to various types of radiation, in general, could detrimentally affect their electrical performance, sometimes leading to complete failure. Understanding radiation effects on the operation of semiconductor devices remains crucial to the advancements in space applications. There have been extensive studies on the sources of radiation and its effects on the semiconductor devices [95, 96, 97]. The main motivation prompting the serious investigation of the radiation effects dates back to 1962, when the Telstar 1 communication satellite failed due to radiation from the Starfish Prime operation [98] and the Van Allen belts [99]. Furthermore, erroneous behaviours have been registered in the electronic systems in many applications including space [100, 101], avionics [102, 103], nuclear [104], and military [105]. When operating in such environments, the electronic devices may get struck by electrons, protons, neutrons or other heavier particles, thus altering their functionality/electrical properties and causing their failure. Another driving force for the active research in the area of radiation is the radiation damage caused by fabrication processing techniques such as electron-beam lithography [106, 107], X-ray lithography [108], reactive ion etching [109]. In this regard, investigation of radiation effects in the semiconductor devices is of paramount importance for the development of the circuits that can operate properly in radiation-rich environments.

Ionizing radiation exposure in semiconductor devices generates electron-hole pairs (EHPs). In case of MOS devices, these EHPs are created by the energy deposited in the gate oxide layer. These generated charge carriers further induce the buildup of charge leading to device degradation. The major mechanisms contributing to such degradation are depicted using a band diagram as shown in Figure 2.5 for a p-substrate SiO_2 MOS capacitor under a positive gate bias.

Most of the radiation induced free electrons, being extremely mobile, are immediately swept towards the gate under the influence of positive bias, while the holes drift towards the oxide-semiconductor (SiO_2/Si) interface. However, depending on the applied field and the incident radiation energy, a small fraction of electrons and holes recombine within the first few picoseconds which is referred to as initial recombination. The fraction of electron/hole pairs that escape recombination is called charge yield. Figure 2.6 provides the data for the dependence of fraction of unrecombined holes on the electric field in the oxide for different energy particles. As the electric field strength increases, the probability of electron-hole pair recombination decreases and this

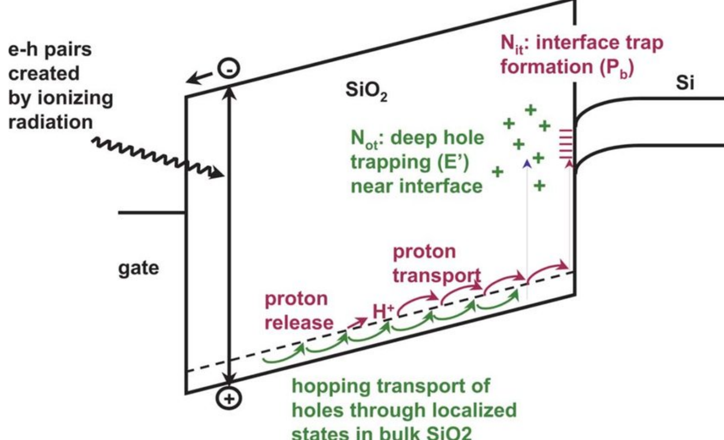

Figure 2.5: Radiation response effects in MOS structures [110].

results in an increase in the total number of unrecombined holes, given by

$$N_h = f(E_{ox}) g_0 D t_{ox} \tag{2.1}$$

where $f(E_{ox})$ is the hole yield as a function of the electric field applied to the oxide, D is the total radiation dose, t_{ox} is the oxide thickness, and g_0 is a material-dependent parameter giving the initial charge pair density per radiation dose.

The holes that escape the initial recombination undergo an anomalous hopping transport through the oxide towards the SiO_2/Si (positively applied gate bias) or the gate/SiO_2 (negatively applied gate bias) in response to an electric field present. Under the positive gate bias, some fraction of holes gets trapped near the interface in the oxygen vacancies formed due to the out-diffusion of oxygen in the oxide [111]. These trapped holes form a cloud of positive oxide-trap charge, denoted by N_{ot}, and cause a negative shift (ΔV_{ot}) in the electrical characteristics of the device. In addition, there is a buildup of radiation induced interface traps, N_{it}, at the SiO_2/Si interface within the silicon bandgap. As seen in Figure 2.5, protons that are released during the hole transport have been linked to the interface trap formation. These interface traps can be positive, neutral, or negative. In general, it is widely accepted that traps in the lower portion of the band gap are predominantly donors and hence are positively charged, while the traps in the upper portion of the band gap are predominantly acceptors i.e., the traps are negatively charged [110]. Thus these traps can contribute either a net positive or negative charge depending on the silicon surface potential and therefore resulting in a negative or positive shift (ΔV_{it}) in the device characteristics. So, considering the effects of the two types of traps, the shift in the threshold voltage, ΔV_{th}, of the device is the sum of the threshold-voltage shifts due to oxide-trap and interface-trap charges, i.e.,

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it} \tag{2.2}$$

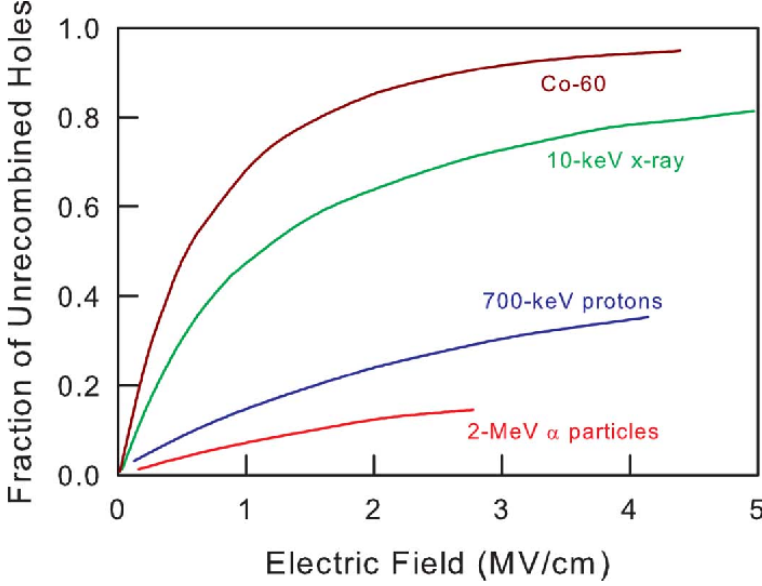

Figure 2.6: Charge yield vs electric field in the oxide for low energy protons, alpha particles, gamma rays (Co-60), and x rays [110].

These undesirable radiation induced shifts in the threshold voltage due to the trapped charge could result in malfunction and sometimes failure of the systems. For example, in case of CMOS devices, if ΔV_{th} is large enough, the device may enter into ON state even at zero bias applied, resulting in an undesired device operation. Besides, trapping of positive charge can create leakage paths by inverting the underlying Si and enables leakage current to flow in the OFF state (i.e., $V_{GS} = 0$). This means an increase in the static power supply current, which eventually could result in the failure of an IC.

The irradiation of MOS structures has gone through a lot of research for different kinds of radiation exposures. A lot of research work related to radiation is driven by the need for the development of radiation-hardened devices. It has been observed that exposure to any ionizing radiation with a photon energy more than the bandgap of SiO_2 can induce a net positive trapped charge in the oxide region. Typical radiation dos over which most of the radiation effects could occur ranges between 10 Gy(SiO_2) and 1 MGy($SiO2$), see Figure 2.7.

The shift in threshold voltage of an NMOS transistor with irradiation dose biased at different gate voltages is shown in Figure 2.8. It can be seen that the more positive the field is from the gate to the substrate, the faster is the threshold voltage shift. But, as the bias voltage increases to 10V, the holes traverse the oxide too fast to get trapped and so the threshold voltage shifts less. In case of n-channel transistors [113], an irradiation sensitivity of 1.2 mV/Gy(SiO_2) is obtained at 500 Gy(SiO_2), whereas displacement of 0.4 mV/Gy(SiO_2) at 1 kGy(SiO_2) is obtained in [114].

Similarly, MOS capacitor with SiO_2 as dielectric subjected to $Co60$ irradiation at a total dose of

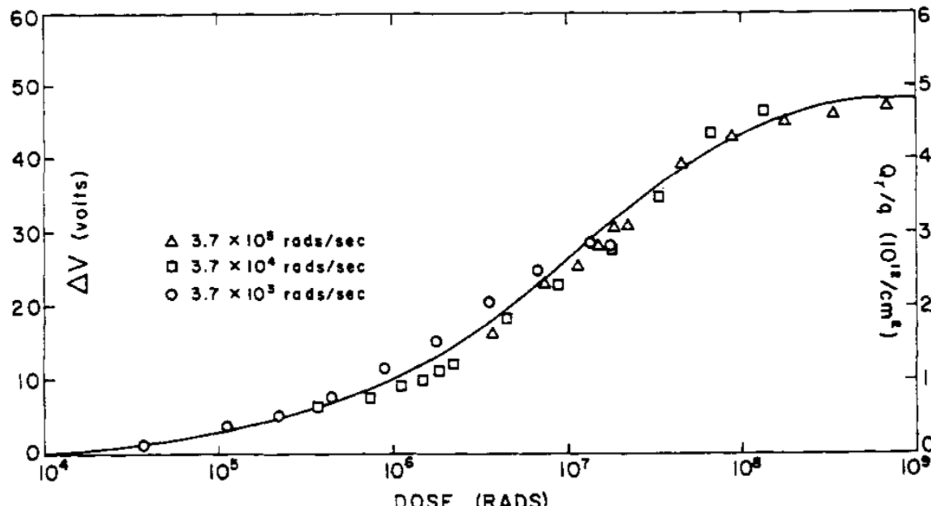

Figure 2.7: Voltage shift in the CV characteristics of the MOS capacitor and the corresponding trapped oxide charge as a function of radiation dose at various dose rates [112].

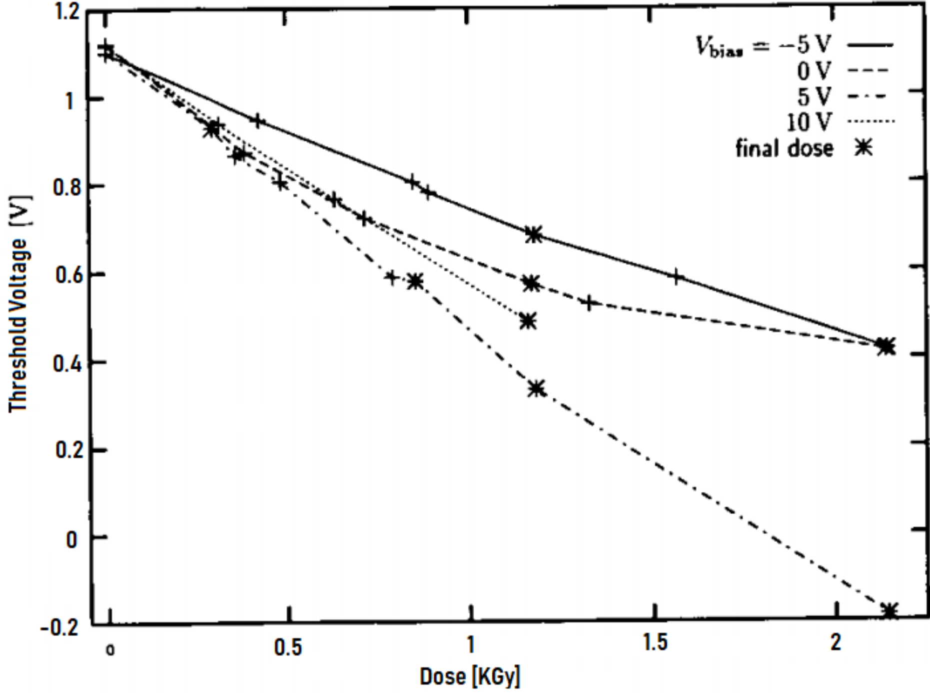

Figure 2.8: Threshold voltage vs irradiation dose [115].

1 KGy with 10V applied to the gate results in an irradiation sensitivity of 2mV/Gy(SiO_2) [116] corresponding to the generation of nearly $1.1e^{11}$ electron-hole pairs. The capacitors measured in [117], biased at 10V during irradiation, exhibit displacements of 1.33 mV/Gy(SiO_2) for a total dose of 300 Gy(SiO_2), decreasing to 0.8 mV/Gy(SiO_2) for 1kGy(SiO_2). In [118], 0.625 mV/Gy(SiO_2) at 120 Gy(SiO_2) is obtained with 5 V biased MOS capacitors. For a 100-nm-thick oxides, the sensitivity obtained has been 2.38 mV/Gy [119]. In case of high-k dielectric based MOS devices, the irradiation sensitivity is approximately 72 mV/Gy for a 140-nm thick Al_2O_3 [120], 10 mV/Gy for 120-nm thick Sm_2O_3 [121], and 5.32 mV/Gy for 150-nm thick La_2O_3 [122]. The irradiation sensitivities for various MOS capacitors can be seen in Table 2.9.

Oxide	Thickness (nm)	Frequency (kHz)	Dose (Gy)	Sensitivity (mV/Gy)	Flat band voltage shift direction
$BiFeO_3$	300	1000	16	~48.1	Continuous right side shift
Er_2O_3	254	100	16	107	Bidirectional shift
Er_2O_3	254	100	76	61	
Gd_2O_3	114	100	50	39.7 ± 1.4	Continuous right side shift
HfO_2	180	1000	480	~1.9	Continuous right side shift
La_2O_3	150	1000	64	5.3	Continuous left side shift
SiO_2	240	1000	16	7.8	Continuous left side shift
SiO_2	240	1000	64	4.0	Continuous left side shift
Sm_2O_3	120	100	30	—	Continuous right side shift
Sm_2O_3	120	1000	30	10	Continuous left side shift
Y_2O_3	150	1000	128	10.8 ± 0.4	Continuous left side shift
Yb_2O_3	114	100	70	27.5 ± 1.1	Continuous left side shift
Yb_2O_3	114	1000	70	28.1 ± 1.3	Continuous left side shift

Figure 2.9: Irradiation sensitivity values for different MOS capacitors [123].

In case of MEMS, different studies about the effects of ionizing radiation on RF-MEMS switches have been carried out to determine the influence of this phenomenon on the device lifetime [124, 125, 126]. Alternate design configurations have been implemented to reduce dielectric charging due to polarization and radiation [127]. In [128], it has been reported that X-ray radiation induced noticeable negative charge in MEMS dielectric. However, the recovery of the device has been slow and charge removal is partial at the end of experiment, as seen in Figure 2.10.

Amidst all these reliability issues due to ionizing radiation, there is a need to develop radiation hardened components in order to ensure proper operation of the systems. Changes in the processing conditions and incorporation of high-k dielectric materials into ICs may tend to improve the radiation response. In [129], it has been shown that Al_2O_3 devices, when received the additional O_2 anneal exhibited enhanced radiation hardness relative to the devices which received only a FGA (Forming Gas Anneal). The electrical characteristics and radiation response of high-k dielectric MOS devices can be influenced by the quality of oxide/Si interface, the film growth process, energy bandgap of dielectric resulting in an increase of interface traps. Also, the thickness of the interfacial layer in a high-k dielectric stack devices can impact the buildup of the radiation induced trapped charge. The defect microstructures in these dielectric stacks can lead to degraded interface quality

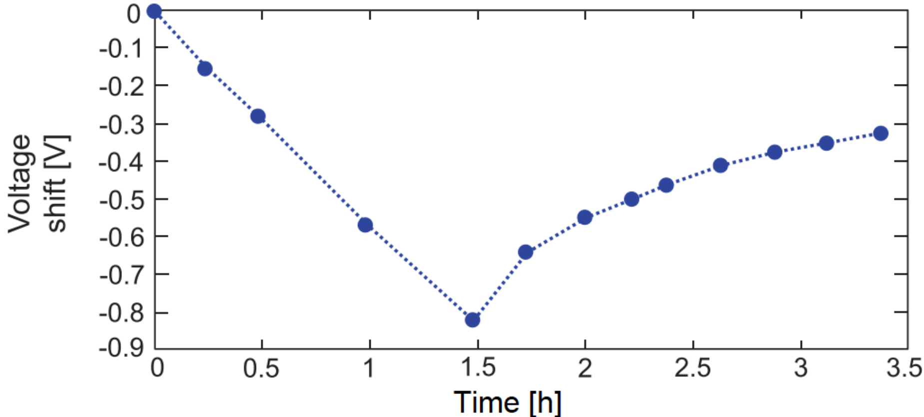

Figure 2.10: Evolution of voltage shift when the MEMS is irradiated for the first 1.5 h, then not irradiated for the next 2 h. The actuation bias is 0V during all the time [128].

with interface trap densities 100 times larger than in conventional SiO_2 oxides [130].

As a part of this thesis, the effects of ionizing radiation (Gamma rays and X-rays) on charge trapping in the dielectric layer of a MOS capacitor is discussed in Chapter 4. A closed loop control scheme has been implemented on the device to compensate the radiation induced charge trapping and improve the lifetime of the device operating in hardness environments. Real-time information about the charge being induced by radiation can be obtained by monitoring the average bitstream provided by the control loop. This may allow the possibility of using this method in radiation detection applications such as RADFET devices specially designed for radiation sensing.

RADFETs or radiation dosimeters operate using the principle of sensing the radiation dose or charge trapped by measurement of the drift in threshold voltage [131]. MOS dosimeters have found wide range of applications due to its small size, low power requirements, reproducibility etc. However, in some cases, exposure to high energy radiation would saturate the drift in threshold voltage making the readings incompatible. Several techniques have been proposed to extend the lifetime of the RADFETs by delaying/avoiding the saturation of the shift of threshold voltage with accumulated dose. In [132] periodical charge neutralization of radiation-induced trapped charge is performed to keep the threshold voltage of RADFETs between some predetermined limits. Measurement is carried out in open loop configuration between bias switching operations. Some works have focused on obtaining a trapped hole annealing in order to delay the saturation of the sensor and to keep it working in near optimal conditions. This has been achieved by applying bias switching [133]. On the other hand, Fowler-Nordheim tunnelling is used in [134] to compensate holes trapped in the buried oxide layer of a monolithic pixel detector used in high-energy physics, X-ray imaging etc.

2.2 Modeling of Charge Dynamics

The characterization of the charge trapping dynamics in MOS devices has been extensively studied [135]. In this thesis, a state-space model characterizing the dynamics of trapped charge in MOS capacitor using Diffusive Representation (DR) has been obtained and the behavior of the device under control has been predicted using a specific analytical model, derived from the Sliding Mode Control (SMC) theory.

In the recent times, the models based on continuous sliding mode controllers (SMCs) have been employed to analyze the charge dynamics in MEMS [136], and improving the response of wind sensors [137]. On the other hand, discrete-time SMCs proposed for applications such as position tracking control of linear motors [138], [139] have been found to achieve better performances compared to the continuous SMCs. In addition, non-singular terminal sliding mode (NTSM) control, combined with finite-time observers [140] and backpropagating constraints [141] has been implemented for accurate tracking of systems with unknown dynamics affected by external disturbances.

In this regard, DR and SMC have been applied together in trapped charge analysis, where the diffusive symbols extracted using DR modeling have been used to predict the behavior of the system under closed loop control and in the presence of external disturbances.

2.2.1 Diffusive Representation

Diffusive Representation is a mathematical tool well-suited to describe any diffusion-based physical phenomena, thanks to the properties of diffusion equations. It has been successfully used in approximation of fractional-order systems in practical implementations, such as thermal [142, 143, 144] and electrical [145, 146] modelings. This method allows the description of a physical phenomena based on diffusion using state-space models of arbitrary order.

The main advantage of diffusive representation is that it is possible to obtain reduced order models of long-memory systems without great computational load. Besides, these state-space models are very well suited to describe the behavior of diffusive systems under nontrivial controls, such as sliding mode controllers (see section 2.2.2). Therefore this has been the method employed in the characterization of the systems related to the content of this Thesis.

The theory of DR was developed with an aim of transforming long memory fractional operators, which is often present in most physical models, into input-output dynamic representation of systems [147, 148]. Although fractional integrodifferential operators can accurately model the systems with long memory dynamics, the state space representation has been revealed to be convenient for analysis as well as modeling and control issues, in particular, when long-memory dynamics are present [149, 150, 151, 152]. The dynamic systems describing complex physical phenomena, which follows a power-law time-dependence, could be effectively modelled using DR as an input-output state-space model.

The modeling approach based on DR has recently been employed recently in thermal characterization of the wind sensors [153, 154, 155], modeling of power electronic components [156], and trapped charge characterization in MEMS [157]. In this Thesis, we have applied this modeling

method to the identification of the dynamic model of a MOS capacitor and the obtained model describes the dynamics of trapped charge in the dielectric layer. In this regard, the theoretical concept about Diffusive Reperesentation has been explained in this section.

Diffusive representation allows obtaining exact and approximation state realizations of a wide class of integral operators [158, 159] of rational or non-rational nature. Given a non-rational transfer function, $H(p)$, associated with a convolution causal operator denoted by $H(\partial_t)$, the diffusive realization of this operator is expressed by the following input (u) – output (y) state-space realization of $u \longmapsto y = H(\partial_t)u = h * u$ of the form [145]:

$$\begin{array}{lcl} \frac{\partial \psi(\xi,t)}{\partial t} & = & -\xi\psi(\xi,t) + u(t), \quad \psi(\xi,0) = 0 \\ y(t) & = & \int_0^\infty \eta(\xi)\psi(\xi,t)d\xi \end{array} \tag{2.3}$$

where $\xi \in \mathbb{R}^+$ is frequency, $\eta(\xi)$ is the diffusive symbol of $H(\partial_t)$ that represents how the system behaves, and the state-variable $\psi(\xi,t)$ is a time-frequency representation of the input, called the diffusive representation of $u(t)$ [145]. In general, and in the case of linear processes, the identification under diffusive representation consists in the determination of the difffusive symbol $\eta(\xi)$, (or $\eta(\xi,t)$ if applicable), that completely characterizes the system in a state-space form. It must to be noted that the non-linear case can also be approached through the extension of the theory [160]. The diffusive symbol $\eta(\xi)$ is a solution of the frequency domain equation (2.4), which is directly obtained from the Laplace transform (with respect to t) of the trasfer function $H(p)$ [145]:

$$H(j\omega) = \int_0^\infty \frac{\eta(\xi)}{j\omega + \xi} d\xi \quad \omega \in \mathbb{R} \tag{2.4}$$

The impulse response $h := \mathcal{L}^{-1}H$ can also be expressed from $\eta(\xi)$ [145]:

$$h(t) = \int_0^\infty e^{-\xi t}\eta(\xi)d\xi \tag{2.5}$$

and, reciprocally, the diffusive symbol can be given also as the inverse Laplace transform of the impulse response: [145]

$$\eta = \mathcal{L}^{-1}h \tag{2.6}$$

It must be noted that since ξ is a continuous variable it is possible to handle infinite order systems, such as in the case of fractional operators. The complexity of equation (2.3) is intermediate between ordinary differential equations (ODE)s and partial differential (PDE)s ones. Therefore, this unified form benefits from the combination of the dynamic richness of a PDE together with the straightforward rational approximation [145].

To be able to handle experimental data, a finite-dimensional approximation, arbitrarily close to the original operator, $H(\partial_t)u$, can be built discretizing the continuous variable ξ into $\{\xi_k\}_{1\leq k\leq K}$, where K is the finite order of the discretized model. This leads to an input – output approximation $u \longmapsto \tilde{y} \approx H(\frac{d}{dt})u$. The discretized model can be described by:

$$\begin{aligned} \frac{d\psi_k(t)}{dt} &= -\xi_k\psi_k(t) + u(t), \quad \psi_k(0) = 0 \\ \tilde{y}(t) &= \sum_{k=1}^{K} \eta_k\psi_k(t) \end{aligned} \tag{2.7}$$

where $\psi_k(t) = \psi(\xi_k, t)$ and $\eta_k = \eta(\xi_k)$ with $\eta_k \in \mathbb{R}^K$.

Figure 2.11 shows the block diagram of the discrete diffusive representation of the Laplace transform of equation (2.7).

The goodness of the approximation will depend on the chosen frequency mesh $\{\xi_k\}_{1\leq k\leq K}$, in the band of interest and in concordance with the dynamic characteristics of the system [142]. The mesh is usually chosen so that the frequencies are geometrically spaced:

$$\xi_{k+1} = r\xi_k, \qquad r = \left(\frac{\xi_K}{\xi_1}\right)^{\left(\frac{1}{K-1}\right)} \tag{2.8}$$

This choice allows a constant quality of approximation (in terms of relative error) in each frequency decade over the whole frequency band under consideration [145]. The chosen bandwidth for ξ goes from $\xi_{min} = 2\pi/T$ to $\xi_{max} = \pi/T_s$, (in rad/s), where T is the total duration of the measurements (long enough for the stabilization of the system), and T_s is the sampling period. Therefore, the experiment duration and the sampling period set a limit on the minimum and maximum frequency, respectively. When the system under consideration is time-invariant, η_K converges, under suitable conditions, to the exact (but unknown) diffusive symbol:

$$\eta_K \underset{K\to\infty}{\longrightarrow} \eta \tag{2.9}$$

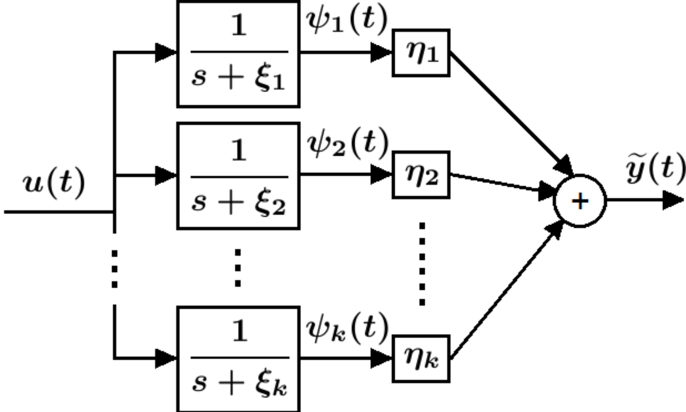

Figure 2.11: Block diagram of the Laplace transform of the discrete diffusive representation model of (2.7)

Which means that if the frequency mesh is sufficiently dense, it is possible to describe with arbitrary accuracy the response of any fractional system.

The inference of the diffusive symbol is done from the experimental data. Considering that the measurement data is distributed in a temporal mesh, $[t_n]_{1\leq n\leq N} \in \mathbb{R}^+$, we can define the matrix $\mathbf{A} = [\psi_k(t_n)]$ and the output vector of measurements as $\mathbf{Y}^T = [y(t_0), \ldots, y(t_n), \ldots, y(t_N)]$. Taking this notation into account, the solution to the identification problem is found solving the finite dimensional least squares problem formulated by [142]:

$$\min_{\eta\in\mathbb{R}^K} ||\mathbf{A}\hat{\boldsymbol{\eta}} - \mathbf{Y}||^2 \tag{2.10}$$

that is clasically solved by the standard pseudo-inversion method:

$$\hat{\boldsymbol{\eta}} \quad = \quad [\mathbf{A}^*\mathbf{A}]^{-1}\mathbf{A}^*\mathbf{Y} \tag{2.11}$$

The model identfication problem is often ill-conditioned because the matrix $[\mathbf{A}^*\mathbf{A}]$ is close to a non-invertible one. This problem is usually solved by adding a small penalization term $\epsilon > 0$ to the equation [142]

$$\hat{\boldsymbol{\eta}} \quad = \quad [\mathbf{A}^*\mathbf{A} + \epsilon\mathbf{I}]^{-1}\mathbf{A}^*\mathbf{Y} \tag{2.12}$$

where $\mathbf{I}$ is the identity matrix and the parameter ϵ is chosen as small as possible as long as $\hat{\eta}$ remains quasi-insensitive to important relative variations of ϵ. In practice, very small values of ϵ are sufficient to stabilize the problem.

It has to be mentioned that when solving numerically the integral of equation (2.3), to deal with numerical approximations, standard quadrature methods have to be used. One method is based on the use of linear interpolation [145]:

$$\eta_k = \eta(\xi_k)\int_0^{+\infty} \Lambda_k(\xi)d\xi = \eta(\xi_k)\frac{\xi_{k+1} - \xi_{k-1}}{2} \tag{2.13}$$

with Λ_k the classical interpolation function defined by:

$$\Lambda_k(\xi) = \begin{cases} 0, & \text{for } \xi \leq \xi_{k-1} \text{ or } \xi \geq \xi_{k+1} \\ \frac{\xi-\xi_{k-1}}{\xi_k-\xi_{k-1}}, & \text{for } \xi_{k-1} < \xi < \xi_k \\ \frac{\xi_{k+1}-\xi}{\xi_{k+1}-\xi_k}, & \text{for } \xi_k < \xi < \xi_{k+1} \end{cases} \tag{2.14}$$

where for $k = 1$ and $k = K$, fictious points are introduced: $\xi_0 = \xi_1/r$ and $\xi_{K+1} = r\xi_K$, being r the ratio of the geometric sequence of the mesh of ξ defined in (2.8). Regarding to the identification problems of this Thesis, to solve the integral from equation (2.3) a logarithmic change of variable has been used due to the fact that ξ variable has been chosen to be spaced geometrically. Specifically, $\xi = 10^x$ and $d\xi = ln(10)10^x dx$. Taking this into account, the second expression of equation (2.3)

becomes:

$$y(t_n) \quad = \quad \int_{x_0}^{x_1} \eta(10^x)\psi(10^x, t)ln(10)10^x dx \approx \sum_{k=1}^{K} \eta_k \psi_k(t_n)\lambda_k \tag{2.15}$$

Therefore, $\eta_k = \frac{\hat{\eta}_k}{\lambda_k}$, where $\lambda_k = ln(10)log(r)\xi_k$.

In this thesis, we have considered the general case of η_k being time-varying considering the varying charge injection conditions with applied voltage waveforms. With respect to that, in order to maintain the linearity of the model, it was necessary to reformulate the discretized approach from equation (2.7).

$$\begin{array}{rcll} \psi_k^{(n)}(t) & = & 0 & t \in [t_0, t_n] \\ \dot{\psi}_k^{(n)}(t) & = & -\xi_k \psi_k^{(n)} + u(t) & t \in [t_n, t_{n+1}] \\ \dot{\psi}_k^{(n)}(t) & = & -\xi_k \psi_k^{(n)} & t > t_{n+1} \end{array} \tag{2.16}$$

$$\tilde{y}(t) \quad = \quad \sum_{n,k} \eta_k^{(n)} \psi_k^{(n)}(t) + \sum_k^K c_k e^{-\xi_k (t - t_0)}$$

where $\eta_k^{(n)} \in \mathbb{R}^K$ is the diffusive symbol associated to the conditions of the system in the n-th interval in $t \in [t_n, t_{n+1}]$. In this general formulation, the state of the system at the beginning of the measurements is taken into account thanks to $c_k \in \mathbb{R}^K$ that represents the initial conditions of the system, at $t = t_0$. The time intervals are a discretization of time for which the diffusive symbols can be considered constant in a experiment. From an experiment the discrete number of diffusive symbols that will be obtained is J. For example, in the case where the dielectric trapped charge is being characterized, J will be the number of voltage waveforms applied in the experiment. Each event $\{a_j\}_{j=1,\dots,K}$ represents the time interval of a experiment where the diffusive symbol $\eta_k^{(n)}$ is constant.

The solution again to this identification problem is found solving the finite least squares problem from equation (2.10), but in this general case, matrix $\mathbf{A}$ is of the form shown in equation (2.17) and $\hat{\boldsymbol{\eta}}^T$ is that of equation (2.18):

$$\mathbf{A} = \begin{bmatrix} \sum\limits_{n:g(n)=a_1} \psi_1^{(n)}(t_0) & \cdots & \sum\limits_{n:g(n)=a_1} \psi_K^{(n)}(t_0), & \cdots & \sum\limits_{n:g(n)=a_J} \psi_1^{(n)}(t_0) & \cdots & \sum\limits_{n:g(n)=a_J} \psi_K^{(n)}(t_0), & [1]_k \\ \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ \sum\limits_{n:g(n)=a_1} \psi_1^{(n)}(t_F) & \cdots & \sum\limits_{n:g(n)=a_1} \psi_K^{(n)}(t_F), & \cdots & \sum\limits_{n:g(n)=a_J} \psi_1^{(n)}(t_F)] & \cdots & \sum\limits_{n:g(n)=a_J} \psi_K^{(n)}(t_F), & [e^{-\xi_k (t_F - t_0)}]_k] \end{bmatrix} \tag{2.17}$$

for a experiment with $t \in [t_0, t_F]$. The function $g(n)$ returns the a_j event at every n-th time interval in $t \in [t_n, t_{n+1}]_{n=0,\dots,N}$ at which $\eta_k^{(n)}$ is constant. Returning to the wind sensor example, $g(n)$ will return the wind applied at every interval n. The last column of matrix (2.17), $[1]_k \in \mathbb{R}^K$ is an all ones vector and $[e^{-\xi_k (t - t_0)}]_k = [e^{-\xi_1 (t - t_0)}, \dots, e^{-\xi_K (t - t_0)}]$. The diffusive symbol vector that is

going to be inferred is of the form of Eq. (2.18):

$$\hat{\boldsymbol{\eta}}^T = [[\eta_1^{a_1}, \ldots, \eta_K^{a_1}]^T, \ldots, [\eta_1^{a_J}, \ldots, \eta_K^{a_J}]^T, [c_1, \ldots, c_K]^T] \tag{2.18}$$

where $[\eta_k^{a_j}]^T$ is the diffusive symbol corresponding to the a_j event. The measurements vector, $\mathbf{Y}^T$, remains as in (2.10), and the solution to the inference problem is classically given by (2.11).

In practice, small values of the model order, K, are mostly sufficient to obtain good aproximations. From the literature [145, 142] and the experiments it has been observed that low order models are enough to obtain a good fitting of the experimental data and to recover the analytical diffusive symbol. It is usually observed that increasing the model order does not improve the root mean square error between the experimental and the fitting data beyond a certain order value [157].

2.2.2 Sliding Mode Control

Sliding Mode Control (SMC) is a non-linear control technique that uses discontinuous control signals to alter the dynamics of a non-linear system in order to allow it to slide along a desired system behavior [136, 161]. The control technique has discontinuous control law designed such that the state variables of the system are forced to be confined to a predefined surface in state-space, known as sliding surface. As soon as the desired surface is reached, the feedback control maintains the system along the sliding manifold by switching between the two control signals based on the current position of the state variable. Thus, with the application of such high frequency control signals, the control technique alters the dynamics of the system. This non-linear technique inherently provides robust features such as fast dynamic response, insensitivity to variations in plant parameters and external disturbances and hence proved to be appropiate for a wide range of problems, such as robotics, process control and vehicle and motion control [162, 163, 164, 165].

The models based on continuous sliding mode controllers have been successfully employed to analyze the charge dynamics in MEMS [136], and wind sensors [137]. On the other hand, discrete-time SMCs proposed for applications such as position tracking control of linear motors [138], [139] have been found to achieve better performances compared to the continuous SMCs. In addition, non-singular terminal sliding mode (NTSM) control, combined with finite-time observers [140] and backpropagating constraints [141] has been implemented for accurate tracking of systems with unknown dynamics affected by external disturbances.

Suppose a non-linear dynamical system is described using a model with state space representation in a usual control system:

$$\dot{x} = f(x, u) \tag{2.19}$$

where $x \in \mathbb{R}^n$ is a vector which represents the state and $u \in \mathbb{R}^m$ is the control input. It is assumed that $f(\cdot)$ is differentiable with respect to x and represents a system of equations such that

$$f^+ = f(x, u^+), f^- = f(x, u^-), \tag{2.20}$$

The control u is a discontinuous function of the state such that:

$$u_i = \begin{cases} {u_i}^+(x), & \text{if } \sigma_i(x) > 0 \\ {u_i}^-(x), & \text{if } \sigma_i(x) < 0 \end{cases} \tag{2.21}$$

where $i = 1, 2, ..., n$ and we can define $\sigma_i = S_i x(t)$, being S a surface in the state space given by:

$$S = \{x : \sigma(x) = 0\} \tag{2.22}$$

An ideal sliding mode is said to take place on equation (2.22) if the states $x(t)$ evolve with time such that $\sigma(x(t_r)) = 0$ for some finite $t_r \in \mathbb{R}^+$ and $\sigma(x(t)) = 0$ for all $t > t_r$. The control u that drives the state variables $x(t)$ to the sliding surface of (2.22) in finite time, and keeps them on the surface thereafter is called a sliding mode controller [166]. The main objective is to select an admissible control law u such that the control surface $\sigma(x) = 0$ is reached in a finite time.

The closed loop dynamics of the system, under the control law of (2.21) in a discrete time interval $[nT_s, (n+1)T_s]$, is given by:

$$\dot{x} = \frac{1 + sgn(\sigma(nT_s))}{2} f(x, u^+(x)) + \frac{1 - sgn(\sigma(nT_s))}{2} f(x, u^-(x)) \tag{2.23}$$

For this section, the sign function is redefined as $sgn(\rho) = +1$ when $\rho \geq 0$ and $sgn(\rho) = -1$ when $\rho < 0$. Under the infinite sampling approximation, when T_s tends to zero, the system can be written as a switched system [161]:

$$\dot{x} = \begin{cases} f^-(x), & \text{if } \sigma > 0 \\ f^+(x), & \text{if } \sigma < 0 \end{cases} \tag{2.24}$$

If solutions starting nearby the surface are directed towards it, the switching surface is determined as attractive, which guarantees the existance of a sliding region within the control surface. This occurs if $\sigma\dot{\sigma} < 0$, [167], with $\dot{\sigma}$ computed over the system trajectories:

$$\dot{\sigma} = S\dot{x} = \begin{cases} Sf^-(x), & \text{if } \sigma > 0 \\ Sf^+(x), & \text{if } \sigma < 0 \end{cases} \tag{2.25}$$

The attractive sliding region or sliding domain, Ω is given by [167]:

$$\Omega := \{x \in \mathbb{R}^n : Sf^-(x) < 0\} \cap \{x \in \mathbb{R}^n : Sf^+(x) > 0\} \cap \{\sigma(x) = 0\} \tag{2.26}$$

Let us assume that the system defined in (2.24) undergoes over the switching surface with a sliding motion, i.e., the sliding domain Ω is nonempty. The obtention of the ideal sliding dynamics consists on obtaining a solution in the sense of Filippov [167]. A solution in the sense of Filippov is obtained when the system is defined on the sliding surface as a convex linear combination of $f^-(x)$ and $f^+(x)$, acting in the corresponding space region:

$$\dot{x} = \left(\alpha(x) f^{-}(x) + (1-\alpha(x)) f^{+}(x)\right)|_{\sigma(x)=0} \tag{2.27}$$

for $\alpha(x) \in [0,1]$. This convex combination, will be such that the derivative will be tangent to the sliding surface. This last condition, implies that the time derivative of $\sigma(x)$, evaluated at any point such that $\sigma(x) = 0$, must be zero:

$$\dot{\sigma} = 0 = S\dot{x} = \left(S\left(\alpha(x) f^{-}(x) + (1-\alpha(x)) f^{+}(x)\right)\right)|_{\sigma(x)=0} \tag{2.28}$$

Taking this into account, we have that $\alpha(x) \in [0,1]$ must be such that:

$$\alpha(x) = \left(\frac{Sf^{+}(x)}{Sf^{+}(x) - Sf^{-}(x)}\right)_{|_{\sigma(x)=0}} \tag{2.29}$$

The function $\alpha(x)$ may be seen as the equivalent control, u_{eq}, necessary to keep the system in the sliding surface. With this expression, the time evolution of the system once it has reached the sliding surface, this is, the sliding motion $\dot{x}$, can be described as:

$$\dot{x} = \frac{Sf^{+}(x) f^{-}(x) - Sf^{-}(x) f^{+}(x)}{Sf^{+}(x) - Sf^{-}(x)} \tag{2.30}$$

Accordingly to the above, we have derived the state-space models necessary to carry out the sliding mode analysis of trapped charge dynamics in MOS capacitors using the diffusive representation modeling in Chapter 5. Also, the dynamics of trapped charge has been analyzed using SMC and insensitivity of closed loop response to external disturbances such as ionizing radiation (X-rays, Gamma radiation) has been studied.

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Chapter 3

Dielectric Charge Trapping Controls for MOS Capacitors

The aim of this chapter is to introduce a closed loop control strategy and demonstrate its effectiveness in controlling the charge trapping in MOS capacitors. The chapter has been organized in three main sections. Section 3.1 focuses on the description of charge control method based on Sigma-Delta modulator, the fabrication process and modeling of MOS capacitors. Section 3.2 discusses the experimental results obtained when the first order sigma-delta control is applied to the device. The experimental results have been compared with the predictions from the analytical model described in section 3.1.3 to demonstrate the ability of the proposed method to control charge trapping. Finally, a second order sigma-delta control is discussed in section 3.3. The experimental results obtained demonstrates the advantages of second order control over the first order control.

3.1 Introduction

3.1.1 Sigma-Delta Control

An analog-to-digital converter (ADC) is a system that converts an analog input signal into a digital signal. Sigma-Delta ADC is a popular and well-known class of conversion scheme that has been used extensively for decades [1, 2, 3]. In particular, an oversampling sigma-delta ADC is widely used conversion technique owing its popularity to the factors such as simplicity and robustness in front of circuit imperfections and component mismatch because of the usage of a two-level quantizer. The block diagram of such an ADC is show in Figure 3.1.

Here, the sampler block samples the incoming analog input signal at a rate, f_S, much greater than the typical nyquist rate, f_N, so that the number of reference levels would be reduced to a minimum of two, allowing it to use a simple 1-bit quantizer. The sampled analog signal is sent to the modulator block which converts it into digital representation. A single loop Sigma-Delta modulator is well-suited for such conversion due to its ease of realization. These modulators provide

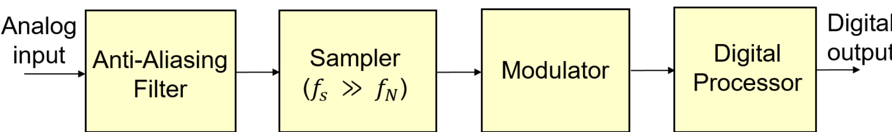

Figure 3.1: Oversampled analog-to-digital converter [4].

quantization noise shaping, which means that the circuit moves the quantization noise out of the frequency band of interest of the analog input. By finally filtering the stream of symbols in the band of interest the quantization noise is removed to a large degree, depending on the oversampling ratio and the order of the converter. Oversampling of the input signal in conjunction with the property of noise shaping [5, 6] allows the circuits with sigma-delta modulation to reach higher resolutions than in the case of other A/D converters, without the use of high-precision components. Moreover, the robustness against circuit imperfections and component matching inaccuracy allows the widespread use of sigma-delta modulators in audio and other signal processing applications [7, 8, 9, 10].

Besides, in the recent years, sigma-delta modulators have been used as a way of implementing Sliding Mode Controllers. The control method based on sigma-delta modulator has been applied in thermal delta-sigma modulators for wind sensors [11, 12], active control of surface potential in chemical sensors [13, 14, 15], and dielectric charge control in MEMS switches [16, 17]. In the case of wind sensing application, the control loop senses the temperature difference (which here is the control parameter) between the sensor temperature and the desired temperature and applies a series of pulses to the heater and maintain it at a desired level thus compensating the convection heat loss of the sensor. Similarly, in MEMS switches, compensation of dielectric charge is obtained by periodically monitoring the net dielectric charge through an indirect measurement and applying the actuation waveforms to maintain it constant. This way it is possible to achieve a closed-loop control of a given variable (such as temperature or dielectric charge) and an implicit analog-to-digital conversion of a given magnitude. The average bitstream generated by the control loop will provide the information about the state of the device. For example, in [11], the output bitstream provides the value of average power injected to the sensor from which the thermal conductance between the hot point and the atmosphere has been evaluated. On the other hand, it has been reported that operating in closed loop configuration enhances the time response of the wind sensors [18], and chemical gas sensors [14].

In this work, a similar control strategy based on sigma-delta modulation has been implemented on MOS capacitors to demonstrate its ability to control the dielectric charge trapping. The next section gives the fabrication details of the capacitors that have been used in this work.

3.1.2 MOS Capacitors - Fabrication Process

The capacitors used for the experiments in this chapter have been fabricated in the clean room at UPC. The capacitors were fabricated on a n-type c-Si ⟨ 100 ⟩ wafer, 280 μm thick and resistivity

of 2.5±0.5 Ωcm.

- The process starts with an RCA clean in order to remove the organic and ionic contaminants.
- This step is followed by a thermal oxidation for 30 minutes with a temperature ramp between 850-1080°C. During this process, a SiO_2 layer of ∼40 nm thick is grown on both sides of the wafer.
- The SiO_2 in the rear side is removed with HF etching while the front side is protected with photoresist.
- Now, a stack consisting of ∼4 nm a-SiC_x(i) (x∼0.1), 15 nm n-doped a-Si and 35 nm a-SiC_x (x∼1) is deposited on the back side of the wafer by PECVD to obtain a good ohmic contact at the back surface.
- Then, a laser doping technique [19] is applied trough this dielectric stack to create localized n^{++} regions with 400 μm pitch.
- After this laser processing step, the bottom side of the sample is ready to be contacted with 480 nm of Ti/Al stack deposited by RF sputtering. A second deposition of Ti/Al is made at the front side to create the upper contact.
- The active device area is delimited by photolithography patterning and wet etching.
- A final annealing in N_2 atmosphere at 400 C for 30 min improves the contacts and the adherence with the c-Si.

Now, Figure 3.2 shows a cross section of the device obtained after following the above fabrication process.

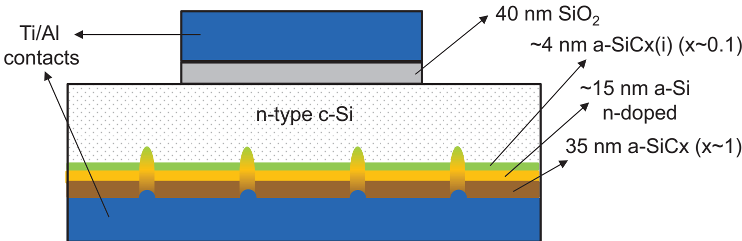

Figure 3.2: Cross section of the MOS capacitor used in the experiments.

3.1.3 Modeling the Device Capacitance

The objective of this section is to model the device capacitance and investigate the effects of dielectric charge trapping on the voltage shifts in the characteristic curves of the device. In general, there are four kinds of charges associated with the $SiO_2 - Si$ systems [20]:

- Mobile ionic charge: These are positive charges present in the oxide bulk primarily due to ionic impurities such as Na^+, K^+.
- Oxide-trapped charge: These are positive or negative charges due to the trapping of holes or electrons in the oxide bulk. Ionization radiation, avalanche injection are some of the mechanisms that result in the formation of these kinds of traps.
- Fixed oxide charge: This is a positive charge located closer to the oxide-semiconductor interface and formed due to structural defects. The density of these charges depend on the oxidation ambient and temperature, and cooling conditions.
- Interface-trapped charge: These can be positive or negative charges formed due to process induced defects, metal impurities and bond-breaking processes (induced by radiation) and are located at the oxide-semiconductor interface. The polarity of these trapped charges depend on the surface potential and usually most of them can be neutralized by low temperature H_2 or H_2/N_2 annealing.

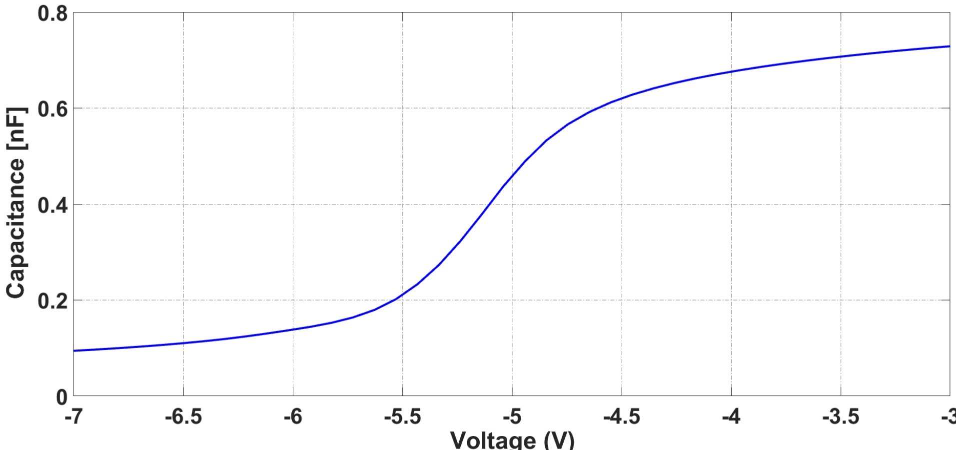

Figure 3.3: Typical CV characteristic curve of a MOS capacitor.

The typical capacitance-voltage (CV) characteristic curve of a MOS capacitor is shown in Figure 3.3. The first three types of charge lead to rigid shift of the CV curve whereas the interface traps results in the stretching of the curves along the gate voltage axis. The model obtained in this work includes the charge accumulated in the oxide bulk and the charge trapped near the $SiO_2 - Si$ interface. For the frequencies that we have used in our experiments, we consider that there is no contribution from interface states to the high frequency capacitance, although some could be present under accumulation and depletion conditions for traps very close to the conduction band (< 0.2 eV) with very high interface state densities [21]. Thus, the capacitance per unit area of the structure C is a series combination of the oxide layer capacitance C_{ox} and the depletion layer-semiconductor

capacitance C_s,

$$C = \frac{C_{ox} C_s}{C_{ox} + C_s} \tag{3.1}$$

where $C_{ox} = \epsilon_{ox}\epsilon_0/d_{ox}$, being ϵ_{ox} and d_{ox} the oxide permittivity and thickness respectively.

An analytical expression of C_s for uniformly-doped silicon and high frequency (HF) conditions is obtained in Chapter 7 of [22] from the equivalent charge density in the semiconductor Q_s. For n-type silicon the latter is,

$$\begin{aligned} Q_s &= \pm\frac{\sqrt{2}\epsilon_s\epsilon_0}{\beta L_D}\sqrt{\frac{n_i^2}{N_D^2}(e^{-\beta\psi_s} + \beta\psi_s - 1) + e^{\beta\psi_s} - \beta\psi_s - 1} \\ &= \pm\frac{\sqrt{2}\epsilon_s\epsilon_0}{\beta L_D} F(\beta\psi_s, \frac{n_i}{N_D}) \end{aligned} \tag{3.2}$$

where n_i and ϵ_s are the intrinsic carrier concentration and the permittivity of silicon, N_D is the donor concentration, $L_D = \sqrt{\epsilon_s\epsilon_0/q\beta N_D}$ is the Debye length, $\beta = q/k_B T$ and ψ_s is the potential, or energy band bending, at the silicon surface.

The semiconductor capacitance can be obtained as,

$$C_s = \frac{dQ_s}{d\psi_s} = \frac{\epsilon_s\epsilon_0}{\sqrt{2}L_D}\left|\frac{\frac{n_i^2}{N_D^2}(1 - e^{-\beta\psi_s}) + e^{\beta\psi_s} - 1}{F(\beta\psi_s, \frac{n_i}{N_D})}\right| \tag{3.3}$$

This implies that ψ_s must be calculated first to obtain C_s.

Now a voltage bias V_G is applied to the gate of the device. The voltage drop across the entire structure must be zero,

$$V_G - \Delta\phi_{ms} - \psi_s - \psi_{ox} = 0 \tag{3.4}$$

where $\Delta\phi_{ms}$ is the work function difference between the metal and the semiconductor and ψ_s and ψ_{ox} are respectively the potential drops along the semiconductor and along the oxide. ψ_{ox} can be calculated as Q_m/C_{ox}, being Q_m the charge density in the metal layer. Additionally, by charge neutrality Q_m must be equal to the charge at the oxide-semiconductor interface and the charge in the semiconductor Q_s. As discussed later in this section, the charge at the oxide-semiconductor interface can be modelled as $Q_{ox} + Q_{it}$, where Q_{ox} is an equivalent oxide charge and Q_{it} is the charge due to interface traps. According to all this, charge neutrality leads to,

$$\psi_{ox} = \frac{Q_m}{C_{ox}} = -\frac{Q_{ox}}{C_{ox}} - \frac{Q_{it}(\psi_s)}{C_{ox}} - \frac{Q_s(\psi_s)}{C_{ox}} \tag{3.5}$$

Note that both Q_{it} and Q_s are functions of the surface potential ψ_s. By substituting (3.5) into (3.4), one can obtain

$$V_G - \Delta\phi_{ms} - \psi_s - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{it}(\psi_s)}{C_{ox}} - \frac{Q_s(\psi_s)}{C_{ox}} = 0 \tag{3.6}$$

The surface potential ψ_s and therefore the total capacitance of the device $C(V_G)$ can be calculated by numerically solving equation (3.6) and then using equations (3.3) and (3.1). Interface traps are

electrically connected with the semiconductor and therefore can be charged or not depending on the surface potential ψ_s. It is well known that interface traps can be acceptor-like (negatively-charges when filled with an electron and neutral when empty) or donor-like (positively-charged when empty and neutral when filled with an electron). Additionally, it is not possible to determine this trap characteristic from the capacitance measured at 2 MHz, where only the variation of the interface-trapped charge Q_{it} coming from both types of traps can be obtained. Then, the simplified model of Q_{it} used in this work assumes that: a) there is a constant trap density D_{it} along the silicon gap, being half of it acceptor-like and half of it donor-like, i.e. $D_{it} = D_{it}^A/2 = D_{it}^D/2$, b) all trap levels below the Fermi level E_f are full and all above E_f are empty. Under these assumptions the expression below is obtained, where N_V and N_C are the valence and conduction levels, respectively.

$$Q_{it}(\psi_s) = D_{it}\left(k_BTln(\frac{n_i}{N_D}) - \frac{1}{2}k_BTln(\frac{N_V}{N_C}) - q\psi_s\right) \tag{3.7}$$

The above analytical model of the device is obtained after the classical theory for Metal-$SiO_2 - Si$ structures [22, 23]. The effects of oxide and interface trapped charges are evaluated by fitting with the results obtained from the experiments. In the next section, description of the charge control scheme used in this work is presented.

3.1.4 Charge Control Method: Sigma-Delta Approach

In this section, the control method based on sigma-delta modulation similar to the one implemented in [11, 16], has been introduced. The discrete-time circuit shown in Figure 3.5 (a) corresponds to a first order 1-bit sigma-delta converter. Note that this circuit is basically composed of an integrator and a quantizer (sign function). In many applications this integrator is not in the electrical domain. It can be in the thermal domain, as in thermal sigma-delta modulators [24], or in the mechanical domain, as in the case of some force feedback accelerometers [25].

Now, this control method has been implemented to control the charge trapped in the oxide layer of MOS capacitors. This can be achieved by periodically monitoring the horizontal displacement of the CV characteristic of the device and applying the adequate voltage waveforms to maintain it at a desired position. Figure 3.7 shows the closed loop circuit designed for this purpose. It is a sampled circuit which monitors the capacitance at a reference voltage in periodic sampling intervals, nT_S, and evaluates this control parameter using a negative feedback loop to maintain it around a fixed threshold value. In our case, the actual magnitude to control is the total charge in the dielectric layer of a MOS capacitor, which is indirectly sensed by observing the horizontal displacement of the CV curve or in other words, voltage shift.

Figure 3.4 illustrates this idea, where C_2 and C_3 represent the shifted versions of the original CV curve C_1 due to the accumulation of trapped charges. The detection of whether the CV lies to the right or to the left of its desired position can be achieved by observing the value of the capacitance at a constant voltage of interest, $C_1[V_1]$.

The objective of the control is to shift the CV curve of the device so that the value of the capacitance at the voltage reference V_1 is C_{th}, i.e., $C[V_1](t) \approx C_{\text{th}}$. To this effect an adequate

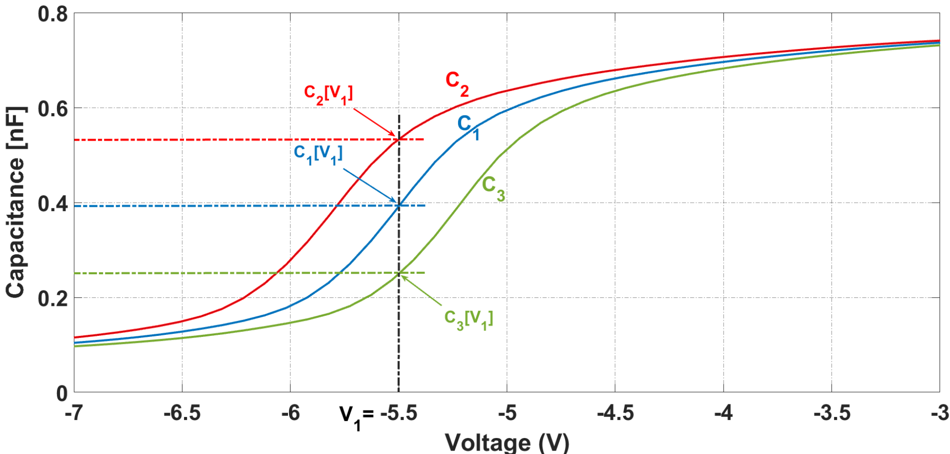

Figure 3.4: Illustration of the working of control method. If $C_1[V_1]$ represents the target capacitance at the voltage of interest, the control loop applies adequate voltage waveforms to shift the CV curves to left ($C_2[V_1]$) or to right ($C_3[V_1]$) around the target capacitance. The CV displacements are intentionally enlarged for the purpose of demonstration.

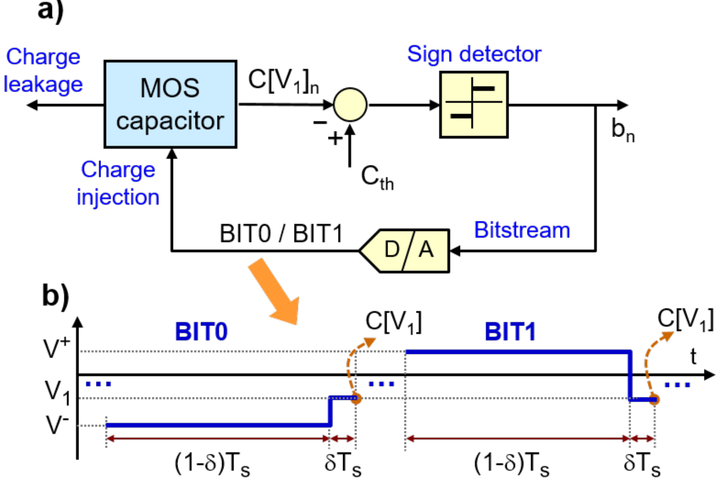

Figure 3.5: a) Control feedback loop for CV control. The device capacitance is measured periodically at voltage V_1 and compared with a threshold value, C_{th}. Depending on the result, either a BIT1 or BIT0 waveform is applied during the next sampling period. b) BIT0 and BIT1 voltage waveforms. The sampling period is T_S and V_1 is applied for a short time δT_S in each waveform. The capacitance measurement is taken at the end of each V_1 application.

sequence of voltage waveforms are being applied by the feedback loop to the device. The voltage waveforms, also named as BIT0 and BIT1 waveforms, should be designed in order to obtain two

separate results:

- The applied waveforms must allow periodical monitoring of $C[V_1](t)$ at times $t = nT_S$. In order to have such periodic measurements at a fixed reference voltage at each sampling interval, it is necessary to switch the voltage levels during the sampling period. The designed voltage waveforms can be seen in Fig. 3.5 (b). In both cases the waveform ends with a segment of time of duration δT_S, during which V_1 is applied to the device to be able to monitor the relative position of the C-V curve, with regard to the desired position, i.e., make the comparison between $C[V_1]_n = C[V_1](nT_S)$ and C_{th}.
- The chosen voltage levels must apply the correct excitation to shift the CV in the adequate direction. In this regard, the actuation voltages, $\{V^+, V^-\}$, which are being applied during $(1-\delta)T_S$, are chosen so that they generate horizontal shifts of the CV of different sign: if $C[V_1]_n < C_{th}$ a BIT1 is applied during the next clock cycle, and a BIT0 otherwise (see Fig. 3.5). Accordingly the following control law has been defined:

$$\text{Next symbol} = \begin{cases} \text{BIT0}, & \text{if } C[V_1](nT_S) > C_{th} \\ \text{BIT1}, & \text{otherwise} \end{cases} \tag{3.8}$$

Now the implementation of the charge control method can be described in the form of the following flowchart:

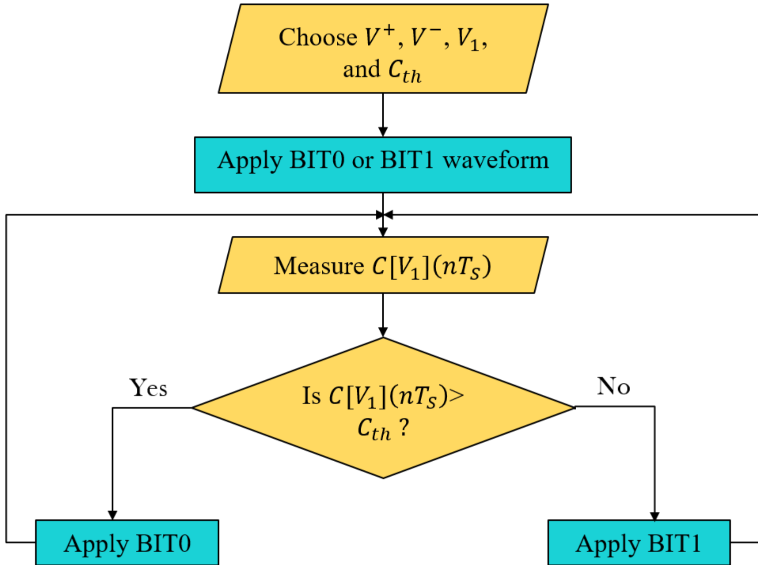

Figure 3.6: Flowchart description of the control method.

The comparison between $C[V_1]_n$ and C_{th} at the end of each sampling period, nT_S, generates a bitstream at the output of the modulator, $b_n = sgn(C_{\text{th}} - C[V_1]_n)$. Averaging of these bits over

a period of time provides the average voltage required to maintain the desired charge level in the dielectric. From this signal it is possible to obtain real time information of the charging dynamics in the dielectric of the device.

In order to analyze the charge dynamics involved with the proposed control method (see Chapter 5), it would be convenient to establish a link to a first-order sigma-delta modulator, as shown in Figure 3.7. Considering a constant input, β, to the system, the output of the modulator, y_n, is a bit stream obtained by quantizing the accumated or integrated sum of the error signals over each sampling period, T_S. Since the quantizer is a two-level comparator, the output will be either 1 or -1. The main objective of the modulator is to minimize the difference between the integrated modulator ouput and the integrated input. This can be expressed in the form of a typical equation of Sigma-Delta modulator [4] as

$$u_{n+1} = u_n - \beta + y_n \tag{3.9}$$

Comparing the charge control circuit, see Figure 3.5, with the 1st order sigma-delta modulator,

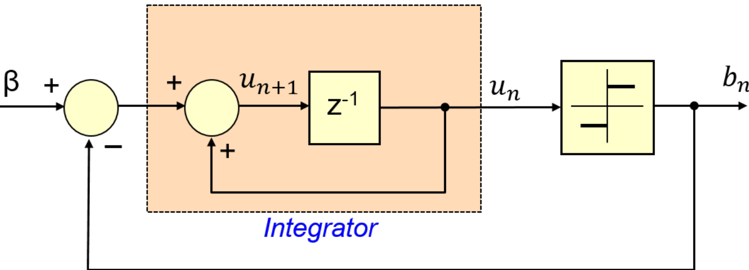

Figure 3.7: First order sigma-delta modulator [11].

we can notice that the function of integration in our control method is performed by the dielectric layer, which is considered to be a reservoir of charge. Since the control parameter is the capacitance at the reference voltage, $C[V_1]$, which is an indirect measurement of the net dielectric charge, the input to the quantizer can be seen as difference between the target charge and the net charge in the dielectric. And this net charge in the dielectric at the end of each sampling interval is the sum of the previously stored charge and the integral over the sampling period of two charge contributions: charge injection and charge leak. Thus the control method maintains the net charge around a fixed value and generates an average bitstream, $\bar{b}$, such that the balance between charge leak and charge injection, given by β, fixes the net charge around the desired target value.

$$\beta = \bar{b} = \lim_{N\to\infty} \frac{1}{N} \sum_{n=1}^{N-1} b_n \tag{3.10}$$

The steady-state average bitstream corresponds to a stable level of dielectric charge, therefore the amount of trapped charge in the dielectric can be inferred from the average of the output bitstream given by $\bar{b}$. Any change in the desired level of charge (or in other words, C_{th}) results in a change

in the average bitstream thus we obtain a unique relation between $\bar{b}$ vs C_{th}.

In the next section, a set of experiments have been performed on a MOS capacitor, described in Section 3.1.2, in order to validate the control method discussed in this section.

3.2 First Order Sigma-Delta Control

In this section the first order sigma-delta control described in the previous section has been implemented as a tool to provide a sliding mode control of net trapped charge [26, 17]. To this effect, a long experiment has been planned with the control being applied on a MOS capacitor for different target capacitances.

3.2.1 Experimental Setup

The experimental setup used to implement the control strategy, described in section 3.1.4, is depicted in Figure 3.8. A Keysight E4980A LCR meter, controlled from a computer, periodically measures the capacitance and applies the voltage waveforms at each sampling interval according to the control law 3.8. The control parameters must be chosen so that the continuous application of BIT0 waveforms must generate shifts of different sign to the continuous application of BIT1 waveforms. So the voltage levels for BITx waveforms are selected such that $V^- = -3V$, and $V^+ = 6V$ generate, respectively, shift to the right and to the left of the CV curve of our device. The value $V_1 = -4.5V$ gives good sensitivity to sense the displacements of the CV curve produced during the experiments. The sampling period has been chosen to be $T_S = 350$ms with $\delta = 1/3$.

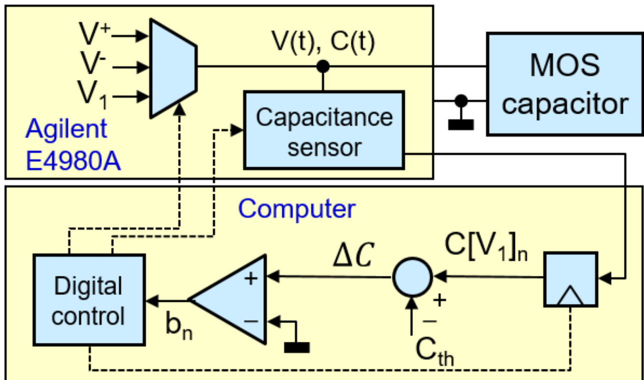

Figure 3.8: Implementation of the charge control method. The LCR meter monitors the capacitance,$C(t)$, and decides to apply either the symbol BIT0 or BIT1 from the comparison between $C(t)$ and C_{th}.

3.2.2 Results and Discussion

The experiment consists of applying the control method on the capacitor for 16h with 8 different target capacitances, each one lasting for 2 hours (see Table 3.2).

Figure 3.9 shows the evolution as a function of time of the capacitance measured at the end of each clock cycle, $C[V_1]_n$. At the beginning of each interval a transient can be observed in which the measured capacitance either increases or decreases till the target threshold value is reached. During this transient period, a continuous sequence of BITx waveforms is being applied. Once the desired value has been reached, the feedback loop applies the excitation required to keep it constant.

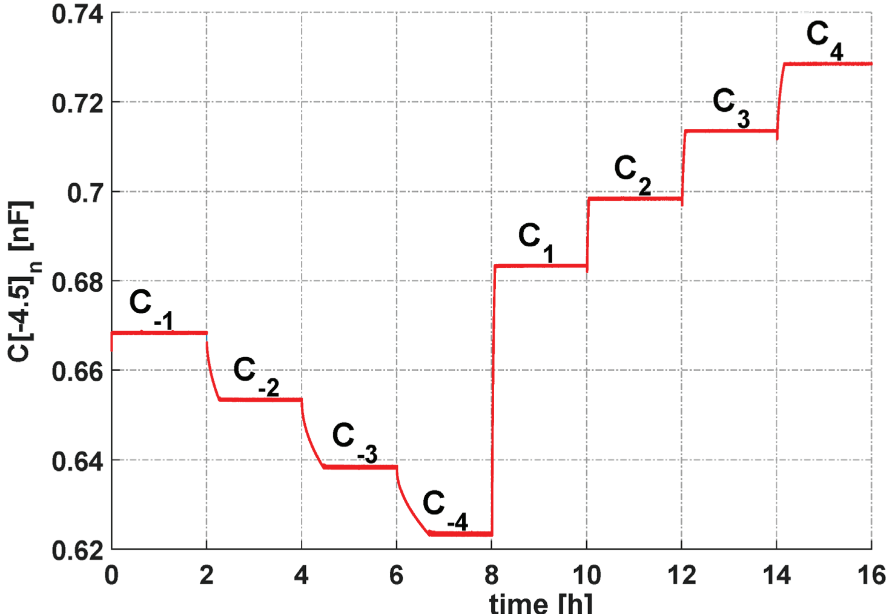

Figure 3.9: Time evolution of $C[V_1]_n$ during the experiment. For each C_i segment this value is almost constant and matches its corresponding target value, C_{th}. $V_1 = -4.5V$.

A zoom of the evolution of the capacitance measured at V_1 can be observed in Figure 3.10. As it can be seen, each time the capacitance is below the desired threshold value (C_{th}=0.6231nF for segment C_{-4}) the feedback loop applies a BIT1, and in this case it takes between 3 and 4 consecutive BIT0s to take it down again below the threshold. This is compatible with the standard behaviour of first-order sigma-delta modulators [16]. The CV characteristics of the device at the end of each 2-hour controlling segments (C_i) are depicted in Figure 3.11. We can observe that by choosing different target values and applying the control method, it is possible to shift the CV curve horizontally and maintain it around a desired operating point. The corresponding values of the voltage shift, measured at 0.4nF of device capacitance, are listed in Table I.

The average bitstream generated by the feedback loop during the experiment is shown in Figure 3.12. As it can be observed, it is necessary to inject more BIT0 waveforms (the average bitstream

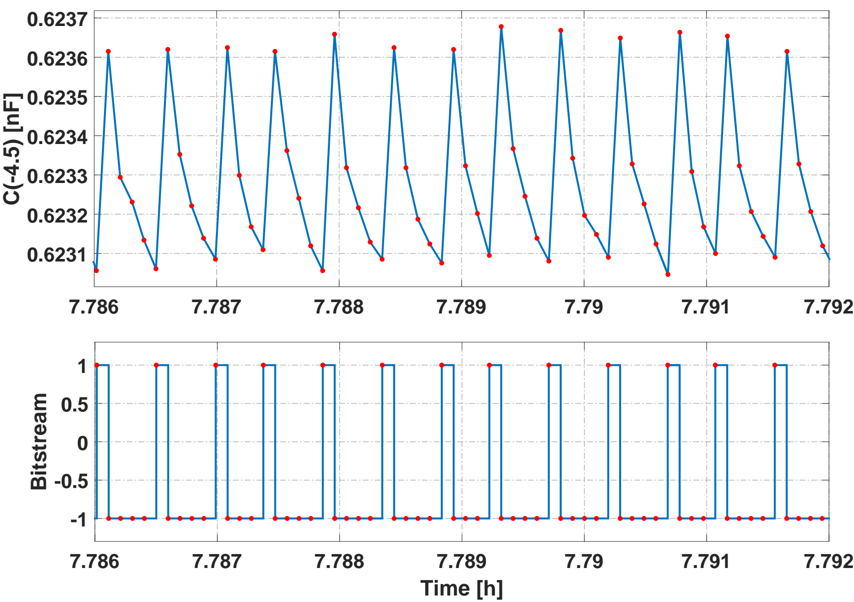

Figure 3.10: Top: Zoom of $C[V_1](nT_S)$ for a short time within segment C_{-4}. Bottom: sequence of bits applied during this time.

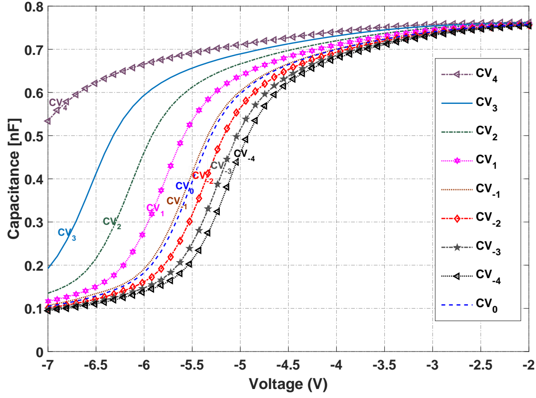

Figure 3.11: C-V curves obtained at the end of each C_i segment. For each CV_i curve shown, it is $C(-4.5V) \approx C_{\mathrm{th}i}$, as defined in Table 3.2.

C_i	Time [h]	$V_{\mathrm{sh}}(0.4nF)$ $[mV]$
C_0	$t < 0$	0 (Initial Value)
C_{-1}	$t \in [0, 2]$	-36
C_{-2}	$t \in [2, 4]$	135
C_{-3}	$t \in [4, 6]$	275
C_{-4}	$t \in [6, 8]$	384
C_1	$t \in [8, 10]$	-288
C_2	$t \in [10, 12]$	-624
C_3	$t \in [12, 14]$	-1034
C_4	$t \in [14, 16]$	—

Table 3.2: C_{th} values used during the experiment. Voltage shifts of the obtained C-V curves measured at $0.4nF$.

decreases) to achieve lower C_{th} values. On the other hand, increasing the average number of BIT1 waveforms generates higher values of $C[V_1]$.

Each time a new target value is applied the control saturates i.e it applies a continuous sequence of either BIT0 or BIT1 waveforms till the new C_{th} value is reached. Once in this range, the average bitstream follows a slow time evolution, which has also been observed in previous works [17].

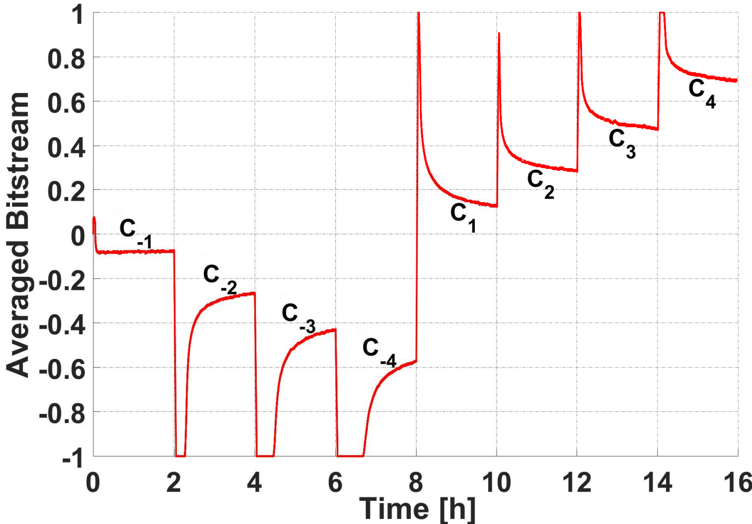

Figure 3.12: Average bitstream obtained during the experiment. Each time the target capacitance, C_{th}, is changed the bitstream saturates till such target value is reached. Increasing the average number of BIT1 waveforms allows to increase the value $C[V_1]$, hence displacing the C-V to the left.

A distinctive feature of sigma-delta modulators is the power spectrum density of the generated bitstream. For the first order case it is known that the quantization noise presents a zero at $0Hz$ and the slope is approximately $20dB/dec$ (see Fig. 3.13).

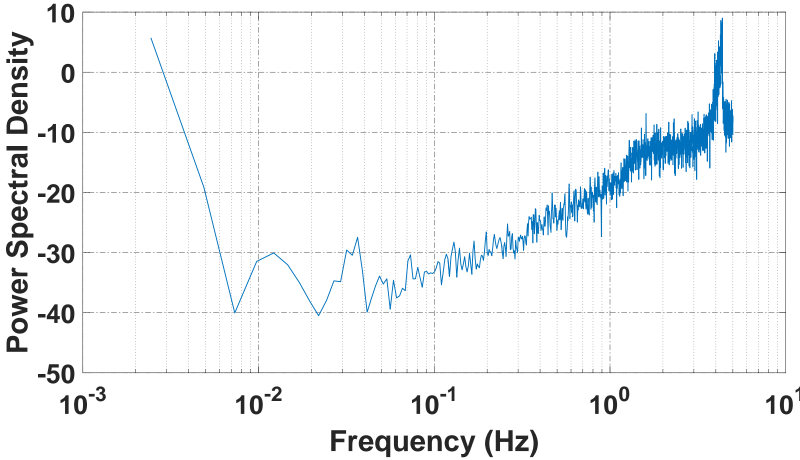

Figure 3.13: Power spectral density obtained from the C_1 step of the experiment (between t=8h and t=10h). Total number of bits of the sequence: 16312.

3.2.3 Simulations versus Experimental Data

Fittings of the experimental CV curves reported in Figure 3.11 with the analytical model described above have been performed, taking Q_{ox} and D_{it} as parameters. The results are shown in Figure 3.14. In good agreement with theory, these results indicate that the horizontal-rigid CV shifts correspond to variations of the charge trapped in the oxide Q_{ox}. Moreover, both the mobile ionic charge and the fixed oxide charge components of Q_{ox} depend on the fabrication process and they can hardly vary during the experiments. Then it can be concluded that such CV shifts correspond to positive and negative variations of the charge trapped in the bulk of the oxide, being the total oxide charge positive in the cases reported.

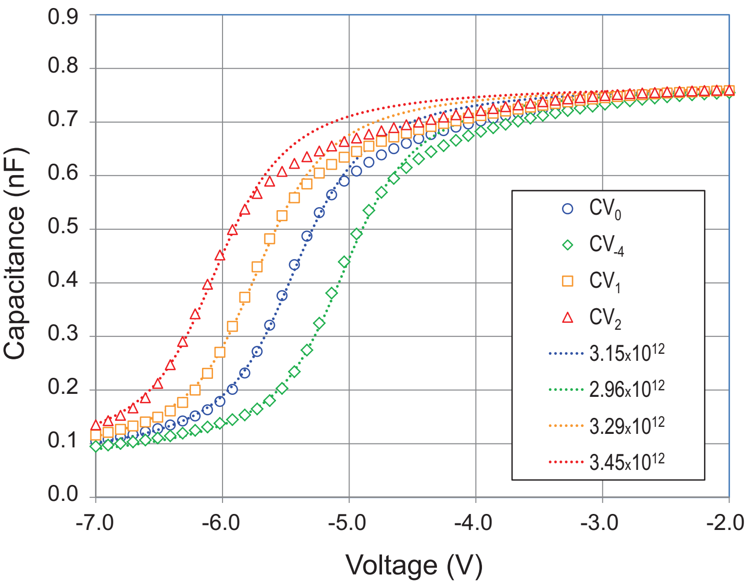

Figure 3.14: Comparison between experimental CV curves (ticks) and simulation results of the reference device (dashed lines). The value of Q_{ox} used in each simulation is given in cm^{-2}. An interface trap density D_{it}=1.55×10^{12}cm^{-2}eV^{-1} was used in all simulations.

Additionally, the charge trapped in the interface Q_{it} can be either positive or negative depending on the surface potential, thus on the gate voltage, V_G. This produces opposite shift in the accumulation and depletion sections within the same C-V curve, a phenomenon known as CV stretch-out [22]. This phenomenon may also explain the CV stretching observed for the CV$_4$ case in Figure 3.11. In Figure 3.14 a small discrepancy between simulation and experimental results is seen in the accumulation section. However, this discrepancy is due to the simplified model used, which assumes a constant D_{it}. This is a rough approach, since in practice D_{it} can exhibit noticeable variation along the band gap [27] and, as mentioned before, some response could be related to interface traps close to the conduction band edge [21].

3.3 Second Order Sigma-Delta Control

3.3.1 Charge Control Method

In the previous sections, a first order control of charge trapping for MOS capacitors based on sigma-delta modulators has been implemented. The control allows to obtain a desired shift of the CV characteristic of the device (and hence of the net trapped charge in the oxide) and then to maintain it by the application of a proper sequence of bipolar voltage waveforms. However, one of the known problems of first order sigma-delta modulators is the appearance of plateaus [10], conventionally known to be Devil's staircase.

The occurance of this non-linear effect is associated with leaky integrators, usually finite-gain op-amps in practical realizations of a modulator. This devil's staircase behavior has been observed in the case of systems such as MEMS oscillators [28], Capacitive MEMS devices [16, 29, 30], gas sensors [31] where control strategy based on 1st order sigma-delta modulator is implemented. In these devices, the dielectric layer, which is considered to be a reservoir of charge, works as a leaky charge integrator and the sampling time, T_S, associated with this integrator can be seen as an analog to the leakage parameter. If the sampling time is of the same order or greater than the shortest time constant of the charging and discharging processes of the device, the control may provide a constant output during certain time intervals in which the system is effectively in an open loop configuration. It must be noted that the charging and discharging time constants will depend on the applied voltages in a non-linear way and that several processes may coexist in a single device, resulting in a complex dynamics that is generally difficult to predict beforehand.

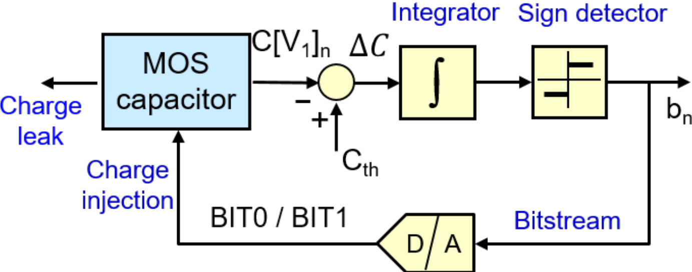

Figure 3.15: a) Block diagram of the second order sigma-delta control circuit of charge trapping. b) Experimental implementation of the second order control.

Now, a second order sigma-delta control method is introduced in order to control the charge trapping in MOS capacitors. Figure 3.15 shows the double loop sigma-delta modulator with two integrators and two feedback loops. The objective of this section is to present a second order control of charge trapping for MOS capacitors. This topology effectively removes the presence of plateaus in the experimental measurements.

The block diagram of the second order control circuit proposed is shown in Figure 3.15. The main difference compared to the first-order topology is the use of an integrator before the sign

detector. The error signal,, obtained at the end of each sampling interval, T_S, is integrated numerically and the sign of the result decides the actuation BITx waveform to be applied in the next sampling period. The addition of an integrator element will result in a second order zero in the quantization noise at the output of the modulator, and also in the disappearance of the unwanted plateaus [29, 32].

3.3.2 Fabrication Process

The processing steps followed to fabricate the capacitors used for these experiments are described:

- The process starts with an RCA clean in order to remove the organic and ionic contaminants.
- This step is followed by a thermal oxidation for 45 minutes with a temperature ramp between 850-1080°C. During this process, a SiO_2 layer of ∼25 nm thick is grown on both sides of the wafer.
- Next, the SiO_2 in the back side is removed with HF etching, while the front side is protected with photoresist.
- Then, aluminum is deposited at the back side of the wafer by evaporation, resulting in a layer thickness of approximately 700 nm. Later, a laser doping technique is applied.
- Finally, the top electrode is conformed via a sputtering deposition of aluminum using a shadow mask for patterning.

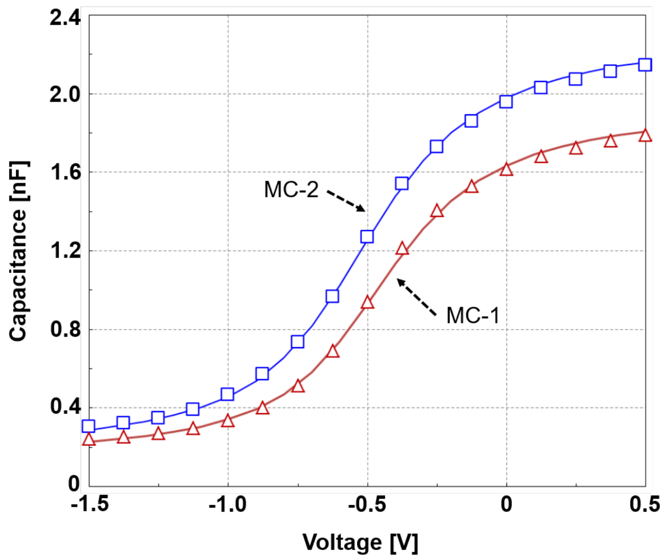

Figure 3.16: Measured (ticks) and fitted (solid lines) CV curves for the capacitors MC-1 and MC-2. The fitting has been done using the model described in section 3.1.3.

3.3.3 Results and Discussion

Two sets of MOS capacitor devices used here, named as MC-1 and MC-2, from the same fabrication batch have been used. The CV characteristics of the devices have been shown in Figure 3.16.

An initial set of experiments have been performed in order to evaluate the effectiveness of the sigma-delta control method using devices MC-1 and MC-2. The parameter values chosen for BIT0 and BIT1 waveforms are reported in Table 3.3. .

Table 3.3: Parameter values used in BIT0 and BIT1 waveforms.

Device	V^+	V^-	V_1	T_S	δ
$MC-1$	$5V$	$-1V$	$-0.5V$	$350mS$	$1/3$
$MC-2$	$6V$	$-1V$	$-0.5V$	$350mS$	$1/3$

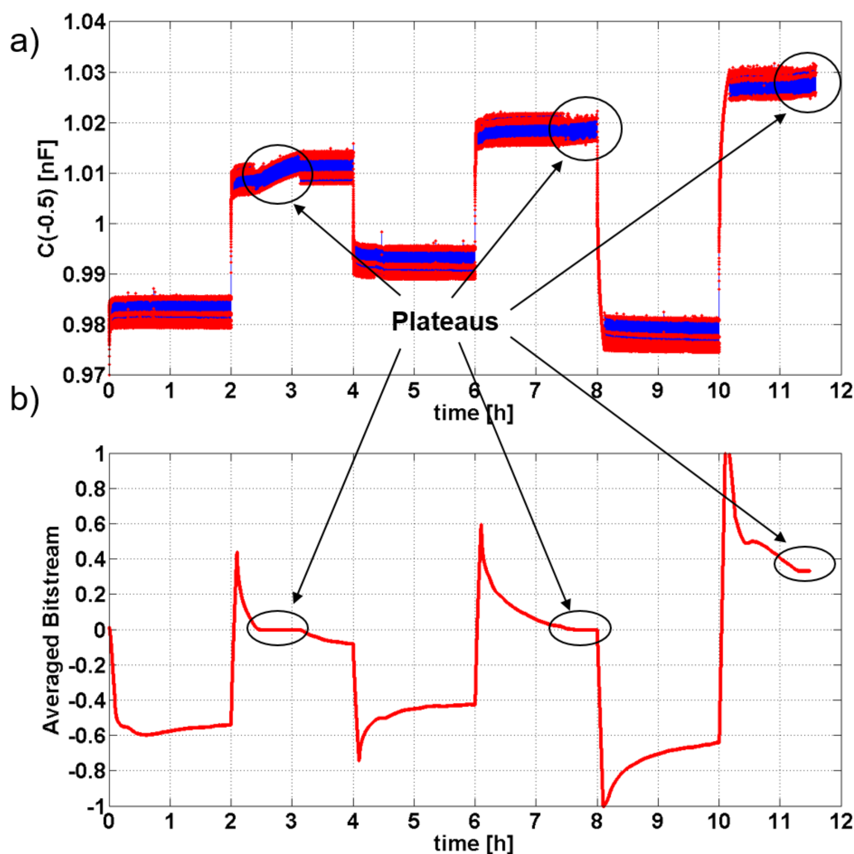

Figure 3.17: First order sigma-delta control applied to MC-1 to obtain a sequence of six target capacitances. a) Device capacitance measured during the experiment. b) Averaged bit stream provided by the control loop. Circles denote time intervals in which the control is in a plateau.

In a first experiment, first order sigma-delta control was applied to device MC-1 to achieve a sequence of six target capacitances, $C_{th} = \{0.98, 1.01, 0.99, 1.02, 0.975, 1.03nF\}$. Each target-step lasted for 2 hours. From the results of this experiment, shown in Figure 3.17, it can be seen that the control method allows to reach the desired target levels and maintain them. For example, at $t = 4h$ more BIT0s (V^- dominant) are being applied by the control forcing the C-V to shift to the right and thus decreasing $C[V_1](t)$ until the target, $C_{th} = 0.99nF$, is reached. From then until $t = 6h$, the bit stream keeps the capacitance successfully around this target value.

However, plateau-associated phenomena can be observed in three different time intervals highlighted with a circle in Figure 3.17. When the control becomes trapped in a plateau, it provides constant bit stream output, and the observed variable, $C[V_1](t)$, is in fact left uncontrolled and exhibits open-loop behaviour. The time length of such control-locking effect is unpredictable, therefore plateaus must be avoided when possible.

The aim of the next set of experiments is to investigate the eventual improvements provided by the second order sigma-delta control when applied to devices that exhibit fast charging dynamics. Figure 3.18 shows the results of an experiment when a first order and a second order sigma-delta controls have been applied to device MC-1 with four target levels, $C_{th} = \{0.95, 0.935, 0.96, 0.925nF\}$, in $3h$ steps. A plateau has been detected in case of a first order sigma-delta control, which implies that control was lost for approximately 145 minutes, whereas in case of second order sigma-delta control, there has been no sign of plateau during the control.

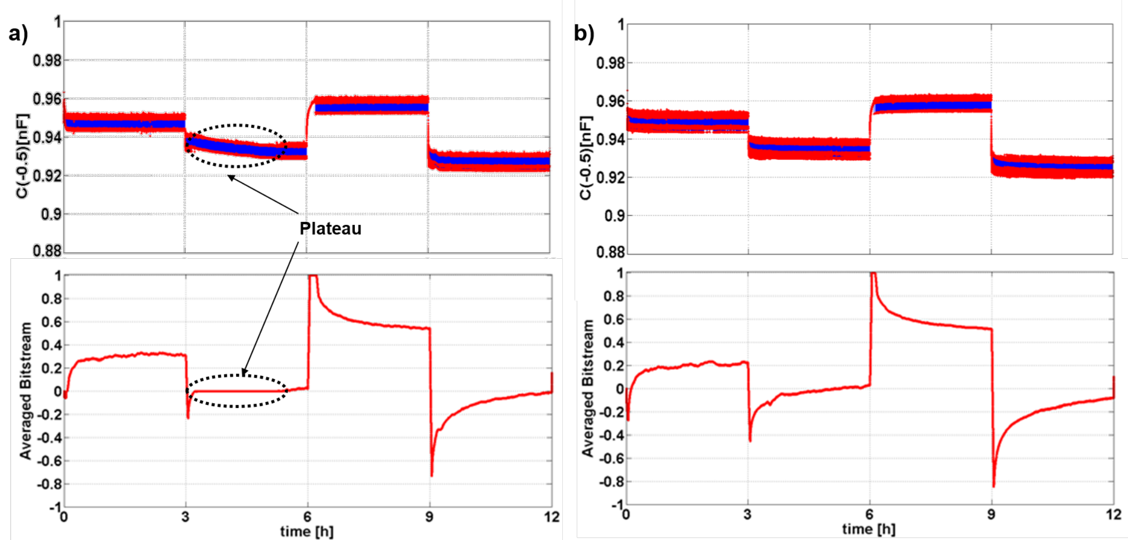

Figure 3.18: Results of (a) 1st order and (b) 2nd order sigma-delta controls applied to MC-1 to obtain a sequence of four target capacitances. The circle denotes an interval in which the control is in a plateau.

Figure 3.19, taken from experimental data, illustrates how first and second order controls do work. In the first order case, the behaviour of the capacitance and of the bit stream are

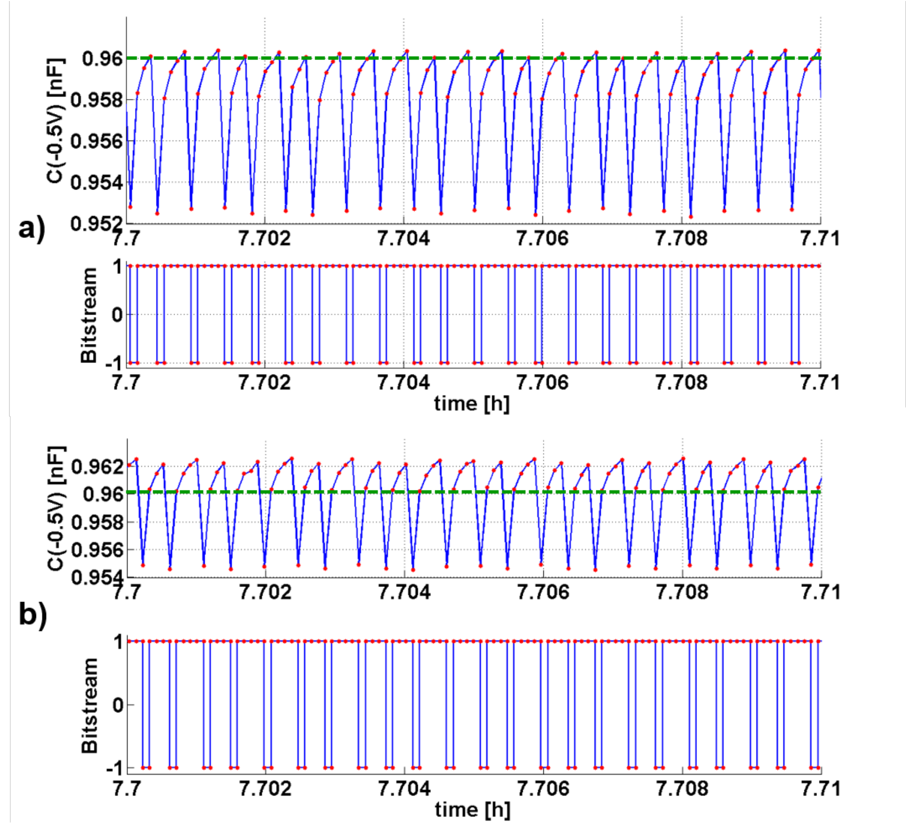

Figure 3.19: Sampled capacitance and bit stream taken from the experiment of 3.18(a) and from the experiment of 3.18(b), both in the $C_{th} = 0.96nF$ time step.

straightforward related: the next BIT changes each time $C[V_1]$ exceeds C_{th}. However, in case of second order controller, the presence of the integrator makes this relationship not so easy to see, but the behaviour obtained fully agrees with the sigma-delta modulator theory [33] and with the experiments reported in [30].

Figure 3.20 compares the spectral power densities of the bit streams obtained from two experiments in which MC-2 was set to C_{th} = 1.33 nF for 16 hours using both first and second order controls. The presence of the additional integrator in the 2nd order method produces noticeable differences. The noise at low frequencies becomes considerably reduced and the slope of the quantization noise rolled out of the band of interest increases in the 2nd order case.

3.4 Conclusions

A new CV control for MOS capacitors has been implemented. The proposed method, based on sigma-delta modulation, allows to horizontally displace the CV characteristic of the device and

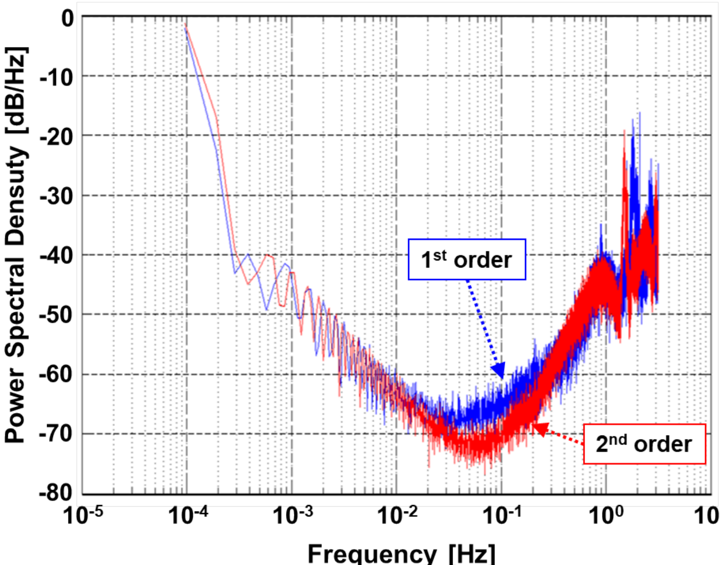

Figure 3.20: Power spectral density estimation, obtained using Welch's method in MatLab after 105 samples of the control bit stream. First and second order controls were applied to device MC-2 for 16 hours to obtain the same target capacitance, $C_{th} = 1.33$ nF.

maintain it at a desired point so that the net charge trapped in the dielectric layer remains constant. The control capability relies on the complementary sign of the shift generated by voltages of different polarity, in what is a sliding mode control. Several analysis and experiments have been undertaken to explain how the changes in the CV can be related to charge trapping in the bulk of the oxide layer and in the silicon-oxide interface, and how charge trapped can be sensed and actuated. A second order method of dielectric charging control for MOS capacitors has also been presented and checked experimentally. The main advantages being that the quantization noise shaping is second order and that the typical plateaus of first order sigma-delta controllers can be avoided. These control strategies can be seen as a promising way of improving the reliability of MOS structures.

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Chapter 4

Compensation of Charge Induced by Radiation in MOS Capacitors

Radiation, in general, is the emission or transmission of energy in the form of waves or particles through space or through a material medium. Depending on the energy carried by the radiating particles, radiation is often categorized as either non-ionizing or ionizing. Non-ionizing radiation is a low frequency electromagnetic radiation that does not carry enough energy (often less than $10eV$) to ionize atoms or molecules, while ionizing radiation has high frequency and carries enough energy to detach electrons and ionize atoms or molecules. Exposure to ionizing radiation could be detrimental to electronic systems in the sense that it alters the electrical properties of active components and results in the degradation of circuit performance and even circuit failure. Hence, a good understanding of the physical mechanisms underlying the response of the devices to radiation is essential in order to improve the tolerance of the electronic circuits and develop radiation hardened circuits.

Charge trapping induced by ionizing radiation in semiconductor devices represents a major reliability issue in many applications [1, 2, 3]. Most of the modern integrated circuits (ICs) employ insulators and oxides as key components and exposure to ionizing radiation results in the buildup of trapped charge, often leading to device degradation and failure [4, 5]. Under the influence of high energy ionizing radiation, these devices suffer from a drift in the threshold voltage, an increase of the leakage current, and a decrease of the transconductance [6, 7]. This results in a degraded performance thereby increasing the failure rate of the device operation [8, 9, 10, 11].

Over the past 40 years, the effects of total ionizing dose on radiation-induced trapped charge buildup in MOS devices have been investigated [12, 13].

However, most works related to reducing the effects of charge trapping focus on the design and characterization of materials and structures. Alternatively, it is equally important to develop some active control techniques such as proposed in [14, 15] to improve the radiation response of the devices. This control method, based on sliding control [16], effectively compensates the dielectric

charge induced by ionizing radiation by the application of bipolar actuation voltage waveforms.

Now, the objective of this chapter is to explore the capability of a charge trapping control loop to improve the radiation response of MOS capacitors made of SiO_2 and Al_2O_3 dielectrics by compensating the oxide-trap charge induced by ionizing radiation. To this effect, two sets of devices made with silicon dioxide and alumina have been irradiated with gamma radiation and X-rays respectively. Each set has two capacitors exposed to irradiation, one operating at constant voltage bias while the other working under a dielectric charge control. The experiments show substantial charge trapping in the uncontrolled device whereas, at the same time, the control loop is able to compensate the charge induced by ionizing radiation in the second device.

4.1 Charge Trapping Control under Ionizing Radiation

The objective of this section is to introduce the closed-loop control strategies that can effectively cope with charge induced by ionizing radiation. The charge control circuit shown in Figure 4.1 corresponds to a first order sigma-delta converter, as discussed in Chapter 3. The dielectric in the MOS capacitor can be seen as a reservoir of trapped charge which is continuously being filled/emptied by three different contributions:

- the trapped charge injected/extracted by the applied voltage actuation,
- the trapped charge being leaked out, and
- the trapped charge generated by ionizing radiation.

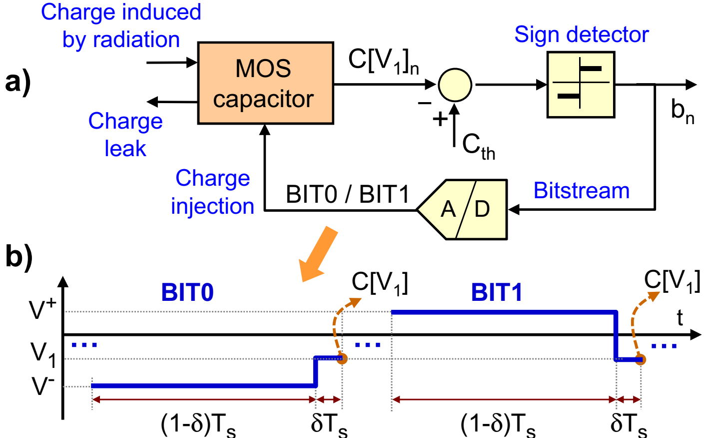

Figure 4.1: (a) Sigma-Delta feedback loop implemented on device under irradiation. The device capacitance at voltage V_1 is measured periodically and compared with C_{th}. Depending on the result, either a BIT1 or BIT0 waveform is applied during the next sampling period. (b) BIT0 and BIT1 waveforms. Capacitance measurements are taken at the end of each V_1 application.

All three contributions will depend on the instantaneous applied electric field and on the state of the trapped charge, among other parameters. The generated control signal, composed of a sequence of voltage waveforms tries in average to inject the necessary charge into the dielectric to keep the total net charge constant. Since the net trapped charge is a hidden variable it is indirectly obtained by keeping track of the capacitance of the device measured at a constant reference voltage, V_1, chosen beforehand.

The aim of the control is therefore to keep this value constant, and at a desired level C_{th}. Any displacement or stretching of the C-V curve due to radiation will generate unwanted shifts in this capacitance. This is perceived by the control loop as a deviation from the target value for the capacitance, and therefore it tries to generate the adequate compensation in the next sampling period.

4.2 Experimental

This section presents the control experiments performed on MOS capacitors to observe how dielectric charge induced by ionizing radiation such as gamma radiation and X-rays could be effectively compensated by a charge control strategies based on sigma-delta modulation. To this effect, two sets of devices have been fabricated. The first set of capacitors (Set-1) have SiO_2 as dielectric layer and is used for gamma irradiation experiments, whereas the second set of devices (Set-2) with Al_2O_3 as dielectric is irradiated with X-rays. The fabrication details of the capacitors used for the radiation experiments are described in the next section.

4.2.1 Device Fabrication Process

Set-1

The capacitors (SiO_2 devices) used for gamma irradiation experiments were fabricated in the clean room at UPC. The steps followed during the fabrication process are:

- The process starts with an RCA clean in order to remove the organic and ionic contaminants.
- This step is followed by a thermal oxidation for 30 minutes with a temperature ramp between 850-1080°C. During this process, a $\mathrm{SiO_2}$ layer of ∼40 nm thick is grown on both sides of the wafer.
- The $\mathrm{SiO_2}$ in the rear side is etched with hydrofluoric acid (HF) while the front side is protected with photoresist.
- Now, to form the upper contact, a stack of Ti/Al is deposited by RF sputtering with a thickness of 480 nm on the front side of the wafer.
- The active device area is patterned by photolithography and wet etching.
- The next step is to deposit a stack of Ti/Al with a thickness of 540 nm on the rear side of the wafer by RF sputtering.

- A final annealing in N_2 atmosphere at 400ºC for 30 min is performed to reduce the resistance and improve the adherence with the c-Si.

The cross section of the devices is shown in Fig. 4.2.

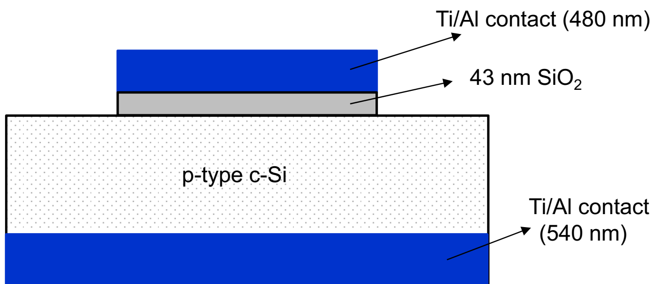

Figure 4.2: Cross section of SiO_2 MOS capacitors.

Set-2

The capacitors (Al_2O_3 devices) used in the X-ray experiments are fabricated at UPC. They have been fabricated on a p-type c-Si ⟨ 100 ⟩ wafer, 280 μm thick and resistivity of 2.5±0.5 Ωcm.

- The process starts with an RCA clean in order to remove the organic and ionic contaminants.
- This step is followed by a thermal atomic layer deposition of Al_2O_3 at 200°C. During this process, an oxide layer of ∼40 nm thick is grown on both sides of the wafer.
- The front side of the wafer is covered with photoresist and then the Al_2O_3 layer on the rear side is etched using HF solution.
- Now, a 700 nm thick Al layer is evaporated on top of the Al_2O_3 layer.
- Next, photolithography is used to pattern the capacitors and the unwanted Al and Al_2O_3 are removed with isopropyl and phosphoric acid solution.
- Then the rear side of the wafer is covered with Al evaporated by electron beam to form the back contact.
- A final annealing in N_2 atmosphere at 350ºC is performed to reduce the resistance and improve the adherence with the c-Si.

The schematic view of vertical cross section of the device is shown in Fig. 4.2.

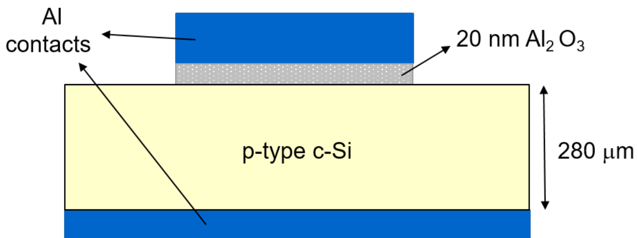

Figure 4.3: Cross section of Al_2O_3 MOS capacitors.

4.2.2 Experimental Setup

The gamma irradiation tests have been performed at the ESTEC ^{60}Co Facility [17], exposing the devices to the rays emitted from a 2000 Ci Co-60 gamma source. The test setup is shown in Figure 4.4.

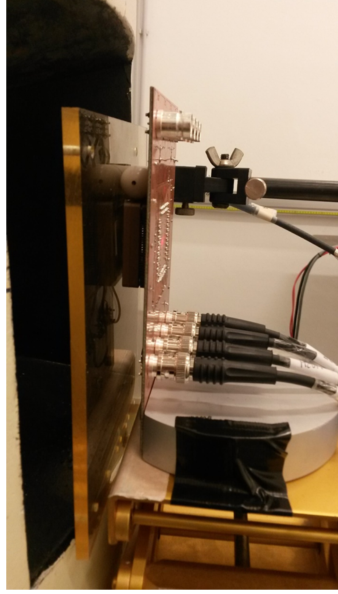

Figure 4.4: Test setup: The PCB containing DUTs are placed in vertical position in front of the radiation source using vertical supports provided by the facility.

The Co-60 has an half-life of 5.25 years, Co-60 decays by beta decay to Ni-60. The activated Ni nucleus emits two photons with energies of 1.173MeV and 1.332 MeV photons and its activity was 76.7 TBq at the time of testing. The source is stored in its own special housing, built of steel with integral lead shielding. When the source is raised to the irradiation position, the gamma beam produced by the Co-60 decay exits the irradiation unit through a collimator window into

the radiation cell. The setup has been positioned at a distance corresponding to a dose rate of 1.1 Krad/h. Real time dosimetry has been performed using a 2670 Farmer Dosimeter equipped with a 2571 Farmer 0.6 cc air Ionisation Chamber, the associated uncertainty is 4.4% to the dose rate measurement. The methods for the determination of the Total Ionizing Dose (TID) and the Dose Rate (DR) used in the laboratory have been accredited against ISO-17025 standard.

On the other hand, the X-Ray experiments have been performed at the Radiation Physics Laboratory of University of Santiago de Compostela. The PCB (Printed Circuit Board) containing the packaged devices is placed facing the radiation source. The capacitors under test are irradiated by a 50 kV X-Ray beam delivered by an Oxford Instruments Neptune tube. The beam output has been characterized by measuring the spectrum and exposure rate. These tests have been carried out in compliance to ESA/SCC 22900 and other standards.

The experimental setup used here for gamma irradiation and X-ray measurements is similar to the one described in Chapter 3, section 3.2.1. However, in the current experimental arrangements, shown in Fig. 4.5, we allow simultaneous irradiation of two capacitor devices, with one device operating in open loop configuration while the other device is under closed loop using sigma-delta control. Periodical C-V measurements have been performed for both the devices every 2 hours over the course of the entire experiment. The parameters for the closed loop control have been carefully chosen in order to obtain the desired behavior.

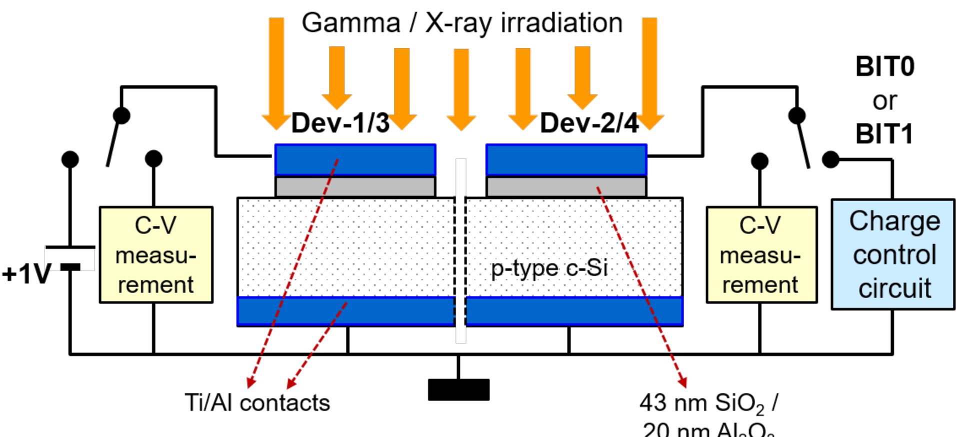

Figure 4.5: Experimental setup: MOS capacitors Dev-1/Dev-3 and Dev-2/Dev-4 are irradiated simultaneously with the same dose rate patterns. A constant bias is applied to Dev-1/Dev-3, whereas the control is being applied to Dev-2/Dev-4 to set a target capacitance. Short C-V measurements are taken in Dev-1/Dev-3 in constant time intervals, whereas only initial and final C-V measurements are taken for Dev-2/Dev-4.

4.2.3 Experiment 1: Gamma Radiation

In order to analyze the behavior of the charge trapping control method applied to devices under gamma radiation, two different capacitors from the same fabrication batch, Dev-1 and Dev-2, have been irradiated simultaneously. A long experiment has been scheduled in which Dev-1 was kept at a constant voltage bias of +1V, while the control was being applied to Dev-2 to achieve and maintain a previously given target capacitance, C_{th}. The experiment has been scheduled for 70 hours with the following three phases:

- *Phase*#0: During this phase, no radiation has been applied to the devices for the first 4 hours. This step is necessary in order for Dev-2 to reach the target level by the application of appropriate BITx waveforms and later maintain the control.
- *Phase*#1: In this phase, a constant radiation dose rate DR of 11 Gy(water)/h has been applied for the next 22 hours. Significant horizontal diplacements in the CV curves to the left can be observed for Dev-1 with radiation, while a stable CV characteristics have been guaranteed for Dev-2 working under closed loop control. The measured TID at the end of this irradiation phase was 237.6 Gy.
- *Phase*#2: During this phase of 42 hours, no radiation has been applied to the devices. We notice that as soon as the radiation is turned off, the devices starts recovering towards the previous state.

Radiation Response under Open Loop

The evolution with time of the CV characteristic curves of Dev-1 with and without radiation are shown in Figure 4.6. The device is kept under a constant bias and fast C-V measurements have been taken in 2-hour intervals during the entire experiment.

No significant displacement in the CV curve has been registered during the initial phase of zero irradiation. When the capacitor is exposed to the gamma radiation (DR=11 Gy/h) during the *Phase*#1, we notice a left-shift of the C-V which implies an accumulation of net positive charge in the dielectric, consistent with the theory described in section **??**. Finally, during the post-irradiation phase, the displacements in the CVs to the left come to a halt and we can even notice a small shift to the right. The closely spaced CVs observed in Figure 4.6 corresponds to the final rest phase.

The evolution of the voltage shift corresponding to the CV curves of Dev-1 during the experiment is depicted in Figure 4.7, along with the dose rates applied. The time evolution of the capacitance measured at a reference voltage, V_1 = -7.25 V has also been plotted. We notice that a maximum voltage shift of approximately -450 mV has been obtained at the end of the irradiation phase while a large variation of the capacitance of the device is measured at constant voltage. The total dose is 237.6 Gy(SiO_2) and therefore this represents an average voltage shift of 1.9 mV/Gy(SiO_2).

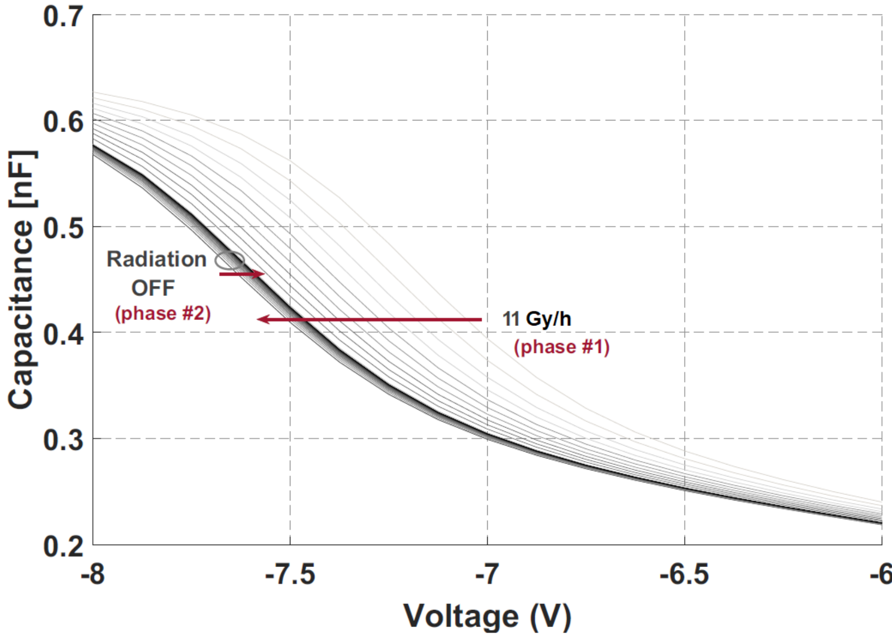

Figure 4.6: Plot of successive CVs periodically obtained in the open loop device Dev-1 polarized at 1V bias. The first plot is just after having switched on radiation (DR=11 Gy/h).

Radiation Response under Closed Loop Control

Let us now consider the case of Dev-2 operating under the closed loop sigma-delta control with the same sequence of irradiation and non-irradiation phases. In this case the feedback loop was configured to set the capacitance to a target value C_{th} = 0.495 nF at V_1 = -6.25 V, being the control voltages V^{+}= 4 V and V^{-}= -8 V. These voltage levels are chosen so that the application of the BITx waveforms results in the displacement of C-Vs in the opposite direction. Figure 4.8 depicts the time evolution of the capacitance and the average bitstream for the controlled device.

The top graph of Figure 4.8 shows the time evolution of the capacitance at the reference voltage, V_1 during the course of the control. In $Phase\#0$, as soon as control starts working at t=0, only BIT1 waveforms are being applied to the device until the capacitance rapidly reaches the target value. Once the desired capacitance C_{th} is reached, the feedback loop applies the required stream of voltage waveforms to maintain the capacitance approximately constant. When the average bitstream reaches a stable value, we begin the irradiation phase ($Phase\#1$), where the device under control is subjected to gamma irradiation, resulting in the gradual accumulation of positive charge in the oxide layer. As we have seen in the previous section, this phenomenon tends to shift the C-V to the left. Therefore $C[V_1]_n$ starts decreasing and the control forces the feedback loop to apply less BIT1 waveforms such that the target capacitance, $C[V_1]_n \approx C_{\text{th}}$ is kept constant. Decreasing the average number of BIT1s tends to displace the CV curve to the right, therefore increasing $C[V_1]_n$

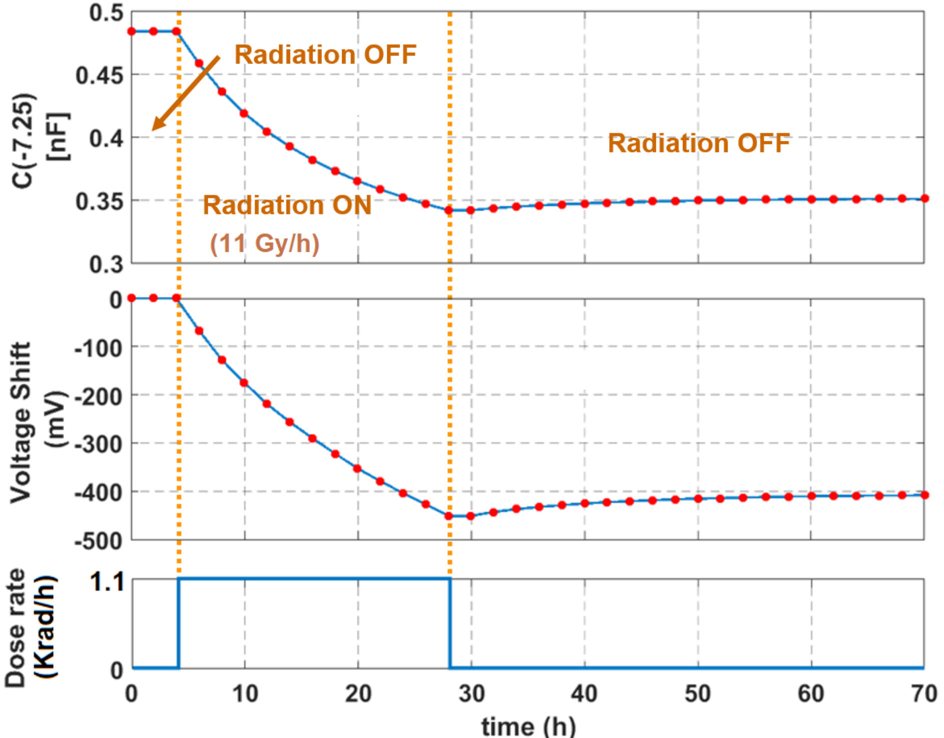

Figure 4.7: Top: Time evolution of the capacitance of Dev-1, biased at +1V during the irradiation experiment. Middle: time evolution of the voltage shift of the CV curve of the same device. Bottom: sequence of dose rates applied.

and compensating the charge generated by radiation. As the accumulated radiation dose grows, the average bitstream necessary to maintain constant the CV curve decreases, therefore implying the application of more negative voltages.

Finally, during *Phase*#2, when the irradiation is turned off, we notice that the average bitstream slowly starts to recover until it reaches a quite stable regime. The behavior of the average bitstream during the three phases shown in Figure 4.8 for Dev-2 can be related to that of the voltage shift shown in Figure 4.7 for Dev-1. This clear correlation indicates that the control loop is continuously compensating the effect of the dielectric charge induced by the radiation regime applied.

Finally, Figure 4.9 shows the C-V curves of Dev-2 obtained at the beginning and at the end of the control experiment. As it can be seen, the curves are almost undistinguishable indicating that under ionizing radiation the control loop guarantees a long-time stable CV characteristic.

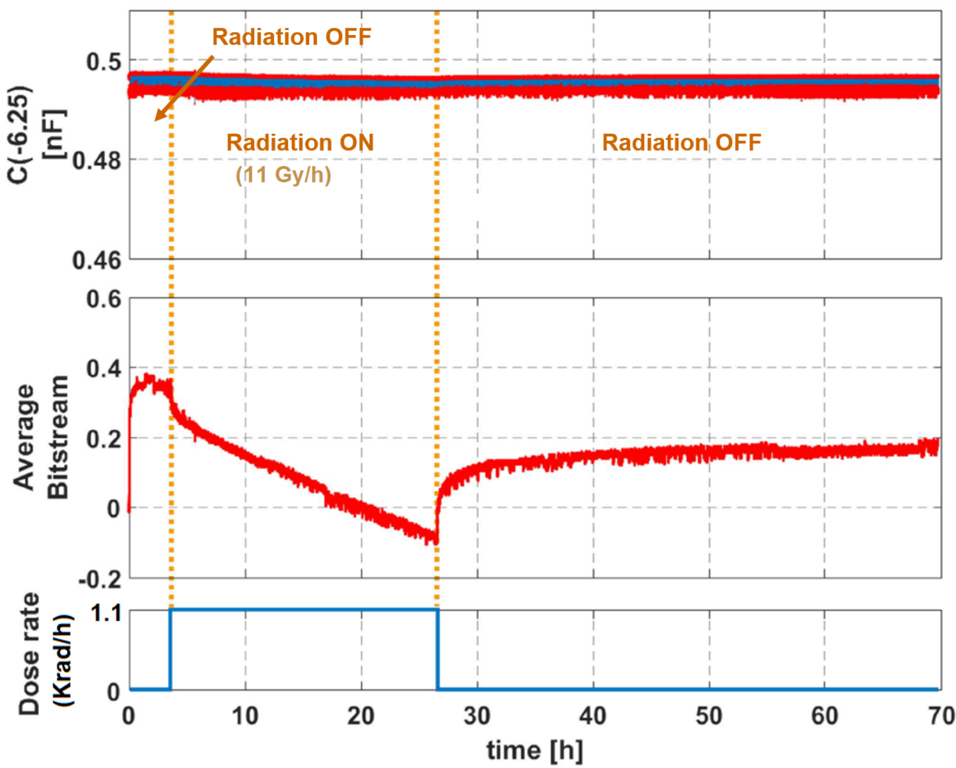

Figure 4.8: Closed loop experiment with Dev-2 under control, simultaneously irradiated with Dev-1. Top: time evolution of the capacitance measured at the reference voltage, $V_1 = -6.25V$. Middle: Average bitstream evolution (each sample is the average of 500 bits of the bitstream). Bottom: Sequence of dose rates applied.

4.2.4 Experiment 2: X-radiation

In this section, the second set of devices, containing two capacitors (Dev-3 and Dev-4) with Al_2O_3 as dielectric layer, have been exposed to irradiation from an X-ray source. Dev-3 is operated in open loop configuration at a constant bias voltage of +1V, while the control loop is applied to Dev-4 to effectively compensate the oxide-trap charge induced by X-rays.

Given the conditions of the experiment, a second-order loop is used to improve the reliability of the control, avoiding potential effects such as the existence of plateaus that can be present in first-order loops, as discussed in Chapter 3, section 3.3. In this case the capacitance of DUT4 at voltage V_1 is sampled periodically and compared with C_{th} to obtain an error signal, which is then integrated and depending on the sign of the integral, either a BIT1 or BIT0 waveform is applied during the next sampling period.

The voltages used in BIT0 and BIT1 are V^+=5V, V^-=-3V and V_1=1.5V, whereas the target capacitance is C_{th}=0.6nF. The timing parameters are T_S=350ms and δ=1/3, being T_S smaller than

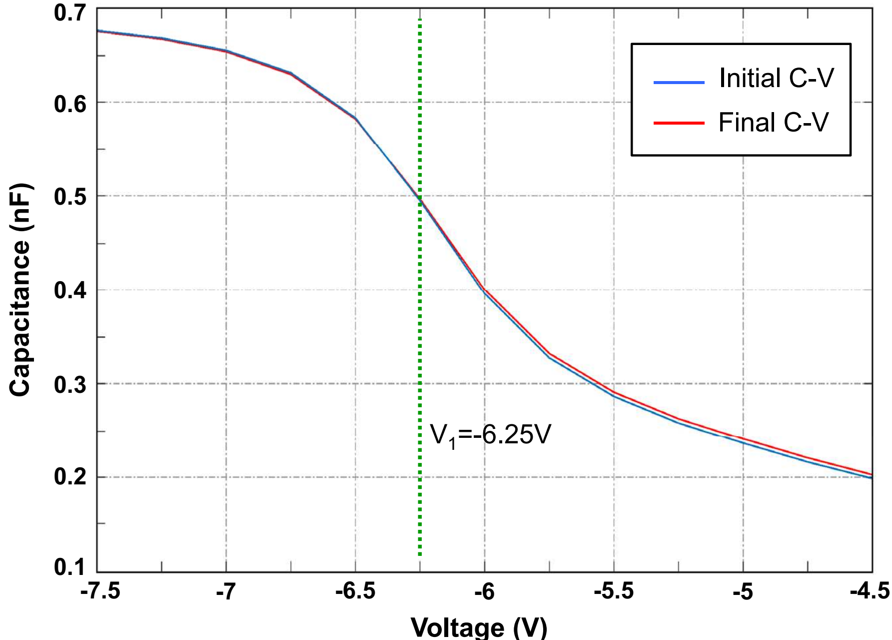

Figure 4.9: Initial and final CV of Dev-2 during the irradiation experiment. This device was controlled with a target capacitance value of C_{th} = 0.495nF at V_1 = -6.25V. The CV curves are hardly distinguishable.

the fastest time constant observed in the charging dynamics when these voltages are applied. Two precision LCR Meters generate the BITx waveforms and perform the capacitance measurements on each device.

Radiation Response under Open Loop

The experiment starts with no radiation for 90 minutes, followed by X-ray irradiation for 9 hours (at a constant dose rate of 10Gy/h), and an 8-hour final stage with no radiation.

Fig. 4.10(a) shows the evolution of the CV of DUT3, which is under constant +1V bias. The CVs exhibit noticeable rigid left-shifting during the irradiation stage. Since other effects such as stretch-out are not observed, it can be concluded that the shifts are produced by increasing amounts of positive net charge trapped in the dielectric during irradiation [12].

Additionally, a constant shift rate of 0.25 mV/Gy during the irradiation phase is observed in Fig. 4.10(b). It is also seen that the device starts getting stabilized once radiation is turned off, and that the charge generated in the radiation phase remains once radiation ceases. This indicates that the charge accumulated by radiation is not removed after irradiation.

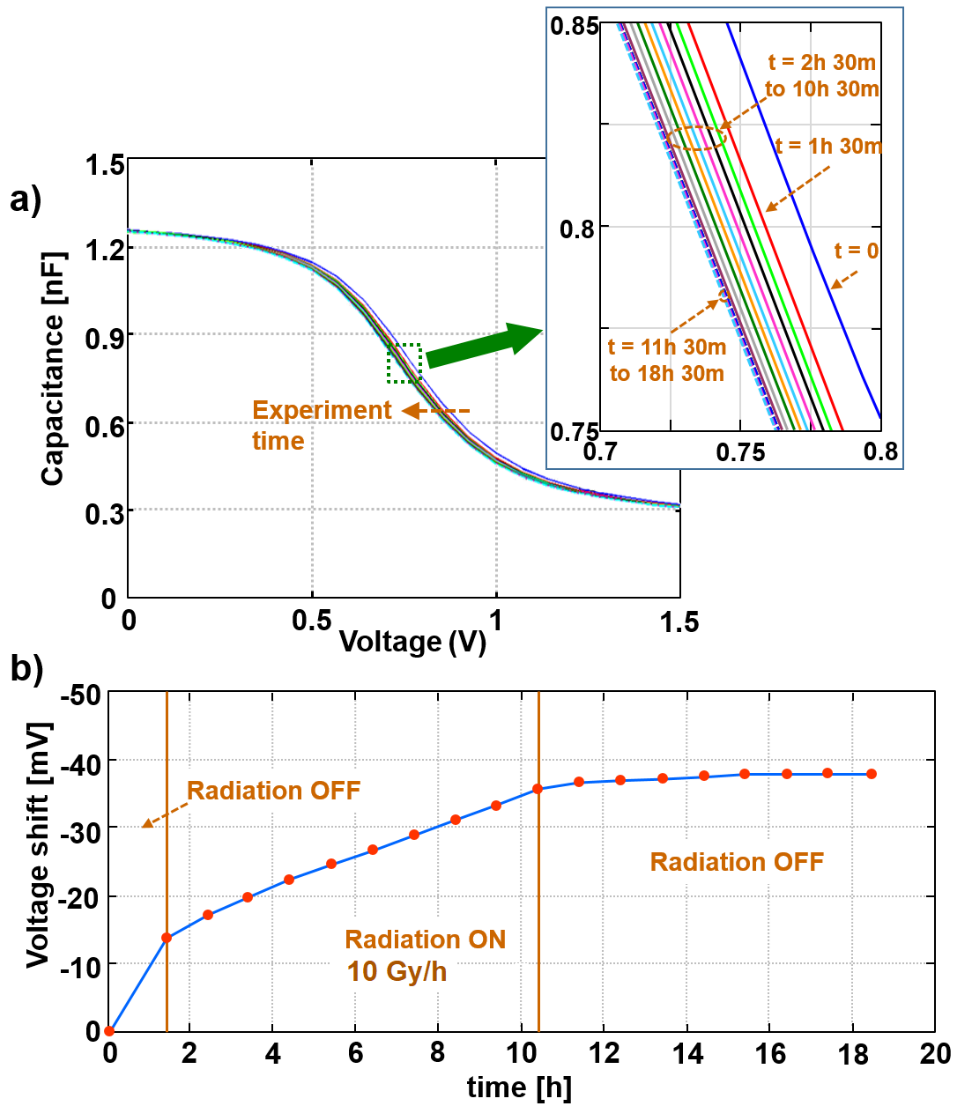

Figure 4.10: Results obtained with DUT3 in experiment 2. The device was under constant V_{bias}=1V. a) CV curves measured periodically during the experiment. The inset shows a closer view of the transition region of the CVs. b) Evolution of the voltage shift of the CVs during the experiment. Noticeable left-shifting due to positive charge induced by the radiation is observed.

Radiation Response under Closed Loop Control

On the other hand, the top graph in Fig. 4.11 shows the evolution of the capacitance at V^0=1.5V of DUT4, which is under charge control. During the initial stage (radiation off) the control acts until (at t=30 minutes) the target capacitance C_{th} =0.6nF is achieved. Once this value is reached,

it is successfully maintained during the rest of the experiment, irrespective of whether the radiation is on or off.

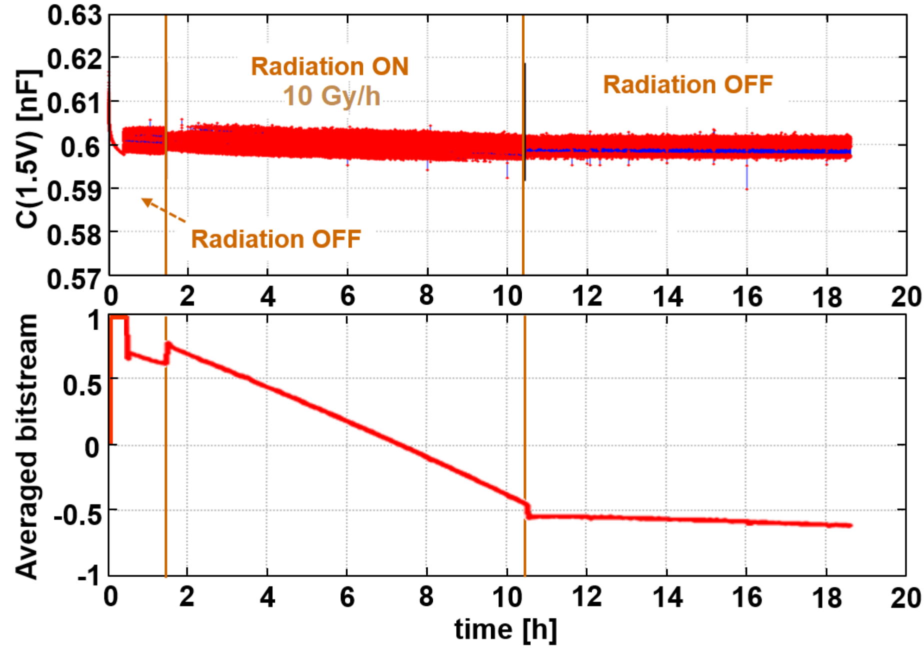

Figure 4.11: Evolution of the capacitance at V_1 = 1.5V (top) and of the control bit stream (bottom) of DUT4 during experiment 2. The device was under second order charge control with target capacitance C_{th} =0.6 nF.

The bottom graph in Fig. 4.11 shows the evolution of the bit stream provided by the control loop. It illustrates how the control works; initially only BIT1s are applied, accumulating positive charge in the dielectric and moving the CV to the left to reach C_{th}. During the irradiation stage (from t=90 min to t=10h 15 min), the control increases the number of BIT0s, thus injecting more negative charge that compensates the accumulation of positive charge produced by the radiation. Once irradiation stops, the accumulated-remaining charge leads the bit stream to stabilize. A straight relationship between the voltage shifts of Fig. 4.10 and the control bit stream of Fig. 4.11 can also be observed.

Finally, Figure 4.12 shows three CV curves of DUT4, measured during the experiment. The inset shows the curves at t=0m when the device is in its initial state, at t=45m when the device under closed loop control, and finally at t=18h 30m just before the control has ended. As expected, once the target value is reached (at t=45 m) the CVs are hardly distinguishable.

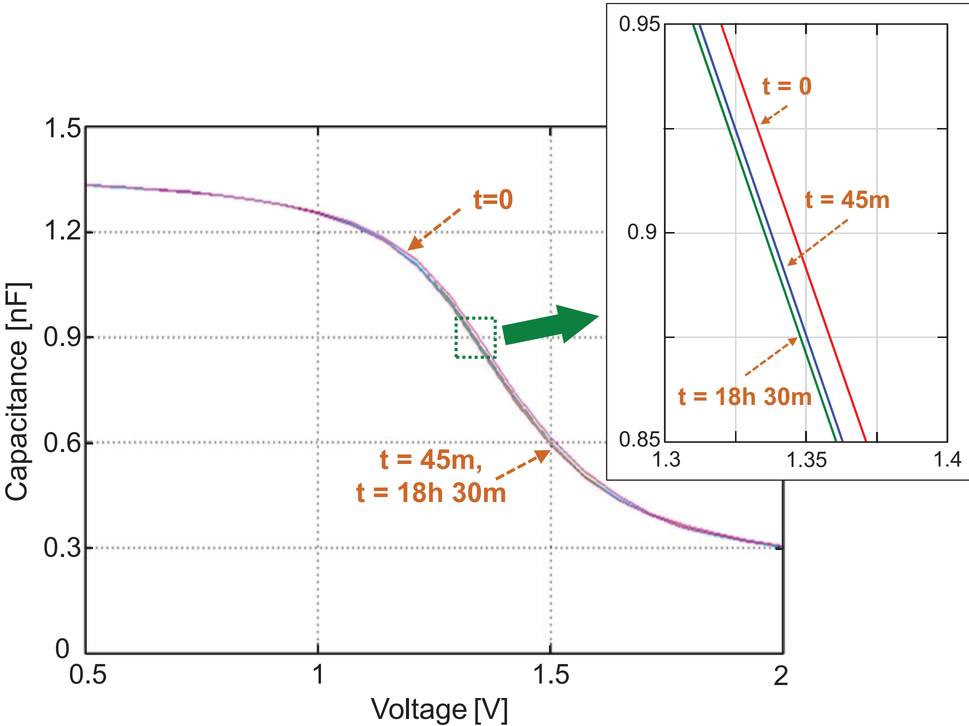

Figure 4.12: CV curves of DUT4 measured at three different times of the experiment reported in Fig. 4.11. The inset shows a closer view of the transition region of the CVs.

4.3 Conclusions

An active control technique based on sigma-delta modulation has been implemented on MOS capacitors operating under ionizing radiation to keep constant the CV characteristic during the whole operation of the devices. The evolution of the voltage shift of the CV curve and the correlation between the control bitstream and the dose rates applied indicate that the dielectric charge generated by irradiation can be compensated. Experiments have been shown in which this compensation is obtained with gamma radiation and X-rays. The results obtained open the possibility of using this technique to improve the reliability of MOS-related devices working in hardness environments. One of the possible applications could be in the field of radiation detection such as RADFETs (RADiation sensitive Field Effect Transistors), devices specially designed for radiation sensing.

Using the charge trapping control method proposed in this thesis, it would be possible to avoid the saturation of the threshold voltage shift with accumulated dose, thereby extending the life time of RADFETs. Also, the real-time information about the charge being induced by radiation can be obtained from the binary bitstream provided at the output by the control loop.

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Chapter 5

Modeling and Analysis of Charge Trapping Dynamics in MOS Capacitors

The purpose of this chapter is to characterize the dynamics of charge trapped in the dielectric layer of a MOS capacitor using Diffusive Representation (DR) technique. An experimental model has been drafted from a series of predetermined test signals applied to the device and recording the corresponding responses. The model thus obtained represents the properties of the device thus allowing us to understand better the device. An experimental corroboration has been made in order to validate the model predictions under open and closed loop actuation strategies. Further, the behavior of the device under closed loop control has been predicted using the tools of sliding mode control. The obtained time-varying model is in very good agreement with the experimental data even under the influence of the external disturbances. In this regard, the chapter has been organised as follows: Section 5.1 derives the DR model used to characterize the charge dynamics and validates it using the experiments. Section 5.2 presents the sliding mode model to analyze the charge dynamics when the device is being controlled by a sigma-delta control. The experimental measurements validating the proposed models discussed in the previous sections are presented in Section 5.3. Finally, section 5.4 concludes this chapter.

5.1 Characterization of Trapped Charge Dynamics

Diffusive Representation technique, introduced in Chapter 2, has been used for the identification of the dynamic model of charge trapping in MOS capacitor structures. The diffusive nature of the charge trapping phenomena allows their behavioral characterization using state-space models based on DR. In recent times, DR tools have been successfully used for modeling and prediction purposes in several diffusion-based systems, such as thermal [14, 15] and electrical [16, 17] fractional systems.

In this thesis, DR has been used since it allows directly obtaining models from measurements that can be very easily simulated and are compatible with physical processes including diffusion and dispersion in general.

5.1.1 Diffusive Representation

DR is a convenient mathematical tool used to represent the complex integral operators in terms of approximate state realizations making the time analysis and numerical implementations simple. This tool enables a modeling strategy for complex systems that provides simpler analysis of their dynamics with reduced computational cost. In this section, a model based on DR is developed to characterize the dynamics of the charge trapped in the dielectric of MOS capacitors. Later, the the model predictions are validated using the experiments under arbitrary voltage excitations.

Given a non-rational transfer function, $H(p)$, associated with a convolution causal operator denoted by $H(\partial_t)$, the diffusive realization of this operator is expressed by the following input (u) – output (y) state space realization of $u \longmapsto y = H(\partial_t)u = h * u$ of the form [28, 16]:

$$\begin{aligned} \dot{\psi}(\xi,t) &= -\xi\psi(\xi,t) + u(t), \qquad \psi(\xi,0) = 0 \\ y(t) &= \int_0^\infty \eta(\xi)\psi(\xi,t)d\xi \end{aligned} \tag{5.1}$$

where $\xi \in \mathbb{R}$ is frequency and $\psi(\xi,t)$ the diffusive representation of the input, $u(t)$ [16] and it stores a part of the history of input. The weight distribution of $\psi(\xi,t)$ in the output, $\eta(\xi)$, is the diffusive symbol of the operator that represents the behavior of the system.

The diffusive symbol $\eta(\xi)$ is a solution of the equation shown below, directly obtained from the Laplace transform with respect to time. Note that the diffusive symbol depends on the operator but not on the input.

$$H(p) = \int_0^\infty \frac{\eta(\xi)}{p+\xi}d\xi \tag{5.2}$$

The DR model used in this work is obtained by finite order approximation of the operator $H(\partial_t)$, with the continuous variable ξ discretized into $\{\xi_k\}_{1\leq k\leq N}$, where N is the order of the model. This gives us the input-output approximation $u \longmapsto \tilde{y} \approx y = H(\frac{d}{dt})u$ of the dynamical system described as:

$$\begin{aligned} \dot{\psi}_k(t) &= -\xi\psi(t) + u(t), \qquad \psi(0) = 0 \\ y(t) &= \sum_{k=1}^{N} \eta(\xi_k)\psi_k(t) \end{aligned} \tag{5.3}$$

This approach allows working with experimental data, which consist on periodical samples of the output (a variable related to the variation of the trapped charge), when specific time-varying input functions are applied to the device. These input functions, described later in this section, are sequences of voltage waveforms that imply switching between a reduced number of M voltage

levels. According to this, let us consider the input function $v(t) : V \longrightarrow R$, of the form,

$$v(t) = \sum_{i=1}^{M} V_i \; 1_{S_i}(t) \tag{5.4}$$

where $1_{S_i}(t)$ is an indicator function, defined as,

$$1_{S_i}(t) = \begin{cases} 1, & v(t) = V_i \\ 0, & v(t) \neq V_i \end{cases} \tag{5.5}$$

and where $\{S_i\}$ is a sequence of disjoint measurable sets. Now, the charge trapping in the device can be modelled as a time-varying linear system and the time evolution of such a system is described with the following set of $M \times N$ equations,

$$\dot{\psi}_k^i(t) = -\xi_k \psi_k^i(t) + 1_{S_i}(t), \qquad i = 1 \cdots M \tag{5.6}$$

where $\{\xi_k\}_{1 \leq k \leq N}$ is the frequency mesh [20].

The state vector is $\psi(t) = (\psi^1(t) \; \psi^2(t) \; ... \; \psi^M(t))^T \; \in \mathbb{R}^M$

where $\psi^i(t) = (\psi_1^i(t) \; \psi_2^i(t) \; ... \; \psi_N^i(t)) \; \in \mathbb{R}^N$. This state vector is always continuous during the switching between voltages.

The output of the system can be expressed as,

$$y(t) = \sum_{i=1}^{M} \sum_{k=1}^{N} \eta_k^i \psi_k^i(t) \tag{5.7}$$

where η_k^i is the diffusive symbol related to the frequency ξ_k and the voltage V_i. The set of diffusive symbols related to each voltage V_i is defined as $\eta^i = (\eta_1^i \; \eta_2^i \; ... \; \eta_N^i) \; \in \mathbb{R}^N$.

Since the device could be in an arbitrary charge status at the beginning of an experiment (i.e at $t = t_0$), adding an exponential decay term with coefficients a_k allows including such 'initial condition' in the model. In this case, the output $y(t)$ becomes:

$$y(t) = \sum_{i=1}^{M} \sum_{k=1}^{N} \eta_k^i \psi_k^i(t) + \sum_{k=1}^{N} a_k e^{-\xi_k (t - t_o)} \tag{5.8}$$

The diffusive symbols η_k^i and the coefficients a_k are obtained by fitting the output corresponding to the finite order approximation of the operator with experimental data. Here, the diffusive symbols obtained by pseudo-inverting $H(p)$ provide a close approximation to the operator.

The accuracy of this model depends on the distribution of the frequency mesh $\{\xi_k\}_{1 \leq k \leq N}$, which in our case is chosen to be geometrically spaced in the band of interest

$$\xi_{k+1} = r \xi_k, \;\; r = \left(\frac{\xi_N}{\xi_1} \right)^{\frac{1}{N-1}} \tag{5.9}$$

The minimum and maximum frequencies (and hence the bandwidth) depend respectively on the total duration of the measurements, T (then $\xi_{min} = 2\pi/T$), and on the sampling time, T_S (then $\xi_{max} = 2\pi/T_S$).

The output of the system in our model is the amount of voltage shift generated in the C-V characteristic of the device due to the accumulation of charge. Thus the voltage shift can be interpreted as an indirect representation of the changes in the net charge trapped in the dielectric. This is compatible with the observations in [27], which indicated that charge injection changed when the net charge levels around which they were studied were far apart one of the other. In practice, this means that constant multi-exponential charge models are valid for MOS capacitors, so long as the total displacement of the net charge is not significantly changed.

5.1.2 Model Prediction and Validation using DR

In order to obtain the DR model, an open loop experiment has been performed to characterize the capacitor by applying a sequence of BIT0s and BIT1s as the input data. Concretely, a Pseudo Random Binary Sequence (PRBS) technique has been used to this purpose. PRBS is a simple binary sequence especially used for the purpose of system identification. It is a random sequence of finite length predetermined signals, synthesized using linear-feedback shift registers of length n by taking the exclusive-NOR from several taps. In our case, PRBS is a random sequence of macro-bits, each one composed of a specific number of identical BIT0 (or BIT1) waveforms with the specific number (in our case 30) chosen based on the duration of the BITx waveform, T_S, and the frequency of the PRBS sequence. The BITx parameters chosen are V^+=V^1=1.5V, V^-=-3V, δ=1/3 and T_S=420ms. The voltage levels have been chosen to simplify the process of obtaining the DR model. Since the length of the experiment is 21 hours, the frequency ranges approximately from f_{min}=8.5μHz to $f_{max} = 0.1Hz$, with values spaced geometrically.

The experiment has been divided into two parts of equal duration. During the first half, the diffusive symbols are extracted from fittings of the experimental data. The DR model derived is then used for prediction purposes in the second half of the experiment. There, the DR model simulation is compared with the remaining experimental data. Let us remark here that the data obtained from the experiment is the evolution of the sampled device capacitance at a given voltage, $C(V^1)|_n$. However, since we are interested in the charge control characteristics in terms of shifts of the CV curves, the capacitance variation has been converted into voltage shift variation. Let us also remark that the DR model describes the time evolution of the net charge in the device for given constant voltages. For a given voltage, this net charging will generally be the result of the injection of both positive and negative charge.

A DR model of order $N = 5$ has been chosen to fit the data from the first part of the experiment, reported in Figure 5.1. The time evolution of both the experimental voltage shift and the model data are shown there. Note that a perfect match exists. The order of the DR model is the minimum allowing good accuracy in the fittings, since further increasing the order does not improve such accuracy, as shown in [29]. The diffusive symbols inferred from the fitting, associated with the two voltage levels used, are shown in Figure 5.2. As discussed above, the dependence of the

obtained symbols only on the operator but not on the input allows modeling the charge/voltage shift dynamics of the device for arbitrary input sequences. The difference when a positive or negative voltage is applied can be observed in the diffusive symbol, as well as a difference in the amplitudes due to the absolute voltage values. The non-convergence of the diffusive symbols observed at high frequencies is due to the lack of high frequency components.

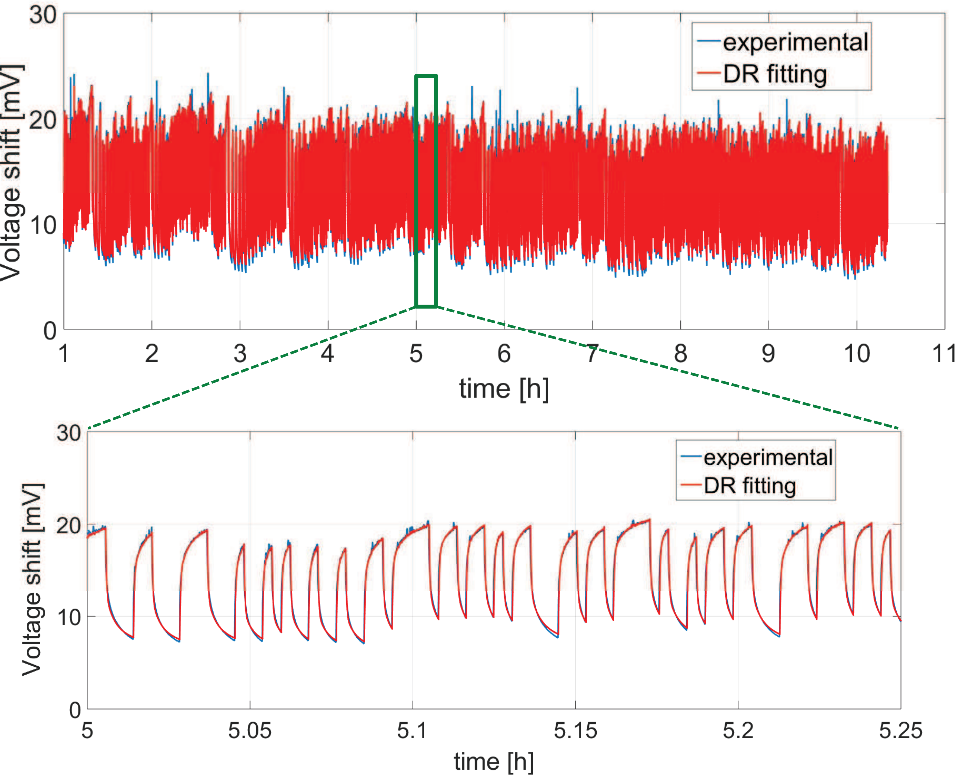

Figure 5.1: Top: Evolution of the voltage shift of the C-V (in blue) and diffusive representation fitting (in red) for an experiment in which a PRBS was applied to the device for 10.5 hours. The root mean square error (RMSE) value obtained from fitting is 0.69mV. A 15-minute zoom is shown at the bottom. The diffusive symbols obtained from the fitting are shown in Figure 5.2.

The next objective is to validate the model through comparison of its predictions with the experimental results obtained taking the second half of the PRBS as the input signal. This step is necessary to investigate the capability of the model to describe the charge dynamics when other arbitrary waveforms using the same voltages are applied. The result of this second half of the experiment is reported in Figure 5.3, where very good match between prediction and experimental data is observed.

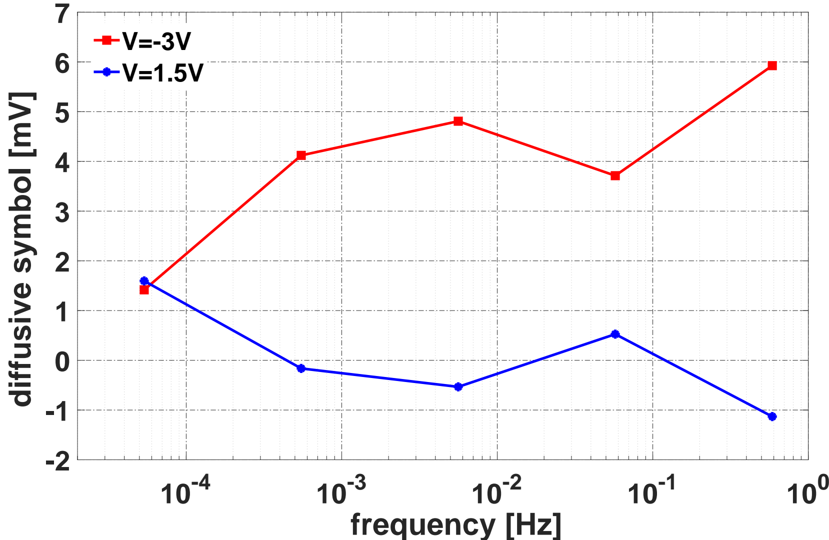

Figure 5.2: 5-th order diffusive symbols of the voltage shift for the two voltages used in the BIT0 and BIT1 waveforms applied to the device: $V^{+} = +1.5V$ and $V^{-} = -3V$.

5.2 Sliding Mode Controllers (SMC): Sigma-Delta Modulation Approach

In this section, the state space models obtained in the previous section have been used to analyze the charge dynamics of a capacitor device, operating under sigma-delta control, using the tools of sliding mode controllers for an infinite sampling frequency approximation. The sigma-delta control method, introduced in Chapter 3, is aimed to provide sliding mode control of the net charge trapped in the dielectric of a MOS capacitor. Sigma-delta modulators have been linked to sliding mode controllers [31, 32]. The link comes from the fact that the modulator tries to minimize the quantization noise of the quantizer (in the case of Fig. 5.4 the sign function), in the frequency band of interest. In Fig. 5.4, for example, the modulator tries to enforce a zero average value of the integrator output: $\overline{u_n} \approx 0$. This may be seen as a sliding motion on a desired control surface within the space of state variables (here, only one state variable: the integrator output). In order to obtain this result, the average value of the bitstream must be the same as the average value of the input signal: $\overline{x_n} = \overline{b_n}$. Finally $\overline{b_n}$ provides, therefore, the well-known equivalent control signal of sliding mode controllers which will be discussed further in the next sections.

Here, no specific design of sliding mode controllers has been made, but a simplified analytical model, which allows to predict and analyze the sequence of control signals, has been introduced and then validated with experimental data.

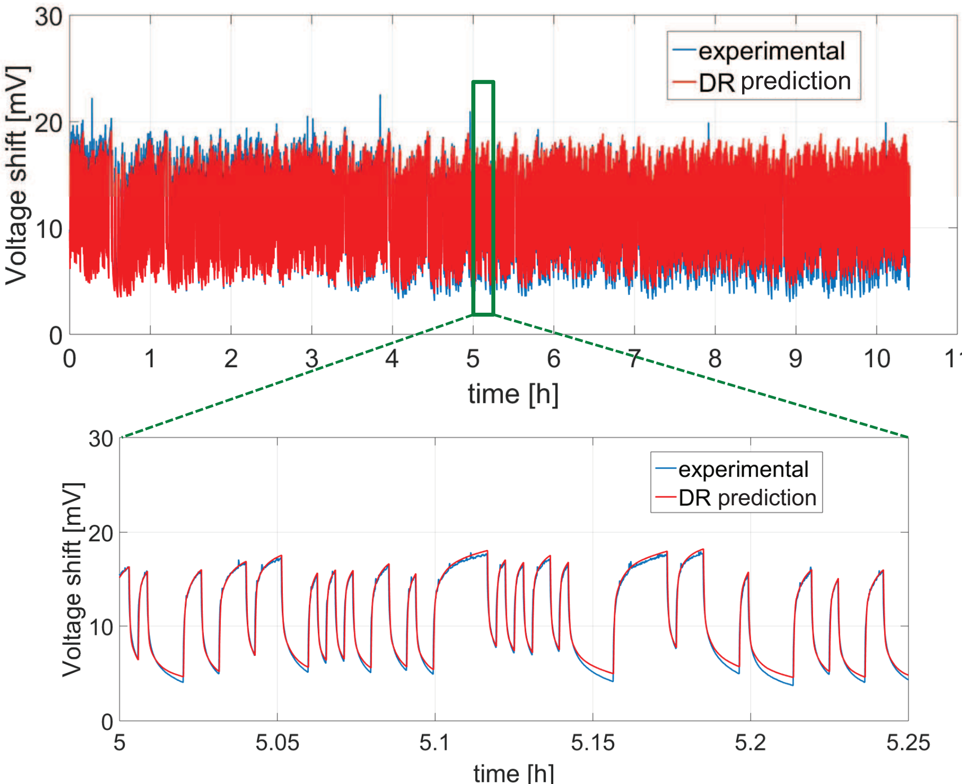

Figure 5.3: Evolution of voltage shift (in blue) versus DR model prediction (in red) for an experiment in which a PRBS was applied to a MOS capacitor for 10.5 hours. The root mean square error (RMSE) value obtained from comparing the model prediction with the experimental data is 0.86mV. This experiment followed that shown in Fig. 5.1. A 15-minute zoom is shown at the bottom.

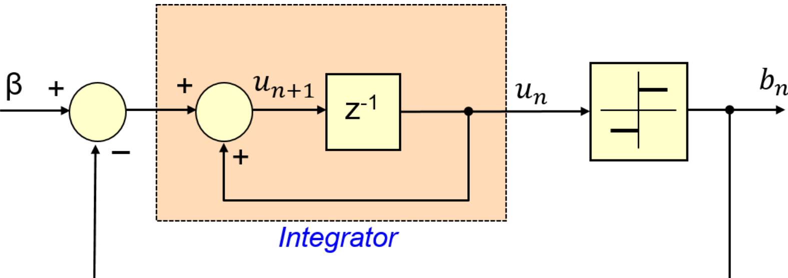

Figure 5.4: First-order sigma-delta charge control loop [18].

5.2.1 SMC: Linear Time-Varying Charge Model

In this subsection, a linear time-varying charge model is presented to describe the sigma-delta charge control system using the tools of SMC. The time evolution of the system for an arbitrary voltage waveforms with different voltage levels, say $v(t) \in \{V_1, V_2, V_3\}$, can be analyzed using the time-varying linear systems described as:

$$\dot{\psi}_k^i(t) = -\xi_k \psi_k^i(t) + 1_{s_i}(t), \qquad i = 1...M \tag{5.10}$$

where $1_{s_i}(t)$ is an indicator function defined in equation (5.5) The output of the system, as can be seen in the case of SISO systems, is expressed as a weighted combination of the state variables. The weight coefficients in this particular case are the diffusive symbols, η_k, obtained by fitting with the experimental data as discussed in section 5.1.2. So the output of the system in our case is the voltage shift in the C-V characteristics due to the accumulation of dielectric charge and is given/expressed as

$$V_{sh}(t) = \eta^T \psi(t) \tag{5.11}$$

The voltage waveforms, as we call them BITx waveforms, used to actuate the device/system are composed of different voltage levels with different durations. In our experiments, each BITx waveform consists of two voltage levels, the voltage level with longer duration is used to control whereas the other voltage level senses the state of the system at the end of each sampling time period, T_s.

The actuation voltage waveforms BIT0 and BIT1 can be described as:

$$v_{\mathrm{bit0}}(t) = \begin{cases} V_1, & t \in [0, (1-\delta)T_S) \\ V_2, & t \in [(1-\delta)T_S, T_S) \\ 0, & t \notin [0, T_S) \end{cases} \tag{5.12}$$

$$v_{\mathrm{bit1}}(t) = \begin{cases} V_3, & t \in [0, (1-\delta)T_S) \\ V_2, & t \in [(1-\delta)T_S, T_S) \\ 0, & t \notin [0, T_S) \end{cases} \tag{5.13}$$

where $V_1 = V^-$, $V_2 = V^1$ and $V_3 = V^+$. Taking into account the definitions of time-varying linear system, and the actuation waveforms described earlier, one can write a first-order sigma-delta

control loop as:

$$\begin{aligned} \dot{\psi}_k^i(t) &= -\xi_k \psi_k^i(t) + 1_{s_i}(t) && (5.14) \\ v(t) &= \frac{1}{2}\sum_n (1+b_n) v_{\text{bit1}}(t - nT_S) \\ &\quad +(1-b_n) v_{\text{bit0}}(t-nT_S) && (5.15) \\ V_{sh}(t) &= \sum_{i=1}^{M}\sum_{k=1}^{N} \eta_k^i \psi_k^i(t) = \eta^T \psi(t) && (5.16) \\ b_n &= \text{sgn}(V_{sh}(nT_S) - V_{target}) && (5.17) \end{aligned}$$

where b_n is the control bit stream, and V_{sh} and V_{target} are respectively the actual and the target values of the voltage shift.

As can be seen from (5.12), and (5.13), $v_{bitx}(t)$ waveform is discontinuous signal, the components of which switch from V_1 to V_2 and V_3 to V_2 respectively within the sampling interval $[nT_s, (n+1)T_s]$. This discontinuous switching can be eliminated by imposing an 'infinite sampling frequency approximation' on control bits/signals and the current sigma-delta control system can be approximated to an average system. The obtained average system, as described in the next section, conserves all the essential features of the original system dynamics.

5.2.2 Deterministic Switching: Average System

The voltage waveforms BIT0 and BIT1 present a two level hierarchy. The first level is voltage switching within each waveform and it provides an instantaneous amount of voltage shift at the end of each sampling time interval. The second level is the switching between different waveforms, which depends on the instantaneous value of the net charge at the sampling times nT_S and therefore on the sampled state vector, ψ.

Now the average system is a smooth dynamical system obtained from (5.14), and (5.15) when the sampling frequency of the system tends to infinity. Assuming this 'infinite sampling approximation', which in this case implies that the sampling period, in the limit $T_S \to 0$, is at least one order of magnitude below the shortest time constant in the affine models, the continuous voltage switching within the bits can no longer be considered. Thus the discontinuous control bit waveforms can be replaced by a continuous waveform which is a convex combination of the available voltage components with the average parameter defined by the duty cycle associated with the voltages. According to this the time evolution of the state variables under the application of either BIT0 or BIT1 can be written as:

$$\dot{\psi}_k^i(t) = -\xi_k \psi_k^i(t) + \alpha_0^i 1_{b_0(t)} + \alpha_1^i 1_{b_1(t)} \tag{5.18}$$

where the function $1_{b_x}(t)$ indicates whether a BIT0 or a BIT1 is applied at time t (then $\sum_x 1_{b_x}(t) = 1$) and α_x^i is the percentage of time within BITx in which the voltage V_i, $i \in [1, ..., M]$, is applied. This therefore means that $0 \le \alpha_x^i \le 1$ and $\sum_i \alpha_x^i = 1$. To illustrate this, we consider three voltage

levels, V_1, V_2, and V_3 such that the waveforms for BIT0 and BIT1 can be expressed as

$$\begin{aligned} v_{\text{bit0}}(t) &= V_1 1_{[0,(1-\delta)T_S)}(t) + V_2 1_{[(1-\delta)T_S,T_S]}(t) \\ v_{\text{bit1}}(t) &= V_3 1_{[0,(1-\delta)T_S)}(t) + V_2 1_{[(1-\delta)T_S,T_S]}(t) \end{aligned} \tag{5.19}$$

From this, we get $(\alpha_0^1, \alpha_0^2, \alpha_0^3) = (1-\delta, \delta, 0)$ for BIT0 and $(\alpha_1^1, \alpha_1^2, \alpha_1^3) = (0, \delta, 1-\delta)$ for BIT1, respectively.

The dynamics of this system under the sigma-delta control can be described as:

$$\dot{\psi}_k^i(t) = -\xi_k \psi_k^i(t) + \alpha_0^i \frac{1-\text{sgn}(\sigma)}{2} + \alpha_1^i \frac{1+\text{sgn}(\sigma)}{2} \tag{5.20}$$

where $\sigma = V_{sh}(t) - V_{target}$.

So under the assumption of an infinite sampling frequency approximation, we have shown that an average system can be expressed as convex combination of subsystems with averaging parameter given by α_0^i and α_1^i for BIT0 and BIT1 respectively.

Finally, equation (5.20) can be simplified to express in the form of a conditional expression as:

$$\dot{\psi}_k^i(t) = \begin{cases} -\xi_k \psi_k^i(t) + \alpha_0^i, & \sigma < 0, \\ -\xi_k \psi_k^i(t) + \alpha_1^i, & \sigma > 0, \end{cases} \tag{5.21}$$

5.2.3 Sliding Mode Analysis

The set of equations (5.21) can be seen as the description of a particular case of sliding mode controller, in which the sliding function is defined as $\sigma = V_{sh}(t) - V_{target}$ and where the time dynamics of two average systems depend on whether the state vector is on one side ($\sigma < 0$) or the other ($\sigma > 0$) of the control surface $\sigma = 0$. This result is very similar to that obtained for charge control in MEMS [19] and is in perfect accordance with the relationship between sliding mode control and sigma-delta modulation explained in [31].

The sliding mode control can be understood as consisting of two successive phases. The first part is the reaching phase, where the control applies a constant sequence of actuation waveforms to make the average system reach the sliding surface ($\sigma = 0$) from an arbitrary initial position, say $\psi^-(0)(\sigma < 0)$ or $\psi^+(0)(\sigma > 0)$, depending on whether the system initially lies above or below the sliding surface. A series of continuous BITx waveforms is being applied until it reaches the designed surface. The second part consists of the sliding phase, during which the state of the system moves along the sliding surface. The system/control dynamics depend on the system parameters during the reaching phase whereas they strictly depend on the surface in the sliding mode. The time evolution of the state variables is determined by the equivalent control necessary to maintain the system within the control surface.

The ability of the system to reach the control surface depends on the target level, the applied voltage levels and also on the parameter δ. Once a target level has been set, the control will try to reach this level and depending on the chosen charging models, the target may or may not be

reached. In our case, the control surface is defined as $\sigma = \sum_{i=1}^{M}\sum_{k=1}^{N}\eta_k^i\psi_k^i(t) - V_{target} = 0$. Suppose that the initial state of the system, $\psi(0)$ is such that $\sum_{i=1}^{M}\sum_{k=1}^{N}\eta_k^i\psi_k^i(0) < V_{target}$ (i.e in the plane $\sigma < 0$), then the control surface is reached if the asymptotic point of this trajectory $(\psi(t\to\infty) = \sum_{i=1}^{M}\sum_{k=1}^{N}\frac{\eta_k^i\alpha_0^i}{\xi_k})$ lies on the other side of the plane (i.e $\sigma < 0$) which gives us the condition

$$\sum_{i=1}^{M}\sum_{k=1}^{N}\frac{\eta_k^i\alpha_0^i}{\xi_k} > V_{target} \tag{5.22}$$

A similar analysis when applied to the system lying in the plane $\sigma > 0$ provides us with the condition given by

$$\sum_{i=1}^{M}\sum_{k=1}^{N}\frac{\eta_k^i\alpha_1^i}{\xi_k} < V_{target} \tag{5.23}$$

If the conditions (5.22) and (5.23) are satisfied, then the system reaches the control surface from any arbitrary initial position in finite time.

Now, assuming that the conditions for reachability are fulfilled and that an attractive sliding domain exists with the control surface, then the control surface,$\sigma = 0$, will be reached. A solution is obtained in the sense of Filippov for these systems with discontinuity, as a convex linear combination of the vector fields applied on both sides of the control surface:

$$\dot{\psi}_k^i(t) = -\xi_k\psi_k^i(t) + \lambda(\psi)\alpha_1^i + (1-\lambda(\psi))\alpha_0^i \tag{5.24}$$

where $0 \leq \lambda \leq 1$ must coincide with the average values of the bit stream (properly windowed by a low pass filter) and must ensure that $\dot{\sigma}$ must be zero i.e., the system slides on the control surface. It is important to note that, in fact, the average bitstream λ depends on the state vector ψ. However, to simplify the notation we will not explicitly indicate this dependence in the next equations.

Taking into account the expression of the voltage shift given in (5.16), the condition $\dot{\sigma} = 0$ leads to:

$$\dot{V}_{sh}(t) = \sum_{i=1}^{M}\sum_{k=1}^{N}\eta_k^i(-\xi_k\psi_k^i(t) + \lambda(\psi)\alpha_1^i + (1-\lambda(\psi))\alpha_0^i) = 0 \tag{5.25}$$

The solution of the above equation is $\lambda(\psi)$, the control equivalent which keeps the system on the control surface:

$$\lambda = \frac{\sum_i\sum_k\eta_k^i\xi_k\psi_k^i(t) - \sum_i\sum_k\eta_k^i\alpha_0^i}{\sum_i\sum_k\eta_k^i(\alpha_1^i - \alpha_0^i)} \tag{5.26}$$

Now, expressions (5.24) and (5.26) together provide the non-linear equation evaluating the time response of the system after reaching the sliding surface, $\sigma = 0$.

5.2.4 Effect of External Disturbances and Parameter Uncertainties

SMC is an attractive control technique for systems with parametric uncertainties and unknown disturbances due to its disturbance rejection capabilities. Suppose the disturbances can be represented

by a vector $\phi(\psi,t)$ then (5.24) can be rewritten as

$$\dot{\psi}_k^i(t) = -\xi_k \psi_k^i(t) + \lambda(\psi)\alpha_1^i + (1-\lambda(\psi))\alpha_0^i + \phi(\psi,t) \tag{5.27}$$

Now, disturbances can be decomposed as matched,$\phi(\psi,t)$ and mismatched$\phi(\psi,t)$ components. The matched component enters the system through the control input and can be successfully cancelled out directly by the equivalent control, whereas the mismatched component affects the states directly and generates changes in both the equivalent control and the control surface.

Let us now investigate the case in which the device, with or without control, is under an external disturbance such as ionizing radiation. As it will be shown experimentally in the next section, ionizing radiation creates additional charge trapping that should be added to the analysis of the previous sections. According to this, it can be supposed that the voltages applied to the device have an almost negligible effect on the dynamics of the charge generated by the disturbance. Under this consideration, the effect of this charge can be seen as an additional term in (5.24) and consequently as a shift of the C-V of value $\phi(t)$. Then, the 'effective' voltage shift becomes:

$$V_{sh}(t) = \sum_{i=1}^{M} \sum_{k=1}^{N} \eta_k^i \psi_k^i(t) + \phi(t) \tag{5.28}$$

and the new expression for λ is:

$$\lambda = \frac{\sum_i \sum_k \eta_k^i \xi_k \psi_k^i(t) - \sum_i \sum_k \eta_k^i \alpha_0^i - \dot{\phi}(t)}{\sum_i \sum_k \eta_k^i (\alpha_1^i - \alpha_0^i)} \tag{5.29}$$

This result can be interpreted as follows: an external disturbance produces changes in both the control surface and the average bit stream that are necessary to keep the voltage shift (or the net charge) constant at the target value V_{target}.

5.3 Experimental Results and Discussion

The purpose of this section is to validate the effectiveness of the DR model when charge control is applied to a MOS capacitor. Another objective is to verify that the control system behaves as a sliding controller and therefore it can be analyzed and interpreted by means of the analytical model introduced in the previous section.

5.3.1 Experiment 1: Charge Trapping Control

In this experiment, sigma-delta control is applied to an Al_2O_3 capacitor to set a constant target voltage shift for 25 hours. The BITx parameters used are: V^+=V_1=1.5V, V^-=-3V, T_S=350ms and δ=1/3. The target voltage shift is V_{target}=7.8mV, which for the device chosen corresponds to a target capacitance C_{th}=0.6nF at V_1=1.5V. As in previous experiments, a precision LCR Meter generates the BITx waveforms and measures the capacitance of the device $C(V_1)$ at times nT_S. The

decisions of the control algorithm and the data processing are implemented with a simple computer program. Fig. 5.5 provides a comparison between:

- the experimental results obtained with the capacitor (in blue),
- the discrete time simulation of the 5-th order DR model obtained in the characterization process (in red),
- and the analytical expressions in ((5.24)) and (5.26) obtained from the Sliding Mode analysis of the dynamics of the system when assuming an infinite sampling approximation (in green).

From all the results in Figure 5.5(a) it can be seen that, after a short initial transient of about 15-20 minutes, the target value is reached. Once the device reaches the target value, it is then maintained successfully during the entire experiment by applying an adequate sequence of voltage waveforms. This long-term phase where the control is maintained corresponds to the sliding phase in SMC and it can be seen as a straight line (in green) in Figure 5.5(a). On the other hand, Figure 5.5(b) shows the slow time evolution of the bit stream during the sliding phase. Similar behavior has been observed in other devices, in which this type of controls has been implemented [29, 20]. Finally, taking into account the similarity between the three curves in Figure 5.5(b), the infinite sampling approximation appears to be a very adequate approximation for understanding the control.

Furthermore, the evolution of the bit stream provides additional information about the behavior of the system. In the initial transient only BIT1s are applied to the device. This means that injection of positive charge is necessary to compensate an initial amount of net negative dielectric charge. This produces left-shifting of the CV until V_{target}=7.8mV is obtained. From then on, control is achieved and therefore the bit stream becomes progressively stabilized. Note that the bit stream shows a very long transient, which means that by the end of the experiment the steady-state has not completely been reached.

As shown in the Figure 5.5, the DR model simulation demonstrates perfect agreement with experimental data, thus validating DR as a powerful prediction tool for systems of this type. On the other hand, the analytical model allows straight interpretation of the system behavior in terms of sliding mode control. According to this, the initial transient is the reaching phase towards the control surface. Moreover, once the control surface is reached the system "slides" on it. In this sliding regime, the bit stream produced by the control loop coincides with the analytical predictions of eqs. (5.24) and (5.26), see Figure 5.5(b).

Adding disturbances

The extended analytical model provided by eq (5.29) has been used to predict the effect of external disturbances in the control experiment shown in Figure 5.5. To approach the charge generation due to ionizing radiation in a scenario similar to the experiment reported in the next section, the disturbance transients are divided into three steps: 1) no radiation (then $\phi = 0$) during the first 2 hours, 2) radiation, modeled as constant charge generation rate ($\phi = \beta t$), for the next 8 hours,

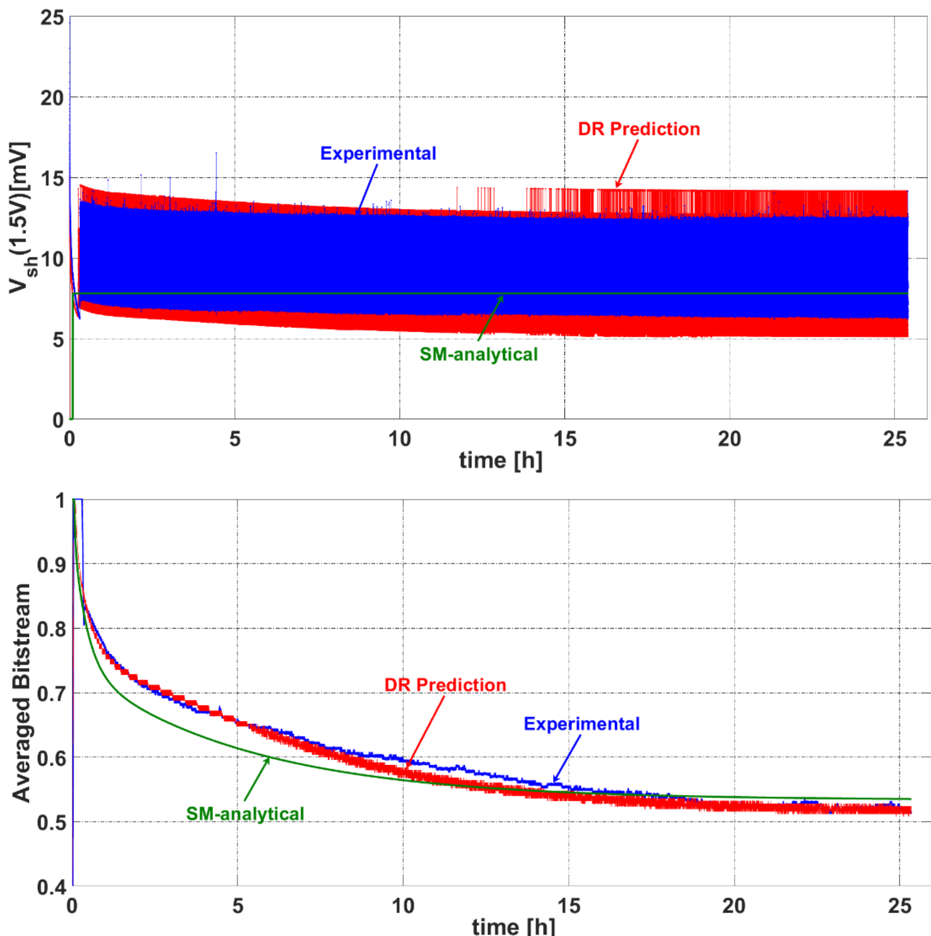

Figure 5.5: Comparison of experimental data (in blue) with SR (in red) and sliding mode control (in black) predictions for a MOS capacitor in which charge control was applied for 25 hours. a) Evolution of the voltage shift of the CV curve. b) Evolution of the bit stream provided by the control loop.

3) no radiation (then ϕ constant) for the last 6 hours. This disturbance model is compatible with trapped charge being generated by radiation that is never removed from the dielectric. The bit streams necessary to keep the same target voltage shift for four different values of the generation ratio β are shown in Figure 5.6. It is seen that the increasing amounts of positive charge generated between t=2 and t=10 hours are compensated by the control by increasing the number of BIT0s, which eventually increase the negative charge. When the disturbance episode ceases, the average bit streams always tend to stable-constant values. It is also seen that the charge generated by radiation is successfully compensated, but not removed.

The disturbance model developed would help understand the influence of external disturbances

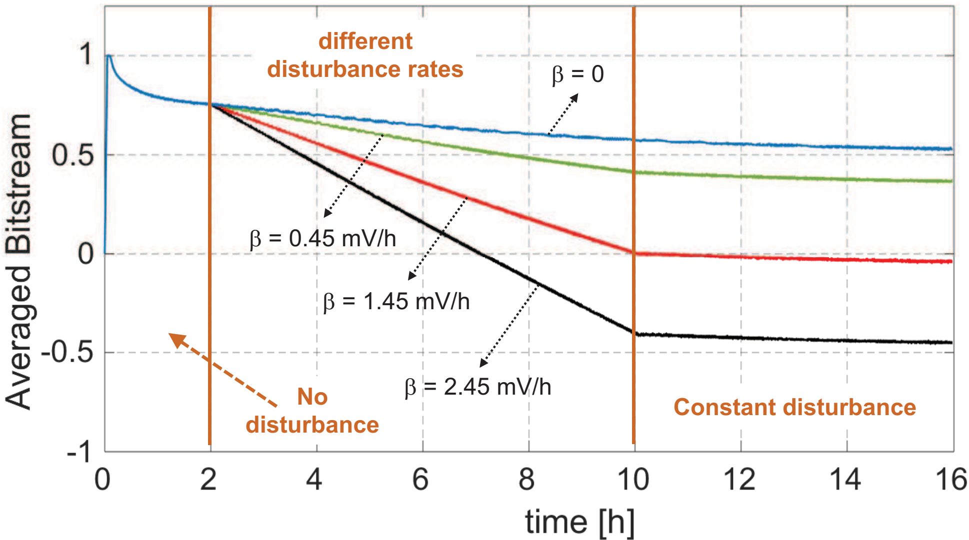

Figure 5.6: Evolution of the bit stream provided by the control loop, as predicted by the sliding analytical model, when a set of disturbance functions, with different charge generation rates (β), are applied for 8h during the experiment reported in Fig. 5.5.

on the closed loop control of the device. In particular, the model demonstrates the effect of ionization radiation dose rate on the amount of trapped charge generated (thus the amount of voltage shift) and the average bit streams needed to compensate it.

5.3.2 Experiment 2: Charge Control under Ionizing Radiation

This experiment investigates the effects of ionizing radiation on Al_2O_3 MOS capacitors operating under charge trapping control method. A specific objective is to check the goodness of the predictions of the sliding analytical model introduced when charging generated by the radiation occurs. To this effect, a pristine MOS capacitor has been irradiated with X-rays.

The device, DUT1, has been operated under sigma-delta control to achieve and maintain a given target capacitance C_{th}. Given the conditions of the experiment, a second-order loop has been used to improve the reliability of the control, avoiding potential effects such as the existence of plateaus that can be present in first-order loops [30]. In this case, the capacitance at voltage V_1 is sampled periodically and compared with C_{th} to obtain an error signal, which is then integrated and depending on the sign of the integral, either a BIT1 or BIT0 waveform is applied during the next sampling period.

The voltages used in BIT0 and BIT1 are V^+=5V, V^-=-3V and V_1=1V, whereas the target capacitance is C_{th}=0.498nF. The timing parameters are T_S=350ms and δ=1/3, being T_S smaller than the fastest time constant observed in the charging dynamics when these voltages are applied. The precision LCR Meter generates the BITx waveforms and performs the capacitance measurements

on the device.

The experiment starts with no radiation for 40 minutes, followed by X-ray irradiation for 8 hours (at a constant dose rate of 10 Gy/h), and an 8-hour final stage with no radiation. The top graph in Fig. 5.7 shows the evolution of the capacitance at V^0=1V of DUT1, which is under charge control. During the initial stage (radiation off) the control reaches the target capacitance C_{th} =0.498nF within a finite time, t=5min. Once this value is reached, it is successfully maintained during the rest of the experiment, irrespective of whether the radiation is on or off.

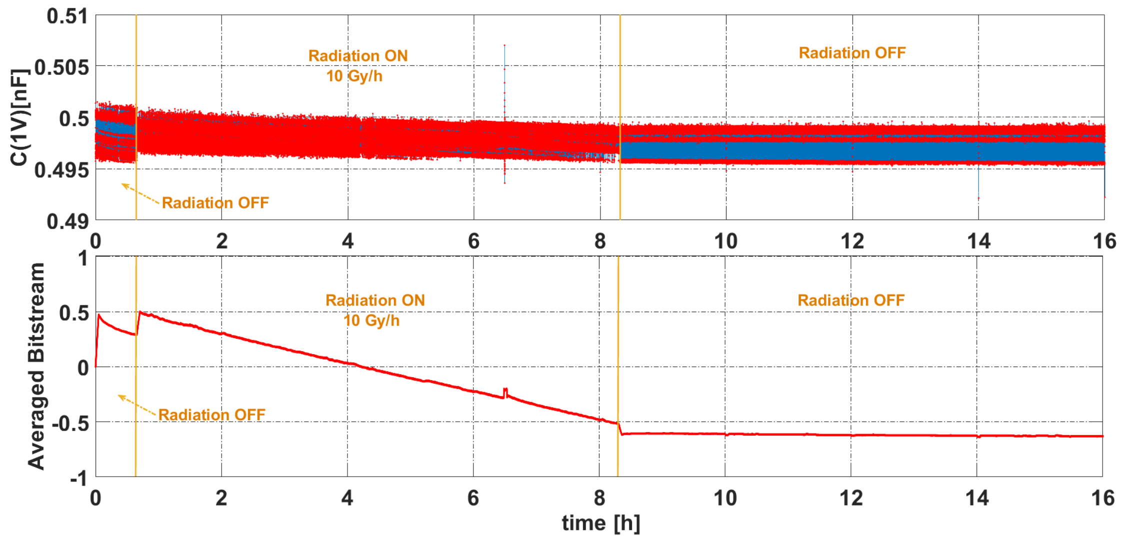

Figure 5.7: Evolution of the capacitance at $V_1 = 1$V (top) and of the control bit stream (bottom) of DUT1 during experiment 2. The device was under second order charge control with target capacitance C_{th} =0.498 nF.

The bottom graph in Figure 5.7 shows the evolution of the bit stream provided by the control loop. It illustrates how the control works; initially only BIT1s are applied, accumulating positive charge in the dielectric and moving the C-V to the left to reach C_{th}. During the irradiation stage (from t=40 min to t=8h 30min), the control increases the number of BIT0s, thus injecting more negative charge that compensates the accumulation of positive charge produced by the radiation. Once irradiation stops, the accumulated-remaining charge leads the bit stream to stabilize.

Finally, it can be observed that the experimental bit stream shown in Figure 5.7 matches with the predictions of the sliding control model summarized in Figure 5.6. As in experiment 1, this allows explaining the experimental results obtained in terms of a sliding mode controller: once the system reaches the target capacitance, or the control surface, the applied bit stream keeps the capacitance constant. Exposure to ionizing radiation generates an additional term, as in (5.28), that works as a mismatched disturbance, since the average bit stream is continuous. The changes in the dynamics generated by this disturbance clearly follow the predictions obtained in Section 5.2.4.

5.4 Conclusions

Diffusive representation has been used to characterize the dynamics of charge trapping in MOS capacitors, seen as time-varying diffusive systems in which time variability comes from the voltages applied to the devices. Experimental corroboration has been obtained. The obtained time-varying model has very good agreement with the experimental data obtained in both open and closed loop actuation strategies. Moreover, the state-space models are very well suited to describe the behavior of such diffusive systems under non-trivial controls, as sliding mode controllers.

Experiments involving ionizing radiation in MOS capacitors under charge control have also been presented. The results indicate that the trapped charge induced by radiation is not removed but successfully compensated by the control loop. Applying the theory of sliding mode controllers, the changes observed in the control bit streams due to radiation are compatible with the effect of mismatched external disturbances on the system dynamics.

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Chapter 6

Sigma-Delta Charge Control Applied to Other Devices

In this chapter, charge control methods similar to that used for MOS capacitors in Chapter3 have been applied to other devices such as eMIM capacitors and perovskite solar cells. The main objective here is to investigate the goodness of these controls to improve the performance or the reliability in these types of devices which can also suffer from charging effects. Accordingly, several preliminary experiments applying open loop and closed loop bias voltages to the devices have been performed, and the results are compared and discussed. These results are very promising and they give room to further investigation.

6.1 MIM Capacitors

Metal-insulator-metal (MIM) capacitors are one of the essential components in analog, RF and mixed signal ICs due to their low parasitic capacitances and high conductive electrodes [1, 2]. Several studies have been made to improve the capacitance density and reduce the leakage current for SOC (system-on-chip) applications [3, 4, 5] and have been fabricated conventionally using photolithographic technology with continuous dielectric layer between the metal layers.

In recent years, nanoparticles as dielectric material between the metal electrodes have been investigated to build an enhanced capacitor with improved capacitance values [6, 7, 8]. In [9], it has been reported that a metal-insulator-metal structure with SiO_2 nanoparticles fabricated using an electrospray technique (eMIM capacitor or supercapacitor) showed an increment in capacitance value by a factor of 4.4 compared to a continuous dielectric layer. The typical electrosprayed Metal-nanoparticles-Metal (eMIM) capacitor consists on several layers of dielectric nanospheres sandwiched between two metal electrodes (typically aluminium). This capacitance increment is mainly due to charge accumulation on the nanospheres surface. Also, increasing the number of layers of nanospheres by reducing their diameter results in an increase in the capacitance.

Figure 6.1 shows the schematic of the eMIM concept.

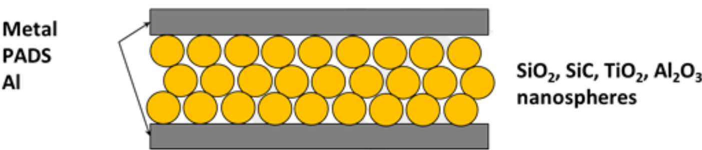


Figure 6.1: eMIM device concept: several layers of nanospheres sandwiched between two metal electrodes (typically aluminium).

The next section provides with the details of the fabrication process used to obtain an eMIM device with SiO_2 nanoparticles.

6.1.1 Fabrication Details

The eMIM devices used for the experiements have been fabricated at UPC. An electrospray technique has been used to deposit nanoparticles as insulator layer. The fabrication process involves the following steps [9]:

- The process starts with the deposition of a photoresist layer on a glass substrate. A mask has been used to remove photoresist and open an active area.
- A thick layer of Al film is deposited by sputtering.
- Lift-off technique is used to etch away the photoresist and the target bottom electrode remains on the top of the glass.
- An aqueous colloidal solution with $5\% SiO_2$ nanoparticles of $250nm$ diameter is placed in a reservoir connected to a needle. A high voltage has been applied between the needle and the bottom electrode to generate an aerosol of tiny droplets containing the nanoparticles that transport over the top of the substrate.
- Finally, a layer of Al (which is the top electrode) is deposited by sputtering through a shadow mask.

Figure 6.2 shows the cross section and the top view of the fabricated device schematically.

6.1.2 Implementing the Control Method

The main objective of our work involves investigating the effects of bias voltage on the charge redistribution in nanospheres which in turn generate changes in the impedance of the device. In this regard, we have initially performed constant polarization experiments on the device to study the evolution of the Nyquist plots with the application of bias voltages.

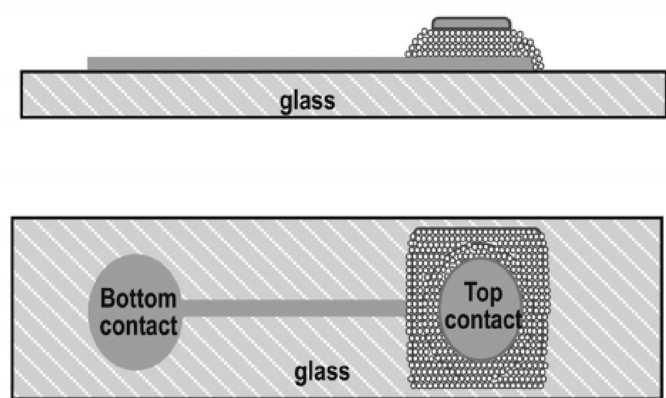


Figure 6.2: Schematic cross section and top view of the fabricated eMIM device [9].

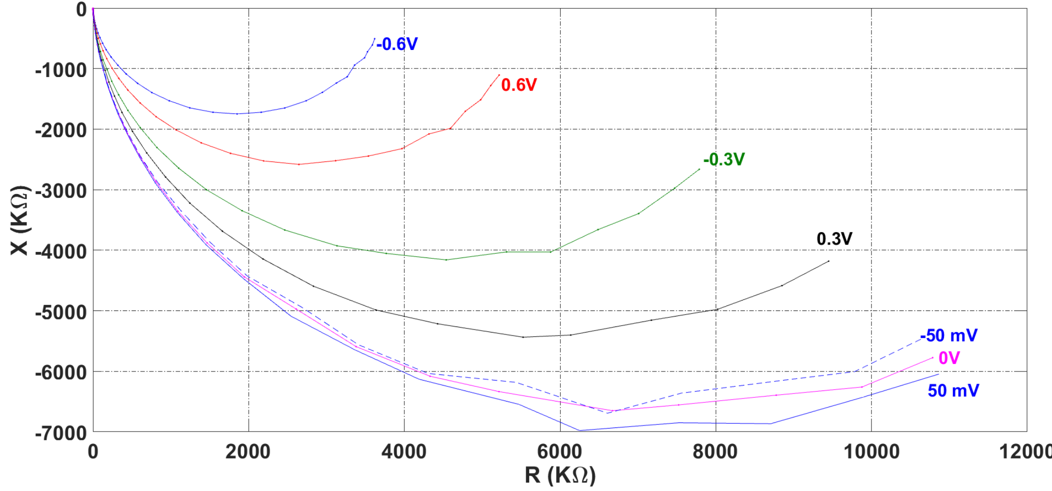


Figure 6.3: Nyquist plots of a SiO_2 MIM capacitor subjected to constant bias voltages.

The application of a constant bias voltages to the MIM capacitor results in the observation of two effects. The first one has a fast dynamics and generates changes in the impedance of the device which are reflected as changes in its Nyquist plot. This effect can be seen in Figure 6.3. Here, the Nyquist plots have been obtained consecutively in time, taken at different bias voltages. The differences observed in the impedance are attributed to the fast redistribution of electronic and ionic charge in the nanospheres, generating large swings in the resulting impedance.

On the other hand, the application of a constant bias for a long time implies slow change in the charge dynamics. To observe this effect, constant bias voltages have been applied periodically and drift in the differential capacitance was monitored. A 14-hour experiment has been made in which a constant bias of 0.6V was applied during the first 2 hours, -0.6V during the next 2h, repeating

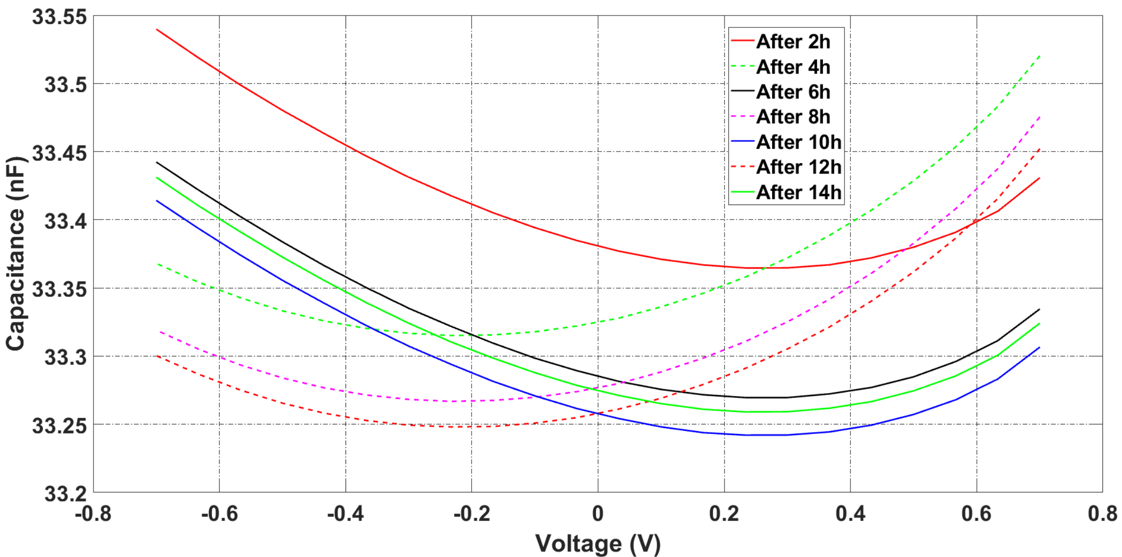


Figure 6.4: Successive CV curves measured every 2h at the end of constant bias voltages in a 14h experiment.

the sequence. The CV curves have been measured periodically at the end of each constant bias cycle and the plots can be seen in Figure 6.4.

The voltage shifts as a function of time corresponding to the displacements of the CV characteristic have been plotted as shown in Figure 6.5. As it can be observed the application of positive

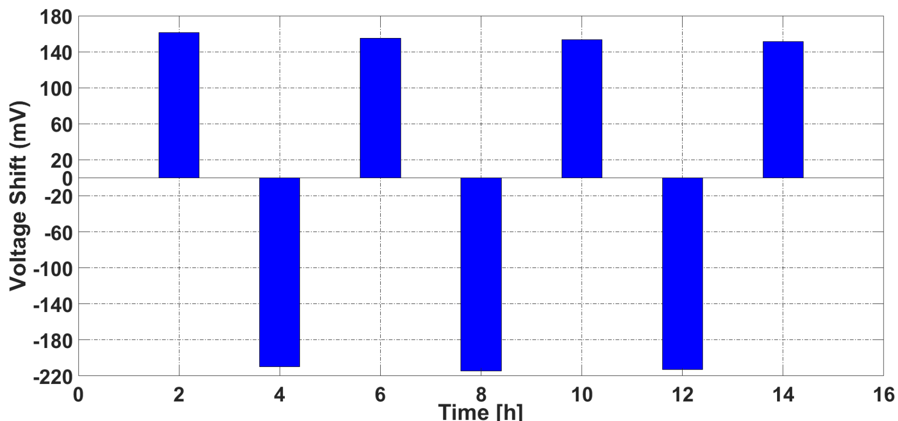


Figure 6.5: Position of the bottom of the CV, as a function of time, for the experiment in Figure 6.4. Application of positive bias tends to increase the voltage shift (displacement of the CV to the right). Application of negative bias tends to decrease the voltage shift (CV displacement to the left).

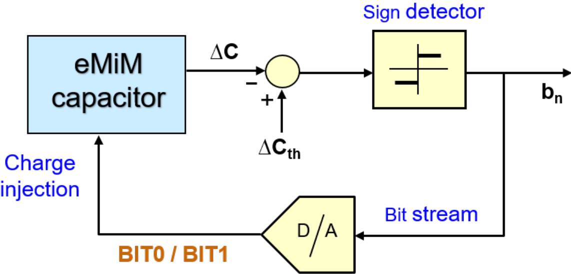


Figure 6.6: First order sigma-delta control of the voltage shift of the MIM device.

bias tends to increase the voltage shift (displacement to the right), whereas the application of negative bias tends to decrease the voltage shift (displacement to the left). This behaviour opens the possibility of designing a control based on polarity of the applied bias voltage.

We can notice that the CV characteristic of the MIM capacitor is quite similar to that of a MEMS switch in open state i.e. it has parabolic shape. This property of parabola function has been exploited in MEMS switches, where measuring the shift of the bottom of the CV curve gives the estimation of the voltage shift due to dielectric charging [10, 11]. This technique, referred to as center-shift method, has the advantage of being minimally invasive since voltage levels applied are well below the pull-in range. A new strategy based on this method has been proposed [12, 13] to monitor the CV shifts through quasi differential capacitance measurements. Here, change of pull-in voltage has been obtained from the variation of capacitance, ΔC, measured at two voltages of different polarity in close instants of time.

In this work, we have used similar control strategy based on sigma-delta modulation as in [13], as shown in Figure 6.6 . Here, the main objective of the control is to maintain the desired state or parameter of a system by periodically monitoring the state and applying an appropriate sequence of control signals. In this case of MIM capacitors, the state/parameter to be monitored and controlled is the differential capacitance, rather than the capacitance at a single voltage reference value. The control circuit evaluates the capacitance values at two different voltage levels at periodic instances nT_s, and applies an adequate sequence of positive or negative voltage pulses during the next sampling intervals $(n+1)T_s$ using the feedback loop to maintain it around a desired value.

The design of actuation voltage waveforms, BIT0 and BIT1, is shown in Figure 6.7(a). These waveforms have a total duration of T_s with two different voltage levels, V^+ and V^-. For BIT0/BIT1, V^-/V^+ is applied during most of the time, $(1-\delta)T_s$, whereas V^+/V^- is applied for a short time interval, δT_s. The parameters V^-, V^+, δ, T_s have been chosen appropriately such that the BIT0 and BIT1 waveforms generate horizontal shifts of C-V curves of different sign. In case of MIM capacitor, application of BIT0 waveform results in the left shift of the C-V curve while applying BIT1 waveform shifts it to the right.

The illustration of how the closed loop control works in this case is shown in Figure 6.7(b). The differential capacitance, ΔC, has been obtained from the capacitance measurements preformed

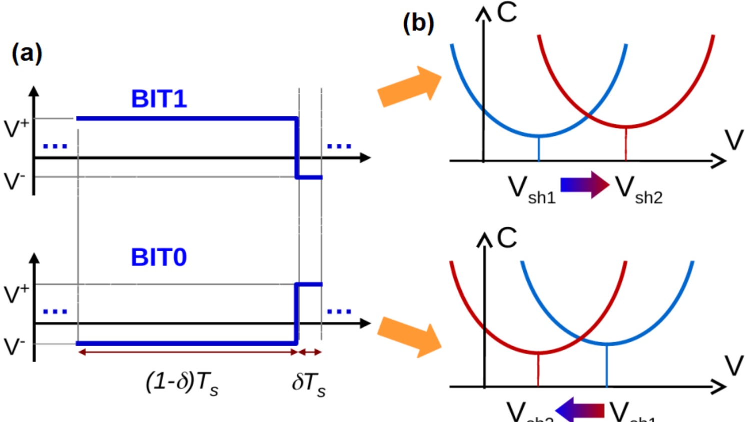


Figure 6.7: (left) BIT1 and BIT0 actuation sensing waveforms. Application of BIT1 (BIT0) waveforms tends to increase (decrease) the voltage shift of the C(V) characteristic of the device [14].

at times $(n-1)T_s + (1-\delta)T_s$ and nT_s corresponding to the application of V^+/V^- and V^-/V^+ respectively for BIT1/BIT0 symbols. Comparing this value with the desired threshold capacitance value ΔC_{th}, the next symbol,$BITx$, to be applied is decided as,

$$BITx = \begin{cases} BIT1, & \Delta C - \Delta C_{th} < 0, \\ BIT0, & \Delta C - \Delta C_{th} > 0, \end{cases} \tag{6.1}$$

In general, the relation of MIM capacitance with voltage is parabolic and therefore can be modeled as:

$$C(V,t) = \alpha(V - V_{sh}(t))^2 + C_0 \tag{6.2}$$

where the parameter α is obtained by fitting the above equation with measured C-V curve, V_{sh} is the amount of voltage shift and C_0 is the minimum capacitance value.

Since the small changes in temperature or humidity could result in the generation of vertical displacements in the CV curve, these influences have been accounted for the slow time variation in $C_0(t)$. In order to minimize these effects, the capacitance measurements are taken at two different points of the CV curve at the end of the sampling period in close instants of time t and $t+\Delta t$ such that Δt is smaller than the time constants involved in the dynamics of the device. In such a case, we can write $C_0(t) = C_0(t+\Delta t)$. Suppose the capacitance values obtained by applying $V^+ > 0$ at time t is $C(V^+)$ and $V^- < 0$ at time $t+\Delta t$ is $C(V^-)$, the differential capacitance ΔC obtained at the end of the sampling period can be written as:

$$\begin{aligned} \Delta C &= C(V^+) - C(V^-) \\ &= \alpha[(V^+)^2 - (V^-)^2] - 2\alpha V_{sh}[V^+ - V^-] \end{aligned} \tag{6.3}$$

From equation (6.3), it is obvious that ΔC is independent of the variations in $C_0(t)$. Thus it is possible to eliminate the effects of vertical shifts during the measurements.

Now, in the next sections, we apply open loop stress ($BIT0/BIT1$) to the device to monitor the drift in the differential capacitance with time and implement the charge control scheme that allows controlling the time evolution of this drift. This entails the possibility of controlling the impedance of the device.

6.1.3 Experimental Results and Discussion

Open loop Experiments

We have observed in the previous section that the application of a constant bias voltage to the devices generates drifts in the impedance. In this section, a set of open loop experiments have been performed on the capacitor where the device is excited with a constant BIT voltage waveforms with periodic monitoring of the differential capacitance, ΔC. Extensive measurements have been made in order to optimise actuation waveforms by choosing optimal values for the actuation voltages (V^+ and V^-), the value of δ and the sampling period (T_S). Accordingly, $BITx$ waveforms with voltage levels $V^+ = 0.6V$, $V^- = -0.6V$, and a sampling time period, $T_s = 1s$ with $\delta = 1/5$ have been chosen.

Figure 6.8 shows the evolution of $\Delta C(t)$ for the continuous application of $BIT0$ and $BIT1$ waveforms, in time intervals of 4h. As it can be seen, $BIT1$s tend to decrease $\Delta C(t)$, therefore increasing the associated voltage shift, whereas the opposite behaviour can be noticed with the application of $BIT0$ waveforms. These results are consistent with those in Figure 6.5, where the continuous application of 0.6V increased the voltage shift (and the reverse behaviour was obtained for -0.6V). The successive CV measurements have been interspersed each 2h during this 16h experiment, allowing to directly measure the resultant voltage shift. These results have been plotted in Figure 6.9.

Now, Figure 6.10 shows the Nyquist plots of the same experiment, measured every 4h. The inset shows the zoom of the final part of the Nyquist plots. The order to the initial plot is (70mV $\rightarrow$ 40mV $\rightarrow$ 0V). The application of BIT1s tends to impose this order in the Nyquist plot: (70mV $\rightarrow$ 40mV $\rightarrow$ 0V). The application of BIT0s tends to impose either (40mV $\rightarrow$ 0V $\rightarrow$ 70mV) or (0V $\rightarrow$ 40mV $\rightarrow$ 70mV). This means that applying BIT0s (which is equivalent to apply a negative voltage most of the time) tends to decrease the Nyquist plot for 0V, whereas the opposite behaviour is obtained for BIT1.

From these open loop experiments, it is obvious that BIT0 and BIT1 waveforms are effective in generating voltage shifts of different sign. These voltage shifts can be understood as small shifts of the Nyquist plots taken at any bias voltage. In our case, since the observed shifts in the CV curves are small ($< 100mV$), the effect can be seen more easily when the Nyquist plots are taken with low bias voltages (voltages of the order of the shifts in the CV curves). In our case, then, the Nyquist plots at 0V, 40mV and 70mV are reordered.

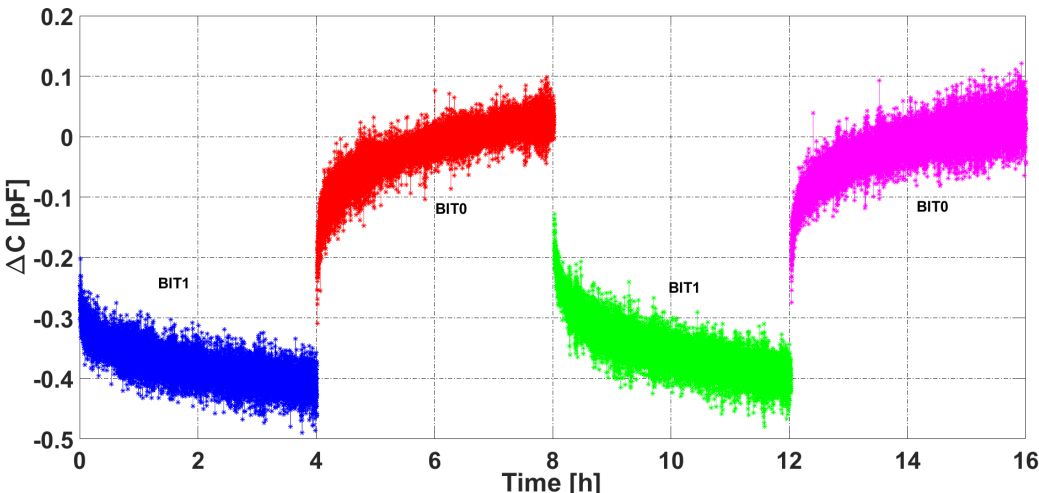


Figure 6.8: Evolution of $\Delta C(t)$ for an experiment in which BIT1 and BIT0 waveforms were alternated in intervals of 4h each. Capacitance is measured at 10KHz.

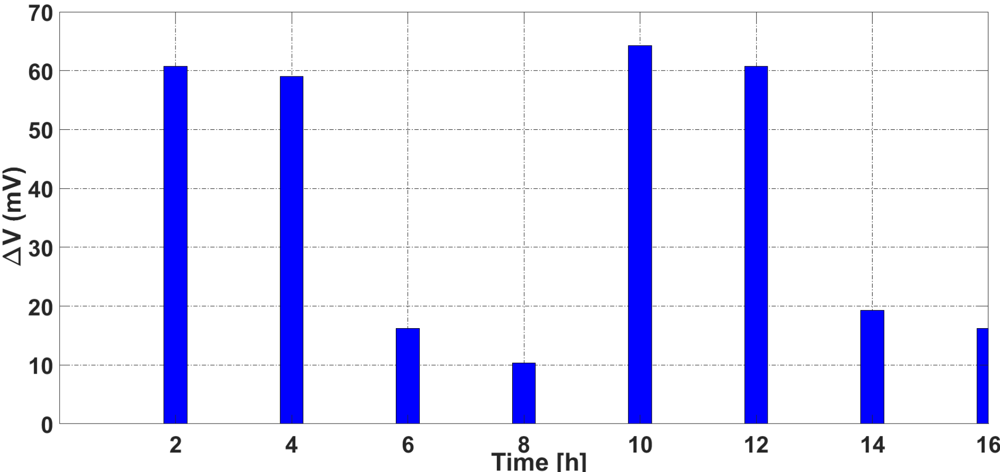


Figure 6.9: Voltage shift measured each 2h in the experiment of Figure 6.8. BIT1 waveforms increase the voltage shift whereas BIT0 waveforms decrease it.

Closed loop Experiments

The 1st order control method described in Section 6.1.2 has been applied to the MIM capacitor structure. In order to minimize the effects of temperature and/or humidity variation, the device is maintained at a constant temperature on a thermal chuck using a STC200 temperature controller. A precision LCR Meter E4980A has been used to perform periodic capacitance measurements and

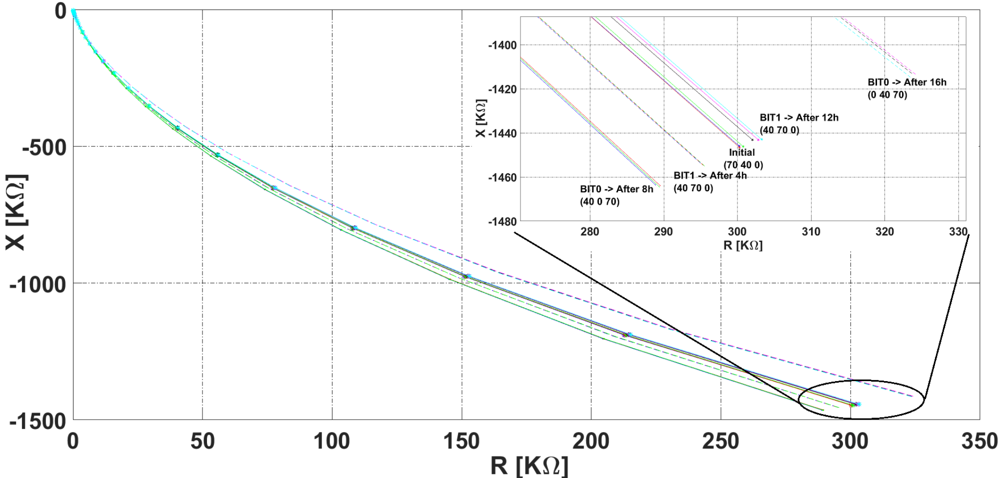


Figure 6.10: Groups of Nyquist plots at bias voltages: 0V, 40mV and 70mV. Each group of three Nyquist plots is measured at time intervals of 4h. (Inset) Zoom of the nyquist plots. The Nyquist plots change their order depending on the history of the actuation waveform applied.

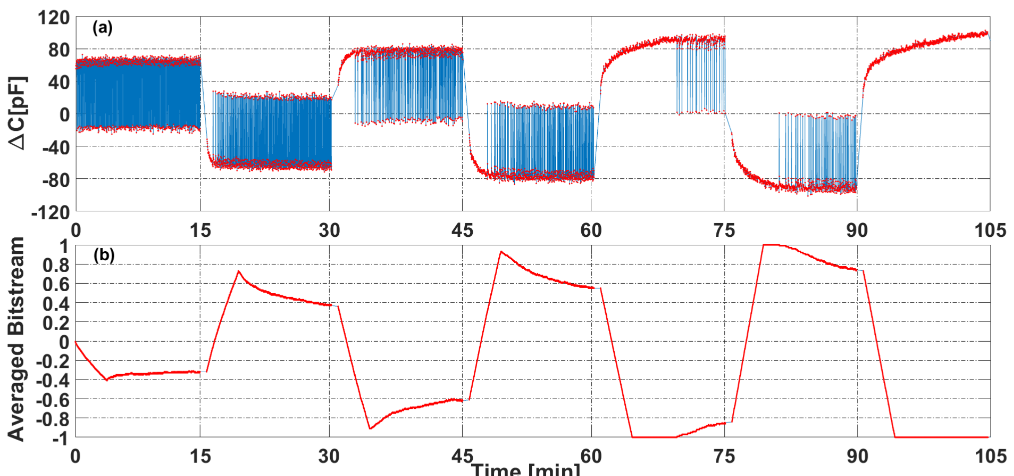


Figure 6.11: a) Time evolution of differential capacitance, ΔC measured when the control method is applied. The parameters used are $V^{+} = 0.6V$, $V^{-} = -0.6V$, $T_s = 1s$, and $\delta = 1/5$. b) The average bitstream extracted at the end of each control loop experiment.

generate the BIT waveforms. The amplitude of AC signal used is 500mV and the test frequency is 100KHz. It has been observed from the open loop experiments that the continuous application of $BIT1$ symbols would shift the CV curve to the left while the application of $BIT0$ symbols would result in the right shift.

The first experiment has been carried out for 105 min with seven different target values, each

lasting for 15 min. A constant temperature is maintained to minimize the vertical displacements in the CV curves. Figure 6.11 shows the evolution of differential capacitance as a function of time taken periodically at the end of each sampling time, nT_s. The high mobility of the ions results in the fast dynamics of the control parameter with the applied BIT waveforms. A transient can be observed at the beginning of each interval where the capacitance either increases or decreases with the application of $BIT0/BIT1$ waveforms until it reaches the desired target value. Once the target value has been reached, the control loop injects appropriate BIT sequences to keep it constant. This can be observed using the average bitstream generated during the control. It can be seen that each time a new target has been chosen, the feedback loop applies a continuous sequence of $BIT0/BIT1$ waveforms until it reaches the target level, after which a slow evolution of the average bitstream is observed. However, the capacitance level set at t=90 min is so large that the feedback control loop could not reach the target within the limited table available. In other words, the control becomes saturated (only BIT0s are applied) but the target value is not achieved.

Figure 6.12 shows the horizontal displacements of the CV characteristics of the device obtained at the end of each control experiment. The corresponding voltage shift values measured with respect to 0V are shown in Figure 6.13.

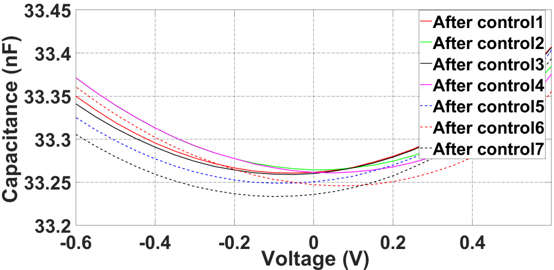


Figure 6.12: CV characteristics obtained at the end of each control. The ac frequency used is 100 KHz.

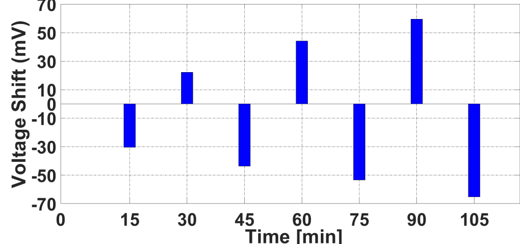


Figure 6.13: Voltage shifts corresponding to the CV curves obtained at the end of each control segment.

The Nyquist plots obtained at the end of the control loop are also shown in Figure 6.14. We can notice that the positions of Nyquist curves at the end of each control segment correspond to the voltage shifts obtained in Figure 6.13.

Now, a long experiment has been scheduled with seven different targets each lasting for 2h. The time evolution of ΔC measured at periodic sampling time intervals is plotted in Figure 6.15. As observed in the previous closed loop experiment, the feedback loop applies either only a $BIT0$ or only a $BIT1$ waveform during the initial transient phase, and once it reaches the target level, injects an appropriate sequence of $BIT0 - BIT1$ waveforms to maintain the threshold value. The slow evolution of average bitstream gives the voltage levels required to maintain the control during the experiment.

Figure 6.16 shows the horizontal displacements of the CV characteristics obtained at the end of each target control step. The corresponding voltage shift values measured with respect to 0V are shown in Figure 6.17.

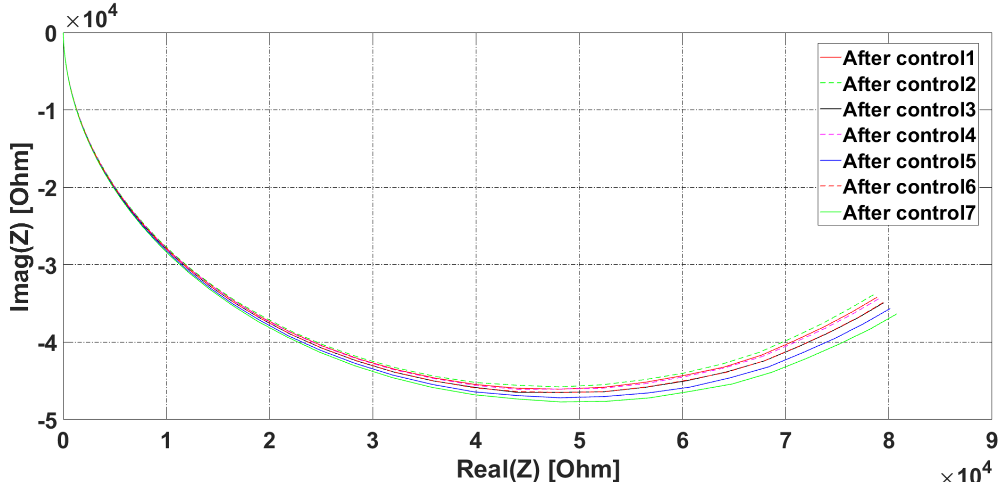


Figure 6.14: Nyquist plots measured at the end of the control segments.

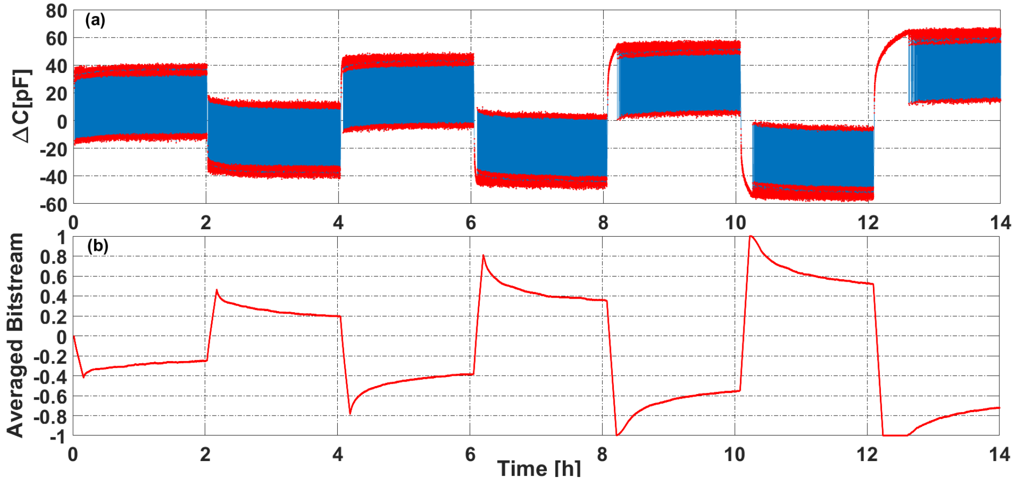


Figure 6.15: a) Time evolution of differential capacitance, ΔC measured when the control method is applied. The parameters used are $V^+ = 0.6V$, $V^- = -0.6V$, $T_s = 1s$, and $\delta = 1/5$. b) The average bitstream provided by the control loop during the experiment.

6.2 Perovskite Solar Cells

In recent years, the use of perovskite materials in photovoltaic, optical and superconductor applications has experienced considerable growing interest. For instance, perovskite solar cells combine good performance (i.e. a spectacular 8% efficiency improvement was obtained in just three years [15]) reaching an efficiency of 22.1% [16, 17, 18] with a relatively cheap manufacturing process. However, serious reliability problems slow down the rise of this technology, being the biggest prob-

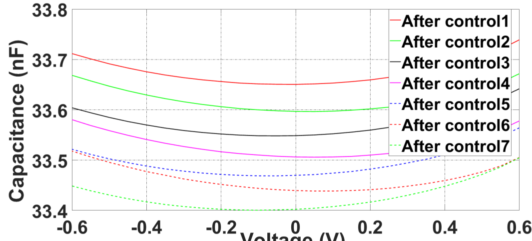


Figure 6.16: CV characteristics obtained at the end of each control. The ac frequency used is 100KHz.

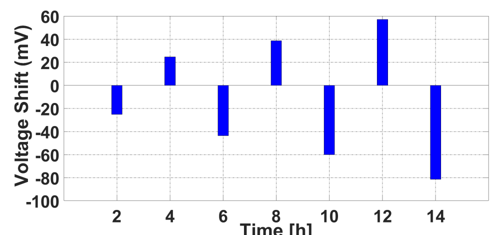


Figure 6.17: Voltage shifts corresponding to the CV curves obtained at the end of each control segment.

lem the degradation of the material [19, 15]. There is wide consensus in identifying environmental conditions -oxygen, temperature [20], humidity [21, 22], light [23] and electrical stress [24, 25] as the factors responsible for the degradation, but there is still little understanding on the physical mechanisms involved.

Although most works try to improve perovskite stability varying the fabrication process or the chemical composition of the materials used, a radical new approach is implemented here. It consists in using a sigma-delta loop to control the charge trapped in the perovskite, allowing to place the J-V of the device at a desired-stable position. This strategy, inspired in that used for MOS capacitors, may open a new way to mitigate perovskite degradation. According to this, in this work charge control is applied to perovskite solar cells that suffer noticeable degradation effects. Let us note that the objective here is to investigate the feasibility of charge control to stabilize the J-V of the device. Specific application targets such as mitigating the degradation of key photovoltaic parameters will be the objective of future work.

6.2.1 Fabrication Details

The perovskite solar cells used in the experiements have been fabricated at ICFO (Instituto de Ciencias Fotonicas). The devices were fabricated on patterned ITO substrates and the process involves the following steps:

- The substrate is covered with a 2.5%wt in methanol TiO_2 nanoparticle precursor (20%wt in water). The precursor was previously mixed with 2.5%wt of Ti diisopropoxidebis (acetylacetonate).
- Then, the perovskite (methylammonium lead iodide/$CH_3NH_3PbI_3$/$MAPbI_3$) was deposited as in [26], without adding the triiodide solution.
- Next, a 72.3 mg/ml 2,2',7,7'-Tetrakis [N, N-di(4-methoxyphenyl) amino]-9,9'-spirobifluorene (Spiro-OMeTAD) solution in chlorobenzene with 17 μL of a 520 mg/mL bis (trifluoromethylsulfonyl) amine Li salt solution in acetonitrile and 29 μL of 4-tert-butylpyridine was spin-coated on top of the perovskite.

- Finally, gold was thermally evaporated and patterned to form the top electrode.

The resulting stack of layers is: ITO(140 nm), TiO_2(40 nm), perovskite(500 nm), Spiro-OMeTAD(200 nm) and Au(60 nm), with 0.06 cm^2 of active area. The schematic of the fabricated device is depicted in Figure 6.18

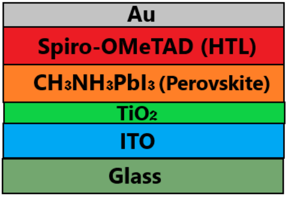


Figure 6.18: Schematic view of the fabricated perovskite solar cell.

Now, the control scheme based on sigma-delta modulation is implemented on the perovskite device. The objective of this control method is to set the Current density-Voltage (J-V) curve to a desired position. This is done by applying the voltage waveforms BIT0 and BIT1 shown in Figure 6.19. In BIT0/1, a voltage V_0/V_1 is applied for $(1-\delta)T_S$, while V_C is applied for a short time δT_S, $0 < \delta < 1$. As shown later, V_0 and V_1 are chosen so that their application produces opposite J-V shifts. According to this, the control method consists in sampling the current at the control voltage $J(V_C)$ at each BITx end. Depending on whether $J(V_C)$ is above or below a previously given target J_{th}, either a BIT0 or a BIT1 is applied in the next sampling period.

To investigate the suitability of the control method proposed, open loop and closed-loop control experiments have been performed both in dark and illumination as described in the next section.

6.2.2 Experimental Results and Discussion

A Keysight 2912A SMU has been used to generate the voltage waveforms and to perform the periodic current measurements. The sampling time T_S is chosen such that the voltage switching within the BITx waveform, necessary to measure $J(V_C)$, has fairly unnoticeable effect on the state of the device. V_C is chosen to ensure sufficient current sensibility.

Figure 6.20 shows the J-V curves measured in a pristine device in dark and under illumination. Noticeable differences between forward and reverse scans can be observed. The solar cell devices fabricated using perovskite materials differs from conventional silicon devices in that they show discrepancy in the J-V measurements with voltage scan direction and scan rate [27, 28]. This is due to the slow charge redistribution owing to slow charge collection in the perovskite, which results in preventing the fast response to the applied voltage scan [28].

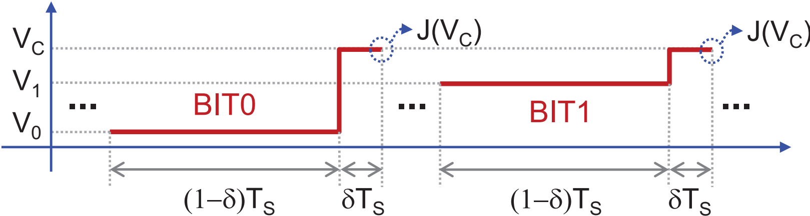


Figure 6.19: BIT0 and BIT1 voltage waveforms used in the control. The current at the control voltage $J(V_C)$ is sampled at the end of each waveform.

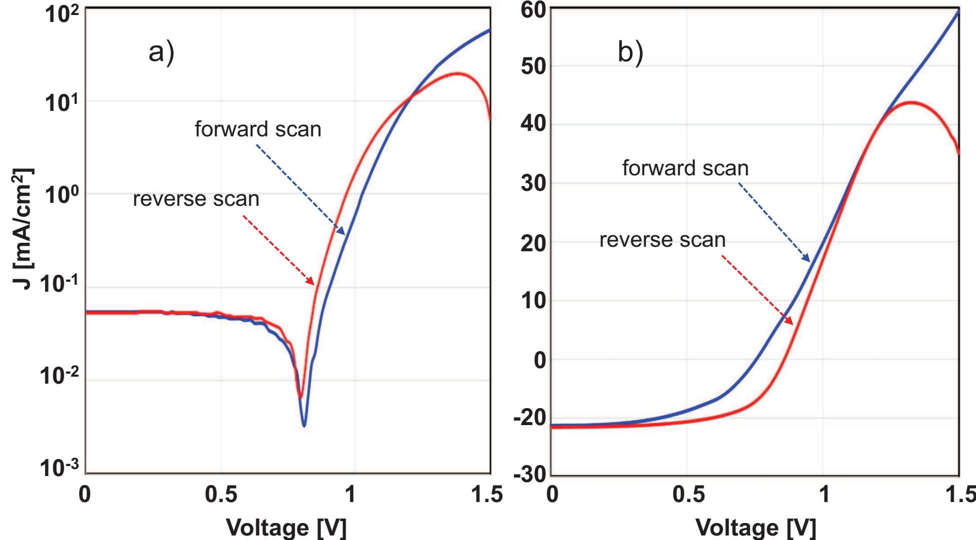


Figure 6.20: J-V characteristics of a pristine device in dark (a) and under illumination (b). The scan rate is 440 mV/s.

Experiments in dark

In the first experiment, an open loop stress (consisting in applying either only BIT0 or only BIT1 waveforms) has been applied to the device in order to monitor the evolution of $J(V_C)$. As shown in Figure 6.21(a), application of a BIT0 stress produces an initial sharp increment in the current, and then it slowly appears to decrease towards a stable value. That is, the continuous application of BIT0s produces a shift in the J-V characteristic to the right. On the other hand, applying BIT1 waveform produces left shifts of the J-V, as shown in Fig. 6.21(b). Summarizing, the application of BIT0 and BIT1 waveforms results in opposite shifts of the J-V curves.

Since no photogenerated carriers are present during this experiment, the possible ion species present in the perovskite layer are $CH_3NH_3^+$, Pb_2^+, and I^- [29]. While I^- ions are predicted to

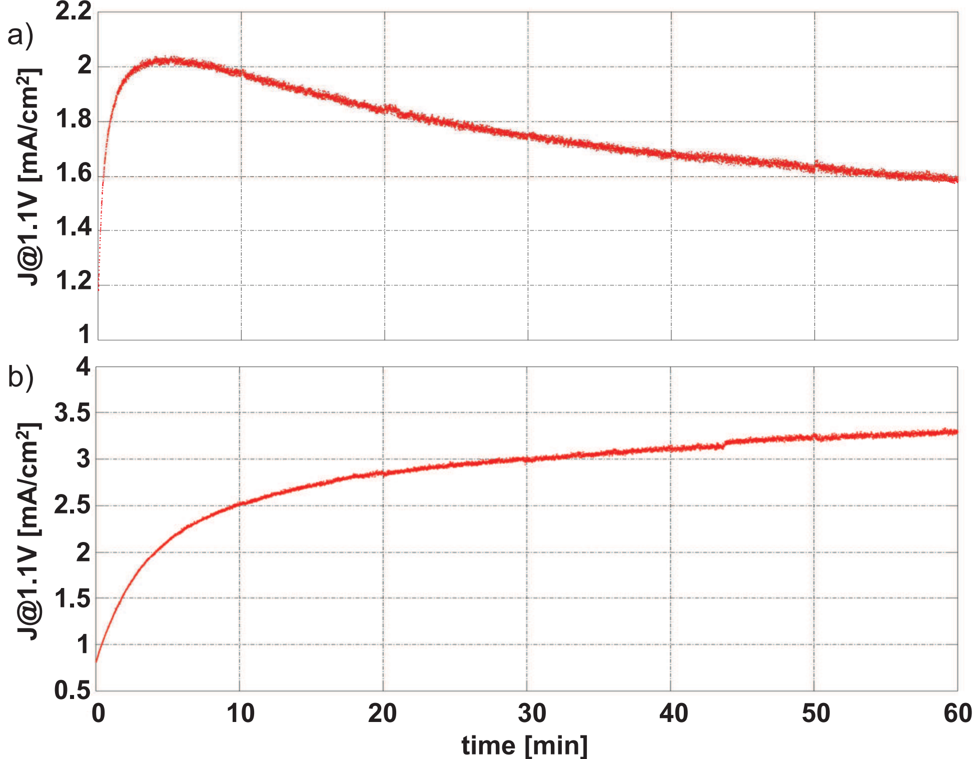
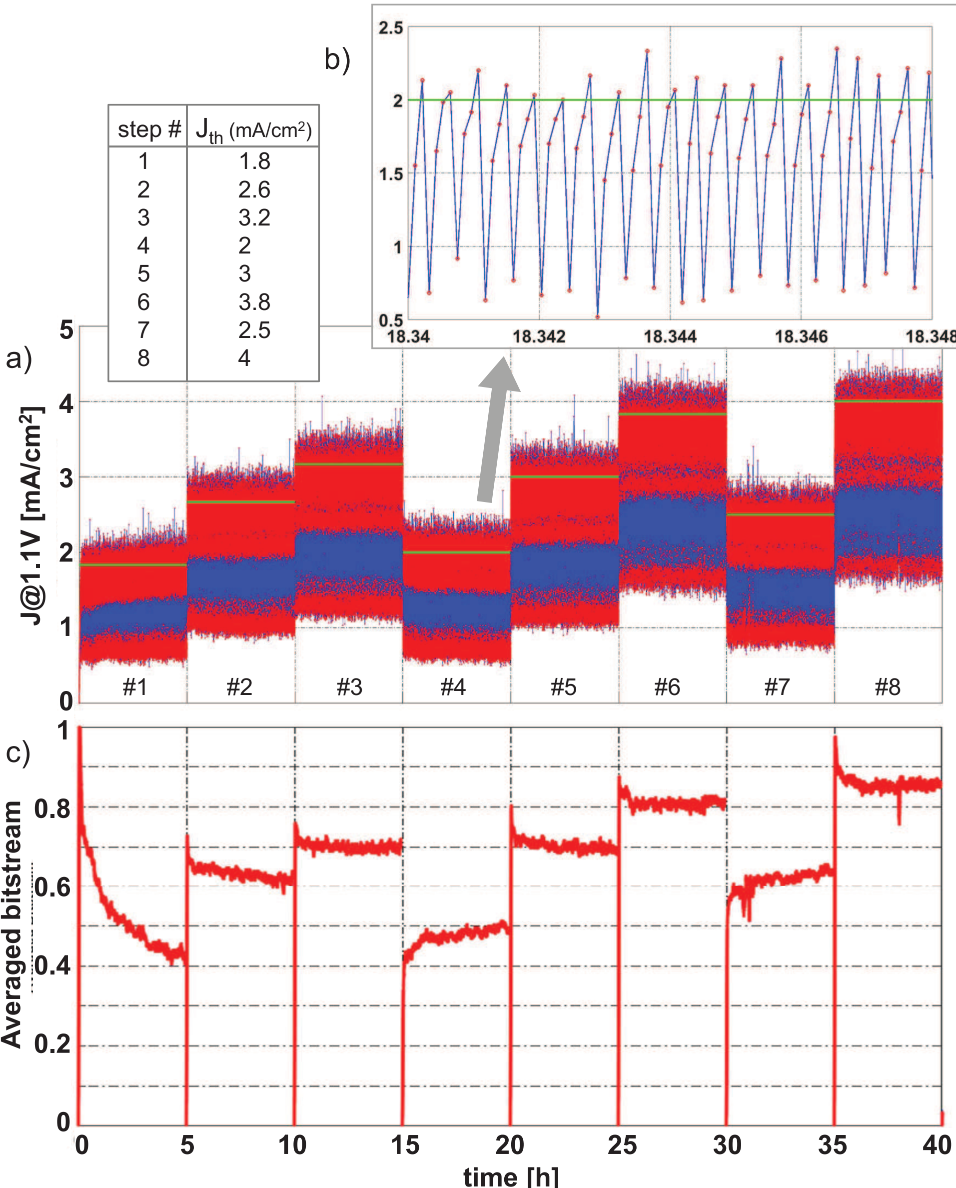


Figure 6.21: (a) Evolution of the current monitored at the control voltage when only BIT0s (a) or BIT1s (b) are applied to the device. BIT0/1 parameters: T_S=400ms, δ=1/3, V_0=0.3V, V_1=0.7V, V_C=1.1V. To set comparable initial conditions, the device was at 0V bias for 15min before each BITx stress.

be dominant due to their low activation energy [30], the fast migration of these ions would not respond to the sampling times used here. Besides, $CH_3NH_3^+$, and Pb_2^+ ions would be probably responsible for the slow dynamics observed, since their migration times are of the order of tens of ms to minutes [31] compatible with the sampling times involved in the control method.

In the next experiment, closed loop control has been applied to check the effectiveness of the control method by applying a sequence of eight 5h steps, each with a different target, J_{th}. The time evolution of $J(V_C)$ and the bit stream genereated during the control were continuously monitored, and a fast J-V measurement was made at the end of each control step. The J_{th} values and the evolution of $J(V_C)$ during the experiment have been depicted in Figure 6.22(a). We can notice that all target levels have been achieved succesfully: at each step, the current reaches very fast the target level, then the control loop keeps the current around J_{th} by applying an appropriate sequence of BIT0s and BIT1s. The inset of Figure 6.22(b) shows a zoom of the evolution of $J(V_C)$ during step 4. Each time $J(V_C)$ is below J_{th}=2mA/cm^2, the feedback loop applies BIT1s until the current goes above J_{th}. Once this happens, a BIT0 is applied to decrease the current below J_{th}.



step #	J_{th} (mA/cm²)
1	1.8
2	2.6
3	3.2
4	2
5	3
6	3.8
7	2.5
8	4

Figure 6.22: (a) Evolution of $J(V_C)$ while control is applied with the target values J_{th} listed in the table. The green line represents the target current levels. (b) Zoom of $J(V_C)$ for a short time interval within step 4. (c) Average bit stream provided by the control loop during the experiment. BIT0/1 parameters: V_0=0.25V, V_1=0.75V, V_C=1.1V, T_S=400ms, δ=1/3.

This behavior is typical of 1st-order sigma-delta controllers [32]. The noticeable large deviations of the instantaneous current values from the target levels could be attributed to the fast dynamics of

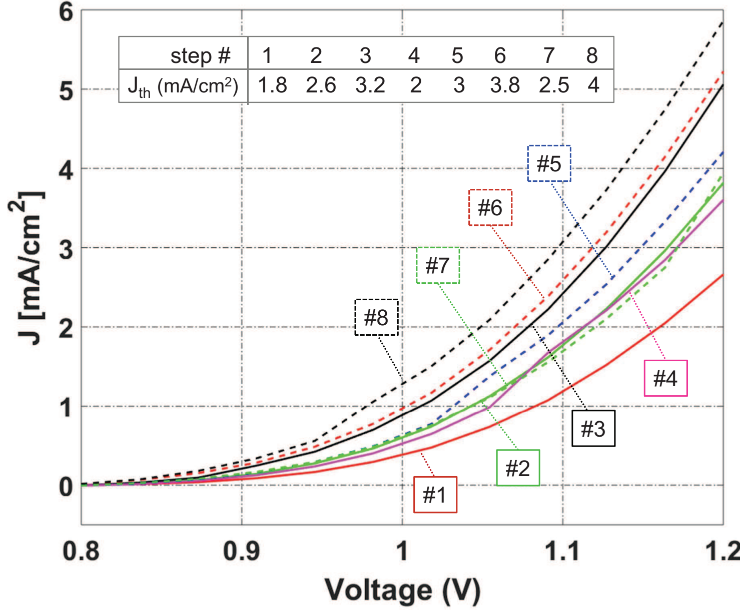


Figure 6.23: J-V curves obtained at each step end in the experiment of Fig. 6.22. The instantaneous current deviates from the desired value due to the J-V measurement itself.

the current due to the small time constants involved in the control waveforms, when compared to the migration times of the mobile ions [31, 33].

The average bit stream generated by the control loop is plotted in Figure 6.22(c). It can be seen that higher the level of J_{th}, more the injection of BIT1s, and that the bit stream exhibits slow time evolution once the target levels are reached. The *fall to zero* distortions of Figure 6.22(c) are due to the J-V measurements made at each control step end. The curves thus obtained, plotted in Figure 6.23, show that the control allows to set and maintain successfully the J-V around the desired targets.

Effect of sampling time on control

In this section, the influence of T_S on the effectiveness of the control has been investigated. To this end, control was applied with J_{th}=3 mA/cm^2 and two values of T_S in 4h steps. Figure 6.24 shows the evolution of $J(V_C)$ and the average bistream. A plateau-like behavior is clearly observed during the control with T_S=1s: the average bit stream is stacked at zero -having alternate sequence of BIT0s and BIT1s- while $J(V_C)$ has noticeable variation and, therefore, no control is obtained. In perfect agreement with sigma-delta theory [32], reducing the sampling time mitigates this undesired effect, as seen for the case of T_S=400ms.

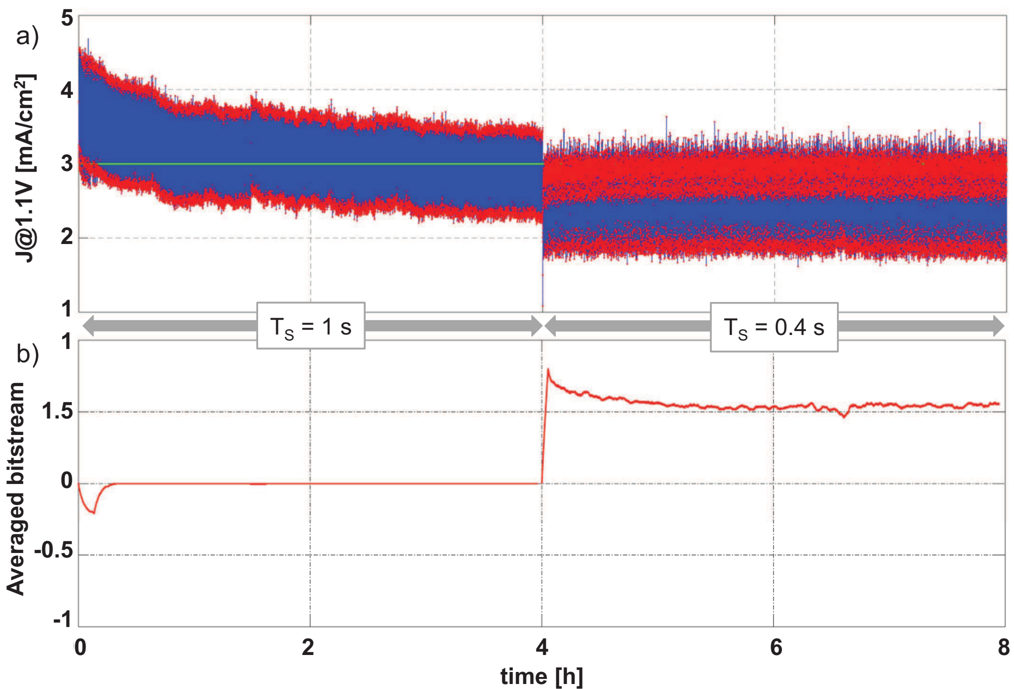


Figure 6.24: Evolution of $J(V_C)$ (a) and average bit stream (b), while control is being applied with J_{th}=3 mA/cm^2 (green line) and two values of T_S. Other BIT0/1 parameters: V_0=0.25V, V_1=0.75V, V_C=1.1V.

Experiment under illumination

In this section, the sigma-delta control has been applied to the device under illumination. Following a similar strategy than in the experiment of Figures 6.22 and 6.23, several different values of J_{th} were applied in 1h steps, with fast J-V measurements made at the end of control steps. Figure 6.25(a) shows the evolution of $J(V_C)$ and of the average bit stream. Each time J_{th} changes, the control loop has been successful in reaching and maintaining the new desired level, although the control is lost due to a fractal-like episode for some time in step 7.

Photo-excitation of $MAPbI_3$ creates iodide vacancies that allow the migration of I^- ions. With the application of an external bias under illumination, redistribution of these ions occurs causing the ions move towards the electrodes depending on the applied bias. Applying BIT0 waveform causes I^- ions to move towards TiO_2 layer also referred to as ETL (electron transport layer) while MA^+ ions migrate towards spiro-OMeTAD or HTL (hole transport layer), resulting in the creation of a barrier for the charge carriers at the contacts. On the other hand, applying BIT1 waveforms causes ions to move in the opposite direction thus improving the charge carrier extraction at the contacts.

Finally, Figure 6.26 shows the sequence of J-V curves measured at the end of each control step.

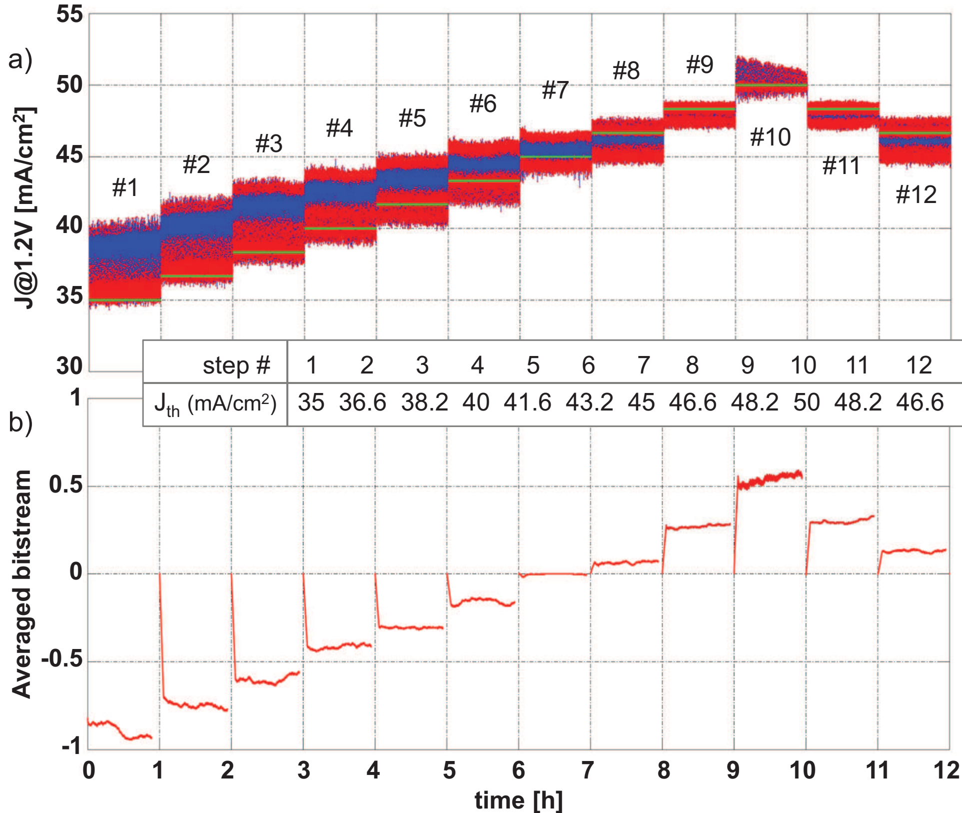


Figure 6.25: (a) Evolution of $J(V_C)$ while control is being applied under illumination with the target values J_{th} listed in the table. The green line represents the target current levels. (b) Average bitstream provided by the control loop during the experiment. BIT0/1 parameters: V_0=0.25V, V_1=0.75V, V_C=1.2V, T_S=400ms, δ=1/3.

The same complementary behavior seen when applying BIT0s or BIT1s in dark is also observed under illumination, therefore enabling the control loop to place the J-V to previously given target positions. Thus the proposed control allows to displace the J-V of the device and maintain it at a desired point, even in dark or illumination conditions.

6.3 Conclusions

We have investigated the influence of bias voltage on charge dynamics of a MIM structure with nanoparticles. The constant application of a bias voltage to the MIM device generates drifts in the impedance and presents a double dynamics: a fast one in which the Nyquist plot changes instantaneously and a second one, in which the application of the bias for long times (hours, for example) generates small drifts in the Nyquist plots. We have observed that it is possible to control

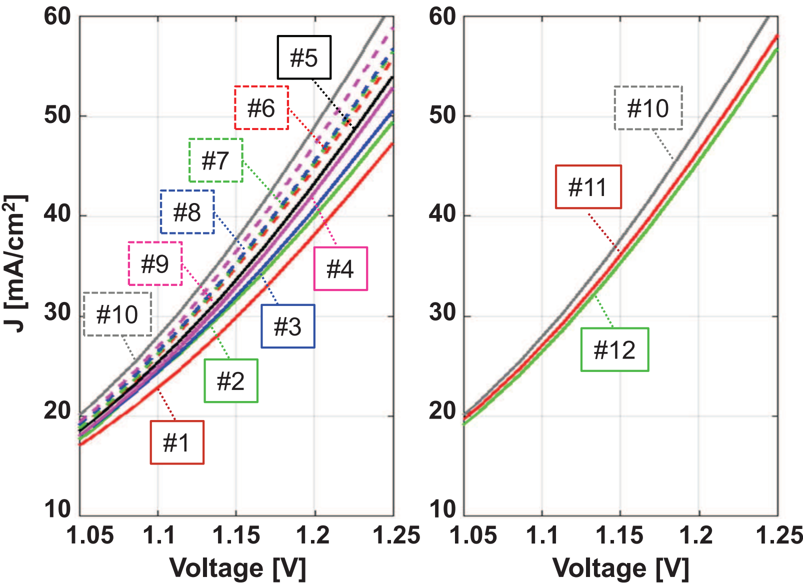


Figure 6.26: J-V curves measured at each step-end in the experiment of Fig. 6.25.

the voltage shifts by generating the adequate average bias voltage using a closed loop control based on sigma-delta modulation. This entails the possibility of controlling the impedance of the device. The potential applications of this type of controls could be the improvement of energy storage capability of the device.

In case of devices made of perovskite materials, trapped charge is one of the most triggering factors in the degradation of perovskite devices. Most of the research work done in this line of improving the stability of the perovskite is focused on the variations in the fabrication process and/or the materials used. In this work, we have implemented an active control scheme for charge trapping in solar cell devices. The control capability relies on the complementary J-V shifting produced by the voltages applied. This may be seen as a promising way to improve the reliability and practical applicability of devices based on perovskites.

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Chapter 7

Conclusions and Future Work

7.1 Conclusions

This Thesis addressed the issue of dielectric charge trapping in heterogeneous systems. More specifically, smart charge control techniques to effectively control the charge trapping in MOS capacitors and improve the operative lifetime of the devices have been proposed, designed and tested experimentally. This Thesis also contributed to the analysis and modeling of the charge trapping dynamics in MOS capacitors using Diffusive Representation and Sliding Mode Control. Furthermore, application of these control strategies have been extended to devices which also suffer from the effects of charge trapping.

The main conclusions of the research work are summarized as follows:

- Closed loop control strategies based on sigma-delta modulation have been implemented to control the net amount of charge trapped in the dielectric layers of MOS capacitors. These controls use specific voltage waveforms, allowing to continuously monitor the status of the net dielectric charge and to maintain it around a desired target level. The experimental results show that the controls implemented are successful in controlling the trapped charge. An improved second order sigma-delta control has also been implemented and checked experimentally.

- The response of MOS capacitors operating under ionizing radiation while they are being controlled has also been investigated. The experiments demonstrate that the charge induced by ionizing radiation can be successfully compensated by the control loops. The bit stream generated at the output serves as an indirect measure of the total amount of trapped charge and therefore provides information on the ionizing dose received by the device. These experiments were carried out at ESA-ESTEC Co-60 facility and at Radiation Physics Laboratory of University of Santiago de Compostela.

- The dynamics of the charge trapped in a MOS capacitor has been modeled using Diffusive

Representation. The model predictions successfully describes the charge dynamics in the dielectric and are validated using the experiments under arbitrary waveforms.

The charge dynamics of the device operating under sigma-delta controls has been analyzed using the tools of Sliding Mode Control. The analytical model has been very successful in predicting the system behavior even under the influence of external disturbances such as ionizing radiation.

- The charge control techniques have been extended to other devices such as eMIM capacitors and pervoskite solar cells. Preliminary results demonstrate that the control loops successfully avoid the impedance drifts in MIM devices, while they effectively allow to control the displacement of the J-V characteristic in a perovskite solar cell.

As a result of this Thesis, four peer reviewed journal papers have been published and three communications have been presented in congresses. The experimental findings from eMIM devices and perovskite devices have been submitted for publication.

7.2 Future Work

Although the major goals of the Thesis have been accomplished, there is always scope to address charge trapping issues in other devices or applications. The work carried out in this Thesis provides basis for future research in several areas.

- Extend the application of closed loop control techniques to MOS-based devices like MOSFETs. These devices, in general, suffer from problems such as threshold voltage instability and reduced mobility, due to charge trapping. Future work will focus on implementing the proposed controls to improve their reliability.

- Implementation of charge trapping compensation control loops on Radiation Sensing Field Effect Transistors (RADFETs) to extend their lifetime by avoiding the build-up of trapped charge with accumulated dose. This will be achieved by implementing a continuous charge trapping control to keep constant the threshold voltage during the whole operation of the device.

- Further experimental studies are needed to investigate the possibility of control strategies improving photovoltaic features such as open-circuit voltage or efficiency in perovskite solar cells and energy storage ability in eMIM capacitors.

- Application of Diffusive Representation and Sliding Mode Control techniques to perovskite solar cells to characterize and model the charge dynamics. The developed model would allow us to understand the charge transport mechanisms in the device and contribute to the improvement of its efficiency.

- Investigation of the impact of device processing changes on charge trapping behavior in MOS capacitors under irradiation. The future work in this area can be directed towards the development of radiation-hard devices for space applications.

Appendices

Appendix A

Journal Publications and Conferences

This appendix summarizes the Journal publications and Conference works related to the main subject of this Thesis.

Works:

1. **Diffusive Representation and Sliding Mode Control of Charge Trapping in Al_2O_3 MOS Capacitors** on page 141.

   Published in *IEEE Transactions on Industrial Electronics*, Jan 2019.

2. **Second order sigma-delta control of charge trapping for MOS capacitors** on page 142.

   Published in *Microelectronics Reliability*, 76, pp. 635-639, Sept 2017.

3. **Closed-Loop Compensation of Charge Trapping Induced by Ionizing Radiation in MOS Capacitors** on page 143.

   Published in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2518-2524, Aug 2017.

4. **Charge trapping control in MOS capacitors** on page 144.

   Published in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 4, pp. 3023-3029, Sept 2017.

5. **Second order sigma-delta control of charge trapping for MOS capacitors** on page 145.

Presented in *28th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis*, in Bordeaux, France, Sept 2017.

6. **Sliding mode control of fractional order systems: applications to sensors** on page 146.

   Presented in 2nd *Fractional Calculus Meeting*, in Madrid, Spain, Nov 2018.

7. **Active charge trapping control in dielectrics under ionizing radiation** on page 147.

   Presented in *American Geophysical Union, Fall Meeting 2017*, in New Orleans, USA, Dec 2017.

8628 IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 66, NO. 11, NOVEMBER 2019

Diffusive Representation and Sliding Mode Control of Charge Trapping in Al_2O_3 MOS Capacitors

Chenna Reddy Bheesayagari, Joan Pons-Nin, Maria Teresa Atienza, and Manuel Dominguez-Pumar, *Senior Member, IEEE*

***Abstract*—The objective of this paper is to introduce a modeling strategy to characterize the dynamics of the charge trapped in the dielectric of MOS capacitors, using diffusive representation. Experimental corroboration is presented with MOS capacitors made of Alumina in three different scenarios. First, the model predictions are compared with the trapped charge evolution due to arbitrary voltage excitations. Second, the predictions are compared with the measurements of a device in which a sigma–delta control of trapped charge is implemented. Finally, the time evolution when the device is simultaneously controlled and irradiated with X-rays is compared with the predictions. In all cases, a good matching between the models and the measurements is obtained.**

***Index Terms*—Charge trapping control, diffusive representation (DR), ionizing radiation, MOS capacitors, sliding control.**

I. Introduction

DIELECTRIC charge trapping is widely identified as a key factor affecting the reliability of many metal-oxide-semiconductor (MOS) related devices [1]. The physical mechanisms responsible for such charge trapping are rather complex and, for a given device type, mainly dependent on the fabrication process, the temperature, and the voltage applied [2]–[9]. Other factors, such as external disturbances (i.e., due to ionizing radiation), have also a remarkable influence on charge trapping.

The characterization of the charge trapping dynamics in MOS devices has been extensively studied [10]. Trap distributions are obtained from impedance spectra for different voltages in [11] and [12]. Other works analyze the charging dynamics as the result of the application of voltage, or temperature, stress, while observing discharging currents or shifts in the threshold voltage. In these methods, the stress factor is instantaneously changed and changes in drain currents or threshold voltage shifts are monitored and fitted. Models with one or two time constants, as well as, more generally, stretched exponentials have been used to this purpose. In stretched exponentials, the charge transient is characterized by the function $\exp(-(t/\tau)^{\beta})$, with $\beta \in (0, 1)$. This model has been linked to Gaussian distributions in the energy barriers found in charge trapping and detrapping [13]. However, in all these cases, the analysis of the time evolution of systems under arbitrary excitation becomes difficult because it is necessary to take into account the distributed nature of the processes involved.

Besides, the diffusive nature of the charge trapping phenomena allows their behavioral characterization using state-space models based on diffusive representation (DR). In recent times, DR tools have been successfully used for modeling and prediction purposes in several diffusion-based systems, such as thermal [14], [15] and electrical [16], [17] fractional systems. In this paper, we use DR since it allows to directly obtain models from experimental data, which can be very easily simulated and are compatible with physical processes including diffusion and dispersion in general.

On the other hand, charge trapping controls based on sigma-delta loops have been proposed recently for MOS capacitors in [18]. Under some limits, these controls allow to set and maintain a previously given amount of net dielectric charge, thus mitigating long-term reliability issues such as C–V shifting or threshold voltage drifts. In these controls, the charge being continuously leaked out of the dielectric is compensated in average by applying an adequate sequence of bipolar voltages. The same type of sigma–delta strategies had been previously used to control the charge in micro-electromechanical systems (MEMS) [19]–[21]. In this case, DR and sliding-mode control tools were used successfully to analyze and predict the dynamics of the trapped charge.

Furthermore, charge trapping generated by ionizing radiation in harsh environments such as space applications has been extensively studied. Changes in the threshold voltage of MOS transistors are among the most noticeable effects [22]–[26]. To mitigate this problem, extensive design and shielding strategies are routinely implemented. Besides, compensation of charge trapped in SiO_2 MOS capacitors induced by gamma radiation using sigma–delta controls has been demonstrated recently in [27]. Ionizing radiation such as gamma and X-ray radiation

Manuscript received July 6, 2018; revised October 7, 2018 and November 19, 2018; accepted December 9, 2018. Date of publication January 8, 2019; date of current version June 28, 2019. This work was supported in part by the Spanish MINECO Project ESP2016-79612-C3-2R. *(Corresponding author: Manuel Dominguez-Pumar.)*

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Digital Object Identifier 10.1109/TIE.2018.2890488

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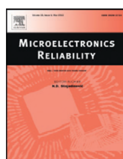
Microelectronics Reliability 76–77 (2017) 635–639

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Second order sigma-delta control of charge trapping for MOS capacitors

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ARTICLE INFO

Article history:
Received 20 May 2017
Received in revised form 17 June 2017
Accepted 30 June 2017
Available online 14 July 2017

Keywords:
Charge trapping
MOS
Dielectric charging
Sigma-delta
Sliding mode control

ABSTRACT

This paper presents the circuit topology of a second order sigma-delta control of charge trapping for MOS capacitors. With this new topology it is possible to avoid the presence of plateaus that can be found in first-order sigma-delta modulators. Plateaus are unwanted phenomena in which the control is locked for a certain time interval (of unknown duration). In this case the control output is constant and therefore the controlled device is in fact in open-loop configuration. It is shown that the presence of plateaus is avoided in MOS capacitors using the proposed approach.

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1. Introduction

Charge trapping is a ubiquitous phenomenon present in almost any device containing dielectric materials. Among the devices for which charge trapping represents a reliability problem we find:

- MOS capacitors and related structures such as ultrathin gate oxides used in MOSFETs [1–4]. Charge trapping generates changes in the threshold voltage of the transistors, among other effects.
- Electrostatic MEMS/NEMS [5–7]. Charge trapping generates shift of the C-V characteristic of the device, shift of the pull-in voltage and even permanent stiction. This has been a particularly difficult problem for RF-MEMS switches [8].
- Organic FETs (OFETS). Charge trapping also generates changes in the threshold voltage of the transistors [9].

In general, this phenomenon alters device performance, affecting its circuital features and even reducing its effective lifetime. The physical mechanisms responsible for charge trapping are rather complex and dependent on fabrication processes, temperature, and electrical stresses applied to the device [10–14].

Many research works focus on characterization and mitigation of the effects of dielectric charging from very different approaches. For example, specific geometries and dielectricless structures have been proposed for MEMS [15,16], while new dielectric materials and stack arrangements allowing charge trapping reduction have been proposed for MOS structures [17–19]. Moreover, some circuit strategies to compensate dielectric-related degradation effects during device lifetime have been proposed for specific MOSFET applications [20,21].

Additionally, several actuation strategies using smart voltage waveforms have been proposed to mitigate and even control the effects of dielectric charging in MEMS [8,22,23]. These strategies are based on the opposite effects produced by bipolar voltages on the charge dynamics. Following this complementarity principle, a first order control of charge trapping for MOS capacitors was presented in [24]. This control allows to obtain a desired shift of the C-V characteristic of the device (and hence of the net trapped charge in the oxide) and then to maintain it. This is achieved through a control loop based on sigma-delta modulation that applies a proper sequence of bipolar voltage waveforms to have the average charge injection necessary to keep the desired charge level, see Fig. 1.

However, one of the known problems of first-order sigma-delta modulators is the appearance of plateaus [25]. If the sampling time is of the same order or greater than the shortest time constant of the charging and discharging processes of the device, the control may provide a constant output during certain time intervals in which the system is effectively in an open loop configuration. It must be noted that the charging and discharging time constants will depend on the applied voltages in a nonlinear way and that several processes may coexist in a single device, resulting in a complex dynamics that is generally difficult to predict beforehand.

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http://dx.doi.org/10.1016/j.microrel.2017.06.096
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2518 IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 65, NO. 3, MARCH 2018

Closed-Loop Compensation of Charge Trapping Induced by Ionizing Radiation in MOS Capacitors

Manuel Dominguez-Pumar, *Senior Member, IEEE*, Chenna Reddy Bheesayagari, Sergi Gorreta, *Student Member, IEEE*, Gema Lopez-Rodriguez, and Joan Pons-Nin

***Abstract*—The objective of this paper is to explore the capability of a charge trapping control loop to continuously compensate charge induced by ionizing radiation in the dielectric of metal–oxide–semiconductor (MOS) capacitors. To this effect, two devices made with silicon oxide have been simultaneously irradiated with gamma radiation: one with constant voltage bias and the other working under a dielectric charge control. The experiment shows substantial charge trapping in the uncontrolled device, whereas, at the same time, the control loop is able to compensate the charge induced by gamma radiation in the second device.**

***Index Terms*—Charge trapping control, ionizing radiation, metal–insulator–semiconductor (MIS) capacitors, metal–oxide–semiconductor (MOS) capacitors, radiation effects.**

I. Introduction

CHARGE trapping induced by ionizing radiation in metal–oxide–semiconductor (MOS) devices represents a reliability issue in space applications [1]. Under the influence of high energy ionizing radiation, these devices suffer from a drift in the threshold voltage, an increase of the leakage current, and a decrease of the transconductance [2]. This results in a degraded performance, thereby, increasing the failure rate of the device operation [3]–[6].

In the opposite direction, radiation sensitive field-effect transistors (RADFETs) are MOS structures especially designed for radiation sensing. In recent years, some works have focused on obtaining a trapped hole annealing in order to delay the saturation of the sensor and to keep it working in near optimal conditions. This has been achieved by applying bias switching [7]. In [8], periodical charge neutralization of radiation-induced trapped charge is performed to keep the threshold voltage of RADFETs between some predetermined limits. Measurement is carried out in open-loop configuration between bias switching operations. On the other hand, Fowler–Nordheim tunneling is used in [9] to compensate holes trapped in the buried oxide layer of a monolithic pixel detector used in high-energy physics, X-ray imaging, etc. As a consequence, techniques focused on controlling the total charge in dielectrics may have many different applications (drift avoidance or sensor optimization).

Dielectric charge controls, first proposed in [10], have been recently achieved in the case of electrostatic microelectromechanical systems (MEMS) [11], [12] and MOS capacitors [13]. This paper presents results obtained in gamma radiation experiments carried out to observe how dielectric charge induced by ionizing radiation can be effectively compensated by a charge control loop. In particular, we prove that the control loop presented in [13] can also be used to compensate the charge induced by ionizing radiation in MOS capacitors with silicon oxide as dielectric. A first result in this direction has already been obtained for electrostatic MEMS [14]. To the best knowledge of the authors, this is the first time that charge induced by ionizing radiation has been compensated in an MOS structure. This new approach opens the possibility of establishing active compensation techniques of radiation-induced charge in MOS structures.

II. Charge Control Loop

The control method implemented in this paper, presented in [13], is based on sigma-delta modulation [15], used as a tool to provide a sliding mode control of net trapped charge [16], [17].

A. Sigma-Delta Modulation and Sliding Mode Control

Sigma-delta modulators are extensively used in analog-to-digital and digital-to-analog conversion. In the analog-to-digital case, they are oversampled circuits that use rough quantizers (reaching even the 1-bit case, or sign function) to produce a stream of symbols from which the final digital conversions are obtained by filtering and decimation. These modulators provide quantization noise shaping, which means that the circuit moves the quantization noise out of the frequency band of interest of the analog input. By finally filtering the stream of symbols in the band of interest, the quantization noise is removed to a large

Manuscript received December 12, 2016; revised March 30, 2017, May 26, 2017, and July 18, 2017; accepted August 22, 2017. Date of publication August 31, 2017; date of current version December 15, 2017. This work was supported in part by the Spanish projects TEC2013-48102-C2-1P and ESP2016-79612-C3-2R. *(Corresponding author: Manuel Dominguez-Pumar.)*

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Digital Object Identifier 10.1109/TIE.2017.2748033

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IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 64, NO. 4, APRIL 2017 3023

Charge Trapping Control in MOS Capacitors

Manuel Domínguez-Pumar, *Senior Member, IEEE*, Chenna Reddy Bheesayagari, Sergi Gorreta, *Student Member, IEEE*, Gema López-Rodríguez, Isidro Martín, Elena Blokhina, *Senior Member, IEEE*, and Joan Pons-Nin

***Abstract*—This paper presents an active control of capacitance–voltage (C–V) characteristic for MOS capacitors based on sliding-mode control and sigma–delta modulation. The capacitance of the device at a certain voltage is measured periodically and adequate voltage excitations are generated by a feedback loop to place the C–V curve at the desired target position. Experimental results are presented for an n-type c-Si MOS capacitor made with silicon dioxide. It is shown that with this approach, it is possible to shift the C–V curve horizontally to the desired operation point. A physical analysis is also presented to explain how the C–V horizontal displacements can be linked to charge trapping in the bulk of the oxide and/or in the silicon–oxide interface. Finally, design criteria are provided for tuning the main parameters of the sliding-mode controller.**

***Index Terms*—Dielectric charge control, MOS capacitors, sliding-mode control.**

I. Introduction

DIELECTRIC charge trapping is widely known as an important reliability issue in MOS capacitors and related structures such as ultrathin gate oxides used in MOSFETs [1], or in MEMS. This phenomenon alters device performance, affecting its circuital features and even reducing its effective lifetime. Shift of the capacitance–voltage (C–V) characteristic [2], [3], and therefore of the threshold voltage, or negative-bias temperature instability (NBTI) degradation observed in p-MOSFETs [4] are examples of serious reliability problems due to oxide charge trapping.

The physical mechanisms responsible for charge trapping are rather complex and dependent on the fabrication process, the temperature, and the electrical stress applied to the device [5]–[10]. Most works focus on the design and characterization of materials and structures to reduce the effects of charge trapping.

Manuscript received June 28, 2016; revised October 3, 2016 and October 31, 2016; accepted November 12, 2016. Date of publication December 26, 2016; date of current version March 8, 2017. This work was supported in part by the Project TEC2013-48102-C2-1P. *(Corresponding author: Manuel Domínguez-Pumar.)*

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Digital Object Identifier 10.1109/TIE.2016.2645159

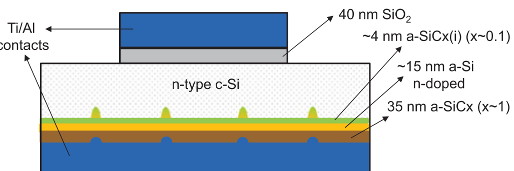

Fig. 1. Cross section of the MOS capacitor used in the experiments.

Although these methods have substantially reduced the charge trapping in the dielectrics, shift of the C–V characteristic due to charge trapping still represents a reliability issue in MOS transistors and capacitors. The purpose of this paper is to show how a simple control technique, based on sliding control [11], can be used to deliberately shift the C–V characteristic to a desired operation point, either for compensating dielectric charging or for other circuital requirements.

The method is similar to that used in MEMS devices [11], [12] consisting in the application of bipolar actuation voltage stresses and a sigma–delta modulation control loop. It has been successfully demonstrated in silicon dioxide MOS capacitors.

II. Fabrication Process

The capacitors used in the experiments were fabricated on an n-type c-Si ⟨ 100 ⟩ wafer, 280 μm thick and resistivity of 2.5 $\pm$ 0.5 $\Omega\cdot$ cm. The process starts with an RCA clean followed by a thermal oxidation for 30 min with a temperature ramp between 850 °C and 1080 °C. An SiO_2 layer of ~40-nm thick is grown on both sides of the wafer. The SiO_2 of the back side is removed with high-frequency (HF) etching, whereas the front side is protected with photoresist. To obtain a good ohmic contact at the back surface, a stack consisting of ~4-nm a-SiC_x(i) ($x \sim 0.1$), 15-nm n-doped a-Si and 35-nm a-SiC_x ($x \sim 1$) is deposited on the back side of the wafer by PECVD. Then, a laser doping technique [13] is applied trough this dielectric stack to create localized n^{++} regions with 400 μm pitch. After this laser processing step, the bottom of the sample is ready to be contacted with 480 nm of Ti/Al stack deposited by RF sputtering. A second deposition of Ti/Al is made at the front side to create the upper contact. The active device area is delimited by photolithography patterning and wet etching. A final annealing in N_2 atmosphere at 400 °C for 30 min improves the contacts and the adherence with the c-Si. Fig. 1 shows a cross section of the device.

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Second order sigma-delta control of charge trapping for MOS capacitors

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Abstract

This paper presents the circuit topology of a second order sigma-delta control of charge trapping for MOS capacitors. With this new topology it is possible to avoid the presence of plateaus that can be found in first-order sigma-delta modulators. Plateaus are unwanted phenomena in which the control is locked for a certain time interval (possibly of infinite duration). In this case the control output is constant and therefore the controlled device is in fact in open-loop configuration. It will be shown that the presence of plateaus is avoided in MOS capacitors using the proposed approach.

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Sliding mode control of fractional order systems: application to sensors

Dominguez, M.; Bermejo, S.; Bheesayagari, C.; Pons, J.

Sliding mode controls (SMCs) are applied during sensor operation in order to accelerate their time response and/or obtain other improvements in performance. The main objective is to avoid the typically slow dynamics of the underlying physical structures (thermal circuits, diffusion processes, etc.). This can be achieved by designing controls that continuously compensate the effects of the external factors to be measured, so that the state variables of the system remain constant. The necessary control actions are then the new system output, which can be significantly faster than in open loop operation. Additionally, it is also possible to improve in other ways such as increasing sensitivity, or avoiding effects of some parasitic elements or even mitigating the effects of undesired external influences. In many applications, the dynamics of the physical structures can be modelled using fractional calculus (thermal sensors, charge trapping in dielectrics, chemical sensors, etc.). In this paper we present how Diffusive Representation can be used to model fractional order systems, and how the dynamics of the system, working under SMCs, can be analysed in the infinite sampling approximation. We will present how external disturbances trigger changes in the control actions, which must be adapted to compensate their effect. Experimental examples will be presented for two different applications: compensation of charge trapping generated by ionizing radiation in MOS capacitors, and control applied to heat flux sensors.

Active charge trapping control in dielectrics under ionizing Radiation

Dominguez-Pumar, M.; Bheesayagari, C.; Gorreta, S.; Pons-Nin, J.

Charge trapping is a design and reliability factor in plasma sensors. Examples can be found in microchannel plate detectors in plasma analyzers, where multiple layers have been devised to ensure filled trapped electrons for enhanced secondary emission. Charge trap mapping is used to recover distortion in telescope CCDs. Specific technologies are designed to mitigate the effect of ionizing radiation in monolithic Active Pixel Sensors. We report in this paper a control loop designed to control charge in Metal-Oxide-Semiconductor capacitors. We find that the net trapped charge in the device can be set within some limits to arbitrary values that can be changed with time. The control loop periodically senses the net trapped charge by detecting shifts in the capacitance vs voltage characteristic, and generates adequate waveform sequences to keep the trapped charge at the desired level. The waveforms continuously applied have been chosen to provide different levels of charge injection into the dielectric. The control generates the adequate average charge injection to reach and maintain the desired level of trapped charge, compensating external disturbances. We also report that this control can compensate charge generated by ionizing radiation. Experiments will be shown in which this compensation is obtained with X-rays and gamma radiation. The presented results open the possibility of applying active compensation techniques for the first time in a wide number of devices such as radiation sensors, MOS transistors and other devices. The continuous drive towards integration may allow the implementation of this type of controls in devices needing to reject external disturbances, or needing to optimize their response to radiation or ion fluxes.