NONLINEAR CONTROL OF DC-DC SWITCHING CONVERTERS WITH CONSTANT POWER LOAD

Blanca Areli Martínez Treviño

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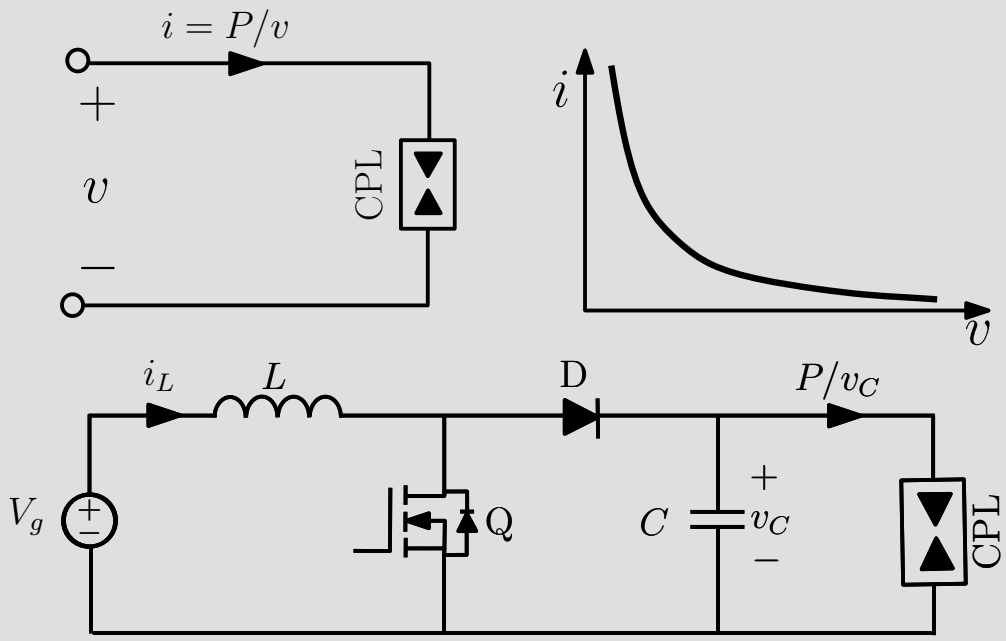

DOCTORAL THESIS

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Doctoral Thesis

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UNIVERSITAT ROVIRA i VIRGILI

Tarragona 2019

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FEM CONSTAR que aquest treball, titulat "Nonlinear control of dc-dc switching converters with constant power load", presentat per Blanca Areli Martínez Treviño per a l'obtenció del títol de Doctor, ha estat realitzat sota la meva direcció al Departament d'Enginyeria Electrònica Elèctrica i Automàtica d'aquesta universitat.

HAGO CONSTAR que el presente trabajo, titulado "Nonlinear control of dc-dc switching converters with constant power load", que presenta Blanca Areli Martínez Treviño para la obtención del título de Doctor, ha sido realizado bajo mi dirección en el Departamento de Ingeniería Electrónica Eléctrica y Automática de esta universidad.

I STATE that the present study, entitled "Nonlinear control of dc-dc switching converters with constant power load", presented by Blanca Areli Martínez Treviño for the award of the degree of Doctor, has been carried out under my supervision at the Department of Electronic, Electric and Automatic Control Engineering of this university.

Tarragona, 01 April 2019

El/s director/s de la tesi doctoral
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To my parents for
everything they have
done for me.

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Nomenclature: acronyms, parameters, symbols and variables

Acronyms

ADC	Analog-Digital Converter
BOF	Boost with Output Filter
CCM	Continuous Conduction Mode
CMC	Current-Mode Control
CPL	Constant Power Load
DCM	Discontinuous Conduction Mode
DPWM	Didital Pulse Width Modulation
DSMC	Digital Sliding-Mode Control
DSP	Digital Signal Processor
EP	Equilibrium Point
EPL	Equilibrium Point Locus
ESM	Existence Sliding-Mode
ESR	Equivalent Series Resistance

Nomenclature: acronyms, parameters, symbols and variables

EV	Electric vehicle
IC	Integrated Circuit
LHP	Left Half-plane
PCB	Print Circuit Board
PD	Proportional Derivative
PI	Proportional Integral
POPI	Power Output is equal to Power Input
PP	Polypropylene
PRS	Parametric Region of Stability
PWM	Pulse Width Modulation
RHP	Right Half-plane
SMC	Sliding-Mode Control
VMC	Voltage-Mode Control

Parameters

C	Capacitance
L	Inductance
R	Resistance

Symbols

D	Diode
D_a	Auxiliary start-up diode
Q	MOSFET

Variables

D	The steady-state of the duty cycle
d	The duty cycle in continuous-time
d_e	The duty cycle in discrete-time
i_{CPL}	The current of the CPL
$\hat{i}_L$	The incremental value of the continuous-time variable of the inductor current i_L
$\overline{i}_L$	Continuous-time variable representing the average value of the inductor current i_L in a switching cycle
i_L	Continuous-time variable of the inductor current
$i_L[n]$	The sample of the continuous-time variable of the inductor current
I_L^*	The steady-state average value of the inductor current
i_{ref}	The inductor current reference in continuous-time
$i_{\text{ref}}[n]$	The inductor current reference in discrete-time
P	The power of the CPL
$\hat{P}$	The estimated power
$P_{\text{min}_{\text{CCM}}}$	The minimum power value delivered by the converter in CCM operation
T_{OFF}	The non conduction time of the switch Q
T_{ON}	The conduction time of the switch Q
u_{eq}	The equivalent control
$\hat{v}_C$	The incremental value of the continuous-time variable of the capacitor voltage v_C
$\overline{v}_C$	Continuous-time variable representing the average value of the capacitor voltage v_C in a switching cycle

Nomenclature: acronyms, parameters, symbols and variables

v_C	Continuous-time variable of the capacitor voltage
$v_C[n]$	The sample of the continuous-time variable of the capacitor voltage
V_C^*	The steady-state of the capacitor voltage
V_g	The input voltage
V_{ref}	The capacitor voltage reference

Chapter 1

Introduction

Multiconverter systems are usually employed in modern electric vehicles (EV) [1–5], sea and undersea vehicles [6–10] or dc micro-grids [11–14] involving a great number of interconnected converters [15]. The key element in these systems is a dc bus, which performs the power distribution to supply both dc and ac loads using the energy provided by the different dc sources, *i.e.* batteries, fuel cells, photovoltaic generators and ultra-capacitors.

Besides the series and parallel connections in both converter ports or in only one of them, and the particular case of paralleling operation due to interleaving, cascade connection is a relevant example of association. It consists in connecting the output port of the first converter to the input port of the second one. The first stage is called source converter while the second one is denominated load converter, as is illustrated in Fig. 1.1.

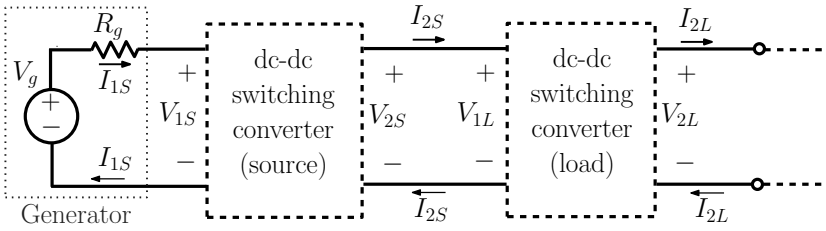


Figure 1.1: Cascade connection of power converters.

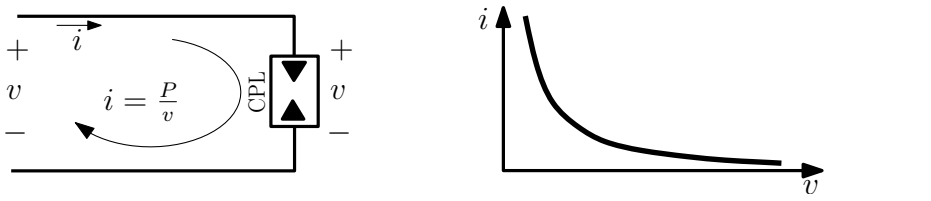
1.1 Constant Power Load Definition

A particular case of the cascade connection is characterized by the operation of the load converter absorbing constant power or, equivalently, by the operation of the source converter supplying a constant power load (CPL) [1, 3, 13, 15–18].

A CPL can be defined as one-port device with a voltage-current characteristics given by

$$vi = P, \qquad P \in \mathbb{R}^+,\ i \in \mathbb{R}^+,\ v \in \mathbb{R}^+ \tag{1.1}$$

The symbol of a CPL is a power sink as shown in Fig. 1.2(a), where the current absorbed by the sink is expressed as $i = P/v$. Fig. 1.2(b), in turn, depicts the corresponding voltage-current characteristics of the CPL.



(a) Symbol (b) voltage–current characteristics $vi = P$

Figure 1.2: CPL definition.

1.2 Risk of Instability

It is well-known that a dc-dc switching converter with ideal regulation at the output, *i.e*, infinite bandwidth and 100% power conversion efficiency can result in unstable behavior when combined with an input filter [19, 20]. This phenomenon was reviewed in [16] by modelling for the first time an ideally regulated high efficiency power converter by means of a CPL. This case is reproduced in this section for the sake of illustrating the risk of instability that emerges in the supply of a CPL.

Fig. 1.3 depicts a model of a high efficient converter in closed-loop combined with a second order LC input filter. The resistance R_g represents the losses. The state

equations of the system in Fig. 1.3 can be expressed as follows

$$\frac{di_L}{dt} = \frac{1}{L}\left(V_g - R_g i_L - v_C\right) \tag{1.2}$$

$$\frac{dv_C}{dt} = \frac{1}{C}\left(i_L - \frac{P}{v_C}\right) \tag{1.3}$$

The coordinates of the equilibrium point of (1.2)-(1.3) are given by

$$I_L^* = \frac{P}{V_C^*} \tag{1.4}$$

$$V_C^* = \frac{V_g}{2} \pm \sqrt{\left(\frac{V_g}{2}\right)^2 - R_g P} \tag{1.5}$$

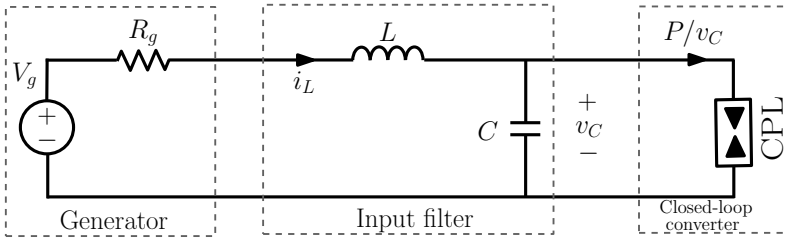


Figure 1.3: Model of an ideally regulated high efficient converter with input filter.

Note from (1.5) that,

$$\text{Case 1} \quad \left(\frac{V_g}{2}\right)^2 > R_g P \quad \text{implies two equilibrium points} \tag{1.6}$$

$$\text{Case 2} \quad \left(\frac{V_g}{2}\right)^2 = R_g P \quad \text{implies one equilibrium point} \tag{1.7}$$

$$\text{Case 3} \quad \left(\frac{V_g}{2}\right)^2 < R_g P \quad \text{implies no equilibrium point} \tag{1.8}$$

The above conditions can be interpreted geometrically in the plane $i_L - v_C$ by representing the equations (1.2)-(1.3) in the equilibrium as illustrated in Fig. 1.4.

Equations (1.2) and (1.3) can be expressed in equilibrium as follows

$$v_C = V_g - R_g i_L \tag{1.9}$$

$$v_C i_L = P \tag{1.10}$$

Equations (1.9) and (1.10) are plotted in Fig. 1.4 to illustrate conditions (1.6)-(1.8) for different values of R_g. Note that condition (1.6) corresponds to Case 1, condition (1.7) to Case 2 and condition (1.8) to Case 3.

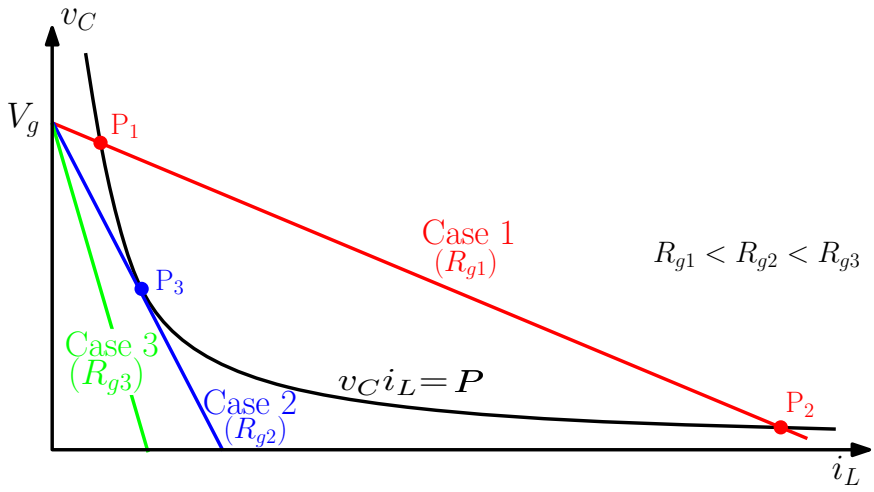


Figure 1.4: Intersection of CPL characteristic curve and load line.

Besides, determining the existence of equilibrium point in (1.2)-(1.3), the study of their stability has to be subsequently considered. Let $v_C = V_C^* + \hat{v}_C$ and $i_L = I_L^* + \hat{i}_L$. Then, linearizing equations (1.2)-(1.3) around the equilibrium point given by (1.4)-(1.5) results in the following small-signal model

$$\frac{d\hat{i}_L}{dt} = -\frac{R_g}{L}\hat{i}_L - \frac{1}{L}\hat{v}_C + \frac{1}{L}\hat{V}_g \tag{1.11}$$

$$\frac{d\hat{v}_C}{dt} = \frac{1}{C}\hat{i}_L + \frac{P}{CV_C^{*2}}\hat{v}_C \tag{1.12}$$

The characteristic equation corresponding to (1.11)-(1.12) is given by

$$s^2 + s\left(\frac{R_g}{L} - \frac{P}{CV_C^{*2}}\right) + \frac{1}{LC} = 0 \tag{1.13}$$

Therefore, the small-signal dynamics (1.11)-(1.12) will correspond to a stable system if the following condition is satisfied

$$R_g > \frac{L}{C}\frac{P}{V_C^{*2}} \tag{1.14}$$

On the other hand, from (1.6)-(1.7), the existence of equilibrium point requires

$$R_g \leqslant \frac{V_g^2}{4P} \tag{1.15}$$

Finally, conditions (1.14) and (1.15) can be written as a single expression

$$\frac{L}{C}\frac{P}{V_C^{*2}} < R_g \leqslant \frac{V_g^2}{4P} \tag{1.16}$$

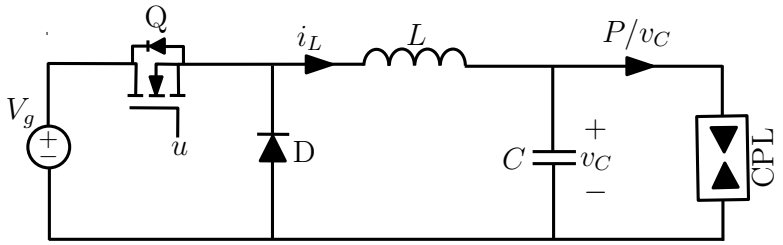
Note that constraint (1.16) can be expressed in terms of the maximum allowed power $P_{\max}$ for a given set of values of $L,\ C,\ V_g,\ R_g$ and V_C^* as follows

$$P_{\max} = \min\left(\frac{V_C^{*2}R_g}{L/C}, \frac{V_g^2}{4R_g}\right) \tag{1.17}$$

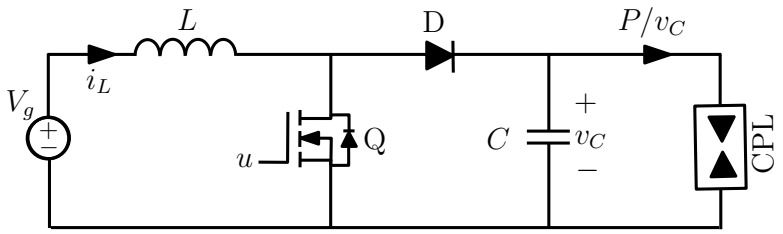
It can be concluded from the analysis above that the cascade connection of an input filter and a tightly regulated high efficient converter is prone to instability for power values higher than a certain bound $P_{\max}$.

1.3 Dc-dc Switching Converters in CCM Loaded with a CPL

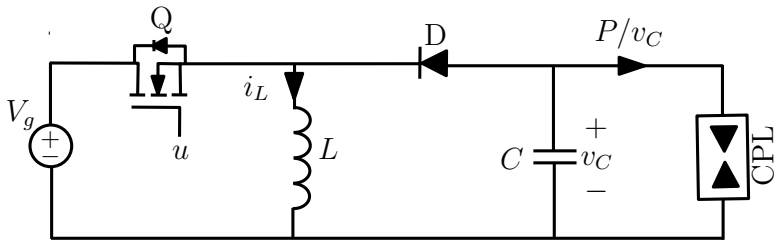
Instead of modelling an ideally regulated high efficient converter by means of a CPL, it seems now pertinent to refine our approach by exploring the behavior of the converter configurations. In other words, we analyze in this section the effect of the CPL in the ON and OFF behavior of the converter in continuous conduction mode (CCM). With this aim, Fig. 1.5 illustrates the canonical converters loaded with a CPL.



(a) buck



(b) boost



(c) buck–boost

Figure 1.5: Elementary converters loaded with CPL.

By simple analysis, it is found that the output voltage of the buck converter can be expressed as

$$\frac{d^2v_C}{dt^2} - \frac{P}{v_C^2 C}\frac{dv_C}{dt} + \frac{v_C}{CL} = \frac{V_g}{CL}u \tag{1.18}$$

where u is a binary signal, such that $u = 1$ during the conduction time of switch Q (T_{ON}) and $u = 0$ during the non conduction time of the same switch (T_{OFF}). It can be observed that (1.18) is a nonlinear differential equation, which results in an unbounded behavior of voltage v_C due to the negative nonlinear damping term $-P/v_C^2 C$.

Similarly, the output voltage dynamics in the boost converter can be expressed as

$$\frac{d^2v_C}{dt^2} - \frac{P}{v_C^2 C}\frac{dv_C}{dt} + \frac{(1-u)^2 v_C}{CL} = \frac{(1-u)V_g}{CL} \tag{1.19}$$

Finally, the differential equation describing the output voltage behavior in the buck–boost converter is given by

$$\frac{d^2v_C}{dt^2} - \frac{P}{v_C^2 C}\frac{dv_C}{dt} + \frac{(1-u)^2 v_C}{CL} = \frac{-(1-u)uV_g}{CL} \tag{1.20}$$

From (1.18), (1.19), (1.20) it can be concluded without loss of the generality that the behavior of the dc-dc switching converters in both ON and OFF states is unstable. Fig. 1.6 illustrates the unstable behavior of the canonical converters in ON and OFF states by showing the trajectories of the state-vector in the plane i_L-v_C.

It can be expected that the combination of both ON and OFF trajectories in any converter irrespective of the duty cycle value will result in an open unbounded trajectory.

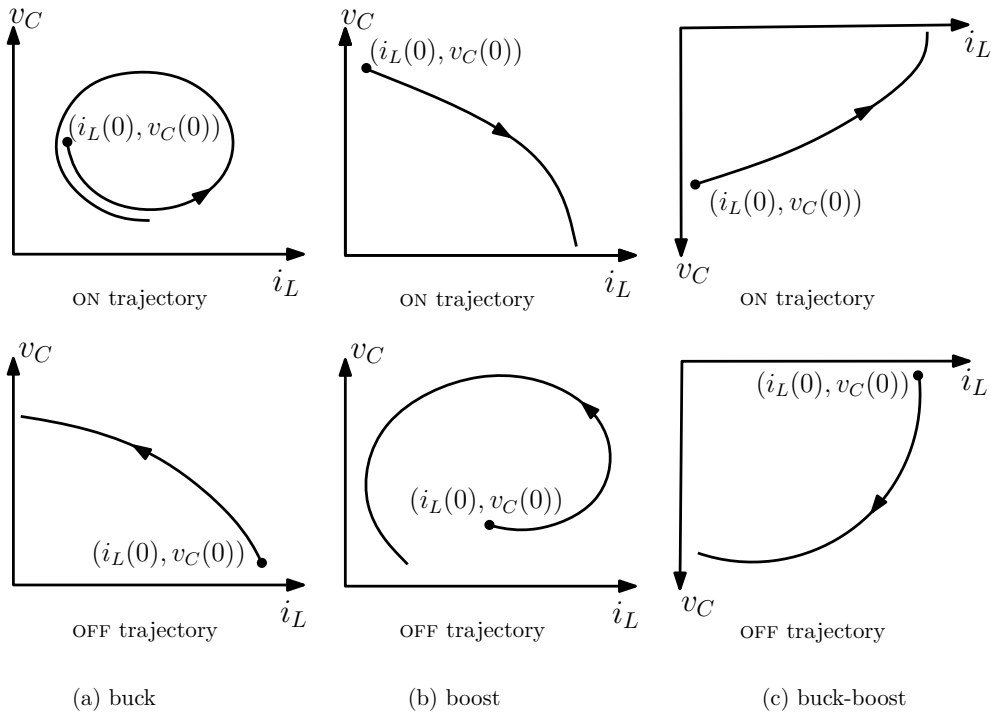


Figure 1.6: ON and OFF trajectories corresponding to the elementary dc-dc converters with CPL.

1.4 Transfer Functions of Unstable System

The nonlinear nature of the capacitor voltage dynamics, due to its connection with the CPL, precludes the use of matrix-based analysis techniques such as the state-space averaging method [21]. This technique is based on the description of dc-dc switching converters with resistive load as piecewise-affine system because they can be expressed as follows

$$\dot{\mathbf{x}} = \mathbf{A}_i\mathbf{x} + \mathbf{B}_i V_g, \qquad i = 1, 2 \tag{1.21}$$

where $\mathbf{x}$ is the state-vector and $i = 1$ for ON state and $i = 2$ for OFF state.

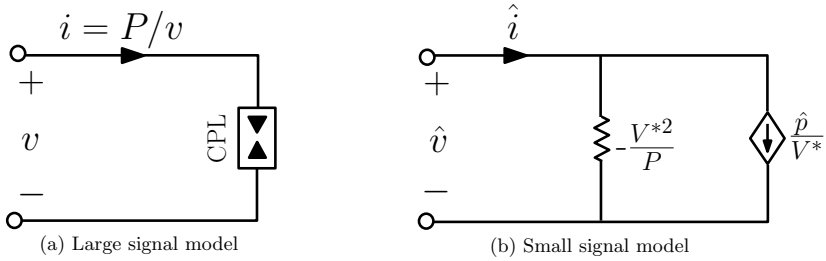
Nonetheless, the CPL can be linearized around its operating point of voltage V^* and power P. Hence, from (1.1) the following expression is obtained

$$\Delta i = \frac{d(\frac{P}{v})}{dv}\Delta v + \frac{d(\frac{P}{v})}{dP}\Delta P \tag{1.22}$$

Solving the above equation, the linearizing model of a CPL is given by

$$\hat{i} = -\frac{P}{V^{*2}}\hat{v} + \frac{\hat{p}}{V^*} \tag{1.23}$$

The equivalent model of the CPL is depicted in Fig. 1.7. Then, the resulting negative incremental resistance can be used in a mathematical description similar to (1.21) while the current source can be considered as an external perturbation. As a result, this approach leads to modelling dc-dc switching converters with negative resistance load [22, 23]. The underlying idea is to take advantage of the state-space average predictions by assuming that a constant value of the output voltage and the inductor current only makes sense if the converter is appropriately regulated, *i.e.*, if it operates in closed-loop with a correct feedback law that can ensure the steady-state values of the state variables required in the dynamic modelling.



(a) Large signal model (b) Small signal model

Figure 1.7: Linearization of a CPL.

Therefore, we will derive next transfer functions that represent small-signal unstable dynamic behavior in open-loop around the mentioned steady-state values, which would be ensured by the insertion of an appropriate control loop.

To illustrate the procedure, Fig. 1.8 shows the starting point, which is the averaged dynamic model of a boost converter with resistive load R in the case of duty cycle variations ($\hat{d} \neq 0$) and constant input voltage ($\hat{v}_g = 0$) [24]. Parameters I_L^* and V_C^* are the steady-state values of i_L and v_C respectively.

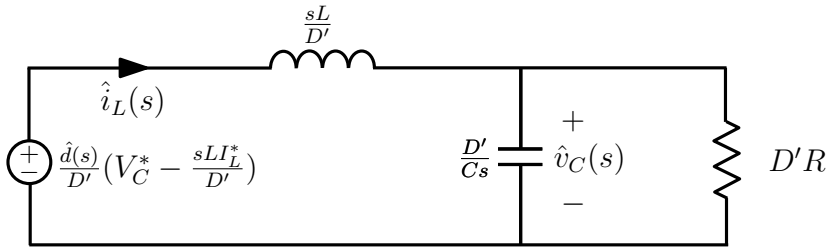


Figure 1.8: Small-signal average dynamic model of a boost converter with resistive load and control variations.

The model for the CPL case will be obtained by substituting R in Fig. 1.8 by $-R$ as shown in Fig. 1.9, where the value of R is given by V_C^{*2}/P as illustrated in Fig. 1.7(b), and I_L^* is expressed as

$$I_L^* = \frac{P}{V_g} = \frac{P}{V_C^{*2} D'} \tag{1.24}$$

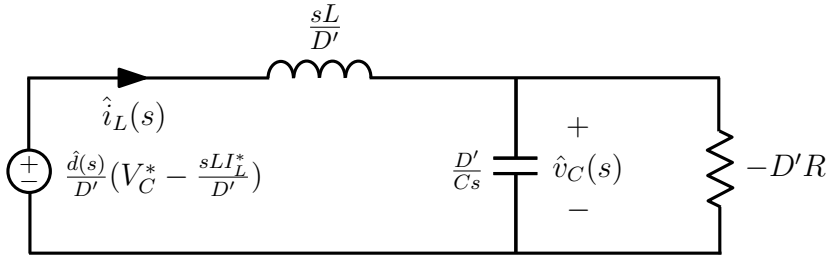


Figure 1.9: Circuit model of the small-signal dynamic behavior of a boost converter with CPL for control variations.

By simple analysis of the circuit of Fig. 1.9, the control to output voltage transfer function $G_{vd}(s)$, and the control to inductor current transfer function $G_{id}(s)$ can be expressed as follows

$$G_{vd}(s) = \frac{\hat{v}_C(s)}{\hat{d}(s)} = \frac{V_C^*}{D'} \frac{1 - sL\frac{P}{V_C^{*2}D'^2}}{1 - \frac{LP}{D'^2V_C^{*2}}s + \frac{LC}{D'^2}s^2} \tag{1.25}$$

$$G_{id}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V_C^*}{D'^2} \frac{Cs}{1 - \frac{LP}{D'^2V_C^{*2}}s + \frac{LC}{D'^2}s^2} \tag{1.26}$$

It is worth mentioning that both transfer functions have poles in the right half-plane (RHP) while they differ as in the positive resistance load case in the existence or not of RHP zeros. Thus, (1.25) is as expected a non-minimum phase transfer function while (1.26) is a minimum phase transfer function.

1.5 Motivation

Several methods have been proposed to cope with the mentioned CPL instability. Passive damping added to one of the filter elements in the cascade connection of a voltage source, an LC filter, and a CPL is used in [25] to stabilize the system without requiring the modification of the source or the load control. An active damping method based in the insertion of a virtual resistor and based on a supercapacitor energy storage system

to compensate the negative incremental impedance of the CPL is successfully employed in [26] and [27] respectively. Feedback linearization is reported in [28] in the context of a medium voltage dc bus for power distribution on ships to compensate the nonlinearity introduced by the CPL. Active compensation has been also explored in the case of a source converter of boost type by using current control to introduce damping into the system dynamics [29, 30].

In solutions based on linear controllers, the starting point is an unstable transfer function relating either the control to output voltage or the control to inductor current. The transfer function is unstable because it is derived by simple substitution of the resistive load corresponding to a conventional supplying case by the negative incremental resistance of the CPL as it has been explained in Section 1.4 of this document. We recall that the steady-state values of the state variables required in the transfer function are the ones imposed by the closed loop behavior of the system provided that an appropriate controller stabilizes the converter. Nonetheless, the hypothesis of stable closed-loop steady-state is not achieved in some cases in spite of introducing some control loops. For example, the introduction of an inner current loop for the average value regulation of the inductor current stabilizes a boost converter with CPL but it fails in a buck converter with the same type of load as demonstrated in [31]. Only the additional introduction of an outer loop allows the system stabilization in the latter case.

In [32], a robust control approach has been considered for the elementary power switching converters with a CPL. In [33] a robust controller based on linear programming is proposed to regulate the output of buck converters loaded by another buck converter acting as a CPL.

Passivity-based control has been also explored in a buck converter with CPL [34] leading to a simple linear PD control, which provides virtual damping without affecting the system efficiency.

Sliding-mode control (SMC) [35–44] has been also studied in [45] to regulate a boost converter feeding a CPL connected in parallel with a resistive load. A switching surface made up of a linear combination of the capacitor voltage error and the difference between the inductor current and its high frequency component is used with the aim of

regulating the output voltage in front of load changes of step type. Simulation results have shown a good performance of the proposed control and the existence of bifurcations when the gain of the current error is used as a parameter. An SMC-based pulse width modulation (PWM) approach is employed in [46] with a nonlinear switching surface in the output voltage regulation of a boost converter supplying a CPL. The previous nonlinear switching surface is modified in [47] by including a linear term proportional to the voltage error to improve the output voltage regulation. While the first approach operates at constant switching frequency, the second one results in a highly variable switching frequency due to the action of an ideal comparator in the control loop. In the context of an island dc micro-grid, SMC-based PWM is used again satisfactorily to regulate a 380 V dc bus with multiple photovoltaic generators, several boost converters and a battery bank [48]. The same approach is used in [49] for the case of a buck-boost converter feeding a composite load (constant resistance, constant current and constant power), which is dominated by CPL, showing robustness in front of input voltage and load disturbances. A sliding-mode duty-ratio control to operate a constant switching frequency is proposed in [9, 50] for a buck converter with CPL in a ship dc bus power distribution system. Switching surfaces based either on the current error or on a linear combination of current and voltage error are used to regulate the dc bus voltage in the different modes of the system.

Moreover, also in the case of dc micro-grids, active stabilization techniques based on a combination of load shedding, additional resistive loads and other circuits have been used in [11]. Stabilization has been also achieved in the same micro-grid context by the inclusion of external circuitry emulating a capacitor as reported in [51].

On the other hand, the direct cascade connection of two buck converters where the second stage acts as a CPL, has been analyzed by means of boundary [52] or synergetic control [53] to eventually derive sufficient stability conditions and mitigate the instability effect produced by the CPL.

All contributions on the CPL subject are based on continuous-time models, the exception being the work reported in [54], where a discrete-time approach is used in the analysis of a buck converter with a fourth order output filter supplying a CPL with the aim of identifying slow-scale and fast-scale instabilities.

To summarize, most of the existing contributions are theoretical approaches exploring how to counteract the inherent instability of the CPL. Their main goal has been demonstrating the stabilizing effect of the proposed strategies without showing other important aspects such as rejection to input voltage changes or load variations, inrush current minimization and practical implementation of the control.

1.6 Objectives

The main goal of this research is to describe analytically the cascade connection of converters under constant power supply conditions, and propose simple control solutions that can cope with the potential instability caused by the CPL. With this aim, the use of different strategies such as linear control, SMC, digital SMC (DSMC), and nonlinear PWM control is studied in the regulation of a boost converter supplying a CPL.

The thesis is organized as follows;

Chapter 2 reexamines the analysis of the elementary converters in open-loop in the boundary between CCM and DCM carried out in reference [55].

In Chapter 3, the SMC of a boost converter feeding a CPL is exhaustingly covered by a continuous-time approach leading to an analogue implementation.

A discrete-time approach for sliding-mode control using a PWM resulting in a digital implementation is presented in Chapter 4.

Chapter 5 introduces two analogue PWM-based nonlinear controllers as alternative solutions to regulate the output voltage in constant switching frequency operation. First, the use of a virtual mesh is developed to both stabilize the converter and indirectly regulate the output voltage. Then, a mechanism to estimate the power of the CPL is presented.

Chapter 6 addresses the implementation of converters with CPL behavior by presenting a general systematic procedure of synthesis.

Finally, the conclusions of the thesis are summarized in Chapter 7.

Chapter 1. Introduction

Chapter 2

Open-loop dc-dc Converters with CPL in the Boundary CCM-DCM

2.1 Introduction

It has been shown in the introductory chapter that there is an upper bound for the power that a tightly regulated converter with input filter can supply. Beyond that value, stability problems or inexistence of equilibrium point can arise. Also, it has been demonstrated that the output voltage exhibits a nonlinear unstable dynamics that results in unbounded trajectories in both ON and OFF states in any converter. Thus, it has been conjectured that the combination of ON and OFF trajectories in open-loop operation would result in an open unbounded trajectory irrespective of the duty cycle.

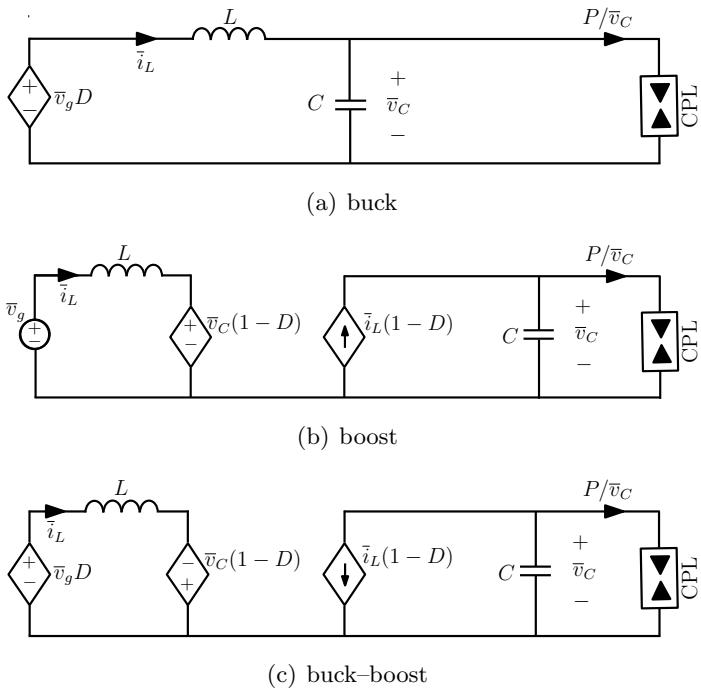
Nonetheless, it was demonstrated in [55] that a stable behavior could be obtained in open-loop operation when the converters were working in the boundary between CCM and DCM. Like in the resistive load case, the boundary was derived in terms of the switching period, inductance value and a function of the duty cycle. However, the expression of the boundary was determined by a value of the power $P_{\min_{\text{CCM}}}$, which established the minimum value of the CPL power to operate in CCM for a given value of the input voltage V_g.

We can observe again that an upper bound of the power emerges to separate stable and unstable behavior, or equivalently DCM and CCM operations.

The analysis reported in [55] is reviewed in this chapter under the optics of an averaged model of the switching converter [24].

2.2 Average Circuit Model of the Elementary Converters with CPL in CCM

The converters shown in Fig. 1.5 can be modelled as depicted in Fig. 2.1. It has to be pointed out that both control and state variables are continuous-time functions representing the average value in a switching cycle [24] of the respective variables illustrated in Fig. 1.5. Assuming that an equilibrium point can be reached, the circuits depicted in Fig. 2.1 can be represented as illustrated in Fig. 2.2. It can be observed in all cases the POPI nature of the steady-state model as it can be expected.



(a) buck

(b) boost

(c) buck–boost

Figure 2.1: Averaged circuit model of elementary converters with CPL.

2.2 Average Circuit Model of the Elementary Converters with CPL in CCM

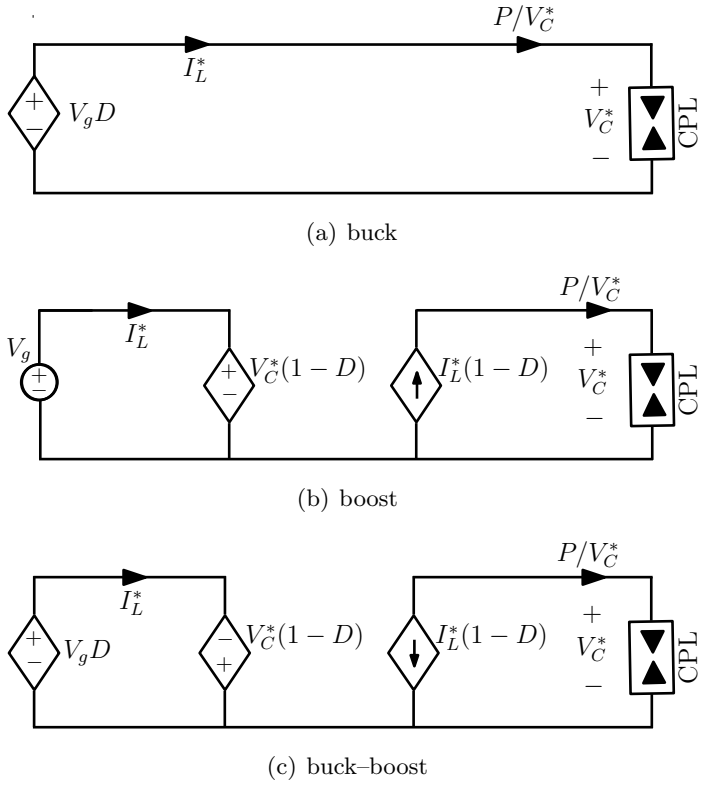


Figure 2.2: Steady-state model corresponding to the circuits in Fig. 2.1.

For the buck converter:

$$P_{\mathrm{DC_{in}}} = V_g D I_L^* = V_g D \frac{P}{V_C^*} = V_C^* \frac{P}{V_C^*} = P = P_{\mathrm{DC_{out}}} \tag{2.1}$$

For the boost converter

$$P_{\mathrm{DC_{in}}} = V_g I_L^* = (1-D) V_C^* I_L^* = V_C^* \frac{P}{V_C^*} = P = P_{\mathrm{DC_{out}}} \tag{2.2}$$

For the buck-boost converter

$$P_{\mathrm{DC_{in}}} = V_g D I_L^* = -(1-D) V_C^* I_L^* = V_C^* \frac{P}{V_C^*} = P = P_{\mathrm{DC_{out}}} \tag{2.3}$$

2.3 Boundary CCM-DCM

In the boundary between CCM and DCM the inductor current i_L of any elementary converter behaves in steady-state as illustrated in Fig. 2.3.

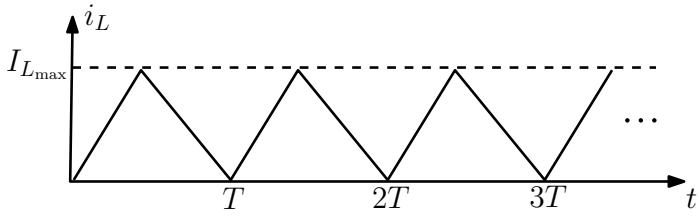


Figure 2.3: Steady-state inductor current i_L in the boundary CCM-DCM for any elementary converter.

The steady-state average value I_L^* of inductor current in any converter is related to the maximum value $I_{L_{\max}}$ as follows

$$I_L^* = \frac{I_{L_{\max}}}{2} \tag{2.4}$$

2.4 Minimum Power of the CPL for CCM Operation

2.4.1 Buck Converter

From (2.4) the following expression is obtained for the buck converter

$$\begin{aligned} I_L^* &= \frac{I_{L_{\max}}}{2} = \frac{V_g D(1-D)T}{2L} = \frac{V_g D^2(\frac{1}{D}-1)}{2L}T = \\ &= \frac{V_g D^2(\frac{V_g}{V_C^*}-1)}{2L}T = \frac{V_g D^2 T}{2L}\frac{(V_g - V_C^*)}{V_C^*} \end{aligned} \tag{2.5}$$

Hence, the power delivered by the buck converter to the CPL in the boundary CCM-DCM will be

$$P_{\min_{\text{CCM}}} = V_C^* I_L^* = \frac{V_g D^2 T(V_g - V_C^*)}{2L} = \frac{V_g^2 D^2 T}{2L}(1-D) \tag{2.6}$$

2.4.2 Boost Converter

Similarly, expression (2.4) becomes in the boost converter

$$I_L^* = \frac{V_g DT}{2L} \tag{2.7}$$

The power delivered by the converter to the CPL in the boundary CCM-DCM is

$$P_{\min_{\text{CCM}}} = V_C^* I_L^* (1-D) = \frac{V_C^* V_g D(1-D)T}{2L} = \frac{V_g^2 DT}{2L} \tag{2.8}$$

2.4.3 Buck-Boost Converter

Note that expression (2.7) also applies for the buck-boost converter, so the value of $P_{\min_{\text{CCM}}}$ will be

$$P_{\min_{\text{CCM}}} = -V_C^* I_L^* (1-D) = V_g D I_L^* = \frac{V_g^2 D^2 T}{2L} \tag{2.9}$$

2.4.4 Comparison of Minimum Values of Power

Expressions (2.6), (2.8) and (2.9) can be compared taking the minimum value of power in the buck-boost as a reference case. Defining

$$P_{\min_{\text{CCM(buck-boost)}}} = \frac{V_g^2 D^2 T}{2L} \triangleq P_{\text{critical}}, \tag{2.10}$$

it can be observed that

$$P_{\min_{\text{CCM(buck)}}} = \frac{V_g^2 D^2 T}{2L}(1-D) = P_{\text{critical}}(1-D) < P_{\text{critical}} \tag{2.11}$$

and

$$P_{\min_{\text{CCM(boost)}}} = \frac{V_g^2 DT}{2L} = \frac{P_{\text{critical}}}{D} > P_{\text{critical}} \tag{2.12}$$

2.5 Stability of the Equilibrium Point in the Boundary CCM-DCM

2.5.1 Buck Converter Case

We consider now the dynamic behavior of the buck converter shown in Fig. 2.1(a). The dynamics of the output port can be expressed as

$$\bar{i}_L = \frac{C d\overline{v}_C}{dt} + \frac{P}{\overline{v}_C} \tag{2.13}$$

From (2.4), the dynamic behavior of $\bar{i}_L$ in continuous-time becomes as follows

$$\bar{i}_L = \frac{V_g D^2 T}{2L} \frac{(V_g - \overline{v}_C)}{\overline{v}_C} \tag{2.14}$$

Introducing (2.14) in (2.13) leads to

$$\frac{V_g D^2 T}{2L} \left(\frac{V_g - \overline{v}_C}{\overline{v}_C} \right) - \frac{P}{\overline{v}_C} = \frac{C d\overline{v}_C}{dt} \tag{2.15}$$

In equilibrium

$$\frac{d\overline{v}_C}{dt} = 0, \qquad v_C = V_C^* \tag{2.16}$$

Hence,

$$\frac{V_g D^2 T}{2L} (V_g - V_C^*) = P \tag{2.17}$$

or equivalently,

$$V_C^* = V_g - \frac{2LP}{V_g D^2 T} \tag{2.18}$$

Observe that the existence of equilibrium point in (2.18) implies that

$$V_g > \frac{2LP}{V_g D^2 T} \tag{2.19}$$

Equivalently

$$P < \frac{V_g^2 D^2 T}{2L} \tag{2.20}$$

Note that (2.20) is exactly condition (2.11). Therefore, there always will be an equilibrium point in a buck-converter feeding a CPL in the boundary CCM-DCM.

To analyze the stability of the equilibrium point we will assume in (2.15), $\overline{v}_C = V_C^* + \Delta v_C$, so that $|\Delta v_C| < V_C^*$.

Therefore, (2.15) becomes

$$\frac{V_g D^2 T}{2L}\left(\frac{V_g - V_C^* - \Delta v_C}{V_C^* + \Delta v_C}\right) - \frac{P}{V_C^* + \Delta v_C} = C\frac{d(\Delta v_C)}{dt} \tag{2.21}$$

After a simple manipulation, (2.21) becomes

$$\frac{d(\Delta v_C)}{dt} = -\frac{V_g D^2 T}{2LC}\frac{\Delta v_C}{V_C^* + \Delta v_C} \tag{2.22}$$

It can be observed in (2.22) that

$$\Delta v_C > 0 \quad \text{implies} \quad \frac{d(\Delta v_C)}{dt} < 0 \tag{2.23}$$

$$\Delta v_C < 0 \quad \text{implies} \quad \frac{d(\Delta v_C)}{dt} > 0, \tag{2.24}$$

As consequence, it can be concluded that the equilibrium point (2.18) exists and is stable.

2.5.2 Boost Converter Case

The output port dynamics of the boost converter is given by

$$\bar{i}_L(1-D) = C\frac{d\overline{v}_C}{dt} + \frac{P}{\overline{v}_C} \tag{2.25}$$

Following a similar procedure to the one developed in the buck converter case, the dynamic behavior of variable $\bar{i}_L$ will be given by

$$\bar{i}_L = \frac{V_g D T}{2L} \tag{2.26}$$

On the other hand, we can also write

$$\bar{i}_L(1-D) = \frac{V_g^2 T}{2L}\frac{D}{\overline{v}_C} = \frac{V_g^2 T D^2}{2L(\overline{v}_C - V_g)} \tag{2.27}$$

Hence, (2.25) becomes

$$\frac{V_g^2 T}{2L}\frac{D^2}{\overline{v}_C - V_g} = C\frac{d\overline{v}_C}{dt} + \frac{P}{\overline{v}_C} \tag{2.28}$$

In equilibrium condition (2.16) applies. Hence,

$$\frac{V_g^2 T D^2}{2L}\frac{V_C^*}{V_C^* - V_g} = P \tag{2.29}$$

Solving for V_C^* in (2.29), we obtain

$$V_C^* = \frac{P V_g 2L}{2LP - V_g^2 T D^2} \tag{2.30}$$

The existence of equilibrium point given by (2.30) requires that

$$P > \frac{V_g^2 T D^2}{2L}, \tag{2.31}$$

which is exactly condition (2.12). Therefore, there exists an equilibrium point in a boost converter supplying a CPL in the boundary CCM-DCM.

Assuming in (2.28) $\overline{v}_C = V_C^* + \Delta v_C$, such that $|\Delta v_C| < V_C^* - V_g$, we derive from (2.28)

$$\frac{V_g^2 T}{2L}\frac{D^2}{V_C^* + \Delta v_C - V_g} = C\frac{d(\Delta v_C)}{dt} + \frac{P}{V_C^* + \Delta v_C} \tag{2.32}$$

After a simple manipulation, we obtain

$$C\frac{d(\Delta v_C)}{dt} = -\frac{\Delta v_C (2LP - V_g^2 T D^2)}{2L(V_C^* + \Delta v_C - V_g)(V_C^* + \Delta v_C)} \tag{2.33}$$

Note that again conditions (2.23) and (2.24) are fulfilled, so the equilibrium point given by (2.30) is stable.

2.5.3 Buck-boost Converter Case.

In the boundary, the dynamics of the output capacitor voltage in the buck-boost converter is given by

$$\bar{i}_L(1-D) = -C\frac{d\overline{v}_C}{dt} - \frac{P}{\overline{v}_C} \tag{2.34}$$

where the dynamic behavior of variable $\bar{i}_L$ is also given by expression (2.26).

Therefore, we can write

$$\bar{i}_L(1-D) = \frac{V_g}{2L}D(1-D) = \frac{-V_g^2 D^2 T}{2L\overline{v}_C} \tag{2.35}$$

Introducing (2.35) in (2.34) leads to

$$\frac{V_g^2 T}{2L}\frac{D^2}{\overline{v}_C} = C\frac{d\overline{v}_C}{dt} + \frac{P}{\overline{v}_C} \tag{2.36}$$

Equivalently,

$$C\overline{v}_C\frac{d\overline{v}_C}{dt} = \frac{V_g^2 D^2 T}{2L} - P \tag{2.37}$$

Defining $z(t) = \frac{1}{2}C\overline{v}_C^2$, we derive

$$\frac{dz}{dt} = \frac{V_g^2 T D^2}{2L} - P = P_{\text{critical}} - P_{\min_{\text{CCM}}} \tag{2.38}$$

From (2.10), we conclude that the right term of equation (2.38) is zero.

Hence,

$$\frac{dz}{dt} = 0 \tag{2.39}$$

Therefore

$$z(t) = \frac{1}{2}C\overline{v}_C(0) \tag{2.40}$$

Expression (2.40) only provides a generic information since it states that the stored energy in the capacitor is constant in steady-state, which is a well-known property for any reactive element in a switching converter. Also, note that no information is given of the actual value of V_C unlike what occurs in the buck and boost cases (see expressions (2.18) and (2.30)).

If we define

$$P_{\text{critical}} - P_{\min_{\text{CCM}}} = \epsilon \tag{2.41}$$

Then,

$$\frac{dz}{dt} = \epsilon \tag{2.42}$$

Therefore,

$$z(t) = z(0) + \epsilon t \tag{2.43}$$

If $\epsilon > 0$, then $\lim_{t\to\infty} z(t) = \infty$, which implies that $\lim_{t\to\infty} \overline{v}_C(t) = \infty$.
If $\epsilon < 0$, then mathematically $\lim_{t\to\infty} z(t) = -\infty$, and $\lim_{t\to\infty} \overline{v}_C(t) = -\infty$, but physically when $z(t)$ reaches zero, no real solution will exist.

We can conclude that the equilibrium point in the buck-boost converter in CCM-DCM boundary cannot be defined in terms of P, V_g, T, D and L. Besides, the equilibrium point is unstable. A small difference between P_{critical} and $P_{\min_{\text{CCM}}}$ results in either an unbounded or a zero value for the output capacitor voltage.

2.6 Simulation of Elementary Converters Operation in the Boundary CCM-DCM

In order to verify the theoretical predictions, numerical simulations in PSIM© software of the buck and boost converters depicted in Fig. 1.5 are performed.

2.6.1 Buck Converter

The parameter values of the power stage are summarized in Table 2.1. Note that the minimum value delivered by the converter in the boundary will be $P_{\min_{\text{CCM}}} = 319.72$ W.

Table 2.1: Summary of parameter values for the buck converter with CPL.

L	C	V_g	D	T
196 μH	15 μF	350 V	42%	10 μs

The waveforms of the inductor current and capacitor voltage of the buck converter operating in the boundary CCM-DCM are depicted in Fig. 2.4. It can be observed that the capacitor voltage in steady-state is $V_C^* = 147$ V, as predicted by (2.18). Besides, the system is stable.

On the other hand, a power in the CPL smaller than $P_{\min_{\text{CCM}}}$ ($P = 290$ W) leads the system to operate in DCM. Therefore, the buck converter operating in DCM is stable as shown the Fig. 2.5.

On the contrary, if the delivered power to the load is greater than $P_{\min_{\text{CCM}}}$ ($P = 350$ W) the converter will operate in CCM. Fig. 2.6 illustrates the converter behavior in this mode. It can be observed that the buck converter operating in CCM loaded by CPL is unstable in open loop.

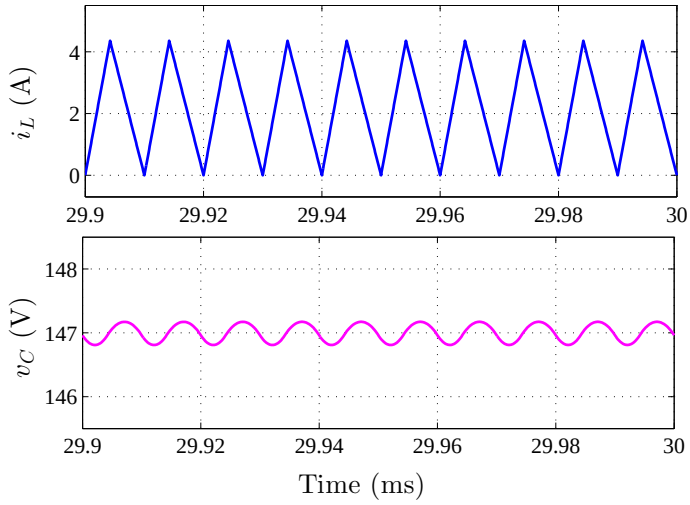


Figure 2.4: Buck converter behavior with CPL in open loop in the boundary CCM-DCM operation mode.

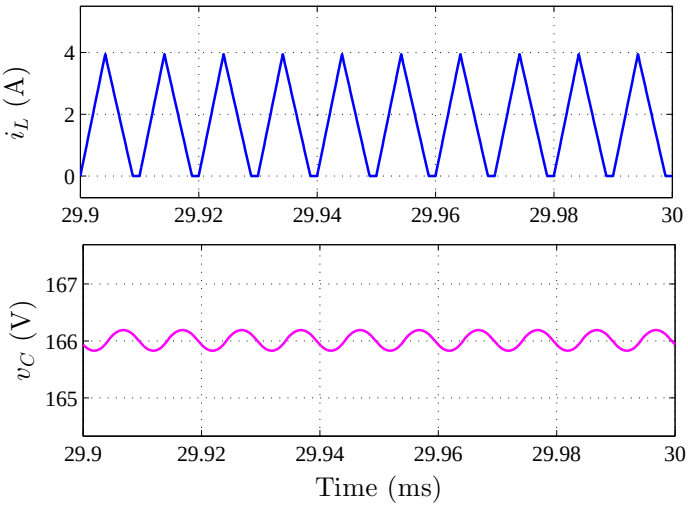


Figure 2.5: Buck converter behavior with CPL in open loop in DCM $P = 290$ W $< P_{\text{min}_{\text{CCM}}}$.

2.6.2 Boost Converter

Let us consider the nominal values of the power stage parameters summarized in Table 2.2. The minimum value of the power delivered in the boundary between CCM and

Chapter 2. Open-loop dc-dc Converters with CPL in the Boundary CCM-DCM

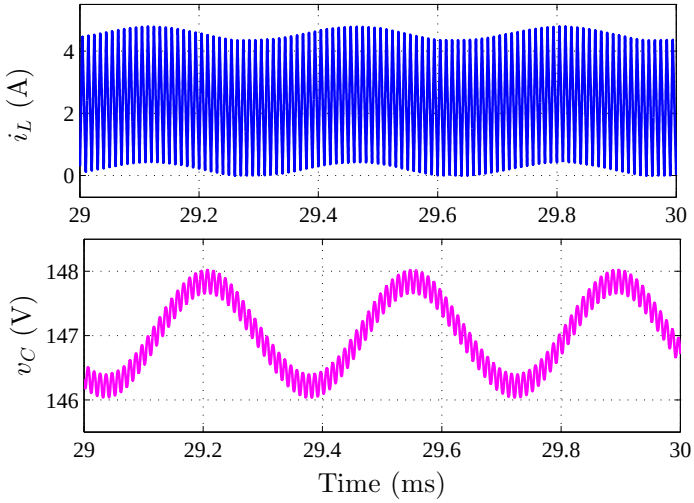


Figure 2.6: Buck converter behavior with CPL in open loop in CCM $P = 350$ W $> P_{\min_{\text{CCM}}}$.

Table 2.2: Summary of parameter values for the boost converter with CPL.

L	C	V_g	D	T
326 μH	20 μF	200 V	42%	10 μs

DCM is $P_{\min_{\text{CCM}}} = 257.66$ W. The converter behavior in open loop for this power value is shown in Fig. 2.7. Note that the boost converter supplying CPL is stable in this operation mode. The steady-state average value of the capacitor voltage is $V_C^* = 344.82$ V, which corroborates the value predicted analytically by expression (2.30). The converter behavior in DCM ($P < P_{\min_{\text{CCM}}}$) is depicted in Fig. 2.8. It can be noted that the boost converter working in DCM is stable. In Fig. 2.9 the operation of the system working in CCM ($P > P_{\min_{\text{CCM}}}$) is illustrated. Note that, as in buck converter case, the boost converter loaded with CPL working CCM is also unstable in open-loop.

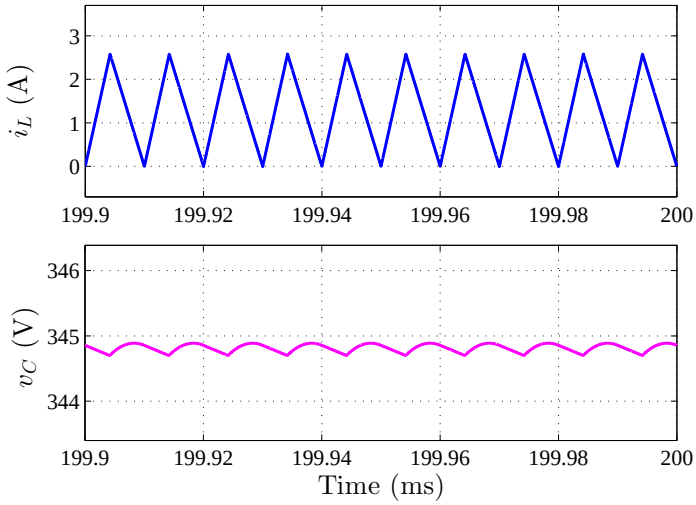


Figure 2.7: Boost converter behavior with CPL in open loop in the boundary CCM-DCM operation mode.

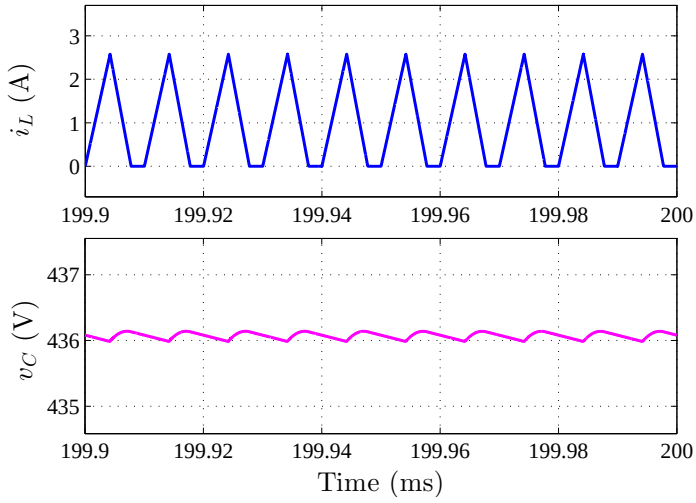


Figure 2.8: Boost converter behavior with CPL in open loop in DCM $P = 200$ W $< P_{\min_{\text{CCM}}}$.

Chapter 2. Open-loop dc-dc Converters with CPL in the Boundary CCM-DCM

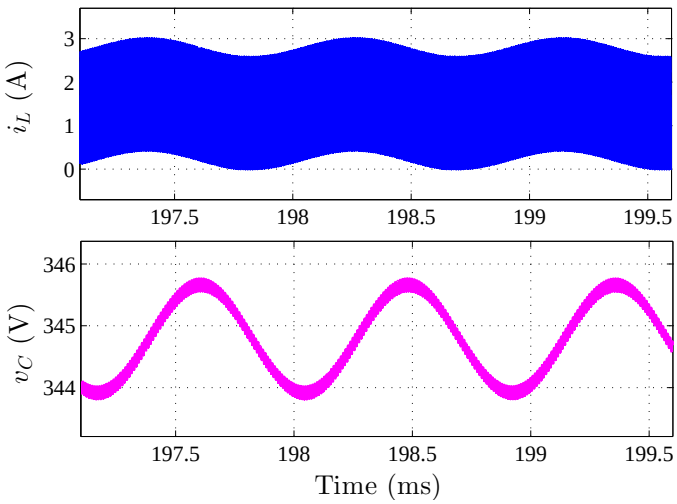


Figure 2.9: Boost converter behavior with CPL in open loop in CCM $P = 300$ W $> P_{\min_{\text{CCM}}}$.

Chapter 3

Two Approaches for the Closed-loop Operation of Power Converters with CPL in CCM: Two-loop Linear Control and SMC

3.1 Introduction

It has been demonstrated in Chapter 2 that both buck and boost converters with CPL exhibit a stable open-loop behavior in the boundary CCM-DCM while the buck-boost converter is unstable under the same operating conditions.

Therefore, a CCM operation for levels of power higher or equal than $P_{\mathrm{CCM}_{\mathrm{min}}}$ requires a closed-loop strategy in the elementary converters that can also simultaneously ensure output voltage regulation.

Two possible candidates appear as a first choice: a linear approach based on peak current control and a nonlinear strategy based on SMC.

The linear approach is based on the linearized model of the CPL and the subsequent transfer functions with RHP poles of the power converter explained in Chapter 1. The

underlying hypothesis in this case is that an appropriate feedback can stabilize the converter in CCM and provide at the same time a good degree of output voltage regulation.

The nonlinear control proposed combines the unstable ON and OFF trajectories shown in Chapter 1 to create a stable trajectory that slides along an appropriate switching surface to reach the desired steady-state behavior (equilibrium point).

This chapter covers exhaustingly both approaches by providing a detailed analytical study of both cases and by validating the respective theoretical predictions. The validation is carried out by means of simulation in the case of the linear control and by means of both simulations and experiments in the SMC alternative.

For the sake of simplicity, and without loss of generality, the study will be limited to the boost converter with CPL.

3.2 Two-loop Linear Control

The control used in this section is based on a two-loop linear control strategy, in which the inner loop corresponds to a peak-current control and the outer voltage loop uses a PI compensator. Fig 3.1 shows a block diagram of the two-loop PWM linear analog control of a boost converter loaded with a CPL. In the power stage, diode D_a creates a path during the start-up to minimize the effect of the inrush current in the inductor. It has been added to create a unidirectional path from the source to the load hence guaranteeing the condition $v_C = V_g$ at the starting time and thus minimizing the effect of the inrush current in the inductor. Variable u is a binary signal that activates MOSFET Q. Note that the inner loop uses an auxiliary ramp to preclude the existence of subharmonics. This type of linear control has been used extensively in the case of resistive load [56] and has been applied to the case of a boost converter feeding a CPL [30], although the validity of the design has been demonstrated only by simulations performed basically in the frequency domain.

The transfer functions given in (1.25) and (1.26) are used to design the control.

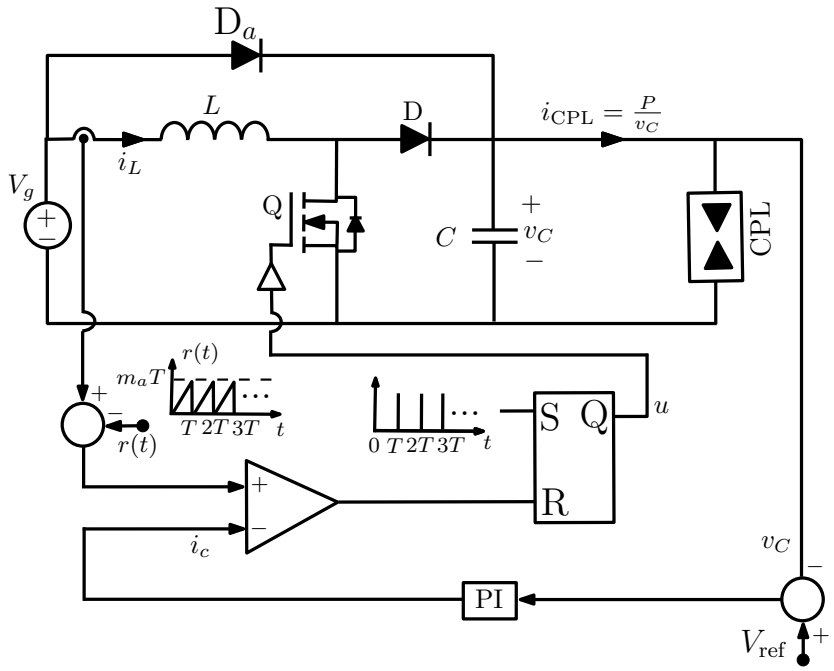


Figure 3.1: Block diagram of a two-loop linear analog control of a boost converter loaded with a CPL

3.2.1 Inner Loop based on a Peak-Current Mode Control

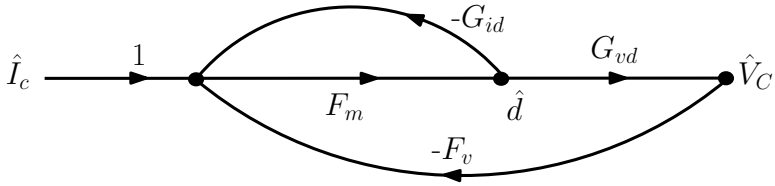
The dynamic model of the inner current loop is shown in Fig 3.2(a). F_m is associated with the artificial ramp $r(t)$ and F_v is a gain specific for each converter. The expression of F_m and F_v for the boost converter are given as follows [56]

$$F_m = \frac{1}{m_a T}, \qquad F_v = \frac{(1-D)^2 T}{2L} \tag{3.1}$$

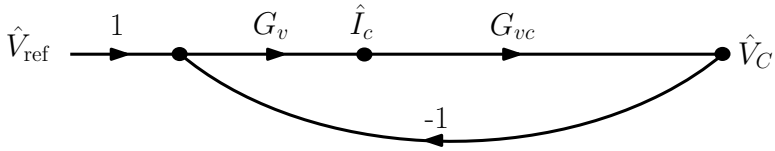
Therefore, from Fig 3.2(a), the transfer function relating the output voltage ($\hat{V}_C(s)$) and the control signal ($\hat{I}_c(s)$) becomes

$$G_{vc}(s) = \frac{\hat{V}_C(s)}{\hat{I}_c(s)} = \frac{F_m G_{vd}}{1 + G_{id} F_m + F_m G_{vd} F_v} \tag{3.2}$$

Chapter 3. Two approaches for the closed-loop operation of power converter with CPL in CCM



(a) Inner control loop



(b) Two-loop control

Figure 3.2: Dynamic models of the two control loop PWM linear analog control.

Substitution of (1.25), (1.26) and (3.1) into (3.2) yields

$$G_{vc}(s) = \frac{P}{CV_C^* m_a T(1-D)} \frac{s - \frac{(1-D)^2}{LP} V_C^{2*}}{s^2 + s(\frac{2CV_C^{*3} - P(2m_aLT + (1-D)V_C^*T)}{2LCm_aTV_C^{*2}}) + \frac{(1-D)^2}{LC}(1 + \frac{(1-D)V_C^*}{2Lm_a})} \tag{3.3}$$

According to (3.3) the system with a simple CMC will be stable if the following constraint is satisfied

$$P < \frac{2CV_C^{*3}}{T(2m_aL + (1-D)V_C^*)} \tag{3.4}$$

3.2.2 Outer Loop based on a PI Compensator

In order to ensure the system stability while voltage regulation is achieved, an outer loop is proposed. The voltage controller is a PI compensator, which provides the reference for the inner loop. The transfer function for the outer PI compensator $G_v(s)$ can be expressed as follows

$$G_v(s) = \frac{K_{pa}s + K_{ia}}{s} \tag{3.5}$$

where K_{pa} and K_{ia} are the proportional gain and the integral gain respectively.

The dynamic model of the two-loop control is illustrated in Fig 3.2(b). Hence, the

loop gain of the system $\mathcal{L}(s) = G_v(s)G_{vc}(s)$ becomes

$$\mathcal{L}(s) = -K\frac{(s-z_1)(s+z_2)}{s(s^2+2\xi\omega_0 s+\omega_0^2)} \tag{3.6}$$

where,

$$K = \frac{K_{pa}P}{CV_C^* m_a T(1-D)} \tag{3.7a}$$

$$z_1 = \frac{(1-D)^2}{LP}V_C^{2*} \tag{3.7b}$$

$$z_2 = \frac{K_{ia}}{K_{pa}} \tag{3.7c}$$

$$\xi = \frac{\frac{1}{2}(-\frac{P}{CV_C^2}+\frac{V_C^*}{m_a LT}-\frac{P(1-D)}{2m_a LCV_C^*})}{\frac{(1-D)}{L}\sqrt{\frac{L}{C}+\frac{(1-D)V_C}{2Cm_a}}} \tag{3.7d}$$

$$\omega_0 = \frac{1-D}{L}\sqrt{\frac{L}{C}+\frac{(1-D)V_C}{2Cm_a}}, \tag{3.7e}$$

From (3.6), it can be noted that, there will be one zero in the RHP (z_1) and one zero in the LHP (z_2). Considering $K > 0$, the system feedback will be positive. Besides, assuming $s^2+2\xi\omega_0 s+\omega_0^2 = (s+p_1)(s+p_2)$, where $p_1, p_2 > 0$, the system stability will depend on the value of K, which is proportional to the power P of the CPL.

3.2.3 Simulation Results

The control previously described for the boost converter under CPL, is now studied by PSIM© simulations. Fig 3.3 shows the pole-zero map of the system for the circuit diagram of Fig. 3.1 with the parameter values for the converter given in Table 3.1 and the following control parameter values $K_{pa} = 1$, $K_{ia} = 1000$, $T = 10$ μs and $m_a = 460$ kV/s.

Table 3.1: The used parameter values for the boost converter supplying a constant power.

L	C	P	V_g	V_{ref}
326 μH	20 μF	1 kW	200 V	350 V

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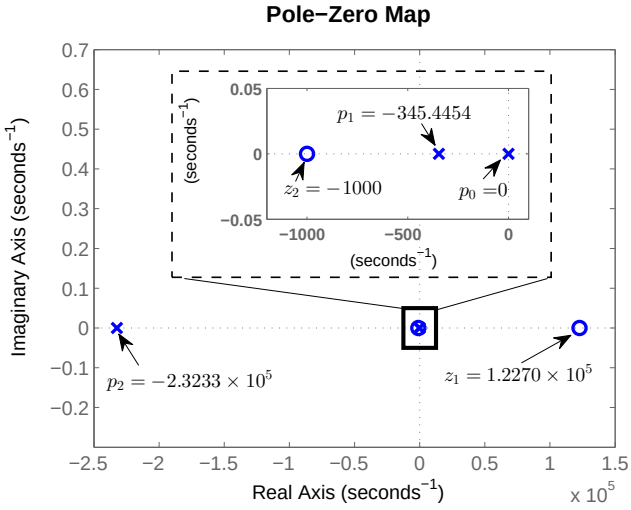
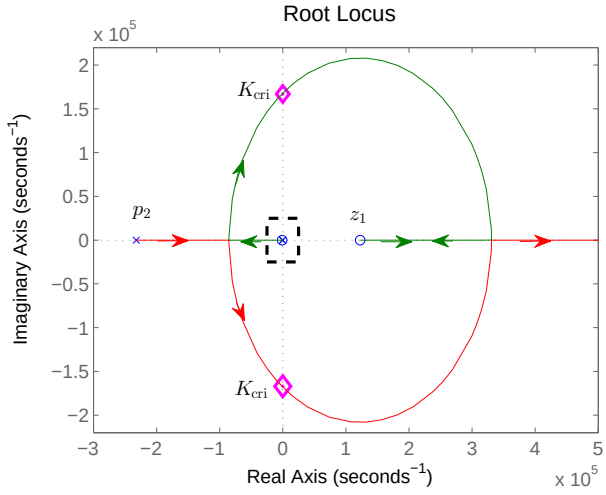


Figure 3.3: Pole-zero map in s-plane of the boost converter supplying CPL under the proposed control.

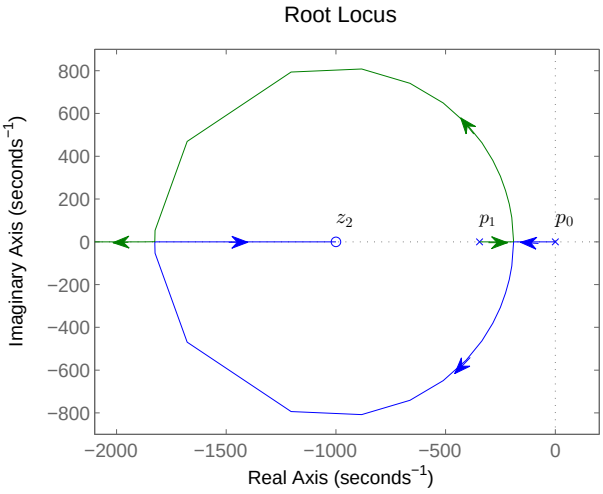
As can be observed, there is one zero in the RHP, which corresponds to the non-minimum phase exhibited by boost converters. In Fig. 3.4 it can be observed the root locus of the system and the risk of instability for a critical value of P ($P_{\text{cri}} = \frac{K_{\text{cri}} C V_C^* m_a T(1-D)}{K_{pa}}$).

Fig. 3.5 depicts the transient response of the converter in start-up and in steady-state. It can be observed a very large inadmissible inrush current in Fig. 3.5(a) and Fig. 3.5(b). In order to avoid the inrush current, the output of the PI compensator can be limited during the start-up to a maximum level I_{clim}, which significantly reduces the inrush current as illustrated in Fig. 3.5(c) and Fig. 3.5(d), where $I_{\text{clim}} = 10$ A. It is worth remarking that for this control it is mandatory to use a soft-start technique that allows the converter to reach the equilibrium point without any risk of damage to the system.

Fig. 3.6 illustrates the converter waveforms in front of changes of step type in the power load from 1 kW to 0.5 kW and restored back. Note a good regulation in the capacitor voltage, a negligible overshoot and undershoot during the transitions and a recovery of 5 ms approximately, after every transition.



(a) Root locus

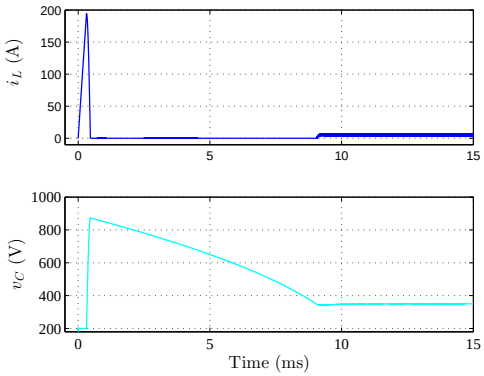


(b) Zoom of the root locus

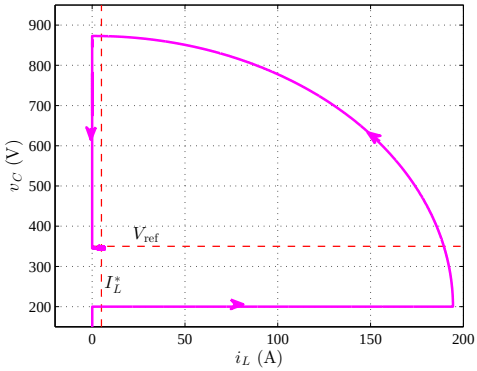
Figure 3.4: Root locus of the of the system.

On the other hand, the two-loop control, in front of changes of step type in the input voltage from 200 V to 250 V and again to 200 V, shows a good performance as is corroborated in Fig. 3.7. Note that the overshoot and the undershoot are less than 0.5% in every perturbation and the capacitor voltage remains at its reference value 350 V.

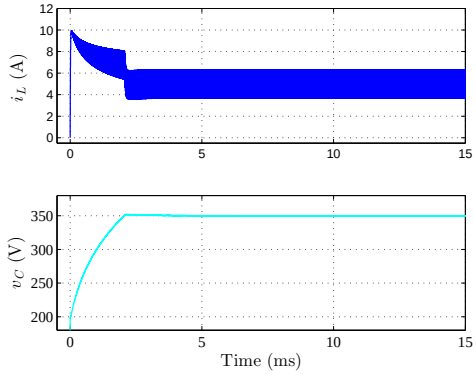
Chapter 3. Two approaches for the closed-loop operation of power converter with CPL in CCM



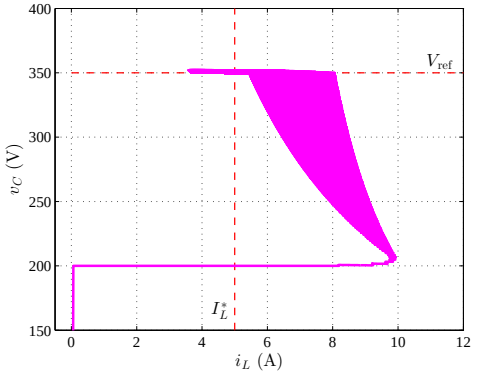
(a) Time domain



(b) Phase-plane $i_L - v_C$



(c) Time domain



(d) Phase-plane $i_L - v_C$

Figure 3.5: Start-up and steady state of the boost converter under CPL with the two-loop control without soft-start ((a)-(b)) and with soft-start((c)-(d)).

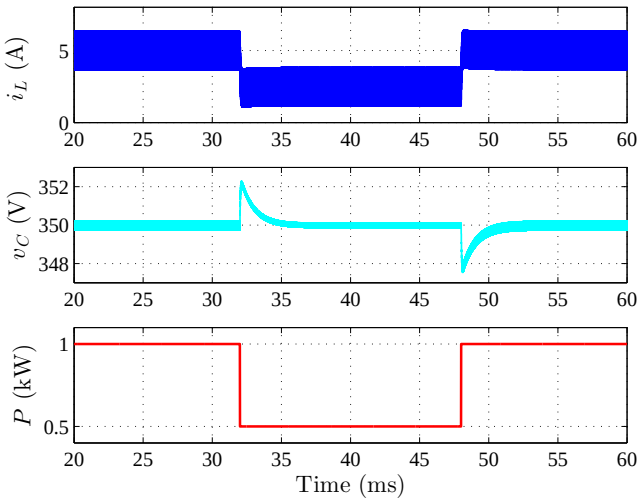


Figure 3.6: Numerical simulation of the boost converter under the two-loop control in front of power load changes (1 kW → 0.5 kW at 32 ms, 0.5 kW → 1 kW at 48 ms).

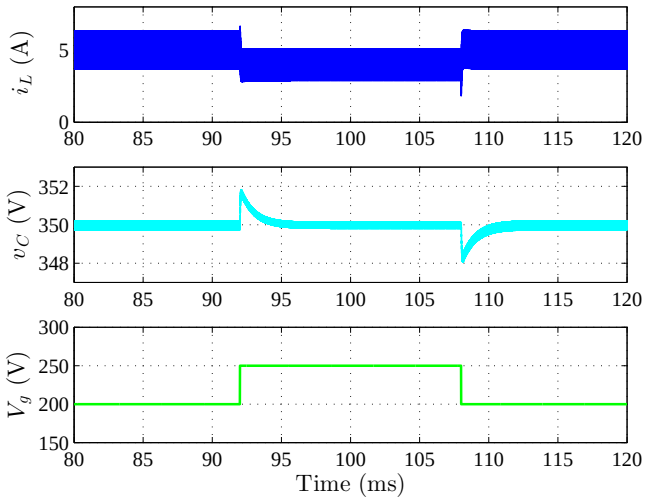


Figure 3.7: Numerical simulation of the boost converter under two-loop front of input voltage changes (200 V → 250 V at 92 ms, 250 V → 200 V at 108 ms).

3.3 SMC of a Boost Converter with CPL

In Section 1.3, the unstable behaviour of the boost converter with a CPL, during the ON and OFF intervals has been demonstrated. Also, in the previous section it has been shown that a linear control has some disadvantages for the control of the system, mainly during the start-up. In this section an SMC is proposed to regulate the boost converter feeding a CPL. SMC method offers a natural way to control switching converters, by combining their ON and OFF vector state trajectories allowing to drive the system from zero initial conditions to the desired equilibrium point.

From Fig. 1.5, the corresponding state equations of the converter can be expressed as follows

$$\frac{di_L}{dt} = -\frac{v_C}{L}(1-u) + \frac{V_g}{L} \tag{3.8a}$$

$$\frac{dv_C}{dt} = \frac{i_L}{C}(1-u) - \frac{P}{Cv_C} \tag{3.8b}$$

3.3.1 Equilibrium Point Locus

The equilibrium points locus (EPL) is obtained assuming that the derivatives of the trajectories in the phase-plane during ON and OFF states are opposite with equal absolute value [57].

$$\left.\frac{dv_C}{di_L}\right|_{T_{\text{ON}}} = -\left.\frac{dv_C}{di_L}\right|_{T_{\text{OFF}}} \tag{3.9}$$

According to (3.9), the EPL is given by:

$$i_L = \frac{P}{V_g} \tag{3.10}$$

3.3.2 Sliding Surface

It is apparent that an equilibrium point (EP) can result from the intersection of the switching surface and the EPL provided than an appropriate switching policy can be imposed to the converter. This switching policy has to combine unstable trajectories

to create a trajectory that slides on average along the switching surface to attain the desired equilibrium point of the switching converter.

The basic idea in the use of SMC is illustrated in Fig. 3.8, where the switching policy consists in turning ON the switch when the state vector trajectory is below the switching surface and turning OFF the switch when the trajectory is above the surface.

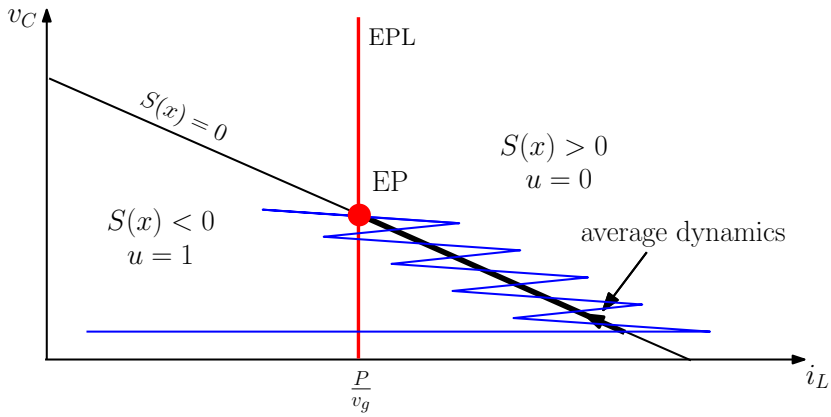


Figure 3.8: Combining ON and OFF trajectories to create a stable trajectory that attains the desired equilibrium point from zero initial conditions.

A simple sliding surface like the one depicted in Fig. 3.8 is the linear combination of the errors of the state variables i_L and v_C, with respect to their steady-state values. Hence, the proposed linear sliding surface is $\Sigma = \{x|S(x) = 0\}$, $S(x)$ being as follows

$$S(x) = K_C(v_C - V_{\text{ref}}) + K_L(i_L - I_{\text{ref}}) \tag{3.11}$$

where V_{ref} and I_{ref} are the reference values for the capacitor voltage and inductor current respectively, and K_C, K_L are positive constant gains. The corresponding switching policy will be implemented as illustrated in Fig. 3.9.

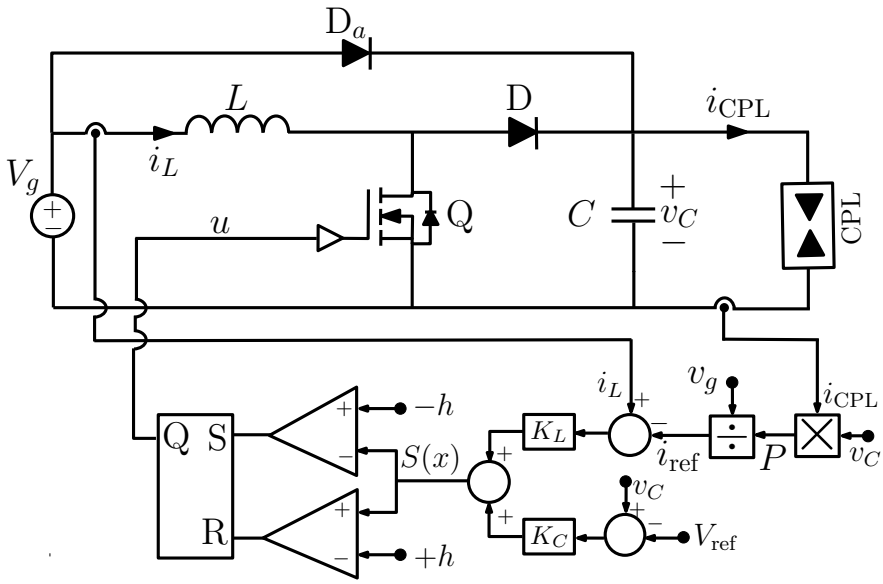


Figure 3.9: Block diagram of a SMC of a boost converter loaded with a CPL

3.3.3 Equilibrium Point

The coordinate of the equilibrium point (I_L^*, V_C^*), can be expressed as follows

$$I_L{}^* = \frac{P}{V_g} \tag{3.12a}$$

$$V_C{}^* = V_{\text{ref}} - \frac{K_L}{K_C}\left(\frac{P}{V_g} - I_{\text{ref}}\right) \tag{3.12b}$$

Note that a necessary and sufficient condition for the existence of an equilibrium point, is that the EPL and Σ intersect. Hence, the gain K_C cannot be null, because it leads to the inexistence of the equilibrium point. This is in a clear contrast with the case of a resistive load where a stable equilibrium point always exists for the case of $K_C = 0$.

According to (3.12a), it can be concluded that the switching surface defined by (3.11) with a constant value of I_{ref} cannot in general ensure an output voltage regulation in front of input voltage variations or output power changes. To circumvent this problem, without inserting an integrator in the feedback loop, we propose an adaptive law to update the current reference $i_{\text{ref}} = P/V_g$ for each pair of the instantaneous input

voltage V_g and power P. Hence, the sliding surface in (3.11) can be rewritten as follows

$$S(x) = K_C(v_C - V_{\text{ref}}) + K_L(i_L - \frac{P}{V_g}) \tag{3.13}$$

Consequently, the new coordinates of the equilibrium point of the system are given by

$$I_L{}^* = \frac{P}{V_g} \tag{3.14a}$$
$$V_C{}^* = V_{\text{ref}} \tag{3.14b}$$

3.3.4 Control Law and Existence Sliding Mode Condition

To maintain the system trajectory in the vicinity of the sliding surface, the following control law is established

$$\begin{array}{lll} u = 0 & \text{if} & S(x) > 0 \\ u = 1 & \text{if} & S(x) < 0 \end{array} \tag{3.15}$$

Sliding motions will exist if the condition $S\dot{S} > 0$ is satisfied, which implies

$$\begin{array}{lll} \dot{S}(x) < 0 & \text{if} & S(x) > 0 \\ \dot{S}(x) > 0 & \text{if} & S(x) < 0 \end{array} \tag{3.16}$$

Differentiating (3.13) results in

$$\dot{S}(x) = K_C\frac{dv_C}{dt} + K_L\frac{di_L}{dt} \tag{3.17}$$

Substitution of (3.8) into (3.17) leads to the following expression

$$\dot{S}(x) = (\frac{K_C i_L}{C} - \frac{K_L v_C}{L})(1-u) - \frac{K_C P}{C v_C} + \frac{K_L V_g}{L} \tag{3.18}$$

Hence, from (3.18) and (3.15), (3.16) results in

$$\frac{K_C i_L}{C} - \frac{K_L v_C}{L} < \frac{K_C P}{C v_C} - \frac{K_L V_g}{L} \quad \text{for} \quad u = 0 \tag{3.19}$$
$$-\frac{K_C P}{C v_C} + \frac{K_L V_g}{L} > 0 \quad \text{for} \quad u = 1 \tag{3.20}$$

It can be observed that the first term of the inequality in (3.20) is equal to the second term of the inequality in (3.19) but with negative value; thus, combining both expressions results in one inequality given by

$$\frac{K_C i_L}{C} - \frac{K_L v_C}{L} < \frac{K_C P}{C v_C} - \frac{K_L V_g}{L} < 0 \tag{3.21}$$

Solving (3.21) for i_L leads to:

$$i_L < \frac{CK_L v_C}{K_C L} - \frac{CK_L V_g}{K_C L} + \frac{P}{v_C} < 0 \tag{3.22}$$

From the above equation, the Existence Sliding Mode (ESM) region will be determined by

$$i_L < f(v_C) \tag{3.23}$$

where $f(v_C)$ is defined as follows

$$f(v_C) = \frac{1}{v_C}\left(\frac{CK_L}{LK_C}v_C^2 + P\right) - \frac{CK_L V_g}{LK_C} \tag{3.24}$$

Note that function $f(v_C)$ has a minimum (M) for $v_C = \sqrt{PLK_C/CK_L}$ whose value is given by

$$M = \sqrt{\frac{CK_L}{LK_C}}\left(2\sqrt{P} - \sqrt{\frac{CK_L}{LK_C}}V_g\right) \tag{3.25}$$

The minimum value in (3.24) can be, positive $(M > 0)$, null $(M = 0)$ and negative $(M < 0)$. In the case of $M < 0$, $f(v_C)$ will be negative for $v_1 > v_C > v_2$, where

$$v_1 = \frac{V_g}{2} + \frac{1}{2}\sqrt{V_g^2 - \frac{4LK_C P}{CK_L}} \tag{3.26a}$$

$$v_2 = \frac{V_g}{2} - \frac{1}{2}\sqrt{V_g^2 - \frac{4LK_C P}{CK_L}} \tag{3.26b}$$

Fig 3.10 shows $f(v_C)$ for the different cases of M and their corresponding ESM region in the $v_C - i_L$ state-plane. Also, it can be observed the sliding surface $S(x) = 0$, the EPL and the equilibrium point.

3.3.5 Equivalent Control

The ideal sliding dynamics corresponding to the average trajectory of the converter on the switching surface can be expressed in terms of the equivalent control (u_{eq}), by imposing the condition $S(x) = 0$ and $\dot{S}(x) = 0$. Hence, u_{eq} can be expressed as follows

$$u_{eq} = 1 - \frac{K_L(K_C LP - K_L C V_g v_C)}{v_C(LK_L K_C P/V_g + V_{\text{ref}} LK_C^2 - v_C(LK_C^2 + CK_L^2))} \tag{3.27}$$

Note that, introducing the coordinates of the equilibrium point (3.14) into (3.27) yields to the equivalent control in steady-state

$$U_{eq} = \frac{V_{\text{ref}} - V_g}{V_{\text{ref}}} \tag{3.28}$$

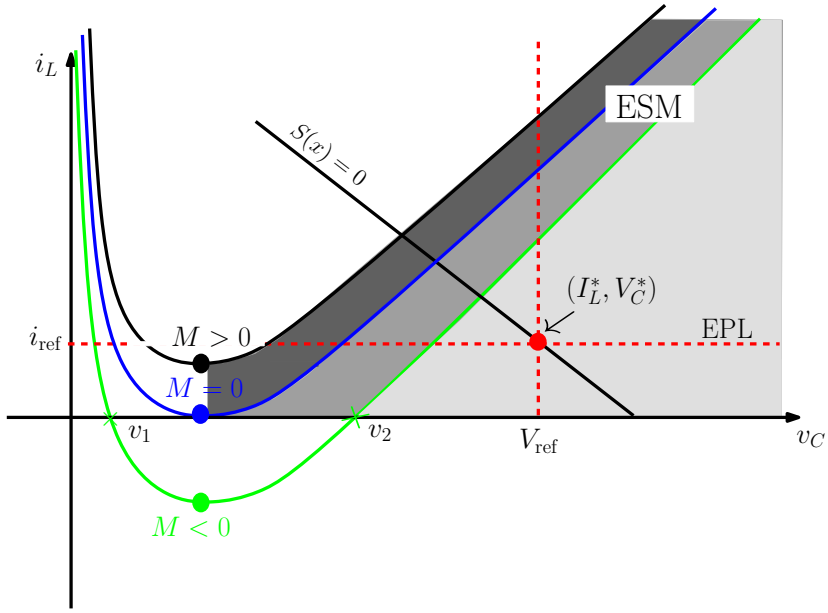


Figure 3.10: Plot of $f(v_C)$ for different values of M, ESM region, $S(x)$, EPL and equilibrium point.

3.3.6 Ideal Sliding Dynamics

The ideal sliding dynamics is obtained by substituting (3.27) for the control action u in (3.8), yielding

$$\frac{dv_C}{dt} = \frac{1}{Cv_C}\left(\frac{i_L K_L (K_C LP - K_L C V_g v_C)}{LK_L K_C P/V_g + V_{\text{ref}} LK_C^2 - v_C(LK_C^2 + CK_L^2)} - P\right) \tag{3.29a}$$

$$\frac{di_L}{dt} = -\frac{1}{L}\left(\frac{K_L (K_C LP - K_L C V_g v_C)}{LK_L K_C P/V_g + V_{\text{ref}} LK_C^2 - v_C(LK_C^2 + CK_L^2)} + V_g\right) \tag{3.29b}$$

Substituting (3.13) in (3.29) and solving for the differential equations in equilibrium corroborate that the coordinates of the equilibrium point $(P/V_g, V_{\text{ref}})$ correspond to the desired values given by (3.14).

One order reduction of the system dynamics is inherently imposed in (3.29) due to the action of sliding-mode. From (3.29a) and the condition $S(x) = 0$, the ideal sliding dynamics in terms of the output capacitor voltage is as follows

$$C\frac{dv_C}{dt} = \frac{K_1 v_C^2 + K_2 v_C + K_3}{K_4 v_C^2 + K_5 v_C} - \frac{P}{v_C} = f_2(v_C), \tag{3.30}$$

where K_1, K_2, K_3, K_4 and K_5 are given by

$$\begin{aligned} K_1 &= K_C K_L C V_g \\ K_2 &= -(K_L^2 C P + K_C K_L C V_{\text{ref}} V_g + L K_C^2 P) \\ K_3 &= K_C K_L L \frac{P^2}{V_g} + L K_C^2 V_{\text{ref}} P \\ K_4 &= -(L K_C^2 + C K_L^2) \\ K_5 &= L K_C K_L \frac{P}{V_g} + L K_C^2 V_{\text{ref}} \end{aligned} \tag{3.31}$$

The equilibrium point of (3.30) is $V_C^* = V_{\text{ref}}$. Let $v_C = V_{\text{ref}} + \hat{v}_C$, linearizing (3.30) around V_C^* leads to

$$\frac{d\hat{v}_C}{dt} = \left.\frac{df_2(v_C)}{dv_C}\right|_{v_C = V_C^*} \hat{v}_C := \lambda \hat{v}_C \tag{3.32}$$

The previous differential equation will be stable if $\lambda < 0$, implying the existence of an upper limit on the power, *i.e.* the condition $P < P_{\text{max}_{\text{SMC}}}$ must hold for the ideal sliding dynamics to be stable, where

$$P_{\text{max}_{\text{SMC}}} = \frac{C K_L V_{\text{ref}} V_g}{K_C L} \tag{3.33}$$

3.3.7 Analysis of Switching Surface

In this part, the effects of the sliding surface parameters K_C and K_L will be analyzed. The sliding surface is a straight line with negative slope. Hence, from (3.13) the following statements can be asserted

1) For $K_C = 0$, the sliding surface becomes $S(x) = K_L(i_L - i_{\text{ref}})$ which corresponds to a vertical line defined by $i_L = i_{\text{ref}}$. That case is equivalent to a CMC. Due to the fact that the switching surface and the EPL are the same, the ideal sliding dynamics will evolve through that line, *i.e.* the inductor current will be equal to the reference value of the current.

2) For $K_L = 0$, the sliding surface takes the form $S(x) = K_C(v_C - V_{\text{ref}})$ which corresponds to a horizontal line defined by $v_C = V_{\text{ref}}$. That case is a Voltage-Mode Control (VMC).

3) For the case that $K_C \to 0$, the sliding surface will approach to the straight line given by $i_L = i_{\text{ref}}$. On the contrary, if $K_L \to 0$, $S(x)$ will approach to the horizontal line determined by $v_C = V_{\text{ref}}$. Hence, it can be concluded that the family of straight lines $S(x) = 0$ is contained within the sector defined by $i_L = i_{\text{ref}}$ (CMC) and $v_C = V_{\text{ref}}$ (VMC). Besides, the slope of the straight line defined by the sliding surface is given by $-K_L/K_C$.

4) For certain values of K_L and K_C, conditions (3.23) and (3.33) cannot be accomplished, consequently, there will be no sliding mode .

5) The inrush current will depend on the slope of $S(x) = 0$. Therefore, in order to achieve small values of inrush current, K_C must be much smaller than K_L.

Fig. 3.11 illustrates the different combinations of K_L and K_C, which results in a family of straight lines constrained by two limits: CCM and VMC.

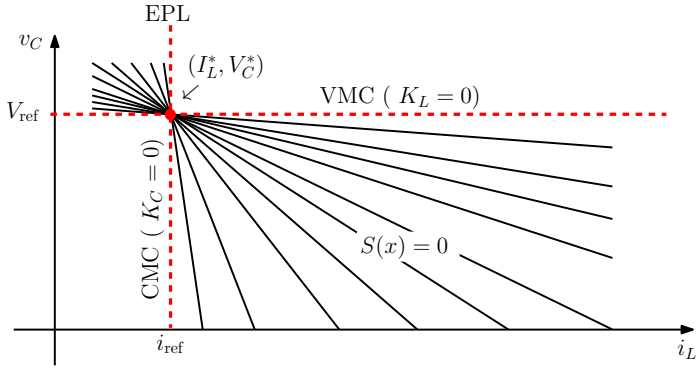


Figure 3.11: Family of switching surfaces for different combinations of K_L, K_C.

3.3.8 Numerical Simulations

A series of simulations have been carried out to validate the correct performance of the system with the proposed control and the theoretical predictions. The block diagram of Fig. 3.9 has been implemented in PSIM© software for the set of parameter values depicted in Table 3.1. The diode D_a is used during the start-up to mitigate the inrush current, thus $v_C(0) = V_g$ is assured. A hysteresis comparator with a hysteresis width

Table 3.2: Different combinations of K_L and K_C corresponding to Fig. 3.12 .

Combination	1	2	3	4	5	6
K_L	21 Ω	100 Ω	150 Ω	350 Ω	100 Ω	450 Ω
K_C	10	15	15	15	2	2

$h = 140$ V has been used to limit switching frequency. In the experimental prototype the value of h is appropriately scaled down. The resulting nominal switching frequency is $f_s = 100$ kHz. Besides, in order to generate the current reference, the load current i_{CPL} and the output voltage v_C are multiplied, to obtain P, which is divided by the input voltage V_g.

As described in Section 3.3.7 the values of K_L and K_C play an important role in the system control. In Fig. 3.12 the simulation of the system behavior is shown for the sliding surface, resulting from each pair of K_L and K_C given in Table 3.2.

It can be noted that the smallest proposed value of K_C correspond to the combination 5 and 6 but the smallest inrush current will be achieved with the combination 6 because the ratio K_L/K_C is greater than in combination 5. On the other hand, the smallest proposed value of K_L is in the combination 1. In this case, it is obvious that the system trajectory does not reach the sliding surface since condition (3.23) is not fulfilled. Furthermore, it can be noted that the fastest output voltage response is achieved for the sliding surfaces with the smallest ratio K_L/K_C but at the expense of high inrush current, as illustrated by combination 2. Therefore, in order to obtain a good compromise between a low inrush current and fast output voltage response, the rest of simulations have been carried out using combination 5.

The ESM region for the desired operation values of the converter and the chosen values of K_L and K_C are illustrated in Fig. 3.13(a) in the i_L-v_C state-plane. Note that in this case the minimum of function $f(v_C)$ defined in (3.25) is negative for v_C =18 V and from (3.26), v_1=198.35 V and v_2=1.64 V. The ESM region determined by (3.22) is colored in gray color.

Fig. 3.13(b) shows the ESM region near the equilibrium point of the system, as well as the switching surface $\Sigma = \{x|S(x) = 0\}$, EPL and V_{ref}. In this figure, the points

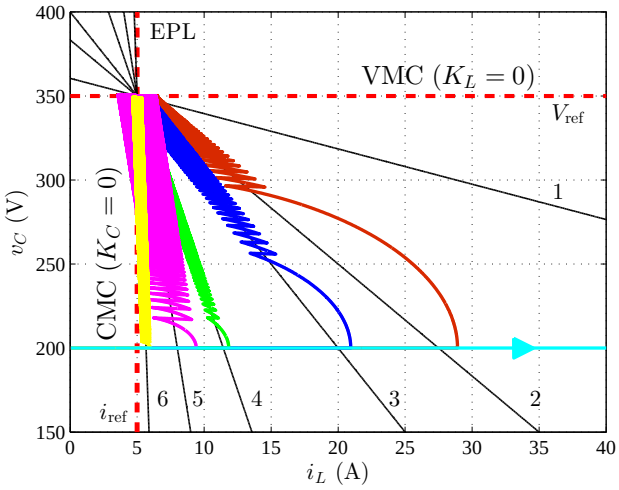


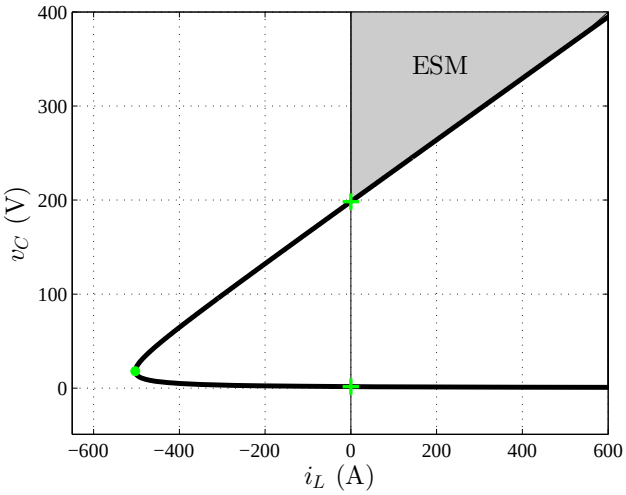
Figure 3.12: Switching surfaces and trajectories with different values of K_L and K_C.

P_1, P_2 and P_3 are different initial conditions for $(i_L(0), v_C(0))$. It can be observed that P_1 and P_2 are outside of the ESM area and consequently do not accomplish condition (3.22), therefore the trajectories starting from these points cannot slide until they arrive to the region of ESM. On the contrary, P_3 starts inside of the ESM region and its trajectory quickly reaches the equilibrium point without any inrush current. In general, for the point of operation, the use of the auxiliary start-up diode (D_a) ensure that $v_C(0) = V_g$, hence the starting point is inside of the ESM region given by (3.22).

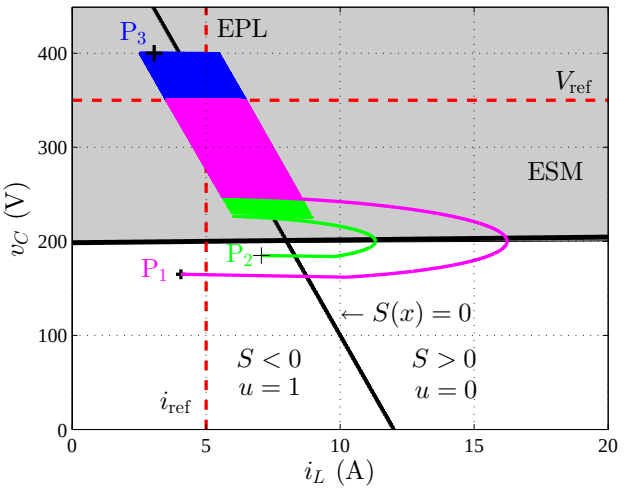
3.4 Simulation and Experimental Results of the Prototype

In order to verify the theoretical predictions in the time domain, numerical simulations in PSIM© software and experimental tests in a prototype have been performed.

Fig. 3.14 shows the power stage and SMC stage of the boost converter with CPL employed in the experimental study. In the power stage, the main switch is based on the complementary action of diode D(IDH20G655C5) and MOSFET Q(STW25NM60ND), activated with the driver MAX4420. Also, the auxiliary diode for start-up is IDH20G655C5. Two current sensors LA 25NP have been employed to measure the inductor current i_L



(a) ESM region



(b) Start-up trajectories from different initial conditions.

Figure 3.13: Region of existence of sliding-mode for the boost converter with CPL.

and the output current i_{CPL} respectively. Input voltage and output voltage are sensed by a voltage divider. The inductor current, output current, output voltage and input voltage are proportional to their respective measured signals. The SMC stage has different blocks, namely, current reference, current error, voltage error and hysteresis

Table 3.3: Summary of components used for the boost converter.

Parameter	Reference
L	design
C	MKP1848C61060JK2
D,D$_a$	IDH20G65C5
Q	STW25NM60ND
driver	MAX4420CPA
V_g	SPS800X13
CPL	EA-EL 9000 HP Series

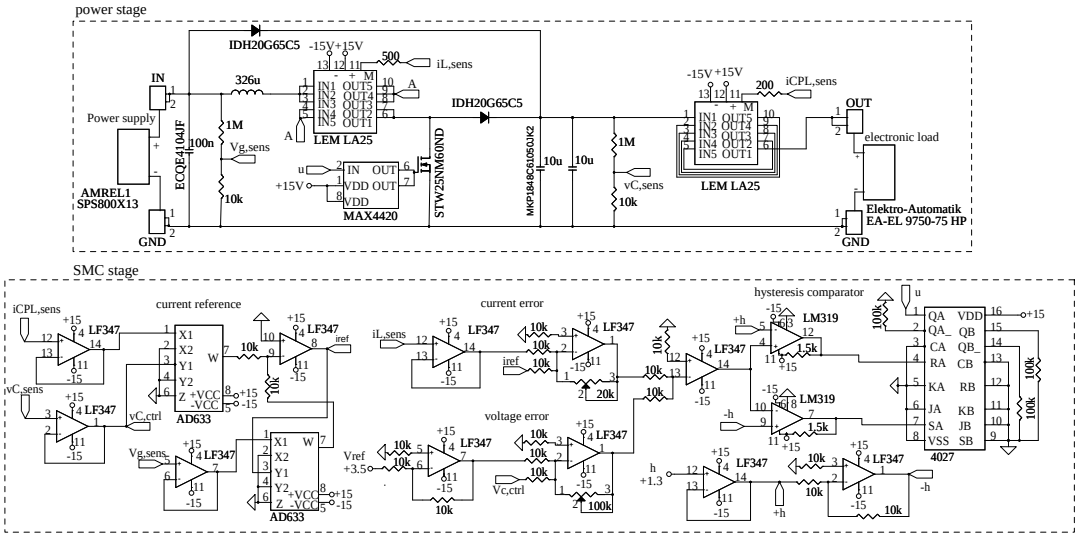


Figure 3.14: Schematic circuit diagram of the experimental prototype of the boost converter with the proposed SMC

comparator. The current reference corresponds to the adaptive modification proposed in Section 3.3.3 and consist in calculating P, by multiplying the signals of the output current and capacitor voltage, and then dividing it by the input voltage. Both calculations are processed by IC AD633. The current and voltage errors are processed by circuits based on OA LF347. These errors are added by a linear circuit based on AO LF347 to obtain the switching function $S(x)$. The hysteresis comparator is of LM319

type, so that one internal circuit compares the switching surface with the negative hysteresis level and the other one compares the function $S(x)$ with the positive hysteresis level. The pulses for the driver are generated by the Flip-Flop CD4027, which is adapted to the comparator output.

The CPL has been emulated by the electronic load EL 9000 from ELEKTRO-AUTOMATIK operating in constant power mode.

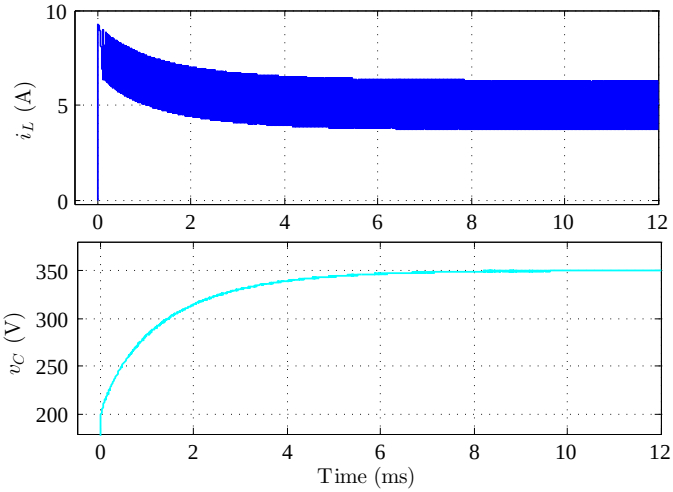
The simulation of the converter start-up and the steady-state behavior is shown in Fig. 3.15(a). Note that the inrush current is not significant and the steady-state is attained in 9 ms, which is similar to that obtained with the two-loop linear control. Besides, from the observation of the waveform i_L is evident the one order reduction introduced by the sliding motion. Fig. 3.15(b) shows in the state-plane $i_L - v_C$ the converter trajectories, starting from zero initial conditions.

The values of v_C and i_L in steady-state are 350 V and 5 A as depicted in Fig. 3.16, which corroborates the predicted values given by (3.14). Furthermore, the switching frequency has the desired value of 100 kHz according to the choice of hysteresis width h. The inductor current ripple corresponds to the expected value (2.5 A). Hence, the experimental results are very close to the simulated ones.

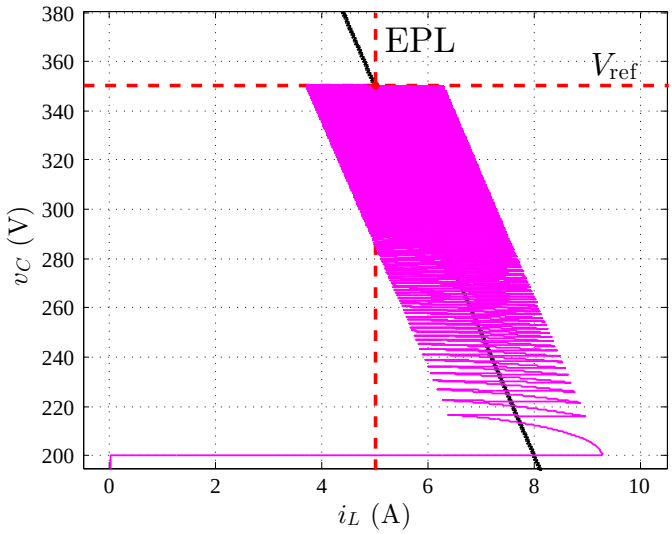
Fig. 3.17(a) and Fig. 3.17(b) verify the previous theoretical prediction by illustrating the response of the converter to power changes of step type in the power of CPL. The power absorbed by the load changes first from 1 kW to 500 W and then restored back. The experimental results in Fig. 3.17(b) corroborate the PSIM© simulations in Fig. 3.17(a). A negligible voltage steady-state error of 2% due to unmodelled resistive losses is observed in the experimental results. It is worth to remark the concordance between theoretical predictions, simulation results and experimental results.

Fig. 3.18 shows the converter simulation waveforms in front of a perturbation in the input voltage V_g from 200 V to 250 V and restored back. Note that the capacitor voltage is maintained at its desired value $V_{\text{ref}} = 350$ V. However, the inductor current steady-state I_L^* absorbs the perturbation and changes from 5 A to 4 A according to (3.14a).

Finally, it has to be pointed out that the switching frequency changes with the value of the equilibrium point. For example, for the cases illustrated in Fig. 3.17 $f_s = 100$ kHz



(a) Time domain waveforms.

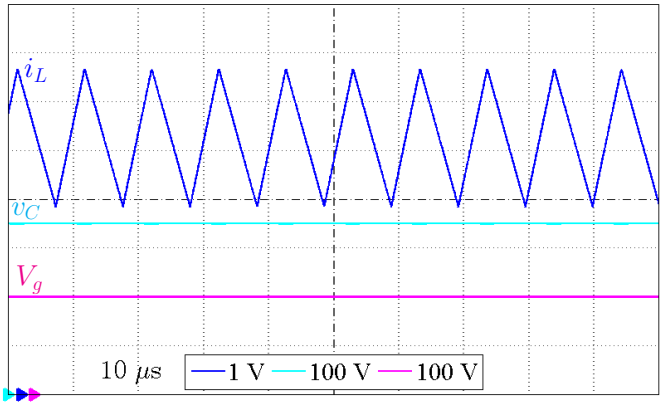


(b) State-plane $i_L - v_C$.

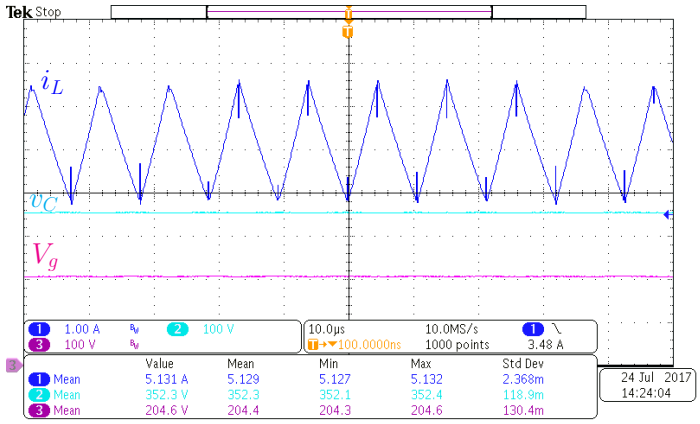
Figure 3.15: System response during start-up.

when $P = 1$ kW, and $f_s = 102$ kHz when $P = 0.5$ kW, while for the cases shown in Fig. 3.18 $f_s = 84$ kHz when $V_g = 250$ V and $f_s = 100$ kHz when $V_g = 200$ V.

Chapter 3. Two approaches for the closed-loop operation of power converter with CPL in CCM

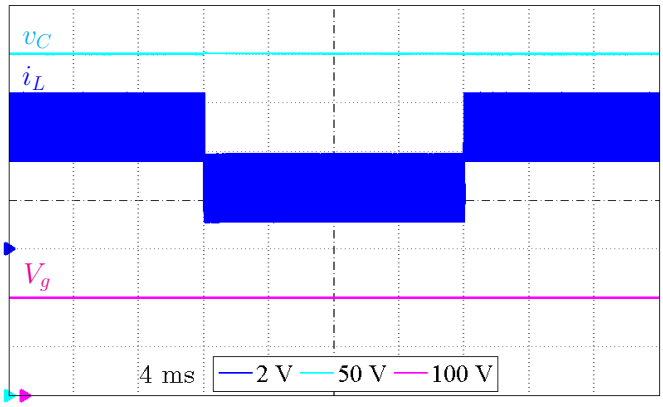


(a) PSIM© simulation result

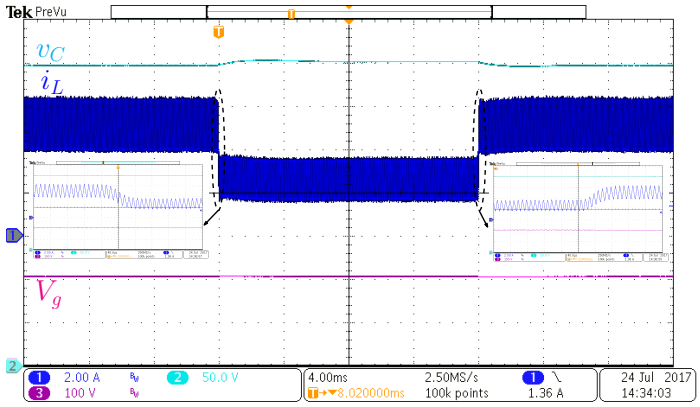


(b) Experimental Result

Figure 3.16: Steady-state waveforms of the boost converter supplying a CPL ($P = 1$ kW).



(a) PSIM© simulation result



(b) Experimental Result

Figure 3.17: Waveforms of the boost converter for power changes of step type in the CPL (from 1 kW to 500 W and restored back to 1 kW).

Chapter 3. Two approaches for the closed-loop operation of power converter with CPL in CCM

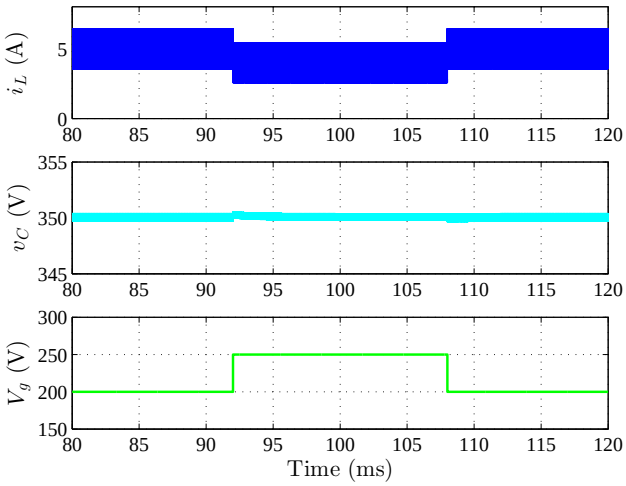


Figure 3.18: Simulation waveforms of the converter for input voltage V_g changes from 200 V to 250 V at 92 ms and from 250 V to 200 V at 108 ms.

Chapter 4

Two-loop PWM-digital SMC of Boost Converter with CPL

4.1 Introduction

Chapter 3 has shown that SMC based on the use of a linear switching surface is an effective solution to regulate the boost converter feeding a CPL. The switching surface leads to small values of inrush current and guarantees output voltage regulation in front of external perturbations. The voltage regulation is achieved by adapting the current reference in terms of the input voltage and the power of the CPL making it equal to the expression of the equilibrium point locus. Hence, no linearization assumptions have been used in the controller design, this eventually resulting in a good global performance under large-signal operation.

However, the main drawback of the analog SMC solution proposed in Chapter 3 is the variable switching frequency that results from the use of hysteresis comparators in the implementation of the switching surface.

In this chapter we propose an alternative to combine a SMC strategy with constant switching frequency. The starting point is the method reported in [58, 59], which is based in a discrete-time modelling of the converter eventually resulting in a digital implementation. Digital SMC (DSMC) is a direct approach offering the advantages of analog SMC combined with a fixed switching frequency operation.

Chapter 4. Two-loop PWM-digital SMC of Boost Converter with CPL

The application of DSMC to the switching converters regulation has been always conditioned by the high switching frequency of the converters and the quasi-sliding effects caused by the sampling frequency [60, 61] constraining the application to slow system variables [62] or to reduced switching frequency cases, some of them eventually requiring a sophisticated digital hardware environment [46]. However, the application of predictive strategies has allowed the use of DSMC in the regulation of fast system variables as the inductor current operating at high switching frequencies [63]. Fixed frequency DSMC technique has recently appeared in the power electronics field. The application of DSMC theory [35] has required first a discrete-time representation of the converter dynamics, and subsequently has been used as a natural technique to analyze and to digitally implement SMC-based controllers with PWM, which have been validated in a classical two-loop control strategy [64].

4.2 Discrete-time Modeling of a Boost Converter Loaded by a CPL

4.2.1 System Description

The results presented in this section and the sections coming later correspond to the boost converter depicted in Fig. 4.1. However, the same approach can be applied to other converter topologies. The aim of the digital controller is to provide the suitable duty cycle for ensuring output voltage regulation and inducing sliding-mode regime in discrete-time. For that, the variables needed for the synthesis of the controller, are first converted into digital signals using analog-digital converters (ADC) at the rate of the sampling frequency and then processed by the controller. Selecting a proper sampling rate is important. Multi-sampling is a recently used approach in switching converters resulting in a sampling frequency larger than the switching frequency. This possibly will lead to unnecessarily overloading the digital processor. On the other hand there are also some approaches using a sampling frequency shorter than the switching frequency. With this approach the controller will possibly miss dynamics of the power stage downgrading the performances of the closed loop system. In switching converter applications, the

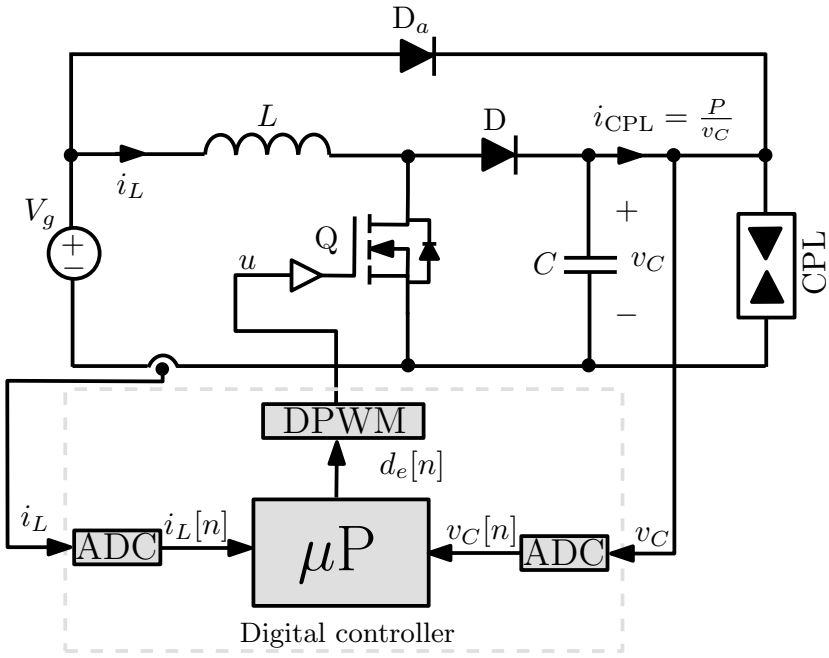


Figure 4.1: Schematic circuit diagram of a boost converter with CPL.

duty cycle is updated once per switching period; for acceptable performances, it is quite appropriate to select the sampling frequency equal to the switching frequency, which leads to a good compromise between accuracy and computing efficiency.

The regulation of the output voltage v_C is required since disturbances in the output power P and the input voltage V_g can take place. What is more, with CPL, closing the output voltage loop is also necessary for stabilizing the system since with voltage loop open the system is unstable as will be shown later. The regulation can be accomplished by an outer voltage loop making the current reference $i_{\text{ref}}[n]$ to be the output of this loop. Fig. 4.2 shows a two-loop control scheme, which is used for output voltage regulation while performing current limiting. The voltage controller consists of two stages. Namely, a digital PI block to process the error $\varepsilon[n] := V_{\text{ref}} - v_C[n]$ and a limiter to avoid that the current reference overpasses an admissible level. The current controller is based on a DSMC strategy to be described below. This controller together with the DPWM directly provides the duty cycle of the driving signal u of the converter MOSFET.

Chapter 4. Two-loop PWM-digital SMC of Boost Converter with CPL

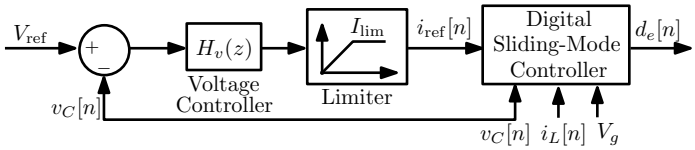


Figure 4.2: Control scheme with a two-loop voltage regulation.

4.2.2 Discrete-time Mathematical Modeling

The development of a digital controller using DSMC concepts is performed in a discrete-time state-space formulation. Hence, for DSMC design, a discrete-time model of the power stage is first needed. Due to the presence of the nonlinear CPL, such a model cannot be exactly obtained in closed form. This is because, in contrast to switching converters with linear loads, the differential equations of the system for each switch position are nonlinear and cannot be solved in closed-form. To overcome this handicap, we deal with the problem approximately by discretizing the averaged model which can be written as follows

$$\frac{d\overline{i_L}}{dt} = -\frac{\overline{v_C}}{L}(1-d) + \frac{V_g}{L} \tag{4.1a}$$

$$\frac{d\overline{v_C}}{dt} = -\frac{P}{C\overline{v_C}} + \frac{\overline{i_L}}{C}(1-d), \tag{4.1b}$$

where d is the duty cycle, $\overline{i_L}$ and $\overline{v_C}$ are respectively the average values of i_L and v_C in a switching period. All parameters and variables appearing in (4.1a) -(4.1b) can be identified in Fig. 4.1. The key issue in the discrete model is the nonlinear differential equation (4.1b) associated to the dynamics of the capacitor in parallel with the CPL. The discrete-time model corresponding to this equation cannot be obtained in closed form. Different approaches can be used for obtaining an approximate discrete-time model. These are the Euler forward, Euler backward and the Tustin (trapezoidal) methods [65]. For sufficiently small switching/sampling period, all these approximations yields to similar results. For the sake of simplicity, let us choose the Euler forward approach for obtaining the discrete-time model. A discrete-time model can be obtained by approximating the continuous-time derivatives by their equivalent rate of change,

hence assuming in the averaged model (4.1a)-(4.1b) that

$$\frac{d\overline{i_L}}{dt} \approx \frac{i_L[n+1]-i_L[n]}{T} \tag{4.2a}$$

$$\frac{d\overline{v_C}}{dt} \approx \frac{v_C[n+1]-v_C[n]}{T}, \tag{4.2b}$$

where T is the switching/sampling period. The previous forward Euler approximation leads to the following discrete-time model of the system:

$$i_L[n+1] = i_L[n] + \frac{T}{L}(V_g - v_C[n]) + \frac{T}{L}v_C[n]d_e[n] \tag{4.3a}$$

$$v_C[n+1] = v_C[n] - \frac{T}{C}i_L[n]d_e[n] + \frac{T}{C}(i_L[n] - \frac{P}{v_C[n]}) \tag{4.3b}$$

Notice that with a constant duty cycle value $d_e[n] = D_e$ (open-loop operation), the coordinates of the equilibrium point are $V_C^* = V_g/(1-D_e)$ and $I_L^* = P/V_g$. It should be noticed that the steady-state inductor current, in contrast to the case of resistive load, does not depend on the operating duty cycle and is only imposed by the power P of the CPL and the input voltage V_g. Moreover, the equilibrium point is unstable for all values of $D_e \in (0,1)$.

When sampling the state variables at the beginning of the switching cycle, depending on the modulation strategy, the samples in (4.3a)-(4.3b) can correspond to the peak values (leading-edge modulation), the valley values (trailing edge modulation) or the average values (double-edge modulation). Here, a double edge modulation will be used and the samples at the starting of each switching period will coincide with the averages.

4.2.3 Open-loop Model Validation

We will show below that the approximate discrete-time model (4.3a)-(4.3b) is enough accurate for control design. The results from this model are compared with those from the circuit-level switched model implemented in PSIM© software. Fig. 4.3 shows the samples of the capacitor voltage and the inductor current obtained from (4.3a)-(4.3b) and the waveforms of the same variables obtained from the switched model. As can be observed, there is a good agreement between the results and therefore (4.3a)-(4.3b) can be faithfully used for digital control purposes. Note that the dynamics of the inductor

current is accurately predicted and that the approximation only induces a relatively small loss of accuracy in predicting the samples of the output capacitor voltage. The small deviation can be perfectly compensated by the controller imposing the closed-loop poles at a desired position.

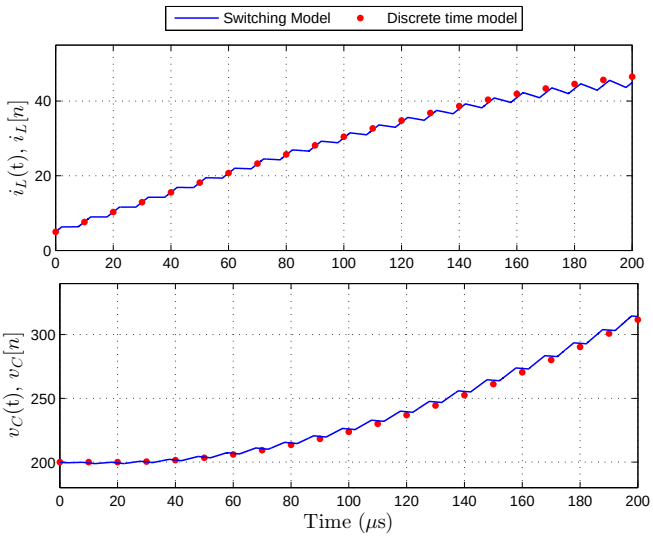


Figure 4.3: Comparison between the evolution of the state variables from the approximate discrete-time model and from the switched model implemented in PSIM© software for the parameter values given by Table 3.1 and $d_e[n] = D_e = 0.5$.

4.3 Discrete-time Sliding-mode Inner Loop Control Design

4.3.1 Large Signal Model with Voltage Loop Open

Let $\mathbf{x} = (i_L,\ v_C)^\intercal$ be the vector of the state variables of the power stage circuit. With the aim to control the samples of the inductor current $i_L[n]$ to their desired reference $i_{\text{ref}}[n]$, the following discrete-time sliding surface is used

$$\Gamma = \{\mathbf{x} | \gamma[n] := i_{\text{ref}}[n] - i_L[n] = 0\} \tag{4.4}$$

When the voltage loop is open, the current reference $i_{\text{ref}}[n]$ is given in a fixed pattern *i.e.* without any feedback loop. Although this is not a normal operation of the converter, the situation arises during start-up while limiting the inrush current and the current reference remains constant at a certain limit I_{lim} during this phase.

4.3.2 Equivalent Control

In a fixed frequency DSMC of switching converters, the duty cycle $d_e[n]$ during a certain switching period is selected in such a way that the controlled variable is imposed to catch its reference one period later. Therefore, $d_e[n]$ is obtained by imposing the discrete-time sliding-mode condition $\gamma[n+1]=0$ in (4.4) and solving for $d_e[n]$. In doing so, the following expression for the duty cycle (equivalent control) is obtained

$$d_e[n]=\frac{L(i_{\text{ref}}[n+1]-i_L[n])}{Tv_C[n]}+\frac{v_C[n]-V_g}{v_C[n]} \tag{4.5}$$

The value of the duty cycle is constrained within the interval (0,1) and its effective expression becomes

$$d_e[n]=\text{sat}(d_e[n]) \tag{4.6}$$

where $\text{sat}(\cdot)$ stands for the saturation function

$$\text{sat}(x)=\begin{cases}1 & \text{if} \quad x>1\\ x & \text{if} \quad 0<x<1\\ 0 & \text{if} \quad x<0\end{cases} \tag{4.7}$$

The saturation will not take place whenever $0<d_e[n]<1$ requiring the following condition to be satisfied:

$$i_{\text{ref}}[n+1]-\frac{TV_g}{L}<i_L[n]<i_{\text{ref}}[n+1]+\frac{T(v_C[n]-V_g)}{L} \tag{4.8}$$

At the initial time ($n=0$) without the presence of the diode D_a, the previous constraints does not hold and the system may have serious problems to startup. With initial conditions $i_L(0)=0$ and $v_C[0]=V_g$ (presence of diode D_a), the previous condition becomes

$$i_{\text{ref}}[1]<\frac{TV_g}{L} \tag{4.9}$$

If the previous constraint is not fulfilled, the system can startup easily but the duty cycle will be saturated during a few number of switching cycles.

4.3.3 DSMC Design

To guarantee convergence of the trajectories of the system to the sliding surface Γ, the following reaching conditions must hold

$$\gamma[n+1] < 0 \quad \text{if} \quad \Delta\gamma[n] > 0 \tag{4.10a}$$

$$\gamma[n+1] > 0 \quad \text{if} \quad \Delta\gamma[n] < 0 \tag{4.10b}$$

where $\Delta\gamma[n] := \gamma[n+1]-\gamma[n]$ is the increment in the variable $\gamma[n]$ during one switching cycle which can be obtained as follows

$$\Delta\gamma[n] = i_{\text{ref}}[n+1] - i_{\text{ref}}[n] + \frac{T}{L}\left((1-d_e[n])v_C[n] - V_g\right) \tag{4.11}$$

Accordingly, (4.10a)-(4.10b) become as follows

$$\frac{V_g - (1-d_e[n])v_C[n]}{L} \leq \frac{i_{\text{ref}}[n+1] - i_{\text{ref}}[n]}{T} \leq \frac{V_g}{L} \tag{4.12}$$

The above inequalities mean that the reference current rate change must be bounded between the negative and the positive slopes of the inductor current. In steady-state operation, these conditions are easily met. But they can be violated during startup or during transient due to abrupt changes. The loss of sliding mode operation could lead to performance degradation manifested by either large overshoots or slow response.

Note that, if the system starts up from zero initial conditions, (4.12) becomes $0 \leq V_g \leq v_C$ and without the presence of the auxiliary diode D_a, sliding condition will not be fulfilled at startup. With the presence of the auxiliary diode D_a, the condition $v_C = V_g$ is guaranteed from the beginning, the system starts in sliding-mode and immediately its trajectory is constrained in the discrete sliding-mode domain defined by the constraint $i_{\text{ref}}[n] - i_L[n] = 0$. The worse cases take place when the duty cycle is saturated. For $d_e[n] = 0$, $\Delta\gamma[n] = \frac{T}{L}(v_C[n] - V_g) \geq 0$ (if $v_C[n] \geq V_g$]) and $\gamma[n+1] \leq 0$. For $d_e[n] = 1$, $\Delta\gamma[n] = -\frac{T}{L}V_g \leq 0$ and $\gamma[n+1] \geq 0$, which ensures the convergence to the switching surface. It will be shown later that at startup, the current reference could be saturated, the voltage loop becomes open and the resulting system is unstable making the voltage v_C to increase above V_g hence guaranteeing the sliding-mode condition. When the output voltage reaches the vicinity of its desired value, saturation disappears and the

PI regulator starts regulating the output voltage to its desired value according to the imposed performances by the outer loop controller.

4.3.4 Control-oriented Full-order Discrete-time Small-signal Model

By substituting the expression of the equivalent control (4.5) in (4.3b) and imposing the discrete-time sliding-mode constraint $i_L[n] = i_{\text{ref}}[n]$ imposed by (4.4), one obtains the following equation describing the output capacitor voltage v_C in the discrete-time domain

$$v_C[n+1] = f_v(v_C[n], i_{\text{ref}}[n], i_{\text{ref}}[n+1]) \tag{4.13}$$

where the function f_v is given by the following expression

$$f_v(v_C[n], i_{\text{ref}}[n], i_{\text{ref}}[n+1]) = v_C[n] - \frac{i_{\text{ref}}[n]}{Cv_C[n]}\left(L(i_{\text{ref}}[n+1] - i_{\text{ref}}[n]) - TV_g\right) - \frac{TP}{Cv_C[n]} \tag{4.14}$$

The equilibrium point of the discrete-time dynamical system described by (4.13)-(4.14) can be obtained by imposing $v_C[n+1] = v_C[n]$ and $i_{\text{ref}}[n+1] = i_{\text{ref}}[n]$ in the same equations. Imposing these constraints implies that $v_C[n]$ takes an infinite value unless the current reference $i_{\text{ref}}[n]$ is chosen to be exactly equal to P/V_g. Indeed, this is the only inductor current value that corresponds to a balance between the input power delivered by the voltage source and the output power imposed by the CPL. Therefore, during startup and while the system is under inrush current limiting phase, this is feeding a CPL with a constant current different from the one that balances input and output powers in the system, and this explains the output voltage divergence. It is worth noting that for inrush current limitation during startup, the converter will unavoidably work under this condition. The output voltage will collapse if the current reference is smaller than P/V_g. This fact appears in a clear contrast with the case of resistive load for which the voltage reaches a finite value in steady-state when the system is under pure CMC [58].

The case studied here is similar to the analog control based on the average inductor current regulation in a buck converter loaded by a CPL, which is still unstable after the introduction of the current control loop [31]. In both cases, the introduction of an outer voltage loop will contribute to the global stabilization of the system apart

from ensuring output voltage regulation. It should also be noted that when an outer loop is added to stabilize the output voltage while establishing the current reference, this current will be imposed to be $I_{\text{ref}} = P/V_g$ in steady-state regardless the desired reference value V_{ref} of the output voltage v_C.

Let V_C^* and I_{ref} be the nominal steady-state values of $v_C[n]$ and $i_{\text{ref}}[n]$ respectively. Let $\hat{v}[n] = v_C[n] - V_C^*$, $\hat{i}_{\text{ref}}[n] = i_{\text{ref}}[n] - I_{\text{ref}}$ the small deviations of the output voltage $v_C[n]$ and the current reference $i_{\text{ref}}[n]$ with respect to their steady-state values V_{ref} and I_{ref} respectively. Therefore, the small-signal model of the system under current mode control can be written as follows:

$$\hat{v}_C[n+1] = \frac{\partial f_v}{\partial v_C[n]}\hat{v}_C[n] + \frac{\partial f_v}{\partial i_{\text{ref}}[n]}\hat{i}_{\text{ref}}[n] + \frac{\partial f_v}{\partial i_{\text{ref}}[n+1]}\hat{i}_{\text{ref}}[n+1] \tag{4.15}$$

The different partial derivatives appearing in (4.15) are

$$\begin{aligned} \frac{\partial f_v}{\partial v_C[n]} &= 1 + \frac{T}{CV_C^{*2}}(P - I_{\text{ref}}V_g) \\ \frac{\partial f_v}{\partial i_{\text{ref}}[n]} &= \frac{TV_g + LI_{\text{ref}}}{CV_C^*} \\ \frac{\partial f_v}{\partial i_{\text{ref}}[n+1]} &= \frac{-I_{\text{ref}}L}{CV_C^*} \end{aligned} \tag{4.16}$$

With abuse of notation, let $\hat{V}_C(z)$ and $\hat{I}_{\text{ref}}$ be the z-transforms of $v_C[n]$ and i_{ref} respectively.

Taking the $z-$ transform of (4.15), the i_{ref}-to-v_C small-signal transfer function of the digital sliding current mode controlled boost converter with voltage loop open and supplying a constant power can be expressed as follows

$$H_i(z) = \frac{\hat{V}_C(z)}{\hat{I}_{\text{ref}}(z)} = -R_i\frac{z - z_c}{z - z_p} \tag{4.17}$$

where R_i, z_c and z_p are given by

$$R_i = \frac{LI_{\text{ref}}}{CV_C^*}, \quad z_c = 1 + \frac{TV_g}{I_{\text{ref}}L}, \quad z_p = 1 + \frac{T}{CV_C^{*2}}(I_{\text{ref}}V_{\text{g}} - P) \tag{4.18}$$

The previous transfer function represent the discrete-time small-signal model of the boost converter under an inner current control loop based on a DSMC strategy and

can be used to design an outer digital voltage control loop in the $z-$domain. Note that the zero z_c is outside the unit circle, which explains the well-known non-minimum phase characteristics of the control to output voltage transfer function in boost converters. Note also that during startup, the current reference i_{ref} will be limited by an upper bound I_{lim} which must be selected larger than the desired steady-state P/V_g, hence, the pole z_p of the previous transfer function is outside the unit circle, which corresponds to an unstable system. Therefore, any designed controller must stabilize the system while regulating the output voltage and exhibiting desired performances in terms of disturbance rejection and transient response.

4.4 Discrete-time Output Voltage Loop Control Design

In order to ensure an output voltage regulation, an outer and slower control loop in cascade with the inner DSMC current loop must be added. This loop is designed in the $z-$domain based on the the i_{ref}-to-v_C transfer function $H_i(z)$ in (4.17) representing the small-signal model around a desired operating point. This second control loop will regulate the output voltage to a desired value V_{ref}. The steady-state current reference I_{ref} will be equal to P/V_g regardless the value of V_{ref} as mentioned before. In order to stabilize the system, a two-loop control strategy will be used, hence the outer voltage loop provides the reference for the inner current loop. Let $\varepsilon[n] = V_{\text{ref}} - v_C[n]$ be the output voltage error. The current reference is updated from the output of a digital PI compensator as follows

$$i_r[n] = K_p\varepsilon[n] + q[n] \tag{4.19}$$

where $q[n] = K_i \sum_{k=0}^{n} \varepsilon[k]$ is the discrete-time accumulative sum of the error voltage weighted by the integral gain K_i, K_p being the proportional gain. In order to avoid high inrush current in start-up, the current reference must be limited and the final expression for the current reference becomes

$$i_{\text{ref}}[n] = \begin{cases} i_{\text{r}}[n] & \text{if} \quad i_r[n] < I_{\text{lim}} \\ I_{\text{lim}} & \text{if} \quad i_r[n] \geq I_{\text{lim}} \end{cases} \tag{4.20}$$

Different approaches can be often used for integral control emulation. For sufficiently small switching/sampling period, all the approaches yield a controller which

produces a closed-loop behavior similar to the one provided by a continuous-time controller. For the sake of simplicity, let us choose the Euler forward approach for emulating the integrator. This approximation yields the following recurrence equation for the discrete-time integral variable:

$$z[n+1] \;=\; z[n] + K_i \varepsilon[n] \tag{4.21}$$

To avoid windup phenomenon, the integral variable $z[n]$ is also limited to an upper bound Z_{lim} and the expression of the variable $q[n]$ becomes as follows

$$q[n] = \begin{cases} z[n] & \text{if } z[n] < Z_{\text{lim}} \\ Z_{\text{lim}} & \text{if } z[n] \geq Z_{\text{lim}} \end{cases} \tag{4.22}$$

The presence of an advanced sample of the current reference $i_{\text{ref}}[n+1]$ in the expression of the control law (4.5) makes it challenging to obtain this law when the reference is to be provided by a feedback loop. A possible solution is to use a predictive approach to get the value of the reference current from (4.19) one switching period ahead of time using (4.3b). While this would work theoretically and in simulation, it would require increased computational resources in an experimental digital platform like a Digital Signal Processor (DSP). A much more simple solution is to redefine the discrete-time sliding-mode surface as follows:

$$\gamma[n] = i_{\text{ref}}[n-1] - i_L[n] \tag{4.23}$$

and the resulting expression of the duty cycle becomes

$$d_e[n] = \text{sat}\left(\frac{L(i_{\text{ref}}[n] - i_L[n])}{T v_C[n]} + \frac{v_C[n] - V_g}{v_C[n]} \right) \tag{4.24}$$

The first term in the expression of $d_e[n]$ in (4.24) is only non null in the reaching phase. Once the sliding-mode regime is reached, this term becomes zero and only the second term forces the system to evolve toward the equilibrium point if the stability of the closed-loop system is ensured. Fig. 4.4 shows a block diagram of the large-signal model of the system with a two-loop control based on DSMC. The presence

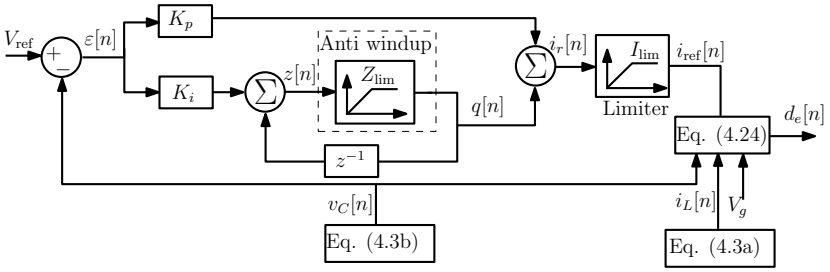


Figure 4.4: Block diagram of the large-signal model of the system with a double control loop based on the proposed DSMC.

of a discrete-time integrator in the external voltage loop will impose that in steady-state $V_C^* := v_C[\infty] = V_{\text{ref}}$. Furthermore, in steady-state one will have $Q^* := I_L^*$ and $I_L^* := P/V_g$. Therefore, the coordinates of the equilibrium point are

$$I_L^* = \frac{P}{V_g}, \tag{4.25a}$$

$$V_C^* = V_{\text{ref}}, \tag{4.25b}$$

$$Q^* = I_L^* = \frac{P}{V_g} \tag{4.25c}$$

where I_L^*, V_C^* and Q^* stand for the steady-state values of the the state variables i_L, v_C and q respectively.

4.5 Design of the Output Voltage Feedback Loop Using the Root-locus Technique

The block diagram corresponding to (4.15) is depicted in Fig. 4.5. The small-signal model can be used to design the feedback compensator to obtain a stable closed-loop system with a regulated output voltage.

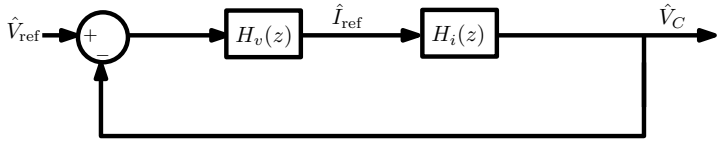


Figure 4.5: Block diagram of the $z-$domain small-signal model.

Chapter 4. Two-loop PWM-digital SMC of Boost Converter with CPL

The focus in this section is on the design of the output voltage regulator. The time response characteristics are related to closed-loop pole locations. Hence, a design based on root locus approach will be used. The aim is to design a controller such that the dominant closed-loop poles have a desired damping ratio and a settling time. According to (4.19) and (4.21), the transfer function for the outer digital PI voltage controller can be expressed as follows

$$H_v(z) = K_p + \frac{K_i T}{z-1} \equiv K_p \frac{z - z_{\text{pi}}}{z-1} \tag{4.26}$$

where $z_{\text{pi}} = 1 - {}^{K_i T}/_{K_p}$ is the zero introduced by the digital PI compensator.

The loop gain of the system $\mathcal{L}_d(z) = H_i(z)H_v(z)$, from (4.17) and (4.26), results in

$$\mathcal{L}_d(z) = -K_p R_i \frac{(z - z_{\text{pi}})(z - z_c)}{z(z-1)(z - z_p)} \tag{4.27}$$

Note that because of the one cycle delay present in the current reference in (4.23), a pole at the origin is added to the loop gain.

Although (4.27) can be used to obtain numerically the suitable parameter values for the desired pole position, it is always more useful to have an explicit mathematical expression. For many applications, the feedback gain K_p is a design parameter that should be adjusted according to the values of other parameters in order to get a system response with the desired performances. The purpose in this section is to perform an analytical study by carrying out a realistic approximation.

In order to simplify the design, the integral gain K_i can be appropriately selected so that the zero of the PI controller is placed slightly smaller than 1. Therefore, K_i becomes as follows

$$K_i = \frac{K_p(1 - z_{\text{pi}})}{T} \tag{4.28}$$

This means that the term ${}^{K_i}/_{K_p}$ must be selected much smaller than 1 and the loop gain can be approximated by

$$\mathcal{L}_d(z) \approx -K_p R_i \frac{z - z_c}{z(z - z_p)}, \tag{4.29}$$

The approximate closed-loop characteristic polynomial equation can be expressed as follows

$$1 + \mathcal{L}_d(z) = 0 \equiv z^2 - (K_p R_i + z_p)z + K_p R_i z_c = 0 \tag{4.30}$$

The closed-loop poles can be selected at the break-away point z_{ba} on the real axis to correspond to a damping factor $\zeta = 1$ and a settling time $t_s = -4T/ln|z_{ba}|$. For finding the break-away points, one has to find the value of $z = z_{\text{ba}}$ that maximizes or minimizes the gain K_p [65] hence obtaining the following approximate expression for the values of the break-away points and the corresponding proportional gain of the PI controller

$$z_{\text{ba}} \approx z_c \pm \sqrt{z_c^2 - z_p z_c}, \tag{4.31a}$$

$$K_{p,\text{ba}} \approx \frac{(z_{\text{ba}} - z_p) z_{\text{ba}}}{R_i (z_{\text{ba}} - z_c)} \tag{4.31b}$$

The value of z_{ba} with positive sign is omitted because it corresponds to a break-in point outside the unit circle leading to an unstable system.

4.6 Numerical Simulations and Experimental Results

In order to validate the previous analysis, numerical simulations in the PSIM© software and experimental tests have been carried out.

4.6.1 System Startup and Steady-state Operation

The initial value of the duty cycle can be obtained from the initial values of the state variables. Usually, the obtained value at startup is saturated. With delay, the number of initial saturated cycles increases since the inductor is continuously charged during a few number of cycles leading to an increase of the the inrush current.

Let us consider the nominal values of the power stage parameters depicted in Table 3.1, the desired output voltage $V_{\text{ref}} = 380$ V and the switching/sampling frequency f_s =100 kHz. The steady-state of the current reference is $I_{\text{ref}} = P/V_g = 5$ A. During the startup, the current reference i_{ref} and the integral variable q were limited to $I_{\text{lim}} = 10$ A and $Z_{\text{lim}} = 10$ A respectively. The PI zero is selected at $z_c = 0.95$. First, the root locus of the closed-loop system is obtained and the result is depicted in Fig. 4.6. Let us select the closed-loop poles at the break-away point $z_{\text{ba}} \approx 0.62 + 0j$, which corresponds to a proportional gain $K_p \approx 0.82$ and a damping coefficient $\zeta = 1$.

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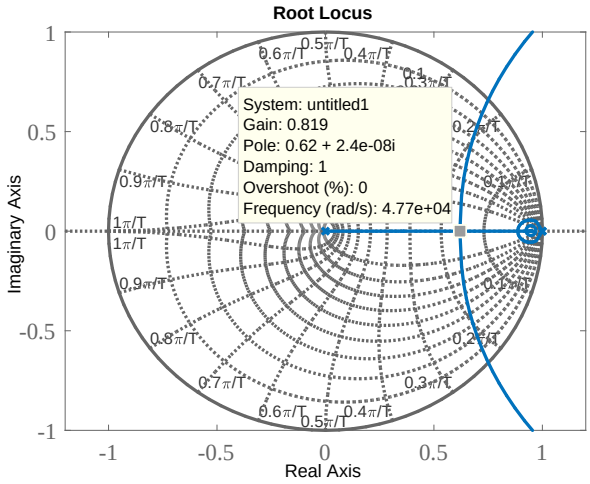


Figure 4.6: Root locus of the system. At the double pole position $z_{\text{ba}} \approx 0.62+0j$, marked by a square on the real axis, the gain $K_{p,\text{ba}} = 0.82$ according to (4.31a) and (4.31b) leading theoretically to damping coefficient $\zeta = 1$ and null overshoot.

The performances of the DSMC will be validated by means of numerical simulations, from both the derived large-signal discrete-time model and from a detailed switched model implemented in PSIM© software, and experimental results.

4.6.2 Experimental Setup

Fig. 4.7 shows the schematic circuit diagram of the implemented experimental prototype. The power stage is the same described in Section 3.4 with different ratios in the sensors. The developed DSMC algorithm was programmed in the DSP TMS320F28335 of TEXAS INSTRUMENTS. The samples of the state variables are captured and adapted to the voltage values supported by the DSP, connecting to a pin of the ADC module through an operational amplifier operating as a buffer to isolate the DSP. The signals are sampled at the switching frequency rate. The duty cycle was calculated according to (4.24) and processed in the PWM of the DSP which uses a symmetric triangular signal to generate the driving signal with a time delay of about $\tau_d = 5.5$ μs. The CPL has been emulated by the electronic load 9000 EL-DE ELEKTRO-AUTOMATIK which has been programmed in constant power mode. The experimental waveforms

shown below, have been measured by using the oscilloscope Tektronix TDS 754C and the probes TEKTRONIX TCP202 for illustrating the current waveforms.

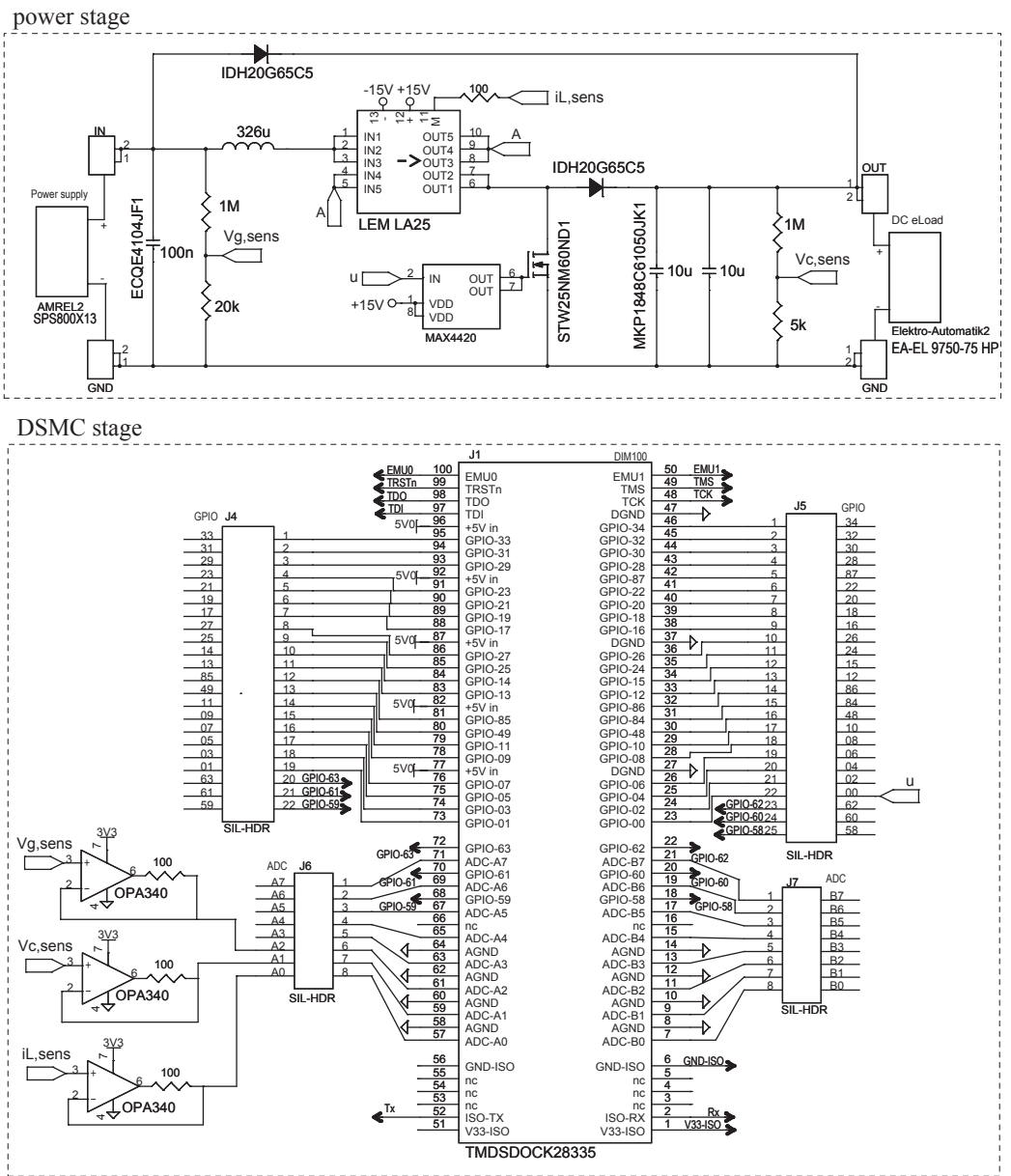


Figure 4.7: Schematic diagram of the implemented experimental prototype.

4.6.3 Results

Fig 4.8 shows the numerical simulation of the start-up and the steady-state responses of the system from both models. It can be observed that during start-up the inductor current reference $i_{\text{ref}} = I_{\text{lim}}$ remains constant due to the saturation, hence limiting the inrush current. As soon as the capacitor voltage reaches the vicinity of the voltage reference V_{ref}, the PI controller comes to play and the current reference is no longer constant but time-varying state-dependent and provided by the PI compensator according to (4.19). The data from the discrete-time model are plotted together with the simulated data from the detailed switched model implemented in PSIM© software. It can be observed that the responses from the two models are very close. The voltage waveforms from the switched model and the discrete-time model cannot be distinguished from each other. Hence, the simulations show that the large-signal model derived in this work can predict accurately the large-signal behavior of the system.

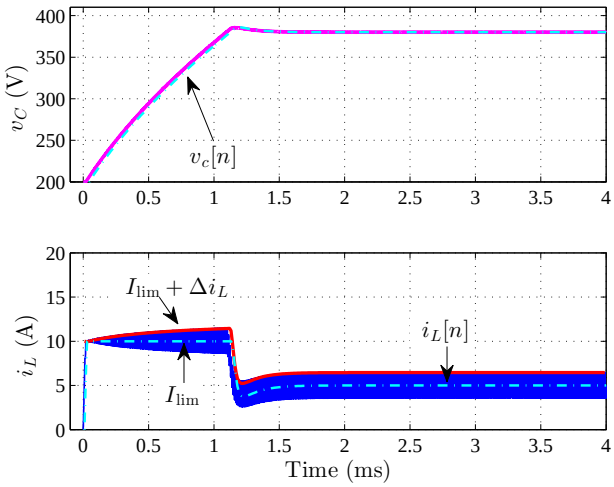


Figure 4.8: Start-up and steady-state response from numerical simulations and from the discrete-time model.

Remark 1: *Since during startup the average inductor current value is the regulated variable and it is supposed to reach the reference current in one cycle, the ripple of this*

variable can only exceed the limit I_{lim} *by the switching ripple* Δi_L *given by*

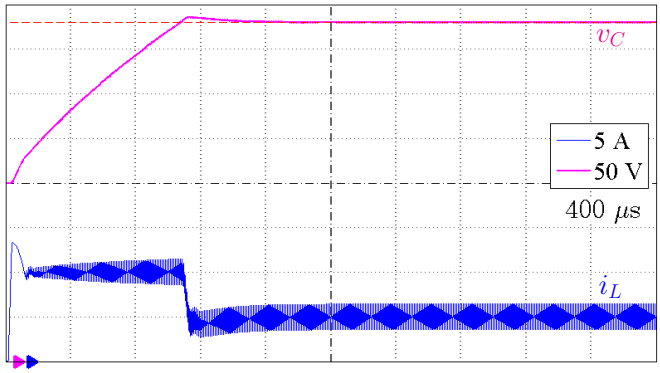
$$\Delta i_L = \frac{TV_g(v_C - V_g)}{2v_C L} \tag{4.32}$$

At the initial time, $v_C = V_g$ *due to the presence of the auxiliary diode* D_a*,* Δi_L *should be zero as can be confirmed in Fig 4.8. However, in a practical implementation of a digital controller, saturation of the duty cycle during the initial cycles and propagation delays always exist and it is expected that the inductor current will still overpass the imposed current limit plus the theoretical ripple given by* Δi_L *in (4.32). The current ripple amplitude* Δi_L *from (4.32), superposed to the averaged current* I_L^* *is plotted in the bottom panel of Fig 4.8 together with the current waveforms obtained from the switched model. The agreement is remarkable both in the startup, in steady-state and in the transient phase.*

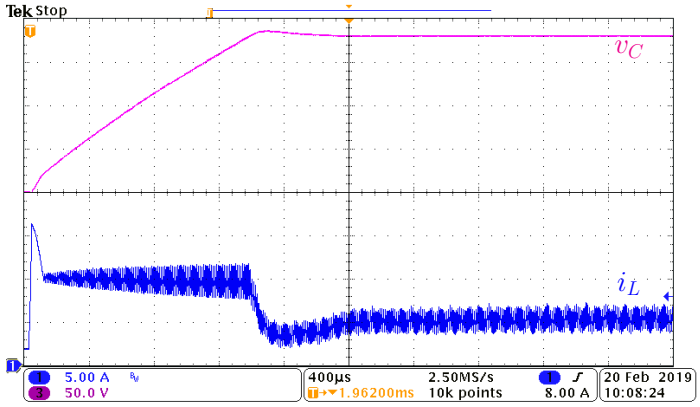
It is worth to note that one cycle delay inherently existing in the used commercial device has been eliminated by appropriately modifying the C code programming of the device. However, computation delay is unavoidable [66]. By adding a computation delay $\tau_d = 5.5$ μs, the results depicted in Fig 4.9 are obtained where it can be observed that a small inrush current still exists in the current startup response. The value of the computation delay used is the one corresponding to the experimental prototype. The propagation delay makes higher the number of cycles during which the duty cycle is saturated making the sliding mode condition not satisfied during these cycles, which, in turn, leads to higher inrush current at startup. Note that in case of experimental results the inrush current is larger than in the numerical simulation. This is mainly due to the saturation of the inductor and the decrease of its inductance value at high current levels.

As a remedy for this problem, one can force the initial values of the duty cycle to lie within the interval (0,1) in a few number of cycles either by scaling down the value of the duty cycle obtained from the control law (4.24) or by limiting the rate of change of the reference current from zero to I_{lim} in startup.

By filtering out the high frequency component of the current reference at the abrupt change in startup, the inrush current can be suppressed. However, the presence of a filter also slows down the system response. Another way to limit the inrush current in



(a) Numerical simulation results with τ_d=5.5μs.



(b) Experimental Results.

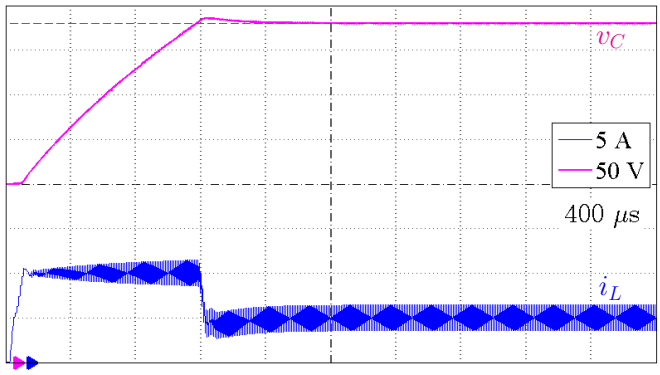
Figure 4.9: Start-up and steady-state of the system.

the presence of computation delays without degrading the system response is limiting the rate of change of the current reference during startup.

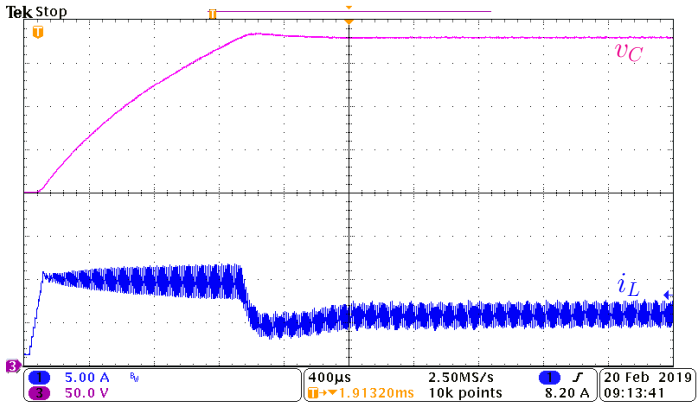
Remark 2: *The system is unstable when the saturation is taking place and the system is under CMC with open voltage loop. During this phase, the output voltage tends to infinity although the average of the inductor current is theoretically well regulated to the maximum allowed current* I_{lim}*. In the case of the boost converter, this type of instability only makes the output voltage to increase from the initial voltage* V_g*. This increase in the output voltage is desired since under this operation the system is*

approaching its desired operating point.

In order to completely suppress the still remaining inrush current due to computation delays, the solution based on limiting the rate of change of the current reference during the start-up is adopted. A slope limiter is introduced in the current reference at the startup in order to guarantee the sliding-mode conditions given in (4.12). The effect of adding this slope limiter is shown in Fig. 4.10 where it can be observed that inrush current is completely suppressed thanks to the operation under sliding mode regime.



(a) Numerical simulation results.



(b) Experimental results.

Figure 4.10: Start-up and steady-state responses of the system from experimental measurements with slope limiter $\frac{\mathrm{d}i_{\mathrm{ref}}}{\mathrm{d}t}\big|_{\mathrm{lim}} = 100$ kA/s.

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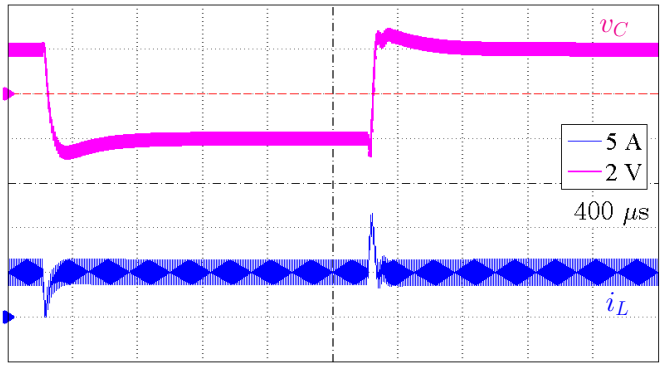
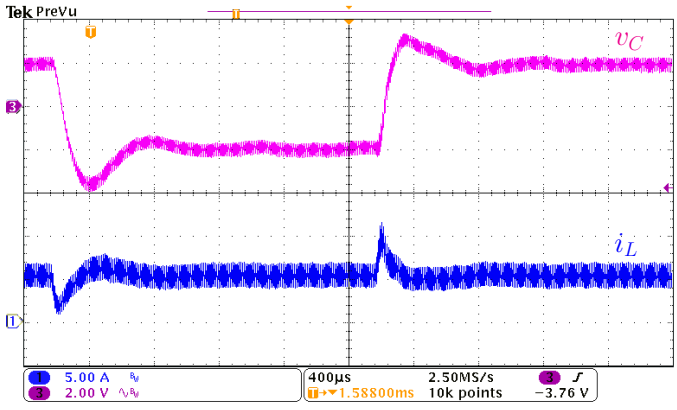
The rate of change of the current reference is $\left.\frac{\mathrm{d}i_{\mathrm{ref}}}{\mathrm{d}t}\right|_{\mathrm{lim}} = 100$ kA/s, which implies that the current reference limiter value will be reached in 10 switching periods. In all the cases, the output voltage regulation to 380 V in steady-state is also well achieved. The experimental results are very close to the simulated ones.

Fig. 4.11(a) and Fig. 4.11(b) shows the response of the system to a ±4 V step change in the reference voltage. It can be observed that the system exhibits a small undershoot in the output voltage response immediately after the positive step change of voltage reference. The inductor current follows the reference current tightly as dictated by the



(a) Numerical simulation results

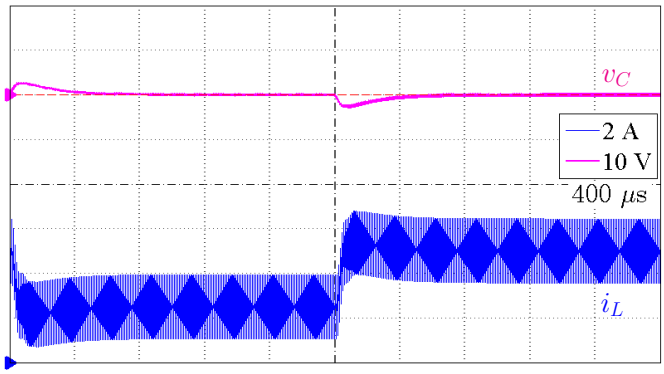


(b) Experimental Results

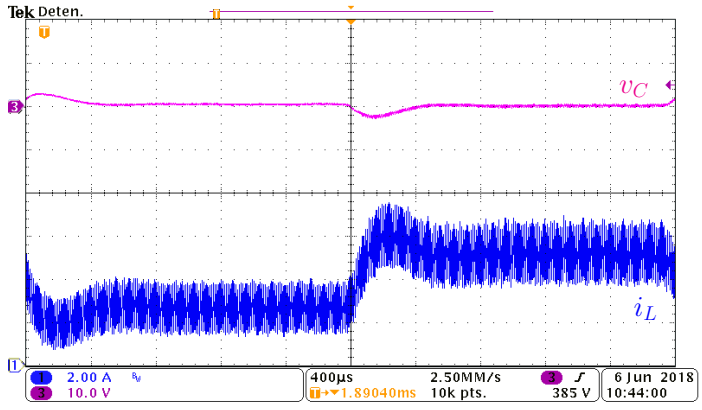
Figure 4.11: Small-signal transient response in front of a ±4 V step change between 378 V and 382 V in the reference voltage.

DSMC. Note that the measured inductor current i_L tracks tightly and accurately the current reference i_{ref} while the output voltage is regulated to its desired reference.

Fig. 4.12 shows the simulation and experimental results of the transient response in the presence of 50% step change in the load power. A zero steady-state error in the output voltage can also be observed while the dynamic current reference i_{ref} is tracked by the inductor current i_L as imposed by the inner DSMC loop. The steady-state value of i_{ref} is $I_{\text{ref}} = P/V_g$ as predicted by the theoretical analysis. As before, both



(a) Numerical simulation results.



(b) Experimental results.

Figure 4.12: Small-signal transient response in front of 50% step change in the nominal power.

inductor current and capacitor voltage show a fast recovery of the steady-state. As can be observed, in all the cases, both small-signal and large-signal responses show an agreement between theory, simulations and experiments, confirming the validity of the model developed in the previous sections. Hence the large-signal model can be used for repeated simulations while the small-signal model can be utilized for control design and performance specifications.

Remark 3: *Theoretically, according to the small-signal design procedure followed, the system should present no overshoot for a positive step change with the chosen values of parameters. However, a small overshoot can be still appreciated in the system response of Fig. 4.12. The discrepancy is mainly due to the computation delay ($\tau_d \approx 5.5$ μs) not taken into account in the analysis.*

Fig. 4.13 shows the transient response in the presence of 20% step change in the input voltage from the detailed switched model implemented in PSIM© software. It can be observed that the output voltage is tightly regulated to its desired value. The steady-state average inductor current is $I_{\text{ref}} = P/V_g$ as predicted by the theoretical analysis. The inductor current and capacitor voltage show a fast recovery of the steady-state after a disturbance takes place.

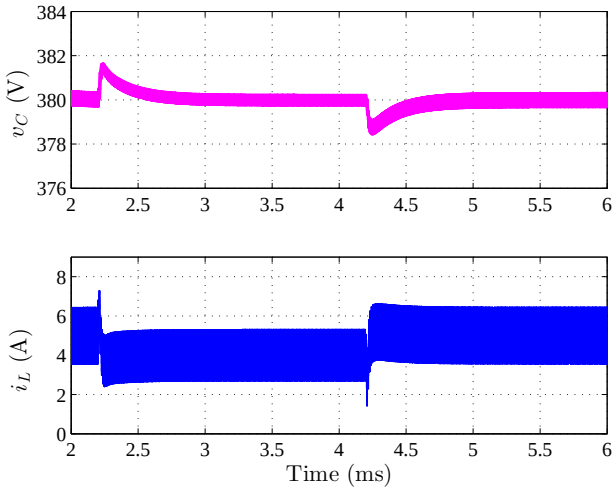


Figure 4.13: Small-signal transient response in front of a 20% step change in the input voltage from numerical simulations.

Chapter 5

PWM nonlinear analog control: virtual mesh approach and adaptive strategy with CPL power estimation

5.1 Introduction

Chapter 4 has shown that SMC and constant switching frequency operation are compatible when a DSMC is derived from a discrete-time model of the converter with CPL. This chapter presents two additional alternatives for constant switching frequency operation based on nonlinear control strategies for output voltage regulation of a boost converter with CPL. Both strategies use a PWM element, are based on a continuous-time analysis and are eventually implemented by means of analog circuitry.

Good global performance under large-signal operation has been attained with PWM nonlinear control based on feedback linearization. With the aim of regulating the output voltage in a buck converter, the equations transformation introduced by that approach has resulted in linear stable dynamics of the output voltage [28], and has been succesfully combined with feedforward of a load power estimated value [67]. Feedback linearization has also guaranteed that the inductor current remains below a maximum

value at any time irrespective of load and input voltage variations in elementary converters [68].

The first approach proposed here uses state-feedback linearization to transform the nonlinear average dynamics of the inductor current in the converter into a linear average dynamics of the inductor current in a virtual mesh, which consists in the series connection of a voltage source, a resistor and the converter inductor. In the virtual mesh, the resistor introduces damping to contribute to the system stability while the voltage source indirectly regulates the output voltage. Although the control has two feedback loops, no separated dynamics between inductor current and capacitor voltage are considered.

The second proposal introduces a mechanism to estimate the power of the CPL. The control law has two terms, the first one being the duty cycle in steady-state. The second term is a correcting element during transient-states, which is proportional to the current error, *i.e.*, the difference between the real average value of the inductor current and the value of the inductor current in steady-state, the latter being indirectly given by as estimation loop of the CPL power.

5.2 PWM Nonlinear Control for Virtual Mesh Emulation

Fig. 5.1 shows the block diagram of a boost converter loaded with a CPL under the proposed control. In CCM the average dynamic behavior of the converter can be expressed as follows:

$$\frac{d\overline{i_L}}{dt} = -\frac{(1-d)}{L}\overline{v_C} + \frac{V_g}{L} \tag{5.1a}$$

$$\frac{d\overline{v_C}}{dt} = \frac{(1-d)}{C}\overline{i_L} - \frac{P}{C\overline{v_C}} \tag{5.1b}$$

With the aim of linearizing the inductor current differential equation in (5.1a), the control law is expressed as follows

$$d = \frac{\overline{v_C} - (V_g + r\overline{i_L} - \overline{e})}{\overline{v_C}}, \tag{5.2}$$

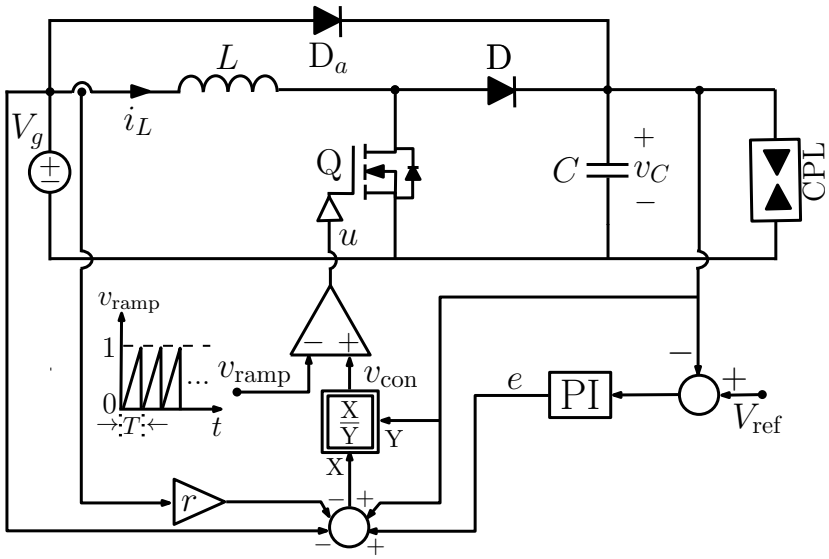


Figure 5.1: Schematic block diagram of the PWM nonlinear control of a boost converter with CPL

where r is the virtual resistance added to the system and $\overline{e}$ is the average value of a new variable e, which corresponds to the output of a voltage loop based on a PI compensator. The new state variable e is defined as follows

$$e = K_{p_e}(V_{\text{ref}} - \overline{v_C}) + K_{i_e}\int_{-\infty}^{t}(V_{\text{ref}} - \overline{v_C}(\lambda))d\lambda, \tag{5.3}$$

V_{ref} being the desired output voltage and K_{p_e} and $K_{i_e} > 0$, are the proportional and the integral gains respectively. As can be observed in Fig. 5.1, the duty cycle d is generated by comparing a control voltage v_{con} with a sawtooth ramp signal v_{ramp}.

5.2.1 Closed-loop Equations

Substitution of (5.2) and (5.3) in (5.1), leads to the closed-loop equations of the system given by

$$\frac{d\overline{i_L}}{dt} = -\frac{r\overline{i_L}}{L} + \frac{\overline{e}}{L} \tag{5.4a}$$

$$\frac{d\overline{v_C}}{dt} = \frac{(V_g + r\overline{i_L} - \overline{e})\overline{i_L}}{C\overline{v_C}} - \frac{P}{C\overline{v_C}} \tag{5.4b}$$

$$\frac{d\overline{e}}{dt} = -K_{p_e}\frac{d\overline{v_C}}{dt} + K_{i_e}(V_{\text{ref}} - \overline{v_C}) \tag{5.4c}$$

It can be observed that the nonlinear control law (5.2) has transformed the nonlinear dynamics of the average inductor current in (5.1a) into the linear dynamics in (5.4a) that can be interpreted by means of a virtual mesh of voltage source $\overline{e}$, resistor r and inductor L. In the virtual mesh the resistor introduces damping to contribute to the closed-loop stabilization while the voltage source indirectly regulates the output voltage since variable $\overline{e}$, is the output voltage of a PI compensator that processes the output voltage error.

Besides, from (5.4), the equilibrium point $(\overline{I_L}^*, \overline{V_C}^*, \overline{E}^*)$ of the system in closed loop becomes

$$\begin{aligned} \overline{I_L}^* &= \frac{\overline{E}^*}{r} = \frac{P}{V_g}, \\ \overline{V_C}^* &= V_{\text{ref}}, \\ \overline{E}^* &= \frac{rP}{V_g} = r\overline{I_L}^* \end{aligned} \tag{5.5}$$

Note, on the one hand, that the expression of $\overline{I_L}^*$ corroborates that both dc input and output powers are equal, and, on the other hand, $\overline{V_C}^*$ is the desired output voltage.

5.2.2 Stability Analysis

Linearizing the dynamics of the system in (5.4) around the equilibrium point (5.5) yields

$$\frac{d\hat{i}_L}{dt} = -\frac{r}{L}\hat{i}_L + \frac{1}{L}\hat{e} \tag{5.6a}$$

$$\frac{d\hat{v}_C}{dt} = a\hat{i}_L - b\hat{e} \tag{5.6b}$$

$$\frac{d\hat{e}}{dt} = -K_{p_e}a\hat{i}_L - K_{i_e}\hat{v}_C + K_{p_e}b\hat{e} \tag{5.6c}$$

where a and b are defined as follows

$$a = \frac{V_g^2 + rP}{CV_{\text{ref}}V_g}, \qquad b = \frac{P}{CV_{\text{ref}}V_g}$$

The small-signal model in (5.6) can be represented in matrix form as $\hat{\dot{y}} = A\hat{y}$, where

$$\hat{\dot{y}} = \begin{bmatrix} \frac{d\hat{i}_L}{dt} \\ \frac{d\hat{v}_C}{dt} \\ \frac{d\hat{e}}{dt} \end{bmatrix}, \qquad A = \begin{bmatrix} -\frac{r}{L} & 0 & \frac{1}{L} \\ a & 0 & -b \\ -K_{p_e}a & -K_{i_e} & K_{p_e}b \end{bmatrix}, \qquad \hat{y} = \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \\ \hat{e} \end{bmatrix} \tag{5.7}$$

The characteristic polynomial of the closed-loop system is $f(s) = |sI - A| = 0$. Hence, from (5.7), this equation is given by

$$|sI - A| = \begin{vmatrix} s + \frac{r}{L} & 0 & -\frac{1}{L} \\ -a & s & b \\ K_{p_e}a & K_{i_e} & s - K_{p_e}b \end{vmatrix} = 0 \tag{5.8}$$

Consequently, developing (5.8) leads to the characteristic equation of the closed-loop system given by $f_s(s) = s^3 + a_2s^2 + a_1s + a_0 = 0$, being a_2, a_1 and a_0 defined as follows

$$a_2 = \frac{r}{L} - \frac{K_{p_e}P}{CV_{\text{ref}}V_g}, \qquad a_1 = \frac{V_g^2K_{p_e} - LK_{i_e}P}{LCV_gV_{\text{ref}}}, \qquad a_0 = \frac{V_gK_{i_e}}{LCV_{\text{ref}}} \tag{5.9}$$

Consequently, $f_s(s)$ becomes as follows

$$f_s(s) = s^3 + \left(\frac{r}{L} - \frac{K_{p_e}P}{CV_{\text{ref}}V_g}\right)s^2 + \frac{V_g^2K_{p_e} - LK_{i_e}P}{LCV_gV_{\text{ref}}}s + \frac{V_gK_{i_e}}{LCV_{\text{ref}}} \tag{5.10}$$

Design Constraints for Stability

- A necessary condition but not sufficient for stability of the system is that the coefficients of polynomial $f_s(s)$ be positive. Hence, from (5.10) the following restriction must be satisfied

$$K_{p_e} < \frac{CrV_{\text{ref}}V_g}{LP} \tag{5.11}$$

$$K_{i_e} < \frac{K_{p_e}V_g^2}{LP} \tag{5.12}$$

- In order to guarantee the stability of the system, its poles must be in LHP. The Routh's table of characteristic equation $f_s(s)$ in (5.10), becomes

$$\begin{array}{lll} s^3 & 1 & a_1 \\ s^2 & a_2 & a_0 \\ s^1 & b_1 & \\ s^0 & a_0 & \end{array} \tag{5.13}$$

  As can be noticed from (5.13), the system stability will be guaranteed if the following conditions hold

  1) $a_2 > 0$, which corresponds to the same constraint given in (5.11).

  2) $b_1 > 0$, where $b_1 = a_2 a_1 - a_0$ is defined as follows

$$-\frac{P}{CV_{\text{ref}}}K_{p_e}^2 + \frac{V_g r}{L}K_{p_e} - (V_g + \frac{rP}{V_g} - \frac{L}{C}\frac{P^2}{V_{\text{ref}}V_g^2}K_{p_e})K_{i_e} > 0 \tag{5.14}$$

  Hence solving (5.14) for K_{i_e} yields to the following additional condition for stability

$$K_{i_e} < f(K_{p_e}), \tag{5.15}$$

  where, the function $f(K_{p_e})$ is defined as follows

$$f(K_{p_e}) \triangleq \frac{V_g K_{p_e}\left(\frac{r}{L} - \frac{P}{CV_{\text{ref}}V_g}K_{p_e}\right)}{V_g + \frac{rP}{V_g} - \frac{L}{C}\frac{P^2}{V_{\text{ref}}V_g^2}K_{p_e}} \tag{5.16}$$

  Consequently, the system stability will be guaranteed for the values of K_{p_e} and K_{i_e}, satisfying the constraints given by (5.11), (5.12) and (5.15).

5.2.3 Parametric Region of Stability

Remark. *The straight line defined by $K_{i_e} = {}^{K_{p_e}V_g^2}/_{LP}$ in the plane (K_{p_e}, K_{i_e}) is always above than the curve of the function $K_{i_e} = f(K_{p_e})$ for all $K_{p_e} > 0$.*

Proof.

$$\frac{K_{i_e}}{f(K_{p_e})} = \frac{CV_{\text{ref}}V_gPr + CV_{\text{ref}}V_g^3 - LP^2K_{p_e}}{CV_{\text{ref}}V_gPr - LP^2K_{p_e}} \triangleq \frac{N_1(K_{p_e})}{D_1(K_{p_e})}$$

where $N_1(K_{p_e})$ and $D_1(K_{p_e})$ are straight lines, such that $N_1(K_{p_e}) > D_1(K_{p_e}) \; \forall \; K_{p_e} > 0$, as it can be observed in Fig. 5.2.

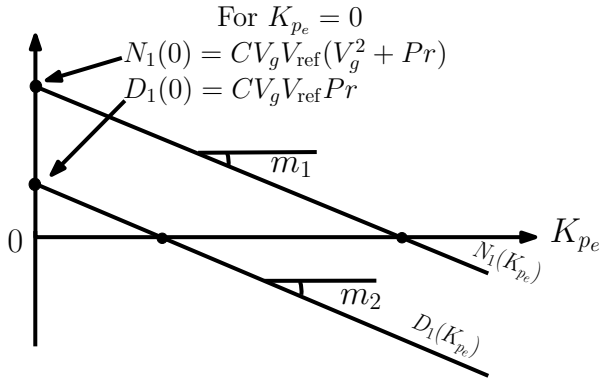


Figure 5.2: Slopes of $N_1(K_{p_e})$ and $D_1(K_{p_e})$

Moreover, the slopes of $N_1(K_{p_e})$ and $D_1(K_{p_e})$ as a function of K_{p_e} are equal

$$m_1 = m_2 = -LP^2$$

Therefore, $\frac{K_{i_e}}{f(K_{p_e})} > 1, \;\; \forall K_{p_e} > 0$ □

Hence, the manifold $K_{i_e} = f(K_{p_e})$ is the upper boundary of K_{i_e}. Besides, from (5.15) and (5.16), the gain K_{i_e} will be as is shown below:

$$\begin{array}{lcllcccl} K_{i_e} & > & 0 & \text{if} & 0 & < & K_{p_e} & < & z_1 \\ K_{i_e} & < & 0 & \text{if} & z_1 & < & K_{p_e} & < & z_2 \\ K_{i_e} & > & 0 & \text{if} & z_2 & < & K_{p_e} & > & \infty, \end{array} \tag{5.17}$$

where z_1 and z_2 are defined as follows

$$z_1 = \frac{CrV_{\text{ref}}V_g}{LP} \tag{5.18}$$

$$z_2 = \frac{(V_g^2 + rP)CV_{\text{ref}}V_g}{LP^2} \tag{5.19}$$

In addition, the manifold $f(K_{p_e})$ has one relative minimum (K_{p1}) and one relative maximum (K_{p2}), given by

$$K_{p1} = \frac{CV_{\text{ref}}V_g}{LP^2}\left(V_g^2 + rP + V_g\sqrt{V_g^2 + rP}\right) \tag{5.20}$$

$$K_{p2} = \frac{CV_{\text{ref}}V_g}{LP^2}\left(V_g^2 + rP - V_g\sqrt{V_g^2 + rP}\right) \tag{5.21}$$

Note that, $0 < K_{p2} < z_1$ and $K_{p1} > z_2$.

On the other hand, note that z_1 is the upper limit value of the constraint (5.11), hence from (5.17), system stability is guaranteed for values of the gain $K_{i_e} < f(K_{p_e})$ between $0 < K_{p_e} < z_1$. Fig. 5.3 illustrates in the plane K_{p_e}–K_{i_e} the parametric region of stability (PRS), which corresponds to the area coloured in grey color. Values of zero z_1, vertical asymptote $K_{i_e} = z_2$, position of relative maximum K_{p2} and position of relative minimum K_{p1} of function $f(K_{p_e})$ are also represented.

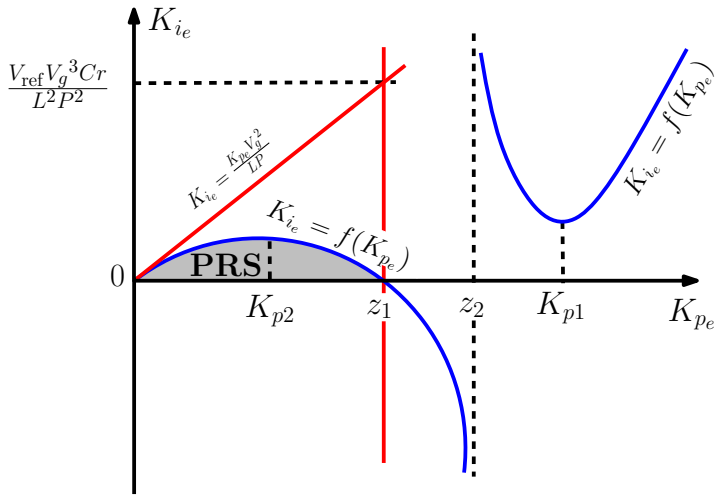
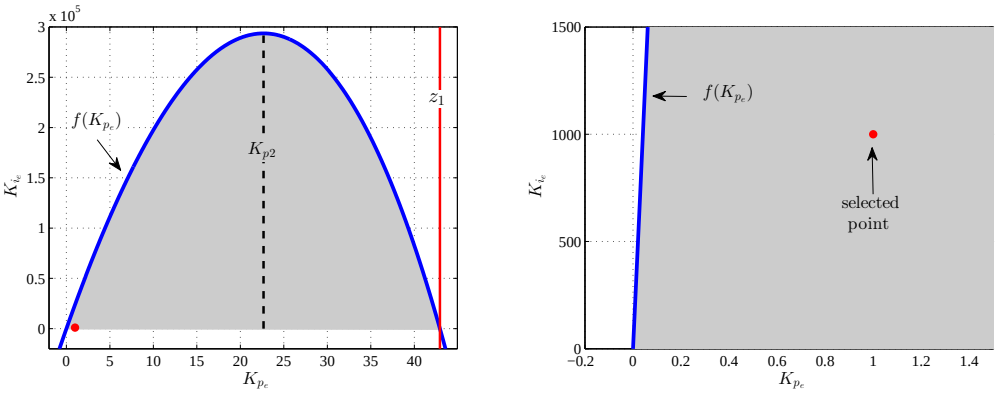


Figure 5.3: Parametric region for stability in the plane K_{p_e}–K_{i_e}

5.2.4 Numerical Simulations and Experimental Results

With the aim of validating the previous calculations, numerical simulations and experimental tests have been performed. PSIM© software was used to carry out the numerical simulations. The same parameters values for the boost converter shown in Table 3.1 have been used in the simulations and experimental verifications.



(a) PRS for the operating values of the system. (b) Zoom of the PRS for the selected point.

Figure 5.4: PRS in the plane K_{p_e}–K_{i_e} for the proposed system.

The control parameters K_{p_e} and K_{i_e} have been selected based on the PRS given in Fig. 5.4(a), which corresponds to a selected value of $r = 10\ \Omega$. Note that according to (5.11), K_{p_e} must be less than 42.94, which is equal to z_1. For that values of K_{p_e} less than z_1, the values of K_{i_e} are the ones under the plot of $f(K_{p_e})$, which has the relative maximum at $K_{p2} = 22.67$ and it is equal to $K_{i_e} = 293\ \text{ks}^{-1}$. In order to avoid high inrush current and a fast settling time without overshoot, the values of K_{p_e} and K_{i_e} have been selected as 1 and 1000 respectively, those values are inside of the PRS as it can be corroborated in Fig. 5.4(b). These values have been used for both the simulations and the experiments.

Experimental Setup

Fig 5.5 shows the schematic circuit diagram of the boost converter with CPL under the proposed nonlinear controller. The power stage is the same described in Section 3.4, but the inductor current i_L has been measured with a gain $1/10$ while input voltage and output voltage are sensed in each case with a gain $1/100$. The CPL has been emulated by the electronic load EL 9000 from ELEKTRO-AUTOMATIK operating in constant power mode. In the PWM nonlinear control stage it can be observed different blocks of the controller, namely, voltage error and PI compensator, control law and modulator. The operational amplifiers used in the control loop are of LF347 type. The analogue

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division is performed by IC AD633. The sawtooth signal v_{ramp} is provided by function generator Tektronik AFG2021 and establishes a switching frequency of $f_s = 100$ kHz and a peak value of 10 V. The comparator used for PWM operation is an LM319, by means of which the sawtooth signal is internally compared with ten times signal v_{con}. Also a Flip-Flop CD4027 is used to synchronize the signal v_{ramp} of function generator with the control signal.

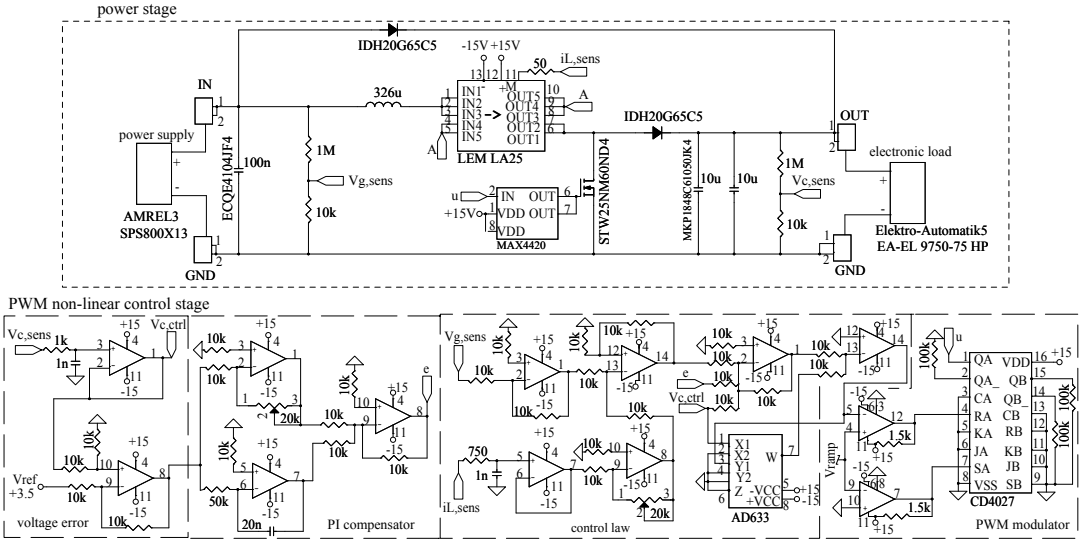

Figure 5.5: Circuit schematic of the prototype of the boost converter with the proposed nonlinear PWM control.

Results

Fig. 5.6 depicts the simulation results of the boost converter with CPL under the proposed control during the start-up and steady-state. Note, that the inrush current is not significant and the capacitor voltage exhibits an irrelevant overshoot before reaching the steady-state. Besides, after a transient time of 4 ms, the state variables reach their steady-state values which are in agreement with (5.5).

The response of the system in front of changes in the input voltage can be observed in Figs. 5.7(a) and 5.7(b) for simulation and experimental results respectively. Power source AMREL SPS800x13-K02D has been used to provide the input voltage changes from 200 V to 250 V with a slope of 6.25 V/ms and from 250 V to 200 V with a

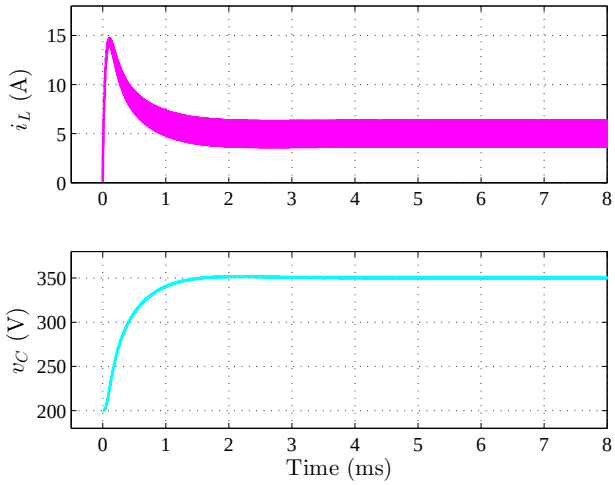

Figure 5.6: Simulated waveforms of the inductor current and the capacitor voltage of the boost converter with CPL under the proposed PWM nonlinear control.

slope of 13.88 V/ms. The inductor current, during the first transition, follows its new reference value of 4 A and remains at that value until the next change, after which it returns to 5 A. Moreover, the capacitor voltage offers a fast recovery and negligible overshoot and undershoot. It can be observed a perfect agreement between simulated and experimental results.

Similarly, Figs. 5.8(a) and 5.8(b) illustrate respectively the simulation and experimental responses of the system under output power abrupt changes from 1 kW to 0.5 kW and restored back to 1 kW. The inductor changes to 2.5 A when the load power is 0.5 kW as is predicted by (5.5). Moreover, the capacitor voltage remains at its desired value 350 V. In both cases, a zero steady-state error is obtained together with both small overshoot (5.42 %) and settling time (2 ms). Also, the resulting undershoot and corresponding settling time are almost the same. A perfect agreement is again observed between simulation and experiments.

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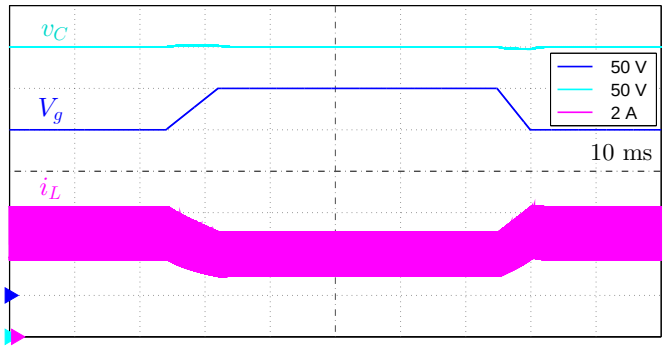
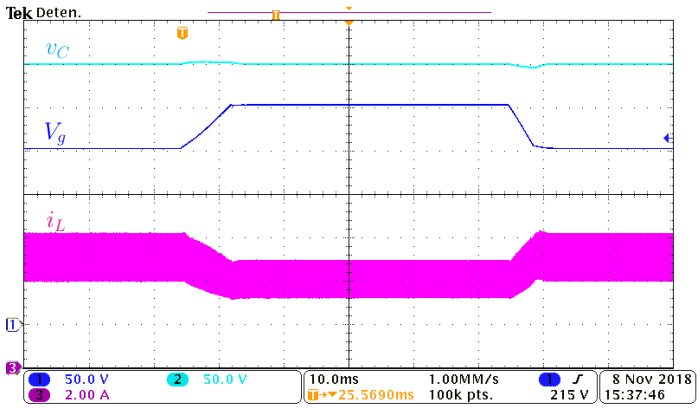
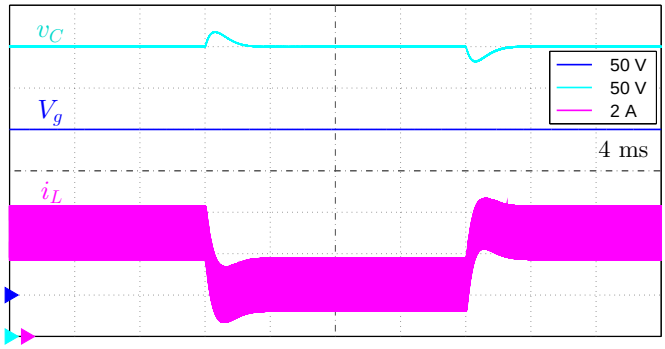


(a) Simulation results.

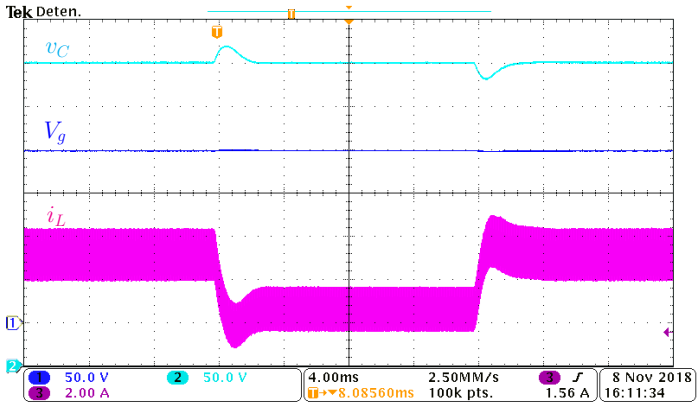


(b) Experimental results.

Figure 5.7: Measured transient response in front of input voltage changes from 200 V to 250 V and restored back.



(a) Simulation results.



(b) Experimental results.

Figure 5.8: Measured transient response in front of load changes from 1 kW to 0.5 kW and restored back.

On the other hand, Fig. 5.9 and Fig. 5.10 show the simulated and experimental results of the system in steady-state for two different values of input voltage, *i.e.*, $V_g = 200$ V and $V_g = 250$ V. From (5.5), the average inductor current is 5 A and 4 A in each case respectively. Therefore, an analog controller operating at constant switching frequency for a boost converter feeding a CPL has been developed.

It has to be pointed out that the control voltage v_{con} is a slight modification of (5.2) because (i) it uses the instantaneous values of the state variables instead of the average ones, and (ii) it is expressed in volts due to its implementation by means of the analogue divider. Hence, no low-pass filtering has been used. The resulting expression

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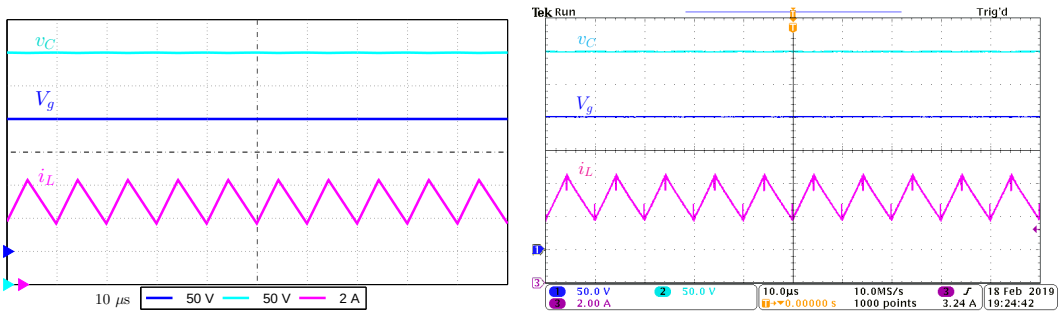
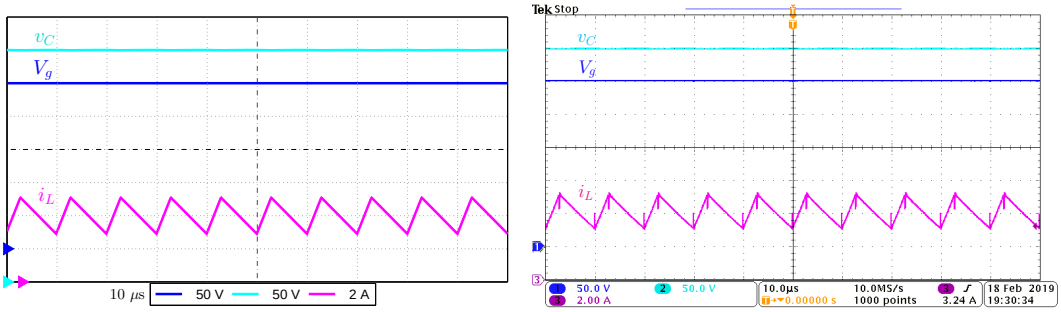


(a) Simulation results. (b) Experimental results.

Figure 5.9: Steady-state of the converter for $V_g = 200$ V and $f_s = 100$ kHz.



(a) Simulation results. (b) Experimental results.

Figure 5.10: Steady-state of the converter for $V_g = 250$ V and $f_s = 100$ kHz.

of v_{con} is

$$v_{\text{con}} = \frac{v_C - (V_g + r i_L - e)}{v_C} \tag{5.22}$$

Note that the ripple in v_{con} is mainly due to the inductor current i_L since the ripple of the other state variables is negligible. It is worth mentioning that a high quantity of current ripple could induce multiple commutations within a switching cycle. To avoid this, the parameter r must be selected smaller than a critical limit r_{lim}. By examining the slopes of ramp signal v_{ramp} and control signal v_{con}, the following approximate expression for r_{lim} has been obtained:

$$r_{\text{lim}} \approx \frac{L V_M \overline{V_C}^*}{T(\overline{V_C}^* - V_g)} \tag{5.23}$$

where V_M is the amplitude of the sawtooth ramp signal.

Fig. 5.11 shows both control and ramp signals scaled by a factor of 10 and the resulting switching signal u. Observe that in order to avoid noise effects on the switching decision in the experimental circuit, signal v_{con} has been scaled-up by the same factor, hence using a value of $V_M = 10$ V.

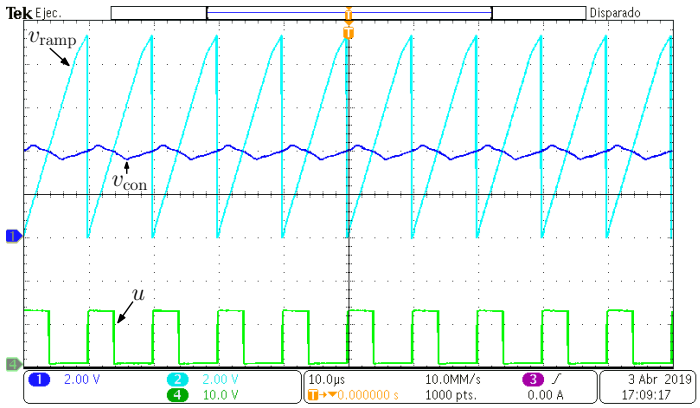


Figure 5.11: Control and sawtooth signals in steady-state.

5.3 PWM Adaptive Control for the Voltage Regulation of a Boost Converter Loaded with CPL

In this section, an adaptive loop to estimate the unknown load power P is proposed. The approach is based on a nonlinear PWM control to regulate the output voltage of a boost converter with an unknown CPL.

5.3.1 Control Design

Fig. 5.12 shows the circuit diagram of a boost converter feeding a CPL under the proposed adaptive control.

The equations that represents the average dynamic behavior of the system are given in (5.1).

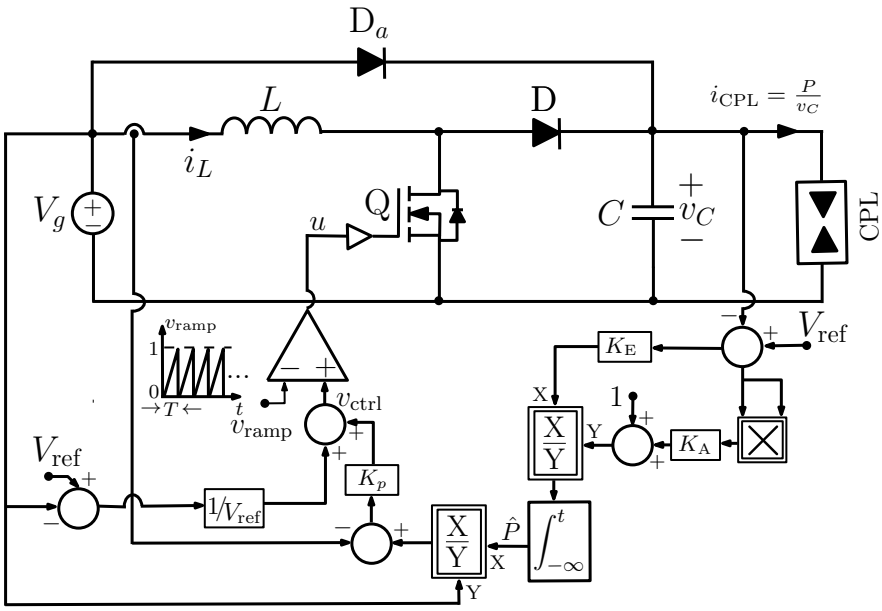


Figure 5.12: Block diagram of a boost converter feeding a CPL under the proposed nonlinear PWM control and power estimation.

The control law proposed here is the following

$$d = \frac{V_{\text{ref}} - V_g}{V_{\text{ref}}} + K_p \left(\frac{\hat{P}}{V_g} - \overline{i_L} \right), \tag{5.24}$$

where V_{ref} is the desired output voltage, $K_p > 0$ is a constant value. Besides, $\hat{P}$ is the load power estimated variable, which is defined as follows

$$\frac{d\hat{P}}{dt} = \frac{K_{\text{E}}(V_{\text{ref}} - \overline{v_C})}{1 + K_{\text{A}}(V_{\text{ref}} - \overline{v_C})^2} \tag{5.25}$$

Note that control law (5.24) has two terms. The first one is given by $V_{\text{ref}} - V_g / V_{\text{ref}}$, which constitutes the steady-state duty cycle required by the boost converter for given values of input and output voltages. The second term is a correcting element during transient states and is proportional to the current error *i.e* to the difference between the actual average value of the current and its steady-state value, provided that the estimated power is equal to the real value of the CPL power. Note that the time derivative of the estimated variable is an odd symmetry function of the output voltage error, which will be responsible of the adaptive behavior of the controller [69]. This adaptive mechanism has been successfully used in the case of a high-gain fourth order voltage step-up converter with resistive load [70].

It is worth to note in Fig. 5.12 that the duty cycle d is generated by comparing a control voltage v_{ctrl} with a sawtooth ramp signal v_{ramp}.

5.3.2 Closed-loop Equations

Substitution of (5.24) and (5.25) into (5.1) results in the following closed loop dynamic equations of the system,

$$\frac{d\overline{i_L}}{dt} = -\frac{1}{L}\left(\frac{V_g}{V_{\text{ref}}} - K_p\left(\frac{\hat{P}}{V_g} - \overline{i_L}\right)\right)\overline{v_C} + \frac{V_g}{L} \tag{5.26a}$$

$$\frac{d\overline{v_C}}{dt} = \frac{1}{C}\left(\frac{V_g}{V_{\text{ref}}} - K_p\left(\frac{\hat{P}}{V_g} - \overline{i_L}\right)\right)\overline{i_L} - \frac{P}{C\overline{v_C}} \tag{5.26b}$$

$$\frac{d\hat{P}}{dt} = \frac{K_{\text{E}}(V_{\text{ref}} - \overline{v_C})}{1 + K_{\text{A}}(V_{\text{ref}} - \overline{v_C})^2} \tag{5.26c}$$

Eq. (5.26) corresponds to a third order nonlinear system. The state of the system is expressed in terms of the inductor current error e_1, capacitor voltage error e_2 and

power estimation error e_3, which are given by

$$e_1 = \frac{P}{V_g} - \overline{i_L} \tag{5.27a}$$
$$e_2 = V_{\text{ref}} - \overline{v_C} \tag{5.27b}$$
$$e_3 = P - \hat{P} \tag{5.27c}$$

In terms of these errors, (5.26) can be rewritten as

$$\frac{de_1}{dt} = -\frac{1}{L}\left(\frac{V_g}{V_{\text{ref}}} + K_p(\frac{P}{V_g} - e_1) - \frac{K_p}{V_g}(P - e_3)\right)(V_{\text{ref}} - e_2) + \frac{V_g}{L} \tag{5.28a}$$
$$\frac{de_2}{dt} = \frac{1}{C}\left(\frac{V_g}{V_{\text{ref}}} + K_p(\frac{P}{V_g} - e_1) - \frac{K_p}{V_g}(P - e_3)\right)(\frac{P}{V_g} - e_1) - \frac{P}{C(V_{\text{ref}} - e_2)} \tag{5.28b}$$
$$\frac{de_3}{dt} = \frac{K_{\text{E}} e_2}{1 + K_{\text{A}} e_2^2} \tag{5.28c}$$

Furthermore the equilibrium point of the system $(\overline{I_L}^*, \overline{V_C}^*, \hat{P}^*)$ in closed loop is given by

$$E_1^* = 0 \quad \Rightarrow \quad \overline{I_L}^* = \frac{P}{V_g} \tag{5.29a}$$
$$E_2^* = 0 \quad \Rightarrow \quad \overline{V_C}^* = V_{\text{ref}} \tag{5.29b}$$
$$E_3^* = 0 \quad \Rightarrow \quad \hat{P}^* = P \tag{5.29c}$$

It can be observed that the value of the capacitor voltage in steady-state will be the desired output voltage. The inductor current in equilibrium depends on the power load and the input voltage. Besides, the estimated power $\hat{P}^*$ corresponds to the power P absorbed by the CPL.

5.3.3 Stability Analysis

Linearizing the dynamics of the system in (5.28) around the equilibrium point (5.29) yields

$$\frac{d\hat{e}_1}{dt} = \frac{K_p V_{\text{ref}}}{L}\hat{e}_1 + \frac{V_g}{L V_{\text{ref}}}\hat{e}_2 - \frac{K_p V_{\text{ref}}}{L V_g}\hat{e}_3 \tag{5.30a}$$
$$\frac{d\hat{e}_2}{dt} = -(\frac{V_g}{C V_{\text{ref}}} + \frac{K_p P}{C V_g})\hat{e}_1 - \frac{P}{C V_{\text{ref}}^2}\hat{e}_2 + \frac{K_p P}{C V_g^2}\hat{e}_3 \tag{5.30b}$$
$$\frac{d\hat{e}_3}{dt} = K_{\text{E}}\hat{e}_2 \tag{5.30c}$$

The system equations in (5.30) expressed in matrix form is $d\hat{y}_1/dt = A_1\hat{y}_1$, being $d\hat{y}_1/dt, A_1$ and $\hat{y}_1$ as follows

$$\frac{d\hat{y}_1}{dt} = \begin{bmatrix} \frac{d\hat{e}_1}{dt} \\ \frac{d\hat{e}_2}{dt} \\ \frac{d\hat{e}_3}{dt} \end{bmatrix}, \quad A_1 = \begin{bmatrix} \frac{K_pV_{\text{ref}}}{L} & \frac{V_g}{LV_{\text{ref}}} & -\frac{K_pV_{\text{ref}}}{LV_g} \\ -(\frac{V_g}{CV_{\text{ref}}} + \frac{K_pP}{CV_g}) & -\frac{P}{CV_{\text{ref}}^2} & \frac{K_pP}{CV_g^2} \\ 0 & K_{\text{E}} & 0 \end{bmatrix}, \quad \hat{y}_1 = \begin{bmatrix} \hat{e}_1 \\ \hat{e}_2 \\ \hat{e}_3 \end{bmatrix} \tag{5.31}$$

The characteristic polynomial is given by $g(s) = |sI - A_1| = 0$. Hence, solving this equation the following expression is obtained

$$|sI - A_1| = \begin{vmatrix} s - \frac{K_pV_{\text{ref}}}{L} & -\frac{V_g}{LV_{\text{ref}}} & \frac{K_pV_{\text{ref}}}{LV_g} \\ \frac{V_g}{CV_{\text{ref}}} + \frac{K_pP}{CV_g} & s + \frac{P}{CV_{\text{ref}}^2} & -\frac{K_pP}{CV_g^2} \\ 0 & -K_{\text{E}} & s \end{vmatrix} = 0 \tag{5.32}$$

After some algebra, the characteristic polynomial is expressed as $g(s) = s^3 + \alpha_2 s^2 + \alpha_1 s + \alpha_0$, where

$$\alpha_2 = \frac{K_pV_{\text{ref}}}{L} - \frac{P}{CV_{\text{ref}}^2}, \quad \alpha_1 = \frac{V_g^2}{V_{\text{ref}}^2}\frac{1}{LC} - \frac{K_{\text{E}}K_pP}{CV_g^2}, \quad \alpha_0 = \frac{K_{\text{E}}K_p}{LC} \tag{5.33}$$

Consequently, the characteristic polynomial $g(s)$ can be written as follows

$$g(s) = s^3 + \left(\frac{K_pV_{\text{ref}}}{L} - \frac{P}{CV_{\text{ref}}^2}\right)s^2 + \left(\frac{V_g^2}{V_{\text{ref}}^2}\frac{1}{LC} - \frac{K_{\text{E}}K_pP}{CV_g^2}\right)s + \frac{K_{\text{E}}K_p}{LC} \tag{5.34}$$

Design Constraint for Stability

- A necessary but not sufficient condition for stability is that all the coefficients of the characteristic polynomial $g(s)$ be positive. From (5.34) the following necessary constraints are derived

$$K_p > \frac{L}{C}\frac{P}{V_{\text{ref}}^3} \tag{5.35}$$

$$K_pK_{\text{E}} < \frac{V_g^4}{V_{\text{ref}}^2}\frac{1}{LP} \tag{5.36}$$

- In order to ensure that the poles of system are in the LHP, which guarantees the system stability, the Routh's criterion is used. From (5.33) and (5.34), the following Routh's table is constructed

$$\begin{array}{ll} s^3 & 1 \quad \alpha_1 \\ s^2 & \alpha_2 \quad \alpha_0 \\ s^1 & \beta_1 \\ s^0 & \alpha_0 \end{array} \tag{5.37}$$

According to Routh's criterion the poles of the system will be in LHP, provided that the following conditions are satisfied

1) $\alpha_2 > 0$, which is the same constraint provided by (5.35).
2) $\beta_1 > 0$, being $\beta_1 = \alpha_2\alpha_1 - \alpha_0$ an additional constraint is obtained

$$K_{\mathrm{E}}K_p\left(-\frac{PV_{\mathrm{ref}}K_p}{LCV_g^2} - \frac{1}{LC} + \frac{P^2}{C^2V_g^2V_{\mathrm{ref}}^2}\right) + \frac{K_pV_g^2}{L^2CV_{\mathrm{ref}}} - \frac{PV_g^2}{LC^2V_{\mathrm{ref}}^4} > 0 \tag{5.38}$$

Hence, solving (5.38) for K_{E} results in

$$K_{\mathrm{E}} < f(K_p), \tag{5.39}$$

where $f(K_p)$ is defined as follows

$$f(K_p) \triangleq \frac{\kappa_1K_p + \kappa_2}{K_p(\kappa_3K_p + \kappa_4)} \tag{5.40}$$

being,

$$\kappa_1 = \frac{V_g^2}{L^2CV_{\mathrm{ref}}} \tag{5.41a}$$

$$\kappa_2 = -\frac{PV_g^2}{LC^2V_{\mathrm{ref}}^4} \tag{5.41b}$$

$$\kappa_3 = \frac{PV_{\mathrm{ref}}}{LCV_g^2} \tag{5.41c}$$

$$\kappa_4 = \frac{1}{LC} - \frac{P^2}{C^2V_g^2V_{\mathrm{ref}}^2} \tag{5.41d}$$

5.3.4 Parametric Region of Stability

Remark. *The hyperbola corresponding to* $K_pK_{\rm E} = V_g^4/V_{\rm ref}LP$ *is above of the manifold defined by* $K_{\rm E} = f(K_p)$ *for all* $K_p > 0$,

Proof.

$$\frac{K_{\rm E}}{f(K_p)} = \frac{V_g^4}{V_{\rm ref}}\frac{1}{LP}\frac{AK_p + B}{DK_p + E} \triangleq \frac{N_2(K_p)}{D_2(K_p)}$$

where $N_2(K_p)$ and $D_2(K_p)$ are straight lines, such that $N_2(K_p) > D_2(K_p)$, $\forall K_p$, as shown in Fig. 5.13. From the slopes of $N_2(K_p)$ and $D_2(K_p)$, m_1 and m_2 respectively,

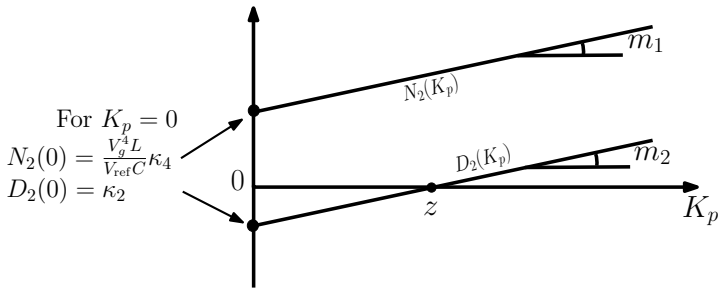


Figure 5.13: Slopes of $N_2(K_p)$ and $D_2(K_p)$

we obtain

$$\frac{m_1}{m_2} = \frac{V_g^4}{V_{\rm ref}}\frac{1}{LP}\frac{PV_{\rm ref}}{LCV_g^2}\frac{L^2CV_{\rm ref}}{V_g^2} = 1$$

Then, it is verified that $\frac{K_{\rm E}}{f(K_p)} > 1$, $\forall\ K_p > 0$ □

Consequently, as constraint (5.39) is more restrictive than (5.36); the manifold $K_{\rm E} = f(K_p)$ will be the upper boundary of $K_{\rm E}$.

The behavior of function $f(K_p)$ is analyzed as follows

a) If K_p tends to zero, $f(K_p)$ becomes as follows

$$\lim_{K_p\to 0} f(K_p) \approx \lim_{K_p\to 0} \frac{\kappa_2}{\kappa_4}\frac{1}{K_p} = \begin{cases} -\infty & \text{if} \quad K_p \to 0^+ \\ \infty & \text{if} \quad K_p \to 0^- \end{cases} \tag{5.42}$$

provided that $\kappa_4 < 0$, which leads to a design hypothesis given by $P < \frac{V_g V_{\rm ref}}{\sqrt{L/C}}$.

b) If the value of K_p tends to infinite, $f(K_p)$ tends to 0.

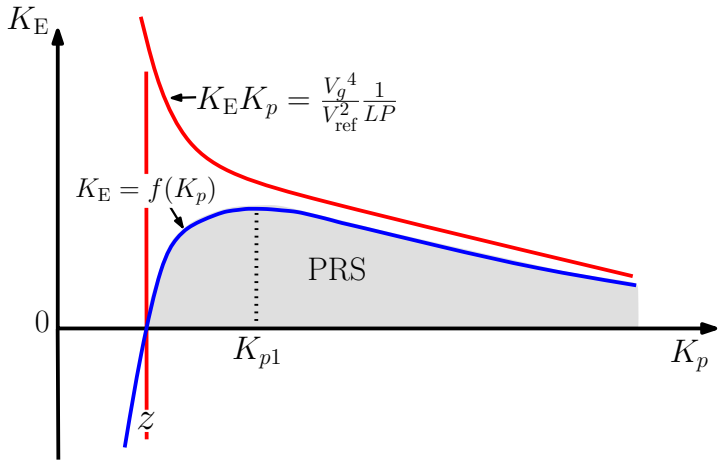


Figure 5.14: Parametric region for stability in the plane K_p–K_{E}

c) The manifold $K_{\mathrm{E}} = f(K_p)$ has a zero given by

$$K_p = z = -\frac{\kappa_2}{\kappa_1} = \frac{PL}{CV_{\mathrm{ref}}^3} \tag{5.43}$$

In summary, the value of K_{E} becomes as follows

$$\begin{array}{lcll} K_{\mathrm{E}} & < & 0 \text{ if} & K_p < z \\ K_{\mathrm{E}} & > & 0 \text{ if} & K_p > z \end{array} \tag{5.44}$$

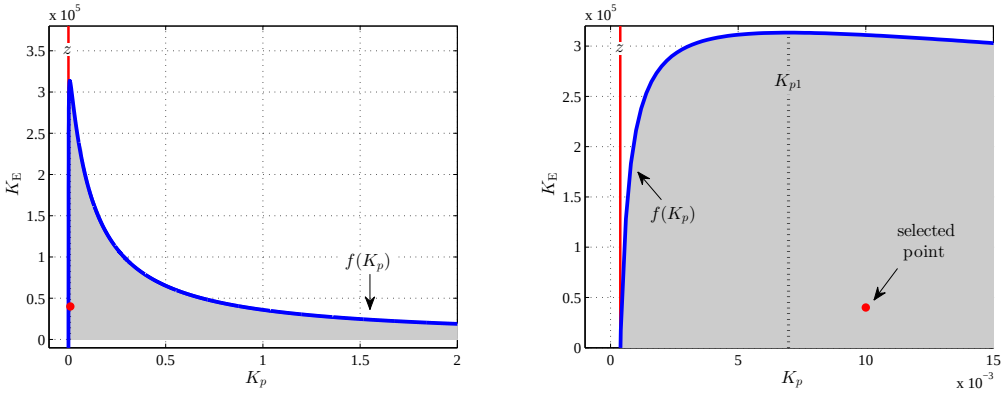
Furthermore, for $z < K_p < \infty$ the function $f(K_p)$ has a relative maximum K_{p1} given by

$$K_{p1} = \frac{PL}{CV_{\mathrm{ref}}} - \frac{V_g}{V_{\mathrm{ref}}^2}\sqrt{\frac{L}{C}} \tag{5.45}$$

On the other hand, note that z is the lower limit value of the constraint (5.35), and from (5.44), the system stability will be ensured for $K_{\mathrm{E}} < f(K_p)$ and $K_p > z$. Fig 5.14 shows in the plane $K_p - K_{\mathrm{E}}$ the PRS, which is coloured in grey. Values of zero z and position of relative maximum K_{p1} are also depicted.

5.3.5 Numerical Simulations and Experimental Results

With the aim of validating the proposed control, numerical simulations and experimental measurements have been performed. The numerical simulations have been carried out using PSIM© software. The parameter values are the same ones shown in Table 3.1.



(a) PRS of the system.

(b) Zoom of the PRS for the selected point.

Figure 5.15: PRS in the plane K_p–K_E for the proposed system.

The control parameters K_p and K_E have been selected in the PRS, which is illustrated in Fig. 5.15(a). Note in Fig. 5.15(b), that according to (5.35), K_p must be greater than $38{\times}10^{-3}$. Also, for the values of $K_p > z$, the values of K_E are the ones under the manifold $K_E = f(K_p)$. The relative maximum is located in $K_{p1} = 0.0070$ and it is equal to $K_E = 313 \times 10^3$. In order to avoid high inrush current and a fast settling time without overshoot, the values of K_p and K_E have been selected as 0.01 and 40000 respectively, these values being located inside of the PRS as it can be corroborated in Fig. 5.15(b). In addition, the value of parameter K_A is equal to 0.002. These gains have been used for both, simulation and experimental tests.

Experimental Setup

The circuit scheme of the boost converter with the proposed PWM adaptive control is depicted in Fig. 5.16. The power stage is the same used in the test described in Section 3.4, but inductor current i_L has been measured with gain $1/2$, while input voltage and output voltage are sensed with gains $1/50$ and $1/100$ respectively. The implemented PWM adaptive stage is based on LF347 operational amplifiers. The analogue divisions and squaring are performed by IC AD633. The sawtooth signal v_{ramp} is provided by the function generator Tektronik AFG2021 and establishes a switching frequency of $f_s = 100$ kHz. The comparator used for PWM operation is an LM319, by means

Chapter 5. PWM nonlinear analog control: virtual mesh approach and adaptive strategy with CPL power estimation

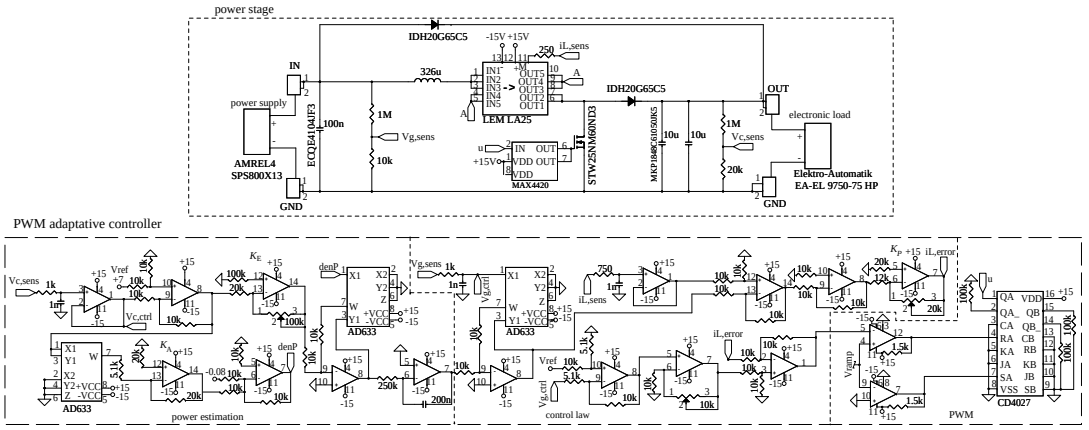


Figure 5.16: Circuit schematic of the boost converter with the proposed PWM adaptive control.

of which the sawtooth signal is internally compared with signal v_{ctrl}. Furthermore, in order to avoid noise effects in the comparator decision, sawtooth signal v_{ramp} and control signal v_{ctrl} have been increased by a factor of 10. Also a Flip-Flop CD4027 is used to synchronize v_{ramp} and v_{ctrl} signals.

Results

Numerical simulations of the system during the start-up and steady-state are illustrated in Fig. 5.17. It can be observed an inrush current of 20 A. The steady-state is attained in 5 ms, without overshoot in the capacitor voltage. Besides, the steady-state average values of the inductor current and the capacitor voltage are in agreement with (5.29), 5 A and 350 V, respectively.

Fig. 5.18(a) and Fig. 5.18(b) illustrate the simulation and experimental results respectively, of the response of the system in front of disturbances of 20 % in the input voltage. Power source AMREL SPS800x13-K02D has been used to provide the input voltage changes from 200 V to 250 V with a slope of 6.25 V/ms and from 250 V to 200 V with a slope of 12.5 V/ms. A zero steady state error in the output voltage is observed, while the inductor current tracks accurately its equilibrium point $\overline{I_L}^* = P/V_g$. Note that both capacitor voltage and inductor current exhibit a fast recovery. The experimental results closely resembled the simulated results.

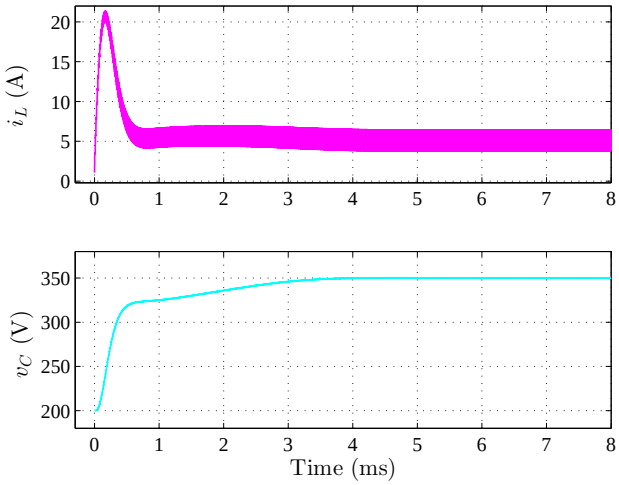


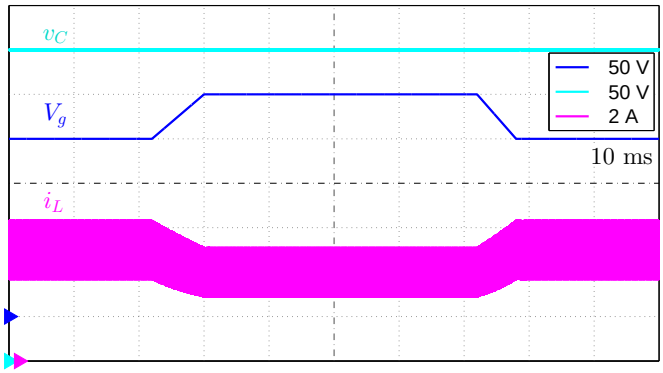
Figure 5.17: Simulated waveforms of the inductor current and the capacitor voltage of the boost converter feeding a CPL with the proposed control.

Moreover, the effects of output power changes, from 1 kW to 0.5 kW and restored back to 1 kW are depicted in Fig. 5.19(a) and Fig. 5.19(b) for numerical simulations and experimental results respectively. The capacitor voltage exhibits a zero steady-state error as well as fast recovery and small overshoot and undershoot. The steady-state of the inductor current $\overline{I_L}^*$ is 2.5 A when the output power is 0.5 kW, as predicted by the theoretical analysis. A perfect agreement is again observed between simulations and experiments.

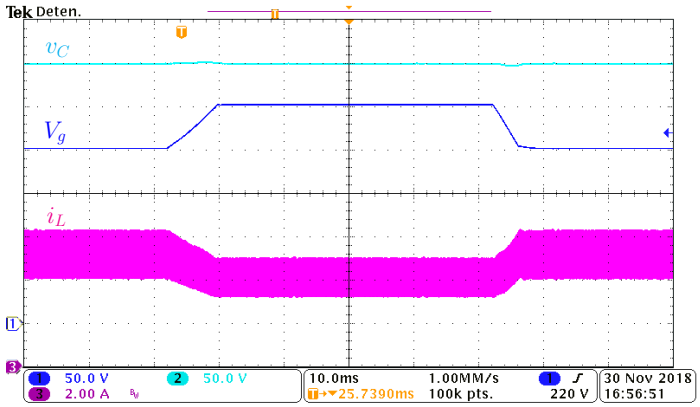
The converter operating in two different equilibrium points is illustrated in Fig. 5.20 and Fig. 5.21, *i.e*, for two different values of input voltage, V_g=200 V and V_g=250 V respectively. It can be observed that the respective average values of the inductor current are 5 A and 4 A. Therefore, an analog control operating at a constant switching frequency has been tested.

On the other hand, the control voltage v_{ctrl} is a slight modification of (5.24) because it uses the instantaneous values of the state variables instead of the average ones. The resulting expression of v_{ctrl} is

$$v_{\text{ctrl}} = \frac{V_{\text{ref}} - V_g}{V_{\text{ref}}} + K_p \left(\frac{\hat{P}}{V_g} - i_L \right) \tag{5.46}$$

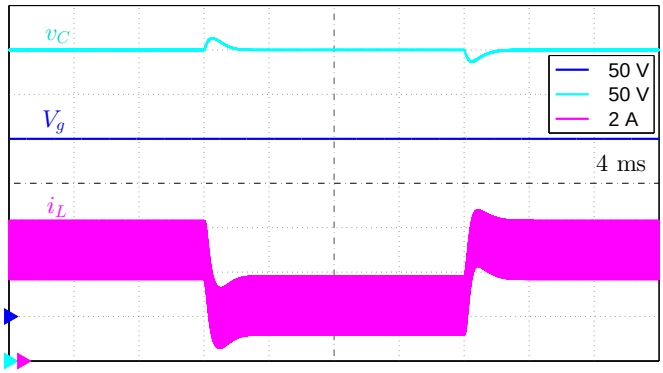


(a) Simulation results

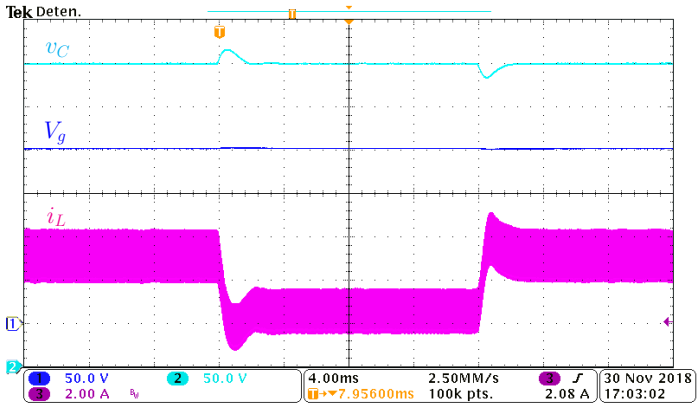


(b) Experimental results

Figure 5.18: Measured transient response in front of input voltage changes from 200 V to 250 V and restored back.



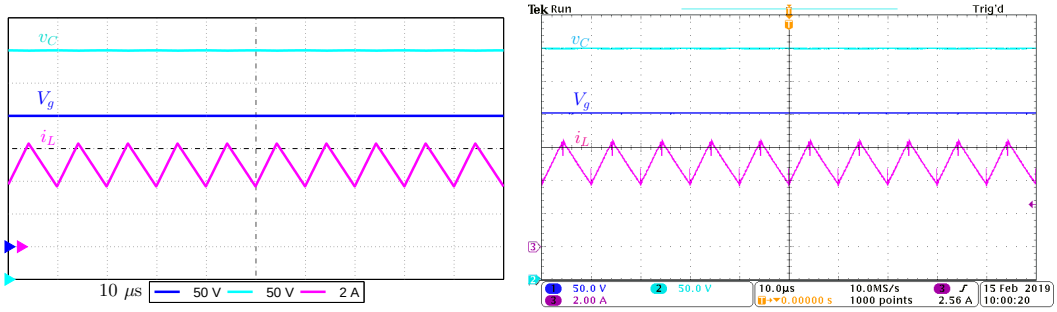
(a) Simulation results



(b) Experimental results

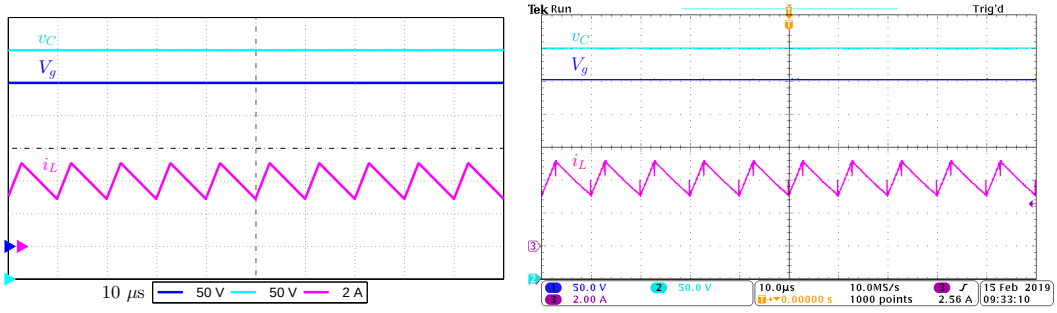
Figure 5.19: Measured transient response in front of load changes from 1 kW to 0.5 kW and restored back.

Chapter 5. PWM nonlinear analog control: virtual mesh approach and adaptive strategy with CPL power estimation



(a) Simulation results (b) Experimental results

Figure 5.20: Steady-state of the converter for $V_g = 200$ V and $f_s = 100$ kHz



(a) Simulation results (b) Experimental results

Figure 5.21: Steady-state of the converter for $V_g = 250$ V and $f_s = 100$ kHz

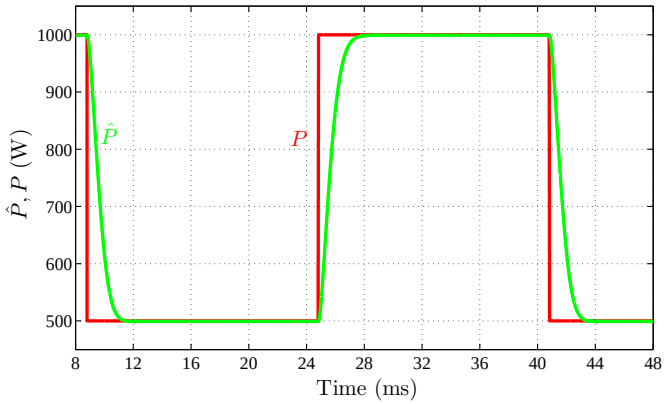
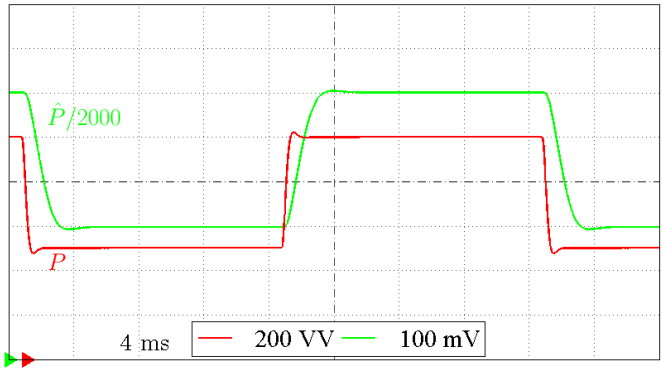


Figure 5.22: Numerical simulation of the power estimation without resistive losses.

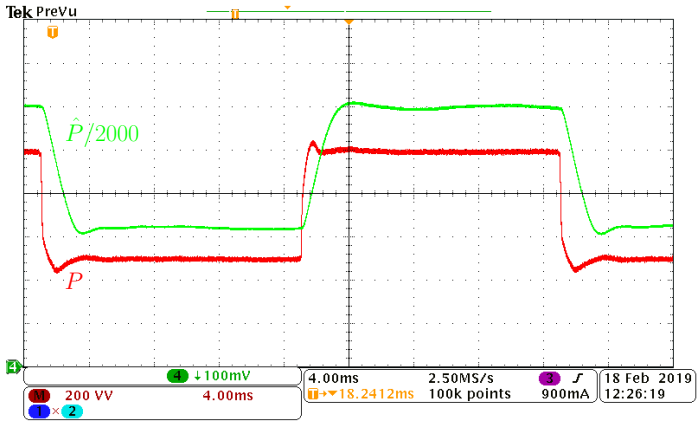
It can be observed that the ripple in v_{ctrl} is mainly due to the inductor current i_L since the ripple of the other state variables is negligible. However the second term of v_{ctrl} is a correcting element that will operate in the transient states.

A numerical simulation of the operation of the power estimation is depicted in Fig. 5.22. It can be observed that the variable $\hat{P}$ quickly reaches the new value of the CPL for power variations of step type in P from 1 kW to 0.5 kW and from 0.5 kW to 1 kW. However, the unmodelled resistive losses provokes a steady state tracking error, as shown in Fig. 5.23. Consequently, theoretical predictions, numerical simulation and experimental results are in remarkable concordance.

Chapter 5. PWM nonlinear analog control: virtual mesh approach and adaptive strategy with CPL power estimation



(a) Simulation results.



(b) Experimental results.

Figure 5.23: Effect of the resistive losses on the output power estimation.

Chapter 6

Synthesis of CPLs Using Switching Converters under SMC

6.1 Introduction

All along the previous chapters, CPLs have been described by their mathematical definition for either analytical or simulation purposes, they having been experimentally emulated by the electronic load EL 9000 from ELEKTRO-AUTOMATIK operating in constant power mode.

In this chapter, we analyze the operating conditions in a power converter to emulate a CPL. First, we explore the closed-loop behavior of a high efficient power converter with a large bandwidth in order to reproduce the ideal regulation behavior describer in Chapter 1. Secondly, we study the use of nonlinear switching surfaces of power type in the SMC of power converters. In the latter case, the analysis covers buck-type converter on the one hand, and non-minimum phase converters such as boost, boost with output filter (BOF), Ćuk or SEPIC on the other hand.

The study in the case of the buck converter is used subsequently to investigate the cascade connection of a boost converter using the SMC of Chapter 3 and a buck converter emulating a CPL.

6.2 Instantaneous CPL based on a Buck Converter

In this section, the design of a buck converter operating as an instantaneous CPL is presented. Fig. 6.1 shows a buck converter that is controlled in sliding-mode.

Two switching surfaces $S_{v2}(x)$ and $S_{P2}(x)$ are considered, namely:

$$S_{v2}(x) = K_{C2}(v_{C2} - V_{\text{ref2}}) + K_{i2}\frac{d}{dt}(v_{C2} - V_{\text{ref2}}) \tag{6.1a}$$

$$S_{P2}(x) = v_{C2}i_{L2} - P_{\text{ref}} \tag{6.1b}$$

The first switching surface was extensively analyzed in the buck converter in the early applications of SMC in power converters [71], where it was demonstrated that output voltage regulation is ensured with fast recovery of the desired value in front of external disturbances. The underlying idea here is that step variations in the load current or in the load resistance will be almost instantaneously absorbed by the inductor current with a negligible variation in the output voltage, which eventually will result in a practically instantaneous change of the output power. Since the converter is a

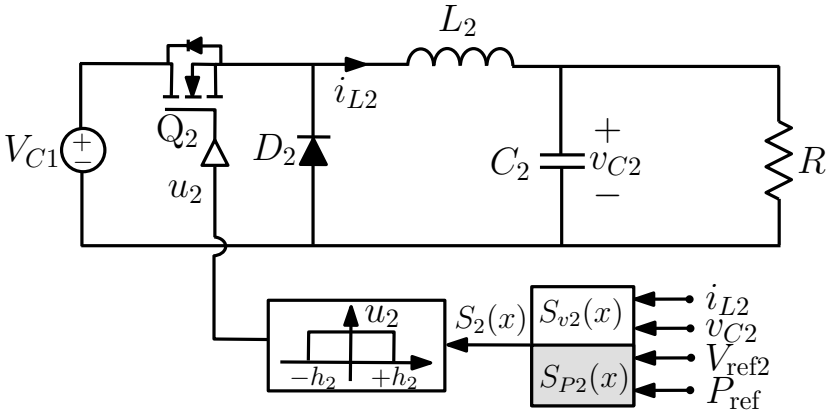


Figure 6.1: Buck-converter-based CPL with the proposed SM control.

two-port network of POPI type (dc input power=dc output power) [72], the average value of the input power will also undergo a fast change, which will confer a CPL nature to the buck converter seen from its input port.

The switching surface corresponding to (6.1b) is nonlinear and will force the product of output voltage and inductor current to be equal to the reference power if sliding

motions can be induced in the system. Below, conditions for existence of sliding mode regime will be derived. The dynamic description of the buck converter can be expressed as follows:

$$\frac{di_{L2}}{dt} = -\frac{v_{C2}}{L_2} + \frac{V_{C1}}{L_2}u_2 \tag{6.2a}$$

$$\frac{dv_{C2}}{dt} = \frac{i_{L2}}{C_2} - \frac{v_{C2}}{C_2 R} \tag{6.2b}$$

The switching law is defined as follows

$$\begin{array}{lll} u_2 = 0 & \text{if} & S_{P2}(x) > 0 \\ u_2 = 1 & \text{if} & S_{P2}(x) < 0 \end{array} \tag{6.3}$$

Conditions to induce sliding motion in the system are given by [35]

$$\left.\begin{array}{lll} \dot{S}_{P2} < 0 & \text{if} & S_{P2} > 0 \\ \dot{S}_{P2} > 0 & \text{if} & S_{P2} < 0 \end{array}\right\} \Longrightarrow \dot{S}_{P2} S_{P2} < 0 \tag{6.4}$$

The time derivative of the switching function S_{P2} is as follows

$$\frac{dS_{P2}}{dt} = \frac{i_{L2}^2}{C_2} - \frac{v_{C2} i_{L2}}{C_2 R} - \frac{v_{C2}^2}{L_2} + \frac{v_{C2} V_{C1}}{L_2} u_2 \tag{6.5}$$

Therefore, it is deduced from (6.4) for $u_2 = 0$

$$\frac{dS_{P2}}{dt} = \frac{i_{L2}^2}{C_2}\left(1 - \frac{v_{C2}}{i_{L2}}\left(\frac{1}{R} + \frac{v_{C2}}{i_{L2}}\frac{C_2}{L_2}\right)\right) < 0 \tag{6.6}$$

Defining $z_w = {}^{v_{C2}}/_{i_{L2}}$, (6.6) is rewritten as follows

$$\frac{dS_{P2}}{dt} = \frac{i_{L2}^2}{C_2} w(z_w) < 0 \tag{6.7}$$

where

$$w(z_w) = 1 - z_w\left(\frac{1}{R} + z_w \frac{C_2}{L_2}\right), \tag{6.8}$$

Hence, the constraint (6.7) will be fulfilled if $w(z_w)$ is negative. Note that function $w(z_w)$ has a maximum value (M_w) for $z_w = -L_2/2RC_2$

$$M_w = 1 + \frac{L_2}{4R^2 C_2} \tag{6.9}$$

It can be easily demonstrated that constraint given by (6.6) will be fulfilled in the region

$$\frac{\frac{1}{R}-\sqrt{\frac{1}{R^2}+\frac{4C_2}{L_2}}}{2\frac{C_2}{L_2}} < z_w < \frac{\frac{1}{R}+\sqrt{\frac{1}{R^2}+\frac{4C_2}{L_2}}}{2\frac{C_2}{L_2}} \tag{6.10}$$

Similarly, for $u_2 = 1$, (6.5) becomes

$$\frac{dS_{P2}}{dt} = \frac{i_{L2}^2}{C_2}\left(w(z_w)+\frac{v_{C2}V_{C1}}{i_{L2}^2}\frac{C_2}{L_2}\right) > 0 \tag{6.11}$$

This condition is satisfied in the region defined in (6.10) provided that

$$\frac{v_{C2}V_{C1}}{i_{L2}^2}\frac{C_2}{L_2} + M_w > 0, \tag{6.12}$$

From (6.9) and (6.12), the condition to ensure the existence of sliding motion becomes

$$\frac{v_{C2}}{i_{L2}^2} > -\frac{1}{V_{C1}}\frac{L_2}{C_2}\left(\frac{1}{4}\frac{L_2}{R^2C_2}+1\right) \tag{6.13}$$

Equivalent control

The equivalent control u_{eq2} is obtained by imposing the conditions $S_{P2} = 0$ and $\dot{S}_{P2} = 0$, which leads to the following expression

$$u_{eq2} = \frac{L_2 P_{\text{ref}}}{C_2 R V_{C1} v_{C2}} + \frac{v_{C2}}{V_{C1}} - \frac{i_{L2}^2 L_2}{V_{C1} v_{C2} C_2} \tag{6.14}$$

Ideal sliding dynamics

Substitution of (6.14) into (6.2a) leads to the ideal sliding dynamics of the system,

$$g(i_{L2}) = \frac{di_{L2}}{dt} = \frac{i_{L2}}{C_2}\left(\frac{1}{R}-\frac{i_{L2}^2}{P_{\text{ref}}}\right) \tag{6.15}$$

Note that (6.15) represents a nonlinear system and has an equilibrium point given by

$$\begin{aligned} {I_{L2}}^* &= \sqrt{\frac{P_{\text{ref}}}{R}} \\ {V_{C2}}^* &= \sqrt{P_{\text{ref}} R} \end{aligned} \tag{6.16}$$

Linearizing (6.15) around the equilibrium point I_{L2}^* results in

$$\left.\frac{dg(i_{L2})}{di_{L2}}\right|_{i_{L2}=I_{L2}^*} = -\frac{2}{RC_2}, \tag{6.17}$$

Finally, it can be concluded from (6.17) that the equilibrium point is stable.

Table 6.1: Used parameter values for the buck converter.

L_2	C_2	V_{C1}	V_{C2}^*	R	$f_{s_{\text{nom}}}$
196 μH	110 μF	350 V	60 V	3.6 Ω	100 kHz

6.2.1 Simulation Results of the Buck Converter Operating as CPLs.

Numerical simulations have been carried out using PSIM© software, where a switched model of the buck converter with the two proposed sliding surfaces has been implemented. The parameter values used for the buck converter [73] are summarized in Table 6.1. On the other hand, note that the control law proposed in (6.3) implies that the system switches with an infinite frequency. Experimentally this would be impossible, so the proposed SMC can be implemented by using a hysteresis comparator with a hysteresis band, which will determine a nominal switching frequency $f_{s_{\text{nom}}}$. Hence, the control law (6.3) turns into

$$\begin{array}{lll} u_2 = 0 & \text{if} & S_{P2}(x) > +h_2 \\ u_2 = 1 & \text{if} & S_{P2}(x) < -h_2 \end{array} \tag{6.18}$$

where $h_2 > 0$ is the value of the hysteresis width. Thus, the proposed SMC can operate at a finite switching frequency. Besides, the same control law is used for S_{v2}.

Simulation results of the buck converter operating as CPLs with the sliding function $S_{P2}(x)$

The schematic circuit diagram implemented in PSIM© software of the buck converter with the sliding function $S_{P2}(x)$, is depicted in Fig. 6.2. In the control parameters, the power reference is $P_{\text{ref}} = 1$ kW, and the hysteresis width is h_2 =76 W for a nominal switching frequency $f_{s_{\text{nom}}}$ of 100 kHz.

The transient response during the start-up and in steady-state of the buck converter under the sliding funtion is illustrated in Fig. 6.3. From the observation of the waveforms, an inacceptable inrush current is appreciated, hence the output power of system is also large. To avoid an excessive inrush current, a soft-start strategy is adopted. It consists in an alternative current sliding surface $\Sigma_a = \{x | S_a = i_{L2} - I_{\text{ref2}} = 0\}$, which is used until the output voltage has reached some pre-established value [74]. Fig. 6.3(b)

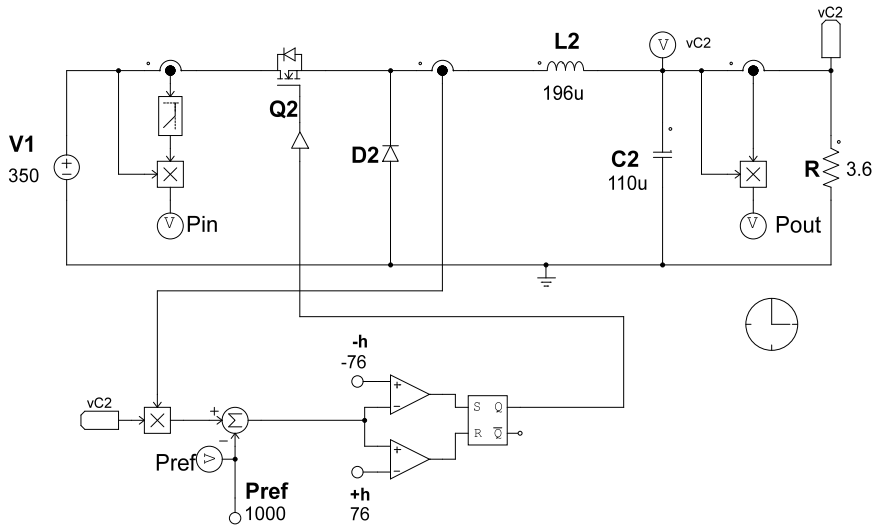


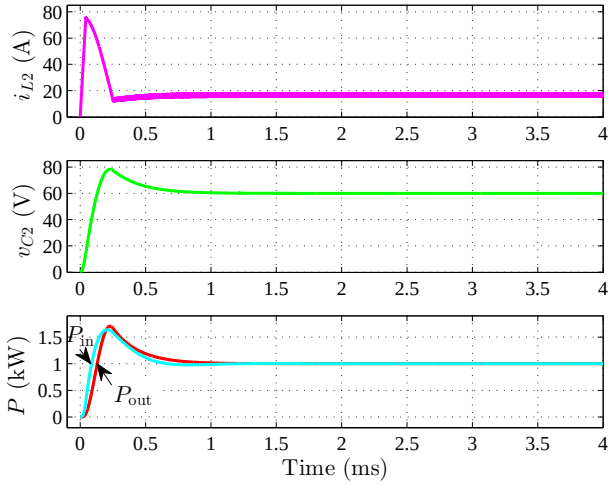
Figure 6.2: PSIM© schematic circuit diagram of the buck converter with the proposed power reference sliding surface $S_{P2}(x)$.

depicts the waveforms of the inductor current, output voltage, and output power of the buck converter with the proposed soft-start control. It can be observed that the inrush current is negligible but the demanded power is not equal to the reference power instantly.

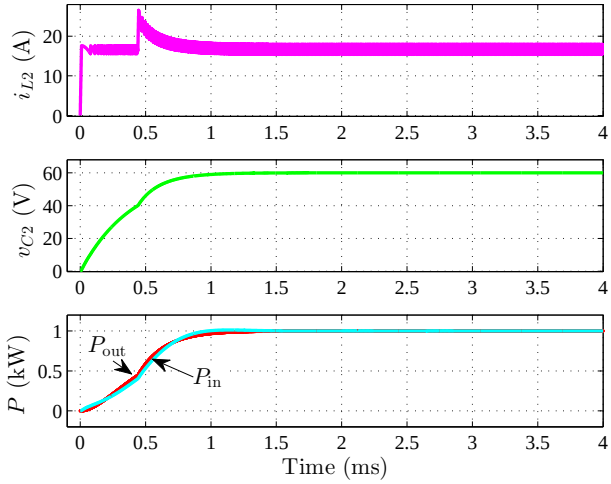
The response of the converter in front of changes in the power reference P_{ref} demonstrates that the buck converter can operate as instantaneous CPL for power reference changes as illustrated in Fig. 6.4. P_{ref} changes from 1 kW to 0.5 kW and from 0.5 kW to 1 kW. Note that the inductor current changes almost immediately and, as a consequence, the output power follows the power reference and the input power equals the power reference. Hence, the buck converter under the proposed control demands a constant power to its voltage source, which could be another converter.

Simulation results of the buck converter operating as CPLs with voltage regulation

The schematic circuit diagram of the buck converter with the sliding function $S_{v2}(x)$ implemented in PSIM© software is depicted in Fig. 6.5. The value of the gains are $K_v = 3$ and $K_d = 0.001$, $V_{\text{ref2}} = 60$ V, and the hysteresis width is 11 V in order to operate at a nominal switching frequency $f_{s_{\text{nom}}}$ of 100 kHz.



(a) without soft-start.



(b) with soft-start.

Figure 6.3: Start-up and steady-state of the buck converter operating as instantaneous CPL under the power reference sliding function $S_{P2}(x)$.

Chapter 6. Synthesis of CPLs using switching converters under SMC

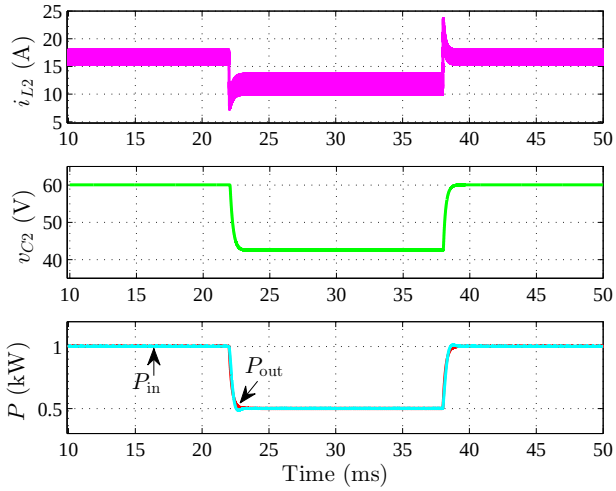


Figure 6.4: Numerical simulation of the transient response of the buck converter in front of changes of step type in P_{ref}.

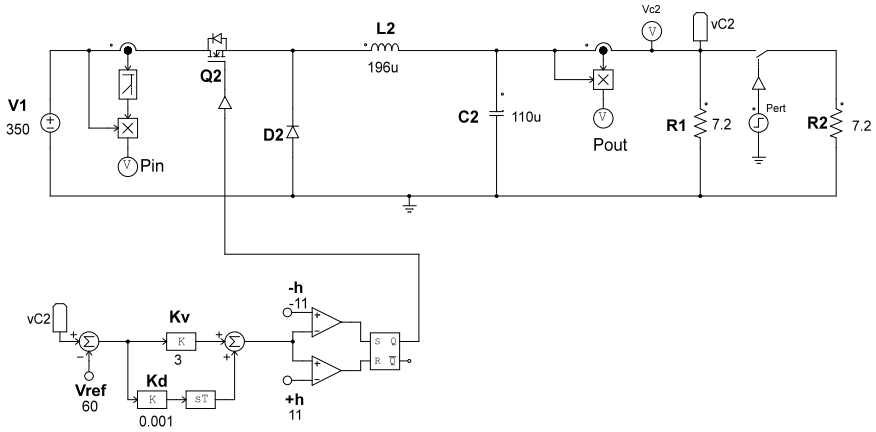


Figure 6.5: PSIM© schematic circuit diagram of the buck converter with the sliding surface $S_{v2}(x)$.

Table 6.2: Summary of components used for the experimental prototype of the buck converter operating as CPL .

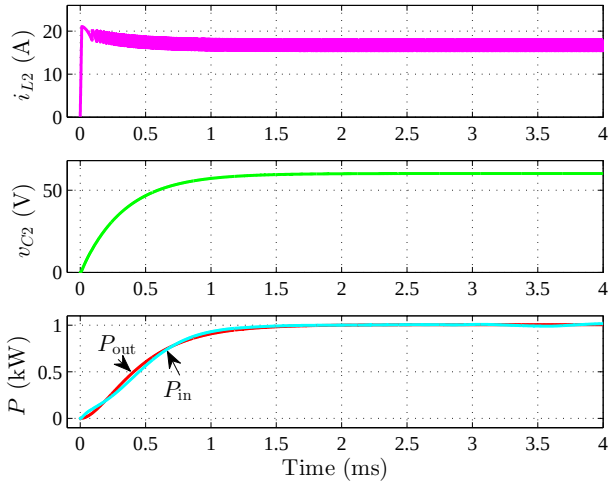
parameter	component
L_2	–
C_2	MKP1848610094P4 and UVZ2W101MRD
C_{in}	ECQE4105JF2
Q_2	STW25NM60ND
D_2	IDH20G65C5XKSA2
R	ARCOL or EA-EL 9750-75 HP

Fig. 6.6(a) shows the response of the instantaneous CPL based on a buck converter during start-up and steady-state. It can be observed that the inrush current is negligible. Note that the nominal power of 1 kW is not achieved until the output voltage reaches the reference voltage.

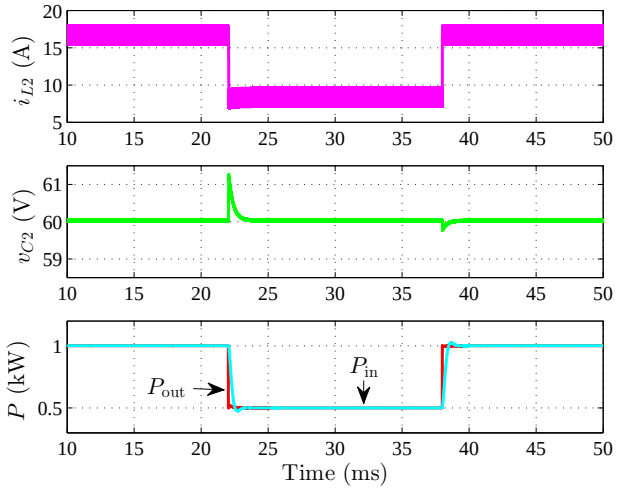
Similarly, the buck converter under the proposed SMC can be tested as CPL at different power levels, which is performed by changing the load resistance, *i.e,* when the resistance R_2 is disconnected, the buck converter will absorb 50% of the nominal power. In Fig. 6.6(b) the response of the system in front of changes in the resistance load from 3.6 to 7.2 Ω and from 7.2 to 3.6 Ω is illustrated. It can be noted that the inductor current changes almost instantly to its new equilibrium value, while the output voltage exhibits fast response. As a consequence, the output power of the buck converter varies between 1 kW and 0.5 kW instantly. Since the buck converter is a POPI system, the average of the input power will correspond to the output power value.

6.2.2 Design and Implementation of the Buck Converter.

In order to verify the theoretical predictions and the numerical simulations, an experimental prototype of the buck converter has been built. The parameter values are the ones shown in Table 6.1 and the list of components is summarized in Table 6.2. On the other hand, Fig. 6.7 shows the schematic circuit of the buck converter and the sliding



(a) Start-up and steady-state.



(b) Changes of step type in the load resistance.

Figure 6.6: Buck converter behavior as an instantaneous CPL under sliding function $S_{v2}(x)$.

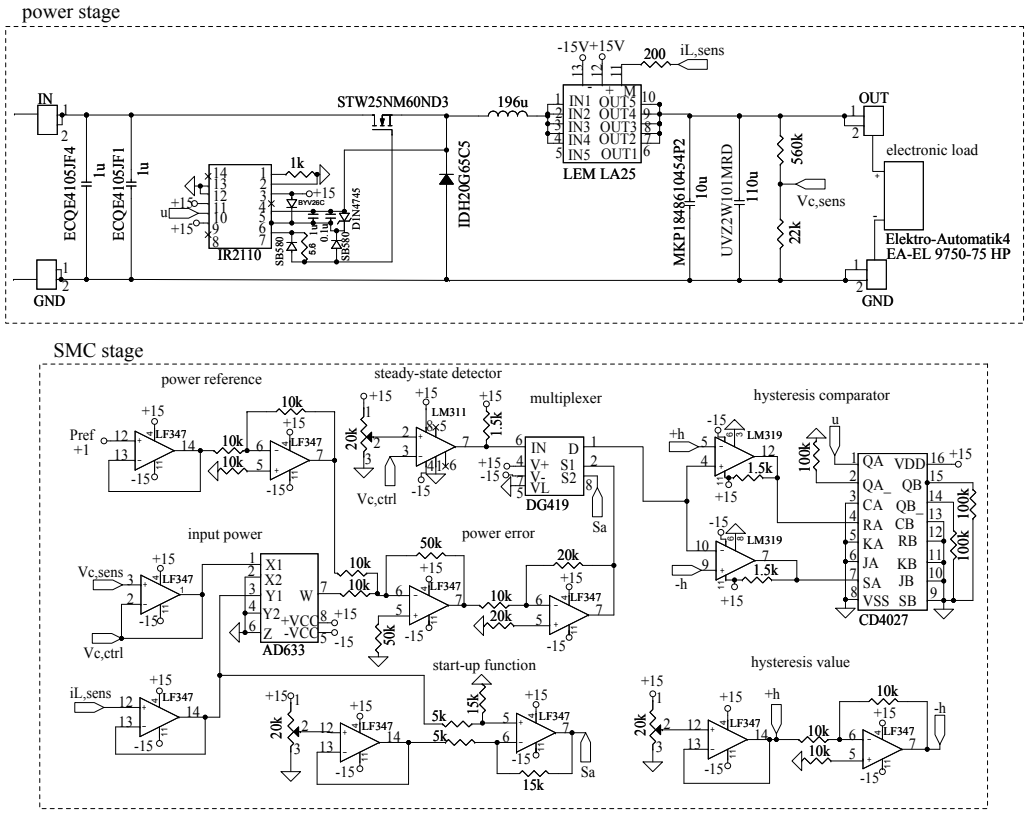


Figure 6.7: Schematic circuit of the implemented experimental prototype of the buck converter under sliding function S_{P2}.

function $S_{P2}(x)$. The inductor current i_{L2} is sensed using an LEM LA-25 sensor with gain $1/5$. A voltage divider with gain $1/100$ has been used to sense the output voltage. In the SMC stage, different blocks can be observed, namely, input power, power reference, power error function, start-up function, steady-state detector, multiplexer, hysteresis value and hysteresis comparator. The operational amplifiers are of LF347 type. The AD633 IC has been used as multiplier, and the power reference is provided externally. In the start-up sliding surface block, the value of the startup current is established and it will operate until the system has reached a given output voltage value. The hysteresis band has been scaled according to the sensed signals and it can be easily changed to adjust the nominal frequency. Finally, the comparator used to implement the proposed control law is the LM319.

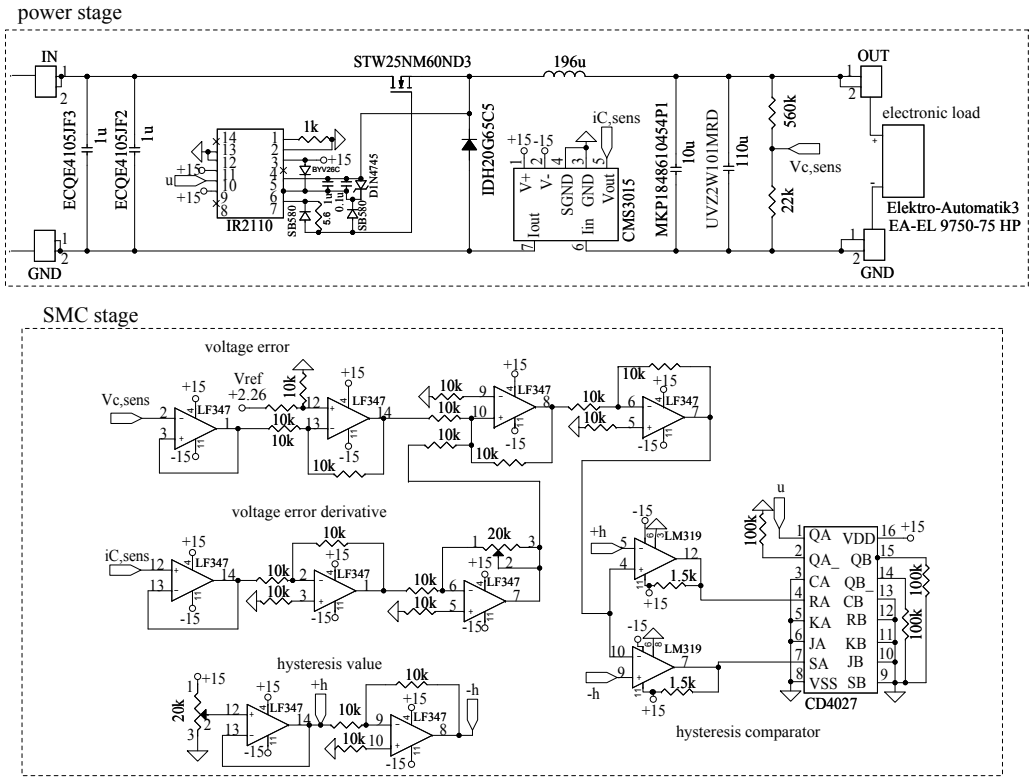


Figure 6.8: Schematic circuit of the implemented experimental prototype of the buck converter under sliding function S_{v2}.

Fig. 6.8 shows the schematic circuit of the buck converter with the sliding function S_{v2}. The inductor current i_{L2} is sensed with gain $1/5$, and the output voltage with gain $1/22$. Furthermore, instead of using the voltage error derivative ($\frac{d}{dt}(v_{C2} - V_{\text{ref2}})$), the current of the output capacitor is measured using the sensor CMS3015 with gain $1/6$. In the SMC stage, different blocks can be observed, namely, voltage error, voltage error derivative, hysteresis value and hysteresis comparator. The operational amplifiers are of LF347 type, and the voltage reference is provided externally. Besides, since the voltage error derivative is replaced by the current of the output capacitor implies a multiplication by C_2, this factor is compensated in the rest of calculations. The hysteresis band has been scaled proportionally with the sensed signals and it can be easily changed to adjust the nominal frequency. Finally, the comparator used to implement

the proposed control law is the LM319.

6.3 Boost Converter Supplying Constant Power to a Buck Converter

Fig. 6.9 shows the cascade connection of the boost and buck converters previously analyzed. Both converters are controlled by means of the corresponding sliding-mode strategies described in Sections 3.3 and 6.2. Namely, the boost converter employs the switching strategy corresponding to (3.11) while the buck converter can be controlled by means of $S_{v2}(x)$ or $S_{P2}(x)$. The buck converter acts as a load converter and absorbs constant power from the boost converter to eventually transfer it to the resistor connected in its output port. Both converters were designed to operate in CCM. The parameter values of the boost and buck converters are depicted in Table 3.1 and Table 6.1.

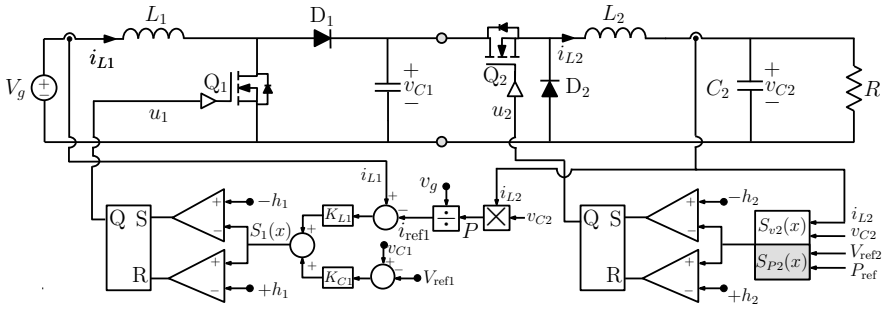
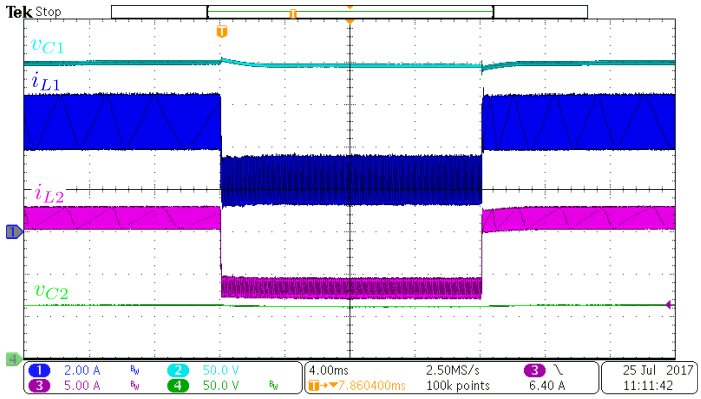
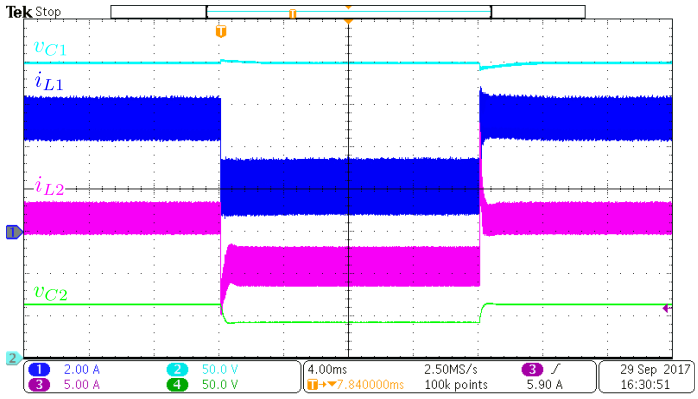


Figure 6.9: Cascade connection of two converters employing SMC: boost converter (source) and buck converter (load).

Fig. 6.10(a) illustrates the response of the boost converter to changes of step-type in the output load of the buck converter (from 3.6 Ω to 7.2 Ω and back to 7.2 Ω) when the switching surface $S_{v2}(x)$ is used to regulate the output voltage of the buck converter at $V_{\text{ref}} = 60$ V. The buck converter operates as an instantaneous CPL and the disturbance introduced by the changes in the load resistance are absorbed by the inductor currents while the output voltage of each converter remains unaltered. It can be observed that the experiment reproduces accurately the same results illustrated in Fig. 3.17(b) for the



(a) $S_{v2}(x)$ is used and the load resistance changes from 3.6 Ω to 7.2 Ω and vice-versa.



(b) $S_{P2}(x)$ is used and the reference P_{ref} changes from 1 kW to 0.5 kW and vice-versa.

Figure 6.10: Measured transient response of the boost-buck cascade connection for load changes of step-type in the power from 1 kW to 0.5 kW and back to 1 kW.

boost converter, where an electronic load in CPL mode was employed. Note also that the simulated results in Fig. 6.6(b) for the buck converter are experimentally verified.

Similar results are obtained when using the switching function $S_{P2}(x)$ in the control of the buck converter to provide abrupt variations of the absorbed power by changing the reference P_{ref} from 1 kW to 0.5 kW and back to 1 kW as illustrated in Fig. 6.10(b). Note that the variations of power affect all the state variables except the regulated

output voltage of the boost converter that remains at the desired output voltage $V_{\text{ref1}} = 350$ V.

6.4 Synthesis of CPLs Using Switching Converters under SMC

In the previous sections the operation of the buck converter acting as an instantaneous CPL under SMC has been described. The underlying idea was to design down-stream dc-dc buck converter absorbing constant power. Thus, the buck converter has mimicked an instantaneous CPL in two cases, *i.e.* (i) by changing abruptly its load resistance when the output voltage is regulated by means of a very fast controller, and (ii) by changing the reference power in a switching surface that imposes the product of capacitor voltage and inductor current to track such reference by means of an appropriate switching policy. Besides, it has been demonstrated that a boost converter supplying constant power to the proposed instantaneous CPL based on a buck converter under SMC, leads to similar results to those obtained when the CPL is emulated by an electronic load.

Hence, the synthesis of loads behaving like a power sink can offer an inexpensive alternative to analyze switching converters feeding CPLs or to be used for some other purposes [75–78]. This section offers a systematic approach to synthesize CPLs using switching converters under SMC. The study shows that switching converters with a series inductor at the input port can be used as instantaneous CPLs under SMC based on a nonlinear switching surface representing the error between the input power of the converter and a suitable power reference. Hence, a simple an inexpensive alternative is proposed to the synthesis and design of CPLs, which can be used to study the cascade connection of switching converters such as in dc distributed power systems and electric vehicles.

The purpose of the synthesis of CPLs is the design of a switching converter, which is characterized by an input port absorbing a constant power instantaneously. A switching converter is a POPI system, namely

$$P_{\text{DC}_{\text{in}}} = P_{\text{DC}_{\text{out}}} \tag{6.19}$$

Consequently, as the input power and the output power remain constant, the system will demand constant power from its power source, which will see the converter as a CPL.

Fig. 6.11 shows the block diagram of a generic dc-dc switching converter under a control law whose purpose is to operate the system as an instantaneous CPL when connected at the output of another source converter. Note that a necessary condition for this control to work is the existence of a series inductor at the input port. In order to induce CPL behavior in sliding mode regime, the sliding surface $\Sigma_{\text{CPL}} = \{x|S(x) = 0\}$ is used, where $S(x)$ is given by

$$S(x) = v_1 i_1 - P_{\text{ref}}, \tag{6.20}$$

i_1 being the current of the series inductor at the input port, v_1 the input voltage and P_{ref} the desired power reference. With the proposed sliding surface, the power at the input port is controlled to the desired value P_{ref} under voltage and current changes. Hence, under sliding mode conditions, switching converters regulated with the proposed sliding surface will behave as CPLs.

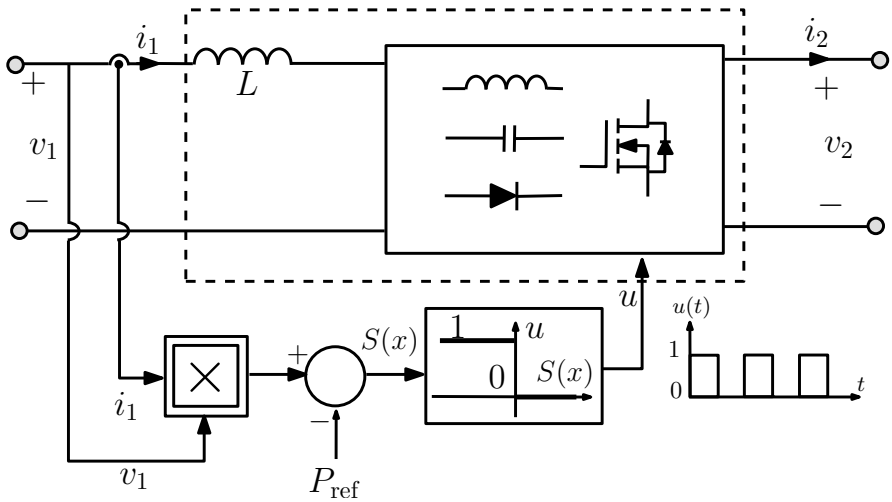


Figure 6.11: Block diagram of dc-dc switching converter with CPL characteristic.

The control law to keep the system switching around the sliding surface is defined

as follows

$$\begin{array}{lll} u = 0 & \text{if} & S(x) > 0 \\ u = 1 & \text{if} & S(x) < 0 \end{array} \tag{6.21}$$

According to the reachability condition, in order to ensure the existence of sliding motions, the following constraints must hold

$$\left.\begin{array}{lll} \dot{S}(x) < 0 & \text{if} & S(x) > 0 \\ \dot{S}(x) > 0 & \text{if} & S(x) < 0 \end{array}\right\} \Longrightarrow S\dot{S} < 0 \tag{6.22}$$

From (6.20), the time derivative of the function $S(x)$ becomes

$$\dot{S}(x) = \frac{dS(x)}{dt} = \frac{di_1}{dt}v_1 + i_1\frac{dv_1}{dt} \tag{6.23}$$

Defining $\dot{v}_1 \triangleq dv_1/dt$, Eq. (6.22) from (6.21) and (6.23), is given by

$$\dot{S}(x) = \frac{di_1}{dt}v_1 + \dot{v}_1 i_1 > 0 \quad \text{if} \quad u = 1 \tag{6.24a}$$

$$\dot{S}(x) = \frac{di_1}{dt}v_1 + \dot{v}_1 i_1 < 0 \quad \text{if} \quad u = 0 \tag{6.24b}$$

6.5 SMC of the Converter Candidates that Can Operate as CPLs.

This section presents some examples of switching converters with a series inductor in the input port that can operate as CPLs under SMC. It has to be pointed out that the converter candidates must have a series inductor at the input port, to ensure that the input current i_1, which is used to impose sliding mode regime, is a continuous time signal. Fig. 6.12 shows the schematic circuit diagram of the boost, Ćuk, transformerless SEPIC, BOF converters, and the buck converter with input filter.

6.5.1 Synthesizing a CPL Using a Boost Converter

The state equations of the boost converter in Fig. 6.12(a) are given by

$$\frac{di_1}{dt} = -\frac{v_2}{L_1}(1-u) + \frac{v_1}{L_1} \tag{6.25a}$$

$$\frac{dv_2}{dt} = \frac{i_1}{C_2}(1-u) - \frac{v_{C2}}{C_2 R}, \tag{6.25b}$$

where v_{C2} is the output voltage of the converter.

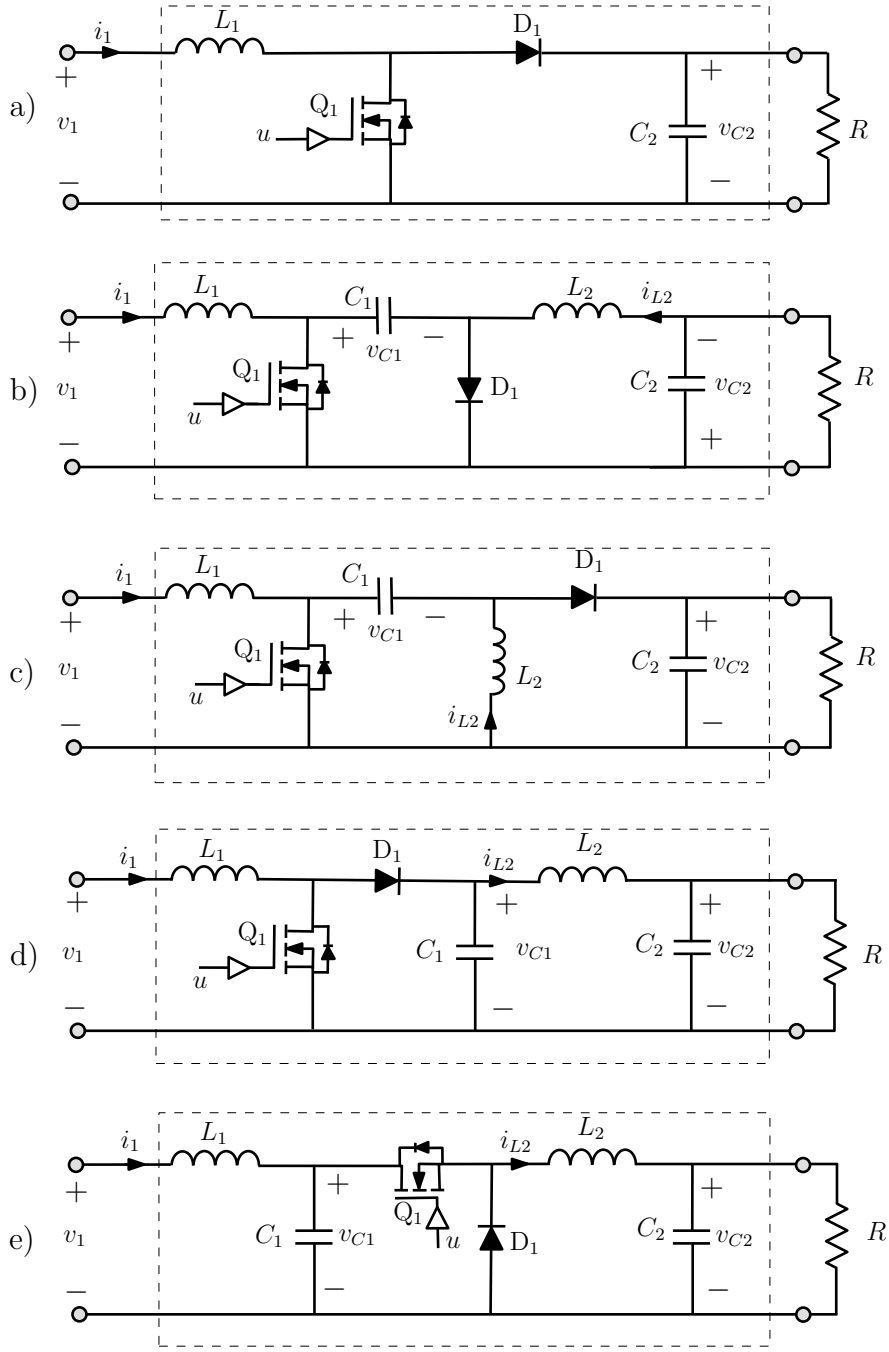


Figure 6.12: Schematic circuit diagram of converter candidates to operate as CPL. a) boost converter, b) Ćuk converter, c) transformerless SEPIC converter, d) BOF converter and e) buck converter with input filter

Existence of Sliding Mode

For $u = 1$, substituting (6.25a) in (6.24a) leads to the following inequality

$$\dot{S}(x) = \frac{v_1^2}{L_1} + i_1 \dot{v}_1 > 0 \tag{6.26}$$

A sufficient condition for (6.26) to be fulfilled is that

$$|\dot{v}_1|_{\max} < \frac{{v_{1,\min}}^2}{i_1 L_1} \tag{6.27}$$

For $u = 0$, substituting (6.25a) in (6.24b), one obtains the following inequality

$$\dot{S}(x) = -\frac{v_1}{L_1}\left(v_{C2} - v_1 - \frac{i_1 L_1 \dot{v}_1}{v_1}\right) < 0, \tag{6.28}$$

which can be rewritten in the following form

$$\dot{S}(x) = -\frac{v_1}{L_1}\left(v_{C2} - K v_1\right) < 0 \tag{6.29}$$

where K is defined as follows

$$K \triangleq 1 + \frac{\dot{v}_1}{\frac{{v_1}^2}{i_1 L_1}} \tag{6.30}$$

It can be observed that (6.29) will always be negative if K is negative. In case of K will be positive, it will be necessary to guarantee that (6.29) is fulfilled. Let us consider the following cases for $K > 0$:

(a) If $\dot{v}_1 < 0$, $|\dot{v}_1|_{\max}$ and $v_{1,\min}$ in K from (6.27), are such that

$$0 < 1 - \frac{|\dot{v}_1|_{\max}}{\frac{{v_{1,\min}}^2}{i_1 L_1}} < 1 \implies 0 < K < 1 \tag{6.31}$$

It can be seen that if $v_{C2} > v_1$, the condition given in (6.29) will be fulfilled.

(b) If $\dot{v}_1 > 0$, $|\dot{v}_1|_{\max}$ and $v_{1,\min}$ in K from (6.27), are such that

$$1 < 1 + \frac{\dot{v}_{1,\max}}{\frac{{v_{1,\min}}^2}{i_1 L_1}} < 2 \implies 1 < K < 2 \tag{6.32}$$

Therefore, in this case, the condition given in (6.29) holds if $v_{C2} > 2v_1$.

Hence, the system will have different ESM conditions depending on the derivative of the input voltage.

On the other hand, considering a constant input voltage ($v_1(t) = V_g$), so $\dot{v}_1 = 0$, and from (6.26) and (6.28), the following condition must hold to ensure ESM

$$0 < V_g < v_{C2}, \tag{6.33}$$

which is a necessary condition for the boost converter operation.

Equivalent Control

The equivalent control (u_{eq}) is obtained by imposing the condition $\dot{S}(x) = 0$. Hence, from (6.23) and (6.25a) the following expression is obtained

$$\dot{S}(x) = \frac{v_{C2}v_1}{L_1}(u_{eq}) + \frac{v_1(v_1 - v_{C2})}{L_1} + \dot{v}_1 i_1 = 0 \tag{6.34}$$

Considering a constant input voltage ($v_1(t) = V_g$) and solving (6.34) for u_{eq} results in

$$u_{eq} = \frac{v_{C2} - V_g}{v_{C2}} \tag{6.35}$$

Ideal Sliding Dynamics

The coordinates of the equilibrium point are given by

$$I_1^* = \frac{P_{\text{ref}}}{V_g} \tag{6.36a}$$

$$V_{C2}^* = \sqrt{P_{\text{ref}}R} \tag{6.36b}$$

Furthermore, the ideal sliding dynamics can be expressed only in terms of the output capacitor voltage, replacing u by u_{eq}, which yields

$$\frac{dv_{C2}}{dt} = \frac{i_1 V_g}{C_2 v_{C2}} - \frac{v_{C2}}{C_2 R}, \tag{6.37}$$

The system stability will be ensured if the linearized ideal sliding dynamics around the equilibrium point has its poles in the LFP. Hence, from (6.37) and imposing $S(x) = 0$ the ideal sliding dynamics of the boost converter in terms of the capacitor voltage is expressed as

$$\frac{dv_{C2}}{dt} = \frac{P_{\text{ref}}}{C_2 v_{C2}} - \frac{v_{C2}}{C_2 R} = g(v_{C2}), \tag{6.38}$$

Linearizing (6.38) around the equilibrium point V_{C2}^* results in

$$\frac{dv_{C2}}{dt} = \frac{dg(v_{C2})}{dv_{C2}}\bigg|_{V_{C2}^*} = -\frac{2}{C_2 R} \tag{6.39}$$

which implies that the system stability is ensured, because the linearized dynamics has a pole in the LHP.

Alternative Sliding Surface

As mentioned previously, the objective of this chapter is to design switching converters, that behave as a CPL under SMC. This objective can also be achieved by using the sliding surface $\Sigma_i = \{x | S_i(x) = 0\}$, where $S_i(x)$ is given by

$$S_i(x) = i_1 - \frac{P_{\text{ref}}}{v_1}, \tag{6.40}$$

The time derivative of $S_i(x)$ is as follows

$$S_i(x) = \frac{di_1}{dt} + \frac{P_{\text{ref}}}{v_1^2}\frac{v_1}{dt} \tag{6.41}$$

The proposed control law is defined as

$$\begin{array}{lll} u = 0 & \text{if} & S_i(x) > 0 \\ u = 1 & \text{if} & S_i(x) < 0 \end{array} \tag{6.42}$$

According to the reachability condition $S_i\dot{S}_i$, from (6.41) and (6.25a), the conditions for the existence of sliding mode are given by

$$\dot{S}_i(x) = \frac{v_1}{L_1} + \frac{P_{\text{ref}}}{v_1^2}\frac{dv_1}{dt} > 0 \quad \text{if} \quad u = 1 \tag{6.43}$$

$$\dot{S}_i(x) = -\frac{v_{C2}}{L_1} + \frac{v_1}{L_1} + \frac{P_{\text{ref}}}{v_1^2}\frac{dv_1}{dt} < 0 \quad \text{if} \quad u = 0 \tag{6.44}$$

Hence (6.43) can be rewritten as follows

$$-\frac{dv_1}{v_1^3} < \frac{1}{L_1 P_{\text{ref}}} dt \tag{6.45}$$

Solving (6.45) leads

$$\int_{t_0}^{t} -\frac{dv_1}{v_1^3} < \int_{t_0}^{t} \frac{dt}{L_1 P_{\text{ref}}} \quad \Rightarrow \quad \frac{1}{v_1^2(t)} - \frac{1}{v_1^2(t_0)} < 2\frac{t - t_0}{L_1 P_{\text{ref}}} \tag{6.46}$$

Supposing that $v_{C2} = \alpha v_1$ and $\alpha > 1$, from (6.44) the following expression is defined

$$L_1 P_{\text{ref}} \dot{v}_1 < (\alpha - 1) v_1^3 \quad \Rightarrow \quad \frac{dv_1}{v_1^3} < (\alpha - 1) \frac{1}{L_1 P_{\text{ref}}} dt \tag{6.47}$$

Integrating and solving (6.47) result in

$$\int_{t_0}^{t} \frac{dv_1}{v_1^3} < \int_{t_0}^{t} (\alpha - 1) \frac{dt}{L_1 P_{\text{ref}}} \quad \Rightarrow \quad -\left(\frac{1}{v_1^2(t)} - \frac{1}{v_1^2(t_0)} \right) < 2(\alpha - 1) \frac{t - t_0}{L_1 P_{\text{ref}}} \tag{6.48}$$

Therefore, from (6.46) and (6.48), the following constraint must be satisfied to guarantee ESM

$$\frac{1}{v_1^2(t_0)} + 2(\alpha - 1) \frac{t - t_0}{L_1 P_{\text{ref}}} < \frac{1}{v_1^2(t)} < \frac{1}{v_1^2(t_0)} + 2 \frac{t - t_0}{L_1 P_{\text{ref}}} \quad \text{for} \quad t > t_0 \tag{6.49}$$

Solving $\dot{S}_i = 0$ for the equivalent control u_{eq_i} results in

$$u_{eq_i} = 1 + \frac{v_1}{v_{C2}} + \frac{L_1 P_{\text{ref}}}{v_{C2} v_1^2} \dot{v}_1 \tag{6.50}$$

Substitution of u for u_{eq_i} in (6.25b) leads to the following ideal sliding dynamics for the converter

$$\frac{dv_{C2}}{dt} = \frac{i_1}{C_2} \left(\frac{v_1}{v_{C2}} + \frac{L_1 P_{\text{ref}}}{v_{C2} v_1^2} \dot{v}_1 \right) - \frac{v_{C2}}{C_2 R} \tag{6.51}$$

Imposing the condition $S(x) = 0$ in (6.51) leads to

$$C_2 v_{C2} \frac{dv_{C2}}{dt} = P_{\text{ref}} - \frac{v_{C2}^2}{R} + \frac{L_1 P_{\text{ref}}^2}{v_1^3} \dot{v}_1 \tag{6.52}$$

Eq. (6.52) can be rewritten as follows

$$\frac{dx}{dt} = -\frac{2}{RC_2} x + P_{\text{ref}} + \frac{L_1 P_{\text{ref}}^2}{v_1^3} \dot{v}_1, \qquad x = \frac{1}{2} C_2 v_{C2}^2, \tag{6.53}$$

It is worth mentioning that the last term in (6.53) only depends on the behavior of v_1. At the equilibrium, it can be consider that $dx/dt = \dot{v}_1 = 0$ and consequently

$$X^* = \frac{RC_2 P_{\text{ref}}}{2} \quad \Rightarrow \quad V_{C2}^* = \sqrt{R P_{\text{ref}}} \tag{6.54}$$

If $\dot{v}_1 = 0$, the equilibrium point defined by (6.54) is asymptotically stable.

However, if $\dot{v}_1 \neq 0$, $x(t)$ in (6.53) becomes as follows

$$x(t) = e^{-\frac{2}{RC_2}t}x(0) + \frac{RC_2P_{\text{ref}}}{2} + \int_0^t \frac{L_1P_{\text{ref}}^2}{v_1^3(\tau)}\dot{v}_1(\tau)e^{-\frac{2}{RC_2}\tau}d\tau \tag{6.55}$$

If the function $\frac{L_1P_{\text{ref}}^2}{v_1^3(t)}\dot{v}_1$ is bounded, $x(t)$ will be bounded. We can note that if ESM conditions are satisfied, we have

$$-P_{\text{ref}} < \frac{L_1P_{\text{ref}}^2}{v_1^3(t)}\dot{v}_1 < \left(\frac{v_{C2}}{v_1} - 1\right)P_{\text{ref}} \tag{6.56}$$

Note that the conditions of existence of sliding are more intuitive in (6.49) than in (6.26) and (6.28), but the analog implementation of the SMC (6.40), is more complicated than the implementation of the SMC proposed in (6.20). For that reason, the switching surface (6.20) is used from now onwards for the synthesis of CPLs based on power converters under SMC.

6.5.2 Synthesizing a CPL Using a Ćuk Converter

The state equations of the Ćuk converter shown in Fig. 6.12(b) are given by

$$\frac{di_1}{dt} = -\frac{v_{C1}}{L_1}(1-u) + \frac{v_1}{L_1} \tag{6.57a}$$

$$\frac{di_{L2}}{dt} = \frac{v_{C1}}{L_2}u - \frac{v_{C2}}{L_2} \tag{6.57b}$$

$$\frac{dv_{C1}}{dt} = \frac{i_1}{C_1}(1-u) - \frac{i_{L2}}{C_1}u \tag{6.57c}$$

$$\frac{dv_{C2}}{dt} = \frac{i_{L2}}{C_2} - \frac{v_{C2}}{RC_2} \tag{6.57d}$$

Sliding motion will exist if the constraints given in (6.22) are satisfied. Hence, substitution of (6.57a) into (6.22) leads to the following conditions for ESM

$$\dot{S}(x) = \frac{v_1^2}{L_1} + i_1\dot{v}_1 > 0 \quad \text{if} \quad u = 1 \tag{6.58a}$$

$$\dot{S}(x) = -\frac{v_1}{L_1}\left(v_{C1} - v_1 - \frac{i_1L_1\dot{v}_1}{v_1}\right) < 0 \quad \text{if} \quad u = 0 \tag{6.58b}$$

It can be noted that (6.58a) is identical to (6.26) and accordingly, boost and Ćuk converters have the same ESM region for $u = 1$. It can also be noticed that (6.58b) and

(6.28) are similar, so the ESM region for $u = 0$, is the same as for the boost converter but with the capacitor voltage v_{C1} of the Ćuk converter instead of the output voltage v_{C2} of the boost converter.

If a constant input voltage is considered ($v_1 = V_g$), (6.58) becomes

$$0 < V_g < v_{C1}, \tag{6.59}$$

which corresponds to constraints for Ćuk converter operation.

6.5.3 Synthesizing a CPL Using a Transformerless SEPIC Converter

The state equations of the SEPIC converter shown in Fig. 6.12(c) are given by

$$\frac{di_1}{dt} = -\frac{v_{C1}}{L_1}(1-u) - \frac{v_{C2}}{L_1}(1-u) + \frac{v_1}{L_1} \tag{6.60a}$$

$$\frac{di_{L2}}{dt} = \frac{v_{C1}}{L_2}u - \frac{v_{C2}}{L_2}(1-u) \tag{6.60b}$$

$$\frac{dv_{C1}}{dt} = \frac{i_1}{C_1}(1-u) - \frac{i_{L2}}{C_1}u \tag{6.60c}$$

$$\frac{dv_{C2}}{dt} = \frac{i_1}{C_2}(1-u) + \frac{i_{L2}}{C_2}(1-u) - \frac{v_{C2}}{RC_2} \tag{6.60d}$$

Substitution of (6.60a) into (6.24a) leads to the following ESM region for $u = 1$

$$\dot{S}(x) = \frac{v_1^2}{L_1} + i_1\dot{v}_1 > 0, \tag{6.61}$$

It can be noted that the previous condition leads to (6.26) and (6.58a) hence, the SEPIC converter for $u = 1$ has the same ESM region as the boost and the Ćuk converters.

Besides, from (6.24a) and (6.60a) the following expression is obtained

$$\dot{S}(x) = -\frac{v_1}{L_1}\left(v_{C1} + v_{C2} - v_1\left(1 + \frac{\dot{v}_1}{\frac{v_1^2}{L_1 i_1}}\right)\right) < 0 \tag{6.62}$$

Assuming $\frac{|\dot{v}_1|_{\max}}{v_{1,\min}{}^2/i_1 L_1} < 1$, $\dot{S}(x)$ can be expressed as follows

$$\dot{S}(x) = -\frac{v_1}{L_1}(v_{C1} + v_{C2} - v_1 K) < 0, \tag{6.63}$$

where $K \triangleq 1 + \dfrac{\dot{v}_1}{v_1^2/i_1 L_1}$

Hence, the following cases are considered

(a) If $\dot{v}_1 < 0$, $|\dot{v}_1|_{\max}$ and $v_{1,\min}$ are such that

$$1 - \frac{|\dot{v}_1|_{\max}}{\frac{{v_{1,\min}}^2}{i_1 L_1}} < 0 \implies K > 0 \tag{6.64}$$

(b) If $\dot{v}_1 > 0$, $|\dot{v}_1|_{\max}$ and $v_{1,\min}$ are such that

$$1 + \frac{\dot{v}_{1,\max}}{\frac{{v_{1,\min}}^2}{i_1 L_1}} < 2 \implies K < 2 \tag{6.65}$$

On the other hand, in the vicinity of the equilibrium point of the SEPIC converter $v_{C1} = v_1$ and (6.63) becomes

$$\dot{S}(x) = -\frac{v_1}{L_1}(v_{C2} + v_1(1 - K)) < 0 \tag{6.66}$$

Then, the following cases appear

$$0 < K < 1, \quad \dot{S}(x) < 0 \tag{6.67}$$

$$1 < K < 2, \quad \dot{S}(x) > 0 \tag{6.68}$$

Note that for (6.68) the time derivative of the sliding function $\dot{S}(x)$ is positive, hence condition (6.66) is not fulfilled. Besides, it is proven that the SEPIC converter will operate as a voltage step-up converter.

On the other hand, near the steady-state $v_{C2} = {}^{D}/_{1-D} v_1$, D being the duty-cycle, (6.66) becomes

$$\frac{D}{1 - D} > K - 1 \tag{6.69}$$

Defining $M(D) = {}^{D}/_{1-D}$, when the SEPIC converter operates as voltage step-down converter, there will be sliding motions if $M(D) > K - 1$ as is illustrated in Fig. 6.13.

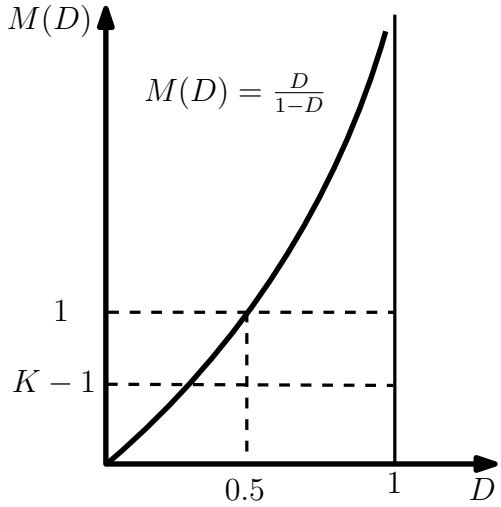


Figure 6.13: Behavior of the conversion gain $M(D)$ of the SEPIC converter with respect to D.

Finally, for a constant input voltage ($v_1 = V_g$), from (6.61) and (6.62), ESM will be ensured if the following conditions holds

$$0 < V_g < v_{C1} + v_{C2} \tag{6.70}$$

6.5.4 Synthesizing a CPL Using a BOF Converter

The state equations of the BOF in Fig. 6.12(d) are given by

$$\frac{di_1}{dt} = -\frac{v_{C1}}{L_1}(1-u) + \frac{v_1}{L_1} \tag{6.71a}$$

$$\frac{di_{L2}}{dt} = \frac{v_{C1} - v_{C2}}{L_2} \tag{6.71b}$$

$$\frac{dv_{C1}}{dt} = \frac{i_1}{C_1}(1-u) - \frac{i_{L2}}{C_1} \tag{6.71c}$$

$$\frac{dv_{C2}}{dt} = \frac{i_{L2}}{C_2}(1-u) - \frac{v_{C2}}{RC_2} \tag{6.71d}$$

Substitution of (6.71a) into (6.22) results in the following expression for existence of sliding mode

$$\dot{S}(x) = \frac{v_1^2}{L_1} + i_1\dot{v}_1 > 0 \quad \text{if} \quad u = 1 \tag{6.72a}$$

$$\dot{S}(x) = -\frac{v_1}{L_1}\left(v_{C1} - v_1 - \frac{i_1 L_1 \dot{v}_1}{v_1}\right) < 0 \quad \text{if} \quad u = 0 \tag{6.72b}$$

It can be noted that the above constraints are identical to (6.58) for Ćuk converter. Hence, both converters have the same conditions for ESM.

6.5.5 Synthesizing a CPL Using a Buck Converter with Input-filter

The state equations of the buck converter with input filter in Fig. 6.12(e) are given by

$$\frac{di_1}{dt} = -\frac{v_{C1}}{L_1} + \frac{v_1}{L_1} \tag{6.73a}$$

$$\frac{di_{L2}}{dt} = \frac{v_{C1}}{L_2}u - \frac{v_{C2}}{L_2} \tag{6.73b}$$

$$\frac{dv_{C1}}{dt} = \frac{i_1}{C_1} - \frac{i_{L2}}{C_1}u \tag{6.73c}$$

$$\frac{dv_{C2}}{dt} = \frac{i_{L2}}{C_2} - \frac{v_{C2}}{RC_2} \tag{6.73d}$$

Substitution of (6.73a) into (6.23) yields

$$\dot{S}(x) = -\frac{v_1 v_{C1}}{L_1} + \frac{v_1^2}{L_1} + \dot{v}_1 i_1 \tag{6.74}$$

Note that the derivative of switching function (6.74) is independent of the control signal u. Therefore, sliding motions cannot be induced in the buck converter with input filter and hence this converter cannot be used to synthesize a CPL.

6.6 Design of the Power Stage of the Converter Candidates that Can Operate as CPLs.

In this section, the basic design criteria of the switching converter shown in Fig. 6.12 are presented. For brevity, only the design and results of the boost converter, the Ćuk converter and the SEPIC converter will be shown in the following sections.

The necessary parameters to design the power stage are the following [79–82]:

1. Nominal input voltage, minimum input voltage and maximum input voltage: V_g, $V_{g_{\min}}, V_{g_{\max}}$
2. Nominal output voltage: V_{out}
3. Nominal power: P_{nom}
4. Maximum output current in the application: $I_{\text{out}_{\max}}$
5. Nominal switching frequency: $f_{s_{\text{nom}}}$
6. Inductor ripple current at the nominal power: $\Delta I_{L1_{\text{nom}}}$, $\Delta I_{L2_{\text{nom}}}$
7. Desired output voltage ripple: ΔV_{out}
8. Desired ripple of the coupling capacitor voltage: ΔV_{C1}
9. Forward voltage drop of the diode D_1: V_{D}
10. Steady-state duty cycle: D

6.6.1 Design of the Boost Converter

Inductor Design

The value of the inductance at the boost converter can be calculated by using the following expression

$$L_1 = \frac{V_g(V_{\text{out}} - V_g)}{\Delta I_{L1_{\text{nom}}} f_{s_{\text{nom}}} V_{\text{out}}} \tag{6.75}$$

Since the inductor ripple current $\Delta I_{L1_{\text{nom}}}$ determines the ripple of sliding surface, it is necessary to impose a wide current ripple. The inductor ripple current $\Delta I_{L1_{\text{nom}}}$ can be located between 20% to 40% of the maximum current of the CPL.

$$\Delta I_{L1_{\text{nom}}} = (0.2 \text{ to } 0.4) I_{\text{out}_{\max}} \frac{V_{\text{out}}}{V_g} \tag{6.76}$$

Capacitor Design

The value of the capacitance depends on the desired output voltage ripple and it can be determined as follows

$$C_2 > \frac{I_{\text{out}_{\max}} D}{f_{s_{\text{nom}}} \Delta V_{\text{out}}} \tag{6.77}$$

Besides, in the implementation it is recommended to use low ESR capacitors such as Polypropylene (PP) film capacitors.

MOSFET Selection

MOSFETs can be selected based on the maximum current they can handle. Hence, the maximum current $I_{\text{SW}_{\max}}$ can be calculated as

$$I_{\text{SW}_{\max}} = \frac{\Delta I_{L1_{\text{nom}}}}{2} + \frac{I_{\text{out}_{\max}}}{1-D} \tag{6.78}$$

Therefore, the MOSFET used should be able to handle this level of current.

Rectifier Diode and Start-up Diode Selection

In order to avoid high inrush current and ensure the conditions for ESM during the start-up an auxiliary diode D_a, which connects the input and output voltage, is used.

The average forward current I_{F} of both diode D and start-up diode D_a is given by

$$I_{\text{F}} = I_{\text{out}_{\max}}, \tag{6.79}$$

Therefore, the diode must be chosen based on this limitation. In addition, the dissipation power of the diode P_{D} can be considered, which is given by

$$P_{\text{D}} = I_{\text{F}} V_{\text{F}}, \tag{6.80}$$

V_{F} being the forward voltage of the diode. It is also recommended to use Schottky diodes in the implementation in order to reduce losses.

6.6.2 Design of the Ćuk Converter

Inductor Design

Inductance values of the Ćuk converter L_1, L_2 should have the same magnitude for the same inductor ripple current. Inductor values can be calculated by using the following

expression

$$L_1 = L_2 = \frac{V_g(1 - D_{\min})}{\Delta I_{L1,L2_{\text{nom}}} f_{s_{\text{nom}}}}, \tag{6.81}$$

where $D_{\min}$ is the minimum duty cycle, which is given by

$$D_{\min} = \frac{V_{\text{out}} + V_{\text{D}}}{V_{\text{out}} + V_{g_{\max}} + V_{\text{D}}} \tag{6.82}$$

Furthermore, the inductor ripple current is calculated as in (6.76).

Output Capacitor Design

The value of the output capacitance C_2, can be determined from the following expression

$$C_2 >> \frac{\Delta I_{L1,L2_{\text{nom}}}}{\Delta V_{\text{out}}} \frac{1}{8 f_{s_{\text{nom}}}} \tag{6.83}$$

The capacitance obtained in (6.83) is the minimum value, so the value of the chosen capacitance should be much higher than that value. Besides, it is recommended to use low ESR capacitors such as PP film capacitors.

Coupling Capacitor Design

The design of the coupling capacitor based on the peak-peak voltage ripple ΔV_{C1} is obtained as

$$C_1 \gg \frac{\Delta I_{L1,L2_{\text{nom}}}}{\Delta V_{C1}} \frac{1}{8 f_{s_{\text{nom}}}} \tag{6.84}$$

It is recommended that ΔV_{C1} is 10% of the nominal capacitor voltage V_{C1}. Hence, a film capacitor with a low capacitance can be used.

MOSFET Selection

MOSFETs can be selected based on maximum peak current $I_{\text{SW}_{\max}}$, which can be obtained as follows

$$I_{\text{SW}_{\max}} = I_{L1_{\max}} + I_{\text{out}_{\max}} + \Delta I_{L1,L2_{\text{nom}}} \tag{6.85}$$

Therefore, the MOSFET used should be able to hold this peak current level. Also, it should be considered that the voltage rating of the MOSFET is $V_{g_{\max}} + V_{\text{out}}$.

Diode Selection

The average forward current I_{F} of the diode D_1 is given by (6.79). Therefore, the chosen diode must be capable to hold this current. In addition, the dissipation power P_{D} of the diode is given by (6.80). In the implementation, the use of Schottky diodes is preferred in order to reduce losses.

6.6.3 Design of the SEPIC converter

Inductor Design

The inductance of the SEPIC converter can be obtained based on the peak-to-peak ripple current. Considering that the ripple current in both inductors L_1 and L_2 are equal, the inductor values are determined by

$$L_1 = L_2 = \frac{V_{g_{\min}} D_{\max}}{\Delta I_{L1,L2_{\mathrm{nom}}} f_{s_{\mathrm{nom}}}}, \tag{6.86}$$

where $\Delta I_{L1,L2_{\mathrm{nom}}}$ and $D_{\max}$ are given by

$$\Delta I_{L1,L2_{\mathrm{nom}}} = 0.4 I_{\mathrm{out}_{\max}} \frac{V_{\mathrm{out}}}{V_{g_{\min}}} \tag{6.87}$$

$$D_{\max} = \frac{V_{\mathrm{out}} + V_{\mathrm{D}}}{V_{\mathrm{out}} + V_{g_{\min}} + V_{\mathrm{D}}} \tag{6.88}$$

Output Capacitor Design

The value of the capacitance C_2, based on the desired output voltage ripple, can be obtained as follows

$$C_2 \geq \frac{I_{\mathrm{out}_{\max}}}{\Delta V_{\mathrm{out}}} \frac{D}{0.5 f_{s_{\mathrm{nom}}}} \tag{6.89}$$

The value of the capacitance obtained in (6.89) is the minimum one, so the value of the chosen capacitance should be equal or greater than that value. Besides, it is recommended to use low ESR capacitors such as PP film capacitors.

Coupling Capacitor Design

The selection of the coupling capacitor C_1 of the SEPIC converter can be obtained based on the desired peak-to-peak voltage ripple, which is calculated as follows

$$C_1 = \frac{I_{\mathrm{out}_{\max}} D_{\max}}{\Delta V_{C1} f_{s_{\mathrm{nom}}}} \tag{6.90}$$

Typically, the voltage ripple on the coupling capacitor is small. Furthermore, the RMS current through the coupling capacitor must be considered and this is given by

$$I_{C1_{\text{rms}}} = I_{\text{out}_{\text{max}}} \sqrt{\frac{V_{\text{out}} + V_{\text{D}}}{V_{g_{\text{min}}}}} \tag{6.91}$$

Hence, the chosen capacitor must be able to handle large RMS current and a voltage greater than the maximum input voltage $V_{g_{\text{max}}}$. Tantalum, ceramic and film capacitors are recommended.

Power MOSFET Selection

MOSFETs can be selected based on $I_{\text{SW}_{\text{max}}}$, which can be obtained as follows

$$I_{\text{SW}_{\text{max}}} = I_{\text{out}_{\text{max}}} \left(1 + \frac{40\%}{2}\right) \left(1 + \frac{V_{\text{out}} + V_{\text{D}}}{V_{g_{\text{min}}}}\right) \tag{6.92}$$

Therefore, the MOSFETs should be able to hold this peak current level. Also, it should be considered that the peak switch voltage rating for the MOSFETs is equal to $V_{g_{\text{max}}} + V_{\text{out}}$.

Rectifier Diode Selection

The average forward current I_{F} of the rectifier diode D_1 must be equal to the maximum output current (6.79). Therefore, the chosen diode must be capable to hold this current. In addition, the dissipation power of the diode P_{D} can be considered, which is given by (6.80).

6.7 Simulation Results of the Converter Candidates that Can Operate as CPLs.

The numerical simulations have been carried out using PSIM© software, where a switching model of boost converter, Ćuk converter and SEPIC converter with the proposed sliding surfaces has been simulated. In simulation results, the input power, output power and power reference are represented.

Table 6.3: Used parameter values for the boost converter.

L_1	C_2	P_{nom}	V_g	V_{out}	R	$f_{s_{\text{nom}}}$
326 μH	20 μF	1 kW	200 V	350 V	122.5 Ω	100 kHz

6.7.1 Simulation Results of the Boost Converter.

The parameter values used for the boost converter are summarized in Table 6.3. The value of the inductance L_1 and capacitance C_2 have been obtained using (6.75) and (6.77) respectively. Fig. 6.14 shows the schematic circuit diagram of the boost converter with the proposed control simulated in PSIM© software. The value of the reference power is $P_{\text{ref}} = P_{\text{nom}} = 1$ kW and the hysteresis width is $h = \pm 250$ W in order to generate a nominal switching frequency $f_{s_{\text{nom}}}$ of 100 kHz.

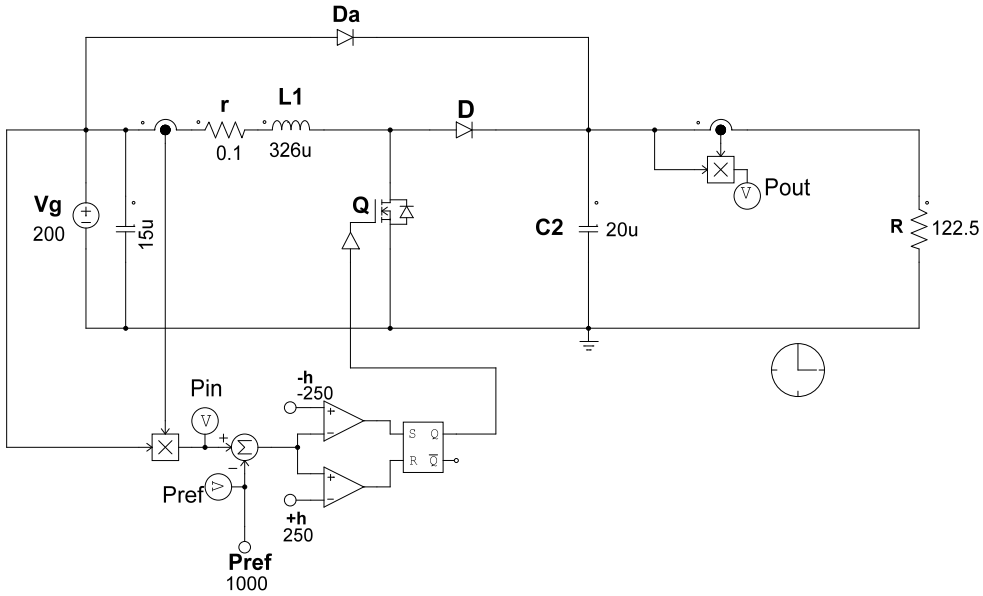
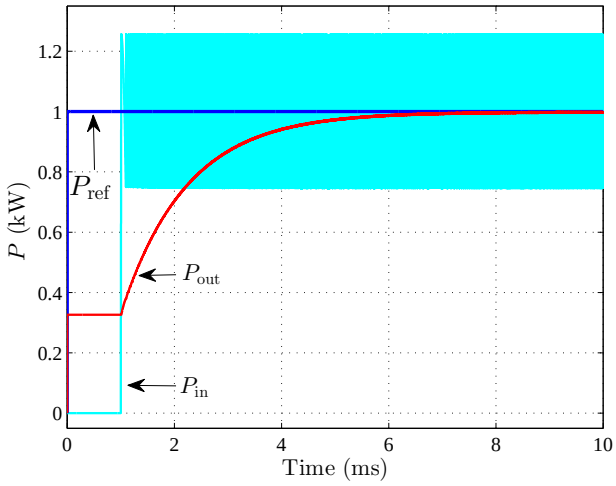
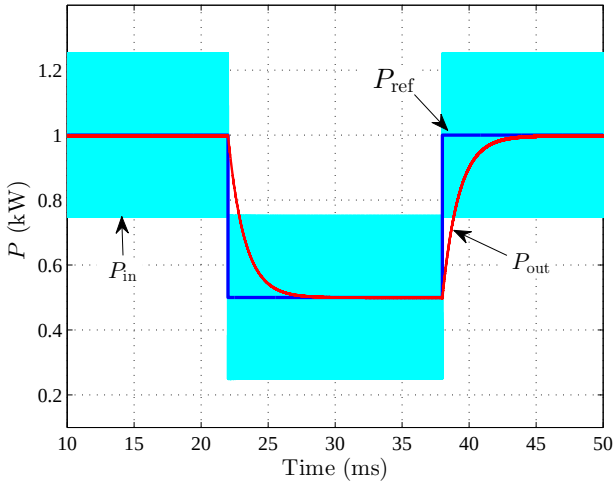


Figure 6.14: PSIM© schematic circuit diagram of the boost converter with the proposed SMC.

Fig. 6.15(a) shows the behavior of the converter with the proposed control. Note that the power at the input port reaches the power reference almost instantaneously.



(a) Start-up and steady-state.



(b) Transient response for step changes in P_{ref}

Figure 6.15: Numerical simulation of the boost converter operating as an instantaneous CPL

Besides, with the start-up diode D_a, conditions for the existence of sliding-mode are satisfied, and as a consequence there is no inrush current.

On the other hand, the transient response of the converter in front of changes at the

desired power reference P_{ref} is illustrated in Fig. 6.15(b). The power reference changes first from 1 kW to 0.5 kW and then from 0.5 kW to 1 kW. It can be observed that the input power and the output power follow accurately the reference power. Besides, the controlled input power of the converter reaches instantly the desired power.

6.7.2 Simulation Results of the Ćuk Converter.

The nominal power P_{nom}, nominal switching frequency $f_{s_{\text{nom}}}$, input voltage V_g and nominal output voltage V_{out} for the Ćuk converter have been considered equal to that of the boost converter. Consequently, the load resistance is also equal to 122.5 Ω. In addition, the inductances L_1, L_2 and the capacitances C_1, C_2 from (6.81), (6.83) and (6.84) are: $L_1 = L_2 = 540$ μH, $C_2 = 10$ μF, and $C_1 = 1$ μF respectively. Besides, the control parameters are: $P_{\text{ref}} = 1$ kW and $h = \pm 230$ W. The schematic circuit diagram implemented in PSIM© software is depicted in Fig. 6.16.

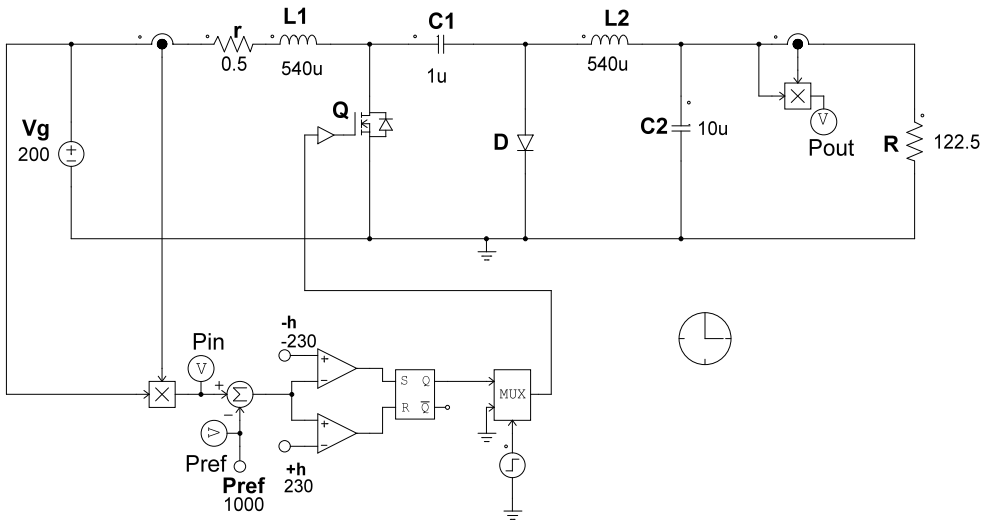


Figure 6.16: PSIM© schematic circuit diagram of the Ćuk converter with the proposed SMC.

Fig. 6.17(a) exhibits the operation of the converter as an instantaneous power sink at the input port, during start-up and in steady-state. It can be noted that there is no inrush current, because capacitor C_1 has been pre-charged to the input voltage

value. Thus, the ESM conditions are satisfied and the input power achieves the power reference almost instantaneously.

Similarly, the desired power reference can be changed to another value, as in Fig. 6.17(b). In this case, the power reference changes from 1 kW to 0.5 kW and restored back to 1 kW. As it can be observed, the input power follows accurately the reference power. Since, the Ćuk converter is a POPI system, the output power after a transition time, also arrives to the power reference.

6.7.3 Simulation Results of the SEPIC Converter.

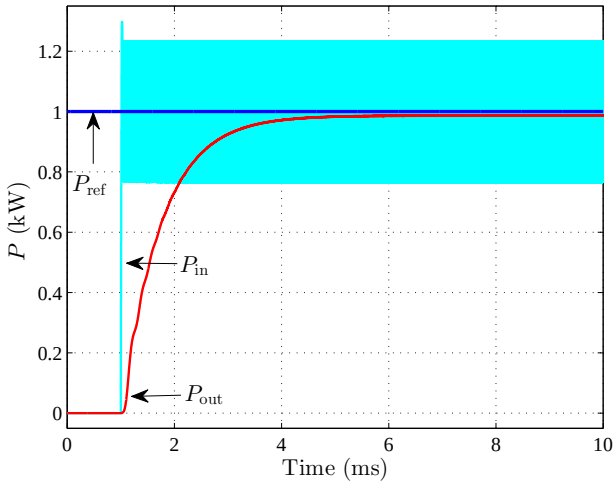
The SEPIC converter controlled to behave as an instantaneous CPL has been simulated using PSIM© software with the circuit depicted in Fig. 6.18. It can be noted that the nominal power P_{nom}, nominal switching frequency $f_{s_{\text{nom}}}$, input voltage V_g, nominal output voltage V_{out} and load resistance R for the SEPIC converter are the same than in the cases of boost and Ćuk converters. Furthermore, from (6.86), (6.89) and (6.90), the value of inductances L_1, L_2, the output capacitance value C_2 and the coupling capacitance value C_1 are: $L_1, L_2 = 580$ μH, $C_2 = 25$ μF and $C_1 = 1$ μF respectively.

Fig. 6.19(a) illustrates the behavior of the SEPIC converter during the start-up and in steady-state. Note that the delivered power at the input port is equal to the reference power almost immediately, which demonstrates the nature of an instantaneous power sink in this converter.

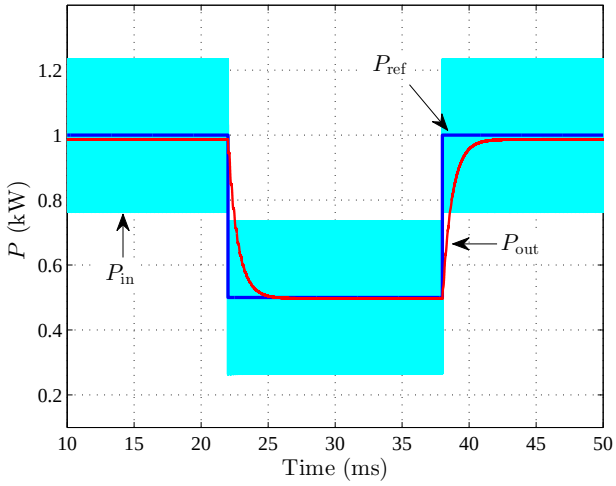
Besides, the power reference of the converter can easily be modified in order to demand a different power. In Fig. 6.19(b), this scenario is exemplified by changes of 50% in P_{ref}, namely, the power reference changes from 1 kW to 0.5 kW and from 0.5 kW to 1 kW. It can be noted that the power at the input port follows the reference power immediately without overshoots and remains in that level until the next transition, where again the operation of the converter as CPL under the proposed approach is demonstrated.

It is worth noting that since the converters are POPI systems, the output power and the input power are the same, as it can be observed in Figs. 6.15, 6.17 and 6.19.

6.7 Simulation Results of the Converter Candidates that Can Operate as CPLs.



(a) Start-up and steady-state.



(b) Transient response in front of changes of step type in P_{ref}.

Figure 6.17: Numerical simulations of the Ćuk converter behavior as an instantaneous CPL.

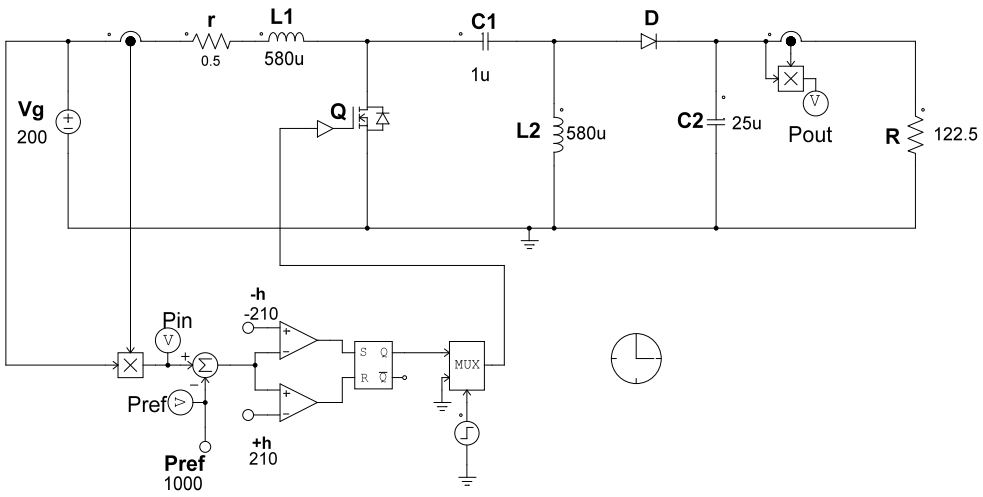


Figure 6.18: PSIM© schematic circuit diagram of the SEPIC converter with the proposed SMC.

6.8 Design and Implementation of Prototypes of the Converter Candidates that Can Operate as CPLs.

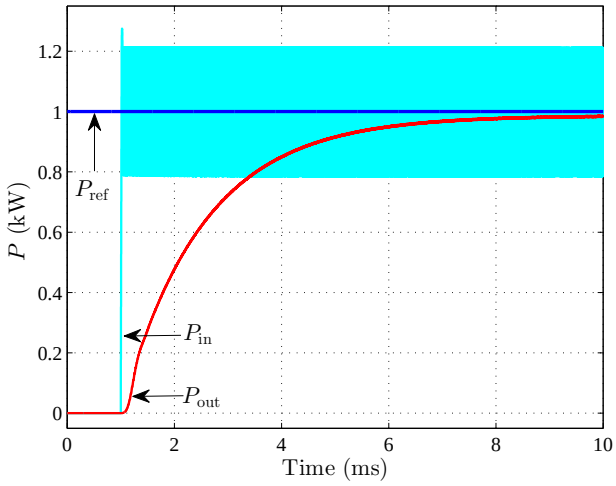
In order to verify the theoretical predictions and the numerical simulations, an experimental prototype of each converter has been built.

6.8.1 Power Stage Experimental Setup.

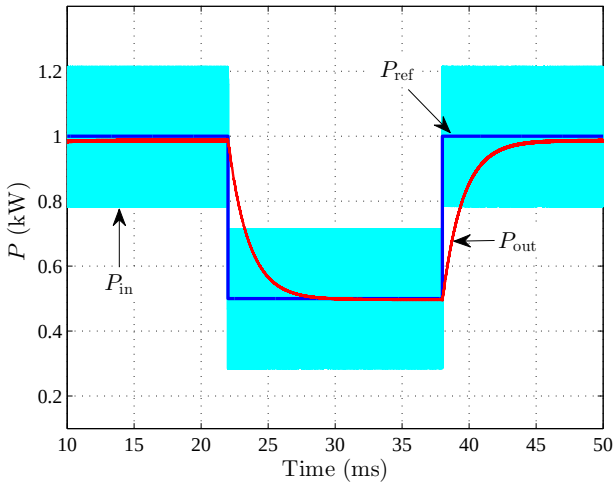
The parameter values and components for the boost, Ćuk converter and SEPIC converters have been design and selected based on the criteria given in Section 6.6.

The inductors used in each converter are of toroidal type, which use a magnetic core from MAGNETICS® company. Hence, the inductors have been in-house built. In addition, in order to implement the control stage, the input voltage V_g and the input current i_1 have to be sensed. A voltage divider with different gains depending on the converter has been used to sense the input voltage. Also, the input current has been measured using a LEM LA-25 with different gains.

On the other hand, the PCB design, according to the selected components features for each converter, has been developed in OrCad Cadence software. Finally, the list of



(a) Numerical simulation of the start-up and steady-state of the SEPIC converter



(b) Numerical simulation of the transient response of the SEPIC converter in front of changes of step type in P_{ref}

Figure 6.19: SEPIC converter behavior as an instantaneous CPL

components are summarized in Table 6.4.

Table 6.4: Summary of components used for the experimental prototype of the converters operating as CPLs.

	boost converter	Ćuk converter	SEPIC converter
Parameter	component		
L_1/L_2	–	–	–
C_1	–	MKP1848510094K2	R75MN41004030J
C_2	MKP1848C61050JK2	MKP1848610094P4	MKP1848C61550JK2
Q_1	STW25NM60ND	C3M0120090D	IRFP27N60KPBF
D_1	IDH20G65C5XKSA2	C4D08120A	C4D08120A
R	ARCOL	ARCOL	ARCOL

6.8.2 Control Stage Experimental Setup.

The proposed sliding function given in (6.20) and the proposed control law (6.18) can be implemented analogically using operational amplifiers and an analogue multiplier IC. Fig. 6.20 shows the schematic circuit diagram of the proposed control. Different blocks can be observed, namely, input power, power reference, power error, hysteresis value and hysteresis comparator. The operational amplifiers used are of LF347 type. The AD633 IC has been used as multiplier, and the power reference is provided externally. The hysteresis band has been scaled proportionally with the sensed signals and it can be easily changed to adjust the nominal frequency for each converter. Finally, the comparator used to implement the proposed control law is the LM319.

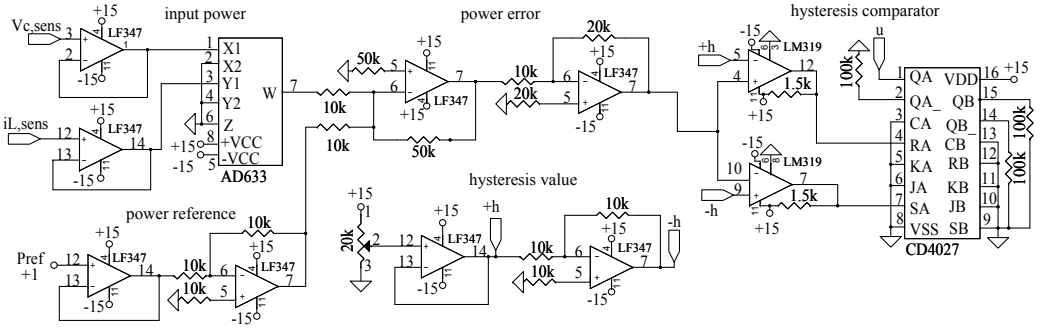


Figure 6.20: Schematic circuit diagram of the implemented control.

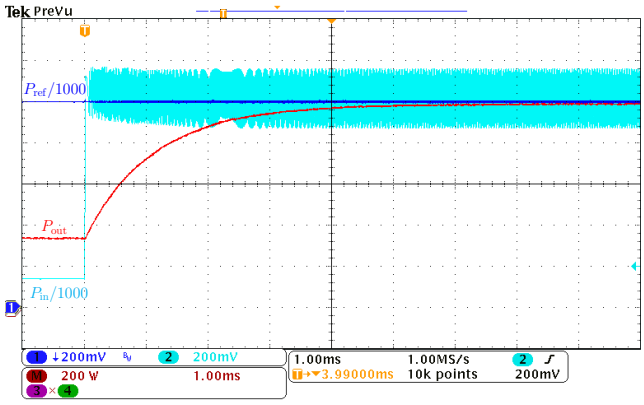
6.9 Experimental Results of the Converter Candidates that Can Operate as CPLs.

The switched converters implemented under SMC have been tested to validate their operation as instantaneous CPLs. For the tests, the power source AMREL SPS800x13-K02D has been used to provide the input voltage. Furthermore, in order to obtain the load resistance at the nominal power, a connection in series and/or in parallel of different resistances has been carried out.

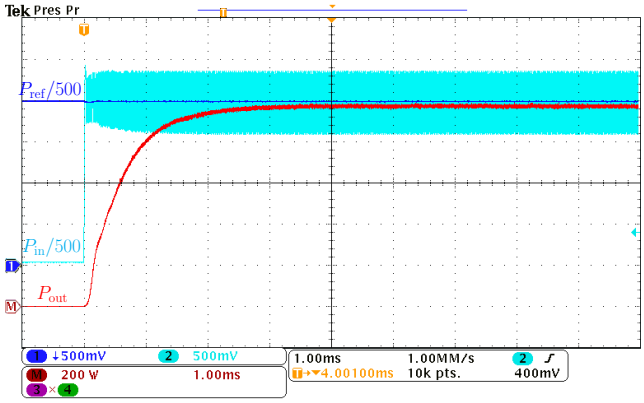
Fig 6.21 shows the response of the boost, Ćuk and SEPIC converters during start-up and in steady-state. Note that the three converters quickly reach the reference power imposed in their input port. Also, it can be observed that the Ćuk converter and the SEPIC converter have an equal settling time. On the other hand, the output power response of the SEPIC converter is the slowest one. Experimental results in Figs. 6.21(a), (b), and (c) are in good agreement with the numerical simulations in Figs. 6.15, 6.17, and 6.19 for the boost, Ćuk, and SEPIC converters respectively.

Similarly, Fig. 6.22 illustrates the response of converters to changes of step type in P_{ref}. It can be observed that the power reference change from 1 kW to 0.5 kW and from 0.5 kW to 1 kW. Note that the input power of the boost, Ćuk and SEPIC converters follows accurately the power reference. The input power changes instantaneously to the reference power in each disturbance. Furthermore, the three converters present a similar behavior during the transitions.

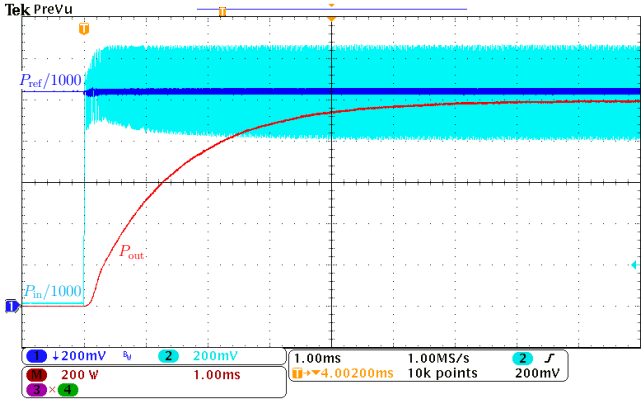
It is worth to note that experimental results closely resembled the simulated results.



(a) boost converter



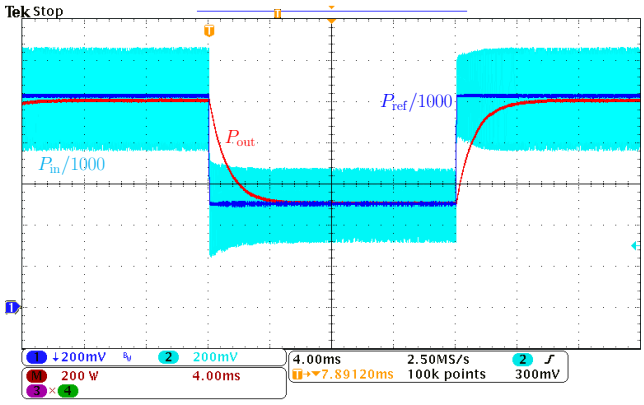
(b) Ćuk converter



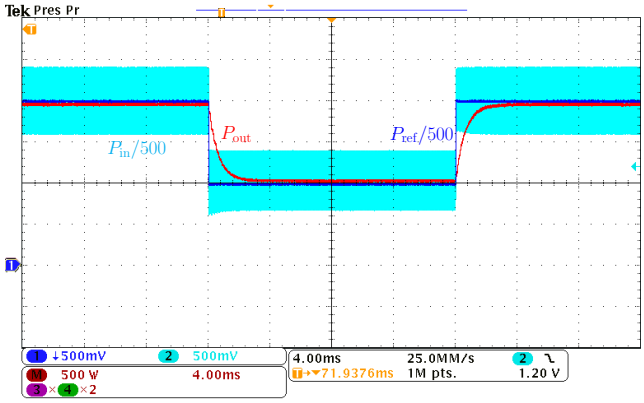
(c) SEPIC converter

Figure 6.21: Waveforms of the input, reference and output powers of the proposed converters operating as instantaneous CPLs during the start-up and in steady-state

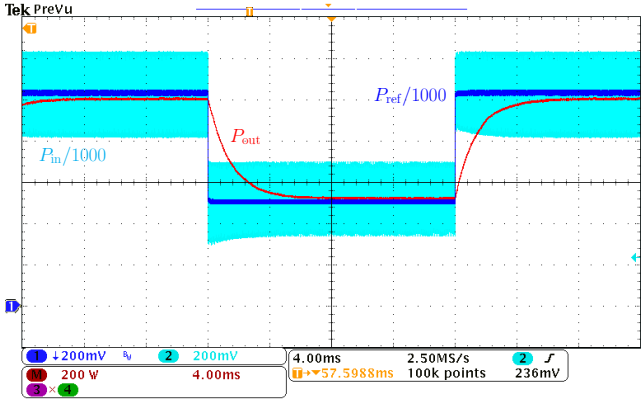
6.9 Experimental Results of the Converter Candidates that Can Operate as CPLs.



(a) boost converter



(b) Ćuk converter



(c) SEPIC converter

Figure 6.22: Transient response of input, reference and output powers of the proposed converters in front of changes on P_{ref}.

6.10 General Procedure to Design Switching Converters Operating as CPLs with the proposed sliding function $S(x)$

The general procedure for using switching converters with the proposed control as CPLs, is given as follows:

1. Select a switching converter with a series inductor at its input port.
2. Obtain the state-equations of the selected converter.
3. Determine the SMC condition using (6.22). If exists ESM, the selected converter could act as an instantaneous CPL. But if does not exist ESM, the selected converter cannot be used as a CPL.
4. Determine the equivalent control, the ideal sliding dynamics and the system stability of the converter with the proposed control. If the system is stable, the selected converter can operate as CPL.
5. Design the power stage based on the desired operation criteria, *i.e*, nominal power, input voltage, nominal output voltage, and calculate the value of the inductance/inductances, the value of the capacitance/capacitances and the value of the resistance load.
6. Use a simulation software to implement the switched model/time model of the switching converter, and to implement the proposed sliding function (6.20) with the control law (6.18). Verify that the system operates as expected.
7. Implement an experimental prototype. Select the components of both power and control stages according to the working point. Adapt the control signals to the levels of the selected IC. Use sensors to measure the input voltage and the input current.
8. Use a PCB software to design the circuit board. Print the PCB and assemble the prototype.
9. Check that the prototype works properly. Use the developed prototype as a CPL; for example, to study the behavior or to test a new controller of a converter feeding a CPL.

Chapter 7

Conclusions

The notion of CPL emerged years ago to model certain operations in multiconverter systems that have in common the cascade connections of power converters.

A first scenario to illustrate a CPL behavior results from the assumption of ideal regulation on highly efficient power converters. The insertion of an input filter in such type of converters could lead to unstable behavior for values of the CPL power higher than a certain limit given by a function of the voltage generator parameters and filter reactive elements.

A first approach to deal with modelling power converters with CPL consists in linearizing the CPL. By substituting the CPL by its negative incremental resistance, the well-known state space averaging method can be directly applied yielding transfer functions with RHP poles. Thus, it is implicitly admitted that the open-loop dynamic model of the power converter with CPL is unstable, and that closing the loop will require an effort of the feedback law to stabilize the converter and ensure output voltage regulation.

Nonetheless, there are some operations in open-loop that result in stable behavior. This is the case of buck and boost converters operating in DCM or in the boundary CCM-DCM. The boundary is established in terms of the CPL power, and again for values higher than this limit the converter becomes unstable.

A first attempt to closed-loop operation in this thesis has consisted in a two-loop PWM linear control with an internal loop based on peak current control to regulate the

output voltage of a boost converter with CPL in CCM operation. It has been shown by means of simulations that the resulting regulator performs well in the rejection to external disturbances, its weakest point being the system start-up, which requires ad-hoc circuitry to limit the high value of the inrush current.

A simple alternative to the mentioned attempt has been based on SMC using a linear switching surface to regulate the output voltage of the same converter. The switching surface leads to small values of inrush current and guarantees output voltages regulation in front of external disturbances. The voltage regulation is achieved by adapting the current reference in terms of the input voltage and the power of the CPL making it equal to the expression of the equilibrium point locus. No linearization assumptions have been used in the controller design, this eventually resulting in a good global performance under large-signal operation.

The analog SMC proposed in the thesis takes the system as it is, *i.e.* unstable during both ON and OFF intervals, and exploits the resulting unstable trajectories in each interval to appropriately combine them to obtain a stable system, which exhibits output voltage regulation and small inrush current. It is worth mentioning that only one-loop control is used and no integrators are inserted. While the PWM linear control has been designed in the frequency domain on the basis of a converter averaged linearized model, the SMC design uses the exact trajectories in the phase-plane to reach a compromise between small inrush current and fast output voltage response. This fact is explicit in the SMC approach but it is hidden in the conventional frequency-domain design, which eventually results in a deficient start-up.

The analog SMC above described exhibits variable switching frequency because the required switching policy has been implemented by means of hysteresis comparators.

To counteract the variable switching frequency of the analog SMC, a DSMC using PWM has been proposed. The design of the DSMC algorithm has been derived from an approximate discrete-time model of the converter, which predicts accurately the dynamics of the switched system. The DSCM uses a cascade control whose inner loop is a discrete-time SMC with a switching surface based on the inductor current error, which results in an unstable bahavior. The insertion of the outer loop has stabilized the system and provided output voltage regulation with negligible inrush current.

The operation under sliding-mode regime in DSMC approach helps in the inrush current limitation. It has to be pointed out that the presence of propagation delay worsens the inrush current but the problem can be relieved by forcing a non-saturated value of the duty cycle within the few initial switching cycles.

Two non-linear controllers using PWM have been also proposed to solve the problem of regulating the output voltage in a boost converter with CPL under large-signal operation and constant switching frequency. First, the use of state feedback has allowed to stabilize and regulate the output voltage in a virtual mesh. The mesh introduces a damping parameter to stabilize the closed-loop system, and an additional variable to regulate the output voltage. It has been proven by both simulations and experiments that the proposed system exhibits a good performance in the rejection of external perturbations. Secondly, a new strategy with an adaptive loop that estimates the power of CPL has been also proposed showing an excellent performance in the mitigation of the disturbances produced by changes in input voltage and CPL power.

In Chapters 3, 4 and 5, the CPL has been emulated by means of an electronic load, and by means of power converters under SMC in Chapter 6 leading to similar results in both cases. Thus, the buck converter has mimicked an instantaneous CPL in two cases, *i.e.* (i) by changing abruptly its load resistance when the output voltage is regulated by means of a very fast controller, and (ii) by changing the reference power in a switching surface that imposes the product of capacitor voltage and inductor current to track such reference by means of an appropriate switching policy. The latter approach has been applied successfully in the input port of boost, Ćuk, SEPIC and BOF converters, this opening the way to design simple and inexpensive emulations of CPLs.

The stability analysis has been performed in the boost converter and it remains open in SEPIC, Ćuk and BOF converters for further research due to the resulting high-order ideal sliding dynamics.

Chapter 7. Conclusions

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Chapter 7. List of Publications

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Chapter 7. List of Publications

UNIVERSITAT ROVIRA I VIRGILI
NONLINEAR CONTROL OF DC-DC SWITCHING CONVERTERS WITH CONSTANT POWER LOAD
Blanca Areli Martínez Treviño

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