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Characterization and Compact Modeling of Flicker Noise and Piezoelectric Effect in Advanced Field Effect Transistors

Wondwosen Eshetu Muhea

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Wondwosen Eshetu Muhea

Characterization and Compact Modeling of Flicker Noise and Piezoelectric Effect in Advanced Filed Effect Transistors

DOCTORAL THESIS

Supervised by Prof. Benjamin Iñiguez

Department of Electrical Electronic Engineering and Automation

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Statement of Supervision

UNIVERSITAT
ROVIRA i VIRGILI

Department of Electrical Electronic Engineering and Automation (DEEEA)

Av. Paisos Catalans 26,

Campus Sescelades, 43007,

Tarragona, Spain

Phone: +34 977 558524

Fax: +34 977 559605

I STATE that the present study, entitled "CHARACTERIZATION and COMPACT MODELING of FLICKER NOISE and PIEZOELECTRIC EFFECT in ADVANCED FIELD EFFECT TRANSISTORS", presented by Wondwosen E. Muhea for the award of the degree of Doctor, has been carried out under my supervision at the DEPARTMENT of Electrical Electronic Engineering and Automation of this university, and that it fulfills all the requirements to be eligible for the European Doctorate Award.

Tarragona (Spain), June 1st, 2019

Prof. Benjamin Iñiguez, Doctoral Thesis Supervisor

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To Emama and Frita....

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1. Fundamental Concepts

Silicon has ruled the advancements in semiconductor technology with the scale of integration unattainable in other materials. According to Moore's law, transistors packed onto Silicon chips have been getting double the number every two years since 1970[1]. Now, we are on the era that computers are ubiquitous in modern society, and they play significant roles in our lives. Due to the integrated circuits made of Si-based semiconductor chips and transistors, a lot of technological wonders become possible in our daily activities. At the same time, technology has been rapidly evolving to realize complex applications as diverse as Active Matrix Liquid Crystal Displays (AMLCD), image sensors, electronic photograph, 5G and 6G foldable phones, millimeter, and THz wave applications-that seemed preposterous a few years ago. Silicon is ill-suited for such technologies because they require performance traits such as flexibility, transparency to visible light, improved electrical properties, low fabrication cost, and capability of functioning in high power and high frequency operating conditions. Instead, amorphous oxide, organic, and wide bandgap semiconductors are found to be potential alternatives and change the course of electronics technology in the past decades.

In this chapter, we introduce the fundamentals of Thin Film Transistors (TFTs) and High Electron Mobility Transistors (HEMTs)-the two most explored FET devices to realize large area/flexible and power-intensive high-frequency electronic circuits for future applications, respectively.

1.1 Amorphous and Organic semiconductors

Flexible and large area electronics are among the technology domains where crystalline Silicon-based conventional MOSFETs fall short. TFT devices with amorphous oxide and organic semiconducting channel materials predominate instead. The key to a proper understanding of the operation of these devices lays in a sound knowledge of the fundamental properties of the materials used to fabricate them.

■ Amorphous oxide semiconductors

The use of amorphous semiconducting materials for device applications traced to 1979 when Spear and Le Comber demonstrated a TFT device with hydrogenated amorphous silicon (a-Si) semiconducting channel layer. Their success employing a functional a-Si:H TFT for driving Liquid Crystal Displays (LCDs) in 1981established a solid foundation for the research and development of such semiconductors in TFT technology[2]–[4].

The nature of the atomic/molecular bonding existing within amorphous semiconductors predominately influence the electrical conduction in materials. In covalent semiconductors such as a-Si:H, the overlapping of randomly distributed SP^3 orbitals give rise to the formation of orbital overlap regions within which carrier transport is possible. However, the strong spatial orientation of the hybridized SP^3 orbitals causes the orbital overlap magnitude to be susceptible to bond angle distortions that are inherent to such type of materials. As shown in Figure *1.1* ((a) and (b)), these semiconductors have degraded predictability, and exhibit a reduced amount and size of orbital overlap regions in the amorphous state[5]. For this reason, these materials have poor electrical properties, particularly low carrier mobility, which in the best-case scenario is in the order of $1cm^2/Vs$ for a-Si:H. Thus, they are not optimal enough for large area electronics, for instance, to determine pixel states over the whole area of emerging flat panel displays[6].

The demand for improved device performance and better uniformity of material properties over a large area insisted on the search for alternatives. In 1996, Hosono *et al.* proposed the idea of fabricating semiconducting thin films from oxides of metals with vacant shell electron configuration of $(n-1)d^{10}nS^0$ ($n \geq 4$). The implication was the conduction band minimum (E_m) in such metal oxides would be constructed from direct overlapping of spatially spread spherical *nS* orbitals of the heavy-metal cations. Hence, the overlapping magnitude would suffer less in amorphous oxides than in the case of covalent amorphous semiconductors (Figure 1.1 for comparison). So does the conduction path of charge carriers, and in turn, the resulting materials would possess high carrier mobility comparable to their crystalline version[5][7].

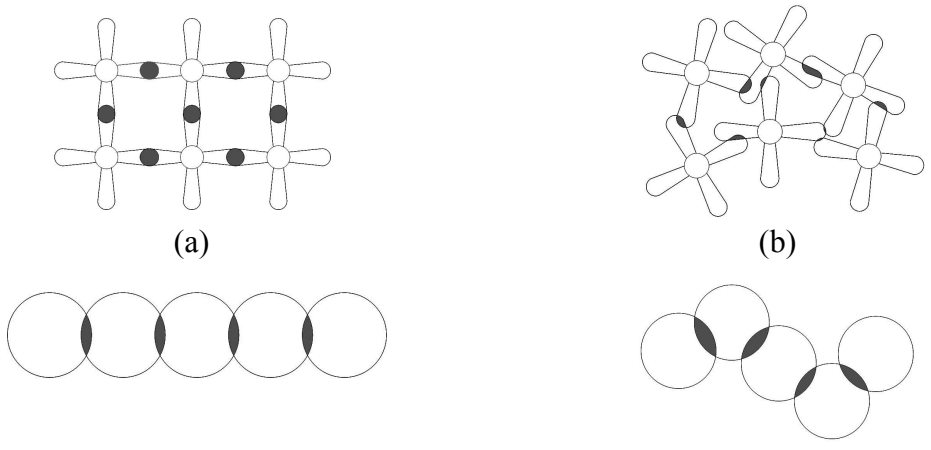


Figure 1.1 Molecular overlap regions in (a) Covalent Crystal (b) Covalent amorphous (c) Ionic oxide crystal (d) Ionic oxide amorphous semiconductor materials
(Adopted from [5])

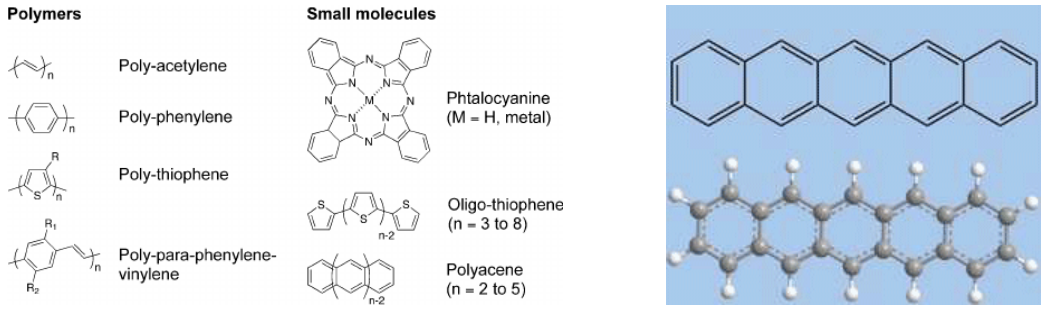
Following the above hypothesis and demonstration of binary metal-oxide thin films, transparent oxide semiconductors have become a subject of intense research[8]–[10]. That opened the door to intense investigation of multicomponent metal oxide materials for fabricating amorphous oxide semiconductors (AOS) with enhanced electrical properties. Practical multicomponent metal oxide TFTs start to appear after Nomura *et al.* reported the first amorphous InGaZnO (a-IGZO) based device processed using pulsed laser deposition

(PLD) in an oxygen atmosphere in 2004[11]. Since then, a-IGZO has been widely pursued from different perspectives. Effects of using different techniques for the deposition of the active material, optimization of the material composition, usage of varieties of substrates as well as high k dielectric gate materials, etcetera have been scrutinized-all targeting to optimize processing technologies and realize devices of superior performance[12]. These days, continuous efforts have been put on application directed study of a-IGZO TFTs to investigate reliability and stability issues, for the devices can soon become central components in a wide range of new and disruptive technologies[13]–[17].

■ Organic Semiconductors

Besides AOS, organic compound semiconductors (OCS) have been actively investigated for TFT device applications. These materials are classified into two categories: small molecules and polymers. The first group of OCSs are composed of compact systems of small molecules, and are further classified into pigments (non-soluble OSCs) and dyes (soluble OSCs).The polymeric OSCs, on the other hand, are formed from the repetition of small units called monomers and are soluble[18][19]. Although OSCs, in general, are easy for processing over their inorganic counterparts, the difference in the chemical nature of the materials determines the technology used during the production of semiconducting thin films. Small molecules are mostly deposited through thermal evaporation, whereas polymeric materials are usually vacuum deposited at low temperatures-drop casting or spin coating from solutions[20].

Both the small molecule and polymeric OCSs possess alternating double and single bonds that created a π-conjugated system across multiple atoms as illustrated in Figure *1.2*. The double bonds contain σ and π bonds. The former involves electrons donated from the atoms' *S* orbitals that are close to the positive nuclei and wherefore, they are tightly localized. However, the π bonds are formed by sharing of *P* orbital electrons between atoms. Thus, π electrons are weakly attracted to the nuclei. They can be delocalized easily because of the π orbital overlaps created between molecules during processing, and they can move from one state to another to contribute to electrical conductivity.



(a) (b)

Figure 1.2 Molecular structure of organic semiconductors (a) common conjugate small molecules and polymers (a) pentacene small molecule. (Adopted from [21] and [22])

Small molecule OSCs, when deposed by evaporation in a vacuum, form a molecular organization perpendicular to the substrate with a crystal geometry structure and morphology that promotes continuous π orbital overlaps[18][19]. As a result, TFT devices with a small molecule active layer manifest remarkable carrier mobility. On the other hand, the molecular structure in organic polymers has a higher level of structural disorder that form defects. This together with the large number of traps induced by chemical impurities hamper carrier transport in polymer-based TFTs. However, with these impediments, polymer OSCs still lend themselves to the low-cost fabrication of organic electronics directed towards large area applications[18][23].

As organic molecules are bound together by the weak van der Waals force, their lattice structure does not have the features of inorganic crystal materials. The intermolecular interactions in OSCs are not strong enough to create the conventional conduction and valance bands. Instead, the alternating conjugation of double bonds create a band like structure from the overlapping π orbitals called the lowest unoccupied molecular orbital (LUMO), and the highest occupied molecular orbital (HOMO)-separated by a forbidden energy gap which is in the order of 0.1% of Si (Figure 1.3).

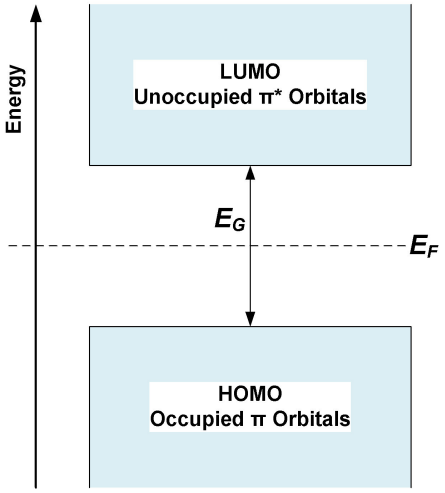


Figure 1.3 Energy band structure of Organic semiconductors.
(Adopted from[24])

The HOMO is constituted of the bonding π orbital with low energy states that are full of electrons as in the case of the valance band in crystalline inorganic semiconductors. Conversely, the LUMO is made of empty anti-bonding high energy state π orbitals and is comparable to the conventional conduction band[24].

■ Charge Transport in amorphous and organic materials

Charge transport in amorphous and organic materials is a complicated process. In amorphous semiconductors, the structural disorder (bond angles and length variations), dangling bonds, non-stoichiometry, and carrier scattering at defect sites create localized subgap states around

the conduction band edge that extend deep into the band gap. The conduction mechanism and the electrical properties of devices built from these materials strongly depend on the density of these subgap states (subgap DOS)[25][26]. Apart from that, the nature of the band structure is also determinant of the carrier transport in organic semiconductor based TFTs. It is therefore of paramount importance to study the charge transport in AOS and organic semiconductors for better understanding of the physics of TFT devices. The following paragraphs discuss the most common models found in the literature about the conduction mechanism in AOS and organic materials.

Percolation Conduction: it is more of a band like transport mechanism observed in single crystal metal oxide thin films at first. In these materials, conduction is associated with percolation of the carriers over Gaussian potential barriers generated around the conduction band edge by the S orbitals of the heavy metal cations. As percolation conduction process is seen in single-crystalline $InGa_3(ZnO)_5$ as reported by Nomura *et al.*[27], some researchers debated that it is the primary means of charge transport in multicomponent amorphous post-transition-metal oxide thin films like a-IGZO as well. That is because not only these materials possess the cations that supposedly create the potential barrier at the band edge, but they manifest high carrier mobility, in the amorphous state, in the order of magnitude close to the crystalline ones[6][28].

Multiple trapping and release conduction (MTR): is adapted to explain charge transport in materials that tend to form polycrystalline thin films such as small molecule OSCs and IGZO. In such type of materials, more efficient charge transfer takes place as band-like transport in extended (delocalized) states band. However, densely localized states present at the band edges and in the bandgap degrade the conduction by trapping/de-trapping of the majority of carriers. Thus, carrier dynamics exhibits a thermal activation behavior and is highly influenced by the multiple capture/release of carriers by the shallow localized traps populated around the mobility band edge. Concomitantly, the average carrier mobility suffers. The number of carriers available for conduction is dependent upon the energy difference between the localized trap states and the delocalized band states. A notable feature of the MTR is that it can be used to evaluate the density of localized states[18][29].

Hopping conduction: this mechanism is ascribed to the presence of a high density of localized states within a disordered material that is inherent to organic and AOS materials. Due to the densely localized DOS available populated near the band tails, charge carriers will be immobile and will more engaged in jumping from one state to another closest localized state in the vicinity (the nearest neighbor hopping) or to a site with the lowest energy level than where there were before (Variable Range Hopping/VRH). Generally, hopping conduction is a thermally activated process. Therefore, mobility is proportional to the temperature, and this usually helps to identify if such transport mechanism exists in materials. Besides, carrier mobility is influenced by the relative position of the Fermi level within the band on account of the presence of a hopping barrier at each localized state site. With the movement of the Fermi level over the localized DOS, the deep states get filled. As a result, the hopping barrier starts

to decrease, and mobility begins to improve. It is for this reason that the power law dependence of carrier mobility on gate voltage is observed in amorphous and organic TFT devices[18][29].

Generally, conduction in AOS and organic TFTs is profoundly affected by device processing technologies and other relevant factors. In some cases, only one of the methods we discussed above per se fails to adequately describe the charge transport process in a particular device of interest, as different conduction mechanisms may co-exist depending on the technologies used for fabrication (specially the process used for the active layer deposition) and the device operating condition. Some researchers conducted extensive experimental studies of charge transport in a group of a-IGZO TFTs and reported percolation conduction accompanied by the VRH/MTR mechanisms best explains their results[6][30][31].

1.2 AOS and Organic Thin Film Transistors

A TFT device shares fundamental structural and operating principles with other field effect transistors. It is a three-terminal device with a gate, source, and drain terminals wherein the gate modulates the flow of current between source and drain terminals. Unlike the MOSFET, TFTs have a non-conducting transparent/flexible substrate onto which the conducting, insulating, and semiconducting thin films are subsequently deposited. Using insulating substrates positively influence the device fabrication cost and inherently eliminates problems such as parasitic capacitances and latch-up which require additional work to avoid them (if it is possible) when using a semiconducting substrate[5].

■ Common device architectures

Since the channel layer is separate from the substrate in TFTs, there is more flexibility in the ways and order of depositing the different layers for resulting in various device configurations. Based on whether the source/drain electrodes and the gate capacitance are placed on the same or opposite sides of the semiconducting layer, a TFT can have either coplanar (C) or staggered (S) architecture as shown in Figure *1.4*.

In the first configuration, the induced channel and the source/drain contacts with the active layer are in the same plane. Thus, the current flows horizontally from the source to the drain terminal. On the other hand, in staggered devices, since the source/drain electrodes and the channel are on opposite sides of the active layer, the current flow is in two directions. Charge carriers travel the entire semiconducting layer thickness to be injected into and extracted from the channel at the source and drain terminals, respectively. For this reason, devices with staggered architecture exhibit high contact resistance that is strongly dependent on the gate voltage relative to coplanar TFTs[5].

Inside the abovementioned structural groups, TFTs are further grouped as top-gate (TG) and bottom-gate (BG) devices depending on the position of the gate electrode. In TG devices, the

gate electrode is placed on top of all layers, whereas, in BG devices, it is deposited on the substrate underneath the whole structure. Additionally, AOS TFTs can be configured into Etch Stop (ES) structure that contains an ES layer to protect damage from plasma bombardment during dry etching processing of devices[32]. TFTs with vertical configurations are also arising these days as a substitute to planar structures in the course of searching for a way to shrink device size[33].

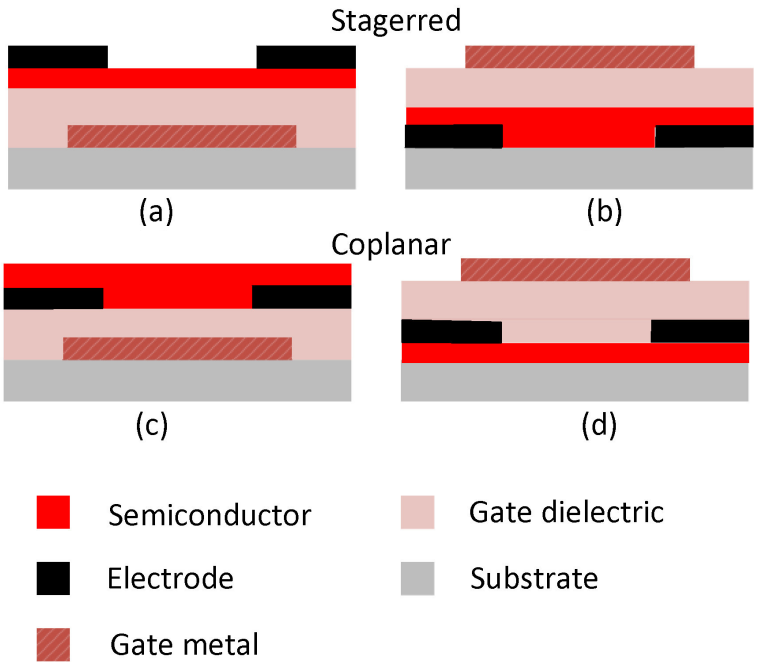


Figure 1.4 Common TFT architectures. (Reproduced from [5])

In general, each of the device configurations has associated pros and cons when it comes to the fabrication process and targeted applications. For instance, in TFTs used for back-plane circuits of LCDs, staggered BG configuration allows prevention of the light-sensitive active layer from the influence of the display backlight. Moreover, the bottom-gate structure provides the opportunity to easily modify the semiconductor, for instance by enabling quick adsorption of impurities during annealing or plasma treatments in a suitable atmosphere, but along with the undesirable instability effects that may arise due to its exposure with air[34].

■ Operating principles

Unlike in crystalline MOSFETs, the current flow in TFTs does not take place through a doped substrate. Thus, both the AOS and organic TFTs are intrinsic meaning that majority carriers are responsible for current transport through the semiconducting channel. To understand the basics of TFT operation, it is necessary to separately investigate the band diagram under zero, negative, and positive biasing conditions. Shown in Figure 1.5 are the band bending and relative position of the Fermi level under the three different scenarios for an n-type device.

With zero applied bias at the terminals (Figure 1.5 (a)), the device is in equilibrium or flat-band state-the majority carriers, which are electrons in this particular case, are not affected while the

layers in the MIS structure come into contact. Conversely, a negative potential at the gate terminal will drive the electrons away from the gate/channel interface, and the conduction band minimum and the valance band maximum will bend upward. The transistor will then be in the off state as the depletion of majority carriers in the active layer with halt the charge transport through it[5][35].

As shown in Figure 1.5 (c), a positive gate bias, on the other hand, will cause the energy bands to bend downwards. In this case, with the V_{ds} kept constant, an n-type AOS-based TFT can operate in either of the deep-subthreshold, subthreshold, and above-threshold regimes depending on the magnitude of applied gate voltage. Deep-subthreshold device operation is activated when the gate bias is far less than the device threshold voltage (the voltage at which the channel material starts to conduct current). Carrier diffusion is the principal mechanism of conduction in this operating regime. Increasing the gate voltage, the Fermi will be moving upward over the deep subgap states. Thus, the transistor enters the subthreshold regime operation where hoping conduction starts to take over and dictate the current flow in the channel layer.

Further increase of the gate voltage drives the device to the above threshold regime, wherefore more electrons will accumulate at the interface. The TFT will be in the ON state (above threshold operation) to conduct current with a potential difference applied between the source and drain terminals. The transport mechanism in this operating regime will depend on the technologies active layer deposition and device fabrication as well as operating conditions of the device.

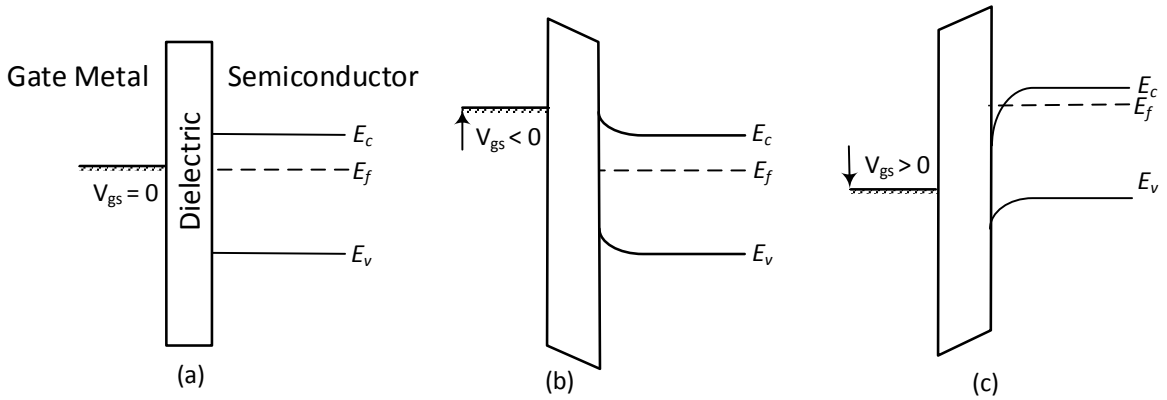


Figure 1.5 Bias dependent operating conditions of TFTs. (Reproduced from [35])

Most of the reported AOS based TFTs with excellent device properties are n-type devices. P-type oxide TFTs have quite low performance. That is because the hopping hole transport paths in p-type amorphous oxides are made of the very localized and anisotropic Oxygen *2P* orbitals. Thus, hole mobility is comparatively very low as the holes will be trapped in the localized states[35]. However, recent reports on this topic demonstrated the future of Nickel oxide in the fabrication of better performing p-type oxide TFTs. A p-type device fabricated using pulsed laser deposition of lithium metal doped NiO channel layer was realized. The device demonstrated hole mobility of 1 cm^2/Vs, on/off ratio in the order of 10^3 with a sharp pinch-off and strong saturation behavior[37]. Another attempt reported the fabrication of p-type

functional oxide TFTs on rigid and flexible substrates using a low temperature processing method that combined solution combustion synthesis and deep-ultraviolet irradiation of Li:NiO. The rigid and flexible devices demonstrated improved field-effect mobility of 1.69 and 1.41 cm^2/Vs, I_{on}/I_{off} ~10^7 and 10^5, and subthreshold swing of 0.21 and 0.54 *V/dec,* respectively[38].

Speaking of OTFTs, classification of these devices as n or p-type is made based on which type of majority carriers (electrons or holes) get injected from the source into the channel. According to Y. Xu, since the majority of metals used for source/drain electrodes have a work function higher than that of the organic semiconducting active layer, hole injection from the source to the HOMO band of the OSC is easier in OTFTs[18]. Thus, previously reported devices are mainly of p-type. Recently, organic thin film transistors with n-type functionally are reported using a channel layer made of materials from the Imide-Functionalized Thiazole-Based polymer semiconductors group. The devices demonstrated good transistor behavior with 1.61 cm^2/Vs, and I_{on}/I_{off} ratio of 10^7–10^8[39]. A Bithiophene imide (BTI) polymer based TFT reported by another group also shows n-type transistor functionality with 3.0 cm^2/Vs carrier mobility which is remarkable compared to the values that have been achieved so far in polymer OSC based devices[40].

■ Applications of AOS and Organic TFTs

The birth of amorphous oxide and organic semiconducting materials pave the way to the new era of electronics[41]. And, TFT devices with AOS and organic channel layer are finding applications in diverse areas of technologies(Figure *1.6*)[42][43].

■ ▸ Display technologies

Amorphous oxide-based TFT devices deposited on flexible substrates are promising candidates for backplane circuits in bendable or large area active matrix displays. Various active matrix liquid crystal (AMLCDs) and organic light emitting diode (AMOLED) displays driven with amorphous oxide, and organic TFT devices have been reported so far.

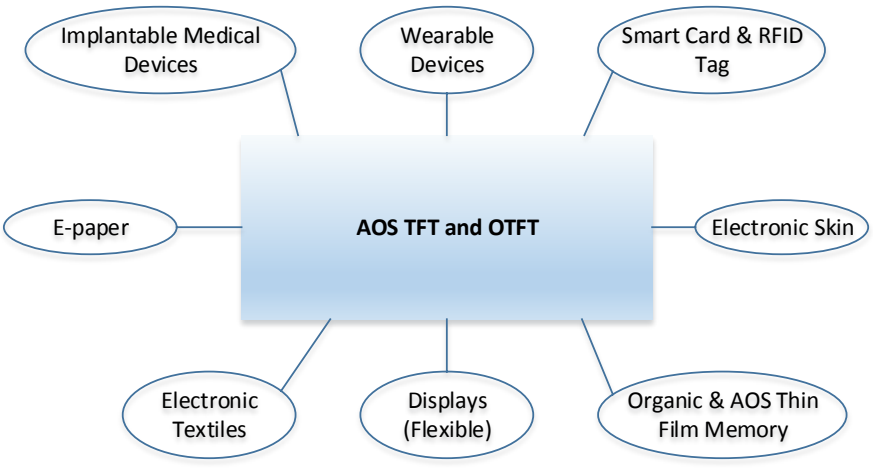


Figure 1.6 Application areas of (a) AOS and (b) Organic TFT device technologies. (Reproduced from[42] and [43]).

A flexible AMOLED color panel which can display static and motion pictures both in the flat and curved states was introduced by Park et al. in 2009. The screen has 6.5 in size and bendable approximately up to 2 cm of curvature. Each of its pixels is driven by a circuit of one storage capacitance and two a-IGZO TFTs fabricated on a PI substrate. The TFTs have electrical characteristics of a remarkable field-effect mobility of 15.1cm^2/Vs, 0.25V/decade subthreshold slope, and 0.9 V threshold voltage[44].

The role of organic TFTs in display technology demonstrated in different works as well. For instance, Mizukami *et al.* reported a 3.2-*in* flexible organic light-emitting diodes display (OLEDs) with a resolution of 50 PPI. The device has a backplane drive circuit composed of 5 *μm* gate length OTFTs that exhibit 1.2 cm^2/(Vs) field effect mobility. It is capable of displaying color videos with 125 cd/m^2 maximum luminance with white light emission while being bent[45]. These examples and other reports (not included here) are indicative of the potential that AOS and organic TFTs deposited on suitable flexible substrates have in the fabrication of high resolution AMLCDs and AMOLEDs with unique features[46]–[48].

■ ▸ Flexible Circuits

The high level of integration required to develop integrated circuits such as transponder chip, RFID, and scan drivers have restricted TFT technologies to monotype devices[42]. However, the effort to realize flexible integrated circuits continues and some success stories are recently appearing in the literature.

Kim *et al.* fabricated an operational amplifier (op-amp) from solution-processed n-type a-IGZO TFTs on a glass substrate. The op-amp has remarkable electrical properties of 24.6 dB total gain, a cutoff frequency of 0.47 kHz, and a 2.0 kHz unity-gain frequency of at ±15 V supply voltage. They further demonstrated a pulse width modulation (PWM) controller constructed from the proposed a-IGZO op-amp[49]. Another group reported a dynamic logic circuit using a-IGZO TFTs wherein the temporary storage of charge in the parasitic capacitances of the soft nodes governs the operation of the logic circuits. They fabricated n-type a-IGZO based dynamic inverter as well as NAND circuits, and then studied power and circuit area issues by comparing the dynamic logic circuits to the static counterparts fabricated using the same technology. A reduced circuit area tailored with less steady-state current consumption, and a broad output voltage range was able to be achieved with the proposed circuits-all are beneficial for VLSI systems[50].

Similarly, OTFTs have been used to build flexible integrated circuits. Ogier *et al.* reported a 5-stage ring oscillator circuits built from small molecule OTFTs fabricated on glass substrates. The OTFTs are composed of small-molecule and high-k binder polymer that enable the formation of thin, uniform films by spin-coating to achieve contact resistance value lower than 300 Ohm-cm. That together with the low dielectric capacitance enhance the charge injection, and thereby, increase the logic operation speed. The proposed circuit can operate at a frequency as high as 1.08 MHz with a 93 ns stage delay[51].

■ ▸ **Flexible Sensors and memories**

Other emerging applications of TFT devices include the development of flexible sensors and memories. PH sensors that consist of a-IGZO TFT are recently reported[52][53]. Due to the capability to fabricate large surface area and flexible AOS and organic TFT devices, they get considerable attention in the development of sensors for wearable electronics and electronic skin applications as well[54]. Furthermore, static random-access memories (SRAM) with a pretty small area and short writing times (for high and low writing states) are fabricated using these devices as reported in [55] and [56].

1.3 Wide bandgap semiconductors

Wide bandgap (WBG) semiconductors are the other class of materials that caused explosive revolution in the semiconductor industry. They are promising candidates to substitute Silicon in device applications for high power micro to mm meter wave operations[57]. Often the term "wide bandgap" refers to materials that have higher energy bandgap than that of Si. From Table 1.1, we can see that SiC and the III-V semiconductors (for example GaN) have superior intrinsic features such as high electron mobility and saturation velocity, large band gap, elevated breakdown electric field, and lower dielectric constant.

Materials with such exceptional attributes, improved durability, and better reliability have brought about remarkable advances in power electronics, producing devices that are smaller, faster, and more efficient than Si-based counterparts. SiC-based MOSFETs with low inter-electrode capacitances, fast switching frequencies, and the ability to withstand higher operating voltage and temperature appeared to facilitate the development of technologies such as hybrid electric vehicles, and renewable energy generation and storage systems[58]. WBG devices also cause significant improvements in efficiency and gain of existing applications. According to Yole development research, it is estimated that a 10% increase (85% to 95%) in DC-to-DC conversion efficiency, 5% rise in AC-to-DC conversion efficiency (85% to 90%), and 3% enhancement in the efficiency of DC-to-AC conversion (96% to 99%) can be achieved by substituting Silicon with SiC or GaN[59].

Table 1.1 List of Wide bandgap Materials and their physical properties[60]

Properties	Materials				
	Si	4H-SiC	GaAs	InP	GaN
Energy band gap (eV)	1.1	3.26	1.4	1.34	3.4
Breakdown Electric field (MV/cm)	0.3	2.0	0.4	0.5	3.3
Dielectric Constant	11.8	10	12.8	10	9.0
Saturation velocity (10^7 cm/s)	1.0	2.0	2.0	0.9	2.5
Thermal conductivity (W/cm.K)	1.5	4.5	0.5	0.68	1.3
Electron Mobility (cm^2/Vs)	1350	720	8500	5400	900

Early research on GaN explored its optical properties and its application in the optoelectronics industry. Due to the direct transition and high band gap, GaN showed superior performance in the production of energy-saving, durable, long-life substitutes for incandescent bulbs. Moreover, GaN is an environmental friendly alternative to mercury in the production of light emitting diodes (LEDs) and laser diodes (LDs)[61].

WBG materials are also a natural fit for RF electronics. Although the extensive research conducted on III-Nitrides revealed the suitability of intrinsic material properties of GaN for the design of power amplifies for high frequency operation, Gallium-Arsenide (GaAs) HEMTs took the leading position in this area at first. Because practical GaN HEMT amplifiers were not feasible for fabrication as there was no substrate material with high thermal conductivity to alleviate the critical issue of heat dissipation in such applications. AlGaN/GaN HEMTs started to receive tremendous attention in the community following the successful manufacturing a 4H-SiC substrate material reproducibly, which is highly conductive to heat. Substantial research has been conducted afterwards, and significant advancements have been achieved in the fabrication of devices for the design of RF amplifiers with remarkable electrical performance and capability to withstand hostile operating conditions.

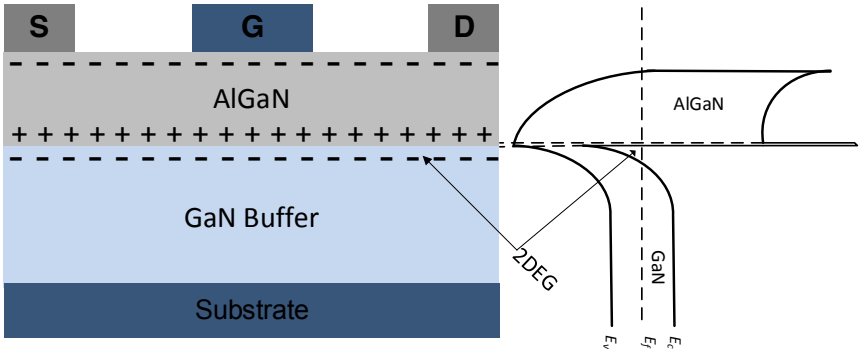
The increasing need for devices with high power handling capability and improved operating speed prompt further research for materials with enhanced properties than that of GaN and SiC for device applications. Recently, Ultra-wide bandgap (UWB) materials such as diamond, BN, high Al-AlGaN, and Ga_2O_3 are under extensive investigation, and Ga_2O_3 high-power transistors start to appear with promising future for next-generation power, and RF electronics. However, the study of these material systems is still in its infancy, and further research is required to address the existing challenges on growth maturity, thermal limits, cost, and reliability of the emerging devices[62]–[64].

1.4 GaN-based High Electron Mobility Transistors

■ AlGaN/GaN HEMTs structure

The basic structure of a HEMT device, in general, is constituted of different semiconductor layers (the substrate, buffer layer, and barrier layer) and three terminal electrodes, as illustrated in Figure 1.7[65]. 1) The substrate is the material onto which the HEMT epitaxy is grown. GaN HEMTs epitaxy is commonly grown on non-native materials that have high thermal conductivity such as SiC that facilitate proper dissipation of the excess heat generated during device operation. 2) The buffer layer is a thick and narrow bandgap III-V material which in the case of GaN HEMTs is a highly resistive GaN. The high resistance is vital for proper saturation of drain-source current, a complete channel pinch-off, low loss at high frequencies, and low cross-talk between adjacent devices in integrated circuits. 3) The barrier layer is a thin ternary alloy of the III-V compound semiconductor used as the buffer layer (AlGaN alloy for GaN HEMTs) and has a wider bandgap. It is the critical layer of the device where the electrons for

conduction are originating from, and its properties are mainly determined by the ternary metal composition (the Al amount in case of AlGaN barrier layer).



(a) (b)

Figure 1.7 Typical GaN HEMT (a) schematics (b) band diagram. (Reproduced from[65])

In addition to the three fundamental layers, a HEMT may include a cap layer grown on top of the structure for preventing the epitaxial surface from oxidation as well as for forming ohmic contacts of low resistance on the heterostructures. Depending on the type of substrate material used and the adopted growth technique, a nucleation material may also be needed in between the barrier and buffer layers for controlling the lattice mismatch (not shown in the Figure *1.7*). The gate electrode is HEMTs a Schottky contact whereas the source/drain electrodes form ohmic contacts and all have similar functionality as in any other FET devices[65].

■ AlGaN/GaN HEMTs Operating principle

In GaN HEMTs, a conduction band notch appears at the heterojunction interface between the AlGaN and GaN layers due to the dissimilarity in the crystal structure of the two materials. That creates a triangular quantum well at the interface. Electrons migrating towards the interface will then be confined in the well to form the so-called two-dimensional electron gas (2DEG) that has high electron concentration in the order of $10^{13} cm^{-2}$, which is the key feature of the device. As the 2DEG electrons are spatially isolated, they exhibit high mobility and saturation velocity.

The Schottky gate terminal controls the electron density within the 2DEG by modulating the potential distribution in the heterostructure below the contact. As electrons are present in the quantum well for conduction with no applied bias to the gate, the device is a normally ON device. That means a negative gate bias is required to toggle the device to the OFF state. Such devices are referred to as depletion-mode (D-mode) FETs. The channel can be depleted of mobile charge carriers and stop conducting current through the application of a substantial negative gate biasing. Conventional AlGaN/GaN HEMTs are D-mode transistors[65].

■ Applications of WBG based devices

For their outstanding material properties, WBGs have become propitious in various areas of applications (Figure *1.8*). Power electronics is among the primary domains, wherein these semiconductors are prevailing-enabling devices to sustain high voltage operation in tandem with kHz to MHz switching frequencies for increased system efficiency. As SiC comes with compelling merits over Si, it has been proven to be efficient for high-power density applications. SiC power diodes and MOSFETs have been evolving and currently are viable replacements for Si-based power semiconductors in development of renewable energy power sources such as solar panels, modular multilevel converters (MMC), micro-grids, power inverters, space applications, and resonant converters[66][67]. Similarly, GaN devices have become primary candidates in applications such as DC/AC convertors, power switches, power inverters, and RF amplifiers.

The rising concern of greenhouse gasses emission has brought about the use of electricity-based technologies in different aspects of vehicles as an alternative solution. The role of WBG materials in these technologies is indispensable. T. Kachi predicted that the emerging GaN technologies, especially the commercialization of GaN on Si devices, will increase the interest of adopting GaN power devices in the automotive industry. They also discussed the available challenges to use such technologies in electric vehicles (EV) and fuel cell vehicles (FCV)[68]. Similarly, Longobardi *et al.* made a detailed analysis of the prospect of GaN-based technologies in electric automobiles and acclaim both vertical and lateral GaN transistors as future central components of the power modules in electric vehicles[69].

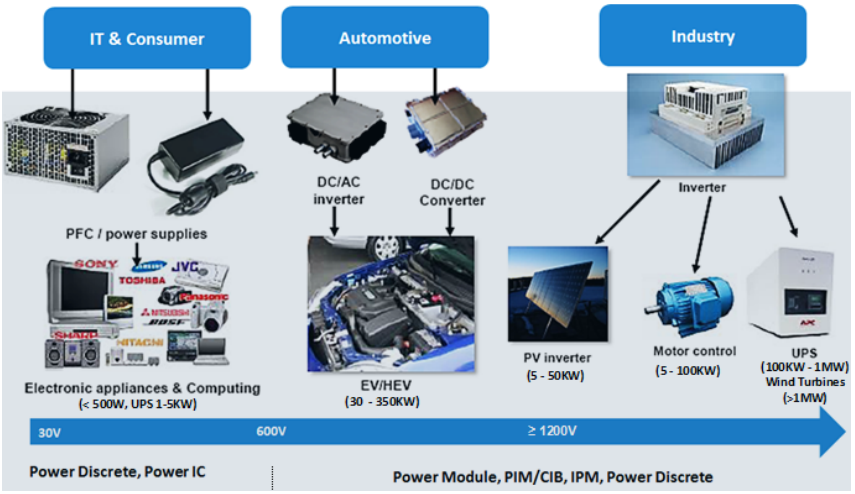


Figure 1.8 The diverse application of GaN and SiC. (Adopted From [70])

Different research groups are demonstrating innovative ways of exploiting GaN HEMTs for mm-wave and THz wave technologies as well. Recently AlGaN/GaN device array combined with optimized metallic metasurface was used to build modulators for amplitude and phase modulation of terahertz waves. With controlling the density of charge carriers in the 2DEG HEMT, it is possible to command the conversion between the two modes of the metamaterial surface. A 93% modulation depth with an associated speed of 3GHz, and a phase shift degree of 137 at approximately 0.35 THz with applied controlling potential of 0-8 V was achieved[71].

In [72], Polli *et al*. also proposed a GaN HEMT based Single-Chip Front-End (SCFE). The SCFE is capable of operating in C-band (from 5.25 GHz to 5.57 GHz) and integrates switching, low-noise and high-power amplification functionalities over 7×7 mm^2 area chip. It demonstrates a good performance of 43% power added efficiency (PAE) and 47.2 dBm output power at 3.5 dB compression in the Tx mode, and a noise figure <1.94 dB and gain 38.5 dB in Receive (Rx) mode.

Ayad *et al.* reported a broadband (low-cost plastic packaged) 5G High Power Frond-End (HPFE) amplifier that has a transmit and receive paths developed using mixed technologies of a 150nm Gallium Nitride on Silicon Carbide (AlGaN/GaN on SiC) and 150nm Gallium Arsenide (GaAs). The HPFE can operate within the 24-31GHz bandwidth. Continuous Wave (CW) measurement records indicate a 2W (33.5dBm) maximum output power ($P_{OUT,Tx}$) with 25% drain efficiency (DE), 24% power added efficiency (PAE), and 36dB of insertion gain ($G_{I,Tx}$) in the transmit path. On the receiver path (Rx), the measured performance reads a maximum output power ($P_{OUT,Rx}$) of 30mW (15.5dBm), 3.6dB average Noise Figure (NF) with a related 20dB insertion gain ($G_{I,Rx}$) from 24 to 31 GHz frequency range. The amplifier exhibits excellent linearity performance on the level equivalent to other HPFEs built using only GaAs amplifiers. Moreover, the mixed technology approach creates better balance between the integration, electrical performances, and fabrication cost[73].

The potential of GaN HEMs in satellite and radar communications has been explored in many works. For instance, S. Kim *et al.* reported a Ku-band 50 W internally-matched power amplifier designed using asymmetrically combined AlGaN/GaN HEMT transistor cells. The GaN HEMT device is grown on SiC substrate with 800 µm × 4800 µm size and a gate length of a 0.25-µm. It operates up to 18 GHz and has 70 W saturated output power capability at the reference plane of its drain pad. The asymmetric power combining in the amplifier design is achieved by applying a slit pattern, oblique wire bonding, and an asymmetric T-junction, for balancing the amplitude and phase of the combined signals at the transistor cell combining position. Thin films processed on titanate and alumina substrates are used in the input and output matching circuits, respectively. Pulsed measurement with a 330 µs pulse period and 6% duty cycle has been conducted. A maximum saturated output power of 57 to 66 W, 40.3 to 46.7% drain efficiency, and 5.3 to 6.0 dB power gain at power saturation were obtained in 16.2 to 16.8 GHz frequency range[74].

The sample application directed works presented here are indicative of the immense role of the AlGaN/GaN device in future communication and power electronics technologies.

1.5 Thesis synopsis

The work presented herein targets characterization and compact physics-based modeling of Flicker noise in amorphous metal oxide and organic TFT and piezoelectric effect in GaN-based HEMT devices. The thesis is organized into chapters as follows.

- **Chapter 2:** discusses parameter extraction and physics-based compact modeling of amorphous TFT devices. The Universal Model Parameter Extraction Method (UMEM), subgap density of states extraction in amorphous TFTs, and the three major theories of low-frequency noise in classical MOSFETs-that are indispensable to *I-V* characteristics modeling, and to identify the conduction mechanism and the origin of Flicker noise in ESL a-IGZO devices, respectively-are explained. Analysis of *I-V* characteristics and 1/f noise experimental data obtained at 298 K, 315 K, and 333 K is carried out to investigate the conduction process and origination of LFN in the targeted devices at different operating temperatures, and the results are discussed. Model validation is presented through comparison to experimental data.
- **Chapter 3:** presents low-frequency noise characterization of organic polymer-based TFT devices. Device fabrication is summarized first. Based on the Flicker noise theories revised in chapter 2, the analysis of noise measurement data obtained at room temperature is carried out and the outcomes regarding the physical origin of 1/f noise in the considered OTFT devices are presented next. The quality of the gate dielectric/channel interface and the effect of contact resistances in device noise performance are also explored.
- **Chapter 4:** focuses on piezoelectric effect modeling in AlGaN/GaN HEMTs. With the understanding of the origin of the 2DEG in GaN HEMTs, Schottky barrier height and threshold voltage models for HET devices of different structures are derived. A quick primer on the charge-based GaN HEMT model previously developed by our group and the integration of the V_{th} models in it is presented. Finally, proposed models are verified by simulation of DC characteristics of various GaN HEMT devices with different structural and geometrical features, and comparison with the corresponding measurement data.
- **Chapter 5:** summarizes the key results of the work presented in this thesis and proposed some future works.

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Part One

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2. Flicker Noise Characterization and Modeling of Amorphous InGaZnO Devices

Noise is defined as the consequence of fluctuations of microscopic variables around their average values due to the random variation in the physical processes that govern the functioning of the system of interest[1]. Often, it needs to be avoided to the possible level as it sets a limit on signal detection and processing without any loss of valuable information (as in the case with communication systems). However, it can also be used to good advantage-e.g., to gain insight into the properties of that particular system under study. Since noise origination in semiconductor devices is from the physical process that makes a device possible, the study of it enables increased understanding of the device physics[2]. In this regard, 1/f noise is a versatile tool to scrutinize causes of device degradation, assess interface quality, evaluate defects/trap states, etcetera in field effect transistors[3]–[6].

Many works have been published in recent years on the topic of Flicker noise characterization of a-IGZO devices from different perspectives[7]–[16]. Cho *et al.* studied the effect of different gate dielectric materials (Al_2O_3 and Al_2O_3 /a-SiNx) on the noise performance of a-IGZO TFT devices[8]. They reported that the Flicker noise originating from the channel is high in devices with the Al_2O_3 gate dielectric which is due to excessive electron-phonon scattering, while contract resistances in devices with Al_2O_3 /a-SiNx dielectric have a significant contribution to the noise level at high drain currents. The influence of device annealing on the noise performance of a-IGZO TFTs have been explored. It was found out that 1/f noise in annealed devices is significantly reduced compared to the level in unannealed devices as reported by T. C. Fung *et al.*[9]. A comparative study of Active Over Metal (AOM) and Metal Over Active (MOA) a- IGZO TFTs presented by Andreas *et al.* reported that the AOM devices have superior performance for their high quality gate-oxide/interfaces and low interface trap density[10]. Many of these published works pinpointed the random variation of carrier mobility within the active layer as the origin of 1/f noise in the explored a-IGZO devices [8], [9][15]–[17]. Whereas, others concluded the dynamic carrier exchange between slow gate insulator traps and the channel layer near the interface as the dominant source of Flicker noise in their corresponding a-IGZO TFTs[11]–[14]. A few cases reported carrier number fluctuation (at low drain currents), and mobility fluctuation (at higher drain currents) interchangeably produce the measured 1/f noise depending on the operating regimes of the devices under study[7][10]. What are common to all these works is that the targeted a-IGZO devices have a thick semiconducting (≥ 50 *nm*) and devices with a very thin a-IGZO layer are seldom studied. Moreover, 1/f noise analysis to identify its physical origin were carried out using crystalline MOSFET *I-V* models[7][9][16][17].

Characterization and modeling of low- frequency noise (LFN) in a-IGZO TFT devices that have Etch Stop structure and a thin a-IGZO film (ESL a-IGZO) are presented in this chapter.

The model is derived based on a robust parameter extraction technique called Unified Model and Parameter Extraction Method (UMEM), developed for TFT device DC characteristics modeling, and unified flicker noise theory. The chapter is organized as follows. A review on the UMEM DC parameter extraction method and I-V characteristics modeling of TFT devices are covered first. Discussion on electronic noise, MOSFET Flicker noise theories, and modeling follows next. And, analysis of DC and LFN experimental data and simulation results are demonstrated followed by conclusions.

2.1 UMEM based DC modeling in AOS TFT

The UMEM based *I-V* modeling of TFTs involves developing models for different device operating regimes separately to bind them into a single continuous expression valid for all regimes of device operation. Hence, it is suitable for modeling the *I-V* characteristics of amorphous TFT devices wherein the relation of the drain current and applied gate voltage takes a different form from deep subthreshold to the above threshold regimes.

■ AOS TFT DC characteristics modeling

■ ▸ Above Threshold regime (V_{gs}>V_t)

For a TFT device, the above threshold drain current I_{ab} is given by[18]–[21]

$$I_{ab} = K\mu_{eff}\frac{(V_{gs}-V_t)}{1+KR\mu_{eff}(V_{gs}-V_t)}\left[\frac{V_{ds}\left[1+\lambda\left(|V_{ds}|-V_{Dse}\right)\right]}{\left[1+\left(\frac{V_{ds}}{V_{sat}}\right)^m\right]^{1/m}}\right] \tag{2.1}$$

where V_{gs} and V_{ds} are the gate and drain bias voltages respectively, $K=(W/L)\times C_i$, W is the device width and L is the length, C_i is the dielectric capacitance, R is the series resistance, and λ represents channel length modulation effect. μ_{eff} is the effective carrier mobility which varies with the gate voltage per the power law equation as[18][19]

$$\mu_{eff} = \frac{\mu_0(V_{gs}-V_t)^{\gamma_a}}{V_{aa}^{\gamma_a}}. \tag{2.2}$$

with μ_0 is a constant set to 1 m^2/Vs for dimensional purpose. V_t is the threshold voltage, V_{aa} and γ_a are model parameters that control the mobility dependence on the gate bias. These parameters are usually extracted from experimental *I-V* data based on the UMEM, but they can also be analytically computed as explained later in the discussion of the conduction mechanism

in TFTs. V_{sat} and V_{Dse} are the saturation voltage and the effective drain voltage-defined as[18][19]

$$V_{sat} = \alpha_s \left(V_{gs} - V_t \right)$$
$$V_{Dse} = V_{ds} \left[1 + \left| \frac{V_{ds}}{V_{sat}} \right|^m \right]^{-1/m} \quad (2.3)$$

Where m sets the transition point in the output characteristics from the linear to the saturation region at a specific gate voltage (i.e. the knee region), and α_s stands for the saturation parameter.

The effect of channel length modulation is accounted for in MOSFET and other TFT models by multiplying the drain current with $(1+\lambda V_{ds})$. However, this approach increases the differential conductance with drain-source bias while it should be the other way around (monotonically decreasing with increasing the drain to source bias). The $(1+\lambda (|V_{ds}|-V_{Dse}))$ term was introduced in (2.1) to address this problem as proposed by V. O. Turin *et al*[19][22].

■ ▸ **Subthreshold regime ($V_{gs}<V_t$)**

The subthreshold current expression in TFTs may take different forms depending on the prevailing conduction mechanisms in the considered range of biasing. For devices with densely localized states, deep tail state DOS control charge transport in the below threshold regime, and the current is defined by the reduced form of (2.1), wherein the flatband voltage V_{FB} replaced V_t[19]:

$$I_{sub} = K\mu_0 \frac{\left(V_{gs} - V_{FB} \right)^{1+\gamma_b}}{V_{bb}^{\gamma_b}} V_{Dse1} \quad (2.4)$$

where V_{Dse1} is defined by (2.3) with V_{sat} substituted by $\alpha_b(V_{gs}-V_{FB})$. The V_{bb} and γ_b are parameters that define the mobility-gate voltage dependence, and α_b is the saturation parameter in the subthreshold regime. Whereas, in the second subthreshold regime of operation (in the deep subthreshold regime), charge carrier diffusion is the principal means of current flow. Thus, the model described in (2.4) is no longer valid. The current has an exponential dependence on the applied gate bias via[19]

$$I_{dsub} = I_{sub} \exp\left(2.3 \frac{\left(V_{gs} - (V_{FB} + V_1) \right)}{S} \right). \quad (2.5)$$

Here, $V_{FB} + V_1$ is a point adjacent to the flatband voltage-that is, chosen for reasonable sewing of the two subthreshold current expressions and S is the subthreshold slope. The total subthreshold region current is then obtained by binding (2.4) and (2.5) using the tanh function as[18][19]

$$I_{subT} = \frac{|I_{dsub}|}{2}\left[1 - \tanh\left[(V_{gs} - (V_{FB} \quad V_1 +))Q_1\right]\right] + \frac{|I_{sub}|}{2}\left[1 + \tanh\left[(V_{gs} - (V_{FB} \quad V_1))Q_1\right]\right] \tag{2.6}$$

A similar use of the tanh function to sew the above threshold current defined in (2.1) with the total subthreshold current in (2.6) gives the continuous drain-current expression valid for all regions of operation[18][19]:

$$I_{DS} = \frac{|I_{subT}|}{2}\left[1 - \tanh\left[(V_{gs} - (V_t \quad V_0 +))Q_2\right]\right] + \frac{|I_{ab}|}{2}\left[1 + \tanh\left[(V_{gs} - (V_t \quad V_0))Q_2\right]\right] \tag{2.7}$$

While Q_1 and Q_2 are adjustable parameters of the weighted tanh function, V_0 and V_1 define the sewing points slightly above the threshold voltage ($V_t + V_0$) and the flatband voltage ($V_{FB} + V_1$), respectively, for a continuous transition of the drain current from one operating regime to another.

■ Universal Model Parameter Extraction Method (the UMEM)

According to Ortiz *et al*., for any semiconductor device, parameter extraction from *I-V* measurement data can be carried out using[23]:

- The small-signal conductance method which is sensitive to measurement errors, as they will be magnified during the derivation of current by voltage.
- External resistance inserted in series with the device in *I-V* measurement setup. The method requires further experimental work.
- Plots generated free of the series resistance influence through the application of complex algebraic manipulations to the experimental *I-V* data.
- Semi-log plot extrapolation of the *I-V* characteristics obtained in the linear regime. While being simple, this method can be less reliable for devices with high series resistance R. This is because the high R can cause a considerable shift in the linear behavior of the *I-V* characteristics.
- Integration of current with respect to the voltage, which significantly decreases the effect of errors generated during measurement.
- Direct vertical optimization of the parameters obtained from the I-V data based on minimizing the vertical quadratic error.

The UMEM is developed to satisfy the need for a reliable parameter extraction method to render the above AOS *I-V* model functional. It functions based on the integration of the *I-V* measurement data (the 5th method in the above list), and as a result, it is insensitive to the measurement errors. The basic building block of this method is an integral function $H(V_{gs})$ defined as[24][25]

$$H(V_{gs}) = \frac{\int_0^{V_{gs}} I_{ds}(x)dx}{I_{ds}(V_{gs})} \tag{2.8}$$

where I_{ds} represents the drain current. The $H(V_{gs})$ can be applied directly on the linear and subthreshold *I-V* experimental data to obtain simple analytical expressions from which model parameters can be easily extracted. To this purpose, we must have measurement data for the linear and saturation transfer, and output (obtained at different gate voltages) characteristic curves, and define the range of biasing conditions optimal for parameter extraction[25]. Before we proceed to the discussion of the extraction procedures, we declare the following terms for better clarity.

V_{dsl}**: -** drain voltage at which the linear transfer characteristic is obtained.

V_{dss}**: -** drain voltage at which the saturation transfer characteristic is obtained.

V_{dsmax}**: -** maximum drain voltage up to which the output characteristic is measured.

V_{gsmax}**: -** maximum gate voltage up to which the transfer curves are measured.

I_{dslinm}**: -** measured linear *I-V* characteristics

I_{dssatm}**: -** measured saturation *I-V* characteristics

I_2**: -** drain current measured at V_{dsmax} and V_{gsmax}

I_{dslmax}**: -** drain current obtained at V_{dsl} and $V_{gsmax.}$

Once we set all the requirements, we can evaluate the parameters (both physical and empirical parameters) defined in (2.1)-(2.5)-i.e., V_t, m, V_{aa}, γ_a, λ, and α_s for the above threshold regime, and V_{bb}, γ_b, S, V_{FB}, and α_b for the subthreshold regime current modeling. The process comprises the following series of steps[18]–[21], [25]–[29].

1) <u>Step 1 V_t and γ_a extraction</u>: - considering the linear regime condition ($V_{gs} > V_t$ and small $V_{ds} < (V_{gs} - V_t)$) and replacing μ_{eff} by (2.2), we can rewrite the expression given in (2.1) as[18]–[21]

$$I_{ab} = \frac{K(V_{gs} - V_t)^{1+\gamma_a} V_{ds}}{V_{aa}^{\gamma_a}}. \tag{2.9}$$

And, by integrating (2.9) based on(2.8), we obtain

$$H(V_{gs}) = \frac{1}{2+\gamma_a}\left(V_{gs} - V_t\right). \tag{2.10}$$

Similarly, integrating the I_{dslinm} yields a function which is linear within a certain V_{gs} range with a slope P_{lin} and an intercept C_{lin}. By equating that with the $H(V_{gs})$ in (2.10), it is possible to extract the threshold voltage V_t and the γ_a parameter separately as[18]–[21]

$$\begin{aligned} P_{lin}(V_{gs} + C_{lin}) &= \frac{1}{2+\gamma_a}\left(V_{gs} \quad V_t\right) \\ V_t &= \frac{-C_{lin}}{P_{lin}} \\ \gamma_a &= \frac{1}{P_{lin}} - 2. \end{aligned} \tag{2.11}$$

2) <u>Step 2 V_{aa} extraction</u>: - by substituting I_{dslinm} for I_{ab}, and using the γ_a parameter from step 1 in(2.9), we can generate the $(I_{dslinm})^{1/(1+\gamma_a)}$ and evaluate V_{aa} from its slope P_{lin1} as[18]–[21]

$$\begin{aligned} \left(I_{dslinm}\right)^{\frac{1}{1+\gamma_a}} &= \left(\frac{KV_{dsl}}{V_{aa}^{\gamma_a}}\right)^{\frac{1}{1+\gamma_a}}\left(V_{gs} - V_t\right) \\ P_{lin1} &= \left(\frac{KV_{dsl}}{V_{aa}^{\gamma_a}}\right)^{\frac{1}{1+\gamma_a}} \\ V_{aa} &= \left(\frac{KV_{dsl}}{P_{lin1}^{1+\gamma_a}}\right)^{\frac{1}{\gamma_a}}. \end{aligned} \tag{2.12}$$

One must ensure that the $H(V_{gs})$ evaluated from I_{dslinm} and the $(I_{dslinm})^{1/(1+\gamma_a)}$ are linear functions of the gate overdrive voltage (V_{gs}-V_t) within the defined V_{gs} range for accurate extraction of the mobility parameters in steps 1 and 2.

3) <u>Step 3 subthreshold mobility parameters extraction</u>: - at this step, the flatband voltage and subthreshold mobility parameters V_{FB}, γ_b, and V_{bb} are extracted from the subthreshold *I-V* experimental data. Applying the integral function to the subthreshold current expression in (2.4) gives[18]–[21]

$$H_{sub}(V_{gs}) = \frac{1}{2+\gamma_b}\left(V_{gs} - V_{FB}\right). \tag{2.13}$$

The $H_{sub}(V_{gs})$ is a linear function of (V_{gs}-V_{FB}) in a range of gate bias defined in the subthreshold regime. Thus, γ_b and V_{FB} can be calculated from the slope (P_{sub}) and intercept (C_{sub}), respectively, as per the expressions in (2.14). The calculations in step 2 are then repeated here on the subthreshold experimental data to extract V_{bb}.

4) Step 4 α_s parameter extraction: - in the saturation operating regime, $V_{ds}>>(V_{gs}-V_t)$. The above threshold drain current in (2.1) approximates (i.e. with μ_{eff} substituted by (2.2)) to the following simple expression[18]–[21]:

$$I_{ab}=\frac{K\alpha_s(V_{gs}-V_t)^{2+\gamma_a}}{V_{aa}^{\gamma_a}}. \tag{2.15}$$

Using the experimental data I_{dssatm}, in place of I_{ab} in the above equation and γ_a from step 1, we can derive a linear function of (V_{gs}-V_t) and obtain α_s from its slope P_{sat} as[18]–[21]

$$\begin{aligned}\left(I_{dssatm}\right)^{\frac{1}{2+\gamma_a}}&=\left(\frac{K\alpha_s}{V_{aa}^{\gamma_a}}\right)^{\frac{1}{2+\gamma_a}}\left(V_{gs}-V_t\right)\\ P_{sat}&=\left(\frac{K\alpha_s}{V_{aa}^{\gamma_a}}\right)^{\frac{1}{2+\gamma_a}}\\ \alpha_s&=\frac{\left(P_{sat}\right)^{2+\gamma_a}}{K}V_{aa}^{\gamma_a}.\end{aligned} \tag{2.16}$$

5) Step 5 series resistance (R) extraction: -extraction of the series source-drain resistance R is done from the maximum of linear regime current experimental data $I_{dslinmax}$. Since $V_{dsl}<(V_{gsmax}-V_t)$, one can adapt the above threshold drain current expression in (2.1) to this condition and rearrange it to solve for R as[25]

$$R=\frac{V_{dsl}}{I_{dsl\max}}-\frac{1}{K\mu_{eff}(V_{gsm\max}-V_t)}. \tag{2.17}$$

In cases when the above evaluation of the series resistance results in a negative value, it can be set to zero. This is valid as long as the effect of the drain-source resistance is insignificant in the device of interest.

6) Step 6 knee region parameter (m) extraction:- by setting the I_{ab} in (2.1) to I_{dsomax} (the measured output drain current at V_{gsmax} and $V_{dssatmax}$ where $V_{dssatmax}=\alpha_s(V_{gsmax}-V_t)$) and neglecting λ, we can formulate an expression to calculate the parameter m[18]–[21]:

$$m = \frac{\log(2)}{\log\left[K\mu_{eff}\frac{\left[\left(V_{gsmax}-V_t\right)\left(\frac{V_{dssatmax}}{I_{dsomax}}\right)\right]}{\left[1+\left[RK\mu_{eff}\left(V_{gsmax}-V_t\right)\right]\right]}\right]}. \quad (2.18)$$

7) ***Step 7 λ parameter extraction:-*** here, λ is extracted in the pinch-off region (i.e. at V_{gsmax} and V_{dsmax} bias points) by replacing the drain current in (2.1) to the maximum measured output current I_2[25]:

$$\lambda = \frac{\left(\frac{I_2}{V_{dsmax}^2}\right)}{\left(\frac{K\mu_{eff}(V_{gsmax}-V_t)}{1+RK\mu_{eff}(V_{gsmax}-V_t)}\right)\left(1+\left[\frac{V_{dsmax}}{V_{dsatmax}}\right]^m\right)^{\frac{1}{m}}} - \frac{1}{V_{dsmax}}. \quad (2.19)$$

Note that, the μ_{eff} used for the computation of the other parameters in steps 5 to 8 is determined using (2.2) at $V_{gs}=V_{gsmax}$.

The UMEM method has been applied to DC characteristics parameter extraction in different types of TFTs such as Silicon based amorphous TFTs (a-Si:H TFTs)[21], amorphous organic semiconductor devices (OTFTs)[20][25][27][28], nanocrystal TFTs[29], and amorphous metal oxide TFTs (AOS TFTs)[18][19].

2.2 Subgap DOS in AOS TFTs

The remarkable electrical properties and stability of AOS TFTs are highly dependent on the sub-band (mobility band) localized density of states. Thus, knowledge of the nature of these states is critical for rough understanding and further optimization of the properties of the devices[30]–[33]. In any n-type amorphous TFT, the localized mobility band DOS comprises exponentially distributed acceptor like tail and deep states and is written as[18][19]

$$g_A(E) = N_{ta}\exp\left(-\frac{E_C-E}{kT_1}\right) + N_{ga}\exp\left(-\frac{E_C-E}{kT_2}\right) \quad (2.20)$$

where E_C is the conduction band minimum, $N_{t/ga}$ are the density of tail/deep states when the above expression is extrapolated to $E=E_C$, respectively, T_1 and T_2 are the corresponding characteristic temperatures, and k is the Boltzmann constant.

In TFT devices, with an assumption that the free carriers are less in number compared to the localized charge in all operation regimes, it is possible to solve Poison's equation to derive analytical expressions for the electric field as well as the induced channel charge. And, by integrating the charge expression along the channel as done in a-Si:H, nanocrystalline TFTs, and organic TFTs, one can obtain the following formula for the subthreshold current[25] [29][34]:

$$I_{ds} = F(T,T_2)Kq\left(C_i^{\left(\frac{2T_2}{T}-2\right)}\right)\frac{T}{2T_2}\left((V_{gs}-V_{FB})^{\frac{2T_2}{T}}-(V_{gs}-V_{FB}-V_{ds})^{\frac{2T_2}{T}}\right) \tag{2.21}$$

where

$$F(T,T_2)=\left(\frac{\sin\left(\frac{\pi T}{T_2}\right)}{2\pi q g_{F0}k_b^2TT_2}\right)^{T_2/T}\left(\frac{k_bT}{(\varepsilon_s\varepsilon_0)^{\frac{T_2}{T}-1}}\right) \times\left(N_C\exp\left[-\frac{E_C-E_{F0}}{kT}\right]\right) \tag{2.22}$$

$$g_{F0}=N_{ga}\exp\left(-\frac{E_C-E_{F0}}{kT_2}\right). \tag{2.23}$$

Substituting (2.23) in (2.22) provides

$$F(T,T_2)=N_C\left(\frac{\sin\left(\frac{\pi T}{T_2}\right)}{2\pi qN_{ga}k_b^2TT_2}\right)^{T_2/T}\left(\frac{k_bT}{(\varepsilon_s\varepsilon_0)^{\frac{T_2}{T}-1}}\right) \tag{2.24}$$

where E_{F0} is the fermi level, q is the elementary charge, N_C is the density of states at the bottom of the conduction band, T is the device operating temperature, ε_s and ε_0 stand for semiconductor dielectric constant and free space permittivity respectively, and $k_b=k/q$. Indeed, with a few mathematics, the subthreshold current expression (2.21) can be simplified to the I_{sub} defined in (2.4) for $V_{ds} << V_{gs}–V_{FB}$ and the subthreshold mobility parameters can be computed as [21][25][29]

$$\gamma_b = 2\left(\frac{T_2}{T} - 1\right)$$
$$V_{bb} = \frac{1}{C_i}\left(\frac{1}{qF(T,T_2)}\right)^{\frac{1}{\gamma_b}}. \tag{2.25}$$

One can see from the above derivation that it is possible to evaluate the maximum deep DOS N_{ga} from the subthreshold mobility parameters obtained based on the UMEM method (***Step 3***) by using the expressions in (2.24) and (2.25)[25]:

$$N_{ga} = \left[q\left(V_{bb}C_i\right)^{\gamma_b}\left(\frac{N_c k_b T}{\left(\varepsilon_s\varepsilon_0\right)^{\frac{T_2}{T}-1}}\right)\right]^{\frac{T}{T_2}}\left(\frac{\sin\left(\frac{\pi T}{T_2}\right)}{2\pi q k_b^2 T T_2}\right). \tag{2.26}$$

The maximum tail states density N_{ta} can be extracted similarly from the above threshold mobility parameters. As discussed in the previous chapter, the subgap electronic structure dictates the means of charge transport, which strongly depends on the fabrication process and operating conditions of the device in question. Thus, unequivocal extraction of the localized DOS helps to understand the means of charge transport in a device from a specific technology at any given operating conditions. M. Estrada *et al.* discussed that in their study of the effect of temperature on the performance of ESL a-IGZO TFT devices[35]. They used the $N_{t/ga}$ values obtained from *I-V* experimental data to explain the decrease in drain current at high temperatures, observed in some of their samples, is associated with a temperature-driven change in conduction mechanism. The same approach is adopted here to investigate the charge transport in the targeted ESL a-IGZO devices (they are from a different technology than those studied in [35]) at different operating temperatures, as we will see later in the results section of the chapter.

2.3 Electronic noise and Power Spectral Density (PSD)

In semiconductor devices, perturbations inherent to the device physics give rise to the random motion of charge carriers. Such stochasticity of carriers' dynamics results in spontaneous fluctuations in the terminal (*I-V*) characteristics of the device around a fixed DC value, which is referred to as electronic noise. The "Hiss" sound heard in radio, the "flickering screen" on television, and the "Buzz" sound in the middle of a telephone conversation are the most common examples of electronic noise. Other fluctuations originated from the influence of external sources such as electrostatic and magnetic coupling effects, light, etc. can be avoided with proper use of shielding and filtering[36]. Hence, they are not classified under electronic noise and are not considered here.

In principle, electronic noise regarded as a stationary random process meaning its joint probability distribution does not depend on time. Integration of the measured current or voltage variations over time will provide a zero-average value, and no compelling information regarding noise can be obtained. Thus, noise analysis is usually carried out in the frequency domain employing the Fourier transform of the autocorrelation of the noise signal. For a continuous and quadratically integrable (finite energy) signal *f(t)*, the square of its continuous Fourier transform defines the signal spectral density as[37]

$$\psi(w) = \left| \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{+\infty} f(t) e^{-iwt} dt \right|^2 . \tag{2.27}$$

And, if the signal is considered random stationary process (sampled signal is not dependent on the sampled time), the Fourier transform of its autocorrelation function *R(t*) gives the power spectral density (PSD) *S(f)* which reads[37]:

$$S(f) = \int_{-\infty}^{+\infty} R(t) e^{-iw\tau} d\tau \tag{2.28}$$

The *S(f)* function contains valuable information regarding the power distribution of that signal over the frequency spectrum. Usually, the PSD is named after the type of signal it is measured as S_{Id}/S_{Vg} for current/voltage and has units of A^2Hz^{-1} /V^2Hz^{-1}, respectively.

■ Electronic noise in Semiconductor devices

A Field Effect Transistor (FET) is regarded as an interconnection of passive and active elements, and electronic noise can be generated by (1) the source, gate, and drain terminal resistances (2) the channel and (3) substrate resistances[38]. The most common types of noise in semiconductors are thermal noise, shot noise, generation-recombination noise, Flicker (1/f) noise, gate-induced noise, and random telegraph signal (RTS) noise.

■ ▸ Thermal noise

It is also referred to as Nyquist or Johnson noise and is originated from the Brownian motion of charge carriers in a conducting medium at equilibrium, regardless of any applied voltage. It has a white spectrum over a broad frequency range (its PSD is constant over the entire frequency spectrum). For a given electrical conductor with resistance R and operating temperature T, the thermal noise generated by thermal agitation of carriers within the material is represented by a voltage /current noise source in series/parallel with R, and its PSD is written as[6][37]

$$S_{VG} = 4kTR$$
$$S_{Id} = 4kTG_D \tag{2.29}$$

where $G_D=1/R$.

The thermal noise representation as a current noise sources in parallel with terminal resistances and the channel is a common practice in FET devices. Thus, the linear regime PSD takes the second form defined in(2.29) whereas in saturation operation, white noise has a PSD[37]

$$S_{Id} = 2CqI_{ds} \tag{2.30}$$

where C is a constant. Note that, since the channel conductance is inversely proportional to the drain bias, the maximum S_{Id} occurs at zero V_{ds} in FET devices.

■ ▸ **Generation-Recombination (GR) Noise**

Generation-recombination noise is typical for semiconductors and is the result of fluctuating free carrier density due to the random transition of carriers between states located in different energy bands. In FET devices, the GR noise is associated with the stochastic generation/recombination of carriers with the channel by traps acting as recombination centers [37]–[41].

■ ▸ **Shot Noise**

This noise pertains to the random transition of charge carriers across a potential barrier such as in pn-junction due to the discrete nature of the electric charge. The PSD of shot noise is proportional to the average current I crossing the potential barrier and the elementary charge q[6][42]:

$$S_{Id} = 2qI. \tag{2.31}$$

■ ▸ **Flicker (1/f) noise**

As its name indicates, Flicker noise has a spectrum inversely proportional to frequency as $1/f^{\gamma}$, where γ can take a value from 0.9 to 1.1. It is dominant at low frequency operation of devices. It sets the lower limit to signal detection in analog circuits, and deteriorate the noise margin of digital CMOS circuits. On the one hand, circuit and device design engineers need to keep the effect of Flicker noise to the minimum level so that the dynamic range and performance of their circuit can be improved. Whereas, on the other hand, they can use it as a diagnostic tool to understand the physics of their device of interest[6][38].

2.4 Theories of Flicker Noise Mechanism in MOSFETs

The physics-based origin of Flicker noise in semiconductor devices has long been debated. Devices from different manufacturers and technologies have been investigated to understand what physical processes give rise to this specific type of noise in MOSFETs. Published results related it to conductance fluctuations due to[38]:

1) Random variation of free carrier density (number fluctuation) near the gate-oxide/channel interface.
2) Carrier mobility fluctuations within the semiconductor.
3) Carrier number-correlated mobility fluctuation, which assumes the change in carrier density because of the trapping/release processes is accompanied by bulk mobility fluctuations because of remote Coulomb scattering.

A lot of efforts have been made to come up with a universal model to explain the Flicker noise experimental data obtained in FET devices. In the following paragraphs, the three widely used 1/f noise models proposed based on the theories presented above are discussed.

■ Carrier number (ΔN) fluctuation model

This model is developed based on McWhorter's 1/f noise theory that states Flicker noise in MOSFET devices is a surface phenomenon, and, it stems from the fluctuation in free carrier number due to the dynamic exchange of mobile charge carriers between the channel and slow gate-insulator traps located in the vicinity of the gate/channel interface[43]–[45]. According to this model, the current noise PSD is directly proportional to the trap density N_{st} uniformly distributed in the gate insulator-close to the interface with the channel, which is given by[44][45]

$$S_{Id} = \frac{k^*}{f^\gamma}\mu\left(\frac{1}{C_{ox}L^2}\right)\frac{I_{ds}V_{ds}}{\left(V_{gs}-V_t\right)}. \tag{2.32}$$

where f is the frequency, γ is the frequency exponent, and C_{ox} is the gate oxide capacitance. k^* is a coefficient that takes into account the tunneling of charge carriers into and out of the gate oxide traps near the interface that reads[44][45]

$$k^* = \left(\frac{q^2 k_b T N_{st}}{\ln\left(\tau_2 / \tau_1\right)}\right) \tag{2.33}$$

where τ_1 represent τ_2 the lower and upper boundaries time constants of the trapping-release process.

■ Hooge's mobility (Δμ) fluctuation model

Flicker noise, in this case, is considered to be a volume phenomenon arising from bulk mobility fluctuation introduced by changes in the phonon population[38]. According to Hooge's model, the expression for the normalized drain current noise PSD reads[46]–[48]

$$\frac{S_{Id}}{I_{ds}^2} = \frac{q\alpha_H}{WLf^\gamma}\int_0^L \frac{1}{Q_{ch}(x)}dx \tag{2.34}$$

where α_H is Hooge's empirical parameter and $Q_{ch}(x)$ is the free charge density at any point in the channel. At low V_{ds} operation (linear regime), the charge distribution along the channel is approximately constant. Therefore, the expression in (2.34) takes the form which is widely known in the compact modeling community as Hooge's empirical formula[46]–[48]

$$\frac{S_{Id}}{I_{ds}^2} = \frac{q\alpha_H}{WLQ_{ch}f^\gamma} \propto \frac{1}{I_{ds}}. \tag{2.35}$$

Q_{ch} represents the total free charge per unit area in the channel. When the transistor enters the non-linear operation (high V_{ds}) regime, the expression defined in (2.35) does not hold true as the charge is no longer uniform along the channel. As a result, redefining (2.34) gives[48]

$$\begin{aligned}\frac{S_{Id}}{I_{ds}^2} &= \frac{q\alpha_H}{WL^2f^\gamma}\int_0^L \frac{1}{Q_{ch}(x)}dx = \frac{q\alpha_H}{WL^2f^\gamma}\int_0^{V_{ds}} \frac{W\mu_{eff}}{I_{ds}}d\phi_c \\ &= \frac{q\alpha_H\mu_{eff}V_{ds}}{L^2f^\gamma I_{ds}}\end{aligned} \tag{2.36}$$

where ϕ_c is the channel potential, μ_{eff} is the average carrier mobility. At this point, one should note that the normalized PSD in (2.36) simplifies to (2.35) in the linear regime operation. Therefore, it is valid for all operating regimes. It is apparent from the above definitions that, the current noise PSD calculated based on Hooge's model is inversely proportional to the drain current in all regimes of device operation. And, if such relation between noise PSD and drain current is identified in the 1/f noise experimental data obtained in a given device, it shows that the measured Flicker noise is originating from mobility fluctuation in the channel.

■ Carrier Number-Correlated mobility (ΔN-Δμ) fluctuation model

In the classical carrier number fluctuation scheme, the dynamic capture/release of charge carriers by oxide traps leads to the fluctuation of the interfacial gate-oxide charge and concomitantly, causes the random variation in carrier number in the inversion layer. The charge trapping/de-trapping in the oxide layer can be regarded as a random change in fixed oxide

charge δQ_{ox} and can be defined using the flatband voltage as $\delta V_{FB}=(\delta Q_{ox}/WLC_{ox})$. Thus, we can subsequently define the random change in the drain current via[47]–[49]

$$\delta I_{ds} = -g_m \delta V_{FB} \tag{2.37}$$

where, g_m is the transconductance. With a more detailed analysis, it is possible to see that the change in total oxide charge density modulates the rate of remote Coulomb scattering of carries, which in turn causes a random change in carrier mobility within the inversion layer.

Considering this effect in the ΔN model leads to the so-called carrier number fluctuation-correlated mobility fluctuation (CNF/CMF) Flicker noise model with a second term added to the expression in (2.37) as[47]–[50]

$$\delta I_{ds} = -g_m \delta V_{FB} - \alpha I_{ds} \mu_{eff} \ \ Q_{st}. \tag{2.38}$$

where α is the scattering coefficient parameter. Thereby, the normalized current noise PSD is evaluated as[47]–[50]

$$\frac{S_{Id}}{I_{ds}^2} = \left(1 \pm \alpha C_{ox} \mu_{eff} \frac{I_{ds}}{g_m}\right)^2 \left(\frac{g_m}{I_{ds}}\right)^2 S_{vfb}. \tag{2.39}$$

The spectral density of the oxide interface charge depends in essence on the physical trapping mechanisms into the oxide. For a tunneling process, the trapping probability decreases exponentially with oxide depth x[48]. Thus, the bias independent flatband voltage noise PSD defined by the S_{vfb} term in (2.39) is written as[48][51][52]

$$S_{vfb} = \frac{q^2 N_{st} k_b T}{f^{\gamma} WLC_{ox}^2} \tag{2.40}$$

Equation (2.39) is valid for all operating regimes of the device under study- that is, from the subthreshold to saturation regimes. It should be noted that the sign of the scattering coefficient in the expression is determined by the condition whether the trap is neutral or charged when filled. The CNF/CMF model is useful to assess the quality of the gate-insulator/channel interface in FET devices. We can notice from the expression that a similarity in the trend of normalized PSD and squared transconductance ratio experimental data plotted against drain current is indicative of a CNF/CMF origination of 1/f noise.

2.5 Experimental Data analysis and Modeling Results

■ Device Fabrication

Various bottom gate top contact ESL a-IGZO TFT samples with schematics shown in Figure 2.1 have been employed for the electrical and low frequency noise characterization. The devices are fabricated by the TNO research center according to the 5μm design rules. A 200 *nm* thick gate dielectric was grown on top of the gate metal, which is deposited on a glass substrate. Then, a 12 nm a-IGZO semiconducting and a 100 nm thick ESL layers are deposited subsequently. The source and drain contacts are formed on top of the a-IGZO layer. The resulting devices have 15 to 50 μm gate lengths and a 100µm channel width. Both the DC and 1/f noise measurements are carried out using AdMOS Flicker measurement system, and the PTC MATHCAD tool is used for parameter extraction and modeling tasks.

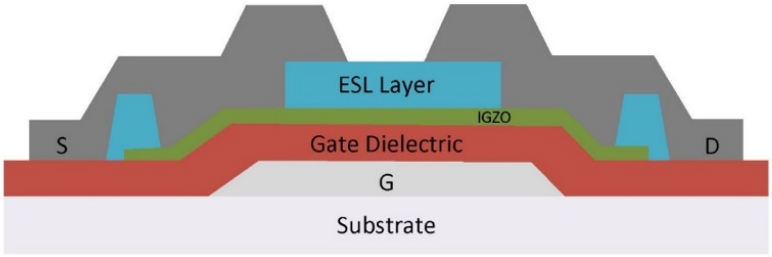

Figure 2.1 The schematics of ESL a-IGZO TFT

■ AdMOS Flicker noise measurement system

Developed by AdMOS GmbH (Advanced Modeling Solutions), this Flicker noise system provides state of the art solution for low frequency noise characterization of electronic devices (discrete or on wafer devices) of any structure. As shown in Figure 2.1, the system comprises a 3022/3023 control unit and a 3012 Filter Unit that should be put near to the device/system under study to lessen the noise originating from long cables. Software installed on a PC and linked to the measurement setup through the control unit allows defining the bias and other operating conditions for the device under test (DUT). The software enables to obtain not only the low frequency noise but also the DC characteristics of the DUT over a broad span of biasing [53].

AdMOS offers two types of systems: 1) the 3002A system where the control unit has a built-in Dynamic Signal Analyzer, 2) the 3001B system, which needs an external Dynamic Signal Analyzer to measure the noise Voltage. The former enables device characterization over an extended range of frequency, from 0.1 Hz to 10 MHz, with fast measurement time and higher resolution of the noise signals than the latter. Thus, we used the 3002A system for characterization of the a-IGZO TFT studied herein[53].

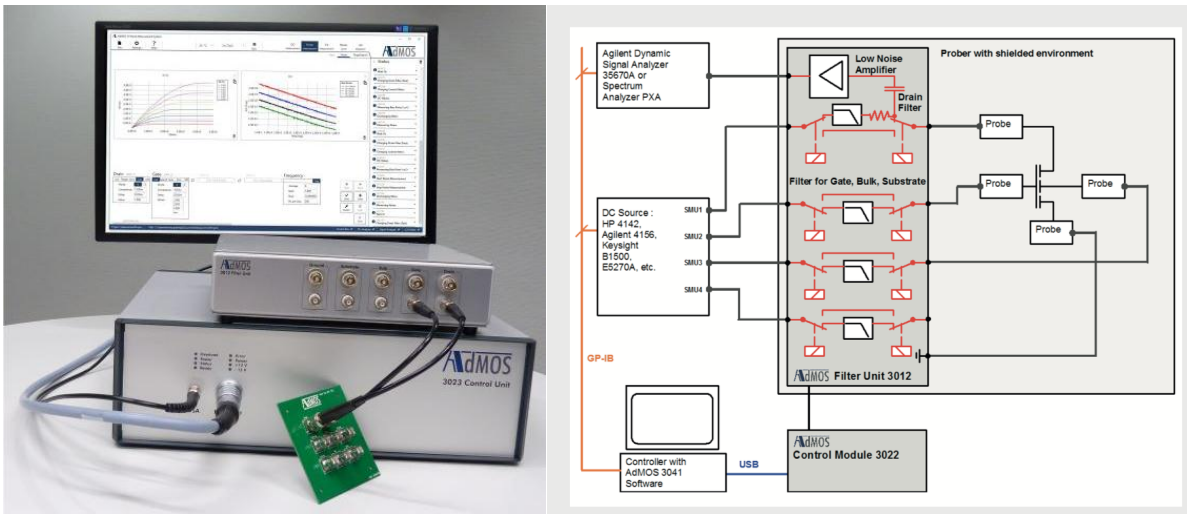

Figure 2.2 AdMOS 3002A Flicker Noise Measurement System[53]

Once the DC and 1/f noise data are measured, model parameter extraction, and Flicker noise mechanism analysis and modeling were carried out. The results are discussed in this section as follows.

■ Parameter extraction and DC characteristics modeling

Using the UMEM method, electrical parameters of all ESL a-IGZO devices in the sample are extracted and analyzed as summarized in Figure 2.3. Subsequently, two devices are selected for investigation of the physical effect of increased operating temperature on the I-V and 1/f noise properties of the devices. Details of extracted model parameters are given in Table 2.1.

Figure 2.4 and Figure 2.5 depict the variation of the modeled output and transfer characteristics along with the experimental data at different operating temperatures. An acceptable level of agreement is obtained between the calculated and measured *I-V* characteristics of all devices, in the range of V_{ds} and V_{gs} in question. In Table 2.1, the decreasing nature of γ_a value with increasing the channel length manifests that the long channel devices maintain a seemingly quasi-crystalline behavior. A similar conclusion can be reached focusing on the γ_a value (Table 2.1) approaching zero with the rise in operating temperature of the 20 μm and 50 μm devices.

A quasi-crystalline behavior at higher temperatures was observed in a few of a-IGZO TFT devices reported in the literature. And, it was described that the rise in operating temperature triggers a change in conduction mechanism from hoping to band like transport (percolation in the conduction band). Since the latter involves a considerable scattering of charge carriers, carrier mobility decreases-an effect which is typical to crystalline devices and worsens at elevated temperatures as more charge carriers will be thermally activated within the channel. Although the threshold voltage was found decreased with temperature in such cases, the mobility effect appeared to be dominant and dictated the variation of drain current with temperature in the corresponding a-IGZO devices[35][54].

On the contrary, high-temperature characterization of the ESL a-IGZO TFTs presented herein demonstrated the increase of mobility with temperature (Table 2.1). That shows Variable Range Hopping (VRH) is still the dominant means of charge transport within the explored temperature range, which is further verified by the increase in the band tail states N_{ta} with temperature as shown in Table 2.1. Thus, the quasi-crystalline behavior observed in the 20 μm and 50 μm devices at higher temperatures is not that much intense and carrier scattering is improbable even though an enormous number of carries are thermally activated. Additionally, strange behavior of increase in the threshold voltage with temperature is observed, and that might be related to the following reasons.

1) The acceptor-like deep sub-band states that govern charge transport in the below threshold regime may act electron traps. And, as the density of these states (N_{ga} values in Table 2.1.) found to be increasing with temperature, it is very likely that the rate of carrier trapping by these localized states exceeds that of thermal activation of carriers. This effect can lead to the trapping of a significant portion of the carriers generated within the channel. Therefore, more gate voltage will be required to commence charge transport, and in turn, result in the increase in the device V_t with temperature.

2) The positive shift of the I_{ds}-V_{gs} saturation curve in the subthreshold regime (Figure 2.4 and Figure 2.5) implies that the threshold voltage of the ESL a-IGZO devices increases in the saturation regime while the subthreshold slope remains constant. That might be attributed to the stress caused to the devices by the application of high drain voltage during earlier measurements. It is reasonable to infer that increasing the operating temperature of the devices adds to the stress and increase the change in V_T with temperature.

3) Finally, but less likely, in such device structures, the ESL layer usually forms a low-quality interface with the channel material compared to the gate dielectric. Thus, traps present in the ESL material may capture more carriers at higher temperatures and enforce the increase in threshold voltage of the devices.

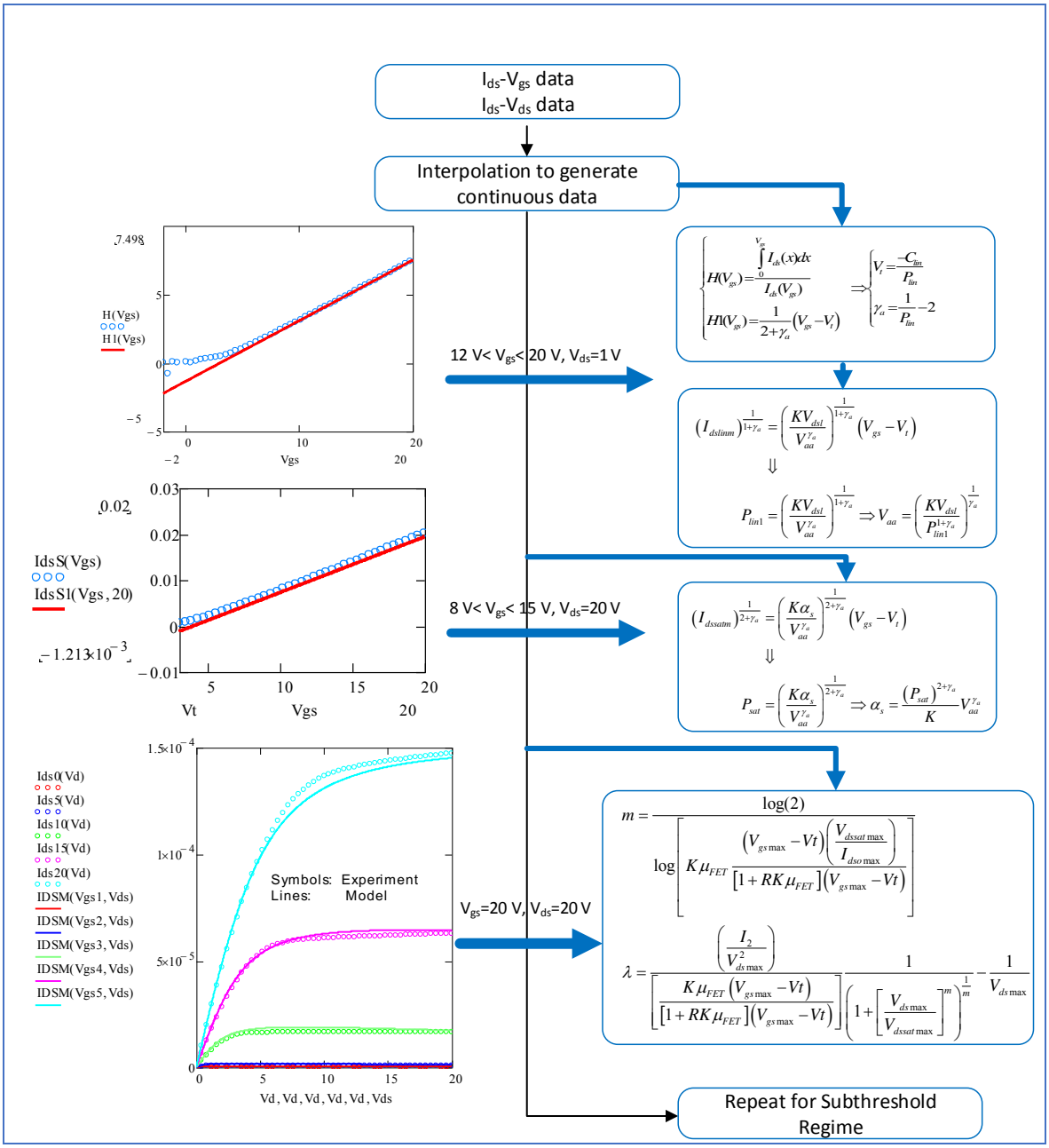

Figure 2.3 UMEM based parameter extraction summary

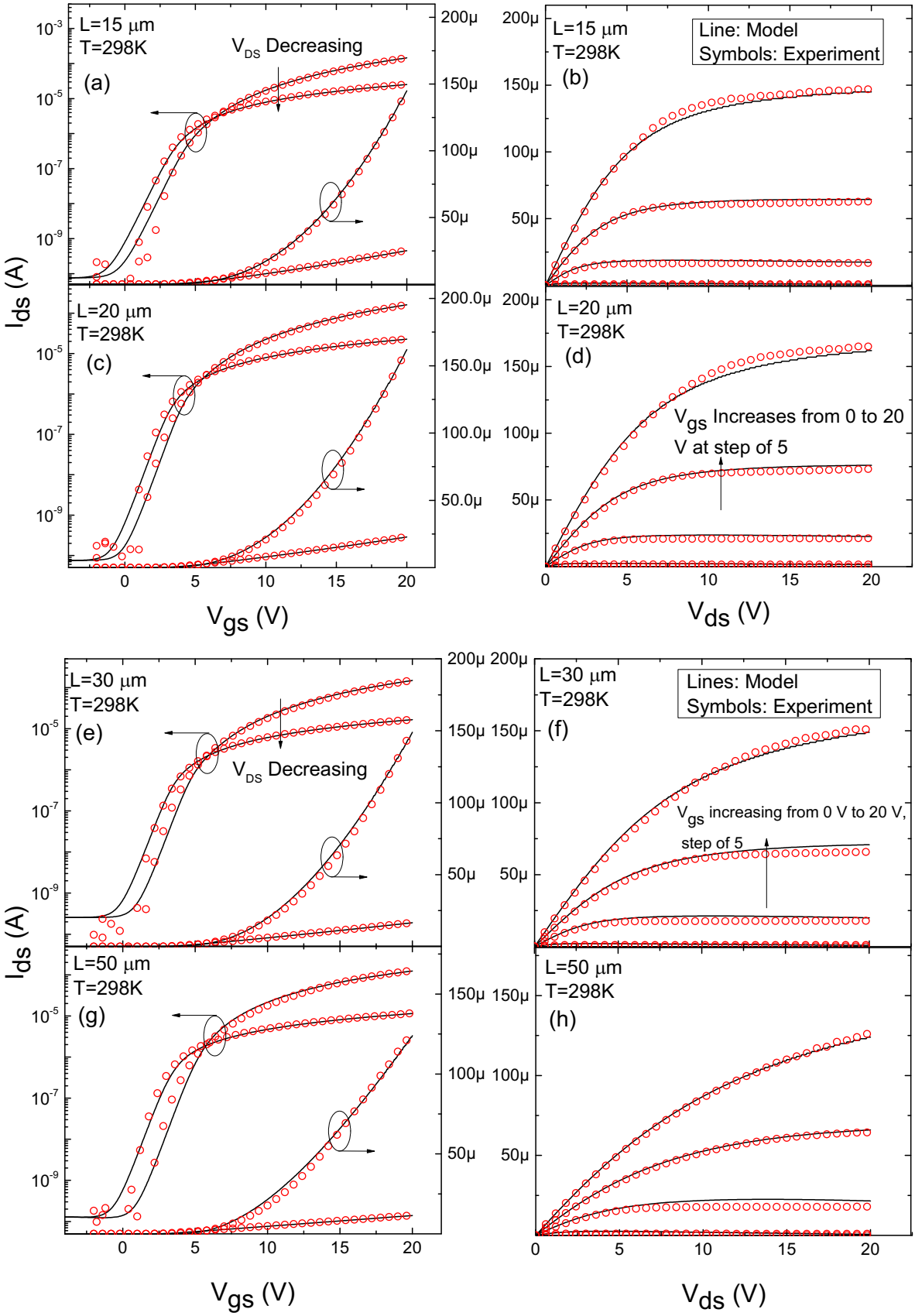

Figure 2.4 Modeled and experimental DC characteristics comparison for $15\times100\mu m^2$, $20\times100\mu m^2$, $30\times100\mu m^2$, and $50\times100\mu m^2$ devices at 298 K temperature. For the transfer characteristics, the drain voltages are V_{ds}=1 V and 20 V.

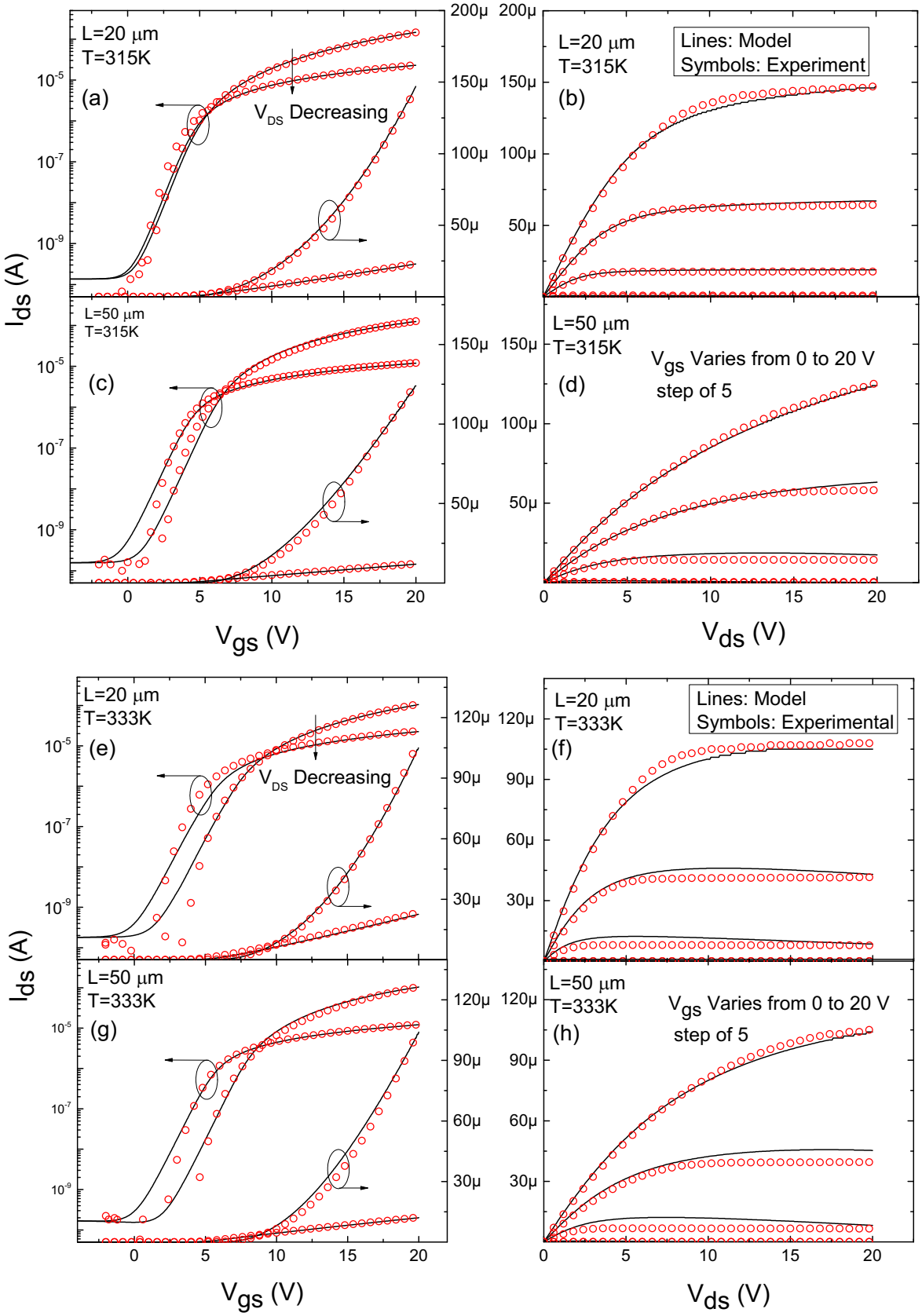

Figure 2.5 Modeled and experimental DC characteristics comparison for 20 × 100μm^2 and 50×100μm^2 devices at 315 K and 333 K operating temperatures. For the transfer characteristics, the drain voltages are V_{ds}=1 V and 20 V.

The increase in threshold voltage with temperature means the gate voltage overdrive (V_{gs}-V_t) decreases and consequently causes the observed drop in drain current at higher temperatures. It is apparent from that the variation of drain current with temperature in the targeted ESL a-IGZO devices is governed more by the dependence of the V_t on temperature than that of the mobility.

■ Analysis of Flicker noise mechanism in ESL a-IGZO TFTs

A typical plot of the measured low frequency noise power spectral density (PSD) over a range of frequencies for the 15μm device is shown in Figure 2.6. The noise exhibits a clear *1/f*$^{\gamma}$ frequency relation where the value γ is from 0.9 to 1.1 (see Table 2.1). Similar results are obtained in all devices in the sample (not shown here).

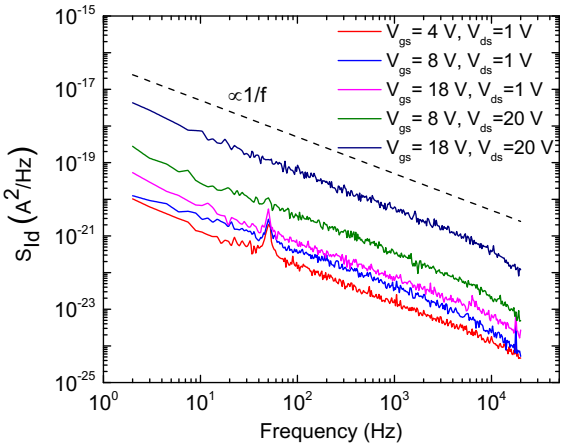

Figure 2.6 Typical plot of current noise PSD for 15×100μm^2 device at 298 K temperature.

The physical origination of the measured 1/f noise is investigated in Figure 2.7 (inset) by studying the variation of the normalized drain current noise PSD with drain current. Analysis of the experimental 1/f noise data was carried out based on the expressions defined in (2.35) and (2.39). The plot of the PSD (S_{Id}/I_{ds}^2) along with the extrapolated squared transconductance-drain current ratio ((g_m/I_{ds})^2) against drain current shows that the PSD varies similarly as the (g_m/I_{ds})^2 over a broad range of I_{ds} (which is also evident in the separate main plots of each term versus drain current). That indicates the measured LFN is a surface phenomenon, and the change in carrier number due to the capture/release process by slow gate dielectric traps account for the noise generated in the devices.

Some dispersions between the S_{Id}/I_{ds}^2 and (g_m/I_{ds})^2 can be seen in the plots at the high drain current regions which are more noticeable in short channel devices. Previous reports of Flicker noise studies in other types of TFT devices ascribed these deviations to noise contributions from correlated mobility fluctuation and series parasitic resistances.

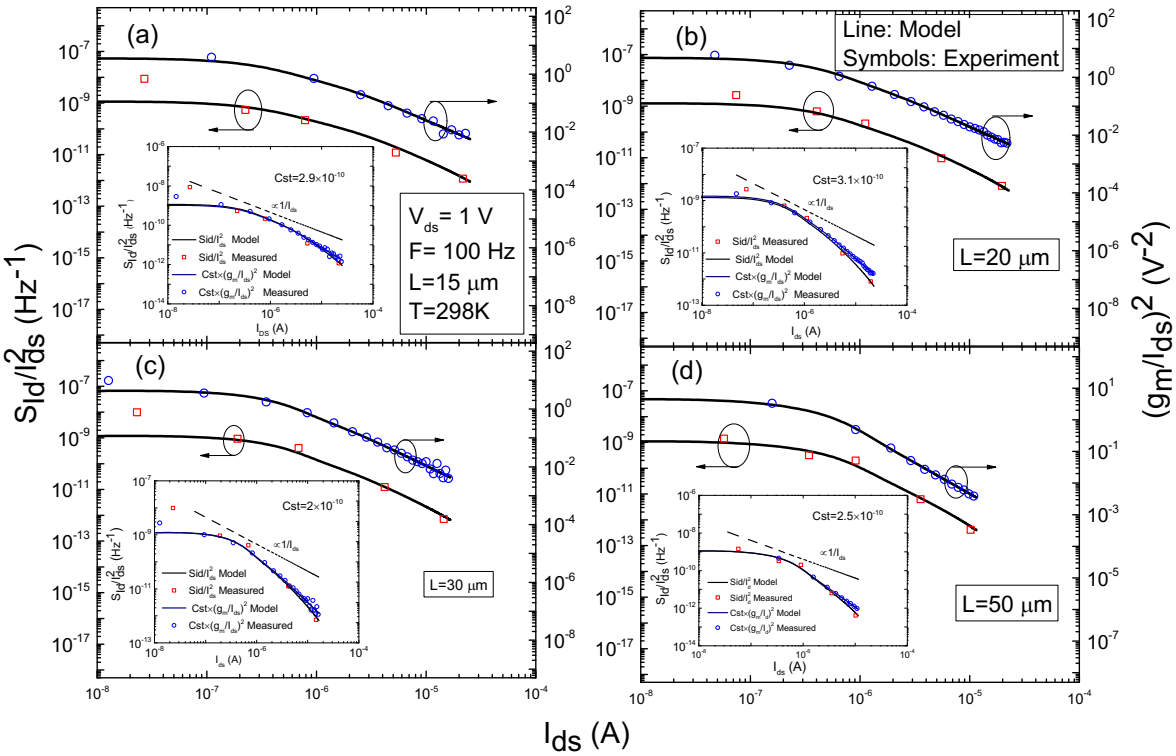

Figure 2.7 Measured and modeled (S_{Id}/I_{ds}^2) and $(g_m/I_{ds})^2$ comparison for $15\times100\mu m^2$ (a), $20\times100\mu m^2$ (b), $30\times100\mu m^2$(c), and $50\times100\mu m^2$(d) devices at 298 K temperature and 100 Hz frequency. Drain voltage V_{ds}=1 V.

Further investigations are carried out to understand what caused the deflections of the noise PSD from the $(g_m/I_{ds})^2$ in the ESL a-IGZO devices. The gate area scaled PSD plot against normalized current ($I_{ds}\times L/W$) results in curves parallel to each other as can be seen in Figure 2.8. That implies the measured LFN is originating from the channel, and the contact resistances have no contribution as no increase in noise is observed in the strong inversion regime. Thus, the observed swing of $(g_m/I_{ds})^2$ away from the S_{Id}/I_{ds}^2 is more likely related to the correlated mobility fluctuation due to remote Coulomb scattering of carriers.

Secondly, a direct comparison of the trap density evaluated from the experimental noise data N_{st} and the surface trap density extracted from the linear *I-V* characteristics measurement data N_{ss} (from the subthreshold slope in particular) have been made. It helps to pinpoint the nature of traps that give rise to the measured noise. As seen in Table 2.1, the calculated N_{st} values are found to be in the same order of magnitude with the N_{ss} in all devices. The result suggests it is highly likely that the same gate-oxide/channel interface traps involved in the LFN generation. And, it further confirms the contact resistances have no role in the LFN generated within the targeted devices.

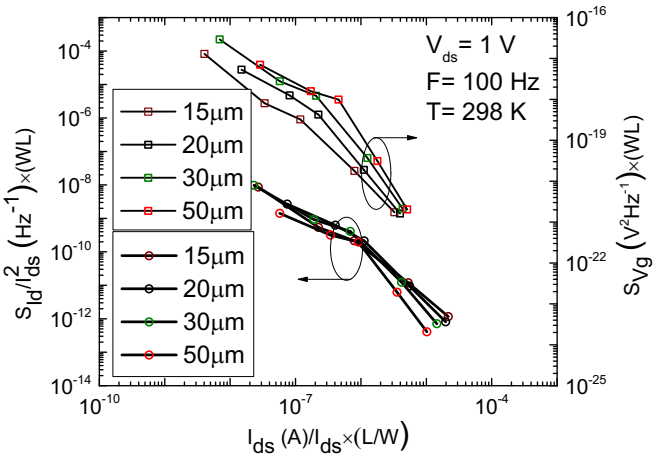

Figure 2.8 Plot of gate area scaled PSD ($S_{Id}/I_{ds}^2 \times WL$) and Voltage noise PSD ($S_{Vg} \times WL$) against normalized drain current ($I_{ds} \times L/W$) for $15 \times 100 \mu m^2$, $20 \times 100 \mu m^2$, $30 \times 100 \mu m^2$, and $50 \times 100 \mu m^2$ devices at 298 K temperature, 100 Hz frequency, and drain voltage V_{ds}=1 V.

■ Flicker Noise Modeling in ESL a-IGZO TFTs

Based on the analysis results, the UMEM DC characteristics and CNF/CMF (ΔN-$\Delta\mu$) Flicker noise modeling approaches are used to derive 1/f noise model for ESL a-IGZO devices valid for all operation regimes[55].

The Flicker model model-experimental data comparison over the frequency spectrum at room and higher operating temperatures are presented in Figure 2.9 and extracted noise model parameters are compiled in Table 2.1. The Coulomb scattering coefficient (α) is negative for all devices-indicating the interface traps responsible for the measured LFN will be charged when filled. Besides, the observed decrease in α with gate length implies the noise contribution from the correlated mobility fluctuation significantly reduced in long channel devices. The same is true for devices operating at higher temperatures as can been seen in the trend of α with temperature.

The presence of the ESL layer seems to enhance the effect of the interface traps, and wherefore the fluctuation in the number of mobile charge carriers at the interfaces, which is evident in the extracted values of trap density N_{st} presented in Table 2.1. An increasing channel length, on the other hand, means a higher fraction of the conduction takes place close to the interfaces since the fraction of conduction crossing the film from the source to the drain decreases, and the carrier trapping and de-trapping process is facilitated by that. Thus, more interfacial traps probably get activated, which is manifested in the observed N_{st} increase with device channel length. Device variability (since only one device is measured per channel length) and the effect of device channel length on the gate oxide capacitance can be another possible reason for the N_{st} difference. Finally, it is relevant to remark that the frequency exponent γ has values higher than unity at very low frequencies in a specific range of biasing, as seen in Figure 2.9 (*e*-*h*), that might be attributed to the thermal activation of numerous traps at high operating temperatures.

Table 2.1 Device geometry, Extracted DC and Noise model parameters

Parameters	Description	Devices							
		D1	D2			D3	D4		
		298K	298K	315K	333K	298K	298K	315K	333K
W (μm)	Width	100	100			100	100		
L(μm)	Length	15	20			30	50		
V_{th} (V)		3.0	2.6	3.5	4.1	3.1	2.4	3.6	4.8
μ_{eff} (cm^2/VS)	Field effect mobility	5.14	7.05	8.3	9.4	10.5	14.5	20	24
α_s	Saturation voltage parameter	0.35	0.43	0.38	0.35	0.57	0.85	0.77	0.64
γ_a	Mobility parameter	0.26	0.20	0.17	0.14	0.11	0.03	-0.04	-0.09
γ	Frequency exponent	1.05	1.02	1.05	1.1	1.01	1.0	1.02	1.04
α ($\times 10^5$) (VS/C)	Coulomb scattering coefficient	2.2	1.8	1.2	1.12	0.8	0.64	0.5	0.35
N_{st} ($\times 10^{11}$) ($eV^{-1}cm^{-2}$)	Oxide Trap density	3.89	4.1	4.3	5.4	5.9	8.3	9.3	9.8
N_{ss} ($\times 10^{11}$) ($eV^{-1}cm^{-2}$)	Surface Trap density	1.5	1.0	4.1	2.5	1.8	3.8	1.5	4.9
T_0 (K)	Characteristic Temperature	337	328	342	358	314	302	308	318
E_a (meV)	Characteristic Energy	29	28	30	31	27	26	28	27
N_{ta} ($\times 10^{21}$) ($cm^{-3}eV^{-1}$)	Density of Tail States	1.3	2.0	2.3	2.6	4.0	3.3	13	58
N_{ga} ($\times 10^{17}$) ($cm^{-3}eV^{-1}$)	Density of Deep states	1.1	1.4	2.0	2.4	4.0	5.0	13.7	23.5

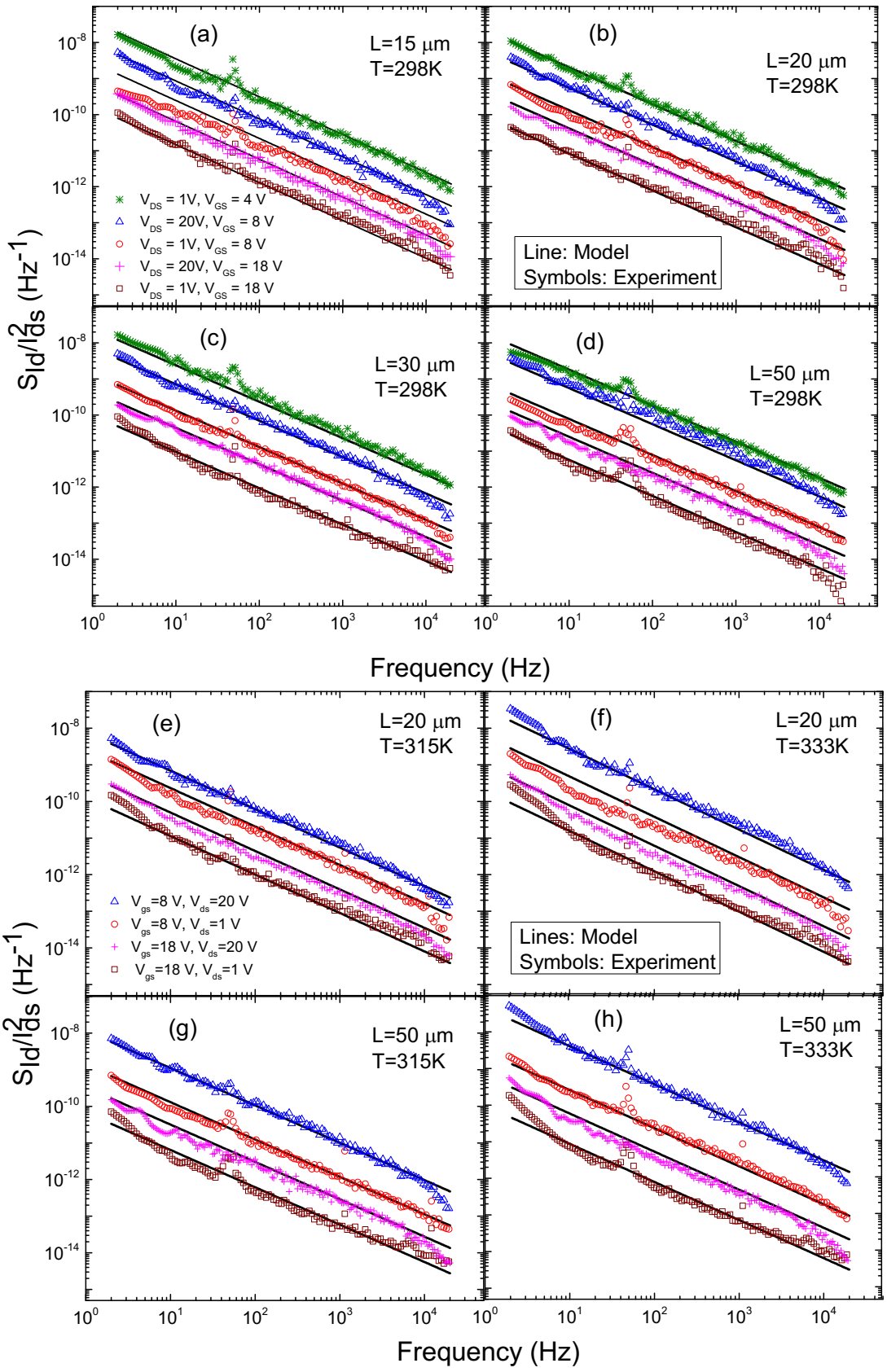

Figure 2.9 Plot of S_{Id}/I_{ds}^2 versus frequency for the $15\times100\mu m^2$ (a), $20\times100\mu m^2$ (b, e, f), $30\times100\mu m^2$ (c), and $50\times100\mu m^2$ (d, g, h) devices at 298 K, 315, and 333K in subthreshold, linear, and saturations regimes.

2.6 Conclusions

This chapter presented electrical characterization and unified modeling of DC and Flicker noise properties of amorphous InGaZnO TFTs with a thin semiconducting active layer and an Etch Stop structure. Analysis of electrical parameters extracted based on the UMEM method indicates that the devices experience a positive threshold voltage shift at high drain voltages. On the one hand, the phenomenon might be because of the bias stress caused to the devices in earlier measurements. On the other hand, densely deep subgap states can act as acceptor-like dopants and capture a considerable number of carriers. Thus, a higher gate voltage will be needed to put the devices in the ON state. The effect found to be pronounced in long channel devices and with the rise in operating temperature of the transistors.

Moreover, the carrier mobility and tail state density at the conduction band edge were found increasing with temperature. That implies the means of charge transport within the explored range of temperature is still Variable Range Hopping (VRH), different from other previously reported ESL a-IGZO devices wherein conduction mechanism changes from VRH to carrier percolation (band-like transport) at high temperatures.

To identify the mechanism of the low frequency noise in the a-IGZO devices under study, the well-known approaches for the analysis of 1/f noise in semiconductor devices-i.e., carrier number fluctuation theory and Hooge's mobility fluctuation theory, were applied. Measured LFN analysis results indicated that the normalized current noise PSD varies similarly to the squared transconductance-drain current ratio over a broad spanning of drain current. Hence, it is concluded that the measured LFN stems from the random exchange of carriers between the channel and gate-oxide traps located near the interface and correlated mobility fluctuation because of remote Coulomb scattering of charge carriers. The excellent agreement obtained between the model and experimental data both in the DC and Flicker noise behavior of the devices in 298K to 333K temperature range validates the proposed model.

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3. Low Frequency noise characterization of Organic Thin Film Transistors

Nowadays, it is common to see outcomes of fundamental science researches initiating instant technological advances. The link between the advancements in the realm of organic chemistry and the resulting technological revolution in the electronics world is one strong evidence for that. Novel Thin Film Transistors (TFTs) with organic molecular/polymeric thin films channel layer have been realized. Organic TFTs (hereafter referred to as OTFTs) have brought about unique electrical, mechanical, and industrial advantages in realizing a variety of new technological applications due to their super flexibility, low cost, and suitability for low temperature manufacturing[1]–[5]. However, issues like low carrier mobility and carrier injection need to be addressed, for the devices to be available in new commercial electronics technologies. Researchers are still striving to enhance the performance of devices through optimization of fabrication processes as well as trying different materials for the channel and gate dielectric. Thus, electrical characterization of these devices is an active area of research. Herein, we presented low frequency (LFN) characterization of SP500 polymer-based Organic Thin Film Transistors (OTFT) constituted of a non-fluorinated organic dielectric material as a gate insulator. The emphasis is very much on identifying the physical mechanism of 1/f noise and inspecting the quality of the gate dielectric/channel interface in the targeted devices.

3.1 Brief review of Flicker noise characterization of OTFTs

Study of 1/f noise property of various polymeric and small-molecule based OTFT devices have been carried out from a wide range of perspectives[6]–[15][16]–[21]. Researchers probed the quality of the dielectric/channel interface as well as source-drain contact surfaces[6][7], explored charge transport mechanisms in OTFTs[8], and evaluate carrier mobility[9], investigated the effects of different surface pretreatment conditions on device electrical properties[10], and studied degradation mechanisms without causing damages to the devices[11]- all by 1/f noise characterization of their devices. Generally, the majority of these studies concluded that carrier interaction with slow gate-insulator traps is highly improbable, and Flicker noise in OTFTs is a bulk phenomenon. It is reported that intergrain boundaries existing in the semiconducting (Organic polymer/small molecule) layer act as trapping centers. And, the fluctuation in free carrier density in the channel due to the random capture and release of charge carriers by the intergrain boundary traps are identified as the source of Flicker noise [12]–[16]. Others claimed otherwise that the randomness in the waiting time of charge hopping between intergrain traps gives rise to the fluctuation of carrier mobility and regarded as the physical origination of the measured Flicker noise[11], [17]–[21].

On the other hand, Yong Xu *et al*. and G. Giusi *et al.* argued that LFN analysis should be made over a wide range of bias to assert either the carrier number or bulk mobility fluctuation as the physical origin of 1/f noise in any devices in question. Though their study of LFN over a broad drain current spanning in Pentacene[6] and SmartKem p-FLEX small molecule[16], they demonstrated that 1/f noise as a surface phenomenon. They reported different from most of the published works that carrier number fluctuation and carrier number-correlated mobility fluctuations (CNF/CMF) due to the gate-oxide traps are the sources of the 1/f noise in their devices, respectively.

Based on the approach presented by Yong Xu *et al.*[6], 1/f noise-based characterization of OTFT devices with a non-fluorinated organic gate dielectric and SP500 polymer channel material is carried out in this thesis. This chapter succinctly presented device fabrication details followed by a quick summary of the 1/f noise measurement system. Important results obtained from analysis of the experimental data are discussed and finally, a conclusion is drawn.

3.2 Experiment

■ Device Fabrication

Top-gate and bottom-contact (BC) structure P-type OTFT devices with the schematics shown in Figure 3.1 are fabricated on a flexible plastic substrate. The Au source and drain contacts are patterned on the substrate with a SAM (Self Assembled Monolayer) deposited on top of the electrodes to ensure a good carrier injection from the source. Next, a 90 nm thick P-type undoped SP500 polymer semiconductor was spin-coated. Finally, 800 nm thick easily printable non-fluorinated gate dielectric and a silver gate were screen-printed over the active layer. Non-fluorinated dielectric materials are highly compatible with OTFT device processing conditions and improve device printability. Hence, they foresee a huge potential in the electronics industry for the low-cost fabrication of devices.

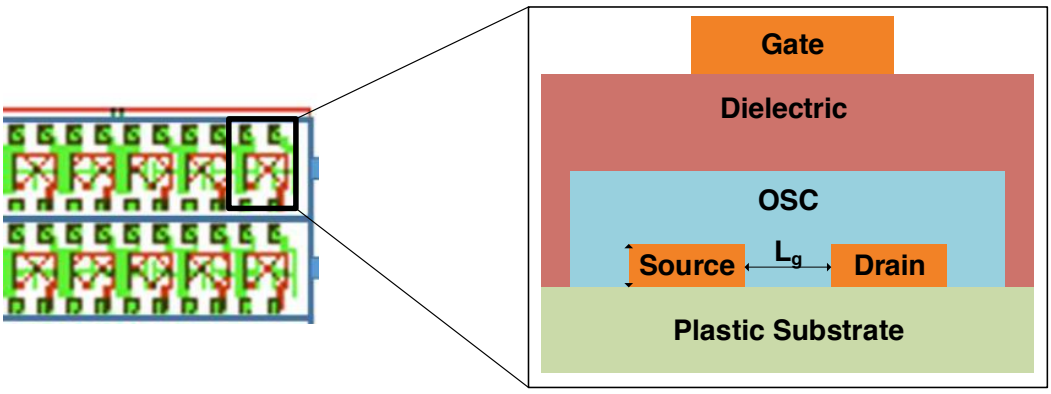

Figure 3.1 Fabricated scribes and structure schematics of the OTFT devices

■ Flicker noise measurement system

A low-frequency noise measurement system called 3PNMS that is constituted of low-noise point-probe wafer-level contacting and a variable gain programmable current amplifier (Figure *3.2*) is used for characterization of the OTFT devices. A software-based control is possible for setting the biasing conditions from a PC connected to the measurement setup. The system has the dynamicity that makes the measurement of the 1/f noise characteristics of the device under test possible at currents varied up to six orders of magnitude and essential features of programmable data acquisition and storage. That means it is capable of generating experimental data over a broad range of biases by automatically adjusting the amplifier gain based on the input from the NOISYS software. By that, the LFN PSD from subthreshold (low current intensity) to strong inversion (high current region) can be obtained, which is sufficient for the analysis to precisely detect the origin of the 1/f noise in the targeted devices[22][23].

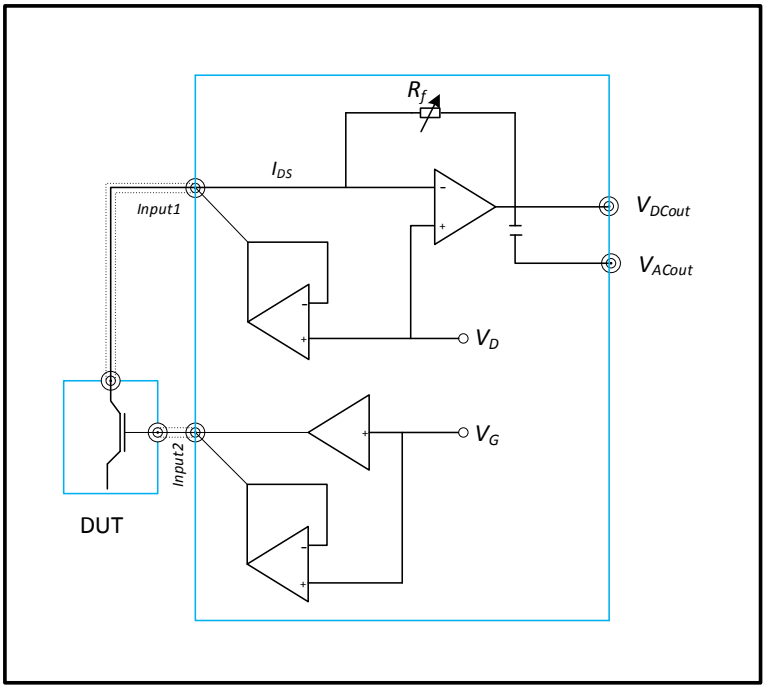

Figure 3.2 The 3PNMS 1/f noise measurement system electronics schematics.(Adopted from [22])

The characterized OTFTs have 1 *mm* width and channel lengths ranging from 10-600 µm. However, only experimental data analysis results for the 10, 40, and 80µm samples are presented here. Illustrated in Figure 3.3 are the transfer characteristics of device samples in a semi-log scale, and a linear plot of the short channel device (10 µm) I_{ds} against V_{gs} in the inset. It can be noted that no degradation of slope due to contact resistances occurs in the I_{ds}-V_{gs} characteristics of the 10 µm device at high gate voltages (Figure 3.3 inset). That is because the deposition of SAM layer on the gold contacts, analogous to what high doping of contact regions in Si process does, enables the formation of good ohmic contacts with minimum contact resistances[24][25].

Furthermore, the gate insulator, which is a bilayer of non-fluorinated organic dielectric materials, is pretreated to have impacts on the device performance. The top layer can firmly adhere to the inner one to reduce the gate leakage current. Whereas, the internal layer is optimized to passivate defects or contaminants created during device processing and form a high-quality interface with the channel material. Moreover, it positively influences the formation of grains at the interface, which in effect facilitate the hopping transport of charge carriers in the OSC. As a result, the devices demonstrated enhanced carrier mobility in the order of 2-3 cm^2/Vs.

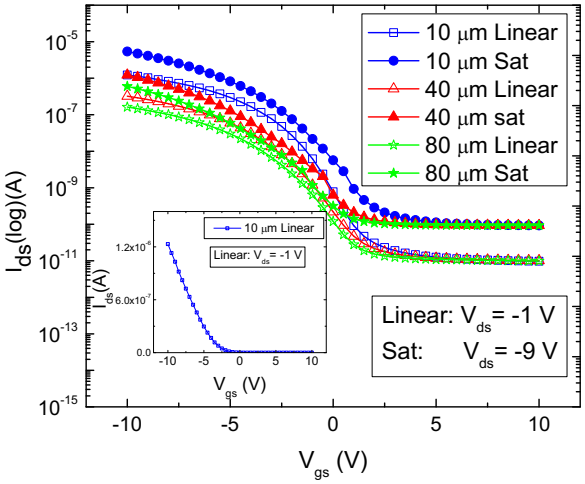

Figure 3.3 Linear and Saturation regime transfer characteristics for selected OTFT samples

3.3 Low Frequency Noise Experimental Data Analysis

Noise measurement was performed in a dark-box at room temperature using the 3PNMS system discussed in the preceding text. Typical Flicker noise behavior is obtained in the measured current noise PSD varying as $1/f^{\gamma}$ (with $\gamma \approx 1$) against frequency within the investigated range of biasing, as shown in Figure 3.4 for the 10 μm device. A small deviation of this behavior is observed in the noise PSD in the 10-30 Hz frequency range with the application of high V_{gs}, which indicates that the defects (traps) that go deeper into the oxide are less in number at that particular biases. Due to the low current present in OTFT devices, the measured current noise PSD is several orders of magnitude below the value reported in crystalline and other amorphous devices[26][27]. It approaches the system noise floor at lower gate bias points marking the corner frequency clearly as depicted in Figure 3.4. The other samples demonstrated similar behavior (not shown here).

As discussed in the previous chapter, carrier number fluctuation (ΔN), mobility fluctuation ($\Delta\mu$), or carrier number-correlated mobility fluctuation (CNF/CMF) 1/f noise models can be employed for analysis of measured LFN data to identify the physical origination of 1/f noise in any given FET device. Thus, based on (2.36), (2.39), and (2.40), we investigated the LFN obtained in the targeted OTFT devices at a sufficiently low frequency range wherein the 1/f noise is dominant.

Shown in Figure 3.5 is the normalized current noise PSD (S_{Id}/I_{ds}^2) plotted along with the extrapolated squared-transconductance drain current ratio $(g_m/I_{ds})^2$ against the drain current in log-log scale (at low and high V_{ds} region). The constant of multiplication for the $(g_m/I_{ds})^2$ corresponds to the flatband voltage noise defined in (2.40). One can see that the normalized current noise PSD does not vary as the inverse of drain current (the broken line in the figures), instead it follows the squared-transconductance ratio over three to four decades of drain current intensity. Hence, it is reasonable to conclude that the carrier number fluctuation is responsible for the 1/f noise measured in the targeted devices.

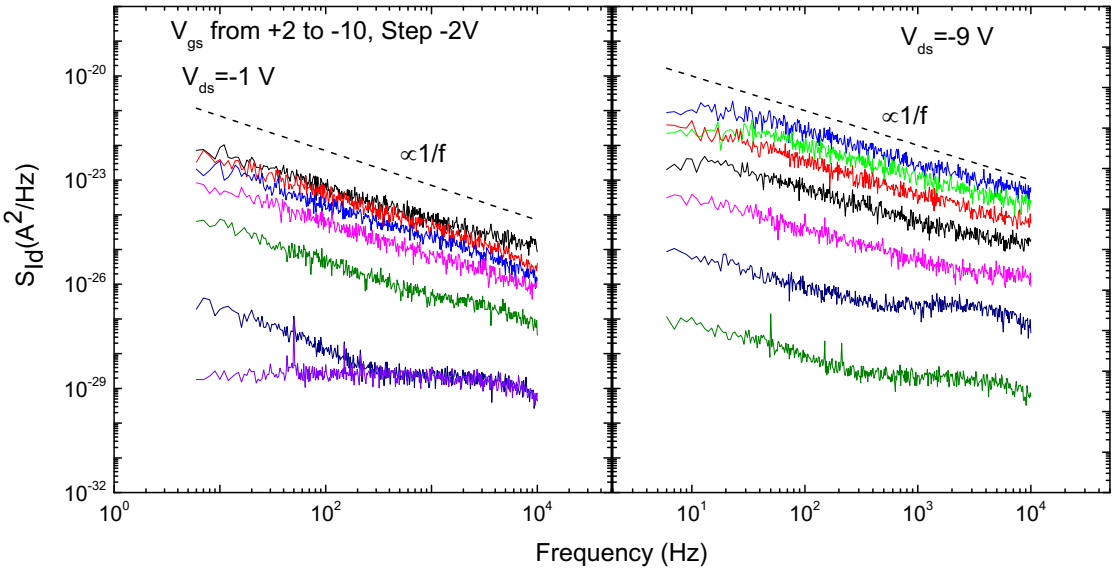

Figure 3.4 Linear and Saturation regime transfer characteristics for selected OTFT samples

By its very nature, measured *I-V* characteristics of a device under study do not provide meaningful information about the semiconducting thin film and interfaces formed between different layers within the device. Further inspection of device quality can be done using measured LFN data analysis. The carrier number fluctuation 1/f noise model helps to quantitatively probe the quality of the interface that the non- fluorinated gate-dielectric forms with the channel material. For that, values of the gate dielectric trap density (N_{st}) is evaluated from the 1/f noise data and found to be equivalent to the slow gate insulator trap density reported in CMOS devices[26]. That is indicative of the proper optimization of the inner gate dielectric layer to create a high-quality interface with the semiconducting organic thin film. Furthermore, comparison of the N_{st} to surface trap density (N_{ss}) obtained from the subthreshold slope of the *I-V* characteristics at V_{ds}=-1 V is presented in Table 3.1. The observed difference between the N_{st} and N_{ss} values implies the trap states that account for the measured LFN are uniformly distributed within the gate dielectric. Whereas, the variation of the N_{st} with device channel length is almost not worth motioning. That indicates the excellent repeatability of gate-insulator/channel interface formation achieved in the adopted device fabrication technology.

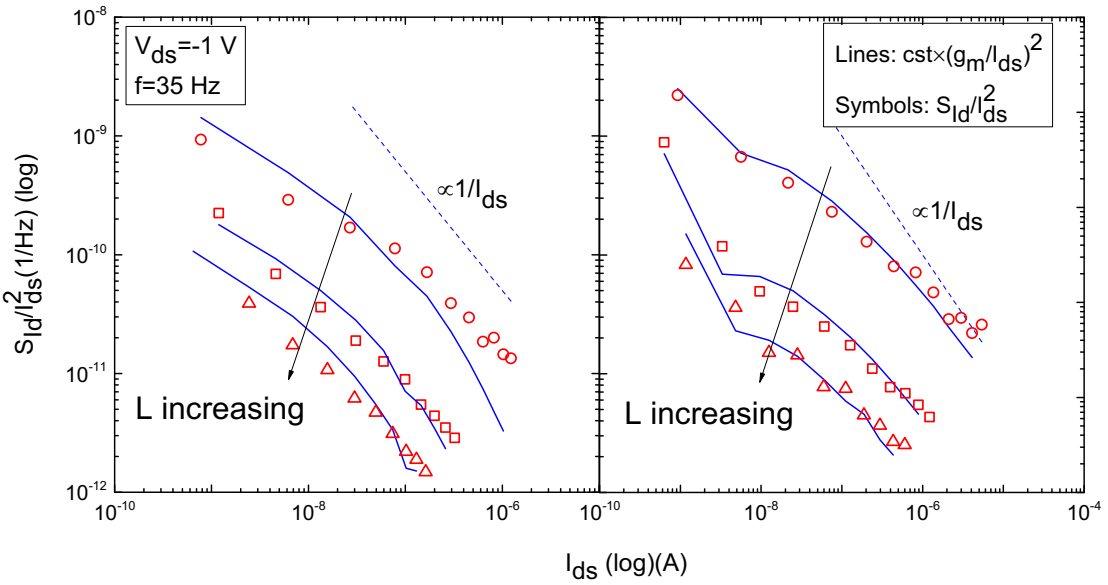

Figure 3.5 Comparison of the S_{Id}/I_{ds}^2 with extrapolated $(g_m/I_{ds})^2$ at low and high V_{ds} values

Furthermore, one can see that no contribution comes from source/drain contact interface states as the voltage/current noise PSDs appeared to be converging in strong inversion operating regime in the plot of S_{Vg}/S_{Id} (scaled with the gate area (×WL)) versus drain current (Figure 3.6). The observed invariance in the S_{Vg} (×WL) values at high drain current regions confirms the uniform distribution of the N_{st} with respect to energy in the gate dielectric as well.

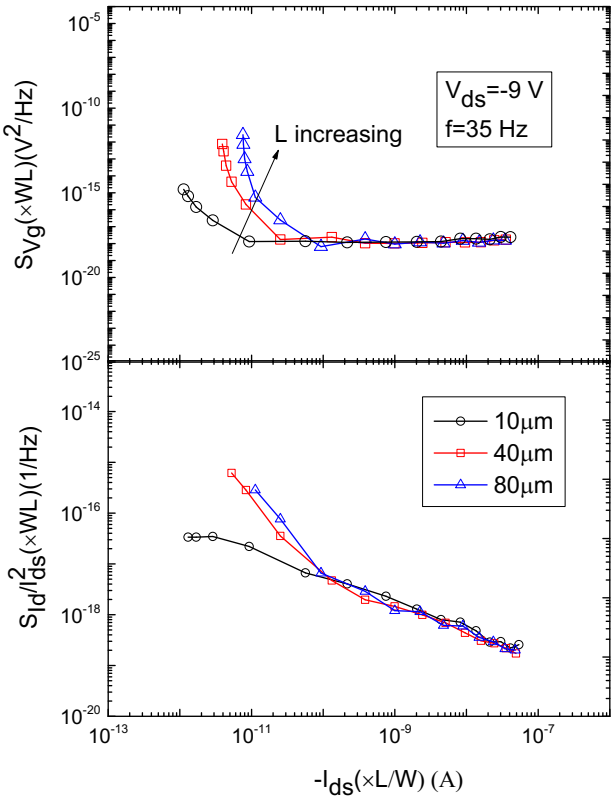

Figure 3.6 Plot of gate area scaled S_{vg} and S_{Id} of devices with different geometrical dimensions

Table 3.1List of device geometry and Extracted Model parameters

Devices	Width (mm)	Length (µm)	Vt (V)	Nst×10^{9} ($cm^{-2}eV^{-1}$)	Nss×10^{11} ($cm^{-2}eV^{-1}$)
BC1	1	10	-3.6	4.7	2.4
BC2	1	20	-3.8	4.4	3.4
BC3	1	40	-4.1	5	3.2
BC4	1	60	-4.1	3.8	2.8
BC5	1	80	-4.3	6.3	3.2

3.4 Conclusions

The chapter presented low-frequency noise characterization of polymeric OTFTs with a non-fluorinated gate dielectric material. Measurement of I-V and Flicker noise device properties is carried out over a sufficient bias range to include device operation from subthreshold to strong inversion in the LFN analysis. That is indispensable to determine the physical origin of flicker noise in the targeted devices. A clear 1/f property is observed in the measured current noise PSD over the explored frequency range. The Flicker noise stems from the carrier number fluctuation due to trapping/release of charge carriers by trap states uniformly distributed within the gate oxide. High-quality gate-insulator/channel interface is achieved in these OTFTs compared to devices from previous technologies. The results demonstrated the excellent progress made in the fabrication of OTFT devices for state-of-the-art flexible electronics applications.

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Part Two

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4. Piezoelectric Modeling in GaN HEMTs

In AlGaN/GaN HEMTs, the strain induced in the AlGaN layer sets the maximum thickness to be grown on a relaxed GaN depending on the Al composition. For a particular Aluminum content, increasing the AlGaN layer thickness beyond this maximum value causes a rapid formation of crystal dislocations due to strain relaxation. The phenomenon results in a decline in the total induced polarization charge in the barrier layer, and in turn, reduce mobile carrier density. Considering the effect and other important factors that cause changes in the energy bandgap, distribution of surface donor states, and the profile of charge distribution in the AlGaN/GaN, this chapter introduces a physics-based approach for modeling the piezoelectric effect in AlGaN/GaN HENT transistors. The main idea is to define a polarization dependent threshold voltage model that is valid for HEMT devices that have an Aluminum content and barrier layer thickness within a practical range.

A summary of previous works and discussion on the physical properties of materials that are essential for piezoelectric effect modeling in GaN HEMTs are introduced. Next, the derivation of polarization dependent threshold models for different device architectures, and a review on a charge based GaN HEMT *I-V* model previously developed by our group are presented. Simulation results of different structures of GaN HEMTs are then demonstrated along with experimental data for validating the proposed models.

4.1 Previous polarization modeling in AlGaN/GaN HEMTs

The majority of physically-based compact GaN HEMT models proposed so far are derived based on the exact definition of the density the 2DEG in terms of device terminal voltages. Experiment and simulation results showed that the 2DEG concentration is strongly dependent on the polarization charge induced in the layers of the HEMT stack, and the models accounted for that in a unified polarization dependent threshold voltage expression given by[1]–[4]

$$V_{th} = \phi_b - \Delta E_C - \frac{qN_D d_d^2}{2\varepsilon} - \frac{\sigma}{\varepsilon}(d_d \quad d_i) \tag{4.1}$$

where the V_{th} is the threshold voltage, ϕ_b is the Schottky barrier height, ΔE_C is the conduction band offset. N_D, d_d, and ε are the donor doping level, thickness, and dielectric constant of the *n* doped barrier layer. q is the elementary charge, and d_i is the thickness of the spacer layer (which is usually an undoped AlGaN or AlN material). However, calculated V_{th} values using the above expression are sufficiently far apart from the values extracted from experimental data for devices with higher Al composition (x). For instance, two AlGaN/GaN sample devices with 0.25 and 0.22 alloy composition, 35 nm and 28 nm barrier layer thickness, Si doping density

of 2×10^{18} cm^{-3} in the charge AlGaN layer, and a 3 nm undoped AlGaN spacer layer have −7 V, and −4.2 V reported V_{th} values, respectively. The values calculated based on the information provided, and (4.1), on the other hand, are −10.14 V and −6.72 V, which by far exceeded the correct parameter values[5][6]. The possible explanations for such apparent inconsistency are:

- While simulation and experimental results show that ϕ_b is an explicit function of x and the barrier layer thickness[7]–[10], in many of the GaN HEMT models, it is defined using a simple extrapolated function of x. That does not catch the underlying physics behind the strong dependence of the parameter on the AlGaN layer thickness and Al content.

- The effect of the high alloy composition and barrier layer thickness on the lattice mismatch between the AlGaN and GaN layers, and in turn, on the polarization charge induced in the barrier layer is not considered in many cases[7]–[10].

- The effect of a GaN-cap or AlN nucleation layer on the energy band diagram and the Schottky barrier height is not mostly accounted for. Furthermore, the thickness and polarization of such layers influence the total polarization charge induced in the heterointerfaces and the 2DEG density. But these effects are neglected in the definition of the threshold voltage, and the expression in (4.1) incorrectly predicts the parameter for HEMTs that have such layers in their structure.

In light of the above effects, physics-based V_{th} models are derived here that are valid for GaN HEMT devices with Al composition and barrier layer thickness within the practical range.

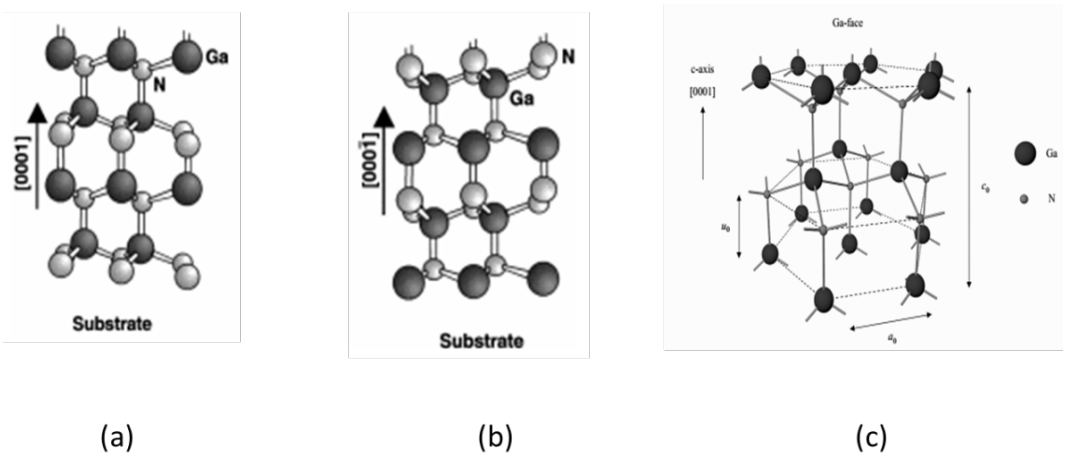
4.2 Polarization

Understanding the crystal structure and physical properties of group III-nitrides and their ternary alloys is fundamental to piezoelectric effect modeling in GaN HEMTs.

■ Lattice Structure and Physical properties of group III-Nitrides and their alloys

III-V compound semiconductors are the basic building blocks of a HEMT device. These materials manifest themselves in Wurtzite (WZ), Zincblende, or rock-salt crystal structures. GaN is among this group of materials. And, when it is used in the fabrication of HEMTs, it crystallizes in WZ structure, which is inherently stable at ambient conditions. The WZ GaN grows either in the [0001] or [000$\bar{1}$] crystallographic axis, yielding two different lattices referred to as Ga-face and N-face, respectively. These crystals exhibit distinct atom sequencing, crystal faces, and chemical properties. However, they have the same hexagonal primitive unit cell composed of four atoms connected in the tetrahedral form, which is defined by the basal edge length (a_0), hexagonal prism height (c_0), and cation-anion bond length (u_0) measured in

units of c_0 as illustrated in Figure 4.1[11]. The values of these lattice parameters and other physical properties of different III-Nitride materials are presented in Table 4.1 for comparison.



(a) (b) (c)

Figure 4.1 Crystallographic structure Ga-faced (a), N-faced (b), unit cell (c) of Wurtzite GaN. (Adopted from[11]).

Ternary alloys of the III-Nitrides are the other essential components of a HEMT device. The crystal structure and other physical properties of these materials are strongly dependent on the alloy composition (the ternary alloy mole fraction). And, they can be obtained through extrapolation of the lattice constants and physical properties of the patent (III-Nitride) binary compounds. For the AlGaN alloy, they are given by[12]–[14]:

Piezoelectric coefficients e_{33} and e_{31}:

$$e_{31}(x) = (-0.11x - 0.49)\ \mathrm{Cm}^{-2}, \tag{4.2}$$

$$e_{33}(x) = (0.73x + 0.73)\ \mathrm{Cm}^{-2}. \tag{4.3}$$

Lattice constant a:

$$a(x) = (-0.077x \quad 3.189).10^{-10}\ \mathrm{m}. \tag{4.4}$$

Elastic constants C_{31} and C_{33}:

$$C_{13}(x) = (5x + 103)\ \mathrm{Gpa}, \tag{4.5}$$

$$C_{33}(x) = (-32x \quad 405)\ \mathrm{GPa}. \tag{4.6}$$

The energy band gap:

$$E_g(x) = (1-x)E_g(GaN) + xE_g(AlN) - bx(1-x) \tag{4.7}$$

where x is the Al composition of the AlGaN crystal, $E_g(x)$, $E_g(GaN)$, and $E_g(AlN)$ are the energy band gap of the AlGaN, GaN, and AlN materials respectively, and b is the bowing parameter [15].

■ Polarization in III-Nitrides

The atom-atom interaction in a WZ III-Nitride crystals are typical of SP^3 covalent bonding nature; meaning that they are formed by sharing of electrons between hybridized outer shall orbitals of the involved atoms. Because of the smaller size of nitrogen atoms and their high electronegativity, the shared electrons experience a strong Coulombic attraction giving the covalent bonds substantial ionic character. This effect, together with the non-centrosymmetric nature of a WZ crystal structure initiates the formation of microscopic spontaneous polarization in the direction of the c-axis. The strength of this polarization is sensitive to the ionicity of interatomic covalent bonds and the change in the non-ideality factor of the crystal (the deviation of a material's lattice constant ratio, c_0/a_0, from the ideal value of a closed packed hexagonal structure which is ≈1.633). In an ideal WZ lattice, only the covalent bonds oriented in the direction of the *c*-axis induce the spontaneous polarization; the contributions from the basal bonds are oppositely directed and cancel each other out. Whereas in the case of non-ideal WZ structures, since the c_0/a_0 value differs from 1.633, the basal bonds produce a non-zero resultant polarization to increase the total polarization in the crystal[16]. One can note these effects from the difference observed between the spontaneous polarization magnitudes (P_{SP} values) of materials listed in Table 4.1.

Table 4.1 Spontaneous polarization, elastic, and lattice constants in group III-nitride compound semiconductors. (Reproduced from [14])

Wurtzite	AlN	InN	GaN
a_0(Å)	3.1112	3.54	3.189
c_0(Å)	4.982	5.705	5.185
a_0/c_0	1.601	1.612	1.627
u_0	0.380	0.377	0.376
$e_{33}(Cm^{-2})$	1.46	0.97	0.73
$e_{31}(Cm^{-2})$	-0.60	-0.57	-0.49
$P_{sp}(Cm^{-2})$	-0.081	-0.032	-0.029

Another remarkable property of III-Nitride materials is that displacement of sub-lattices under the influence of an external strain alters their lattice constants, such that, the non-ideality factor of the crystals deviates from the ideal value of 1.633. Such effect gives rise to the formation of additional strain induced polarization which is defined by

$$P^{pz} = e_{33}\varepsilon_z + e_{31}\left(\varepsilon_x + \varepsilon_y\right) \tag{4.8}$$

where, P^{pz} is the piezoelectric polarization, e_{33} and e_{31} are piezoelectric coefficients of the strained material, $\varepsilon_z = (c-c_0)/c_0$ is the strain directed in the c-axis. ε_x and ε_y are isotropic strains and are equal to $(a-a_0)/a_0$ with a_0 and c_0 being the lattice constants of the unstrained material. The defined strain components are interrelated via[12]–[14]

$$\left(\frac{c-c_0}{c_0}\right) = -2\frac{C_{13}}{C_{33}}\left(\frac{a-a_0}{a_0}\right) \tag{4.9}$$

where C_{31} and C_{33} are elastic constants of the strained material.

By combining (4.8) and (4.9), the piezoelectric polarization in strained group III-Nitride materials and their alloys is redefined as[12]–[14]

$$P^{pz} = 2\frac{a-a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right). \tag{4.10}$$

■ The AlGaN/GaN HEMTs

Shown in Figure 4.2 is a schematic of an AlGaN/GaN HEMT structure with a thin polarization induced sheet charge density ($\pm\sigma_{AlGaN}$) formed at the AlGaN top and bottom surface, the 2DEG confined at the AlGaN/GaN interface, and the surface state charge density. The charge dipole ($\pm\sigma$AlGaN) created in the barrier layer is the combined effect of the induced spontaneous and piezoelectric polarizations.

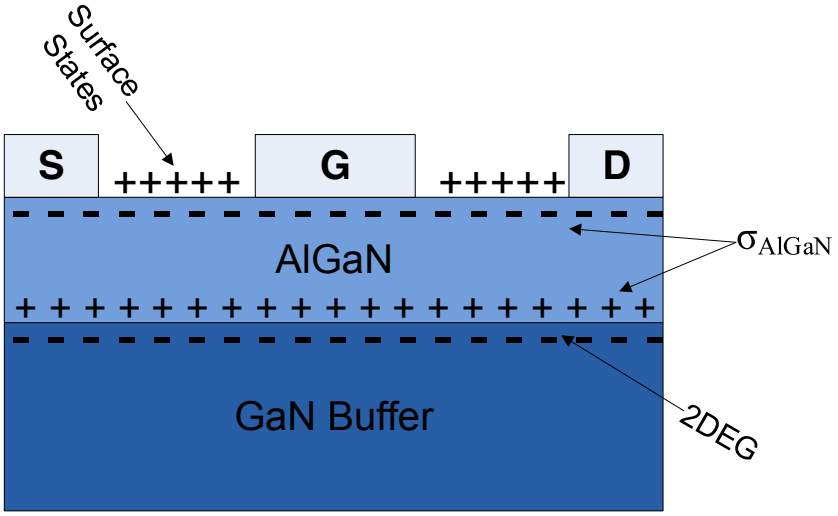


Figure 4.2 Epitaxial structure of AlGaN/GaN HEMT.

Polarization induced in the AlGaN material is highly dependent on its Aluminum composition. The spontaneous polarization is determined by extrapolation of the spontaneous polarization

(P_{AlGaN}^{sp}) of the parent GaN and AlN compounds as it is done above to evaluate the crystal lattice constants of the AlGaN [8][14]:

$$P_{AlGaN}^{sp}(x) = (-0.0052x - 0.029)\ \mathrm{Cm}^{-2}. \tag{4.11}$$

On the other hand, the magnitude of the piezoelectric polarization induced in the AlGaN layer in HEMTs is influenced by the interrelated effect of the Al composition and thickness of the layer. For any given Al mole fraction, strain relaxation sets a critical thickness (d_{crr}) for AlGaN layer that can be grown on GaN without the generation of misfit dislocations it. This d_{crr} value is inversely proportional to the Al content. Based on the inferences made from various experimental observations, Nitin G. *et al.* describes the relationship with a simple mathematical formula as[8]

$$d_{crr} = d_0 x^{-1.04} \tag{4.12}$$

where $d_0 \approx 4.17nm$. Increasing the d beyond the d_{crr} relaxes the strain energy (s_r) stored in the AlGaN layer in an exponential manner as[8]

$$s_r = s_{crr} \exp\left(1 - \frac{d}{d_{crr}}\right) \tag{4.13}$$

where s_{crr} is the empirical parameter, and d is the barrier layer thickness. Thus, the strain induced piezoelectric polarization (P_{AlGaN}^{pz}) follows a similar trend, and its definition in (4.10) is rewritten below to consider this effect as[8]

$$P_{AlGaN}^{pz} = 2s_r\left(\frac{a - a_0}{a_0}\right)\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right). \tag{4.14}$$

Equations (4.11) and (4.14) define the contributions of the spontaneous (P_{AlGaN}^{pz}) and piezoelectric polarization (P_{AlGaN}^{sp}) to the total bound charge induced in the AlGaN layer ($\pm\sigma_{AlGaN}$) which reads[12]–[14]

$$\sigma_{AlGaN} = P_{AlGan}^{sp}(x) + P_{AlGaN}^{pz}(x). \tag{4.15}$$

Generally, the direction of the induced polarization determined by atomic layer ordering in the crystal. Hence, it is essential to note that the expression derived here considers an AlGaN crystal grown on top of a Ga-faced GaN buffer layer.

■ 2DEG formation in AlGaN GaN HEMTs

In GaN HEMTs, it is possible to achieve a two-dimensional electron gas (2DEG) with a sheet carrier concentration of 10^{-13} cm^{-2} in the absence of intentional doping. A substantial number of studies have been conducted to understand what key mechanism controls the formation of such very high electron density. Researchers suggested ideas of piezoelectric doping[17], unintentional impurities in AlGaN layer[18], and polarization assisted thermal generation[19] as possible explanations. However, numerical simulations and experimental observations interestingly tend to show the dependence of the 2DEG electron concentration on the Al content and thickness of the AlGaN layer. This has been explained in previous works based on a concept that identifies donor-like surface states located on top of the AlGaN layer as the likely source of electrons that form the 2DEG. And, the theory is now widely accepted within the compact modeling community to explain 2DEG formation in GaN HEMTs.

How the donor states contribute electrons to the 2DEG can be explained with reference to the AlGaN layer thickness. While the AlGaN is very thin, the top surface-states located far below the Fermi-level thus, no electrons drift towards the potential well. Increasing the barrier thickness lift the donor states up, and align them with the Fermi-level, such that they begin to donate electrons for the 2DEG formation. Some researchers obtained a constant Schottky barrier height (Fermi-level pinning) with varying the barrier height thickness as can be seen in Figure 4.3 (a), and they supported their result with a hypothesis that a high density of donor surface states exists on the AlGaN surface[20][21].

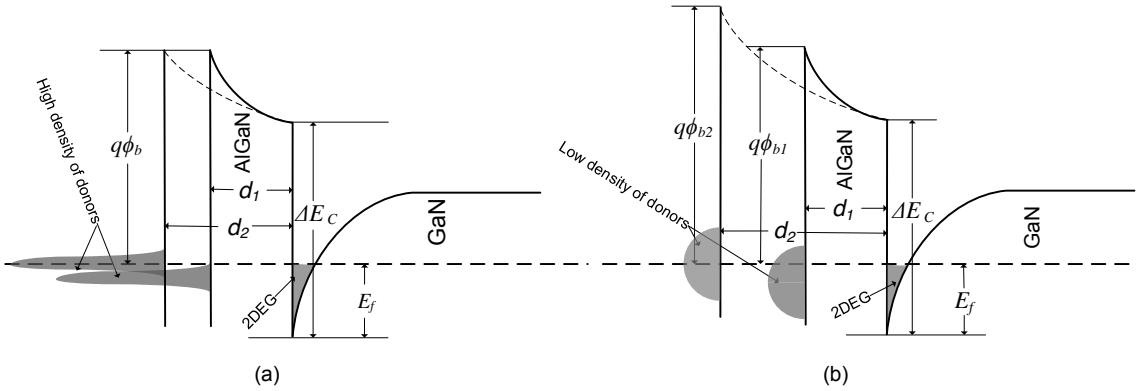


Figure 4.3 Donor surface states density distribution. (Reproduced from [7])

Other groups reported changes in Schottky barrier height (SBH) with the thickness of the AlGaN layer. S. Helkman *et al.* observed varying SBH value from 1 .0 to 1.8 eV for the shift in the AlGaN thickness from 5 to 44 nm[22]. The SBH was found increasing considerably with the barrier layer thickness in other works reported on measurement and modeling of SBH and the 2DEG electron density in GaN HEMTs [7]–[10][23][24]. These results suggested that low density of surface donor states exists distributed over a broad range of energies on the AlGaN top, and the transfer of electrons to the heterointerface depletes a significant amount of these surface states. Thus, the Fermi level is no longer pinned in such a case as it needs to move down to accommodate more donor states for increasing the supply of electrons to the 2DEG with the increase in the barrier layer thickness, and the SBH increases proportionally (Figure

4.3 (b)). Based on this analysis, a simple dual-parameter model for the 2DEG density was proposed by Niting .G. et al. The model is adopted in the derivation of the ϕ_b and V_{th} analytical expressions. Assuming that low density of surface donor states (n_0 per unit area per eV) exist on the AlGaN top distributed over a range of energies, at a particular donor level E_d relative to the conduction band edge of the AlGaN layer, one can tell that the number of electrons contributed to the 2DEG (the green area in Figure 4.4) amounts to[7]–[10]

$$n_s = n_0(q\phi_b - E_d) \tag{4.16}$$

where n_s is the electron density in the 2DEG.

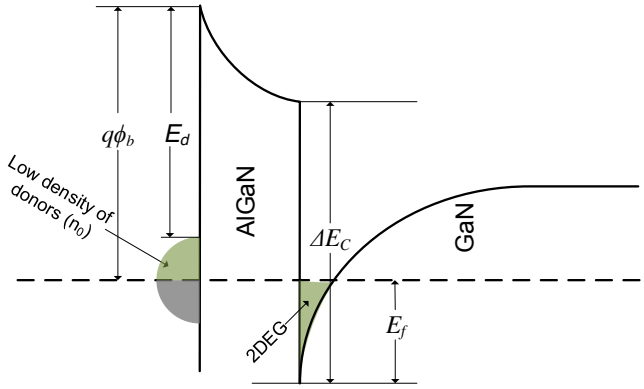


Figure 4.4 Donor surface states density distribution.
(Reproduced from [7])

4.3 Derivation of Schottky Barrier and Threshold Voltage Models

State-of-the-art GaN HEMT device architectures studied in this work are illustrated together with their corresponding energy band diagrams in Figure 4.5.

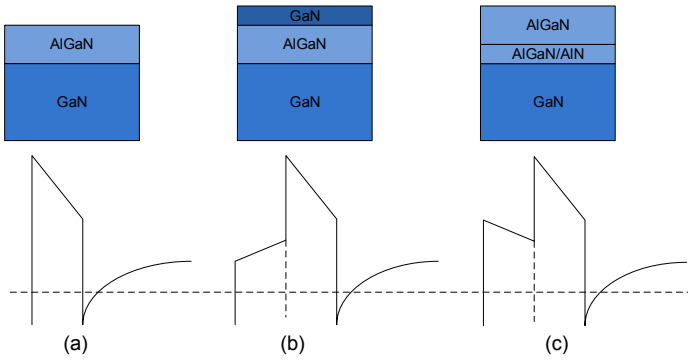


Figure 4.5 Different structures of GaN HEMTs and
their corresponding energy band diagram.

The difference in structural configurations of the devices necessitated deriving ϕ_b and V_{th} models unique to each device architecture separately.

■ The AlGaN/GaN Structure

This is the most common architecture of GaN HEMTs. The energy band diagram and the charge distribution profile in the stack for this typical configuration are shown in Figure 4.6. The electric field in barrier layer reads[25]:

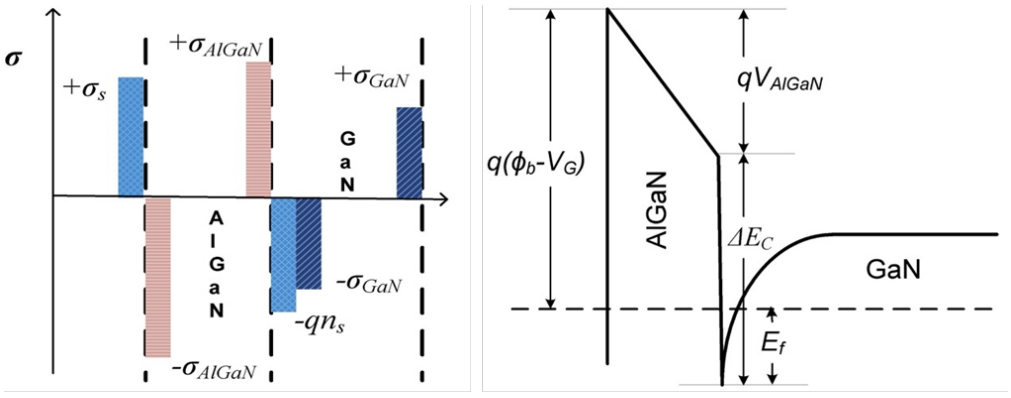
$$\frac{V_{AlGaN}}{d_{AlGaN}} = \frac{\sigma_{AlGaN}}{\varepsilon} - \frac{qn_s}{\varepsilon} \tag{4.17}$$

where V_{AlGaN} the voltage drop across the barrier layer, d_{AlGaN} is the layer thickness, and ε is the dielectric constant. Furthermore, based on the energy band diagram illustrated in Figure 4.6 (b), the following relationship between the Schottky barrier height, the voltage drop across the barrier layer, and the conduction band offset can be obtained[7]–[10]:

$$\phi_b - V_G = V_{AlGaN} + \frac{\Delta E_C}{q} \quad \frac{E_f}{q} \tag{4.18}$$

where E_f is the Fermi-level and ΔE_C is the conduction band offset that reads as[14]

$$\Delta E_C = 0.7\left(\Delta E_g(x) - \Delta E_g(GaN)\right). \tag{4.19}$$



(a) (b)

Figure 4.6 AlGaN/GaN HEMT device configuration (a) charge distribution and (b) Energy band diagram. (Reproduced from [25])

Solving (4.17) and (4.18) simultaneously under two different conditions yields the Schottky barrier and the threshold voltage expressions.

- **Case 1:** by setting V_G to 0, neglecting the E_f as its change is in the order of the thermal voltage, and replacing n_s with the expression defined in (4.16), it is possible to the polarization dependent Schottky barrier height expression[7]–[10]:

$$\phi_b = \frac{\left(\varepsilon / qd_{AlGaN}\right)\left[\frac{\sigma_{AlGaN} d_{AlGaN}}{\varepsilon} + \frac{\Delta E_C}{q}\right] + n_0 E_d}{\left(\frac{\varepsilon}{qd_{AlGaN}} + n_0 q\right)} \tag{4.20}$$

- **Case 2:** Considering V_G *and* E_f, and solving for n_s gives

$$n_s = \frac{\varepsilon}{qd_{AlGaN}}\left(V_G - V_{th} - \frac{E_f}{q}\right) \tag{4.21}$$

where

$$V_{th} = \phi_b - \frac{\sigma_{AlGaN} d_{AlGaN}}{\varepsilon} - \frac{\Delta E_C}{q}. \tag{4.22}$$

One should note at this point that the ϕ_b expression defined in (4.20) is used in (4.22) to calculate the V_{th} parameter. In cases when the barrier layer in GaN HEMTs is partly n-doped to increase the electron density in the 2DEG, the donor charge density must be considered in the calculation of the V_{th}. Thus, (4.1) will be used together with the corresponding ϕ_b and σ_{AlGaN} defined in (4.20) and (4.15).

■ GaN/AlGaN/GaN

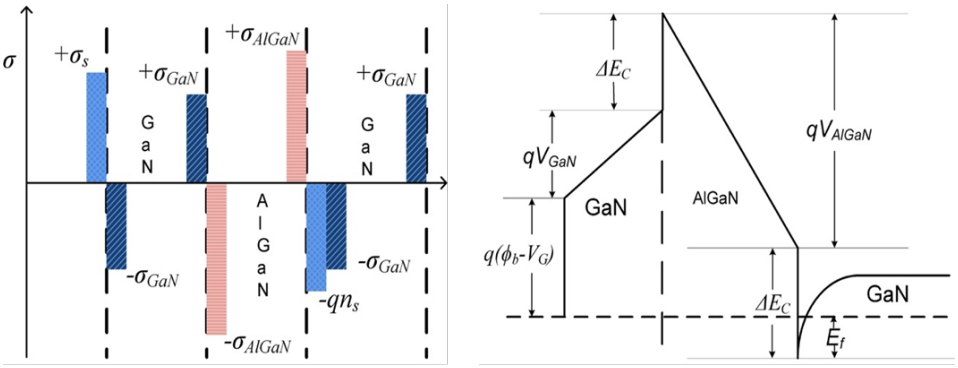
In this structure, the GaN cap layer deposited at the top of the barrier layer partially depletes the donor surface states, so does it alter the charge distribution is the stack and the electron concentration in the 2DEG. As shown in Figure 4.7(a), the charge in each layer can be considered as a dipole: 1) the polarization-induced charge in the cap layer ($\pm\sigma_{GaN}$); 2) the barrier layer polarization-induced charge ($\pm\sigma_{AlGaN}$); 3) polarization-induced charge in the GaN buffer layer ($\pm\sigma_{GaN}$); and 4) the ionized donor surface charge (σ_s) and the electron density in the 2DEG (n_s). With the coordinates defined in Figure 4.7 (a), it is possible to derive expressions for the electric field in each layer independently as[25]

$$\frac{V_{GaN}}{d_{GaN}} = \frac{\sigma_{GaN}}{\varepsilon} - \frac{qn_s}{\varepsilon} \tag{4.23}$$

$$\frac{V_{AlGaN}}{d_{AlGaN}} = \frac{\sigma_{AlGaN}}{\varepsilon} - \frac{qn_s}{\varepsilon} \tag{4.24}$$

where V_{GaN} is the voltage drop across the cap layer, σ_{GaN} is cap layer polarization charge, ε is the dielectric constant which we assumed to be the same for GaN and AlGaN to simplify the models, and d_{GaN} is the cap layer thickness. Similarly, the cap layer potential V_{GaN} is related to the potential drop across the barrier layer as

$$V_{GaN} = (\phi_b - V_G) - V_{AlGaN} + \frac{E_f}{q}. \tag{4.25}$$



(a) (b)

Figure 4.7 GaN/AlGaN/GaN HEMTs (a) charge distribution and (b) Energy band diagram. (Reproduced from [25])

To determine the Schottky barrier height, solving (4.23) to (4.25) simultaneously with the V_G value set to zero, neglecting the E_f as in the case of the AlGaN/GaN HEMT, and using the n_s expression in (4.16) gives (**Case 1**)[26]

$$\phi_b = \frac{\left(\frac{\varepsilon}{qd}\right)\left(\frac{\sigma_{AlGaN} d_{AlGaN}}{\varepsilon} + \frac{\sigma_{GaN} d_{GaN}}{\varepsilon}\right) + n_0 E_d}{qn_0 + \frac{\varepsilon}{qd}} \tag{4.26}$$

where $d = d_{AlGaN} + d_{GaN}$.

On the other hand, solving for n_s considering a non-zero V_G value and E_f returns (**Case 2**)

$$n_s = \frac{\varepsilon}{qd}\left(V_G - V_{th} - \frac{E_f}{q}\right) \tag{4.27}$$

where V_{th} is the polarization dependent threshold voltage that can be computed as[26]

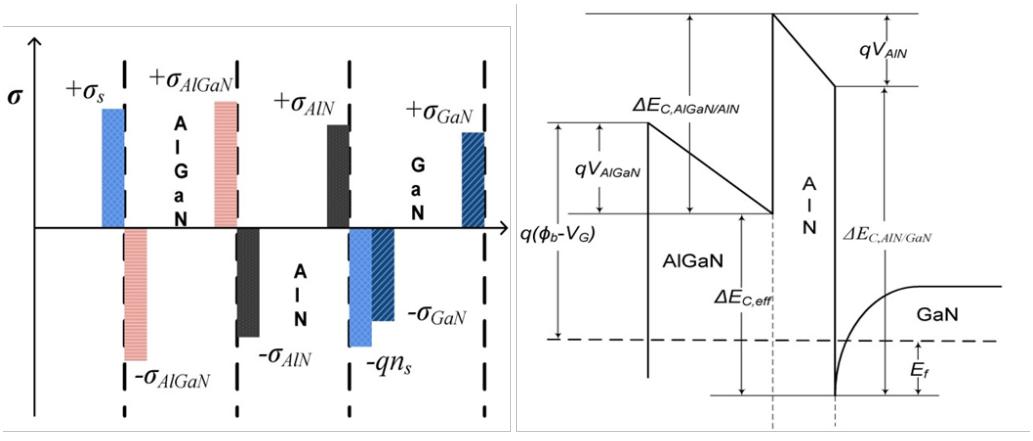
$$V_{th} = \phi_b - \frac{\sigma_{GaN} d_{GaN}}{\varepsilon} - \frac{\sigma_{AlGaN} d_{AlGaN}}{\varepsilon}. \tag{4.28}$$

Equations (4.26) and (4.28) define the Schottky barrier height (ϕ_b) and the threshold voltage (V_{th}) of GaN HEMT devices with a GaN-cap layer, and the first expression (the ϕ_b) has to be used in the computation of the later (the V_{th}) as in the case of the AlGaN/GaN structure[26].

■ AlGaN/AlN/GaN Structure

When a thin AlN spacer layer inserted in a HEMT epitaxy, it strengthens the total polarization in the stack because the material has high spontaneous polarization compared to other group III-Nitride compounds. Thus, more electrons can be transferred from the barrier layer surface towards the 2DEG. A thin AlN interlayer also enhances carrier mobility in the 2DEG by shielding the electrons from remote scattering due to immobile ionized donor atoms present in the barrier layer. For these reasons, GaN HEMT devices with a thin AlN interfacial layer demonstrate remarkable performance improvements. Moreover, the forward Schottky gate current is low in such device structures and that enables a wide range of gate voltage for device operation[27]–[29].

Figure 4.8(a) depicts the charge distribution and corresponding energy band diagram of the AlGaN/AlN/GaN structure.



(a) (b)

Figure 4.8 AlGaN/AlN/GaN HEMT architecture (a) charge distribution and (b) Energy band diagram. (Reproduced from [25])

The electric field in each layer is given as[25]:

$$\frac{V_{AlGaN}}{d_{AlGaN}} = \frac{\sigma_{AlGaN}}{\varepsilon} - \frac{qn_s}{\varepsilon} \tag{4.29}$$

$$\frac{V_{AlN}}{d_{AlN}} = \frac{\sigma_{AlN}}{\varepsilon} - \frac{qn_s}{\varepsilon} \tag{4.30}$$

where the V_{AlN} is the voltage drop across the AlN interlayer and σ_{AlN} is the corresponding induced polarization charge. ε is the dielectric constant that is considered the same for the AlGaN and interfacial AlN layers for model simplicity. Furthermore, the following relationships can be formulated through the application of basic geometry rules on the energy band diagram shown in Figure 4.8(b):

$$V_{AlGaN} = \left(\phi_b - V_G\right) - \frac{\Delta E_{C,eff}}{q} - \frac{E_f}{q} \tag{4.31}$$

where the effective conduction band gap $\Delta E_{c,eff}$ is

$$\Delta E_{C,eff} = qV_{AlN} + \Delta E_{C,AlGaN/AlN} - \Delta E_{C,AlN/GaN} \tag{4.32}$$

with the $\Delta E_{C,AlGaN/AlN}$ and $\Delta E_{C,AlN/GaN}$ are the conduction band offsets at first (AlGaN/AlN) and second (AlN/GaN) interfaces respectively.

To obtain the desired models, firstly, the expression for ϕ_b is derived by using (4.29) to (4.32) , setting V_G=0, ignoring E_f, and substituting n_s from (4.16) to yield[30]

$$\phi_b = \frac{\left(\Delta E_{ef}/q\right) + \left(qd_t n_0 E_d/\varepsilon\right) + \left(\sigma_{AlGaN} d_{AlGaN} + \sigma_{AlN} d_{AlN}\right)/\varepsilon}{1 + q^2 n_0 d_t/\varepsilon} \tag{4.33}$$

where $d_t = d_{AlGaN} + d_{AlN}$ and $\Delta E_{ef} = \Delta E_{C,AlN/GaN} - \Delta E_{C,AlGaN/AlN}$..

Next, taking into account V_G and E_f, to solve for n_s, one will have[30]:

$$n_s = \frac{\varepsilon}{qd_t}\left(V_G - V_{th} - \frac{E_f}{q}\right) \tag{4.34}$$

$$V_{th} = \phi_b - \left(\frac{\sigma_{AlGaN} d_{AlGaN}}{\varepsilon} + \frac{\sigma_{AlN} d_{AlN}}{\varepsilon} \right) \frac{\Delta E_{ef}}{q}. \quad (4.35)$$

4.4 Charge based I-V model

This model was developed by Universitat Rovira i Virgili (NePhos group) in 2013. It is a charge-based version of the ASM GaN HEMT compact model that recently passed the repeated testing and evaluation of various industry players for standardization according to the CMC standard qualification benchmarks.

■ Core current model derivation

A simple charge control model, derived based on the interdependent relationship of the heterojunction parameters and some reasonable assumptions, is the fundamental building block of the charged-based *I-V* model. It reads as[3]

$$V_{go} - V = \frac{q d n_s}{\varepsilon} + \gamma_0 n_s^{2/3} + V_T \ln\left(\frac{n_s}{D V_T} \right). \quad (4.36)$$

And, its derivative with respect to the 2DEG density n_s is[3]

$$\frac{dV}{dn_s} = \frac{qd}{\varepsilon} + \frac{2}{3} n_s^{\frac{-1}{3}} + V_T n_s^{-1}. \quad (4.37)$$

where $V_{go}=V_{gs}-V_{th}$, where V_{th} is one of the threshold voltage expressions defined above in (4.22), (4.28), or (4.35). V is the potential at any point in the channel, V_T is the thermal voltage, D is the density of states, d represents d_{AlGaN}, $d_{AlGaN}+d_{GaN}$, or $d_{AlGaN}+d_{AlN}$ in AlGaN/GaN, GaN/AlGaN/GaN, and AlGaN/AlN/GaN structures, respectively, and γ_0 is a constant estimated from Shubnikov DeHass or cyclotron resonance experiments[31].

The basic definition of channel current in FET devices can be adopted for HEMTs and redefined in terms of the 2DEG concentration as[3]

$$I_{ds} = -\frac{W}{L} q \mu \int_{V_s}^{V_d} n_s dV \quad (4.38)$$

where W is the device width, L is the channel length, and μ is the field effect mobility. By combining (4.36), (4.37), (4.38), solving the integration from source to drain provides[3]

$$I_{ds} = -\frac{W}{L} q\mu \int_{n_s}^{n_d} \left(\frac{qd}{\varepsilon} n_s + \frac{2}{3}\gamma_0 n_s^{2/3} + V_T \right) dn_s ,$$
$$I_{ds} = -\frac{Wq\mu}{L} \left[\frac{qd}{\varepsilon} \left(n_D^2 - n_S^2 \right) + \frac{2}{5}\gamma_0 \left(n_D^{5/3} - n_S^{5/3} \right) + V_T \left(n_D - n_S \right) \right] \quad (4.39)$$

where the n_D and n_S are the total charge carrier concentrations at the drain and source ends of the device respectively. Equation (4.40) defines the charge-based core current model developed for GaN HEMTs by Yigletu *et al.*[3]. An explicit analytical expression proposed by S. Khandelwal *et al.,* valid for all regimes of device operation is implemented here to determine the total 2DEG density at the source and drain ends of the device[2]. And, the following additional but essential factors have been accounted for in the *I-V* characteristics modeling of the HEMT transistors in this thesis.

■ Effects of non-linear access region resistances

The influence of access regions on device performance has become a critical issue that needs further investigation with the shrinking of device dimensions[32]. Many of the previously developed physics-based compact models for GaN HEMTs consider these regions as constant resistances with the DC or AC drain current. However, experimental and simulation research reports showed a strong dependence of the series parasitic access region resistances on the channel current which is ascribed to the saturation of electron velocity in the access regions[33][34]. We have incorporated this effect in our *I-V* model-for optimal fitting of modeled devices *I–V* characteristics with experimental data, as done by Ghosh *et al.* [34]

$$R_{d/s} = \frac{R_{d0/s0}}{\left[1 - \left(\frac{I_{ds}}{I_{acc,sat}} \right)^{\beta a} \right]^{\frac{1}{\beta a}}} \quad (4.41)$$

where $I_{acc,sat}$ is the maximum/saturation current in access regions, $R_{d0/s0}$ is the access resistance at low drain current given by $L_{acc}/(Q_{acc}.\mu_{acc})$. L_{acc}, Q_{acc}, μ_{acc} are the access region length, access region charges, and carrier mobility, respectively whereas βa is an empirical fitting parameter.

■ Channel length modulation and Self-heating effects

Channel length modulation is one of the major short-cannel effects in FET device scaling It is the shortening of the channel due to the shift in the channel pinch-off region point towards the source at higher drain voltages. That decreases the effective device gate length and cause a rise in the drain-source current. We have incorporated this effect in our model based on the widely used expression $I_{ds}(1+\lambda\ I_{ds})$, where λ is the channel length modulation parameter[2][3].

Furthermore, devices may manifest a negative slope of I_{ds} in the output characteristics plot as V_{ds} increases into high power dissipation region. That is attributed to the so-called self-heating effect (SHE)-i.e., an increase in local temperature of the device to a value well above the ambient temperature during high-power operation. This effect is critical for GaN HEMTs as they are potential candidates for high-power applications and is considered in our model based on the approach explained in [2] and [3].

4.5 Device simulation and model validation

Derivation and validation of the threshold voltage models are implemented in a two-step process.

1) ***V_{th} parameter extraction:*** usually, the V_{th} of a conventional MOSFET device is defined as the gate voltage at which the device under study (DUT) enters from weak into strong inversion operating regime. Techniques such as constant current, first derivative, and linear extrapolation are developed to determine the parameter for device modeling. These methods rely on the static I_d–V_g measurement data obtained at a low drain bias point and offer simplicity. However, they may easily lead to an inaccurate parameter prediction when directly applied to HEMTs because of the high series parasitic resistances and mobility degradation effects exist in these devices[35]. Instead, the second derivative method-that evaluates the threshold voltage from the second derivative of drain current with respect to the gate voltage V_{gs} (i.e., $d^2I_{ds}/dV_{gs}{}^2 = dg_m/dV_{gs}$=)-is well-suited for unequivocal extraction of the parameter in GaN HEMTs as it is less sensitive to the drastic increase of access region resistances at high I_{ds} region. According to this method, the V_{th} corresponds to the gate voltage point at which the first peak of the transconductance derivative occurs[35][36]. The V_{th} value obtained this way from the linear regime drain current is used to verify the models' prediction, according to the DUT architecture, as illustrated in Figure 4.9.

2) ***Computation of n_0, E_d, and polarization induced charge:*** n_0 and E_d can be determined experimentally from the 2DEG properties of the device under study. One can extract the dependence of the n_s and ϕ_b on the Al mole fraction x of the barrier layer and calculate the corresponding n_0 and E_d values using the respective expressions of n_s and ϕ_b (depending on the device architecture). Previous studies of n_s and ϕ_b measurement data in GaN HEMTs reported a linear relationship of n_0 and E_d with the AlGaN layer Al composition, and N. Goyal *et. al.* defined this relation via[10][37]

$$\begin{aligned} n_0 &= (2.9x - 0.0893).10^{13} \quad cm^{-2}eV^{-1} \\ E_d &= (2.0x + 0.42) \quad eV. \end{aligned} \tag{4.42}$$

The expressions in (4.42) determine approximated values of the n_0 and E_d in bare surface heterostructures (structures without a gate metal). However, in practical HEMT devices, the deposition of the gate metal depletes a considerable amount of surface donor states[10]. Furthermore, if the barrier layer thickness for a given device is happened to be beyond the

calculated critical value (d_{crr}), a strain relaxation effect will be taken into account in the computation of the induced polarization charge as defined in (4.14). For these reasons, a slight tuning of the n_0 and E_d values calculated using (4.42) as well as the empirical s_{crr} parameter (if the barrier is proven to be relaxed) is necessary to determine the V_{th} parameter precisely.

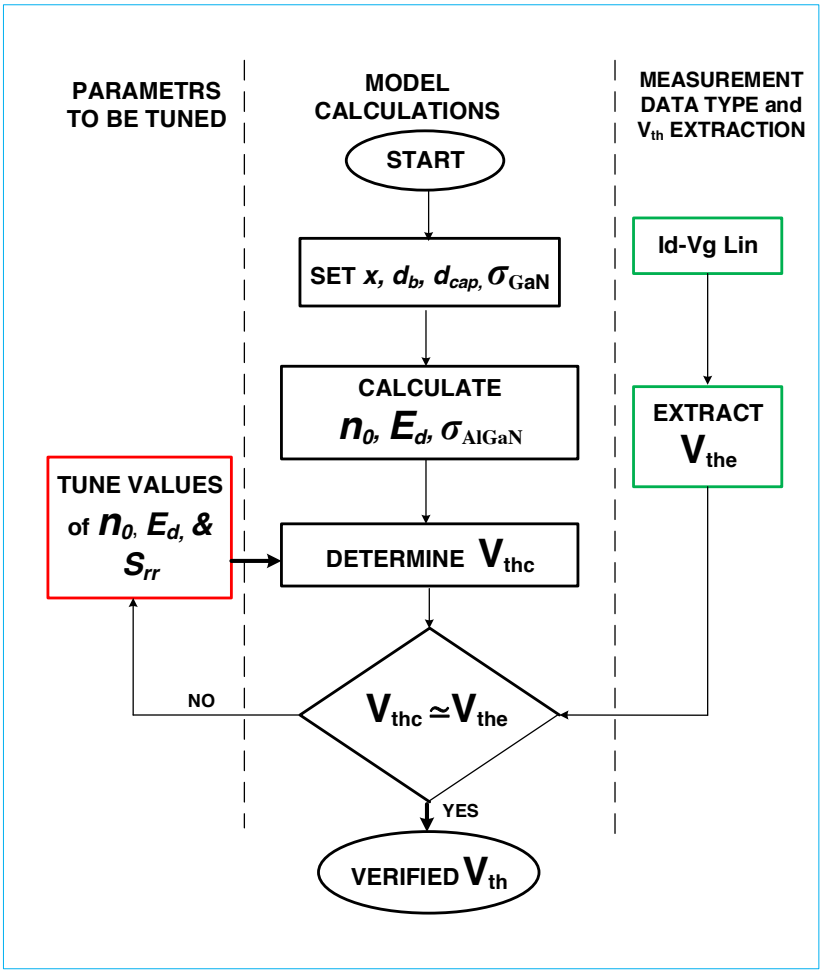


Figure 4.9 V_{th} calculation flow V_{thc} and V_{the} are the calculated and extracted threshold voltage values, respectively.(Reproduced from [26]).

For the validation of the proposed models, two groups of GaN HEMTs, coded from D_1 to D_6, have been employed in this work. The measurement data for the first collection of devices (D_1, D_3, D4, D_5, and D_6) are obtained from the literature, and TOSHIBA Corporation provided the experimental data for D2 as part of SiC-CMC ASM GaN HEMET model standardization process. This section intends to demonstrate the device simulation results and the model verification process.

The V_{th} parameter for each device is computed using the corresponding expressions ((4.22), (4.28), and (4.35)). Table 4.2 compares the performance of the models proposed in this work with the unified V_{th} model referring to values extracted from the corresponding transfer characteristics experimental data. A significant difference between predictions of the new and old expressions is observed, suggesting that the onset of strain relaxation in the barrier layer of

the devices as well as the presence of interfacial and cap layers nullifies the accuracy of the unified expression. Whereas, the new models predict values close to those obtained from the experimental data. The results are incorporated into the charge based *I-V* model, and standard simulation for *I-V* characteristics of HEMT devices has been performed. Model and device-related parameters such as gate length, *L*, width, *W*, barrier and cap layer thickness, d_{AlGaN} and d_{GaN}, and Al mole fraction, *x*, etcetera, are taken from the respective sources, and their values are summarized in Table 4.3.

Table 4.2 Comparison between the performances of proposed threshold voltage models with the widely used unified V_{th} expression

Transistors	*Device code*	*V_{th} values (V)*		
		Unified V_{th} expression	*Models proposed*	*Experimentally extracted V_{th}*
AlGaN/GaN	D_1	-6.9	-3.9	-4.0
AlGaN/GaN2	D_2	-12.8	-3.2	-3.4
GaN- AlGaN/GaN1	D_3	-4.3	-2.3	-2.2
GaN- AlGaN/GaN2	D_4	-8.7	-2.4	-2.3

■ Simulation results of I-V characteristics of AlGaN/GaN devices (D_1, D_2, and D_6)

The influence of intense strain relaxation is investigated through simulation of DC characteristics of AlGaN/GaN HEMT device (D_1) with 50% Al composition, and the results are illustrated in Figure 4.10 and Figure 4.11.

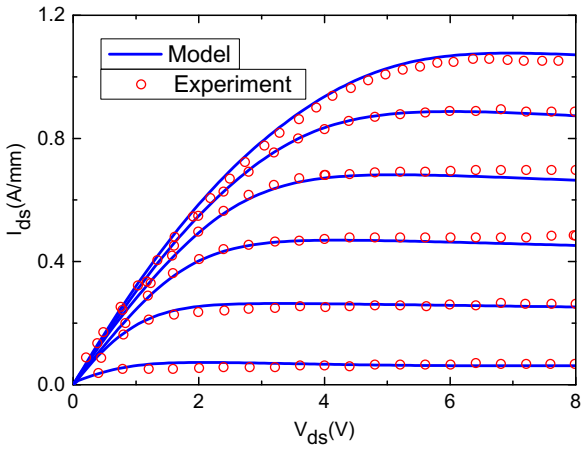


Figure 4.10 Output characteristics of $Al_{0.5}GaN_{0.5}$/GaN (D_1) with L = 0.7 µm and W = 25 µm, when V_{gs} varies from −3 to 2 at a step of 1 V (measurement data from [4]).

Given that the device has an 18 nm n-doped AlGaN layer with 0.5 Al mole fraction (the highest alloy composition compared to the other five devices considered in this work), the calculated critical barrier layer thickness for the onset of crystal dislocation is ≈8.6 *nm*. Thus, one can tell that the layer is under the influence of significant strain relaxation. The new V_{th} parameter is well predicted, which suggests that the impact of donor doping concentration and the high Al content are correctly considered in the proposed model (Table 4.2).

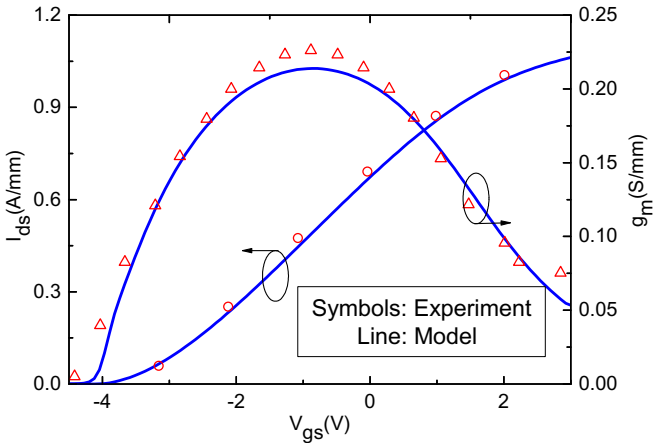


Figure 4.11 Transfer characteristics of $Al_{0.5}GaN_{0.5}/GaN$ (D_1) with L = 0.7 *μm* and W = 25 *μm,* at V_{ds}=4V (measurement data from [4]).

The *I-V* model returns results well matching with the measurement data over the full range of the applied biases. Apart from the severe strain relaxation, it can be noticed that the self-heating, channel length modulation, access region resistance, other short channel effects are negligible in this device. The results validate both the V_{th} and current models derived for the AlGaN/GaN structure for the case in which the HEMT device has high Al composition.

Measurement data provided by Toshiba Corporation enabled us to test the proposed V_{th} expression and the *I-V* model with a power $Al_{0.2}Ga_{0.8}N/GaN$ HEMT(D_2). The focus is a long channel device that has extended access regions and thicker barrier layer with moderate Al composition. The device has a 2 *μm*/14 *μm* long source/drain side gaps and a 30 *nm* thick partially n-doped (20 *nm*) AlGaN layer of 30% Al content. The critical barrier layer thickness for the crystal relaxation to start, in this case, is around 22 *nm*. It is apparent from the information that the strain energy stored in the barrier layer is lightly relaxed. Calculated V_{th} by considering the effect is equivalent to the value obtained from experimental data.

Plot of the variation of modeled I_{ds} with respect to V_{ds} is shown along with experimental data in Figure 4.12. Note that, at higher V_{gs} and V_{ds} values, I_{ds} tends to be non-responsive to significant additional changes in the applied biases. Similarly, an almost constant drain current is obtained in the high drain current region of the transfer characteristics as can be seen in Figure 4.13. Both effects reflect the substantial influence of high nonlinear access region resistances ($R_{d/s}$) at high drain current region.

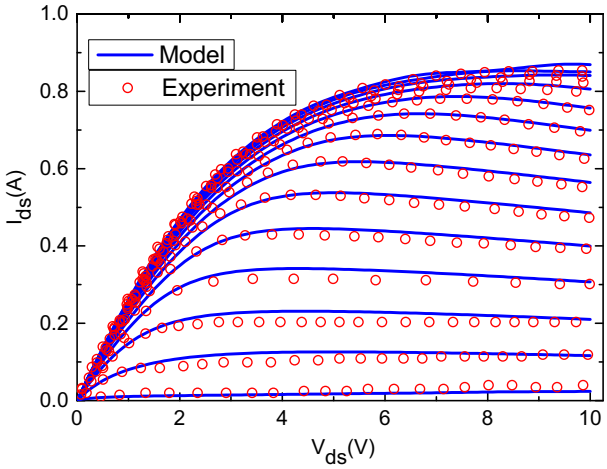


Figure 4.12 Output characteristics of MIS AlGaN/GaN HEMT with field plate structure. V_{gs} varies from −3.5 to 3 at a step of 0.5 V.

Furthermore, the transconductance (g_m) versus the gate voltage is investigated at different drain biases in Figure 4.13. The slope visibly changes in the high V_{ds} (10 V) plot- firstly, within the medium V_{gs} range which is attributed to the presence of self-heating effect, and secondly, at higher I_{ds}/V_{gs} values due to the dramatic increase in parasitic access region resistances with the current. The DC characteristics are correctly predicted over the explored range of biasing conditions, validating the *I-V*, *SHE* and the drain current-dependent nonlinear access region resistances modeling approaches adopted in this work. The result further verifies the V_{th} model ((4.22)) accuracy in predicting the parameter for a device which comprises a thicker AlGaN layer that is subjected to moderate strain relaxation.

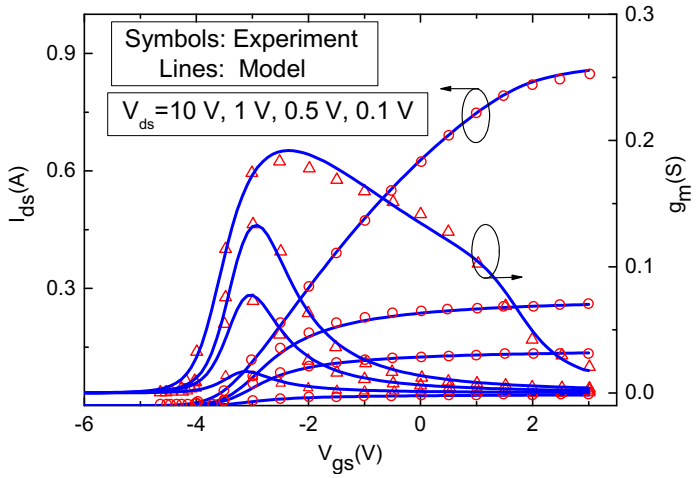


Figure 4.13 Transfer characteristics of MIS AlGaN/GaN power HEMT.

Table 4.3 List of device and model parameters

Model and Device parameters		Description	Devices			
			D_1	**D_2**	**D_3**	**D_4**
W (mm)		*Device width*	0.025	3	0.1	0.1
L (μm)		*Channel Length*	0.7	1	0.12	0.5
N_D $(\times 10^{-18} cm^{-3})$		*Barrier layer donor concentration*	2	2	-	-
d_{AlGaN} (nm)	d_i	*Undoped (spacer) barrier layer thickness*	3	30	12.5	22
	d_d	*Doped barrier layer thickness*	15			
d_{GaN} (nm)		*Cap layer thickness*	-	-	2	3
$-\sigma_{GaN}$ (C/m^2)		*GaN layer polarization*	0.029	0.029	0.029	0.029
E_d (eV)		*Surface donor level*	0.75	0.32	0.9	0.71
n_0 $(\times 10^{13})$ $(cm^{-2}eV^{-1})$		*Surface donor states density*	1.3	0.45	0.3	0.26
μ (m^2/Vs)		*mobility*	0.06	0.15	0.07	0.15
V_{sat} $(\times 10^7)$ (cm/S)		*Saturation velocity*	1.7	1.7	1.7	1.7
x		*Barrier layer Al composition*	0.5	0.2	0.26	0.22

In practice, current collapse or decrease in output power and power added efficiency occur in single channel AlGaN/GaN HEMTs due to the output current-swing compression caused by high-frequency large signal drive. Double channel HEMT devices are developed for mitigating such problems as they have better electric field and potential distribution. And, a robust physics-based compact model will allow better exploitation of the device in circuit design [30][38].

The V_{th} expressions derived for AlGaN/GaN and GaN/AlGaN/GaN structured and the charge based *I-V* model is adopted here for the simulation of the DC characteristics of sample DH-AlGaN/GaN HEMT (D_6) device. In this case, each channel is treated as a single HEMT transistor-labeled as T_1 and T_2 for clarity. The AlGaN layers in T_1 and T_2 have a 30% and 3–6% graded Al composition, and the corresponding critical thickness for the onset of strain relaxation are approximately15 nm and 78 nm, respectively. By comparing these d_{cr} values to the AlGaN layers actual thickness, one can find that the barrier layer in T_1 is partially relaxed. It is apparent from the data in Table 4.4 that the proposed models determine the parameters for both channels with better accuracy, proving the correct consideration of the effects of the strain relaxation in T_1 and the cap-layer in T_2.

The total I_{ds} in DH-HEMT device is evaluated as a sum of the individual Transistor drain-source current. Model and device geometrical parameters used in the DC characteristics simulation are listed in Table 4.4.

Table 4.4 List of model and device parameters for DH-AlGaN/GaN HEMT device (D_6)

Model and device parameters	*Device D_5*	*DeviceD_6*	
		T_1	*T_2*
W (mm)	1	0.1	0.1
L (μm)	0.35	1	1
μ (m^2/Vs)	0.2	0.18	0.18
V_{sat} (× 10^7) (cm/s)	1.7	1.7	1.7
d_{AlGaN} (nm)	20	24	21
d_{AlN} (nm)	1	-	-
x	0.3	0.3	0.03-0.06
n_0 (×10^{13}) ($cm^{-2}eV^{-1}$)	0.62	0.63	0.066
E_d (eV)	0.69	0.57	0.2
N_D (×$10^{-18}cm^{-3}$)	-	2	-
V_{th} (V) (model)	-3.41	-7.61	-4.0
V_{th} (V) (extracted)	-3.4	-7.6	-4.0

Figure 4.14 shows that the total drain-source current slightly varies with increasing the gate voltage up to 4V because the contribution in that range comes only from T_1. However, once the lower channel (T_2) comes into play at V_{gs}=4 V, the drain current increases significantly with the gate voltage. The behavior is further reflected as a hump in the transfer characteristics of the device in Figure 4.15. Moreover, the negative slope of I_{ds} at higher drain voltages manifests that the self-heating effect is intense when the two channels become operational. The excellent correlation between the model and experimental data obtained in the device DC characteristics verify the applicability of models of the V_{th}, *I-V* characteristics, and other additional effects for double channel HEMT devices.

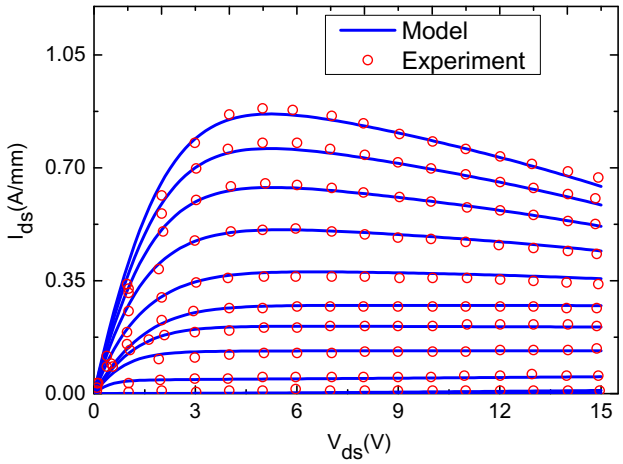


Figure 4.14 Output characteristics of DH-AlGaN/GaN (D_6) with L = 1 μm and W = 100 μm when V_{gs} was ramped from −9 to 1 at a step of 1 V (data from [38]).

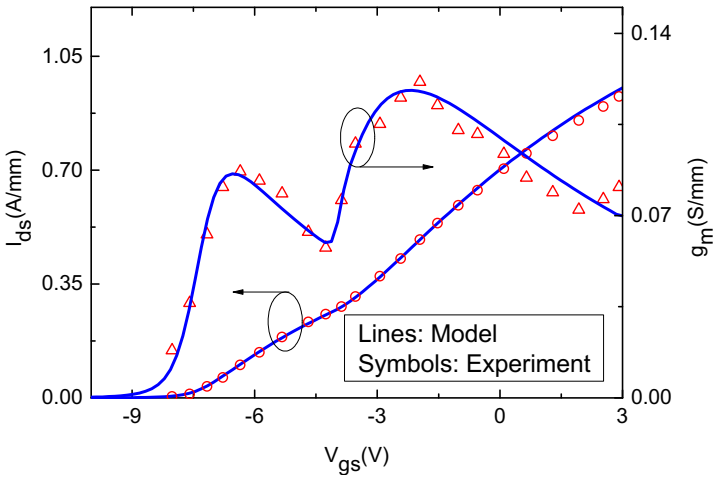


Figure 4.15 Transfer characteristics of DH-AlGaN/GaN (D_6) with L = 1 μm and W = 100 μm when at V_{ds}=10 V (data from [38]).

■ Simulation results of I-V characteristics of GaN/AlGaN/GaN devices (D_3 and D_4)

A further model performance test is performed by simulating a GaN/$Al_{0.26}GaN_{0.74}$/GaN HEMT (D_3). The device has a thin GaN-cap and an undoped AlGaN layer with Al content of 26%. The calculated critical thickness for crystal dislocation onset in the barrier layer is roughly 17 nm, which is greater than the 12.5 nm actual thickness. And, that signifies the AlGaN layer is fully strained. The calculated V_{th} parameter is approximately equal to the extracted value, confirming that the model accounted for the physical effect of the GaN-cap layer on surface donor density, and consequently, on the 2DEG concertation correctly.

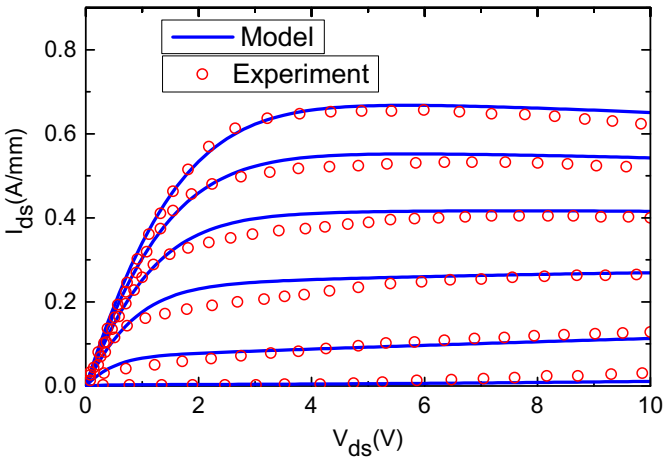


Figure 4.16 Output characteristics of GaN/$Al_{0.26}GaN_{0.74}$/GaN (D_3) with L = 0.12 μm and W = 100 μm when V_{gs} varies from −2.5 to 0 at a step of 0.5 V (data from [39]).

I-V characteristics simulation results are presented in Figure 4.16 and Figure 4.17, and it is apparent that the model reproduces the experimental data in the entire range of V_{gs} and V_{ds} with acceptable accuracy. The results demonstrated the solid physical foundation of the proposed V_{th} model developed for GaN/AlGaN/GaN structure and the *I-V* model. They also validated the models for the case that short channel and access region resistance effects are minimum.

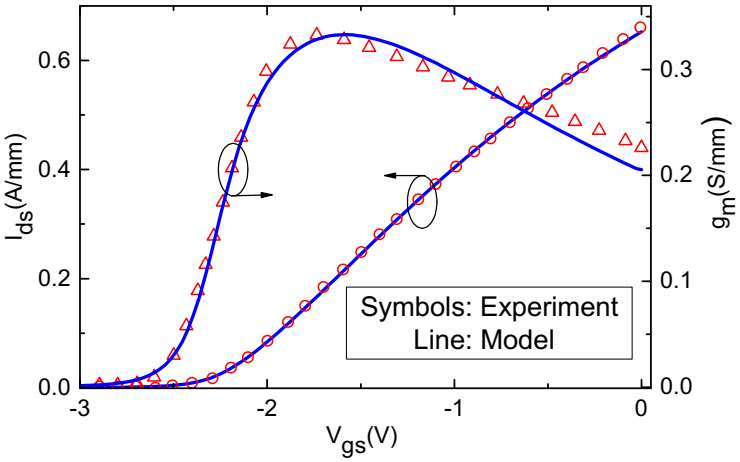


Figure 4.17 Transfer characteristics of GaN/$Al_{0.26}GaN_{0.74}$/GaN (D_3) with L = 0.12 μm and W = 100 μm at V_{ds}=4V (data from[39]).

The influence of cap layer thickness is further investigated through simulation of *I–V* characteristics of a GaN/$Al_{0.22}GaN_{0.78}$/GaN device (D_4) with a thick GaN-cap layer compared to the previous device (D_3). Model–experimental data (obtained at 425 K) comparison results are presented in Figure 4.18 and Figure 4.19. With the given layer dimensions and Al composition of the AlGaN layer, calculated critical thickness d_{cr} is ≈20 nm, and the strain relaxation effect is found to be moderate in this case.

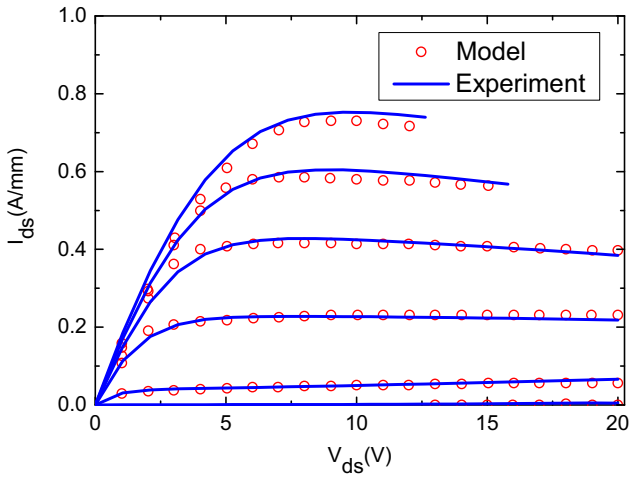


Figure 4.18 Output characteristics of GaN/$Al_{0.26}GaN_{0.74}$/GaN (D_4) with L = 0.5 µm and W = 100 µm when V_{gs} varies from −3 to 2 at a step of 1 V (data from [40]).

The computed V_{th} is comparable to the value extracted from the experimental data (Table 4.2). That demonstrates the proper incorporation of the surface donor density and 2DEG concentration dependencies on the Al mole fraction and cap layer thickness in the model proposed for GaN/AlGaN/GaN HEMT devices.

The output characteristics plot manifests the presence of pronounced self-heating effect (SHE) with a negative I_{ds} slope at higher V_{ds}, as seen in Figure 4.18. The I_{ds} quasi-saturation behavior observed in transfer characteristics of the device at high V_{gs} values is also indicative of a similar effect. Once again, the model agrees well with the experimental data in the explored range of biasing conditions and validates the adopted *I-V* and SHE models.

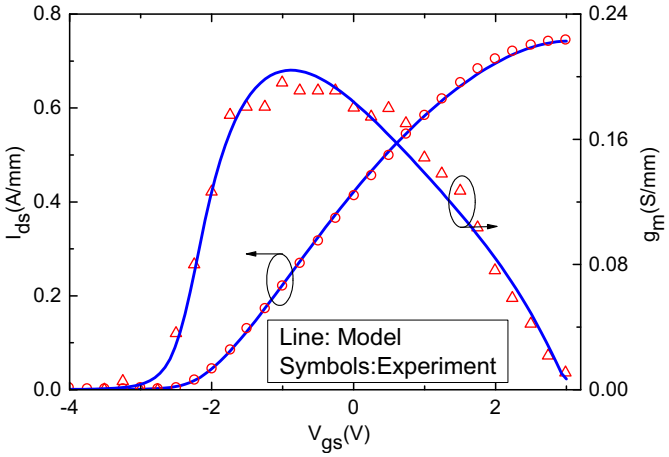


Figure 4.19 Transfer characteristics of GaN/$Al_{0.26}GaN_{0.74}$/GaN (D_4) with L = 0.5 µm and W = 100 µm at V_{ds}=7V (data from [40]).

■ Simulation results of I-V characteristics of AlGaN/AlN/GaN devices (D5)

Finally, yet importantly, the V_{th} model derived for AlGaN/AlN/GaN HEMT configuration is validated using simulation of a device that has a 21 *nm* and 1 *nm* thick barrier and AlN layers, and other geometrical features listed in Table 4.4. It is found that the actual AlGaN layer size exceeds the 14 *nm* calculated barrier layer critical thickness (for 30% Al content). As a result, the strain energy is partially relaxed. While the V_{th} model correctly predicted the parameter, the *I-V* model reproduced the experimental data with an acceptable level of accuracy (Table 4.4, Figure 4.20, and Figure 4.21). The access region resistances influence on the drain current can be observed in the DC plots wherein the current is found to be less responsive to the significant variation of terminal voltages at higher bias regions. The results suggest that effects of the AlN interlayer and strain relaxation, as well as access region resistances, are well considered in the V_{th} model proposed for the specified HEMT architecture and the *I-V* model, respectively.

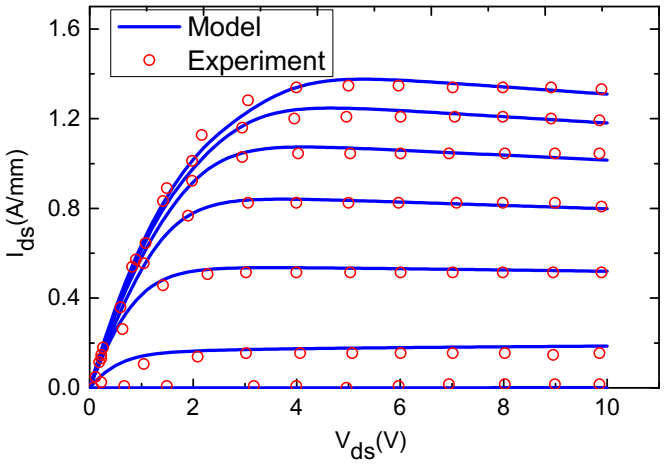


Figure 4.20 Output characteristics of $Al_{0.7}GaN_{0.7}$/AlN/GaN (D_5) with L = 0.35 μm and W = 1mm (V_{gs} starts: 2 V, step: 0.5 V) (data from [41]).

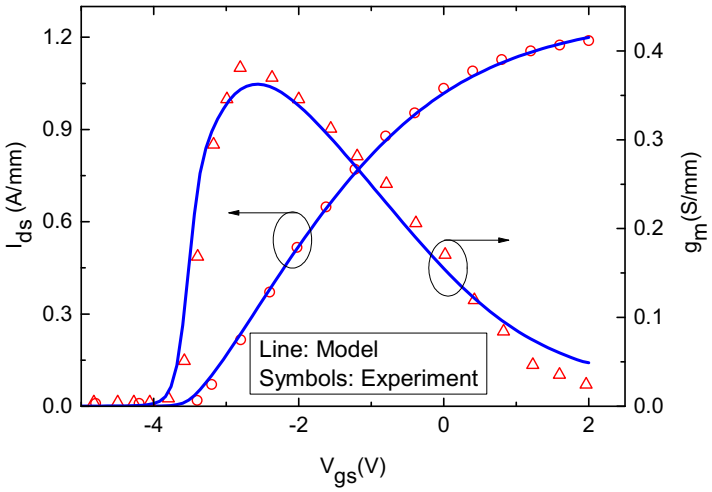


Figure 4.21 Transfer characteristics of $Al_{0.3}GaN_{0.7}$/AlN/GaN (D_5) with L = 0.35 μm and W = 1 mm at V_{ds}=3V (data from [41]).

4.6 Conclusions

In this chapter, physics-based modeling of piezoelectric effect in GaN HEMTs is presented. The model is developed based on the analysis of electrostatics of the barrier layer and the assumption that surface donor states are the origin of electrons confined in the quantum well created at the interface. An analytical expression for the Schottky barrier height ϕ_b is derived based on the condition of charge neutrality across the barrier and other additional layers (if present) and used in the development of the V_{th} models. Effects of introducing a GaN-cap and AlN interfacial layers on the distribution of surface donor states and the influence of strain relaxation due to high barrier layer Aluminum composition are considered in the derivation of the models. Having the V_{th} models integrated in a charge based compact current model

previously proposed by our group, simulation of *I-V* characteristics of GaN-based HEMTs with practical Al composition and barrier layer thickness was carried out. And, the modeled-experimental data comparison to validate the models yields well matching results in all cases.

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5. Conclusions

■ Conclusions

The primary objective of the thesis was electrical characterization and physically-based modeling of amorphous InGaZnO (a-IGZO), polymeric organic TFT, and GaN-based HEMT devices. The most significant results are: 1) A-IGZO and organic polymer-based TFT devices have been characterized, and the physical origination of 1/f noise in the respective devices has been identified. 2) DC and Flicker noise model that is valid for all regimes of device operation was developed for the a-IGZO TFTs and verified with experimental data obtained at different temperatures. Finally, simple analytical expressions for the threshold voltage of GaN-based HEMTs have been derived. Model accuracy was proved to predict the V_{th} parameter for practically available architectures of HEMT devices.

DC and LFN characterization for a-IGZO TFTs devices with a thin channel layer (12 nm thickness) and an etch stop structure was performed over a broad range of biasing, at different operating temperatures. The *I-V* experimental data analysis unveiled that the devices experienced a positive shift in their threshold voltage during the measurement of the transfer characteristics from linear to saturation regimes. Whereas, the subthreshold slope remains unchanged. Firstly, the stress caused to devices because of a higher drain voltage applied in earlier measurements could result in the threshold voltage change in subsequent measurements. Secondly, the densely deep tail states available in the a-IGZO layer can behave as acceptor-like dopants, whereby a large number of carriers might be trapped by these states, and in turn, contribute to the threshold voltage shift. Additionally, increasing trends field effect mobility and drain current with temperature are observed in the investigated devices. Such effects proved that variable range hopping is the primary carrier transport mechanism within the explored range of operating conditions. It is found that the threshold voltage-temperature dependence governs the change in drain current with the rise in operating temperature in all device samples.

Concerning the 1/f noise property of the ESL a-IGZO devices, the experimental data shows a $1/f^{\gamma}$ behavior with γ values between 0.9 and 1.1. Further analysis of the data indicated that the carrier number fluctuation due to the trapping/de-trapping of charge carriers by interfacial oxide traps is the physical origin of the measured 1/f noise. Noise contribution from correlated mobility fluctuation due to remote Coulomb scattering of carriers is also observed at high drain current regions. However, the contact resistances do not play a part in the noise generation. It is found that more interface traps responsible for the measured LFN get activated at particular biases during high temperature operations. Based on these findings, a Flicker noise model was derived using the UMEM technique for DC parameter extraction and carrier number fluctuation-correlated mobility fluctuation (CNF/CMF) 1/f noise modeling approach. The

model is validated for all operating regimes in the considered range of temperature through comparison to the measurement data.

Characterization of the polymeric OTFTs revealed that the devices exhibit attractive electrical properties. Improved carrier mobility is observed, which might be attributed to the excellent pretreatment of the gate insulator to form a high- quality interface with the channel material, and positively influence the formation of grains by passivating defects or contaminants created during device processing. The non-fluorinated dielectrics brought about eminent ease of device printability on flexible substrates during processing, a feature the present-day electronics industry hugely acknowledges for low-cost fabrication of high-performance OTFT devices. Analysis of the noise measurement taken over a broad range of bias unveiled a clear $1/f^{\gamma}$ noise behavior with the exponent close to unity. Similar to the a-IGZO devices, carrier number fluctuation was found to be the source of 1/f noise in these devices. Small deviations from the 1/f behavior are observed at low frequencies and high gate voltages, which might be attributed to the availability of a limited number of slow traps deep in the oxide at that particular biases. The interface trap density extracted from Flicker noise experimental data is comparable to values obtained in classical MOSFETs (with the magnitude in the order of 10^9 $cm^{-2}eV^{-1}$). That proved the high quality and excellent repeatability of the dielectric/channel interface across all OTFTs in the sample.

Finally, AlGaN/GaN *I-V* model developed previously by our group was extended in this doctoral study to include the piezoelectric and other important physical effects. Polarization dependent analytical Schottky barrier and threshold voltage expressions were developed and implemented in the charge-based DC model. The influence of strain relaxation due to high Al content of the barrier layer and the effect of insertion of a GaN-cap and AlN interfacial layers on device performance were considered. Furthermore, other significant physical effects common to GaN HEMTs were included. *I-V* characteristics of devices with different architectures, geometric dimensions, Al mole fraction, and AlGaN thickness were simulated for model validation. It is found that the V_{th} expressions can predict the parameter for all devices in the sample precisely. Moreover, *I-V* model validation was carried out with comparison to experimental data over different bias range, and excellent agreement was obtained, which is important to compact physics-based models.

■ Future work

Field effect transistors are continually evolving in many aspects, on one hand, by optimization of device processing technologies and, on the other, through the adoption of new advancements made in the field of material science. Thus, compact device models should be updated on a regular basis. So, they can keep pace with the fabrication dynamics and ensure proper exploitation of the emerging/improved devices in circuit design. Having that in mind, the following future works are suggested.

- Concerning the ESL a- IGZO TFTs, a comparative study on the performance of devices from different technologies can help to gain insight into the enhancements that a particular technology has brought about on device performance, reliability, longevity, etcetera. Such investigation is essential for understanding the impact of different ESL layers on noise performance and electrical properties of the devices. Characterization of the ESL a-IGZO TFTs at operating temperatures above 333 K are also interesting to identify if a further increase in temperature will invoke a change in conduction mechanism and impact the DC and noise performance of the devices in question.
- Regarding the polymeric OTFT devices characterization, it is crucial to further scrutinize both the DC and low-frequency performance of devices at high and low-temperature operation. As a result, the relation between the device figures of merit and operating temperature can be investigated. Subsequently, detailed modeling the 1/f noise characteristics valid for all regimes of device operation and over a practical range of operating temperature can be done.
- Polarization in GaN-based HEMTs has been long debated. A comprehensive review of previous and newly available polarization models will be significant for the improvement of model simplicity and accuracy. Furthermore, a measurement technique or a model developed to determine the density of surface states (sources of 2DEG) in GaN HEMTs will be a definite plus to enhance the V_{th} models proposed in this thesis.