UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH

Real-time digital signal processing for new wavelength-to-the-user optical access networks

Saeed Ghasemi

UNIVERSITAT POLITÈCNICA
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PhD Thesis

Real-Time Digital Signal Processing for new Wavelength-to-the-user Optical Access Networks

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To my beloved wife Fatima

Abstract

Nowadays, optical access networks provide high capacity to end users with growing availability of multimedia contents that can be streamed to fixed or mobile devices. In this regard, one of the most flexible and low-cost approaches is Passive Optical Network (PON) that is used in Fiber-to-the-Home (FTTH). Due to the growing of the bandwidth demands, Wavelength Division Multiplexing (WDM), and later on ultra-dense WDM (udWDM) PON, with a narrow channel spacing, to increase the number of users through a single fiber, has been deployed.

The udWDM-PON with coherent technology is an attractive solution for the next generation optical access networks with advanced digital signal processing (DSP). Thanks to the higher sensitivity and improved channel selectivity in coherent detection with efficient DSP, optical networks support larger number of users in longer distances.

Since the cost is the main concern in the optical access networks, this thesis presents DSP architectures in coherent receiver (Rx), based on low-cost direct phase modulated commercial DFB lasers. The proposals are completely in agreement with consept of wavelength-to-the-user, where each client in optical network is dedicated to an individual wavelength.

Next, in a 6.25 GHz spaced udWDM grid with the optimized DSP techniques and phase-shift-keying (PSK) modulation format, the high sensitivity is achieved in real-time field-programmable-gate-array (FPGA) implementations.

Moreover, this thesis reduces hardware complexity of optical carrier recovery (CR) with two various strategies. First, based on differential m^{th}-power frequency estimator (FE) by using look-up-tables (LUTs) and second, LUT-free CR architecture, with optimizing the power consumption and hardware resources, as well as improving the channel selectivity in terms of speed and robustness.

Furthermore, by designing very simple but efficient clock recovery, a symbol-rate DSP architecture, which process data using only one sample per symbol (1-sps), for polarization diversity (POD) structure, becomes possible. It makes the DSP independent from state-of-polarization (SOP), even in the case of low-cost optical front-end and low-speed analog-to-digital converters (ADCs), keeps the performance high as well as sensitivity in real-time implementations on FPGA.

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Contents

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Abbreviations & Acronyms

ADC	-	Analog-to-Digital Converter
ASIC	-	Application-Specific Integrated Circuit
AFC	-	Automatic Frequency Control
BD	-	Balanced Detector
BER	-	Bit Error Rate
BERT	-	Bit Error Rate Tester
Carry4s	-	Carry Logics with Look Ahead
CD	-	Chromatic Dispersion
Clk Rec	-	Clock Recovery
CMA	-	Constant Modulus Algorithm
CR	-	Carrier Recovery
DAC	-	Digital-to-Analog Converter
DFB	-	Distributed Feed-Back
DMP	-	Differential M^{th} -Power
DS	-	Downstream
DSP	-	Digital Signal Processing
ECL	-	External Cavity Laser
EQ	-	Equalizer
EPON	-	Ethernet PON
FASN	-	Full-Service Access Network
FC	-	Frequency Compensation
FE	-	Frequency Estimator
FEC	-	Forward-Error Correction
FF	-	Flip Flops
FFT	-	Fast Fourier Transform

FIR	-	Finite-Impulse Response
FPGA	-	Field-Programmable-Gate-Array
FTTH	-	Fiber-To-The-Home
FTTx	-	Fiber-To-The-x
FWHM	-	Full-Width at Half Maximum
GPON	-	Gigabit-capable PON
GVD	-	Group Velocity Dispersion
I	-	In-Phase
IF	-	Intermediate Frequency
ITU	-	International Telecommunication Union
LMS	-	Leas Mean Square
LO	-	Local Oscillator
LOSPR	-	LO-to-Signal-Power-Ratio
LTI	-	Linear Time-Invariant
LUT	-	Look-Up Table
LUT-FF	-	Lookup Table Flip Flop pairs
MM	-	Mueller-Muller
MMCM	-	Mixed Mode Clock Manager
MMSE	-	Minimum Mean Squared Error
MUX	-	Multiplexer
NGPON	-	Next Generation PON
NRZ-PRBS	-	Non-Return-to-Zero Pseudo Random Binary Sequences
OLT	-	Optical Line Terminal
ONU	-	Optical Network Unit
OOK	-	On-Off Keying
OPLL	-	Optical Phase-Locked Loop
P2P	-	point-to-point
Q	-	Quadrature
RAM	-	Random Access Memory

RC	-	Resistor-Capacitor
Ref	-	Reference
RF	-	Radio Frequency
RMS	-	Root Mean Square
Rx	-	Receiver
SIR	-	Signal-to-Interference
SMF	-	Single Mode Fiber
SOP	-	State-Of-Polarization
SRL	-	Shift Register Lookup table
SED	-	Sampling-Phase Error Detector
Rb	-	Symbol Rate
Rs	-	Sample Rate
SP	-	Single Polarization
TDM	-	Time Division Multiplexing
TED	-	Timing Error Detector
TIA	-	Trans-Impedance Amplifier
Tx	-	Transmitter
TWDM	-	Time and Wavelength Division Multiplexing
ud	-	ultra-dense
udWDM	-	ultra-dense Wavelength Division Multiplexing
US	-	Upstream
VCO	-	Voltage-Controlled Oscillator
VOA	-	Variable Optical Attenuator
WDM	-	Wavelength Division Multiplexing

Symbols

T_{ADC}	-	ADC Sampling Period
DS_I	-	Amount of Shifting
ω_{LO}	-	Angular Frequency of Local Oscillator
ω_s	-	Angular Frequency of Transmitted Signal
N_T	-	Averaging Length
ϕ_c	-	Carrier Phase
$u_{I/R}$	-	Coefficients to Recover the Sign of Phase Shift
A_{LO}	-	Complex Amplitude of Local Oscillator
A_s	-	Complex Amplitude of Transmitter
J	-	Cost Function
z^{-P}	-	Delay in Symbols
D	-	Dispersion Parameter
e	-	Electron Charge
$h_{xx/xy/yx/yy}$	-	Equalizer Coefficient of xx/xy/yx/yy
ε	-	Error Function
$\varepsilon_{LMS/CMA}$	-	Error Function of LMS/CMA algorithm
L	-	Fiber Length
τ	-	Fractional Delay
Δf	-	Frequency Error
E_P	-	Gardner Power-Based TED
E_G	-	Gardner TED
r_H	-	Horizontal Signal
Im	-	Imaginary
h	-	Impulse Response of Radio Frequency

ω_{IF}	-	Intermediate Frequency
μ	-	Iteration Factor
$\Delta\nu$	-	Linewidth
P_{LO}	-	Local Oscillator Power
E_{LO}	-	Local Oscillator Signal
b	-	Mathematical Function
f	-	Mathematical Function
g	-	Mathematical Function
ω_b	-	Modulation Bandwidth
m	-	Number of Constellation Points
N_{Taps}	-	Number of Filter Taps
N_S	-	Number of Samples
N_{Sym}	-	Number of Symbols
δ	-	Phase Difference
ϕ_{pn}	-	Phase Noise
ϕ_{LO}	-	Phase of the Local Oscillator
ϕ_s	-	Phase of the Received Signal
$\Delta\varphi$	-	Phase Shift
$\hbar$	-	Planck's Constant
P_H	-	Power of Horizontal Signal
P_V	-	Power of Vertical Signal
α_p	-	Power Ratio
η	-	Quantum Efficiency
Re	-	Real
P_s	-	Received Power
R	-	Responsitivity
k	-	Sample Index
R_S	-	Sample Rate

ε_τ	-	Sampling-Phase Error
c	-	Speed of Light
R_b	-	Symbol Rate
E_s	-	Transmitted Signal
r_V	-	Vertical Signal
λ	-	Wavelength

Chapter 1. Introduction

Optical communication was introduced by Charles Kuen Kao in 1960s, when he discovered certain physical properties of glass which laid the basis for high-speed data transmission [1]. Kao realized that a string of thin fiber is capable of carrying huge amount of information over long distance with few light energy, an alternative for copper in telecommunication technology. For stablishing a new perspective in the information and communication age, he received Nobel Prize in Physics in 2009.

Nowadays, optical access networks provide high capacity to end users with growing availability of multimedia contents that can be streamed to fixed and mobile devices. In this regard, one of the most flexible and low-cost approaches is Passive Optical Network (PON) that is used in Fiber-to-the-x (FTTx), where x = H, for home, B for building, C for curb and N for node [2]. Usually, a PON has a point to multipoint topology, to make connection between Optical Line Terminal (OLT), and Optical Network Unit (ONU) in the customer side.

FTTH increases the user bandwidth to tenths/hundreds of Mbps bidirectionally, as Jacob Nielsen in 1998 predicted that average bandwidth per user increases 50 % per year [3]. Figure 1.1 shows the Nielson's law for bandwidth demand per year.

With the fiber reaching the user premises, and the bandwidth demands exponentially increasing even beyond 100 Mbps per user that today PON systems can hardly offer, telecom operators require an unconstrained upgrade path and set the next generation PON systems. They will benefit from the huge potential bandwidth of the installed

fiber. Different upgrading technologies are being proposed by industry, research institutions and standard organizations, mostly defined by their point-to-multi-point multiplexing form. But the current time division multiplexing (TDM) equipment, mostly based on GPON or EPON, will not be able to deal with the expected demands of the following years. It is so that wavelength division multiplexed PONs (WDM-PONs) will have to be sooner or later deployed [4]. Certainly, WDM-PONs enable service providers to offer dedicated wavelengths straight to business as well as to residential customers, using the existing optical backbone. However, there are two key requirements that will make the WDM-PON successful. First, applying the low-cost devices is mandatory, i.e. devices that can be low-cost to a wide percentage of end users, especially at the end-user side, but also at the central office that must be identical and have a typical cost level of consumer electronics. Secondly, whole upgrading of TDM-PONs must be attained, with compatibility with existing network infrastructure [5].

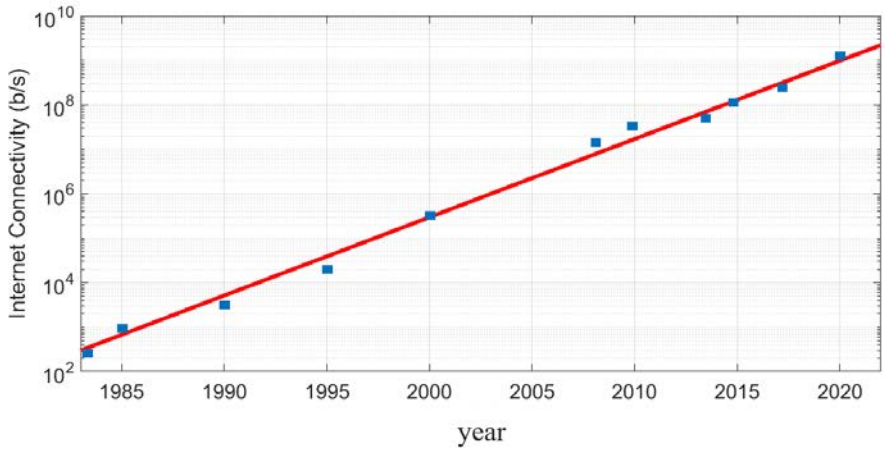

Figure 1.1: Nielsen's law prediction for internet bandwidth, growing 50 % per year.

The standardization of next generation optical access networks operating at over 10-Gbit/s has started to consider more flexible network configuration using WDM and to respond to those demands, Time and Wavelength Division Multiplexing (TWDM-PON) merge as one of the most promising PON solutions in which each wavelength

is shared between multiple ONUs by using TDM mechanism to provide high capacity and supply the bandwidth demand of broadband services. Recently, the FSAN access standardization group has started working on a new international standard, the ITU-T G.989: General requirements for 40-Gigabit-capable passive optical networks (NG-PON2) that, for the first time, considers WDM as the upgrade path, although with very few channels [6]. It has been suggested that optical coherent technologies, similar to those recently developed for the core networks, could be used to enhance the power budget [7], [8]. However, the expensive optical and electronic components do not simply reduce in cost to be low-cost for access networks.

1.1 Thesis Objectives

The scope of this thesis is to focus on two aspects. First is to design, develop and implement a DSP for coherent system with high-sensitivity and fine wavelength selectivity. Then, without losing the performance and high-spectral efficiency, to reduce hardware and DSP complexity and costs as well as the required electronics. This thesis aims to design a new class of DSP for coherent receivers enabling the use of:

- Low-cost lasers such as distributed feed-back (DFB) lasers, rather than expensive low linewidth tuneable external cavity laser (ECL) [9].
- Direct laser modulation analogue processing for reliable and low-latency real-time operation.
- Low-cost receiver front-end optical couplers such as 3×3, rather than 90° hybrids [10], [11].

This new class of DSP initially was designed, developed and implemented in the COCONUT project [12], which demonstrated a low power consumption in comparison with other coherent technologies [13], [14]. Then, was extended and improved with higher performance, lower power consumption, more sensitivity, and higher speed of signal processing [15], [16], [17], [18] as well as simpler electronics

with lower speed analog-to-digital converter (ADC) [19]. Therefore, the main objectives of this thesis are classified as follows:

- *General Objectives*

- Implementation of the wavelength-to-the-user concept as the enabler for the more general goal of offering gigabits-to-the-user flexibly.
- Improvement of electrical bandwidth utilization efficiency, since the user transmits, receives and processes only the own information; this does not happen in current TDM-PON networks.
- Lower energy consumption, due to the fact that it is proportional to the bit rate and we do not have to share it, and optical spectrum efficiency, because of optical channels at 6.25 GHz spacing, thanks to the coherent detection, instead of the current 100 GHz or 50 spacing. In this manner, we can increase the number of channels and users in about one order of magnitude.
- Longer distance reach, thanks to the much better receiver sensitivity of coherent detection and their capability of fully compensating the dispersion effects of the optical fiber by DSP; distances longer than 100 Km at 1.25 Gbps, will be validated for the rural and wide metro scenarios.
- Higher number of users as the splitting ratio can be increased due to the 10-20 dB sensitivity improvement and the higher wavelength selectivity mentioned due to the coherent homodyne detection. The number of users can be increased from 64 to 256 at least.
- To reduce hardware cost as complex optical devices will be avoided, and simple conventional DFB lasers and receiver front-end based on 3×3 couplers.

- *Specific Objectives*

- The DPSK signal at 1.25 Gbps will be detected by the phase-diversity receiver based on a 3×3 coupler, and the sensitivity of -55 dBm at BER = 10^{-3}, with an

ultra-narrow channel spacing of only 3 GHz. This will enable us to safely use a 6.25 GHz spacing.

- To propose new carrier recovery (CR) architectures in the DSP subsystems for dynamic compensation of local oscillator (LO) frequency drifts, phase noise and dispersion effects; we will develop and implement two different kinds of CRs, for field programmable gate array (FPGA) implementations in real-time signal processing.
- To propose a novel DSP architecture for low-cost polarization-independent detection using a simple clock recovery; we will demonstrate a symbol-rate DSP for coherent intradyne M-PSK receivers that uses only one sample per symbol (1-sps) data processing.
- To examine our proposals in the real-time experimental set up with FPGA implementation of the proposed DSP algorithms and subsystems; all the applications will be implemented in the real-time and completely practical scenarios, rather than simple simulations.

1.2 Thesis Outline

All the mentioned objectives and concepts in this thesis will be analysed in 6 chapters as follows:

In chapter 2, a general idea of state-of-the-art of optical access networks, including an ultra-dense (ud) WDM-PON architecture for future optical access networks will be discussed. Then, coherent detection with the main subsystems including optical front end, and the DSP will be introduced. This chapter provides an overview of the DSP subsystems for the coherent receivers, and explains the task of each block with different schemes and algorithms from previous works.

Chapter 3, presents implemented DSP subsystems for the coherent receivers and proposes an optimized CR with real-time FPGA implementation to evaluate the performance of the proposal.

In chapter 4, another optimized CR for optical intradyne receivers with DPSK data will be proposed and will be implemented on FPGA for real-time evaluation.

Chapter 5 will propose a symbol-rate DSP based on proposed architectures for polarization-diversity (POL) PSK receivers, which makes data processing using only 1-sps. The real-time FPGA implementation will assess the proposed DSP and will show that there is not any penalty between the processing based on 1-sps and 2-sps.

Finally, the conclusion chapter will summarize the work and a prospective future research line to continue this topic will be presented.

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Chapter 2. State of the Art: Optical Access Networks

2.1 Active and Passive Optical Networks

There are two major types of network architectures in optical access, active optical network (AON) and passive optical network (PON). AON is also known as active Ethernet or point-to-point (P2P) Ethernet [1], that each user has his own dedicated OLT on an optical connector. An AON, uses electrically powered switching devices, such as switch aggregator or router to manage signal distribution and route data to specific parts [2]. On the other hand, a PON only uses fiber and passive components such as optical splitters to separate and collect optical signals as they move through the network and it is point-to-multipoint solution. In this regard, being low-cost with efficient energy consumption is its advantages over AON, while higher bandwidth per port is possible by AON, due to dedicated port to each user.

2.1.1 Time Division Multiplexing PON (TDM-PON)

Gigabit-capable PON (GPON) and Ethernet PON (EPON), are the low-cost solutions in the PONs, and based on time division multiplexing (TDM), on-off keying (OOK) modulation format in direct detection optical transceivers. In 2000s, International Telecommunication Union (ITU)-T and full-service access network (FASN) defined next generation PONs (NGPONs), which is also low cost and compatible with

existing technology [3]. Figure 2.1 shows the TDM-PON architecture, where different packet colours are corresponding to each ONU. The current TDM equipment, mostly based on GPON or EPON, will not be able to handle the expected demands of the internet connectivity for the following years. It is so that Wavelength Division Multiplexing PONs (WDM-PONs) was eventually deployed [4].

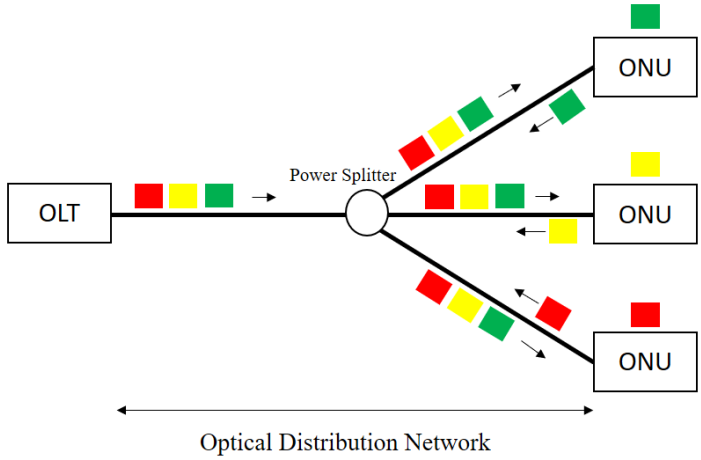

Figure 2.1: TDM-PON architecture.

2.1.2 Wavelength Division Multiplexing PON (WDM-PON)

The advanced applications need more transmission requirements, thus, other options to TDM-PON is WDM-PON. The WDM-PON is a technology and an innovative concept for access and backhaul networks that significantly can enhance the carrier infrastructures. It applies different wavelengths over a physical point-to-multipoint fiber that contains only passive components (PONs). Then, each wavelength is dedicated to an individual home or user, provides customers with the benefit of low fiber counts, resulting in low-cost services. Figure 2.2 shows the WDM-PON architecture, with different wavelengths that are dedicated to each user.

All the concept and research as well as system implementations in this thesis are based on WDM-PON.

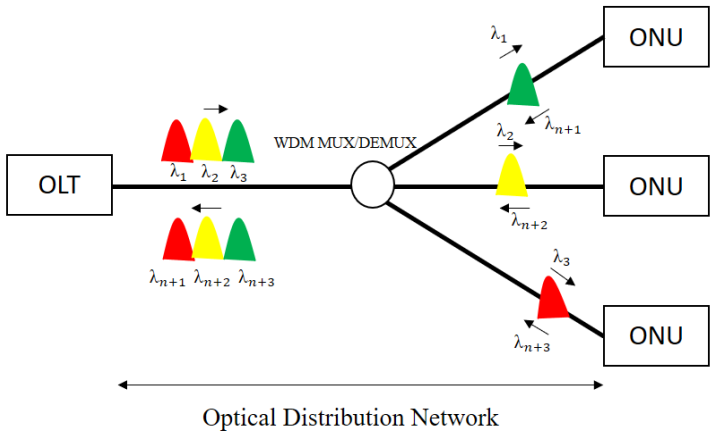

Figure 2.2: WDM-PON architecture.

2.1.3 Ultra-Dense Wavelength Division Multiplexing PON (udWDM-PON)

A significant step to upgrade the WDM-PON is ultra-dense WDM (udWDM) PON, with a narrow channel spacing, is a developing access network that allows increasing the number of optical carriers (channels) through a single fiber and large number of connected users to the network. In udWDM-PON each user is assigned by two wavelengths to cover both upstream (US) and downstream (DS) directions. The udWDM method can be used in infrastructure of current PONs, and different applications such as mobile back-haul and fixed-line users, over the same fiber. Figure 2.3 shows an udWDM-PON architecture, with coherent transmission, elastic spectrum and flexible hardware through the European COCONUT project [5].

The coherent technologies are commonly applied in core networks, and can be used to enhance the power budget and capacity of PONs. The main problem is that expensive optical and electronic components do not simply implemented for access networks, whereas the coherent system must be commercially compatible with cost-effective devices and electronics [6], [7]. In the following, the coherent detection system with the basic theories and the principle subsystems to be applied in udWDM-PON, will be discussed.

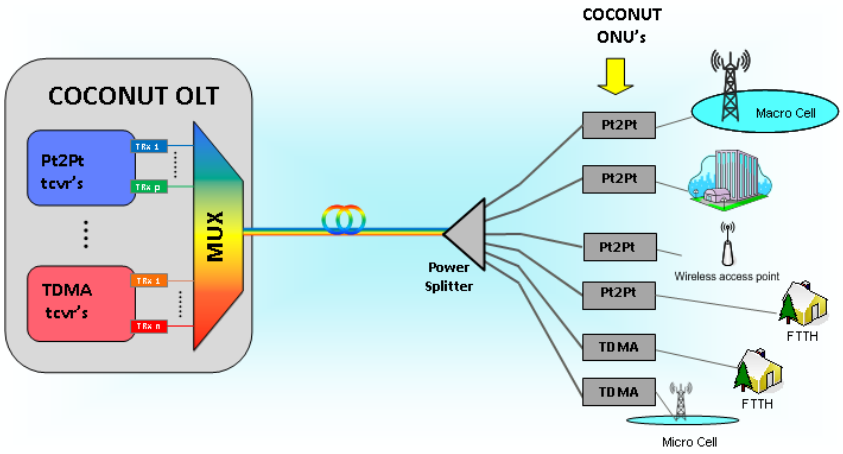

Figure 2.3: udWDM-PON application.

2.2 Coherent Detection

The main supporting technology for the udWDM-PON is coherent transmission to achieve high spectral efficiency whereas the power efficiency is being maximized using in-phase (I) and quadrature (Q) signals in the two fields of polarization. Figure 2.4 shows the architecture of the coherent receiver to get the electric fields of the modulated signal from the transmitter (Tx) and the LO.

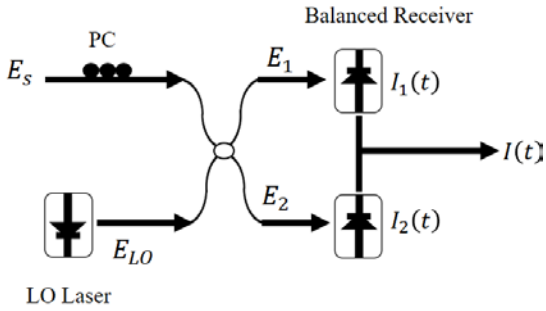

Figure 2.4: Coherent detection architecture.

where E_s and E_{LO} are the incoming signal from transmitter side and the field of the LO, respectively, in the time domain and are written by:

$$E_s(t) = A_s(t)e^{j\left(\omega_s(t) + \phi_s(t) + \phi_{pn}(t)\right)} \tag{2.1}$$

$$E_{LO}(t) = A_{LO}(t)e^{j\left(\omega_{LO}(t) + \phi_{LO}(t)\right)} \tag{2.2}$$

where $A_s(t)$ is the complex amplitude, $\omega_s(t)$ angular frequency, $\phi_s(t)$ the phase of the received signal, and $\phi_{pn}(t)$ is the phase noise. $A_{LO}(t)$ is the constant complex amplitude, $\omega_{LO}(t)$ angular frequency, and $\phi_{LO}(t)$ the phase of the LO. The complex amplitudes $A_s(t)$ and $A_{LO}(t)$ are related to the signal power $P_s(t) = |A_s(t)|^2/2$ and $P_{LO}(t) = |A_{LO}(t)|^2/2$, where $P_s(t)$ and $P_{LO}(t)$ are received power and LO power, respectively [8].

To maximize the signal photocurrents and suppress the dc components, coherent receiver uses balance detection by using a 3-dB optical coupler that mixes the LO signal with the received signal, resulting 180° phase shift between the two signals. When the received and LO signals are co-polarized, the electric fields on two photodiodes (upper and lower) are written as:

$$E_1(t) = \frac{1}{\sqrt{2}}[E_s(t) + E_{LO}(t)] \tag{2.3}$$

$$E_2(t) = \frac{1}{\sqrt{2}}[E_s(t) - E_{LO}(t)] \tag{2.4}$$

and the output photocurrents in electrical domain are given by:

$$\begin{aligned} I_1(t) = \frac{R}{2}\Big[&P_s(t) + P_{LO}(t) \\ &+ 2\sqrt{P_s(t)P_{LO}(t)}\cos\{(\omega_s(t) - \omega_{LO}(t))t + \phi_s(t) + \phi_{pn}(t) \\ &- \phi_{LO}(t)\}\Big] \end{aligned} \tag{2.5}$$

$$\begin{aligned} I_2(t) = \frac{R}{2}\Big[&P_s(t) + P_{LO}(t) \\ &- 2\sqrt{P_s(t)P_{LO}(t)}\cos\{(\omega_s(t) - \omega_{LO}(t))t + \phi_s(t) + \phi_{pn}(t) \\ &- \phi_{LO}(t)\}\Big] \end{aligned} \tag{2.6}$$

where R is the responsitivity of the photodiode and is given by:

$$R = \frac{e\eta}{\hbar\omega_s(t)} \tag{2.7}$$

where e indicates the electron charge, η the quantum efficiency of the photodiode, and symbol $\hbar$ stands for Planck's constant. Consequently, the balanced detector (BD) photocurrent output is obtained by:

$$\begin{aligned} I(t) = I_1(t) - I_2(t) \\ = 2R\sqrt{P_s(t)P_{LO}(t)}\cos\{(\omega_s(t) - \omega_{LO}(t))t + \phi_s(t) + \phi_{pn}(t) \\ - \phi_{LO}(t)\} \end{aligned} \tag{2.8}$$

The phase of LO ($\phi_{LO}(t)$) varies in time due to the phase noise, while the power ($P_{LO}(t)$) remains constant [8].

2.2.1 Heterodyne Detection

In a heterodyne receiver, $\omega_{IF}(t) \gg \frac{1}{2}\omega_b(t)$; where $\omega_b(t)$ is the modulation bandwidth of the optical carrier determined by the symbol rate, and $\omega_{IF}(t)$, intermediate frequency (*IF*), equals to $\omega_s(t) - \omega_{LO}(t)$.

Based on Eq. (2.8), the $I(t)$ is down-converted to the IF signal including the amplitude and the phase information, as shown in Figure 2.5 [8].

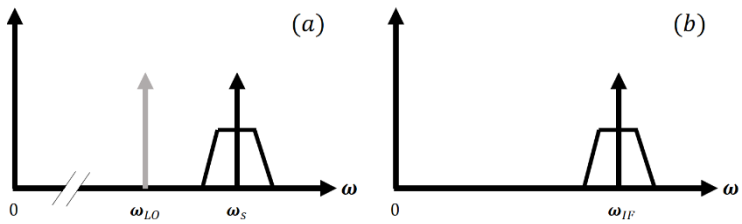

Figure 2.5: Spectra of (a) the optical signal, and (b) the down-converted IF signal.

Due to band-limitation and complexity in filter design, besides the low sensitivity of the heterodyne receivers, this thesis aims to study and implement homodyne receivers, which is the second type of the receivers in the coherent detection system.

2.2.2 Homodyne Detection

Homodyne detection is in the case that angular frequency of the LO is completely tuned with the received signal, resulting in $\omega_{IF}(t) = 0$. Thus, the Eq. (2.8) in homodyne will be given by:

$$I(t) = I_1(t) - I_2(t) = 2R\sqrt{P_s(t)P_{LO}(t)}\cos\{\phi_s(t) - \phi_{LO}(t)\} \tag{2.9}$$

In the homodyne detection to decode the encoded data, an optical phase-locked loop (OPLL) is needed for $\phi_{LO}(t)$ to track the $\phi_s(t)$. There are several OPLLs designs are well known such as those are presented in [9], [10] and also based on subcarrier OPPL [11].

While the Eq. (2.9) only provides the in-phase component, to detect the quadrature component another LO with 90° phase shifted is required. This, can be achieved by a 90° optical hybrid as shown in Figure 2.6.

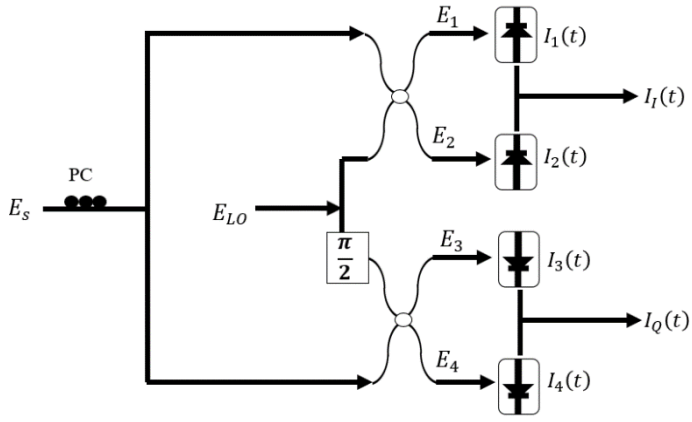

Figure 2.6: Phase-diversity homodyne receiver using 90° optical hybrids.

The electric fields of the output of the 90° optical hybrid can be written as:

$$E_1(t) = \frac{1}{2}[E_s(t) + E_{LO}(t)] \tag{2.10}$$

$$E_2(t) = \frac{1}{2}[E_s(t) - E_{LO}(t)] \tag{2.11}$$

$$E_3(t) = \frac{1}{2}[E_s(t) + jE_{LO}(t)] \tag{2.12}$$

$$E_4(t) = \frac{1}{2}[E_s(t) - jE_{LO}(t)] \tag{2.13}$$

Accordingly, the photocurrents from BPs are given by:

$$I_I(t) = I_{I1}(t) - I_{I2}(t) = R\sqrt{P_s(t)P_{LO}(t)}\cos\{\phi_s(t) - \phi_{LO}(t)\} \tag{2.14}$$

$$I_Q(t) = I_{Q1}(t) - I_{Q2}(t) = R\sqrt{P_s(t)P_{LO}(t)}\sin\{\phi_s(t) - \phi_{LO}(t)\} \tag{2.15}$$

By taking into account Eq. (2.14) and (2.15), the complex current is written by:

$$I_c(t) = I_I(t) + jI_Q(t) = R\sqrt{P_s(t)P_{LO}(t)}e^{j(\phi_s(t) - \phi_{LO}(t))} \tag{2.16}$$

With the complex PD current, received spectrum exists on both sides of frequency axis. This receiver architecture is called phase-diversity homodyne receiver, or in this work we call it intradyne receiver. Due to the baseband signal of the intradyne receiver, it is more useful in comparison to the heterodyne receiver which is working in high intermediate frequency regime.

Practically, in intradyne receivers the polarization of the received signal is not aligned with state of the polarization (SOP) of the LO, because of birefringence effects in optical fiber. There are some works try to make polarization stable [12], or designing a polarization independent architecture receiver [13]. Common and conventional solution to solve this issue is to use polarization diversity structure, where two phase-diversity homodyne receivers with 90° optical hybrids are combined with the polarization diversity configuration, as show in Figure 2.7 [8].

In a polarization diversity coherent receiver, the output photocurrents are given by:

$$I_{PD1}(t) = R\sqrt{\frac{\alpha_p P_s(t)P_{LO}(t)}{2}}cos\{\phi_s(t) - \phi_{LO}(t) + \delta\} \tag{2.17}$$

$$I_{PD2}(t) = R\sqrt{\frac{\alpha_p P_s(t) P_{LO}(t)}{2}} sin\{\phi_s(t) - \phi_{LO}(t) + \delta\} \tag{2.18}$$

$$I_{PD3}(t) = R\sqrt{\frac{(1-\alpha_p) P_s(t) P_{LO}(t)}{2}} cos\{\phi_s(t) - \phi_{LO}(t)\} \tag{2.19}$$

$$I_{PD4}(t) = R\sqrt{\frac{(1-\alpha_p) P_s(t) P_{LO}(t)}{2}} sin\{\phi_s(t) - \phi_{LO}(t)\} \tag{2.20}$$

where α_p is the power ratio and symbol δ shows the phase difference between the two polarization signals, respectively. From above equations, the complex amplitudes of the two polarization diversity receivers can be given by:

$$I_{xc}(t) = I_{PD1}(t) + jI_{PD2}(t) = R\sqrt{\frac{\alpha_p P_s(t) P_{LO}(t)}{2}} e^{j(\phi_s(t) - \phi_{LO}(t) + \delta)} \tag{2.21}$$

$$I_{yc}(t) = I_{PD3}(t) + jI_{PD4}(t) = R\sqrt{\frac{(1-\alpha_p) P_s(t) P_{LO}(t)}{2}} e^{j(\phi_s(t) - \phi_{LO}(t))} \tag{2.22}$$

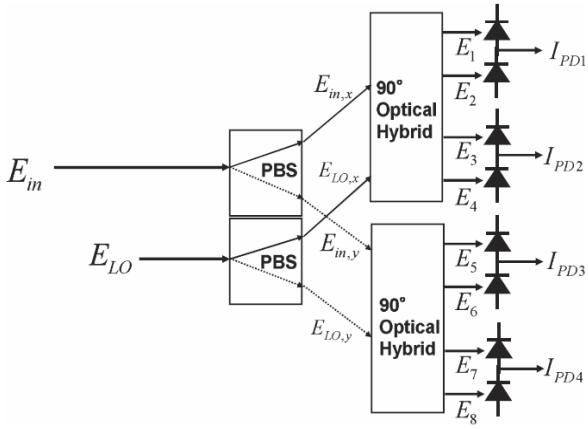

Figure 2.7: Polarization diversity scheme of the intradyne receivers using 90˚ optical hybrids [8].

2.3 Anatomy of Digital Coherent Receivers

The digital coherent receiver mainly contains three main subsystems, including optical front end, to map the optical field into electrical signals, ADC, which converts the electrical signals into discrete-time signals with a specific sampling rate, and DSP, to extract the received data, from the transmitter side [14]. Digital signal processing in coherent receivers has increased the capacity of optical access networks in terms of the number of users, being cost effective and performance. But in contrast, DSP solutions gets involved complexities that this thesis is going to deal with. These subsystems are described in the followings.

2.3.1 Optical Front-End

Optical front-end is to linearly map the incoming optical field into the electrical domain. Phase and polarization diversity with a pair of 90° hybrids, is a common architecture that is used in optical front-end as was shown in Figure 2.8. There is also another scheme based on a symmetric 1:1:1 3×3 coupler and three single-ended photo-detectors, as shown in Figure 2.8 [15].

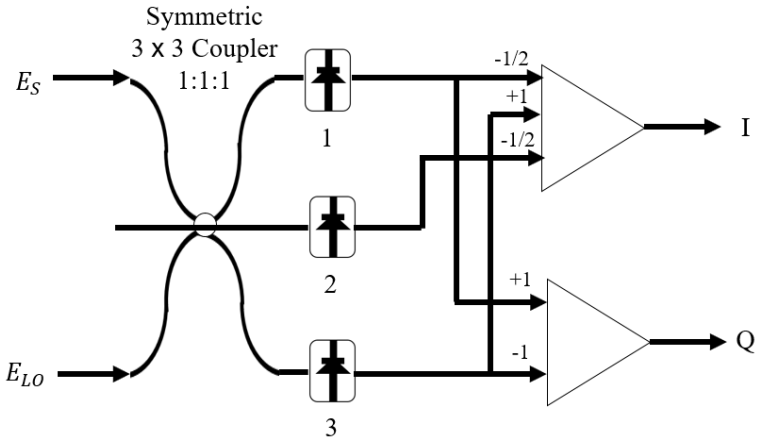

Figure 2.8: Schematic of symmetric 3×3 coupler based 90° hybrids.

With the optical signal and LO fields E_s and E_L at the input of the coupler, the photocurrents are given by:

$$\begin{pmatrix} I_1 \\ I_2 \\ I_3 \end{pmatrix} = \frac{1}{3}\begin{pmatrix} |E_L|^2 + |E_S|^2 \\ |E_L|^2 + |E_S|^2 \\ |E_L|^2 + |E_S|^2 \end{pmatrix} + \frac{2}{3}\begin{pmatrix} |E_L||E_s|cos\left(\varphi + \frac{2}{3}\pi\right) \\ |E_L||E_s|cos(\varphi) \\ |E_L||E_s|cos\left(\varphi - \frac{2}{3}\pi\right) \end{pmatrix} \tag{2.23}$$

where φ represents the phase difference between the received signal and the LO. The direct detection term (the first term in Eq. (2.23)) can become large compared to the beat term (the second term in Eq. (2.23)), if LO-to-signal-power-ratios (LOSPRs) is small or there are many WDM channels. Using a simple analog scaling and subtraction circuits and two ADCs, the direct-detection signal and LO are eliminated from I and Q components which are given by:

$$I_I = I_2 - 0.5I_1 - 0.5I_3 = |E_L||E_s|cos\phi \tag{2.24}$$

It is also possible to use three ADCs to convert the three detected components to digital signals and then performing the operations using DSP. Accordingly, the architecture of the symmetric 3x3 couplers, polarization beam splitter (PBS), and single-ended photo-detectors, including three ADCs is shown in Figure 2.9.

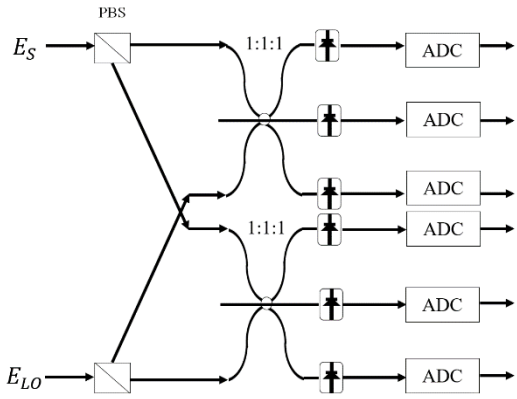

Figure 2.9: Schematic of symmetric 3×3 coupler and single-ended photo-detector.

2.3.2 Analog-To-Digital Conversion

After mapping optical signal into the electrical signal using front-end circuits, the next step is to prepare the analog signals for digital processing by converting it to

digital signal. The ADC, measures the analog signal on each falling or rising edge of the reference clock. Then, the samples get converted into digital values with a fixed precision.

To have a high-speed ADC, there are several types [16], [17]:

1) Flash, or parallel ACD, which consists of a series of comparators where each one compares the input signal with a reference voltage, as shown in Figure 2.10. The performance of this kind of ADC is limited by clock distribution accuracy and the comparator characteristics [17].

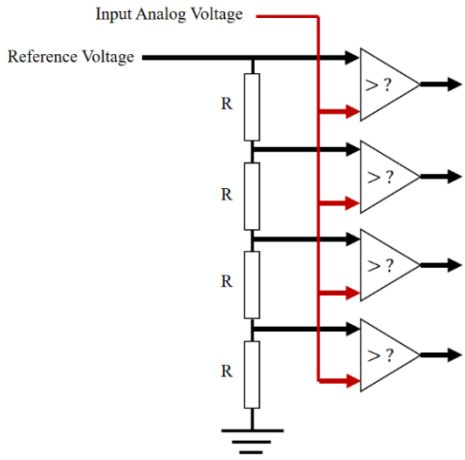

Figure 2.10: Flash ADC type.

2) Flash ADC with track-and-hold, refers to the input sampling circuit of the ADC. In this type of ADCs, the number of comparators is reduced and the performance is depended on track and hold process. Figure 2.11 shows a track-and-hold circuit.

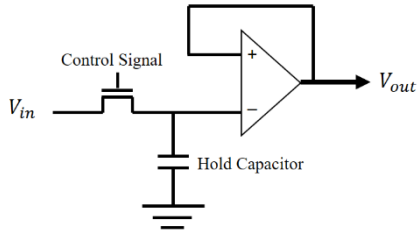

Figure 2.11: Track-and-hold circuit.

3) Time-interleaving ADCs, is a technique to increase the system sampling rate by using several ADCs in parallel. The interleaving process with several ADCs is shown in Figure 2.12.

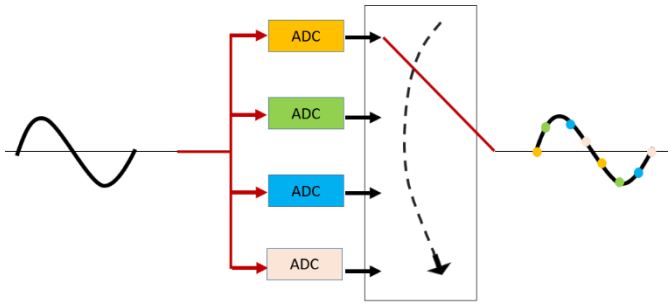

Figure 2.12: Time-interleaving process to increase the analog-to-digital sampling rate.

The third kind of ADCs is very useful for cost-effective applications. Thus, it is an attractive approach for this thesis to get advantage. As a result, in this work we use a 4-channel ADC from 4DSP company, each channel operating at 1.25 Gsps, and upgrading to 2.5 and 5 Gsps, using two and four channel time-interleaving. In some part of our application, we use time-interleaving to achieve 2.5 Gsps.

2.3.3 Digital Signal Processing

The coherent detection based on digital signal processing (DSP) is an advanced technology because of robustness and flexibilities. Although more complex compared with the analog equivalents typically due to the need of high speed ADCs, digital implementation enables effective mitigation of signal impairments such as phase noise, chromatic dispersion (CD) and LO wavelength detuning, as well as fast reconfiguration for different modulation formats and transmission rates valuable characteristics for the new concept of flexible optical networks with software-defined transceivers [18].

Usually, the signal obtained after the ADCs may be distorted by the following effects [14]:

- The sampling process occurs faster or slower than received signal. Also, the sampling phase may be detuned from the optimum symbol position.
- The laser linewidth causes phase noise on the received signal. Besides, LO wavelength detuning generates optical frequency offset on the detected data.
- The received signal may be distorted due to the fiber linear impairments, fiber nonlinearities, and changing the SOP.

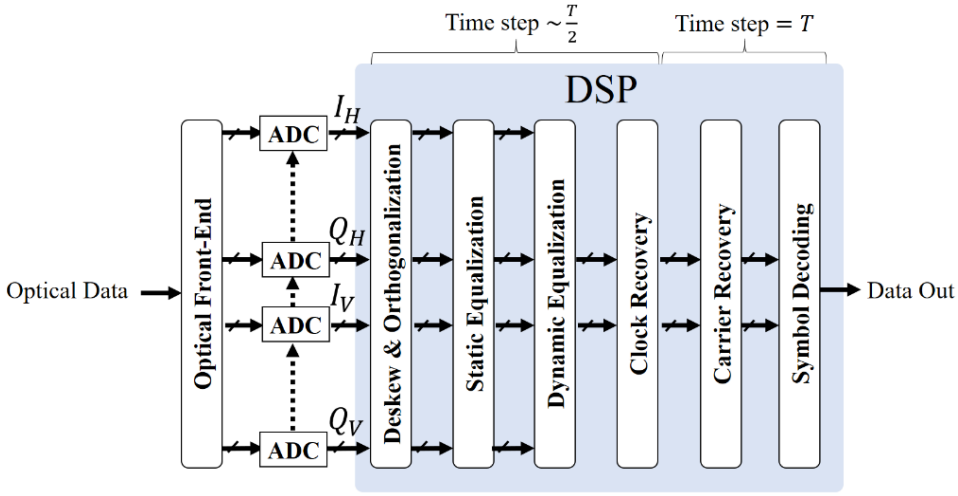

Figure 2.13: A conventional DSP for the coherent receivers.

A well-designed DSP must compensate these effects and distortions, and extract the received signal with as low as possible error rate. Typically, a conventional DSP with basic subsystems is shown in Figure 2.13 [14], where the optical data is converted to the electrical domain by optical front-end, which is based on polarization diversity circuit by 90° hybrids, or symmetric 3×3 couplers. We study and evaluate each conventional DSP subsystem briefly as follows.

2.3.3.1 Deskew and Orthogonalization

The Deskew subsystem is applied to compensate the timing mismatch between the signals arriving at the input of signal processing submodule. This timing mismatches is due to the impairments in O/E or optical front-end. If the timing delay between the

input signals is corresponded to an integer number of samples, it can be measured or estimated by cross correlating the signals. Since the timing delays are not an integer number of samples, the delay is written as [17]:

$$z = iT_{ADC} + \tau T_{ADC} \tag{2.26}$$

where the symbol i and τ are the number of samples and fractional delay, respectively. Moreover, the received I and Q signals from the 90° optical hybrids should be orthogonal to each other. But in practical experiments, the imperfections of transmitter, optical front-end and O/E interfaces, such as incorrect bias point of a modulator, non-exact splitting ratios of couplers, polarization controller impairments destroy orthogonality between I and Q signals [19]. As an example, the Gram-Schmidth algorithm is a common approach that creates a set of mutually orthogonal vectors, then takes the first vector as reference against which all subsequent vectors are orthogonalized. Given two received non-orthogonal signals $r_I(t)$ and $r_Q(t)$, the Gram-Schmidth method results in a new pair of orthonormal signals given by:

$$I^{\circ}(t) = \frac{r_I(t)}{\sqrt{P_I}} \tag{2.27}$$

$$Q'(t) = r_Q(t) - \frac{\rho r_I(t)}{P_I} \tag{2.28}$$

$$Q^{\circ}(t) = \frac{Q'(t)}{\sqrt{P_Q}} \tag{2.29}$$

where $\rho = E\{r_I(t).r_Q(t)\}$ is the correlation coefficient, $P_I = E\{{r_I}^2(t)\}$, $P_Q = E\{{r_Q}^2(t)\}$, and $E\{.\}$ stands for ensemble average operator [20].

2.3.3.2 Static Equalization

The static equalization is applied to compensate CD, that is the result of different wavelengths arriving at receiver at different times, usually for the applications with

more than 10 Gbps speeds, due to the large bandwidth of the wavelength spectrum. The purpose of the static equalization is to compensate the signal group velocity dispersion (GVD) caused because of CD. In the absence of Taylor-expanded propagation equation, the dispersion transfer function H can be written as [19]:

$$H(L,R) = e^{-j\left(\frac{D\lambda^2\pi {R_b}^2 L}{c}\right)} \tag{2.30}$$

where term D denotes dispersion parameter, λ is wavelength, L is the fiber length, R_b is the symbol rate, and c is speed of light. The dispersion function in time domain is given by [19]:

$$h(t) = \sqrt{\frac{jc}{\lambda^2 DL}} e^{-j\left(\frac{\pi c}{\lambda^2 DL}t^2\right)} \tag{2.31}$$

Since the CD is linear time-invariant (LTI), it can be compensated by a fractionally-spaced finite-impulse response (FIR) filter [21]. Thus, the equalized signal can be achieved by a FIR filter as:

$$y(t) = \sum_{n=0}^{N_{Taps}-1} c(n)\, x(k-n) \tag{2.32}$$

where $c(n)$ is obtained from $h(t)$ with a truncated response, N_{Taps} number of filter taps, and $x(k)$ the input signals of $I(k) + jQ(k)$, where $I(k)$ and $Q(k)$ correspond to in-phase and quadrature signals, respectively. The FIR filter design for static equalizer is shown in Figure 2.14:

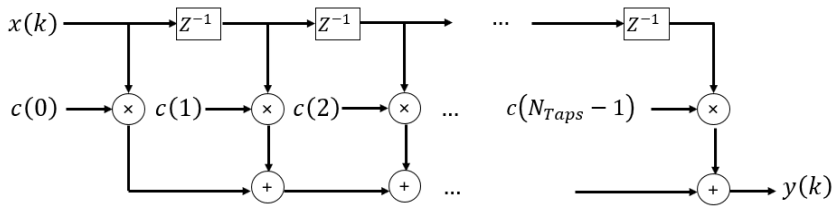

Figure 2.14: FIR filter scheme in static equalization.

2.3.3.3 Adaptive Equalization

To compensate time varying channel impairments, such as polarization mode dispersion (PMD), the equalizer has to be updated for desired response, that makes adaptive equalization. The adaptive equalizer includes two main part as shown in Figure 2.15.

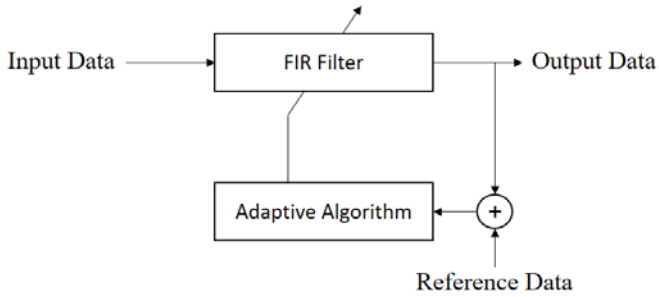

Figure 2.15: Structure of an adaptive equalization.

The filtering part, is same structure as static equalizer in Figure 2.14, and adaptive algorithm is to adjust filter taps dynamically. The main adaptive algorithm that are used in this structure are constant modulus algorithm (CMA) and leas mean square (LMS) approaches.

CMA algorithm uses constant modulus characteristic of the phase-modulated signal to compensate distortions by finding the point that cost function is minimum. In CMA, cost and error functions are [22]:

$$J_{CMA} = E(\varepsilon_{CMA}^2) \tag{2.33}$$

$$\varepsilon_{CMA} = 1 - |x'|^2 \tag{2.34}$$

where J and ε, are cost and error functions, respectively, x' stands for complex input signal from one polarization, and $E(.)$ shows statistical expectation. The goal is to minimize the cost function in desire point where the error function equals to zero. Thus, the tap weights of the equalizer for two complex polarization signals X' and Y' as the output of the equalizer are given by [21], [22]:

$$h_{xx} = h_{xx} + \mu\varepsilon_{CMA,X}X'.X^* \tag{2.35}$$

$$h_{xy} = h_{xy} + \mu\varepsilon_{CMA,X}X'.Y^* \tag{2.36}$$

$$h_{yx} = h_{yx} + \mu\varepsilon_{CMA,Y}Y'.X^* \tag{2.37}$$

$$h_{yy} = h_{yy} + \mu\varepsilon_{CMA,Y}Y'.Y^* \tag{2.38}$$

where μ is the iteration factor, "." is the vector dot product, and "*" denotes complex conjugate of the value. Finally, the output of equalizer based on the CMA algorithm can be obtained by:

$$X' = h_{xx}.X + h_{xy}.Y \tag{2.39}$$

$$Y' = h_{yx}.X + h_{yy}.Y \tag{2.40}$$

In the LMS algorithm, the equalization error is given by:

$$\varepsilon_{LMS} = Ref - x' \tag{2.41}$$

where term Ref stands for the reference signal, and for coherent receivers is obtained from transmitted training data, after being compensated by frequency estimation (FE). The optimum tap weights are updated by:

$$h_{xx} = h_{xx} + \mu\varepsilon_{LMS,X}X^* \tag{2.42}$$

$$h_{xy} = h_{xy} + \mu\varepsilon_{LMS,X}Y^* \tag{2.43}$$

$$h_{yx} = h_{yx} + \mu\varepsilon_{LMS,Y}X^* \tag{2.44}$$

$$h_{yy} = h_{yy} + \mu\varepsilon_{LMS,Y}Y^* \tag{2.45}$$

Normally, each adaptive equalizer requires some training steps with the ideal or reference data, when the system starts working.

2.3.3.4 Clock Recovery

Usually in a coherent receiver, ADCs does not operate in the same speed with the transmitted data. Thus, it is necessary to compensate the difference between the received data clock and the ADC sampling rate. In the coherent receiver, timing or clock recovery subsystem estimates and corrects the sampling phase and keeps the DSP and the received signal synchronized for an ideal sampling instant. Typically, in analog receivers a phase-locked loop (PLL) is used for the signal timing recovery [23]. The PLL is a control system that generates a signal with the same phase of the input signal, and it contains a phase detector (PD), and a voltage-controlled oscillator (VCO). The output of PD through a loop filter goes to VCO, and the output of VCO returns back to another input of PD.

Timing recovery in digital domain is a bit different, and there are some well-known data-aided and non-data-aided techniques that are used to estimated and compensate the phase and frequency difference between the received signal and DSP subsystem. As an example, Mueller-Muller (MM) is a data-aided timing recovery technique which can estimates the timing error using only one sample per symbol [24]. The MM algorithm obtains the channel response from baud-rate samples of the received data, then align the sampling point in the best (middle) point of the pulse response.

The major drawback of MM timing recovery is that it is sensitive to carrier offset. The carrier recovery must be done before the MM timing recovery [25]. The other drawback is that it is only relevant for random data, and an alternating data pattern may cause the MM to be failed [26].

Minimum mean squared error (MMSE) timing recovery is another timing recovery method which estimates the sampling error by minimizing the expected value of the squared error. The drawback of the MMSE is to produce slope and signal errors at high speed data rates [26].

One of the commonly used non-data aided methods is Gardner algorithm [27], [28]. In the Gardner method, two samples per symbol are required to estimate late, ideal,

and early sampling. An amplitude timing error detector (TED)-based Gardner is as follows:

$$E_G = \sum_{k=1}^{m} [I_{2k}(I_{2k+1} - I_{2k-1}) + Q_{2k}(Q_{2k+1} - Q_{2k-1})] \tag{2.46}$$

where I and Q are in-phase and quadrature components, k is sample index, and E_G the output of Gardner TED. For Nyquist signals with small roll-off factors, the performance of the Gardner method reduces until it fails in roll-off factor equal to zero. To avoid this problem a power-based TED was proposed as follows [29]:

$$E_P = \sum_{k=1}^{m} P_{2k}(P_{2k+1} - P_{2k-1}) \tag{2.47}$$

where $P = I^2 + Q^2$, and E_P is the error output of Gardner power-based TED. This method makes a timing recovery strong enough to be immune against laser phase noise, frequency offset and polarization scattering.

2.3.3.5 Carrier recovery

A conventional carrier recovery (CR) for digital PSK receivers consists of FE that is followed by phase recovery (PR). The phase shift $\Delta\varphi$ between two consecutive samples that is caused by a frequency error between Tx and LO lasers, is estimated in FE. To compensate the frequency error, the accumulated frequency offset has to be subtracted from each symbol with corresponding symbol index in PR. Several structures are suitable for FE, like the differential m^{th}-power estimator [30], the IQ correlation based estimator [31], and the pre-decision angle estimator [32]. On the other hand, PR can be achieved by the well-known Viterbi phase estimator [33], or by differential demodulation [34]. As an example, a deferential detections scheme for CR is shown in Figure 2.16.

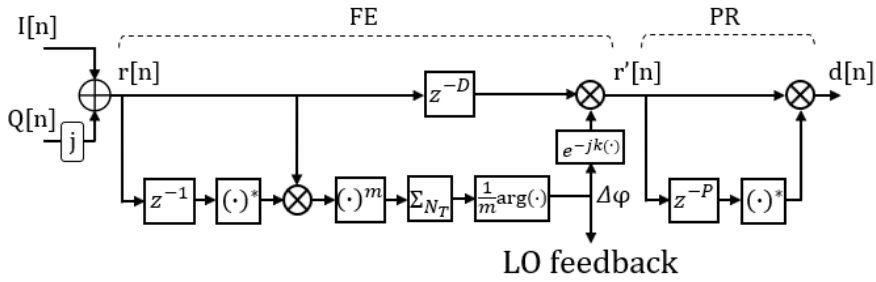

Figure 2.16: Conventional CR based on differential mth-power for FE and differential demodulation for PR.

where m is the number of constellation points of the PSK modulation (e.g., $m = 2$ for DPSK), N_T is the averaging length in number of symbols, D is the process delay (number of clocks) of the FE algorithm, and $(\cdot)^*$ stands for complex conjugate. As this structure assumes Clk recovery before CR, In-phase ($I[n]$) and Quadrature ($Q[n]$) signals are at one sample per symbol. Thus, the phase shift $\Delta\varphi$ produced by the frequency error is given by:

$$\Delta\varphi = \frac{1}{2}\arg\left(\frac{1}{N_T}\sum_{n=0}^{N_T-1}(w[n])^2\right) \tag{2.48}$$

In the mentioned conventional architecture, both FE and PR stages implement a complex correlation with different signal delay to extract the phase difference between samples (z^{-1}) in FE, or between symbols (z^{-P}) in PR, where $P = R_s/R_b$ represents the oversampling factor defined as the ratio between the sample rate (R_s) and the symbol rate (R_b). Usually, $R_s \geq 2R_b$ at the ADCs for mapping into the digital domain, to satisfy the Nyquist sampling criterion.

2.3.3.6 Symbol Estimation and Decoding

After the CR, symbol decoding, or data decision is the final step in coherent receiver to determine the pure received data. The symbol decoding can be done by a soft-decision forward-error correction (FEC), or by hard-decision FEC [17]. For example, in DPSK modulation format threshold-based symbol estimation can be used in this

way that constellations with phase = 0, where data has positive value, are considered logical '1', and constellations with phase = π, where data value is negative, are expected to be logical '0'. Another example is a commonly used method for symbol estimation in QAM systems to make decisions based on minimum Euclidean distance between the received and the reference constellation points, using hard-decision decoding [19]. In this thesis, we only apply a simple threshold-based symbol estimation for simplicity in the hardware implementations.

2.4 Conclusion

The coherent detection technology based on digital signal processing, in spite of being more complex than its analog counterparts, shows higher performance alongside several advantages. The DSP of coherent receiver compromises low-cost devices and lasers, mitigates phase noise, CD, as well as frequency offset estimation and compensation. It also allows the Tx and Rx for free running data with different frequencies to transmit in the Tx side, and to detect in the Rx part. Moreover, the DSP allows for fast reconfiguration to potentially different level of modulation formats, feasible for the future optical networks with software-defined transceivers.

In the next chapters, we will propose CR DSP algorithms and architectures to simplify the operation, reduce the hardware complexity and power consumption, improve the performance, but also practical with low-cost devices, that will cause to the cost reduction of the optical access networks for the final users.

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Chapter 3. DSP for Intradyne Optical PSK Receivers in udWDM-PON

Introduction

As mentioned in previous chapters, the coherent detection based on DSP is an advanced technology because the digital implementation enables effective mitigation of transmission impairments, as well as fast reconfiguration, allowing for different modulation formats and transmission rates, valuable characteristic for the new concept of flexible optical networks with software-defined transceivers [1].

There are some well-known DSP solutions for coherent systems such as the works in [2], [3], [4]. Due to the rapid incensement of the bandwidth demand per user, the real-time development of DSP for the coherent technology is required. As a robust and flexible approach, the efficient hardware implementation of DSP techniques by using FPGA is a solution for deployment of the future optical access networks.

This chapter aims to present hardware and FPGA implementations of the basic DSP subsystems for Intradyne optical PSK receivers as well as proposing optimized CR which reduces hardware complexity and improves the performance to recover the optical carrier from the received data.

3.1 DSP for Intradyne Optical PSK Receivers

The purpose of this chapter is to suggest DSP architectures for intradyne optical PSK and DPSK single-polarization (SP) receivers, in an udWDM-PON. This chapter evaluates the basic operation of DSP subsystems with simple solutions, but requires the SOP to be manually adjusted.

The SP coherent Rx and its developed DSP architecture implemented on the FPGA with well-known and simple techniques for digital coherent receivers, with 2 samples per symbol to meet the Nyquist criteria, is shown in Figure 3.1 [3], [5].

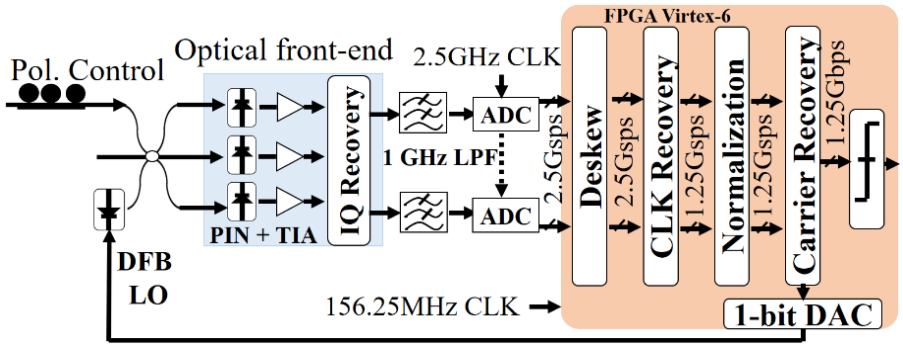

Figure 3.1: SP coherent Rx and its DSP for PSK data.

The DSP is implemented on a commercial FPGA, optical front-end based on low-cost 3×3 couplers, and distributed feed-back (DFB) lasers, with direct DPSK modulation at 1.25 Gbps. In the followings, we evaluate each DSP subsystem for FPGA implementation in real-time digital signal processing.

3.1.1 Deskew

The Deskew block calculates the time delay between *I* and *Q*, that are inputs of the DSP which was shown in Figure 3.1. The process is done by correlating both signals, and a block length of N_T samples is selected for the correlation, to compensate an integer value of delayed samples. Otherwise, to calculate and compensate fractional delays between samples, the Deskew must be fed from interpolated signals. Due to

the constant delays in the hardware in our application, which is mainly occurred in the ADCs, the Deskew process needs to be performed only once, when the receiver starts working.

Since there are only two signals at 1.25 Gbps, and we have a 4-channel ADC, thus each channel operates at 1.25 Gsps, where two interleaving process between each two channels, provide 2-spb for *I* and for *Q*. Figure 3.2 shows an architecture to perform sampling alignments and interleaving to deliver the symbols, then, making the symbols from the re-constructed *I* and *Q*, synchronized.

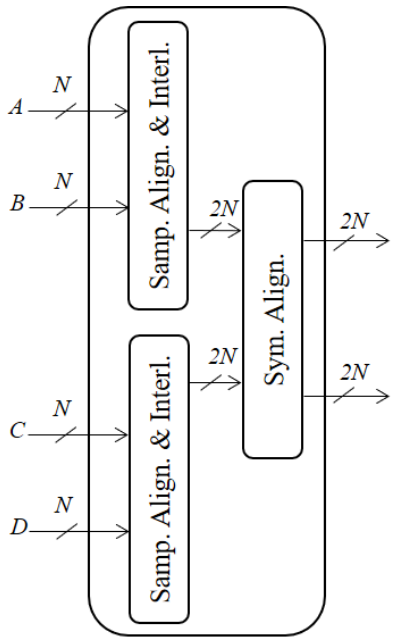

Figure 3.2: Deskew architecture; Samp. Align. & Interl.: Sample Alignment and Interleaving, Symb. Align.: Symbol Alignment.

The term *N* is the number of samples, sampled by each ADC (labled as *A*, *B*, *C*, *D*), where channels *A/B*, and *C/D* are interleaved two by two to achieve 2-spb, and are aligned in *Sample Alignment & Interleaving* block. The product of the interleaved channels needs to be aligned in the symbol level in *Symbol Alignment* module. Whereas interleaving is done on incoming *I* or *Q* signals, the interleaved samples

have the same phase. But, due to the ADC performance, or any hardware delay before DSP, the output of ADC channels might not be aligned. To solve this problem, we use the fact that the minimum of absolute value of a differential-based correlation in a large scale of samples, estimates the delay between the interleaved samples for PSK modulated signals. It simply means if we subtract two similar signals, the result is zero (or is minimum) when they are completely aligned. Therefore, the amount of shifting is given by:

$$DS_I = n_{min\{f(n)\}} \tag{3.1}$$

where

$$f(n) = \left(\sum_{k=n}^{N_S+n-1} |S(k)| \right) \tag{3.2}$$

In Eq. (3.2), k is the sample index, N_S is the total number of samples, N is the number of parallel samples or the signal width, and n is amount of samples are shifted to the right ($n > 0$), or to the left ($n < 0$) in the range of $-N_S \leq n \leq N_S$. Function $S(k)$ calculates the subtracted value of signal x_1 regarded to x_2, and it is obtained by:

$$S(k) = [x_1(k_1) - x_2(k_2)] \tag{3.3}$$

where parameters x_1 and x_2 are the input signals, $k_1 - k_2 = N_S + k$. Deskew sample index (DS_I), shows the amount of samples to be shifted from x_1 with respect to x_2 when the function $f(n)$ reaches to the minimum (i.e. $n_{min\{f(n)\}}$). Finally, each sample index of the shifted signal x_1 is attached to the same sample index of signal x_2, to reconstruct the symbols, yields signal x.

Consequently, and regarding to Eq. (3.1) and Eq. (3.2), the *Sample Alignment* and *Interleaving* block is shown in Figure 3.3, that is appropriate to align signals with the same phase. But, in a coherent receiver with I and Q signals, where they have

different phases, the above method is not effective. For this purpose, we must first cancel the phase noise on the signals.

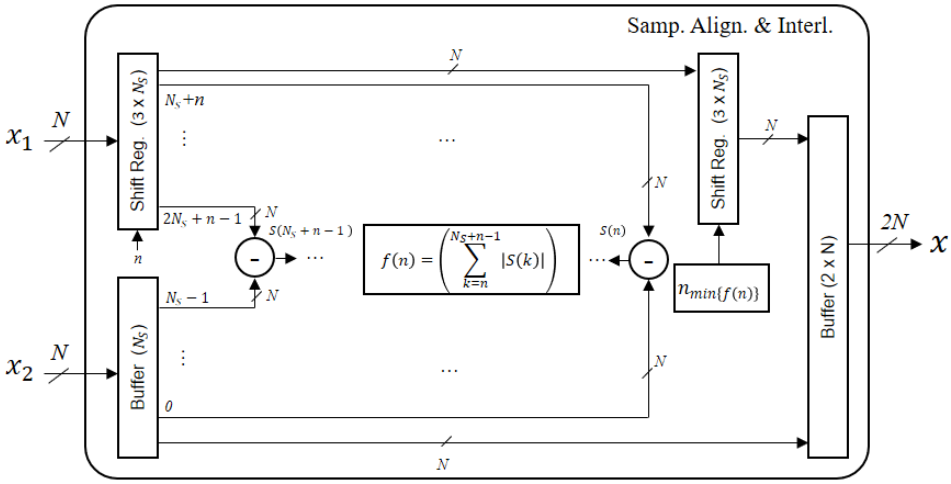

Figure 3.3: Sample Alignment and Interleaving block for PSK data.

Considering a DPSK modulated format for input data, differential demodulation method will cancel the phase noise. From chapter 2, in the SP coherent Rx, I and Q signals in the digital domain with neglecting the noise can be estimated as:

$$I[n] = a[n].cos\{\phi_c[n] - \phi_{LO}[n] + \phi_n[n]\} \tag{3.4}$$

$$Q[n] = a[n].sin\{\phi_c[n] - \phi_{LO}[n] + \phi_{pn}[n]\} \tag{3.5}$$

where $a[n]$ = ±1 is the phase-encoded data (in DPSK), $\phi_{pn}[n]$ is the phase noise, and $\phi_c[n]$ is the carrier phase. By considering $\phi_c[n] = \phi_{LO}[n]$, and $\phi_{pn}[n] \approx \phi_{pn}[n-1]$, the differential demodulation of complex amplitudes, signal $r[n] = I[n] + jQ[n]$ is ideally given by:

$$w[n] = r[n] * r^*[n-1] = a[n].a[n-1] \tag{3.6}$$

where symbol '*' stands for complex conjugate, $a[n].a[n-1]$ represents the differentially-demodulated data. So, for signal w, we can follow almost the same strategy as the *Sample alignment and Interleaving* block, with two assumptions:

1) Data is pseudo random binary sequence (PRBS-word), where word = 7, 15, 23, or 31.

2) N_{Sym} is the total number of symbols length, and is much larger than the size of a unique word of data in the PRBS.

In these cases, the signal w is minimum when the signals I and Q are completely aligned. Accordingly, Figure 3.4 shows the *Symbol Alignment* block:

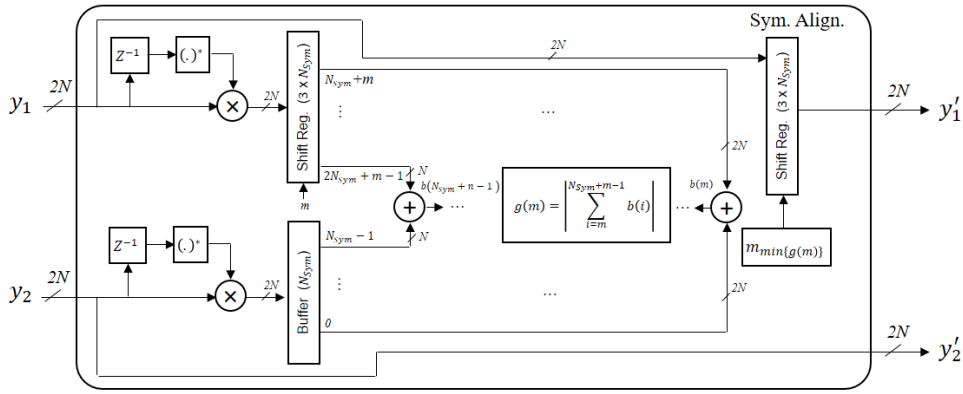

Figure 3.4: Symbol Alignment block for PSK data.

where y_1 and y_2 are the input signals, i is the symbol index, N_{Sym} is the total number of symbols, $2N$ is the number of parallel samples, and m is amount of sample are shifted to the right ($m > 0$), or to the left ($m < 0$) in the range of $-N_{Sym} \leq m \leq N_{Sym}$. Function $b(i)$ calculates the added value of signal y_1 to y_2, and it is obtained by:

$$b(i) = [y_1(i_1) - y_2(i_2)] \tag{3.7}$$

where $i_1 - i_2 = N_{Sym} + i$. Deskew symbol index ($DSym$), shows the amount of symbols to be shifted from y_1 to with respect to y_2 when the function $g(m)$ reaches to the minimum (i.e. $m_{min\{g(m)\}}$). The function $g(m)$ and $DSym$ are given by:

$$g(m) = \left| \sum_{i=m}^{N_{Sym}+m-1} b(i) \right| \tag{3.8}$$

$$DSym_I = m_{min\{g(m)\}} \tag{3.9}$$

At the end, signals y_1' and y_2' are synchronized in the symbol level even though they have different phases.

3.1.2 Clock Recovery

As was explained in chapter 2, in the coherent receivers, the ADCs might not operate in the same speed with the transmitted data. Thus, it is necessary to compensate the difference between the received data clock or processing speed and the ADC sampling rate. The purpose of this chapter is not to present new techniques for the clock recovery, as until will be done in the chapter 5. Thus, it implements very simple form of clock recovery with limited capabilities and without feed-back loop to control the ADCs sampling frequency, where it assumes that Tx clock is completely equal to Rx or DSP process clock in terms of frequency for the maximum performance and the minimum bit error rate (BER).

3.1.2.1 Clock Recovery without Interpolation

Since the received signal is based on 2 samples per symbol to meet the Nyquist sampling rate theorem, clock recovery (Clk Rec.) block selects the best sample to pass it for further processing, including CR and Data Decision subsystems. Figure 3.5 shows the architecture of this simple clock recovery, where input x with two samples S_0 and S_1 is down sampled to output y, with the sample which has larger

energy. In this scheme, the multiplexer (MUX), passes sample S_0 if the selection (Sel.) port is positive, and passes S_1 in the case that port Sel. is negative. To improve the performance of this simple clock recovery, cubic interpolation is one of the straightforward methods.

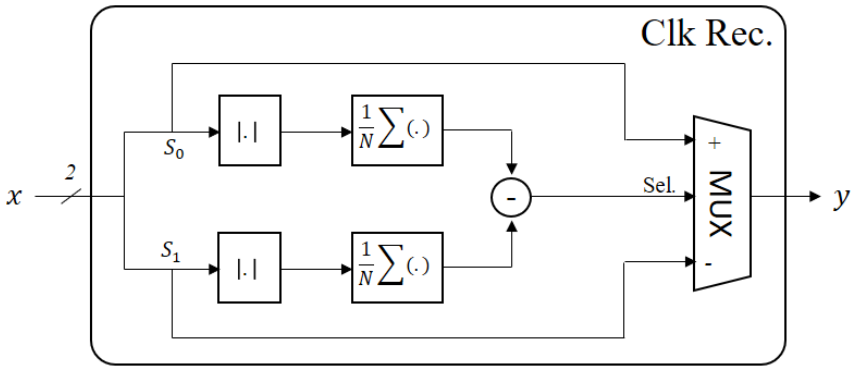

Figure 3.5: Clock recovery block based on 2-sps for PSK data.

3.1.2.2 Clock Recovery with Interpolation

In the mathematic, interpolation is a way of constructing new data points between the range of a discrete set of known data points. There are some well-known techniques to perform interpolation [6], [7]. Linear interpolation is the simplest method to get values within the range of data points. These points are simply joined by straight line segments, but results in disjointedness at the points. The cubic interpolation instead, by using two points before, another two points after the segment measures continuity between the points, and it is given by:

$$y(n'-\tau)=\left(-\frac{\tau^3}{6}+\frac{\tau^2}{2}-\frac{\tau}{3}\right)x(n-3)+\left(\frac{\tau^3}{2}-\frac{\tau^2}{1}-\frac{\tau}{2}+1\right)x(n-2)+\left(-\frac{\tau^3}{2}+\frac{\tau^2}{2}+\frac{\tau}{1}\right)x(n-1)+\left(\frac{\tau^3}{6}-\frac{\tau}{6}\right)x(n) \quad (3.10)$$

where τ is the fractional delay between samples or points, $n'=n-1$, and $y(n'-\tau)$ estimates the interpolated value between consecutive points of $x(n-1)$ and

$x(n-2)$. This interpolator can be implemented by a 4th – order FIR filter. As an example, to make an up sampling of 2 to 8, we need fractional delays of $\tau = \frac{1}{2}$, $\tau = \frac{1}{4}$, and $\tau = \frac{3}{4}$, and the points are obtained by:

$$y\left(n' - \frac{1}{2}\right) = \left(\frac{1}{16}\right)[-x(n-3) + 9x(n-2) + 9x(n-1) - x(n)] \tag{3.11}$$

$$y\left(n' - \frac{1}{4}\right) = \left(\frac{1}{128}\right)[-7x(n-3) + 105x(n-2) + 35x(n-1) - 5x(n)] \tag{3.12}$$

$$y\left(n' - \frac{3}{4}\right) = \left(\frac{1}{128}\right)[-5x(n-3) + 35x(n-2) + 105x(n-1) - 7x(n)] \tag{3.13}$$

Figure 3.6 shows a 4th-order FIR filter structure with 4 taps, where for each fractional delay of τ, taps a_τ, b_τ, c_τ, and d_τ, can be obtained from the Eq.(3.11) to (3.13). After estimating the points in 3 fractional delays between samples, then, each symbol contains 8 samples S_0 to S_7, and the best sampling point is granted by the similar structure in Figure 3.5, but with more decisions. Thus, using interpolation, the clock recovery estimates the best sampling instance more accurate.

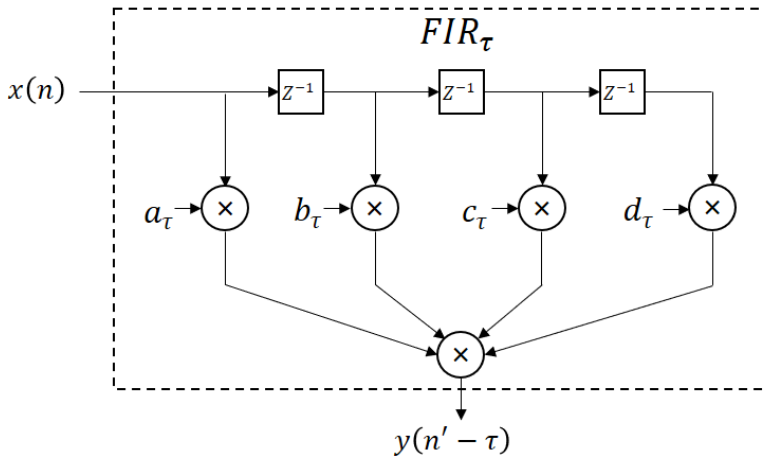

Figure 3.6: FIR filter structure for interpolation.

3.1.3 Normalization

Normalization is a process to adjust the measured values in different scales to a unit and common scale. In a coherent Rx, *I* and *Q* components might be in different scales due to nonsymmetric characteristics of the photo-diodes. The normalization process in this thesis is very simple and for *I* and *Q* is given by:

$$I_{norm} = \frac{I}{\sqrt{I^2 + Q^2}} \tag{3.14}$$

$$Q_{norm} = \frac{Q}{\sqrt{I^2 + Q^2}} \tag{3.15}$$

where I_{norm} and Q_{norm} are the normalized values of I and Q, respectively. For SP DSP, it is observed that normalization improves the performance, but is not a mandatory operation in our systems, since fixed-point operations are performed in fixed-size registers in FPGA implementations.

3.1.4 Proposed Carrier recovery (LUT-Based)

A highly important premise when implementing the access network is to maintain high the performance but lowering the cost, which lies on the final users. This translates into reducing the energy consumption and complexity of the optical network units. To satisfy the requirements of the access networks, efforts in research are being taken to develop the Gigabit-to-the-user concept towards user bandwidths in excess of 1 Gb/s, but enhancing the spectral efficiency by allocating hundreds of wavelengths in ultra-dense grid configuration [8], [9]. Figure 3.7 depicts the architecture of the udWDM-PON, including a standard tree-based PON with dedicated wavelength (λ) per user in separated bands for the DS and the US.

The channel spacing in the ultra-dense WDM grid, denoted by $\Delta\lambda$, is as close as 6.25 GHz for symmetric 1.25 Gb/s per wavelength, serving up to 256 users, in contrast with the 32/64 users of typical PONs. The high sensitivity of the coherent receivers

enables the large power splitting without the need of optical amplification, maintaining the optical distribution network totally passive and compatible with the standards for PONs.

Since the udWDM-PON is filterless, channel selection is done by wavelength tuning of the LO laser at the coherent Rx front-end. Thus, an accurate LO wavelength control is required for correct data detection and channel stability in such a closely-spaced udWDM grid. The LO λ-control is driven by the CR subsystem of the Rx DSP (Figure 3.7, highlighted in red), in which this article focuses on. One of the key points of the Rx DSP in our field trial implementation [10] was the use of differential encoding and detection for optical PR, due to its straightforward implementation and high robustness against the phase noise of low-cost lasers. Although synchronous detection with phase estimation algorithms overcomes the differential phase detection in high data-rate scenarios, for low transmission rates the performance of the differential detection is high, but with a remarkable lower implementation complexity [11]. Additionally, differential encoding is commonly applied, even for synchronous detection instead of differential detection, to avoid the phase-noise induced cycle-slips that produce phase ambiguity and error propagation [12]. Alternatively, data-aided DSP could be used to avoid the effect of cycle slips by transmitting pilot symbols for carrier synchronization and further channel equalization [13].

In this thesis, we propose an optimizer CR architecture based on differential detection for optical PSK modulation format, that shares the 1-symbol complex correlation needed for both the FE and the PR blocks of the Rx DSP, reducing the required hardware resources. This optimizes the parallel hardware prototyping in the FPGA and reduces the overall process delay of the DSP, enhancing the performance of the proposed CR against the fast wavelength drifts of lasers. The operating principle of the proposed method and the first experimental results is reported in [14].

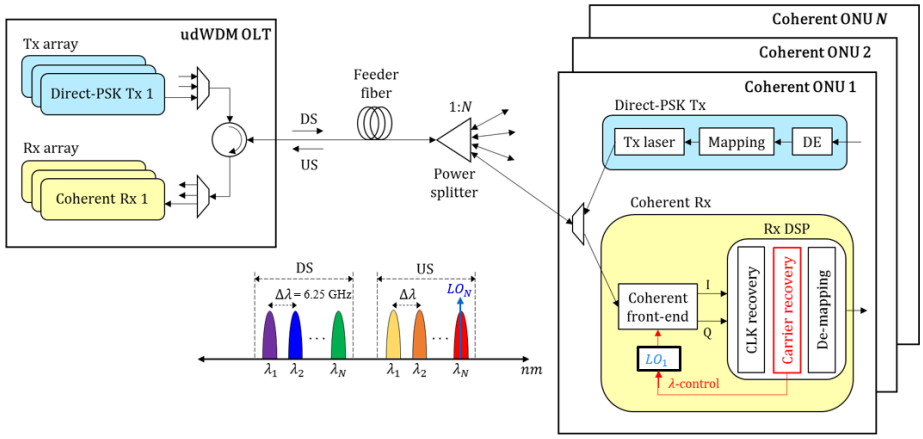

Figure 3.7: Network architecture for the udWDM-PON application scenario; DE: differential encoding.

In a conventional CR, including the differential *m*th-power FE scheme [15], [16], [17] that is followed by differential demodulation for PR [18], [19], [20], the phase shift $\Delta\varphi$ between two consecutive samples that is caused by a frequency error between Tx and LO lasers, is estimated in FE.

This section focuses on the differential detection schemes for CR. We first select the differential m^{th}-power estimator for FE, and the differential demodulator for PR. The complete CR architecture is depicted in Figure 3.8 (upper), where m is the number of constellation points of the PSK modulation (e.g., m = 2 for DPSK), N_T is the block length for averaging, k is the symbol index (or sample index, if CLK recovery is applied after CR) inside the estimation block, D is the process delay of the FE algorithm, and $(.)^*$ stands for complex conjugate. In this CR scheme, the phase shift $\Delta\phi$ induced by the frequency detuning between Tx and LO lasers is estimated from each sample of the received signal $r[n] = I[n] + jQ[n]$, then is removed by the phase rotator $e^{-jk(.)}$ before PR. Afterwards, the corrected signal $r'[n]$ is differentially demodulated by a 1-symbol complex correlation to recover the phase-encoded data $d[n]$. Note that both FE and PR stages implement a complex correlation with different signal delay to extract the phase difference between samples (Z^{-1}) in FE, or between

symbols (Z^{-P}) in PR, where $P = \frac{R_s}{R_b}$ represents the oversampling factor defined as the ratio between the R_s and the symbol rate R_b, where for the ADC $R_s \geq 2R_b$, to satisfy the Nyquist sampling theorem.

Some FE algorithms based on differential detection were specifically designed to estimate the frequency error between samples, requiring a delay of signal for the correlation shorter than the symbol duration, to avoid the influence of phase-modulated data [16]. However, the differential m^{th}-power FE algorithm in this thesis removes the PSK data by rising to the power of *m*, and the frequency error can be correctly estimated either between samples or between symbols [15]. Therefore, if clock recovery at the Rx DSP is performed before CR, then $P = 1$ and both FE and PR blocks in Figure 3.8 (upper) have the same 1-symbol complex correlation for differential phase detection; otherwise, for unrecovered CLK ($P \geq 2$) the signal delays for correlation are different.

As a consequence, for the case of an already recovered CLK ($P = 1$), we can modify the architecture in Figure 3.8 (upper) to calculate the 1-symbol correlation for PR only once per symbol, then reuse it for the next feed-forward FE, as represented in Figure 3.8 (middle) optimizing the implementation and saving hardware resources. A similar idea was proposed and tested in [20], working with differential m^{th}-power estimator for FE and Viterbi phase estimator for PR, both requiring calculation of the m^{th}-power. In such architecture, the m^{th}-power is calculated only once, then shared by the FE and the PR blocks of the DSP. Figure 3.8 (lower) shows the evolution of the signal constellation within the optimized CR in Figure 3.8 (middle), for the case of DPSK data. First, the received signal $r[n]$ completely rotates over the complex plane due to the phase noise and the frequency error ((*i*), left). Then, the optical phase is recovered by differential demodulation, getting rid of the phase noise effect. However, each symbol of $w[n]$ has a phase shift $\Delta\phi = \frac{2\pi\Delta f}{R_b}$ due to the frequency error denoted by Δf. It produces a fixed incremental rotation of the constellation in the complex plane ((*ii*), center). Finally, the residual phase shift $\Delta\phi$ is estimated and

corrected from the phase of each symbol, leading to a phase/frequency-noise-free signal $d[n]$ that goes to the decision part of the receiver ((*iii*), right). The estimated $\Delta\phi$ can also drive an external circuit for automatic LO tuning, as demonstrated in [21]. It is notable that the phase rotator $e^{-j(.)}$ in our proposed CR in Figure 3.8 (middle) does not include the symbol index k, as in Figure 3.8 (upper) for conventional CR, due to the frequency error of the signal $w[n]$ after differential demodulation that performs as a constant phase shift for all the symbols, with time-dependency already suppressed.

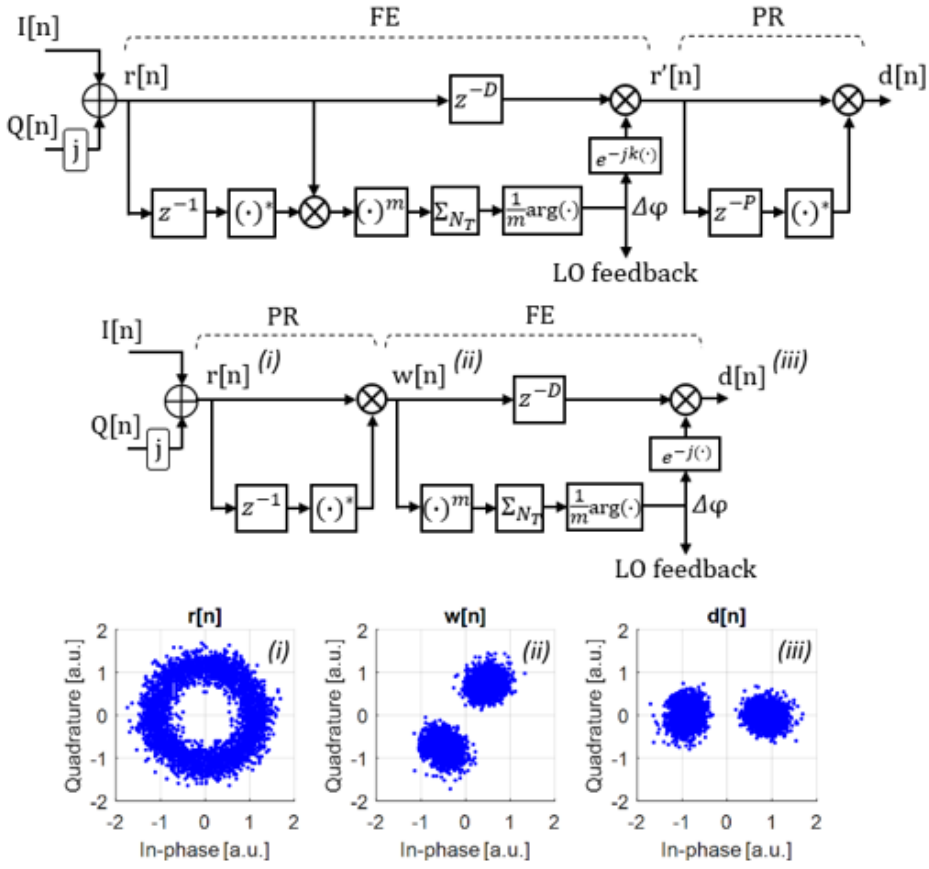

Figure 3.8: Conventional CR based on differential m[th]-power for FE and differential demodulation for PR (upper). Proposed CR that optimizes the architecture by reusing the 1-symbol complex correlation required for both the FE and the PR (middle). Evolution of the constellation for DPSK data along the proposed CR (lower).

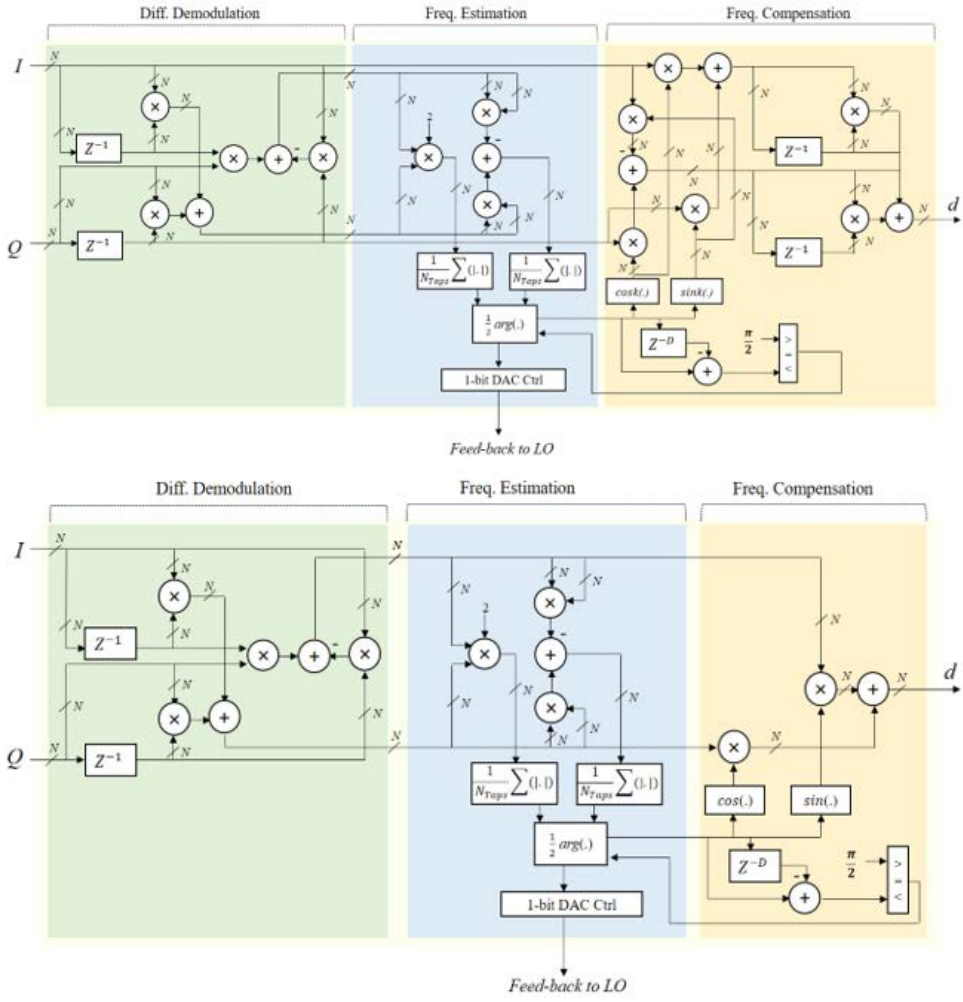

Figure 3.9: Implemented the conventional (upper), and proposed CR architecture (lower) on the FPGA.

The proposed CR requires less operations than the conventional CR, relaxing the hardware resources, as well as the energy consumption, when the coherent Rx is prototyped on the FPGA for real-time operation. Table 3.1 summarizes the required hardware resources for DPSK detection with both CR algorithms, demonstrates 23% and 25% of savings in the number of real adders and multipliers, respectively, with the proposed architecture, as well as 25% reduction in the overall process delay of the CR algorithm expressed in symbols. *N* represents the number of parallel bits

processed by the FPGA. The argument and phase rotator calculations to extract and cancel $\Delta\varphi$ is carried out by look-up table (LUT). Finally, since our proposed CR is completely feed-forward, it is expected to be more robust against the phase noise from low-cost lasers, and less challenging for parallel hardware implementation, compared with feed-back CR architectures.

Figure 3.9 shows exact CR structures implemented on the FPGA for conventional and proposed architectures, respectively. Less hardware requirements but the same functionality can be observed by comparing the implemented CR architectures on the FPGA.

Table 3.1 Hardware resources for the conventional and proposed CR architectures.

CR architecture	Multipliers	Adders	Process delay [symbols]
Conventional	$16 \times N$	$13 \times N - 2$	$4 \times N$
Proposed	$12 \times N$	$10 \times N - 2$	$3 \times N$
Reduction	25%	23%	25%

3.2 Field Trial Setup

The field trial setup in European COCONUT project [10], [22], [23], [24] is schematically shown in Figure 3.10. At the Scuola Sant'Anna lab, we simulated a central office hosting two OLT systems: the COCONUT OLT and a commercially available E-PON, where a concurrence WDM filter combined the two OLTs. The COCONUT OLT included four different groups of transceivers, based on different modulation formats of ASK or/and PSK, modulation types (direct or external), detection schemes (heterodyne or intradyne) and bit-rate (1.25 or 10 Gbps). We used an E-PON system because of availability of the equipment, and equivalent to a G-PON, since E-PON and G-PON shared the same wavelength plan. We also emulated a scenario where asymmetrical bit-rates are used (e.g. 10 Gbps downstream and 1.25 Gbps upstream).

Also, different experiments used three different wavelength allocation plans for the US/DS transmission: ultra-narrow spacing (2.5 GHz), UDWDM spacing (6.25 GHz)

and large spacing (100 GHz ITU grid). In all cases, a cascade of power splitters and a WDM multiplexer combined these signals. The WDM MUX had 100 GHz channel spacing and 100 GHz Full-Width at Half Maximum (FWHM) on each channel. For UDWDM operations, up to 8 channels fitted one MUX port on a 6.25 GHz grid.

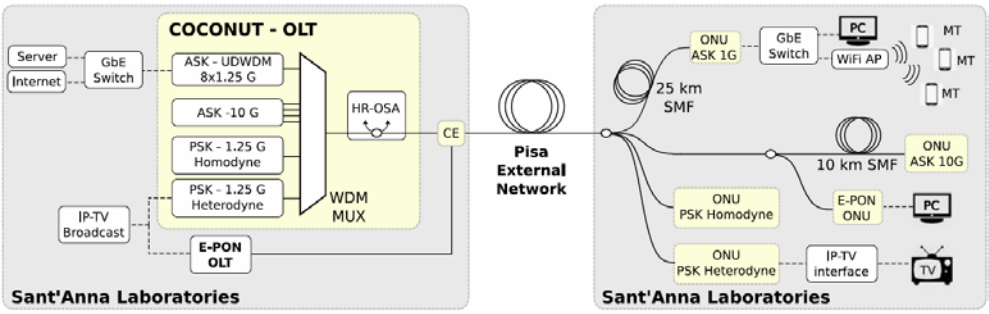

Figure 3.10: Schematic representation of the field trial setup; Gray areas represent the equipment placed in the lab, High-Resolution Optical Spectrum analyzer (HR-OSA), CE: Co-existence Element, PC: Personal Computer; AP: Access Point; MT: Mobile Terminal; TV: Television [10].

The channel monitoring system, provided by a low-cost High-Resolution Optical Spectrum Analyzer (HR-OSA), was placed at the MUX output through an optical by-pass allowing the monitoring of both upstream and downstream traffic. Then, the combined OLT output was directly connected to an external feeder fiber. The feeder was Single Mode Fiber (SMF) with approximately 10 km of loop length, as shown in Figure 3.11.

This external section consisted of several connections in outside cabinets, with a total insertion loss of 10 dB. The end of this fiber loop returned to the lab and connected to a drop fiber system realized by a cascade of power splitters and fiber spools to reach five ONUs, each one communicating with its own corresponding transceiver at the OLT side (either E-PON or the COCONUT ones). The full ODN had a maximum reach of 35 km, a maximum loss of 40 dB and ONUs maximum differential loss of 22 dB [10].

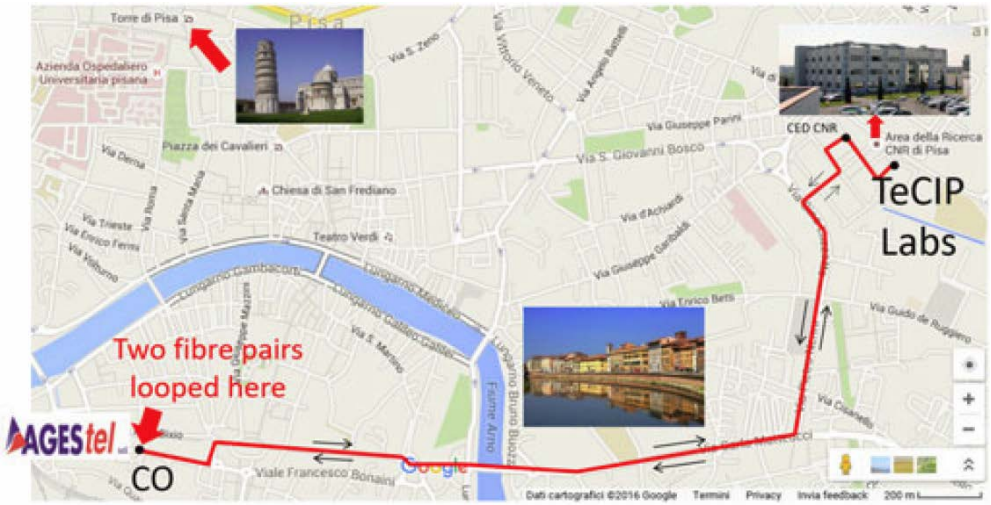

Figure 3.11: Map of the dark fiber deployment in loop configuration connecting the Scuola Superiore Sant'Anna laboratories to the Pisa city center [10].

3.2.1 Real-Time 1.25 Gbps Intradyne Setup

1.25 Gbps intradyne PSK system was implemented by using directly phase-modulated DFB lasers as shown in Figure 3.12. In this case the OLT upstream receiver exploited a dedicated FPGA platform for real-time detection. The ONU upstream included Tx as DFB laser ($\lambda = 1550$ nm) with spectral linewidth $\Delta\nu = 4$ MHz, emitting at 0 dBm, that was properly equalized by a high-pass RC network for direct 0-180º PSK modulation [8]. The Tx Data was a non-return-to-zero pseudo random binary sequences (NRZ-PRBS) from a pulse-pattern generator (PPG) running at 1.25 Gbps. Since PRBS data is used, differential encoding can be assumed at the Tx.

At the OLT, the coherent Rx contained a free-running LO to operate in intradyne regime. The LO was another DFB laser with $\Delta\nu = 4$ MHz, emitting at 3 dBm, and thermally-tunable for automatic frequency control (AFC) from the DSP feed-back. The optical front-end was based on 3×3 coupler instead of the widespread 90º optical hybrid, to beat the incoming optical signal with the LO. This allowed for phase-diversity with only three photodiodes instead of four. Next, the three photodetected

signals were linearly combined in passive hardware, according to the transfer matrix pointed in [21], to recover the I and Q components. Although IQ recovery can be performed by the DSP, this analog pre-processing saves one ADC channel, whose cost increases with its sample rate. The above-mentioned front-end was integrated in an FR4 printed-circuit-board substrate, with commercial TO-CAN packaged PIN photodetectors including trans-impedance amplifier (TIA).

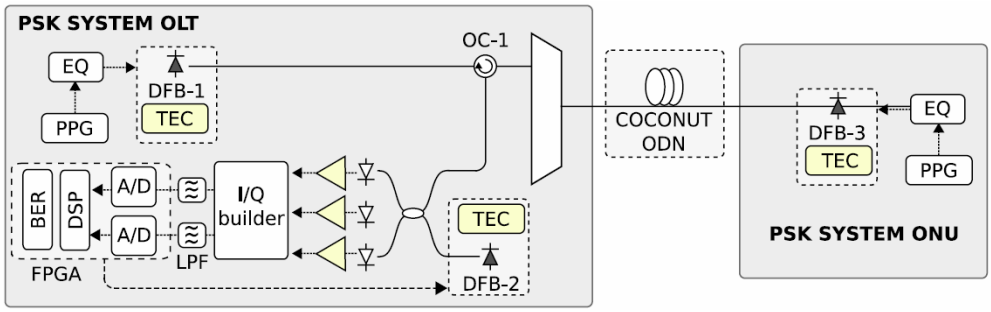

Figure 3.12: PSK Intradyne system setup. OC: Optical Circulator; TEC: Thermo-Electric Cooler; EQ: Equalizer; LPF: Low-Pass Filter; ODN: Optical Distribution Network [10].

Both orthogonal IQ signals were low-pass filtered by two standards 4^{th}-order Bessel filters with 1 GHz cut-off frequency, for antialiasing and noise suppression, then mapped into the digital domain by four ADC channels at 1.25 Gsps which two by two are interleaved to make sampling at 2.5 Gsps.

All the subsequent DSP was carried out by an ML605 Xilinx Virtex-6 FPGA with 8-bit architecture. Its process clock is set to 156.25 MHz for parallel processing of the real-time 1.25 Gbps data streaming.

In the FPGA, the deskew block first, cross-correlates the I and Q signals to compensate for the temporal delays related with non-symmetrical paths in the Rx front-end. The IQ skew is estimated when the receiver lights up, then the required shifting values in all (four) ADC channels are applied to the real-time data streaming. Next, the CLK recovery block down-sampled each I/Q signal, converting from two to one sample per symbol. The implemented algorithm is based on an interpolator to

find the optimal sampling point by looking at the maximum eye diagram aperture. The interpolation is carried out by a 4-tap FIR filter performing the cubic interpolation.

Then, a conventional CR including PR and FE blocks demonstrated in Figure 3.9 (upper), to perform only feed-back LO tuning (not feed-forward) was implemented. Accordingly, the estimated phase shift $\Delta\varphi$ due to the frequency error is fed-back towards the LO for automatic tuning. To make the feed-back loop, the estimated $\Delta\varphi$ controls the duty-cycle of a 20 kHz square wave to obtain a pulse-width modulation (PWM), which is later filtered in the analog domain by a low-pass resistor-capacitor (RC) network with a time constant of 10 ms. It becomes a simple 1-bit digital-to-analog converter (DAC) for continuous thermal tuning of the DFB LO.

3.2.2 Field-Trial Results for Real-Time Intradyne Receiver

The PSK intradyne system featured the best sensitivity of −53 dBm at a FEC level of 10^{-3} in back-to-back. Figure 3.13 shows the receiver performance and two sample eye diagrams, recorded at BER 10^{-9} and 10^{-3} in its polarization dependent configuration. As can be seen after propagation across the network, the performance is not altered significantly when the signal is transmitted in upstream with the other COCONUT channels. But, 4 dB power penalty appears in case of bidirectional transmission with US/DS channel separation of 6.25 GHz. Because, the reflection of the counter-propagating channels is aliased into the signal bandwidth.

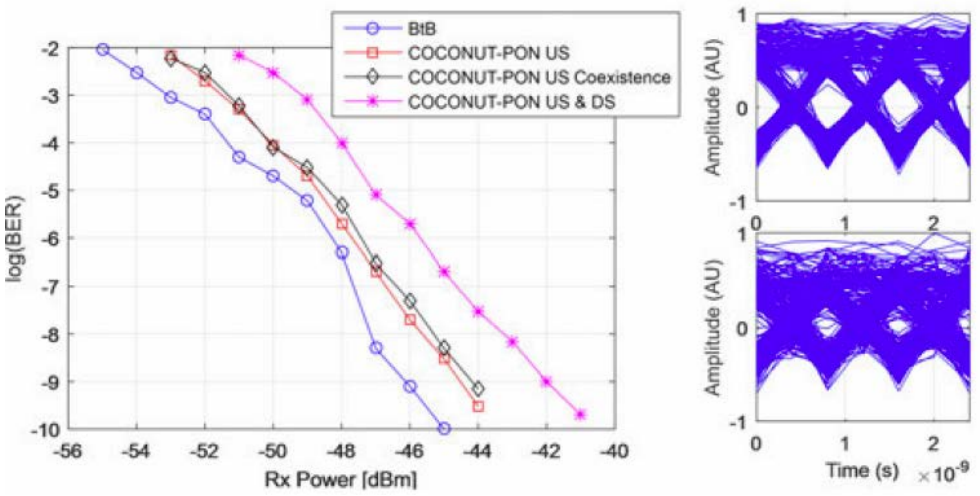

Figure 3.13: US DPSK system performance [10].

3.3 Real-Time Experimental Setup with Proposed CR

To evaluate our DSP for intradyne optical PSK receivers, as well as the proposed CR, another real-time experimental system is applied with DPSK data at 1.25 Gbps. In the new scenario, Tx performs in OLT and the Introdyne Rx including optical front-end and the DSP are operating in ONU, as shown in Figure 3.14.

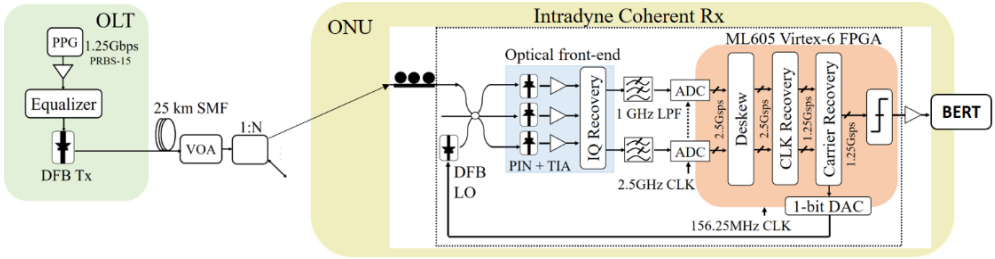

Figure 3.14: Experimental setup for real-time evaluation of the proposed CR with DPSK data at 1.25 Gbps.

After optical modulation, the signal is transmitted through 25 km of SMF. A variable optical attenuator (VOA) emulates for the optical distribution network losses. This

experiment only considers one state of polarization, which is manually adjusted at the input of the Rx.

As an upgrade of the Intradyne system in section 3.2.1, the DSP in this section includes the proposed CR for both feed-back and feed-forward operations with the architecture in Figure 3.9 (lower). Then, binary data is extracted by comparing with a decision threshold, and the real-time error rate is measured by a BER tester (BERT).

3.4 Results with Proposed CR

Initially, the optical transmission system including the DPSK Tx based on direct-DFB modulation and the digital Rx prototyped on the FPGA with both conventional and proposed CR algorithms, is lighted up, achieving error-free transmission of DPSK data at 1.25 Gbps in real-time. Next, the CR algorithm is optimized by evaluating the optimal block length (N_T) for averaging. The received optical power is adjusted to -53 dBm to provide a BER of 10^{-4}. The LO detuning is first set to an arbitrary value of 300 MHz, and the estimation of the frequency error Δf is evaluated 100 times for each value of N_T. Results are plotted in Figure 3.15, in terms of the root mean square (RMS) of the estimated Δf as a function of the block length N_T in symbols, for two different PRBS data. As observed, the estimation converges to the real LO detuning (300 MHz) for N_T larger than 200 symbols. In this work, we select $N_T = 2^8$ in agreement with the test. The same optimal N_T is observed for both PRBS data, as well as for both CR architectures [25].

Then, the system is evaluated in terms of sensitivity and tolerance to the phase noise from lasers, related with the total spectral linewidth Δν. For the test, three different lasers are used as LO: an ECL with narrow linewidth of 100 kHz, and two commercial DFB lasers with 4 MHz and 15 MHz linewidth respectively. Thus, the total spectral linewidth Δν, including the 4 MHz linewidth of the DFB Tx, ranged from 4 MHz to 19 MHz.

Results in Figure 3.16 show that, for a FEC threshold of BER = 10^{-3}, a high sensitivity of -55 dBm is achieved, with no apparent penalty for $\Delta\nu = 4$ MHz and $\Delta\nu = 8$ MHz. In the case of $\Delta\nu = 19$ MHz, the sensitivity penalty at FEC level is about 4 dB, exhibiting error-floor close to BER = 10^{-5}. Both CR architectures show similar performance. We remark that the achieved sensitivity of -55 dBm, operating at a ratio $\Delta\nu/R_b = 0.0064$ with total spectral linewidth $\Delta\nu = 8$ MHz, is the highest reported for a real-time experiment with optical coherent detection, to the best of our knowledge. It validates the high performance and robustness of differential detection despite its simplicity, and makes the proposed CR feasible for commercial low-cost DFB lasers [14], [25].

Figure 3.17 shows the normalized eye diagram for DPSK after CR and before data decision, for BER of 10^{-3} (a) and 10^{-9} (b) respectively.

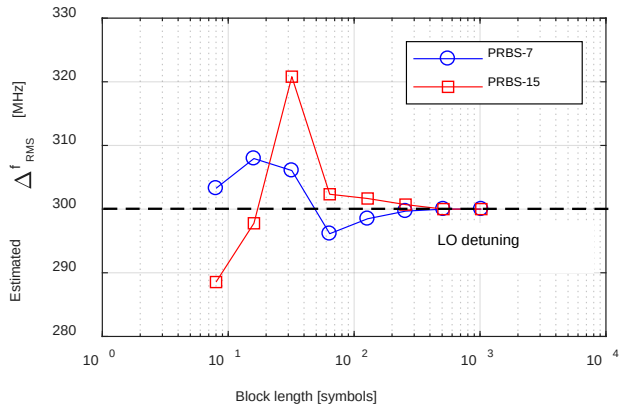

Figure 3.15 RMS of the estimated Δf against the block length N_T for averaging. The RMS value is calculated over 100 estimations for each value of N_T.

In the next test, the frequency error estimation and correction are assessed by sweeping the optical frequency of the LO operating in open loop (without LO feed-back for automatic tuning). Figure 3.18 shows the phase-shift Δφ induced by the LO detuning and estimated by the FPGA within the ±1 GHz range [14], [25]. Larger LO detuning values led to failure of the CLK recovery algorithm and synchronization

loss, then we restricted the estimation to ± 1 GHz range. As expected, the estimated phase exhibits cycle slips when the value goes beyond $\pm \pi/m$ ($\pm \pi/2$ for DPSK), the theoretical limit due to the m^{th}-power in FE. By implementing a simple phase unwrap algorithm [26], the estimated phase is completely linear over all the detuning. In addition, Figure 3.18 (right axis) also plots the analog signal measured at the output of the 1-bit DAC, going towards the LO for AFC.

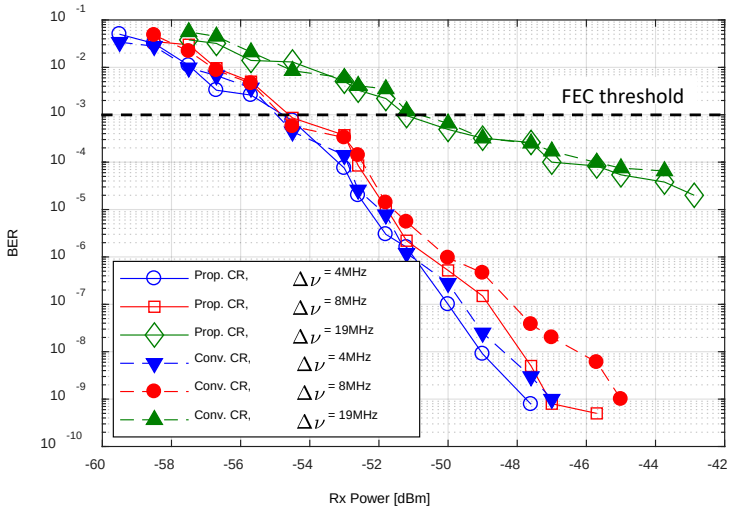

Figure 3.16 BER versus received power for DPSK at 1.25 Gbps, for the case of proposed (prop.) and conventional (conv.) CR, with different total spectral linewidth Δv.

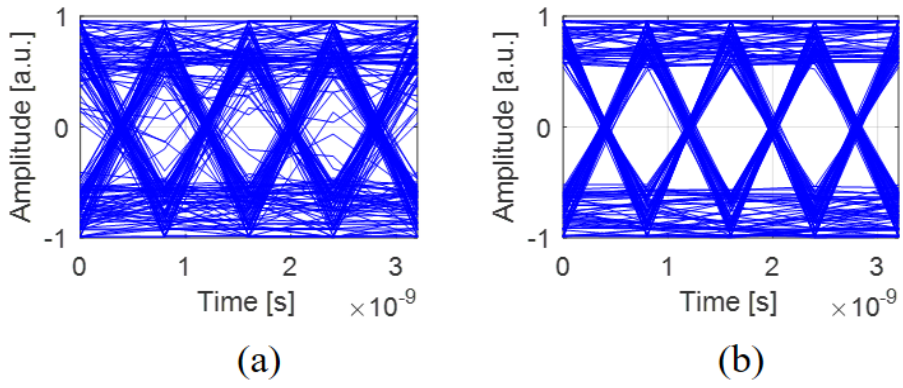

Figure 3.17: Normalized DPSK eye diagram after CR for (a) 10^{-3} and (b) 10^{-9} BER.

The BER curves in Figure 3.19 show the performance of CR without FE, and CR with the conventional and proposed algorithms, for two different values of total spectral linewidth. The received power is adjusted to obtain a reference BER = 10^{-4}. As observed, without FE the BER is highly degraded by the frequency detuning, with about $\pm$60 MHz tolerance for 1 dB sensitivity penalty. On the other hand, FE can effectively correct the frequency error up to $\sim \pm$400 MHz for 1 dB penalty even in presence of strong phase noise, without any difference between 4 MHz and 19 MHz total linewidth, for both CR architectures [14], [25].

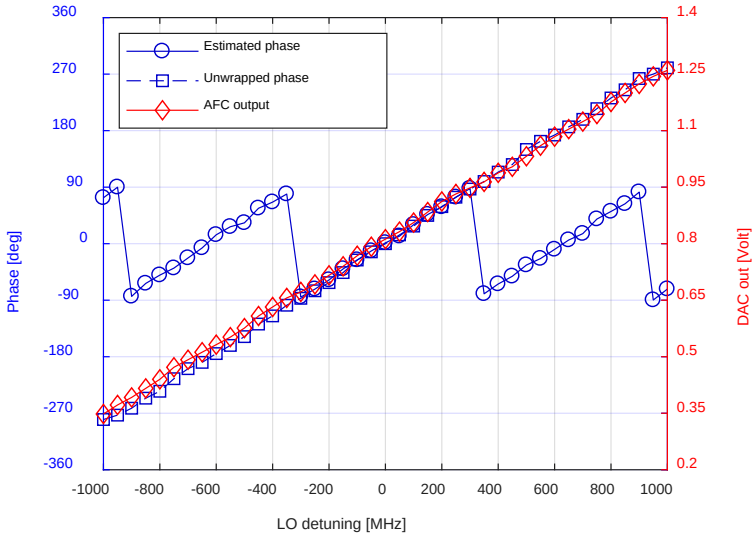

Figure 3.18: Estimated phase $\Delta\varphi$ for frequency error correction, and output of the 1-bit DAC for LO feed-back, as a function of the LO detuning.

Note that the reference BER = 10^{-4} is roughly constant within $\sim \pm$300 MHz detuning, but suffers degradation for larger detuning values. This behaviour is not related to incorrect estimation of the frequency error, which is linear for all the range (see Figure 3.19), but due to the bandwidth of the Rx that is adjusted to be 1 GHz for the 1.25 Gbps DPSK data. For large LO detuning the received spectrum falls beyond the Rx bandwidth, producing penalty at the detection.

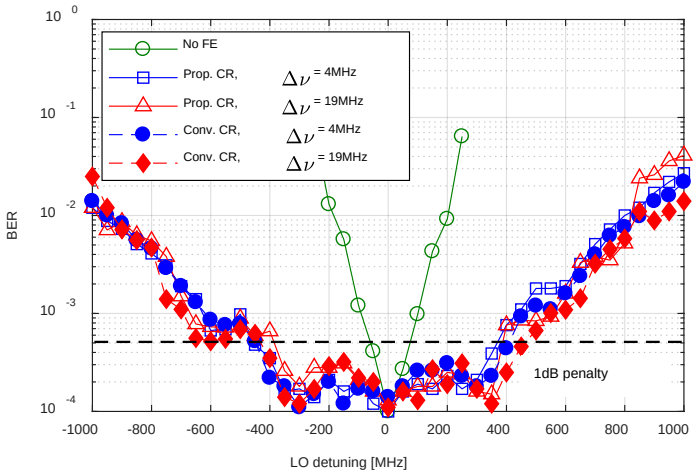

Figure 3.19: BER versus LO detuning for CR with/out FE, for the case of proposed (prop.) and conventional (conv.) CR, with different total spectral linewidth Δν.

At this point, we can see the benefit of simultaneous strategies to correct the LO frequency detuning: the feed-forward DSP corrects the remaining frequency error from each symbol in real-time, whereas the feed-back to the LO continuously adjusts its optical frequency by thermal tuning to maintain the photodetected spectrum in base-band and matched with the electrical filtering of the Rx, that rejects out-band noise and optimizes the detection. Although thermal tuning of commercial DFB lasers does not provide fast frequency drifts, with time constants in the order of seconds, it suffices for the rough correction of the LO detuning, taking into account that the rate of the frequency drifts from free-running DFB lasers due to environmental changes and laser fluctuations, as characterized in [27], is below 3.6 MHz/s.

Next test aimed to evaluate how fast the CR algorithm, prototyped in the FPGA, can effectively estimate and correct the frequency detuning. For this purpose, a triangle current waveform is applied to the bias current of the DFB Tx to produce an optical frequency dithering. The amplitude of the dithering is set to ±250 MHz with respect to its central frequency, to match it to the constant BER region of Figure 3.19, and

the frequency of the dithering is varied to determine the maximum tolerance. Figure 3.20 shows the electrical spectra after photodetection for DPSK data at 1.25 Gbps without dithering at the Tx (upper), and with ±250 MHz dithering amplitude (lower).

Results in Figure 3.21, show that the conventional CR can tolerate up to 70 kHz dithering frequency for 1 dB sensitivity penalty, whereas our proposed CR can tolerate up to 350 kHz due to the substantial reduction in the number of operations and process delay of the CR algorithm, as analysed in Table I, resulting in faster tracking of the frequency error. Note that for these high frequencies of the optical dithering the LO feed-back does not contribute any longer due to the limited speed of the thermal laser tuning. Hence, the frequency error correction is completely done by the DSP [14], [25].

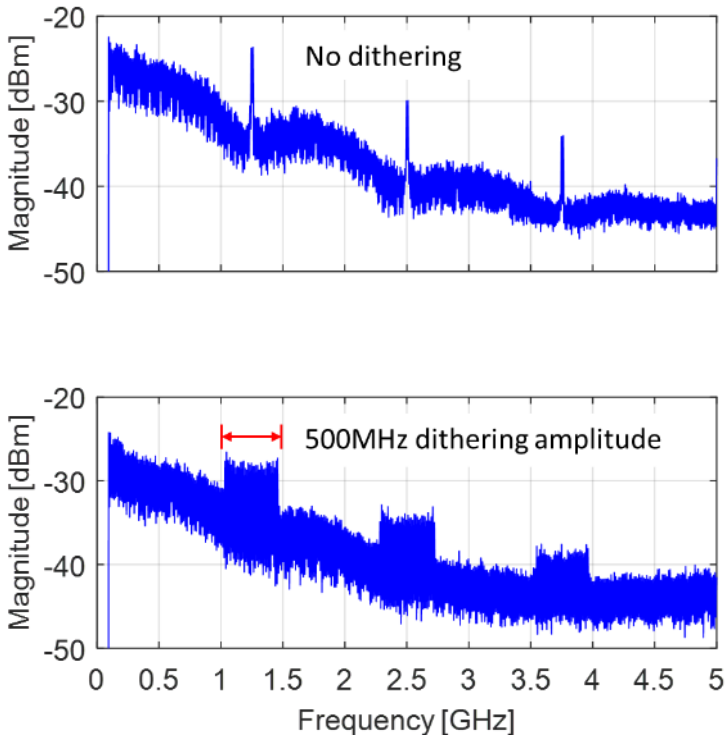

Figure 3.20: DPSK photodetected spectra at 1.25 Gbps for DFB Tx laser without optical frequency dithering (upper), and with ±250 MHz amplitude of the frequency dithering (lower).

Final test, evaluates the required channel spacing in the udWDM grid. The achieved high sensitivity of the coherent receiver which is -55 dBm, enables the power splitting for a large number of users, as large as 256, equivalent to $10 \cdot \log_{10}(1/256) = -24$ dB splitting losses. For the test, a second user (User 2) with another direct-DPSK modulated laser at 1.25 Gbps with uncorrelated data is located. The received power of User 1 is adjusted to obtain BER = 10^{-4} for the case of single user. Next, the optical frequency of User 2 is swept $\pm$10 GHz with respect to User 1 to calculate the power penalty at the reference BER. Figure 3.22 shows the electrical spectra after photodetection for two situations: both users emitting at the same optical power (upper), and User 1 emitting 15 dB lower than the interferer User 2 (lower). Then, emulates for the maximum allowed differential optical path loss, as specified in the ITU-T standard for NG-PON2 [28]. The signal-to-interference ratio (SIR) denotes the optical power ratio between User 1 and the interferer User 2. Results in Figure 3.21, in terms of the sensitivity penalty at BER = 10^{-4} as a function of the spectral separation between users, indicate that for a maximum sensitivity penalty of 0.5 dB, the 6.25 GHz channel spacing can be implemented in the udWDM-PON even for 15 dB differential link loss with adjacent channels. We also remark that the results in Figure 3.23 show the impact of a single adjacent channel interfering the measured channel; however, the conclusions for the minimum channel separation at 0.5 dB penalty can be extended to the complete udWDM scenario, where the users are interfered by two adjacent channels at each side, by adding ~0.6 dB extra penalty yielding to 1.1 dB total power penalty at BER = 10^{-4}. These results are obtained from direct laser modulation and band limited electronics influencing on the spectral width of the DPSK data. Further DSP at the transmitter for spectral shaping may lower the required channel spacing [25].

Although it is not experimentally tested in this chapter, the proposed CR also allows for detection of higher differential modulation formats, like DQPSK or 8-DPSK, to increase the spectral efficiency of the PON, which have already been demonstrated with direct-phase modulation and differential detection [29]. Therefore, a software-

defined transceiver scenario can be envisioned with this CR architecture, where the modulation format can be simply selected by changing the value of m.

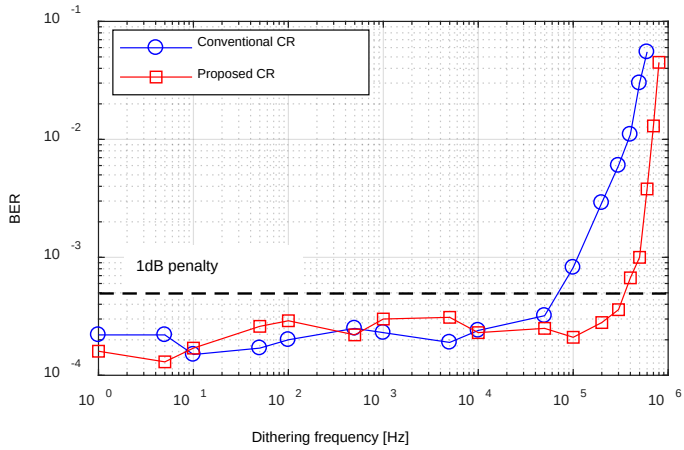

Figure 3.21: BER against frequency of the optical dithering for ±250 MHz amplitude of the dithering, with conventional and proposed CR architectures.

3.5 Conclusion

A DSP architecture with optimized CR architecture with less hardware resources based on differential detection for optical PSK intradyne receivers and using LUTs to store trigonometrical arguments, has been proposed and successfully tested in real-time.

The implemented DSP has been evaluated in real-time with DPSK data at 1.25 Gbps. Results show high sensitivity and tolerance to the phase noise, as well as robustness against the wavelength drifts of lasers, owing to simultaneous feed-forward DSP and feed-back LO tuning strategies for frequency error correction. The achieved sensitivity of -55 dBm in a 6.25 GHz spaced udWDM grid, with commercial DFB lasers, direct phase modulation, and low-cost optical front-end, demonstrates that a cost-effective PON can be implemented with user terminals based on low-cost devices, low-speed ADCs and low-complexity DSP techniques, but still achieving high performance.

Moreover, our developed DSP allows for fast reconfiguration to potentially detect multilevel modulation formats with the same digital receiver, intended for the future flexible optical networks with software-defined transceivers. Furthermore, the results validate that our optimized architecture is feasible with low-cost lasers for cost-effective transceivers in udWDM-PON.

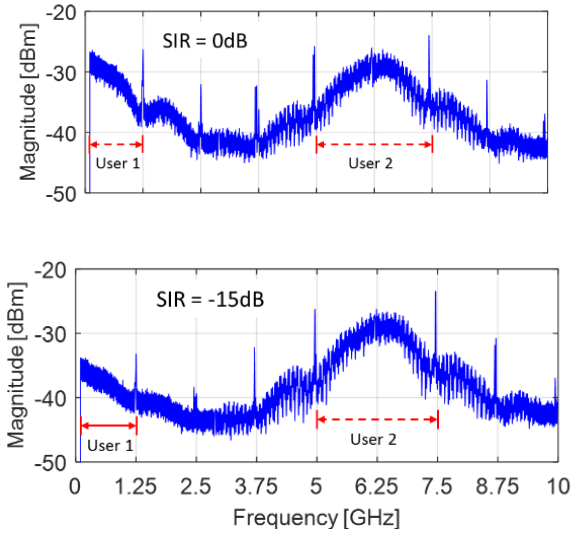

Figure 3.22: Photodetected spectra of two 1.25 Gbps DPSK users spaced by 6.25 GHz, for both users emitting at the same optical power (upper) and with 15 dB optical power difference (lower); SIR: signal-to-interference ratio.

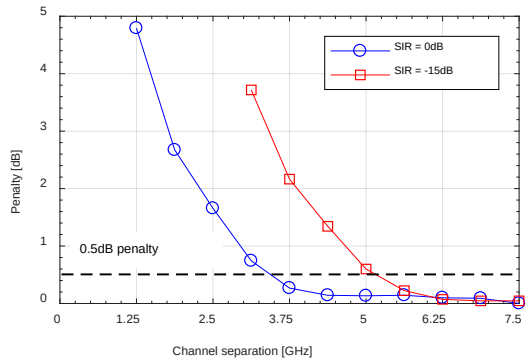

Figure 3.23: Sensitivity penalty at BER = 10^{-4} versus channel separation between DPSK users at 1.25 Gbps, for the two differential link loss scenarios depicted in Figure 3.22.

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Chapter 4. Optimized Carrier Recovery for Intradyne Optical DPSK Receiver

Introduction

In this chapter, we present a DSP with an optimized CR architecture for DPSK data that unlike other conventional ones, does not use m^{th}-power function (m = 2 for DPSK) and lookup tables (LUTs) for frequency error compensation. The LUTs that are referenced in this article, utilize block random access memory (RAM) resources on FPGA [1] to store some mathematical functions (e.g. trigonometric) numerically to avoid complicated implementations. The problem with the LUTs is that they produce delays due to extra processing to access to the values allocated on each address. Regarding to the size and application, the LUTs are also hardware and power consuming, because they may use thousands of active register or RAM resources. The proposed LUT-free CR in this chapter instead, by optimizing frequency estimation step and converting it directly to frequency compensation process using a simple mathematical operation, without losing the performance, saves hardware resources and reduces process clocks and power consumption on the FPGA.

We evaluate our proposal in a real-time experiment with a digital coherent Rx implemented on a commercial FPGA, an optical front-end based on low-cost 3×3

coupler, DFB lasers, and direct DPSK modulation at 1.25 Gbps. The operating principle of the proposed technique and the first real-time experimental results are reported in our previous work [2].

4.1 Proposed LUT-Free Carrier Recovery Architecture

As mentioned in chapter 3, in a conventional CR, including the differential m^{th}-power FE scheme [3] that is followed by differential demodulation for PR [4], the phase shift $\Delta\varphi$ between two consecutive samples that is caused by a frequency error between Tx and LO lasers, is estimated in FE. To compensate the frequency error, the accumulated frequency offset has to be subtracted from each symbol with corresponding symbol index in PR. It requires first, a complex correlation with one sample delay (z^{-1}), to extract the phase difference between samples, and the m^{th}-power estimator. Then, another complex correlation for differential demodulation with P sample delay (z^{-P}), where $P = R_s/R_b$ represents the oversampling factor defined as the ratio between the sample rate (R_s) and the symbol rate (R_b).

By placing the CLK Recovery before CR ($P = 1$), both FE and PR have the same 1-symbol complex correlation. Thus, the conventional CR can be simplified to perform the 1-symbol complex correlation only once. Based on this idea, a differential m^{th}-power (DMP) based CR, which is an optimization of the conventional one, was presented in [5], the same which was described in chapter 3.

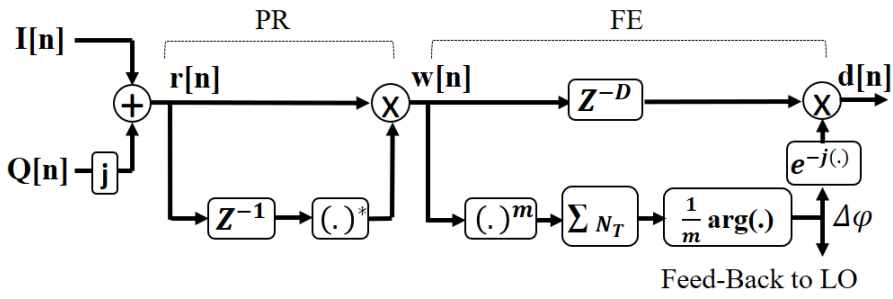

Figure 4.1: DMP CR architecture presented in [5].

The DMP CR is shown in Figure 4.1, where m is the number of constellation points of the PSK modulation, N_T is the averaging length in number of symbols, D is the process delay (number of clocks) of the FE algorithm, and $(\cdot)^*$ stands for complex conjugate.

As this structure assumes CLK recovery before CR, In-phase ($I[n]$) and Quadrature ($Q[n]$) signals are at one sample per symbol. By considering m = 2 due to the DPSK modulation format, the phase shift $\Delta\varphi$ produced by the frequency error is given by:

$$\Delta\varphi = \frac{1}{2}\arg\left(\frac{1}{N_T}\sum_{n=0}^{N_T-1}(w[n])^2\right) \tag{4.1}$$

where $w[n]$ is the differentially demodulated signal at the PR output in Figure 4.1. Real and imaginary parts of the $w[n]$ are given by:

$$\begin{aligned} Re\{w[n]\} &= I[n]I[n-1] + Q[n]Q[n-1] \\ Im\{w[n]\} &= Q[n]I[n-1] - I[n]Q[n-1] \end{aligned} \tag{4.2}$$

Furthermore, as DPSK is a constant-envelope modulation format with constant radius in the complex plane, the following trigonometrical relations are valid:

$$\begin{aligned} sin(\Delta\varphi) &= \tfrac{1}{N_T}\textstyle\sum_{n=0}^{N_T-1}(|Im\{w[n]\}|) \times u_I \\ cos(\Delta\varphi) &= \tfrac{1}{N_T}\textstyle\sum_{n=0}^{N_T-1}(|Re\{w[n]\}|) \times u_R \end{aligned} \tag{4.3}$$

where the averaging counteracts the additive channel noise; the absolute value is to remove the DPSK data instead of the *2nd*-power, and u_I and u_R are coefficients to recover the sign of $\Delta\varphi$ after averaging the absolute value.

Table 4.1 Decision rules based on Re, Im and $\Delta\varphi$

Decision	Region of $\Delta\varphi$
$\lvert Re\rvert > \lvert Im\rvert$, $Re \times Im > 0$	$0 < \Delta\varphi < \frac{\pi}{4}$, $-\pi < \Delta\varphi < \frac{-3\pi}{4}$
$\lvert Re\rvert > \lvert Im\rvert$, $Re \times Im < 0$	$\frac{3\pi}{4} < \Delta\varphi < \pi$, $\frac{-\pi}{4} < \Delta\varphi < 0$
$\lvert Re\rvert < \lvert Im\rvert$, $Re \times Im > 0$	$\frac{\pi}{4} < \Delta\varphi < \frac{\pi}{2}$, $\frac{-3\pi}{4} < \Delta\varphi < \frac{-\pi}{2}$
$\lvert Re\rvert < \lvert Im\rvert$, $Re \times Im < 0$	$\frac{\pi}{2} < \Delta\varphi < \frac{3\pi}{4}$, $\frac{-\pi}{2} < \Delta\varphi < \frac{-\pi}{4}$

From Eq. (4.2) and the complex plane, the u_I and u_R are calculated based on decision rules over (averaging of) the Re and Im, which stand for Re{w[n]} and Im{w[n]}, respectively, as summarized in Table 4.1. Thus

$$u_R = \begin{cases} +1\ , & -\frac{\pi}{2} < \Delta\varphi < \frac{\pi}{2} \\ -1\ , & elsewhere \end{cases}\ ,\quad u_I = \begin{cases} +1\ , & 0 < \Delta\varphi < \pi \\ -1\ , & elsewhere \end{cases} \tag{4.4}$$

As expected on the complex plane, due to the use of absolute value in Eq. (4.3), the estimated phase region exhibits cycle slips when the value goes beyond $\pm\pi/2$. By implementing a simple phase unwrap algorithm [6], the correct estimation of u_I and u_R are considered for $-\pi \leq \Delta\varphi \leq \pi$.

The Eq. (4.3) is a key formula to simplify the DMP CR with an LUT-free architecture, while $\arg(.)$ and $e^{-j(.)}$ functions in the FE were required to be implemented on the FPGA by applying three LUTs [7], [8] . Using CORDIC (coordinate rotation digital computer) was another approach to reduce mathematical operations and hardware resources [9]. As shown in Figure 4.1, the frequency error compensation is obtained by:

$$d[n] = w[n] \times e^{-j\Delta\varphi} \tag{4.5}$$

where $d[n]$ is the recovered signal and $e^{-j\Delta\varphi} = cos(\Delta\varphi) - jsin(\Delta\varphi)$. The DPSK

modulation has only two constellation points with real values. Accordingly, the real component of Eq. (4.5) would show the recovered DPSK data, and imaginary component can easily be discarded. Taking into account the real component of Eq. (4.5), with respect to Eq. (4.2) and Eq. (4.3), $d[n]$ is given by:

$$d[n] = Re \times \left(\frac{1}{N_T}\sum_{n=0}^{N_T-1}(|Re|)\right) \times u_R + Im \times \left(\frac{1}{N_T}\sum_{n=0}^{N_T-1}(|Im|)\right) \times u_I \quad (4.6)$$

To extend Eq. (4.6) for higher modulation formats, such as QPSK, that is our future research, the imaginary component certainly should be remained in the equation.

Figure 4.2 shows practical implementation of the proposed architecture for CR based on Eq. (4.6), with the differential PR (the same as in Figure 4.1) followed by Frequency Compensation (FC), where *N* represents the number of parallel symbols processed by the FPGA, and *Control Unit* makes the decision rules yielding the u_R and u_I with binary values to control multiplexers (MUXs) to pass either the current input or logical *NOT* of that input. In this case, the MUX is an alternative for the multiplier to relax the hardware resources. In addition, the multiplication $Re \times Im$ and the associated averaging block in FC, which are a part of the decision rules, could be replaced by two comparators (e.g. $Re > 0$ and $Im > 0$) after averaging of each component followed by the modified *Control Unit*. To make the feed-back loop, *1-bit DAC Controller* block, by using $sin(\Delta\varphi)$ function, controls the duty-cycle of a 20 kHz square wave to obtain a pulse-width modulation (PWM), that is filtered in the analog domain by a low-pass RC network with a time constant of 10 ms, for continuous thermal tuning of the low-cost DFB LO [2].

4.2 Hardware Resources

As summarized in Table 4.2, a reduction of 40% in the number of adders, 42% for total number of multipliers, and 61% fewer clocks to process with an LUT-free architecture in comparison with the DMP CR, is achieved. The number of clocks is related to the process delay of the CR.

Furthermore, Table 4.3 shows detailed information for implementation of the hardware resources on Xilinx Virtex-6 FPGA in terms of Flip Flops (FFs), Lookup table Flip Flop pairs (LUT-FF), Shift Register Lookup tables (SRLs), DSP blocks and Fast Carry Logics with Look Ahead (Carry4s), for the LUT-free CR, in comparison with the DMP and conventional CRs.

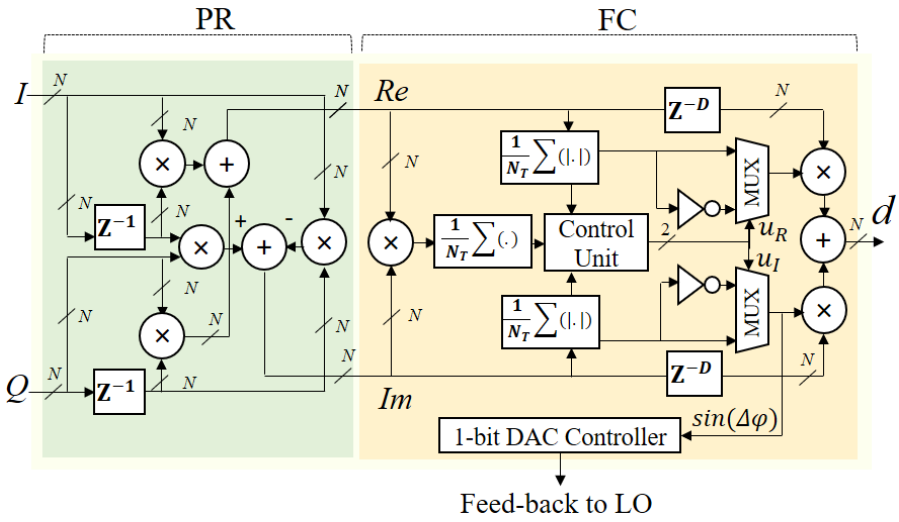

Figure 4.2: Hardware architecture for the proposed LUT-free CR.

Table 4.2 Hardware Resources in terms of Adders, Multipliers, number of required process clocks and LUT for the DMP and proposed CR, implemented on Virtex-6 FPGA.

Approach	**Add.**	**Mult.**	**LUT**	**#Clk**
DMP CR	10×*N*-2	12×*N*	3	23
Prop. CR	6×*N*-3	7×*N*	0	9
Reduction	**40%**	**42%**	**100%**	**61%**

A power analysis using Xilinx Xpower Analyzer tool [10] also shows that the proposed hardware consumes 85% and 95% less power than the DMP and the conventional CR which was implemented in chapter 3, respectively. This

optimization of power results in 14% and 34% savings of total power of DSP Rx on Virtex-6 FPGA, in comparison with the use of DMP and conventional CR architectures, respectively. Likewise, such optimization could be useful in coherent optical transceiver implementations on Application-Specific Integrated Circuit (ASIC) [11].

Table 4.3 Hardware Resources in terms of FFs, LUT-FF, SRL, DSP, Carry4, and power consumption on Virtex-6 FPGA.

Approach	**FF**	**LUT-FF**	**SRL**	**DSP**	**Carry4**	**Power (W)**
Conv. CR	7608	14271	1378	120	1874	0.06878
DMP CR	4472	7978	550	72	1217	0.0235
Prop. CR	1095	652	192	24	107	0. 0035
Reduction (Prop. to DMP.)	**76%**	**92%**	**65%**	**67%**	**84%**	**85%**
Reduction (Prop. to Conv.)	**86%**	**95%**	**86%**	**80%**	**94%**	**95%**

4.3 Real-Time Experimental Setup

To evaluate the proposed CR, a real-time experiment is implemented with NRZ-PRBS data, from a PPG running at 1.25 Gbps. The optical setup is exactly the same setup as Figure 3.12 in chapter 3. In the DSP side, the Deskew, CLK Recovery, Symbol Estimation and Decoding modules are the same as chapter 3. But to improve the performance, Normalization block is added as shown in Figure 4.3. The Tx uses a DFB laser ($\lambda = 1550$nm) with spectral linewidth $\Delta\nu = 4$ MHz, emitting at 0 dBm, that is properly equalized by a high-pass RC network for direct 0-180º phase modulation [12]. The signal is sent through 25 km of SMF, and a VOA emulates the optical distribution network losses. This experiment only considers one state of

polarization, manually adjusted at the input of the Rx.

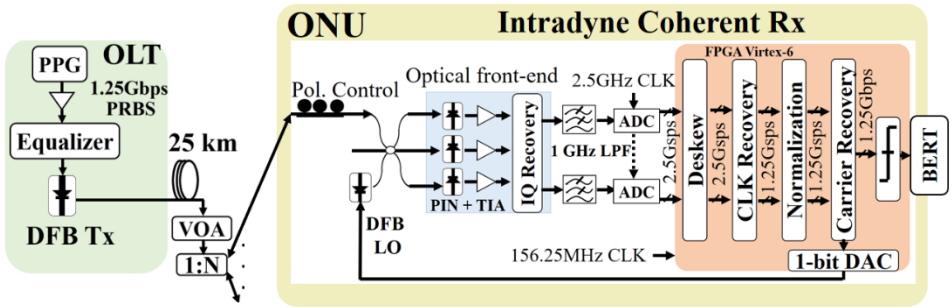

Figure 4.3: Experimental setup for real-time evaluation of the proposed LUT-free CR with DPSK data at 1.25 Gbps.

The coherent Rx includes a free-running LO to operate in intradyne regime. The LO is another DFB laser emitting at 3 dBm, and thermally-tuned for AFC from the DSP feed-back. The optical front-end is based on 3×3 coupler to beat the incoming optical signal with the LO. The three photodetected signals are linearly combined in passive hardware, according to the transfer matrix pointed in [13], to recover the I and Q components. Although IQ recovery can be performed by the DSP, this analog pre-processing saves one ADC channel, whose cost increases with its sample rate.

All the subsequent DSP is carried out by an ML605 Xilinx Virtex-6 FPGA board with 8-bit architecture. Its process clock is set to 156.25 MHz for parallel processing of the real-time 1.25 Gbps data streaming.

4.4 Results

The proposed and DMP CR are optimized by assigning $N_T = 256$ as an efficient value for the number of symbols in the averaging block, based on the experiments reported in Figure 3.13 from chapter 3. For sensitivity test, and tolerance to the phase noise from DFBs, three different lasers are used as LO: an ECL with narrow linewidth of 100 kHz, and two DFB lasers with 4 MHz and 15 MHz linewidth respectively. Therefore, the total spectral linewidth $\Delta\nu$, including the 4 MHz linewidth of the Tx,

ranges from 4 MHz to 19 MHz at a ratio $\Delta\nu/R_b$ from 0.0032 to 0.0152. Results in Figure 4.4 show that for a FEC threshold of BER = 10^{-3}, a high sensitivity of -54 dBm is achieved for $\Delta\nu$ = 4 MHz and 8 MHz, with less than 1 dB penalty in comparison to the DMP CR.

In the next test, the frequency error correction is assessed by sweeping the optical frequency of the LO operating in open loop, without LO feed-back for automatic tuning. The BER curves in Figure 4.5 show the performance of CR with/out FE (for the DMP) and FC (for the proposed), within the $\pm$1 GHz range of the LO detuning for two different values of total spectral linewidth. The received power is adjusted at -52 dBm for $\Delta\nu$ = 4 MHz, and at -46 dBm for $\Delta\nu$ = 19 MHz to get a reference BER = 10^{-4}. As observed, FC can effectively correct the frequency error for 4 MHz and 19 MHz total linewidth, and both CR architectures perform the same. The reference BER is roughly constant within ~ $\pm$300 MHz detuning, but suffers degradation for larger detuning values. This behaviour is not related to incorrect estimation of the frequency error, but due to the bandwidth of the Rx that is adjusted to be 1 GHz for the 1.25 Gbps DPSK data [5], [7].

We also aim to evaluate how fast the proposed CR, implemented on the FPGA, can effectively correct the frequency detuning. For this purpose, a triangle current waveform is applied to the bias current of the DFB Tx to produce an optical frequency dithering. The amplitude of the dithering is set to $\pm$250 MHz, within the constant BER region of Figure 4.5, and the frequency of the dithering varies to determine the maximum tolerance. Figure 4.6 shows that the LUT-free CR can tolerate up to 700 kHz dithering frequency for 1 dB sensitivity penalty, almost twice and fourteen times more than the DMP and the conventional CRs, respectively. This improvement was expected because the LUT-free scheme needs less process clocks that makes it faster to track the frequency errors. It is relevant to mention that, due to the frequency dip in the FM response of the Tx laser [14], it is not possible for us to generate optical frequency dithering beyond this frequency. Thus, our measurements are limited up to 800 kHz of dithering.

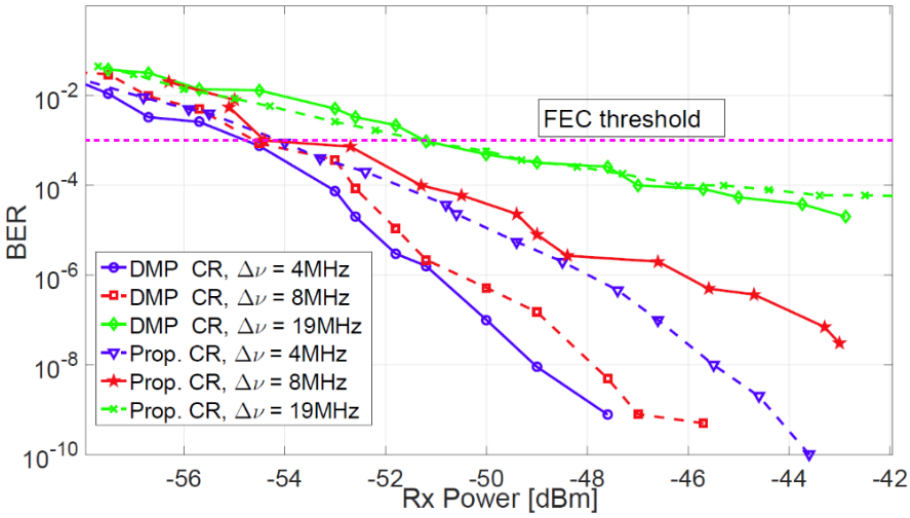

Figure 4.4: BER versus received power for DPSK at 1.25 Gbps, for the proposed (Prop.) and DMP CR, with different total spectral linewidth $\Delta\nu$.

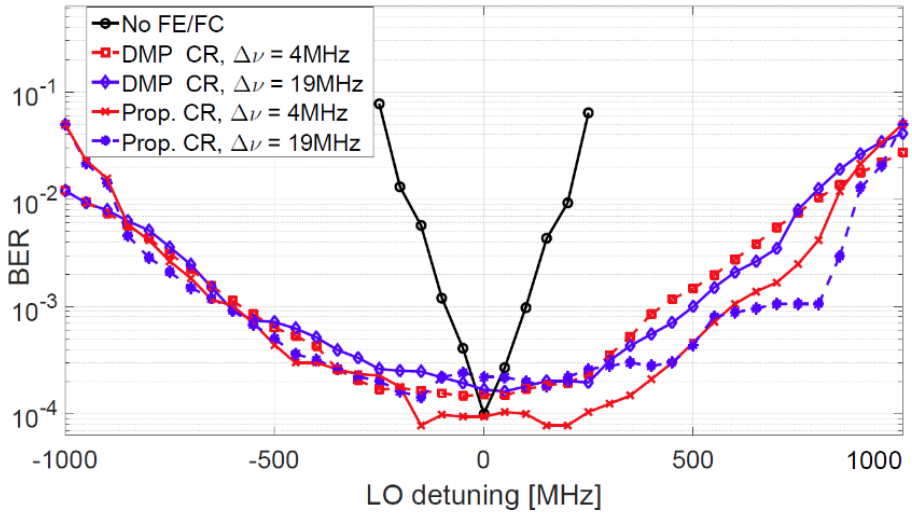

Figure 4.5: BER versus LO detuning with/out FE/FC, for the proposed (Prop.) and DMP CR with different total spectral linewidth $\Delta\nu$.

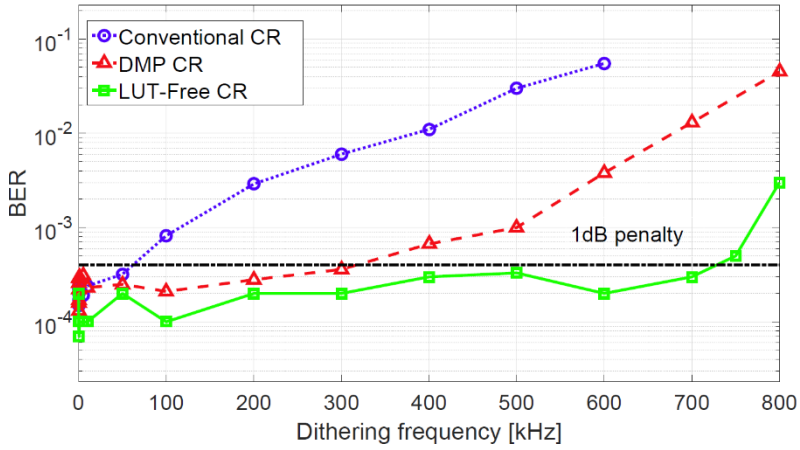

Figure 4.6: BER vs. frequency of the optical dithering for ±250 MHz amplitude of the dithering, with conventional, DMP and LUT-free CR architectures.

As a final test, the required channel spacing in the udWDM grid is evaluated. The achieved high sensitivity of the coherent receiver (-54 dBm) enables the power splitting for a large number of users, as large as 256. For the test, a second user (hereafter User 2) with another direct-DPSK modulated laser at 1.25 Gbps with uncorrelated data is placed. The received power of User 1 is adjusted to obtain BER = 10^{-4} for the case of single user, then the optical frequency of User 2 is swept $\pm$10 GHz with respect to User 1 to compute the power penalty at the reference BER. Figure 4.7 shows the electrical spectra after photodetection for three considered scenarios: User 1 emitting 15 dB higher than the interferer User 2 (upper), both users emitting at the same optical power (middle), and User 1 emitting 15 dB lower than the interferer User 2 (lower). The first and the last emulate for the maximum allowed differential optical path loss, as specified in the ITU-T standard for NG-PON2 [15]. The SIR denotes the optical power ratio between User 1 and the interferer User 2.

Results in Figure 4.8, in terms of BER as a function of the spectral separation between users, indicate that the 6.25 GHz channel spacing can be implemented in the udWDM-PON even for 15 dB differential link loss with adjacent channels. An important conclusion of the test SIR = -15 dB, is that in the process of the wavelength assignment for a new user connecting to the PON, the allocation process can be

achieved without interfering to the other active users, if the new user transmits 15 dB less power than the already active users [16]. Thus, correct static and dynamic wavelength assignment could be done [17].

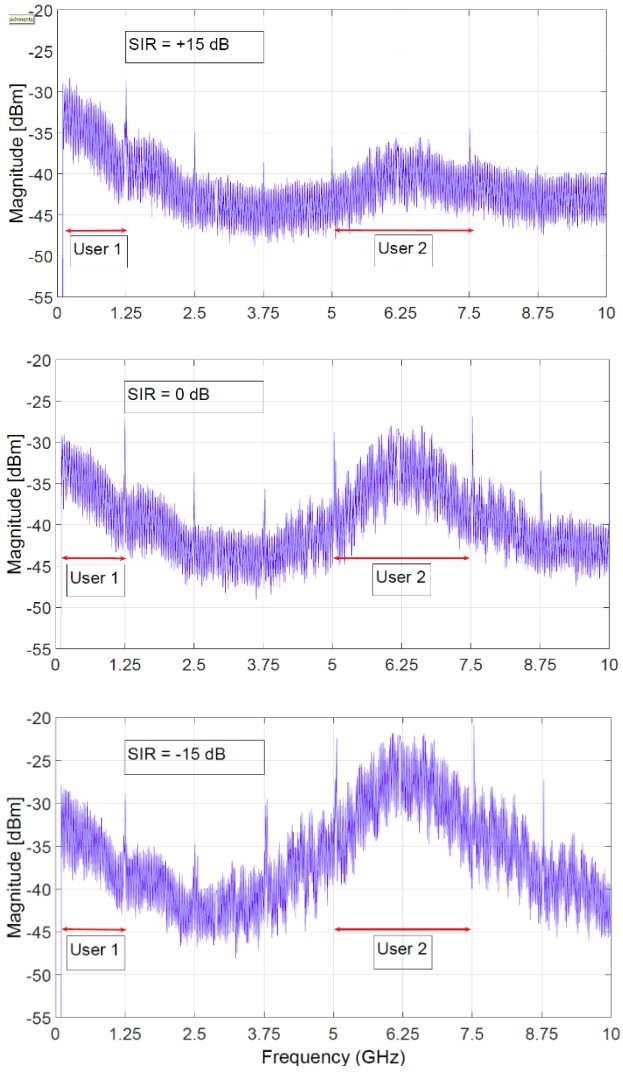

Figure 4.7: Photodetected spectra of two 1.25 Gbps DPSK users spaced by 6.25 GHz, for User 1 emitting 15 dB higher than the interferer User 2 (upper), both users emitting at the same optical power (middle), and User 1 emitting 15 dB lower than the interferer User 2 (lower).; SIR: signal-to-interference ratio.

These results are obtained from direct laser modulation and band limited electronics influencing on the spectral width of the DPSK data. Further DSP at the transmitter for spectral shaping may lower the required channel spacing as low as 3.75 GHz [18].

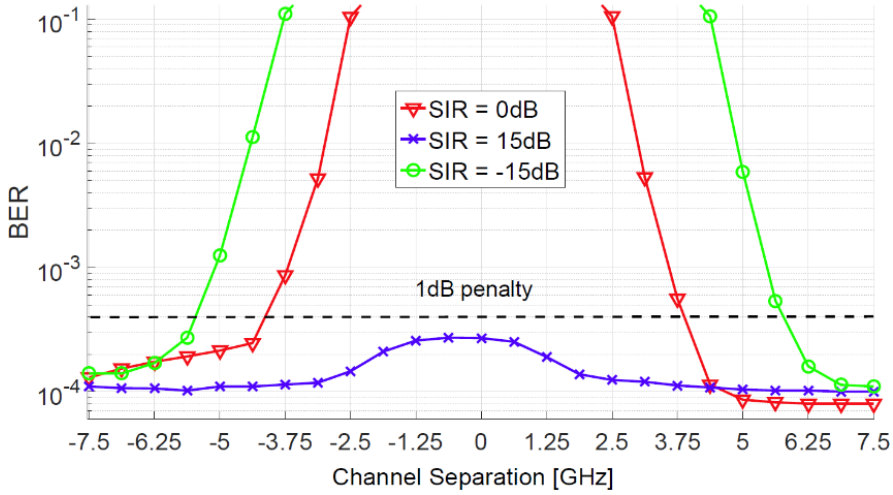

Figure 4.8: BER of user 1, vs. spectral separation of two 1.25 Gbps DPSK users spaced by 6.25 GHz, for SIR = 0dB, SIR = 15dB, and SIR = -15 dB.

4.5 Conclusion

In this chapter, an LUT-free CR architecture for DPSK intradyne receivers has been proposed and successfully tested in a real-time optical transceiver. The implementation on FPGA is done with reduction of ~41% DSP hardware resources, 61% fewer required process clocks, and 85% less power consumption, in 14% saving of total power of DSP Rx on Virtex-6 FPGA, in comparison with the previous CR (DMP) implementations as well as 34% rather than DSP Rx with the conventional CR. Moreover, in a 6.25 GHz spaced udWDM grid, with commercial DFB lasers, direct phase modulation, sensitivity of -54 dBm at a ratio $\Delta\nu/R_b = 0.0064$ and BER = 10^{-3} as well as feed-forward frequency error correction and high robustness against the fast frequency laser drifts is achieved. The results validate that our proposed CR is feasible with low-cost lasers for cost-effective transceivers in the udWDM-PON.

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Chapter 5. Symbol-rate Polarization Independent DSP for Intradyne Optical M-PSK Receivers in udWDM-PON

Introduction

A coherent Rx with polarization diversity (POD) architecture is commonly applied to overcome the difference between the state-of-polarization (SOP) of Tx and LO lasers. Low-cost implementations as well as the use of FPGAs in DSP as a robust and flexible approach are key technologies for development of the coherent Rx [1], [2].

In this chapter, we present a DSP architecture with a simple clock recovery for POD intradyne optical PSK Rx using only one sample per symbol (1-sps). This enables implementation of the coherent Rx with lower ADC cost without increasing the hardware complexity of previous works [3], [4], [5] and insensitive against the SOP. We evaluate our proposal in a real-time experiment with a digital coherent Rx implemented on a commercial FPGA, optical front-end based on low-cost 3×3 couplers, DFB lasers, and direct DPSK modulation at 1.25 Gbps.

5.1 Symbol-Rate DSP Architecture

As was mentioned in chapter 2, in the POD intradyne coherent Rx, there are four photocurrents [6]. Since we have a 4-channel ADC, with the sampling rate of $R_s = R_b$ for each channel, available, all the four photocurrents must be digitalized only at one sample per symbol (1-sps). So, instead of changing the hardware and providing expensive ADCs, we decided to keep the cost low, but to find solutions to process the received signals at symbol-rate (1-sps). For this purpose, we have developed a clock recovery that in one hand tunes the sampling frequency of the ADCs exactly at the rate of the received data, and on the other hand, keeps the sampling point in the best place of the symbol, to create the best aperture for the signal eye diagram. In the followings, we describe our technique to develop a symbol-rate DSP for intradyne PSK receivers.

5.1.1 Proposed Symbol-Rate Clock Recovery

It was shown in [7] that the received clock, can be extracted from the line spectrum of Fast Fourier Transform (FFT) of the signal's power. A clock recovery subsystem should 1) generate clock at the received signal speed, and 2) correctly tune the sampling phase in the optimum point. The clock recovery which is proposed by [7], doesn't provide a solution for tuning the sampling phase. In this section, we analyse a simple clock recovery that has only 1-sps data processing.

It is expected that the sampled complex amplitudes of two POD received signals r_H and r_V in digital domain are given by:

$$r_H[n] = (I_H[n] + jQ_H[n]) * h[n] \tag{5.1}$$

$$r_V[n] = (I_V[n] + jQ_V[n]) * h[n] \tag{5.2}$$

where I and Q are in-phase and quadrature components, h is the impulse response of radio frequency (RF) filters that are placed before ADCs, and n is symbol index. We

assume that h is the low-pass standard 4^{th}-order Bessel filter with 1 GHz cut-off frequency, the same that we use in our laboratory, for antialiasing and noise suppression, with transfer function $HL(f)$ as shown in Figure 5.1:

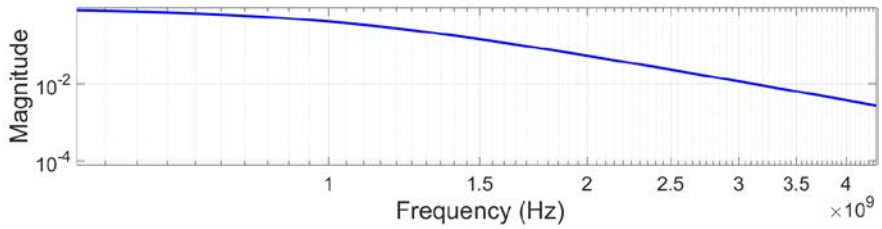

Figure 5.1: $HL(f)$: low-pass 4^{th}-order Bessel filter.

Considering the low-pass filter h, total received power P in the receiver from both H and V (H: horizontal, V: vertical) polarizations is given by:

$$P_H = r_H \,.\, r_H^* \tag{5.3}$$

$$P_V = r_V \,.\, r_V^* \tag{5.4}$$

$$P = P_H + P_V \tag{5.5}$$

where the spectrum of P is shown in Figure 5.2:

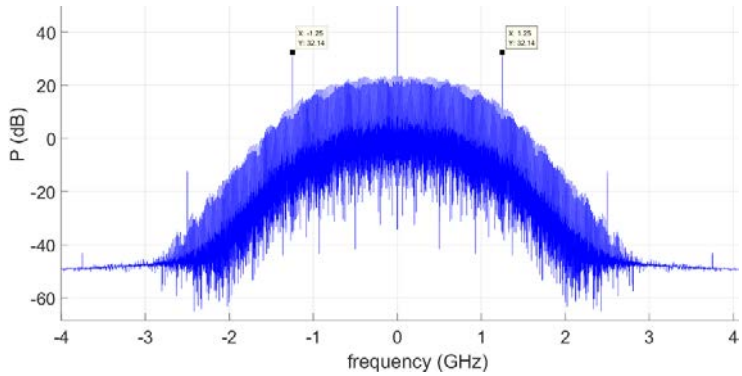

Figure 5.2: Spectrum of the P, with line spectral lines at R_b= 1.25 Gbps, for DPSK signal at 1.25 Gbps.

Consequently, from the spectral line at R_b the clock of received signal is extracted, by either the PLL circuit, or in our proposed method by FPGA. We have applied the FPGA to generate a fixed clock with the dynamic phase-shift for the ADCs [8]. A dynamic phase shifting, can reduce or increase the clock frequency. As observed in Figure 5.2, the maximum received power, can be detected at the baudrate of received signal. Also, it is obvious that better sampling point on the received signal, results in more open eye-diagram as well as further received power. Thus, by comparing the total received powers in consecutive of N_T intervals at R_b, and by applying a corresponding maximum finder, a sampling-phase error detector (SED), can be implemented. For this purpose, DSP needs four signals I_H, Q_H, I_V and Q_V to process and to recover the transmitted data. As a result, four ADCs or a 4-channel ADC, each channel operating at R_s (sample rate), normally twice of R_b (symbol rate) is required in a conventional Rx.

This chapter aims to keep the same ADC, FPGA and DSP complexity, as well as the same modulation format and rate introduced in [5] (with DPSK) and [4] (with PSK), but extending the capabilities of the Rx for POD by means of the clock recovery which is operative using only 1-sps data processing. Therefore, it should accurately estimate and compensate the timing error in presence of optical signal carrier corrupted by noise. To obtain the total power of the POD received signals r_H and r_V, we calculate the complex modulus from Eq. (5.1) and (5.2), then add the products. In this way, based on the fixed optical power of the LO and transmitted data for PSK which is a constant-envelop modulated format with constant radius in the complex plane, the power of received signals remains constant. Thanks to the band-limited impulse response $h[n]$, the optimum sampling point results in the maximum amplitude of the calculated signal power. In this case, by a corresponding gradient ascent algorithm, the best sampling point can be achieved. Accordingly, the 1-sps SED scheme is implemented as shown in Figure 5.3, where averaging counteracts the additive channel noise, N_T is the averaging length in number of symbols and ε_τ is the

sampling phase error. P_H, P_V are the received power from horizontal and vertical SOPs, respectively, and P is the total received power in electrical domain.

The $\langle \frac{(.)}{|.|} \rangle$ operation in Figure 5.3 yields the sign, and for simplicity it is done just by observing the sign bit of its input value in binary, resulting in a 1-bit number for the 1-bit multiplier. The multiplexer (MUX) is to prevent passing the value '0' through the feed-back, to avoid an infinite loop with the '0' in output. If the select (Sel.) port is either -1 or 1, it passes the Sel., else, the MUX output will be 1. As a result, ε_τ can be one of these three values: -1, 0 and 1, when the current sampling from the best (maximum) point is late, ideal, and early, respectively. Next, ε_τ drives a mixed mode clock manager (MMCM) [9], which dynamically shifts the phase of a fixed reference clock (Ref. clock). Depending on the ε_τ, output of MMCM is a negative, zero, or positive phase-shifted clock with resolution of $\varepsilon_\tau \times$23ps. It plays the role of a reference clock for a GTX transceiver [10], with an input pattern of "0101" to transmit, that results in a clock whose phase is continuously adjusted by the ε_τ, as another reference clock input for the ADCs. Thus, the proposed clock recovery includes the SED, the MMCM and the GTX transceiver [8].

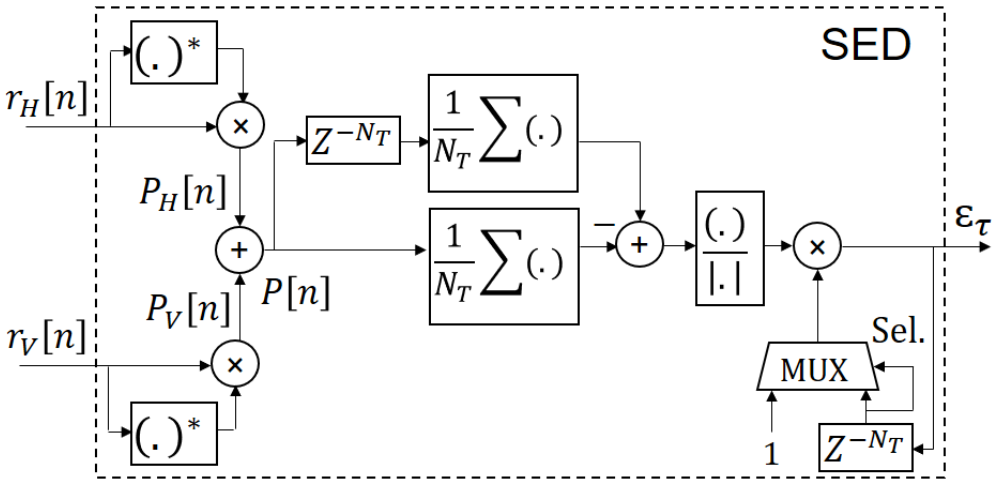

Figure 5.3: Sampling-phase error detector (SED) by using 1-sps for POD coherent PSK Rx.

5.1.2 Proposed Symbol-Rate DSP

A symbol-rate DSP for POD coherent PSK Rx operating at 1-sps, including clock recovery and differential-detection-based carrier recover (CR) [4], is developed as shown in Figure 5.4, where m is the number of constellation points of the PSK modulation.

The term N_T is the block length for averaging in the number of symbols for FE (as well as in SED) in the CR, and $d[n]$ is the recovered data. The MMCM Ref. clock comes from either an on-board oscillator or an external source. In this architecture, an LUT-Free CR [5] for DPSK data can be applied as well, and we call it LUT-Free DSP. Figure 5.5 shows the FPGA implementation of the symbol-rate LUT-Free DSP.

Our clock recovery technique could be comparable with work in [7], which used phase-locked loop (PLL) circuit to restore the clock at frequency of R_b to control sampling instances for the ADCs. We remark that the proposed clock recovery is fully digitalized and without using any external analog circuit, it can be implemented on the FPGA easily.

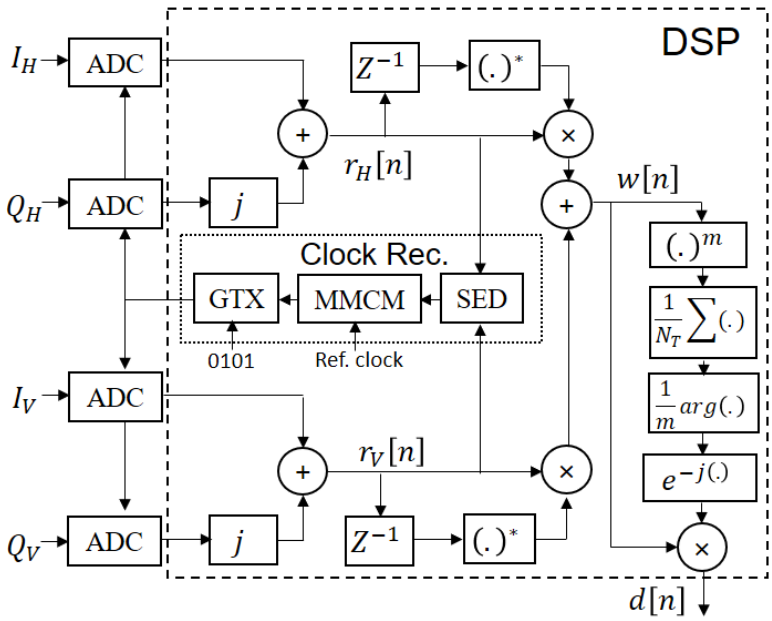

Figure 5.4: Symbol-rate DSP for POD coherent PSK Rx.

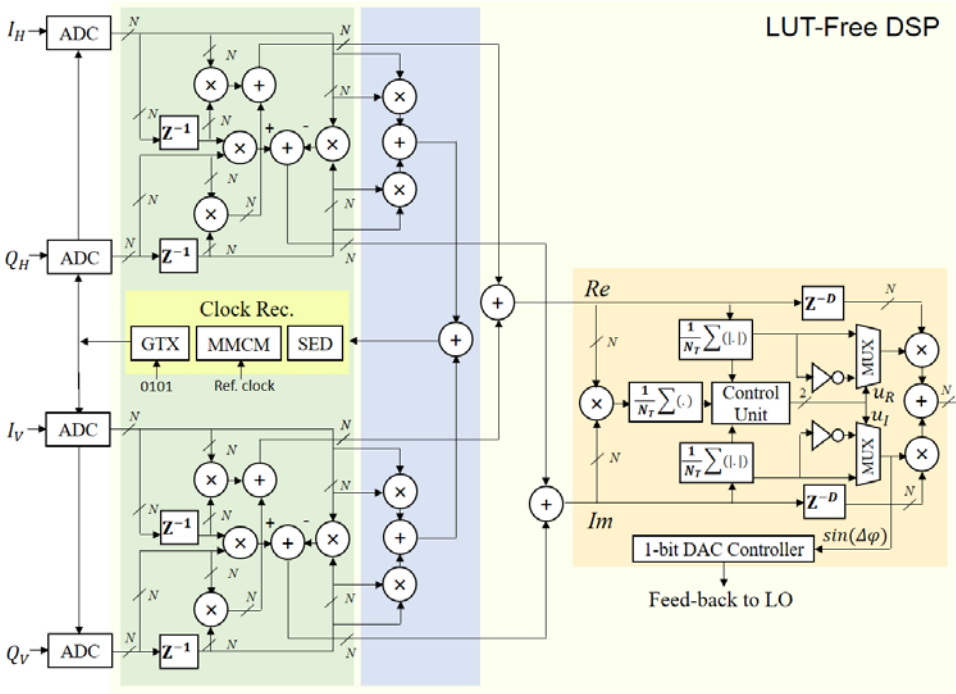

Figure 5.5: Symbol-rate LUT-Free DSP based on LUT-Free CR architecture, implemented on the FPGA for DPSK data.

5.2 Experimental Results

To evaluate the symbol-rate DSP of the POD coherent Rx, a real-time experiment is implemented with NRZ- PRBS data, from a PPG running at 1.25 Gbps, as shown in Figure 5.6.

The Tx uses a DFB laser ($\lambda = 1550$ nm) with direct-phase modulation and spectral linewidth $\Delta\nu = 4$ MHz, emitting at 0 dBm. The signal is sent through 25 km of SMF, and a VOA emulates the optical distribution network losses. The coherent Rx includes a free-running DFB LO to operate in intradyne regime emitting at 1 dBm with automatic wavelength control. The optical front-end is based on 3×3 coupler, and all the DSP subsystems are carried out by the same hardware as [4], [5], as well as in chapters 3 and 4, including an ML605 Xilinx Virtex-6 FPGA board, and a 4-channel ADC, each channel operating at 1.25 Gsps. Rather than ADC channels

interleaving to follow 2-sps data acquisition, this work instead uses all four ADCs independently to process the four POD signals at 1-sps. The ADCs reference clock is obtained from the GTX transceiver at 5 Gbps which generates a 2.5 GHz clock, and is adjusted in phase by the SED. The FPGA process clock is supplied from the Ref. clock and is set to 156.25 MHz for parallel processing of 8 symbols, which yields 1.25 Gbps DPSK data streaming.

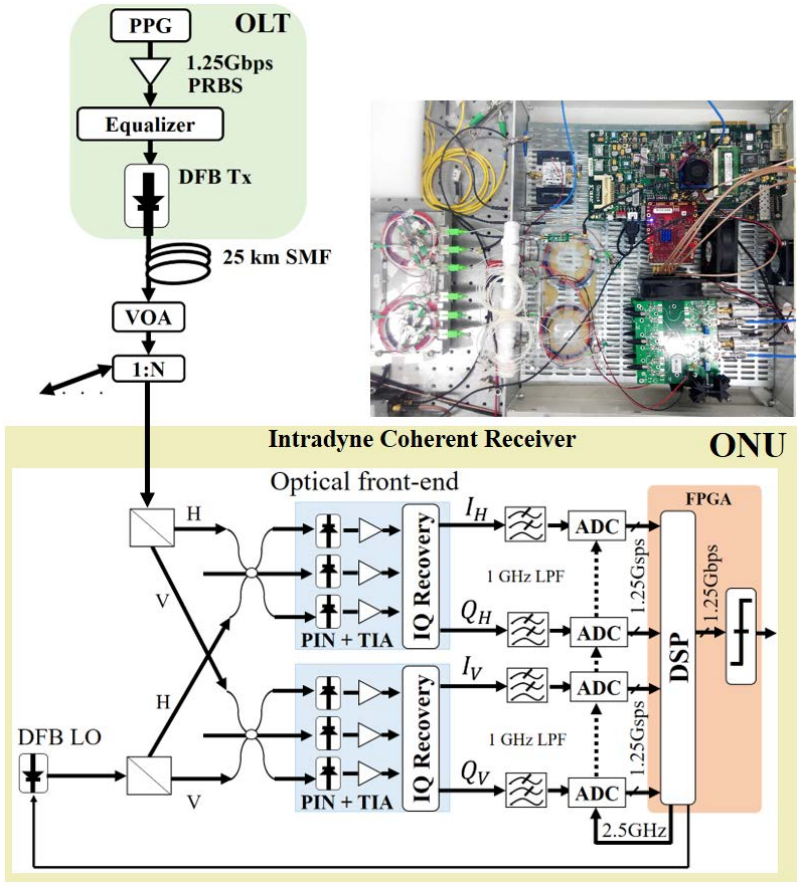

Figure 5.6: Experimental setup for real-time evaluation of the symbol-rate DSP of the POD coherent Rx with DPSK data at 1.25 Gbps.

The first test, evaluates 1-sps clock recovery performance used in the DSP of the POD coherent Rx, with respect to detuned PPG in data rate. Two DFB lasers with 4 MHz linewidth are used for the Tx and LO, thus, the total spectral linewidth $\Delta\nu = 8$

MHz. Figure 5.7 shows the performance of the clock recovery for $N = 2048$ within the $\pm$4 kbps range of PPG detuning for three different received optical powers of -34, -41 and -43 dBm. This test shows that the 1-sps clock recovery with optical power as high as -34 dBm, sustains up to $\pm$2.5 kbps PPG detuning in a constant BER regime, but the tolerance reduces to 60% and 40% of the detuning for the lower optical powers of -41 and -43 dBm, respectively, compared with the high power. Additionally, the 1-sps clock recovery detuning tolerance is not symmetric due to non-symmetric positive and negative slopes of the calculated signal power. It means that rising and falling edge data transitions (in PSK) are not symmetric, which is completely expected in real and practical scenarios.

In the second test, the sensitivity of the coherent Rx is assessed with the following measurements: single polarization (SP), horizontal (POD-H), vertical (POD-V), and random (POD-R) SOP of lightwave. The SP coherent Rx is evaluated for both $\Delta\nu =$ 4 MHz and 8 MHz. Based on Figure 5.7, the optimum BER is occurred when the PPG is detuned 1 kbps. Then, we set the PPG data rate at 1.250001 Gbps. The SP coherent Rx uses exactly the same optical front-end setup in Figure 3.12, but only one branch without polarization beam splitter (PBS) is connected to the DSP. Thus, only I_H and Q_H are processed by the DSP, and the best SOP is adjusted manually. For simplicity in implementation we apply an LUT-Free CR on the DSP.

Results in Figure 5.8 show that over 25 km length of fiber and $\Delta\nu = 8$ MHz with DPSK at 1.25 Gbps for a FEC threshold of BER = 10^{-3}, the sensitivity of -54 dBm and -46 dBm are achieved, by SP and POD coherent Rx, respectively. Results indicate that for the SP coherent Rx, there is not any penalty between the performance of the symbol-rate DSP which uses 1-sps clock recovery, and 2-sps DSP from the previous works [4], [5] that applied a conventional clock recovery. Furthermore, by using POD coherent Rx structure, less than 1 dB penalty for different SOP, and 8 dB sensitivity penalty in comparison to the SP scheme is attained. It should be considered that in the POD coherent Rx, the 8 dB penalty is because of extra excess losses of the PBSs and the optical couplers.

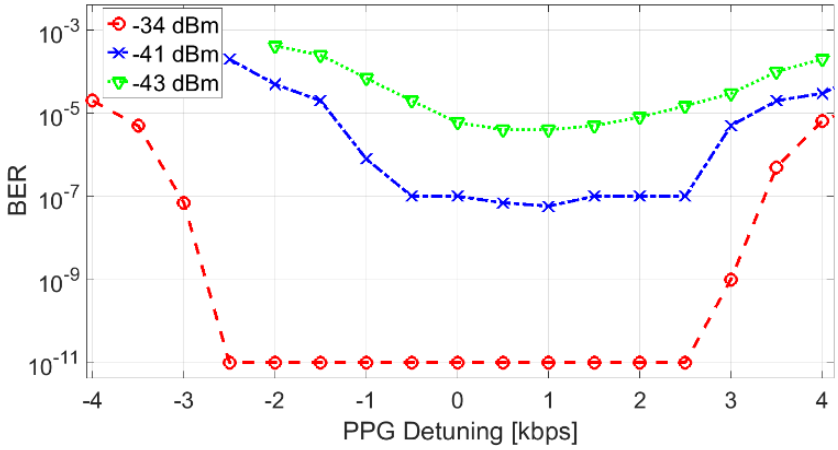

Figure 5.7: BER vs. PPG detuning to evaluate 1-sps clock recovery used in the symbol-rate DSP of the POD coherent Rx, for DPSK data at 1.25 Gbps with different optical powers.

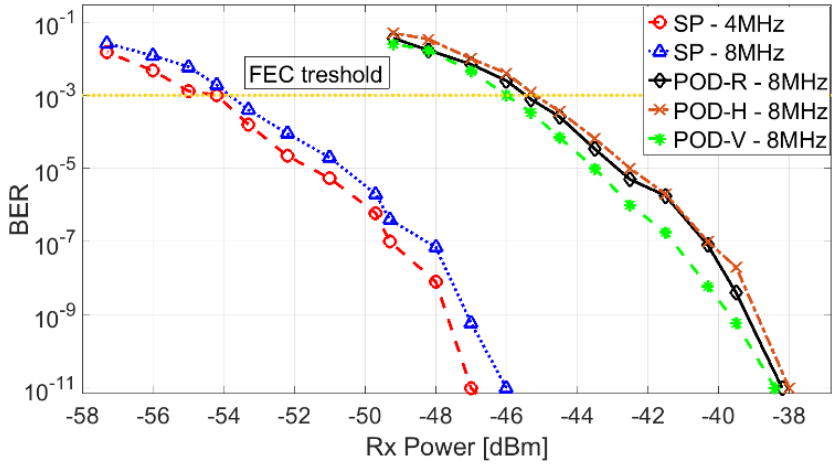

Figure 5.8: BER vs. optical power for SP coherent Rx, and different SOPs for POD coherent Rx by the symbol-rate DSP with $\Delta\nu = 4$ MHz and 8 MHz for DPSK data at 1.25 Gbps.

5.3 Conclusion

A symbol-rate DSP architecture for short-reach polarization diversity PSK intradyne Rx has been evaluated and successfully implemented on FPGA in a real-time optical transceiver. By a simple clock recovery, using only 1-sps for data processing, with commercial DFB lasers and direct-phase modulation, the sensitivity of -46 dBm, at a

ratio $\Delta\nu/R_b = 0.0064$ and BER = 10^{-3}, is achieved. The results validate that our presented architecture is feasible with low-cost lasers and low-speed ADCs for cost-effective transceivers in the udWDM-PON.

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Chapter 6. Conclusions

In this thesis, DSP architectures for coherent intradyne receivers in udWDM-PON was presented and experimentally tested. There were 2 types of DSP, one for single polarization (SP) mode, which SOP is manually adjusted, and the other independent of SOP which is a symbol-rate DSP. General and technical conclusions are described in the followings.

6.1 General Conclusion

In this thesis, we Implemented DSP for wavelength-to-the-user in optical access networks. Using improved methods and algorithms, and in real-time implementations, we obtained spectrum efficiency of the optical channels at 6.25 GHz spacing. Thus, at this point, we are able to increase the number of channels and users.

Moreover, due to the achieved high sensitivity in the receiver, we can reach in longer distance for data transmission, feasible for the rural and wide metro scenarios.

Furthermore, by reducing hardware complexity of the DSP subsystems and optimizing algorithms as well as improving the power consumption, real-time implementations using low-cost hardware and low-speed ADCs, became possible. These architectures were compatible with simple conventional DFB lasers and optical devices such as receiver front-end based on 3×3 couplers. Therefore, the cost-effective transceivers for udWDM-PON in optical access networks has been achieved.

6.2 Technical Conclusion

First, a DSP architecture with optimized CR architecture, which later was called DMP, using less hardware resources in comparison with the conventional ones, based on differential detection for optical PSK intradyne receivers and using LUTs to store trigonometrical arguments, was proposed and successfully tested in real-time. This DSP was implemented on the FPGA and evaluated in real-time with DPSK data at 1.25 Gbps. Results showed high sensitivity and tolerance to the phase noise, as well as robustness against the wavelength drifts of lasers, frequency error correction. Using this DSP, the sensitivity of -55 dBm in a 6.25 GHz spaced udWDM grid, with commercial DFB lasers, direct phase modulation, and low-cost optical front-end, was obtained which is the best results until now based on our knowledge.

Then, an LUT-free CR architecture which was an upgrade of DMP CR, for DPSK intradyne receivers was proposed and successfully tested in a real-time optical transceiver. The implementation on FPGA showed the reduction of ~41% DSP hardware resources, 61% fewer required process clocks, and 85% less power consumption, in 14% saving of total power of DSP Rx on Virtex-6 FPGA, in comparison with the previous CR (DMP) implementations as well as 34% rather than DSP Rx with the conventional CR. Moreover, in a 6.25 GHz spaced udWDM grid, with commercial DFB lasers, direct phase modulation, sensitivity of -54 dBm at a ratio $\Delta\nu/R_b = 0.0064$ and BER = 10^{-3}, feed-forward frequency error correction and high robustness against the fast frequency laser drifts was achieved.

Finally, a symbol-rate DSP architecture for polarization diversity PSK intradyne Rx was evaluated and successfully implemented on FPGA in a real-time optical transceiver. This DSP took advantage from a simple and novel clock recovery, using only 1-sps for data processing, with commercial DFB lasers and direct-phase modulation. It made the DSP independent from SOP, where by implementing on the FPGA, the sensitivity of -46 dBm, at a ratio $\Delta\nu/R_b = 0.0064$ and BER = 10^{-3}, was gained.

These results validate that our presented DSP architectures with the proposed CR

structures, alongside the 1-sps clock recovery, are feasible with low-cost lasers and low-speed ADCs for cost-effective transceivers in the udWDM-PON.

6.3 Future Works

Being involved with the research topic in this thesis and looking at the achieved results, there are still many solutions in the coherent receivers in udWDM-PONs that can be addressed to improve and enhance the optical access networks. Some research lines which are remained for the future investigations are as follows:

- To go beyond 10 Gbps in udWDM-PON grid. From the DSP point of view, it is mandatory to design and develop more DSP subsystems such as adaptive equalizers, to meet the requirements for this rate of communication. There are a lot of research works involved in equalization and chromatic dispersion [1], [2], [3], [4], [5]. In the future work, our own equalizers can be designed and developed, compatible with low-cost lasers, direct modulations, and easy to implement on FPGA.
- To make our SP DSP compatible with higher modulation formats such as QPSK, 8-PSK, and QAM. Since our DMP CR is compatible with M-PSK modulation formats, we just need to upgrade first, the Deskew block to synchronize the incoming signals in theses formats, then, the Data Decision subsystem should be upgraded to detect several levels as well as different constellations. Afterwards, a boosted LUT-free CR should work for M-PSK modulation formats, to reduce the hardware resources, required process clocks as well as power consumptions on the FPGA.
- To make our symbol-rate DSP compatible with higher modulation formats such as QAM [6], [7], [8] as well as beyond 10 Gbps rates. As was achieved in this thesis, our symbol-rate DSP is capable to detect and process M-PSK modulation formats. Our future work will be focused on design and development of DSP subsystems to support data detections for more than 10 Gbps, also compatible

with M-PSK and QAM, using 1-sps clock recovery and the LUT-free CR, to gain a polarization independent DSP with low-cost ADCs and FPGAs.

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Appendix A. Publication List

A.1 Journal Publications

1. **S. Ghasemi**, J. Tabares, V. Polo and J. Prat, "LUT-Free Carrier Recovery for Intradyne Optical DPSK Receivers in udWDM-PON," *Journal of Lightwave Technology*, vol. 37, no. 6, pp. 1608 - 1613, 2019.
2. J. Tabares, **S. Ghasemi**, V. Polo and J. Prat, "Simplified Carrier Recovery for Intradyne Optical PSK Receivers in udWDM-PON," *Journal of Lightwave Technology*, vol. 36, no. 14, pp. 2941 - 2947, 2018.
3. M. Presi, M. Artiglia, F. Bottoni, M. Rannello, I. N. Cano, J. Tabares, J.-C. Velásquez, **S. Ghasemi**, V. Polo, G. Y. Chu, J. Prat, G. Azcarate, R. Pous, C. Vilá, H. Debregeas and Gemma, "Field-Trial of a High-Budget, Filterless, λ -to-the-User, UDWDM-PON Enabled by an Innovative Class of Low-Cost Coherent Transceivers," *Journal of Lightwave Technology*, vol. 35, no. 23, pp. 5250 - 5259, 2017.

A.2 Conference Publications

1. **S. Ghasemi**, J. Tabares and J. Prat, "Symbol-rate Digital Signal processing for Low-Complexity Polarization Diversity Intradyne optical PSK Receivers," in *European Conference on Optical Communication (ECOC)*, Dublin, Ireland, Sep. 2019.

2. **S. Ghasemi**, J. Tabares, V. Polo and J. Prat, "LUT-Free Carrier Recovery for Intradyne Optical DPSK Receivers in udWDM-PON," in *European Conference on Optical Communication (ECOC)*, Rome, Italy, 2018.

3. **S. Ghasemi**, J. Tabares, V. Polo and J. Prat, "Optimized Differential Detection-Based Optical Carrier Recovery for Intradyne PSK Receivers in udWDM-PON," in *Optical Fiber Communications Conference and Exposition (OFC)*, San Diego, CA, USA, 2018.

4. M. Rannello, I. N. Cano, J. Tabares, J. C. Velasquez, **S. Ghasemi**, V. Polo, G. Y. Chu, J. Prat, R. Pous, G. Azcarate, C. Vila, H. Debregeas, G. Vall-llosera, A. Rafel, M. Artiglia, F. Bottoni, M. Presi, and E. Ciaramella, "Field-Trial of a λ-to-the-user high-budget PON using a novel class of low-cost coherent transceivers and compatible with EPON system operation", Spain, ICTON 2017.

5. I. N. Cano, J. Prat, J. Tabares, J. C. Velásquez, **S. Ghasemi**, V. Polo, G. Y. Chu, M. Presi, E. Ciaramella, M. Rannello, F. Bottoni, M. Artiglia,G. Cossu, R. Pous, G. Azcárate, C. Vilà, H. Debrégeas, G. Vall-llosera, A. Rafel, "Field-Trial of Low-Cost Coherent UDWDM-PON with Real-Time Processing, λ-Monitoring and EPON Coexistence", Germany, ECOC 2016.

6. J. Prat, I. N. Cano, M. Presi, J. Tabares, M. Ranello, J. C. Velásquez, F. Bottoni, **S. Ghasemi**, V. Polo, G. Y. Chu, M. Artiglia, R. Pous, G. Azcárate, C. Vilà, H. Debrégeas, E. Ciaramella, "Ultra-dense WDM Access Network Field Trial", Portugal, NOC 2016.

A.3 Submitted Publications

1. J. Tabares, **S. Ghasemi**, J. C. Velásquez, and J. Prat, "Coherent Ultra-Dense WDM-PON Enabled by Cost-Effective Digital Transceivers," submitted to *Journal of Lightwave Technology*, 2019.