UNIVERSITAT ROVIRA I VIRGILI COMPACT MODELING OF MULIPLE GATE MOS DEVICES. Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007



COMPACT MODELING OF MULTIPLE GATE MOS DEVICES

A Thesis Presented to

The University of Rovira i Virgili

Department of Electronic, Electrical and Automatic Engineering

Ву

HAMDY MOHAMED ABD ELHAMID

In Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy in Electrical and Electronics Engineering

Advisor

Professor Benjamin Iniguez



University of Rovira i Virgili

Tarragona-Spain 2007

Contents

List of symbols	1
List of figures	3
List of publications	6
Acknowledgement	9
CHAPTER ONE: Multiple Gate MOS Devices Structures and Performances	
1-A Introduction	
1-B FABRICATING CHALLENGES	
1-C Modeling Challenges	21
CHAPTER TWO : Short Channel Effects (SCEs) in Undoped Multiple Gate MOS Devices	
(2-A) PART (I): SHORT CHANNEL EFFECTS (SCES) IN UNDOPED CYLINDRICAL GATE ALL	
Around MOSFET	
2A-1 Introduction	
2A-2 Potential Model Derivation	
2A-3 Threshold voltage derivation	
2A-4 Threshold Voltage and its sensitivity	40
2A-5 Subthreshold swing model	42
(2-A) PART (II): SHORT CHANNEL EFFECTS (SCES) IN UNDOPED CYLINDRICAL GATE ALL	
AROUND MOSFET INCLUDING DIBL EFFECTS	44
2A-6 Potential Model Derivation	44
2A-7 Virtual Cathode: Value and position	49
2A-8 Inversion charge and Threshold voltage	51
2A-9 Subthreshold Swing model	
(2-B) SHORT CHANNEL EFFECTS (SCES) IN UNDOPED DOUBLE GATE MOSFET	58
2B-1 Introduction	58
2B-2 Potential Model Derivation	60
2B-3 Virtual Cathode: Value and position	68
2B-4 Inversion charge and Threshold voltage	69
2B-5 Subthreshold Swing model	73
(2-C) A 3-D ANALYTICAL PHYSICALLY-BASED MODELS FOR SHORT CHANNEL EFFECTS IN	
UNDOPED FINFETS	76
2C-1 Introduction	76
2C-2 Potential Model Derivation	78
2C-3 Subthreshold Swing Model	
2C-4 Threshold Voltage Model	
(2D) SCALABILITY LIMITS OF SURROUNDING GATE MOSFETS AND DOUBLE GATE MOSFET	\[S
CHAPTER THREE: Current Transport in Undoped Multiple Gate MOS Devices	
(3A) EXPLICIT CONTINUOUS MODEL FOR LONG CHANNEL UNDOPED MULTIPLE GATE MOSI	FETS
(ST) EXELECT CONTINUOUS MODEL FOR EGING CHARNEL CINDOLED MODIL EL GATE MODE	
3A-1 Introduction	
3A-2 GAA Model and results.	
31.2 Girl Model and results	

UNIVERSITAT ROVIRA I VIRGILI COMPACT MODELING OF MULIPLE GATE MOS DEVICES. Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

	3
SCEs in undoped multiple gate MOS	
3A-4 DG MOSFET Model	131
(3B) BALLISTIC AND QUASI BALLISTIC TRANSPORT IN	135
UNDOPED MULTIPLE GATE MOS DEVICES	135
3B-1 Introduction	135
3B-2 Ballistic and Quasi Ballistic Transport In DG and GAA MOSFETs	138
3B-3 Quasi Ballistic Transport in undoped FinFET devices	151
CHAPTER FOUR : Conclusions and recommendations for the future work	
4-1 Summary	157
4-2 RECOMMENDATIONS FOR THE FUTURE WORK	159
APPENDIX (2A-1)	161
APPENDIX (2A-2)	165
APPENDIX (2-B)	170
APPENDIX (2-C)	180

REFERENCES211

LIST OF SYMBOLS

k – Boltzmann constant

n – free electron concentration

 n_i – intrinsic electron density, 1.45*10¹⁰ cm⁻³ at 300 K

q – electron charge

 t_{ox} – gate oxide thickness

 t_{Si} – silicon film thickness

 E_g – silicon band gap, 1.12 eV at 300 K

 I_D – drain current

L – channel length

 N_A – channel doping concentration (of acceptors)

 $N_{D/S}$ – source/drain doping concentration (n+ type)

 Q_{TH} – a real density of free carriers under threshold conditions

S – subthreshold swing

T – absolute temperature

 $V_{bi,i}$ – junction built-in voltage between the source/drain and intrinsic silicon

 V_{DS} – drain-to-source voltage

 V_{GS} – gate-to-source voltage

 V_{TH} – threshold voltage

 $V_{TH,long}$ – long channel threshold voltage

 ΔV_{TH} – threshold voltage roll-off

 β – reciprocal of thermal voltage, q/(kT), 38.68 V^{-1} at 300 K

 ε_0 – dielectric constant of vacuum, $8.854*10^{-12} F*m^{-1}$

 ε_{Si} – relative dielectric constant of silicon, 11.9

 ε_{ox} – relative dielectric constant of silicon oxide, 3.9

 ϕ_B – difference between Fermi level and intrinsic level in silicon

 ϕ_F – difference between Fermi level and electron quasi-Fermi level

 λ_{Di} – intrinsic Debye length, 48.49 μm at 300 K.

 λ_j – eigenvalues, j=1, 2, 3, ...

UNIVERSITAT ROVIRA I VIRGILI COMPACT MODELING OF MULIPLE GATE MOS DEVICES. Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

5

SCEs in undoped multiple gate MOS

- λ_I lowest-order eigenvalue, length scale
- χ electron affinity in silicon, 4.05 eV
- φ electrostatic potential referenced to Fermi level
- $\phi_{\it ms}$ work function difference between gate material and silicon channel
- r back scattering coeffeicent
- η fermi energy level
- g_d- transconductance
- g_d -channel conductance
- v thermal velocity

6

SCEs in undoped multiple gate MOS

LIST OF FIGURES

Fig. 1The existing gate configuration for thin-film SOI MOSFETs
Fig. 2 Schematic and TEM cross section of a FinFET
Fig. 3 Cross-sectional views of the optimized cubical-channel MOSFETs
Fig.4 TEM view of a single and four channel wrap-around-gate MOSFET
Fig. 5. Bottom of subbands and transconductance characteristics of GAA MOSFET23
Fig. 6. Analytical solutions of the subthreshold for symmetric and asymmetric DG MOSFETs24
Fig. 7. Comparison of subthreshold swing from numerical and analytical25
Fig. 2A-1GAA MOSFET: Structure, and cross section
Fig.2A-2 GAA MOSFET: Potential along the channel at low drain-source voltage34
Fig.2A-3 GAA MOSFET: Threshold voltage vs silicon thickness at low Vds
Fig. 2A-4 GAA MOSFET: Threshold voltage vs the channel length at low drain-source voltage38
Fig. 2A-5 GAA MOSFET: Subthreshold swing at low drain-source voltage
Fig. 2A-6 GAA MOSFET: Surface potential distribution along the channel at high Vds45
Fig.2A-7 GAA MOSFET: Virtual cathode position vs. Drain-Source Voltage
Fig. 2A-8 GAA MOSFET: Threshold voltage vs. channel radius, for different Vds48
Fig. 2A-9 GAA MOSFET: Threshold voltage
Fig. 2A-10 GAA MOSFET: Threshold Voltage Roll-off vs. channel length
Fig. 2A-11 GAA MOSFET: Drain Induced Barrier Lowering coefficient vs. channel length50
Fig. 2A-12 GAA MOSFET: Subthreshold swing at low drain-source voltage
Fig. 2A-13 GAA MOSFET: Subthreshold swing for Gate All Around MOSFET at high $V_{\text{ds}}52$
Eig 2D 1 DC MOSEET, Davies structure and areas section
Fig. 2B-1 DG-MOSFET: Device structure, and cross section
Fig. 2B-2 DG MOSFET: Quasi Fermi Potential for DG MOSFET
Fig. 2B-3 DG MOSFET: Center potential distribution along the channel
Fig. 2B-4 DG MOSFET: Minimum potential
Fig. 2B-5 DG MOSFET: Threshold Voltage Roll-off vs. channel length
Fig. 2B-6 DG MOSFET: Drain Induced Barrier Lowering coefficient
Fig. 2B-7 DG MOSFET: Virtual cathode position vs. channel length

UNIVERSITAT ROVIRA I VIRGILI COMPACT MODELING OF MULIPLE GATE MOS DEVICES. Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS	
Fig.2B-8 DG MOSFET: Subthreshold swing	69
Fig. 2C-1 FinFET: Cross section for this work.	72
Fig. 2C-2 FinFET: 3-D potential distribution along channel length.	77
Fig. 2C-3 FinFET: SEM, and TEM image	80
Fig. 2C-4 FinFET: Subthreshold swing at low drain-source voltage	81
Fig. 2C-5 FinFET: Subthreshold swing at high drain-source voltage	82
Fig. 2C-6 FinFET: Measured drain current.	84
Fig. 2C-7 FinFET: Subthreshold swing versus Fin height.	85
Fig. 2C-8 FinFET: Measured drain current in Logarithmic-scale	85
Fig. 2C-9 FinFET: Threshold Voltage coefficients calculations for long channel devices	88
Fig. 2C- 10 FinFET: Extracted threshold charge value	89
Fig. 2C- 11 FinFET: Long channel threshold voltage	89
Fig. 2C-12 FinFET: Threshold voltage for short channel devices	90
Fig. 2C- 13 FinFET: Threshold voltage roll-off	91
Fig. 2C-14 FinFET: DIBL vs. channel length for different	92
Fig. 2D- 1 Channel length vs. oxide thickness for a) GAA MOSFET, and b) DG MOSFET.	95
Fig. 2D- 2 DIBL and channel length vs. channel radius/thickness	96
Fig. 3A-1 GAA MOSFET: Cross section	101
Fig. 3A-2 GAA MOSFET: Channel charge density per unit area	106
Fig. 3A-3 GAA MOSFET: Transfer characteristic.	107
Fig. 3A-4 GAA MOSFET: Output characteristics.	108
Fig. 3A-4 FinFET: 3D potential components vs. channel length	115
Fig. 3A-5 Comparison between the Square GAA MOSFET, and cylindrical GAA MOSFET	116
Fig. 3A-6 FinFET: Transfer characteristic in linear and logarithmic scale	117
Fig. 3A-7 FinFET: Output characteristics.	118
Fig. 3A-8 DG MOSFET: Sheet density of mobile charge.	119
Fig. 3A-10 DG MOSFET: Potential at the channel surface and channel center	119
Fig. 3A-11 DG MOSFET: Carrier charge per unit area induced in the channel	120

UNIVERSITAT ROVIRA I VIRGILI COMPACT MODELING OF MULIPLE GATE MOS DEVICES. Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

5 / 2.21 1. 2011 2007	8
SCEs in undoped multiple gate MOS	
Fig. 3A-12 DG MOSFET: Output characteristics.	120
Fig. 3B-1 Cross section of the symmetrical DG-MOSFET considered in this section	125
Fig. 3B-2 a) Transfer characteristic of a quantum well DG-MOSFET	127
$Fig.~3B-3~Simple~one~flux~representation~of~channel~transport~in~nanoscale~MOSFETs.~\dots \\$	131
Fig. 3B-4 DG MOSFET: Quasi ballistic current	133
Fig. 3B-5 DG MOSFET: Carrier velocity.	134
$Fig.\ 3B-6\ DG\ MOSFET: Channel\ conductance\ for\ scattering\ model,\ and\ ballistic\ model\ .$	135
Fig. 3B-7. DG MOSFET: Ballistic current	136
Fig. 3B-8 FinFET: Measured drain current at different temperature values	139
Fig. 3B-9 FinFET: measured transconducatnce curve at different temperature values	140
Fig. 3B-10 FinFET: Extracted threshold voltage vs the temperature	140
Fig. 3B-11FinFET: Extracted backscattering coefficient vs. channel lengths	141

LIST OF PUBLICATIONS

International Journals

- 1- **Hamdy Abd-Elhamid**, Jaume Roig, Valeria Kilchytska, Denis Flandre, Benjamin Iñiguez " A 3-D Analytical Physically-Based Model for SCEs in Undoped FinFETs," IEEE TRANSACTIONS ON ELECTRON DEVICES, submitted
- 2- Hamdy Abd-Elhamid, Jaume Roig, , Valeria Kilchytska, Denis Flandre, Benjamin Iñiguez " A 3-D Analytical Physically-Based Model for the Subthreshold Swing in Undoped FinFETs", IEEE TRANSACTIONS ON ELECTRON DEVICES, submitted
- 3- Hamdy Abd-Elhamid, Benjamin Iñiguez, and Jaume Roig "Two-Dimensional Analytical Threshold Voltage and Subthreshold Swing Models of Undoped Symmetric Double Gate MOSFETs", IEEE TRANSACTIONS ON ELECTRON DEVICES, inpress,m April 2007
- 4- **Hamdy Abd-Elhamid**, Benjamin Iñiguez, and Jaume RoigAnalytical predictive modeling for the study of the scalability limits of multiple gate MOSFETs", Solid-State Electronics, Vol. 51, Issue 3, March 2007, Pages 414-422.
- 5- Hamdy Abd-Elhamid, Benjamin Iñiguez, and Jaume Roig, "Analytical Model of the Threshold Voltage and Subthreshold Swing of Undoped Cylindrical Gate All Around Based MOSFETs", IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 54, No.3, March 2007
- 6- Hamdy Abd-Elhamid, Benjamin Iñiguez, David Jiménez, Jaume Roig, Josep Pallarès, and Lluís F. Marsal, "Two-Dimensional Analytical Threshold Voltage Roll-Off and Subthreshold Swing Models For Undoped Cylindrical

Gate All Around MOSFET," Solid-State Electronics, vol. 50, no. 5, pp. 805-812, May 2006..

- 7- Benjamin Iñíguez, David Jiménez, Jaume Roig, <u>Hamdy Abd Elhamid</u>, Lluís F. Marsal, and Josep Pallarès "EXPLICIT CONTINUOUS MODEL FOR LONG CHANNEL UNDOPED SURROUNDING GATE MOSFETS", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 52, NO. 8, AUGUST 2005
- 8- <u>Hamdy Abd-Elhamid</u>, Benjamin Iñiguez, David Jiménez, Josep Pallarès, and Lluís F. Marsal "A simple model of the nanoscale double gate MOSFET based on the flux method" physica status solidi (c) Volume 2, Issue 8, Date: May 2005, Pages: 3086-3089

•International Conferences

- 9-(Invited) <u>Hamdy Abd-Elhamid</u>, Benjamin Iñiguez, and Jaume Roig "3-D Analytical Models for the Short-Channel Effect Parameters in Undoped FinFET Devices", Workshop on compact modelling, WCM, May 20-24, 2007 <u>Santa Clara Convention Center</u>, California, U.S.A.
- 10- <u>Hamdy Abd-Elhamid</u>, Benjamin Iñiguez, and Jaume Roig "A 2-D Short Channel Effects Model For Undoped Double Gate MOSFET, Euro-SOI, Leuven, Belgium. 17-19 January, 2007
- 11- <u>Hamdy Abd-Elhamid</u>, Benjamin Iñiguez, and Jaume Roig" NATO International Advanced Research Workshop "Nanoscaled Semiconductor-on-Insulator Structures and Devices" 15-19 October 2006, Sudak, Crimea, Ukraine
- 12- <u>Hamdy Abd-Elhamid</u>, Benjamin Iñiguez, and Jaume Roig, MOS Modeling and Parameter Extraction Working Group MOS-AK/ESSDERC/ESSCIRC

Workshop Compact Modeling for Emerging Technologies, September 2006 Montreux Convention and Exhibition Center "scalability limits of multiple gate MOS devices"

- 13- **Hamdy Abd-Elhamid**, Benjamin Iñiguez, David Jiménez, Jaume Roig, Josep Pallarès, and Lluís F. Marsal "*Threshold voltage, and subthreshold swing for GAA MOSFET*", Euro-SOI, Grenoble, France. 19-21 March, 2006
- 14- Benjamin Iñiguez, <u>Hamdy Abd-Elhamid</u>, "Noise in SOI MOSFETs and Gate-All- Around Transistors" 18th International Conference on Noise and Fluctuations-ICNF 2005, Salamanca, Spain, 19-23 Sept. 2005.
- 15- <u>Hamdy Abd-Elhamid</u>, Benjamin Iñiguez, David Jiménez, Josep Pallarès, and Lluís F. "Compact Modelling for Surrounding Gate MOSFETs" International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES 2005), Krakow (Poland), June 2005.
- 16- (Invited) Benjamin Iñiguez, <u>Hamdy Abd-Elhamid</u>, David Jiménez, "Compact Model of Multiple-gate SOI MOSFETs" ES 2005 NSTI Nanotechnology Conference and Trade Show Nanotech, Workshop on compact modelling, WCM, 2005 May 8-12, 2005 Anaheim Marriott & Convention Center Anaheim, California, U.S.A.
- 17- **Hamdy Abd-Elhamid**, Benjamin Iñiguez, David Jiménez, Josep Pallarès, and Lluís F. "*Quasi Ballistic Model of double gate MOSFET*", First Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits Granada, SPAIN. 19-21 January, 2005
- 18- <u>Hamdy Abd-Elhamid</u>, Benjamin Iñiguez, David Jiménez, Josep Pallarès, and Lluís F. "*Double Gate MOSFET Compact Model Including Scattering*" Conference on Electron Devices (CDE), Tarragona, Spain, 02-05 Feb., 2005

12

SCEs in undoped multiple gate MOS

ACKNOWLEDGMENTS

The completion of this thesis would not have been possible without the assistance and support of many people. First and foremost, I would like to express my sincerest gratitude to my advisor and mentor, Professor Benjamin Iniguez for his guidance and support throughout my years at URV, DEEEA. In ways more than one, he has made me realize my fullest potential, and encouraged me to attain the highest level of professionalism. I would especially like to thank him for giving me the freedom to pursue my research interests. He always provided timely and warm encouragement and support in difficult times. He gave me every

Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

opportunity to advertise my work at important conferences. I especially thank him for his prompt reading and careful critique of my thesis.

I would especially like to thank Dr. Jaume of for developing me by the whole simulation results through the thesis.

My most rewarding experience was the summer I spent at Microelectronics Lab., UCL, Belgium. I would especially like to thank Prof. Denis Flandre, and Dr. Valeria for giving me the opportunity to characterizing and implementing the FinFET model.

I would like to thank Professor Hall Steve in particular, for allowing me to participate in his research group at University of Liverpool, England for two months.

I would like to thank Professor Tor Feljidy for the many discussions we had about my research, for the numerous suggestions and feedback, for his detailed comments on this thesis.

I would like to thank Professor Jamal el din of McMaster University for his fruitful and insightful discussions on SCEs model of GAA MOSFETs.

I would also like to thank Dr. David of UBC for many great discussions, especially for the ballistic models of quantum wire and quantum well.

Special thanks go to Professor Joseph, and Luis Marsal for their advice and encouragement on matters relating to academic and non-academic issues.

My sincere thanks and acknowledgements are due to my wife, my son, "Ahmed", my daughter, "Hana", my parents and my brothers: Dr. Hamada, and Eng. Arfat. I would like to give thanks to my friends Michael, Elizabith, and Lucas for their moral support. The support of the staff from the Department of Electrical and Electronics Engineering, URV is also greatly appreciated

CHAPTER ONE

Multiple Gate MOS Devices Structures and Performances

1-A Introduction

Thin film MOSFETs are very attractive for sub-100 nm CMOS applications because of their steep subthreshold slope and a low body effect coefficient. SOI

ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

15

microprocessors with a 22% speed improvement over bulk have been reported recently [1]. Fully depleted MOSFETs with a gate length of 50 nm and a switching speed less than a picosecond [2] have been reported. To minimize short channel effects and to maintain full depletion if the doping concentration in the channel region is increased, the silicon film thickness must be scaled down with gate length. While devices made in films thicker than 20 nm have excellent mobility and current drive characteristics [2], significant mobility degradation is observed in devices made using a silicon film thickness less than 10 nm [3]. If a metal gate is used instead of N polysilicon the doping concentration in the film can be reduced, which allows for fully depleted operation in thicker silicon films. This decrease of doping concentration, however, degrades the short channel characteristics and subthreshold slope through an increase of penetration of the drain electric field lines in the channel region [4], [5]. To prevent the electric field lines originating at the drain from terminating under the channel region, special multiple-gate structure devices have been reported. Such multiple-gate devices include double-gate and triple-gate structures such as the quantum wire [6], the FinFET [7] and II-channel SOI MOSFET [8], and quadruple-gate devices such as the gate all-around (GAA) device [9], the DELTA transistor [10], Omega MOSFETs [11], and Pi-gate SOI MOSFETs [12]. It is well known that the double-gate (top and bottom gate) silicon-on-insulator (SOI) MOSFET and the gate-all-around device are the most suitable device structures for suppressing short-channel effects such as DIBL and subthreshold slope degradation [9], [12-15]. Unfortunately the process proposed to fabricate such devices is incompatible with standard CMOS or even SOI CMOS manufacturing. The Pi-gate SOI

MOSFET structure was first introduced in [12].

Different multiple gate structures have been proposed: double-gate MOSFET, FinFET, surrounding-gate MOSFET. Fig. 1.1 shows the existing gate configuration for thin-film SOI MOSFETs: 1) single gate; 2) double gate; 3) triple gate; 4) quadruple gate (or GAA). The new proposed gate structure is a triple-gate MOSFET where the gate electrode extends to some depth in the buried oxide on both sides of the device. The gate is in the shape of the uppercase Greek (Pi) letter. The gate extension in the buried oxide shields the back of the channel region from the electric field lines from the drain almost as perfectly as an actual back gate would.

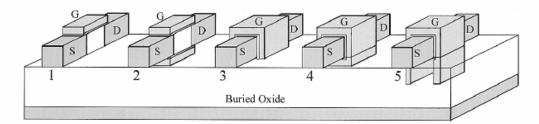


Fig. 1.1 the existing gate configuration for thin-film SOI MOSFETs.

Their main advantage is an excellent electrostatic control of the channel, which reduces the short channel effects. On the other hand, since the conduction takes place in a volume instead of just one surface, these devices present higher mobility than conventional bulk MOSFETs because there is less scattering; their operation can even be near the ballistic limit for very short channel devices.

In multiple gate devices, the use of a very thin film allows to downscale the devices without the need of using high channel doping densities and gradients. In fact, undoped films can be used: the full depletion of the thin film prevents punch-through from happening. Besides, the absence of dopant atoms in the channel increases the mobility by suppressing impurity scattering. On the other hand,

unwanted dispersion of the characteristics is avoided; this dispersion results from the random microscopic fluctuations in ultra-small devices.

Multiple gate nanoscale devices have many advantages in circuit performance. A very high packaging density is possible because of the small size of these devices, caused by the short channel and the thin film. Because of the higher mobility, transconductance can be higher, which gives more current gain and allows a higher operating frequency. Therefore, multiple gate nanoscale devices have a big potential for RF and microwave applications. The analog performance is also very good. Voltage gain is much higher than in conventional bulk MOSFETs, and especially in moderate inversion: the reduction of short channel effects leads to a higher Early voltage (I-V_{ds} characteristics are flatter in saturation), and on the other hand the g_m/I_d characteristics have higher values than in conventional MOSFETs. Regarding digital applications, the small subthreshold swing of multiple gate devices keeps a high ratio between on current and off current even for devices with channel lengths of the order of nm.

1-B Fabricating challenges

Anyway, multiple gate structures present some difficulties in fabrication. In double-gate MOSFETs, the alignment of the top and the bottom gates to each other and to source/drain doping is critical for the device performance; misalignment can cause an additional overlap capacitance between gate and source or drain, as well as an additional series resistance.

Because of its intrinsic self-aligned process, FinFET devices seem to be the first multiple-gate devices that will appear in the market. Devices with channel lengths

of 18 nm have been successfully fabricated. FinFETs work as double-gate devices when the width of the silicon fin is much smaller that its height.

In triple-gate structures an inversion channel forms not only at the planar sides of the device, but also in the corners where two such sides meet. It has been shown that premature inversion can be reached at the corners, which degrades the subthreshold characteristics and creates an undesirable kink in the transconductance versus gate

voltage curve [16]. The FinFET is a double-gate device, since the top of the silicon fin is covered by a hard mask. However, due to processing conditions a slight lateral over-etch of the hard mask can occur. As a result, the top corners of the fins can be exposed to gate oxidation and become the weak point in the gate oxide as well as the host of corner inversion. Similarly, a slight over-etch of the buried oxide below the fin will expose the

bottom corners, in which channels can form as well. Premature corner inversion is an undesirable effect. It can be avoided by reducing channel doping or by rounding the corners of the fins [16]. In [17], hydrogen anneal prior to gate oxidation was proposed to round the corners and thereby reduce leakage currents, as shown in Fig. 1.2. Table 1.1 indicate the improvements taken place in DIBL, threshold voltage, and subthreshold slope due to smoothening the corners.

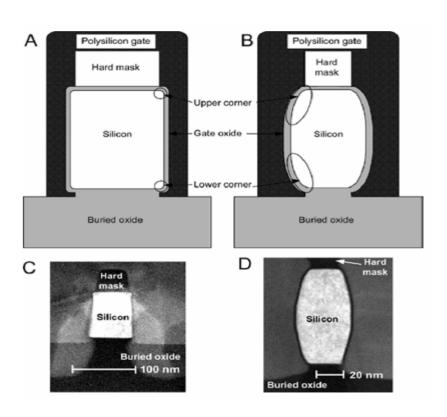


Fig. 1.2 Schematic and TEM cross section of a FinFET without (A, C) and with (B, D) hydrogen annealing [17].

	V _{TH} (mV)	V _{TH} (mV)	DIBL	S	S
	V _D =0.05V	V _D =1.2V	(mV)	(mV/dec) V _D =0.05V	(mV/dec) V _D =1.2V
Device A	185	50	135	87	117
Device B	250	115	135	81	91
Device C	0.05	015	65	66	70

Table 1.1 Threshold voltage, DIBL and subthreshold slope in the n-FinFETs, [17]

Through the previous simulation results for the GAA MOSFETs, the design optimization for proper suppression of short-channel effects yields the following device parameters[18-19]:

the gate length, the fin width, and the fin height were all 30 nm, and the gate-oxide thickness was 2 nm. As a result, the performance of GAA MOSFETs had been improved with a cubical channel.

To study short-channel behavior of corner-effect-free GAA MOSFETs, the simulation for ideal cylindrical-channel MOSFETs was performed as shown in Fig. 1.3. In the case of ideal cylindrical-channel MOSFETs, the main device parameter is the cylinder diameter. The cylinder diameter was set to be 30 nm, which was the same as the fin width in the cubical-channel MOSFETs. Fig. 1.3b shows the transfer characteristics of the cubical-channel MOSFETs and the ideal cylindrical-channel MOSFETs. The results of the simulation were summarized in Table 1.2. In cylindrical-channel MOSFETs, the OFF current was remarkably reduced because the channels were equally affected by the gate electric field while the electric field was out of balance inside the channel in the cubical-channel MOSFETs. SS as well as DIBL in the ideal cylindrical-channel MOSFETs were smaller than those in cubical-channel MOSFETs with corner effects.

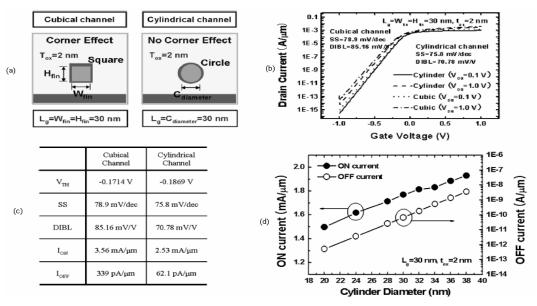


Fig. 1.3. a) Cross-sectional views of the optimized cubical-channel MOSFETs and ideal cylindrical-channel MOSFETs without corner effects. In the case of ideal cylindrical-channel MOSFETs, the main device parameter is the cylinder diameter. The cylinder diameter was set to be 30 nm, which is the same as the fin width in the optimized cubical-channel MOSFETs. b) Transfer characteristics of cubical-channel GAA MOSFETs and ideal cylindrical-channel MOSFETs. c) The SS as well as DIBL in the ideal cylindricalchannel MOSFETs are smaller than that in cubical-channel MOSFETs. d) In cylindrical-channel MOSFETs, the OFF current is remarkably reduced[18].

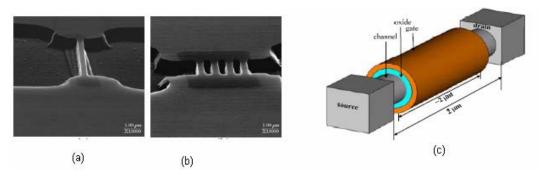


Fig.1.4 TEM view of (a) a single and (b) four channel wrap-around-gate MOSFET, (c) A cross-sectional view of the n-channel nanowire MOSFET [19]

Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

The cylindrical surrounding gate MOSFET, in Fig. 1.4, allows a more drastic

reduction of the short-channel effects. In this device, a gate electrode surrounds

the pillar silicon island, which can be formed by conventional trench process

techniques.

For designers, one of the main challenges is to have appropriate threshold voltage

values for integrated circuits; if the device films are not doped, threshold voltage

control will rely on successfully using metal gates and engineering the work-

function.

Another challenge for device engineers is to reduce parasitics, such as the series

resistance and the fringing capacitance. It has been proposed to reduce the series

resistance by using metal sources/drains, since the resistivity of metal is two

orders of magnitude smaller than that of heavily doped silicon.

1-C Modeling challenges

The multi-gate devices that control the channel from multiple sides and very thin

body devices are new to circuit and system designers. These devices need to be

modeled to understand and predict the functionality of the circuits. Compact

device models are used in circuit design. New compact models that accurately

model these novel devices, and are computationally efficient, are in development.

There are new physical effects that now need to be incorporated into these device

models.

The use of multiple gate devices in circuit design is critically dependent on the

availability of accurate models for these devices, valid for DC, AC, transient and

noise analysis. Using appropriate models, circuit simulation allows to design

circuits with devices of adequate dimensions. Circuit simulation requires accurate models of the current and the terminal charges (from which capacitances are obtained) of the devices. These models should be based on expressions with a sufficiently high order of continuity.

Lack of continuity between the different operating regimes leads to convergence problems in circuit simulation. In conventional MOSFETs, there have been a trend to move from piecewise models (with continuity problems) to unified models with an infinite order of continuity. Smoothening functions are often used to assure the continuity between different operating regimes. For the same reasons, multiple-gate MOSFETs will need unified highly continuous models.

For proper modeling of nanoscale MOSFET for VLSI circuit simulation, accurate and physics-based compact models are required. The modeling principles for these devices are somewhat different from conventional bulk MOSFETs, since volume conduction should be considered. For undoped double-gate and surrounding-gate MOSFETs the depletion charge does not need to be included in Poisson's equation, which allows exact analytic solutions of the potential without the charge-sheet approximation, valid for all operating regimes. The gradual channel approximation (which assumes that the quasi Fermi potential stays constant along the direction perpendicular to the channel) is used. A compact expression of the channel current is obtained assuming that transport is based on drift-diffusion.

Accurate models for undoped double-gate [20-23] and surrounding-gate MOSFETs [20],[24-25] have been recently developed using the above principles, showing good agreement with three dimensional numerical simulations. These models assume that the electrostatic control of the channel is so good that shortchannel effects can be neglected. The inclusion of short-channel effects in

ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

multiple gate MOSFET models, using physical equations and without decreasing the order of continuity of the devices, is still a modeling challenge.

For devices with channel lengths shorter than 50 nm, the drift-diffusion mechanism may not be the dominant transport mechanism. Ballistic or quasiballistic transport may occur. Adequate models for nanoscale devices must consider the balllistic or quasi-ballistic regime[26-44]. So far, several models have been developed for multiple gate MOSFETs in the ballistic regime, in particular double-gate and surrounding gate MOSFETs. In these models it has been assumed that the electrostatic control of the channel is strong enough, so that short channel effects can be neglected. Next step in ballistic regime modeling will be the consideration of the short-channel effects.

Anyway, the main modeling challenge regarding transport is the development of a transport model formulation that makes the current tend to the expression in the ballistic regime for nanometer channel lengths and to the expression in the driftdiffusion limit for longer channel lengths.

On the other hand, for films smaller than 10 nm, quantum confinement in the film may not be negligible. The subband contributions should be considered in the drain current equation. The quantum effects affect the distribution of charge in the film and as a consequence, the threshold voltage (increase of the threshold voltage in an n-channel device). Some recent models which consider the band structure of silicon have been recently presented. At very low temperatures, quantum confinement of the charge becomes more important, and this affects the shape of the transconductance characteristics [25], see Fig. 1.5

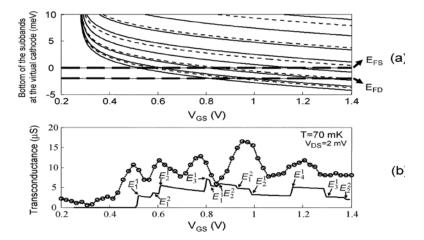


Fig. 1.5. Bottom of subbands and transconductance characteristics of a cylindrical surrounding gate MOSFET with a 65 nm diameter Si film Dotted line: measurements [25] Solid line: model. $V_{ds} = 2 \text{ mV}.$

A succession of peaks and valleys are observed, which correspond, respectively, when the bottom of the subbands cross the quasi-Fermi energy levels at the source and drain. The location of peaks and valleys has been accurately predicted. These models should be still completed with the inclusion of short channel effects.

In the other hand, most of the work done to study the SCEs for the multiple gate MOS devices has neglected the mobile charge density term when solving electrostatic potential. However, it is important in the near threshold regime. For the Double Gate MOSFETs, Linag et. al [45], developed a 2D potential model neglecting the effect of mobile charge term. However they did not introduce any explicit threshold voltage model nor a subthreshold swing model (see Fig. 1.6). Chen et. al [46], have considered the effect of the conduction path to calculate the SCEs for the DG MOSFETs, but the model is not able to calculate the DIBL effect. [47-48] have studied the SCEs for the doped GAA MOS devices, but neglecting the mobile charge. Pie et. al [49], introduced subthreshold swing model

and the threshold voltage roll-off in the FinFET but for high doped channel devices. The model does not provide a good fitting with the numerical simulation, as shown in Fig. 1.7.

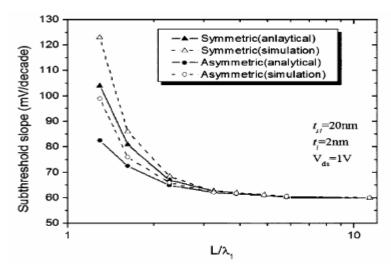


Fig. 1.6. Analytical solutions of the subthreshold slopes for symmetric and asymmetric DG MOSFETs (solid curves) compared with 2-D numerical simulation results (dashed curves)[45]

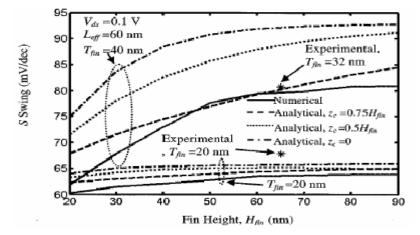


Fig. 1.7 Comparison of subthreshold swing from numerical and analytical solutions for both linear (V = 0.1 V) and saturation (V = 1.5 V) regions. [49]

Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

In this thesis we study the three undoped multiple gate MOS devices, i.e., Double Gate MOSFETs, Cylindrical Gate All Around MOSFET, and Tri-Gate FETs. In this work we have modeled the SCEs for the whole three devices considering the mobile charge density. The SCEs effects that have been studied through this thesis are: Threshold voltage, Subthreshold swing, Threshold voltage roll-off, and DIBL effect. The SCEs have been verified with numerical simulation results from DESSIS, and the allowable experimental results that were done in the Microelectronics Laboratory (DICE) in the Microelectronics Laboratory, Université catholique de Louvain, Belgium.

The thesis organized as: Chapter (2) modeling of SCEs for the undoped three devices, Chapter (3) studies the current transport (Drift-Diffusion, Ballistic, and Quasi Ballistic) for the three devices. Finally chapter (4) summarizes the work done and the future points that needs to studied.

27

CHAPTER TWO

Short Channel Effects (SCEs) in Undoped Multiple Gate MOS Devices

In this Chapter

This chapter is aimed to study the physics insight of the Multiple Gate MOS Devices; Gate All Around MOSFETs, Double Gate MOSFETs, and FinFETs.

The chapter is divided into four parts based on the device structures,

Section 2A) is divided into two main Parts, in both parts an analytical, physicallybased, models for the threshold voltage and the subthreshold swing of undoped cylindrical Gate All Around (GAA) MOSFETs have been derived based on an analytical solution of the two-dimensional (2-D) Poisson equation (in cylindrical coordinates) with the mobile charge term included. In (2A-1), The model was not able to calculate the DIBL effects, it was only valid for low drain-source voltages, as it was done before by Chen., et. al[46] for the Double Gate MOSFET. In (2A-2), the model has been modified by solving the 2-D Poisson equation taking into account the variations of drain-source voltage, therefore the model was finally able to calculate the all SCEs including DIBL effects.

In section 2B) we have studied the Short Channel Effects in the Undoped Double Gate MOS Devices, by introducing new models for subthreshold swing, Threshold Volatge, Roll-Off and DIBL effects.

Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

28

SCEs in undoped multiple gate MOS

Section 2C) A 3-D analytical model for the undoped FinFET devices, has been studied. We introduced for the first time new models for subthreshold swing, threshold voltage, DIBL, and roll-off.

Section 2D) A comparison have been done between the DG, and GAA MOSFET performances at low subthreshold swing value (S=70mV/Dec), and from this comparison we have predicted the device dimensions to verify this subthreshold swing value.

For the whole device structures, we have taken into account the mobile charge density when solving 2D Poisson equation (in DG MOS Devices), or 3-D Poisson equation (in GAA MOS Devices, and FinFET Devices).

We have verified the GAA, and DG MOS device models by comparison with the numerical simulation results. For the FinFET devices we have validated the subthreshold swing model with both numerical and expermintalas results done at the Microelectronics Laboratory, Université catholique de Louvain, Belgium. The rest of FinFET models have been verified by comparison with the numerical simulation results.

(2-A) Part (I): Short Channel Effects (SCEs) In Undoped Cylindrical Gate All Around MOSFET

In this section

The Poisson equation in cylindrical coordinates for undoped cylindrical GAA MOSFETs at low drain-source voltage values has been solved, and from the electrostatic potential we have developed new models for threshold voltage, subthreshold swing, and threshold voltage roll-off [50-53].

2A-1 Introduction

The Gate All Around (GAA) MOSFET is considered one the most promising devices for downscaling below 50nm[54-58]. By surrounding the channel completely (Fig. 2A-1a), the gate gains increased electrostatic control of the channel and short-channel effects can be drastically suppressed. Apart from the benefit of allowing a shorter a channel, the GAA MOSFETs can achieve a higher packing density due to their enhanced current drive compared to planar MOSFETs. The downscaling of device dimensions has been the primary factor leading to improvements in IC performance and cost, which contributes to the rapid growth of the semiconductor industry.

However, even in GAA MOSFET devices, Short Channel Effects (SCE), such as the threshold voltage roll-off, the DIBL and the subthreshold swing degradation, cannot be neglected for channel lengths below 100nm [59].

The threshold voltage roll-off is a consequence of the charge sharing effect and typically considered one of the main indications of the short channel effect ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

(GCE) A d : 4 (GCE : d 1d 1 11

(SCE). Another important SCE is the subthreshold swing degradation, which leads to a higher off-state current.

30

The DIBL (*drain-induced barrier lowering*) effect occurs when the barrier height for channel carriers at the edge of the source is reduced due to the influence of drain electric field, upon application of a high drain voltage. As the voltage drop between the source and drain increases, the depletion region under the drain can lower the potential barrier of the source-to-channel junction. If the barrier between the source and channel is decreased, electrons are more freely injected into the channel region. Therefore the threshold voltage is lowered and the gate has less control of the channel.

Compact and accurate models of the threshold voltage (including DIBL) and the subthreshold swing are needed in order to ease the use of these devices in nanoscale integrated circuits.

Most of the existing GAA MOSFET models are based on one-dimensional (1-D) analysis, and are suitable only for *long*-channel devices [58][63-64]. As consequence, they are unable to reproduce the roll-off as the channel length is reduced.

A two-dimensional analysis is necessary to derive threshold voltage and subthreshold swing models that properly account for the channel length dependence. A few 2-D models of the threshold voltage for doped [60-61] and undoped [62] GAA MOSFETs have been presented; however, all of them neglect the effect of the mobile charge density, which can be important in the near-threshold regime (in particular for undoped devices).

In this section, we present 2-D models for the threshold voltage (including the DIBL effect), and subthreshold swing of a cylindrical undoped GAA MOSFET

ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

including the effect of the mobile charge density. The dependences of channel length, thickness and drain-source voltage are accounted for.

An appropriate definition of the threshold voltage for these devices has been used. In bulk MOSFET, it is usually defined as the gate voltage at which the surface potential is equal to two times the Fermi level (band bending difference at the surface between the Fermi level, and the intrinsic level of silicon in the neutral region). Nevertheless, this definition is not adequate for DG and GAA MOSFETs (in particular for undoped devices), where there is inversion or accumulation in the whole film, and not only at the surface. In DG MOSFETs the threshold voltage has been instead defined as the gate voltage at which the minimum sheet density of carriers, Q_{inv}, reaches a value Q_{TH} which can be identified as the onset of the turn-on condition[46],[65]. We have applied the same definition to GAA MOSFETs.

We observed a quite good agreement with the results obtained from 3-D numerical simulations with DESSIS-ISE for different channel lengths/thickness and from low to high drain-source voltage values. The structure of the section is the following: subsection (2A-2) explains the derivation of the potential model from the solution of the 2D Poisson's equation. In subsection (2A-3), the derivation of the expression of the location of the minimum potential is explained. In subsection (2A-4), the derivation of the threshold voltage model, using the value of the minimum potential, is presented and its dependence with the silicon thickness, channel length and compared with 3D numerical simulation results. Subsection (2A-5), presents the model of subthreshold swing.

2A-2 Potential Model Derivation

Fig. 2A-1 shows the cross section of the symmetrical GAA-MOSFET considered in this work. In order to illustrate the behaviour of the compact model we have assumed a GAA-MOSFET with Si-SiO₂ interface parallel to (100) plane. The channel is undoped ($\cong 10^{16} \text{cm}^{-3}$), the n⁺ source and drain are highly doped, and all calculations have been done at room temperature.

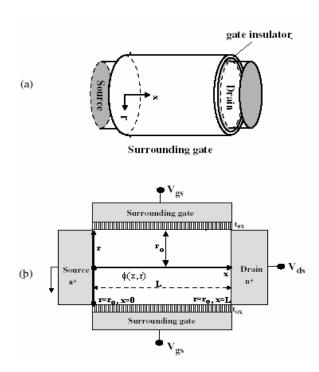


Fig. 2A-1. Cylindrical GAA-MOSFET considered in this work, a) 3-D device structure, and b) Cross section.

The channel electrostatics under threshold condition is governed by the Poisson equation with only the inversion charge term included:

$$\nabla^2 \phi(r, x) = \frac{q}{\varepsilon_{si}} n \tag{2A-1}$$

where ϕ is the electrostatic potential referenced to the Fermi level in the source [66-67], the electron density is given as

$$n = n_i e^{(\phi - \phi_F)/V_T} \tag{2A-2}$$

where n_i is intrinsic electron density in silicon, V_T is the thermal voltage, and ϕ_F is the non-equilibrium quasi- Fermi level referenced to the Fermi level in the source, satisfying the following boundary conditions:

$$\phi_F(0,r) = 0 \tag{2A-3}$$

$$\phi_F(L,r) = V_{DS}, \qquad (2A-4)$$

 V_{ds} being the drain voltage.

The boundary conditions for ϕ are given as:

$$C_{ox}(V_{GS} - \phi_{ms} - \phi(x, \pm \frac{t_{si}}{2})) = \pm \varepsilon_{Si} \frac{\partial \phi(x, r)}{\partial r} \bigg|_{r = \pm \frac{t_{Si}}{2}}$$
(2A-5)

$$\phi(0,r) = V_{bi} \tag{2A-6}$$

$$\phi(L,r) = V_{bi} + V_{ds} \tag{2A-7}$$

where V_{GS} is the gate voltage, ϕ_{ms} is the gate work function referenced to intrinsic silicon, and V_{bi} is the built-in voltage given as $(V_T \cdot ln(N_{S/D}/ni), \sim 0.6V)$, where $N_{S/D}$ is the source/drain doping density. Equation (2A-5) arises from the continuity of the normal component of the displacement vector across interfaces. The sourceand drain-side boundary conditions (2A-6) and (2A-7) are idealized assuming negligible depletion regions inside source/drain, which is justified when the source and drain junctions are abrupt and source/drain are several orders of

magnitude more heavily doped than the channel as in undoped devices.

Determination of the potential ϕ requires Eq.(2A-1) to be coupled with a transport equation (for example, the drift-diffusion equation[75]) for the quasi-Fermi level ϕ_F . Numerical simulations shown that ϕ_F is virtually constant in the channel depth direction and varies only in the channel length direction. While it incurs most of its change near the drain, it stays close to zero in the mid-channel and near-source regions, where the conduction-determining potential barrier (or virtual cathode) is located. Based on these observations, $\phi_F(x,r)$ is approximated to first order as a 1-D δ -function, i.e., is assumed to be zero everywhere except at the end of channel (x=L) where it reaches V_{ds}. Such an approximation is implemented by modifying (2A-1) and (2A-7) as follows:

$$\frac{1}{r}\frac{\partial}{\partial r}r\frac{\partial}{\partial r}\phi(x,r) + \frac{\partial^{2}}{\partial x^{2}}\phi(x,r) = \frac{q}{\varepsilon_{si}}n_{i}e^{\phi(x,r)/V_{T}}$$
(2A-8)
$$\phi(L,r) = V_{bi}$$
(2A-9)

Although this 1-D δ -function approximation of ϕ_F makes subsequent solutions independent of V_{ds} and the final result not able of directly calculating drain induced barrier lowering (DIBL)[46], it is valid to calculate the threshold voltage at low V_{ds} values, and therefore, determine the threshold voltage roll-off. Therefore, the problem is formulated as to solve the 2-D Poisson Eq.(2A-8) for the potential with boundary conditions given in (2A-5), (2A-6), and (2A-9). That is, $\phi(x,r)$ is to be written in the following form:

$$\phi(x,r) = \phi_1(x) + \phi_2(x,r)$$
 (2A-10)

35

SCEs in undoped multiple gate MOS

where $\phi_1(x)$ is the solution to 1-D Poisson equation:

$$\frac{d^2\phi_1(x)}{dx^2} = \frac{q}{\varepsilon_{Si}} n_i e^{\frac{\phi_1(x)}{V_T}}$$
(2A-11)

with boundary conditions:

$$\phi_1(0) = V_{bi} \tag{2A-12}$$

$$\phi_1(L) = V_{bi} \tag{2A-13}$$

And $\phi_2(x, r)$ is the solution to residual 2-D equation,

$$\frac{1}{r}\frac{\partial}{\partial r}r\frac{\partial}{\partial r}\phi_2(x,r) + \frac{\partial^2}{\partial x^2}\phi_2(x,r) = \frac{q}{\varepsilon_{si}}n_i e^{\phi(x,r)/V_T}$$
(2A-14)

with boundary conditions:

$$C_{ox}\left[V_{GS} - \phi_{ms} - \phi_2(x, \pm \frac{t_{si}}{2}) - \phi_1(x)\right] = \pm \varepsilon_{Si} \frac{\partial \phi_2(x, r)}{\partial r}\bigg|_{r = \pm \frac{t_{Si}}{2}}$$
(2A-15)

$$\phi_2(0,r) = 0 \tag{2A-16}$$

$$\phi_2(L, r) = 0 \tag{2A-17}$$

where C_{ox} is an effective oxide capacitance (per unit area) for the cylindrical geometry, given by [67] as:

$$C_{ox} = \varepsilon_{ox} / \left(\frac{t_{Si}}{2} \log(1 + 2t_{ox} / t_{Si}) \right)$$
 (2A-18)

The 1-D equation (2A-11) can be solved [76-78] as:

$$\phi_1(x) = \phi_{0m} + V_T \ln \left\{ \sec^2 \left[B \left(\frac{x}{L} - \frac{1}{2} \right) \right] \right\}$$
(2A-19)

where:

$$\phi_{0m} = V_{bi} - 2V_T \ln \frac{2 + \frac{L}{\lambda_i} e^{\frac{V_{bi}}{2V_T}}}{\pi}$$
(2A-20)

and

$$B = \frac{\pi}{1 + 2\frac{L}{\lambda_i}e^{\frac{-V_{bi}}{2V_T}}}$$
 (2A-21)

 λ_i being the intrinsic Debye length given as:

$$\lambda_i = \sqrt{2V_T \varepsilon_{Si} / q n_i} \tag{2A-22}$$

Fig.2A-2 shows the solution of 1-D Poisson equation in Eq.(2A-19), The minimum potential value, ϕ_{0m} , takes place very close to the middle of the channel length.

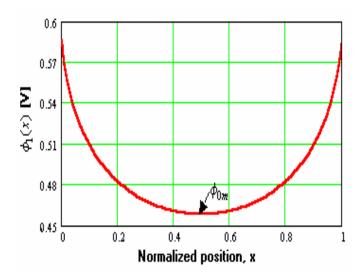


Fig.2A-2 The potential along the channel (normalized) of 1-D Poisson solution, Eq.(2A-19). The channel length is 20nm.

The residual 2-D equation is solved by variable separation, which is a suitable method for solving both Laplace and Poisson equations (a solution guide was introduced in Appendix 2A-1):

$$\phi_2(x,r) = f_1(x) \cdot f_2(r) \tag{2A-23}$$

For $0 \le r \le t_{Si}/2$ and $0 \le x \le L$, $f_1(x)$, and $f_2(r)$ are given as:

$$f_{1}(x) = \begin{cases} 4\sin(\gamma \cdot x) - 2\cos(\gamma \cdot x) \left[\tan(\frac{\gamma}{2} \cdot x_{\min}) + \tan(\frac{\gamma}{2} (x - x_{\min})) - \frac{1}{2} \left(-x_{\min} \right) \right] - \frac{1}{2} \\ \tan(\frac{\gamma}{2} \cdot x_{\min}) \cdot \tan(\frac{\gamma}{2} (x - x_{\min})) \cdot \sin(\gamma \cdot x) \end{cases}$$

$$\left\{ \frac{V_{GS} - \phi_{ms} - \phi_{om}}{\frac{C_{Si}}{C_{ox}}} 2\eta \cdot I_{1}(\eta) + I_{0}(\eta) \right\} \cdot \frac{\sin(\beta)}{3} \cdot \left[1 - \ln(\eta/2) \right]$$

$$(2A-24)$$

$$f_2(r) = I_0(2\eta \cdot r) \cdot (1 - \ln(\eta \cdot r)) \tag{2A-25}$$

where I_0 , and I_1 , are the zeroth order modified Bessel function of the first kind, and the first order modified Bessel function of the first kind. $\gamma(=2B/L)$ is the separation factor and $\eta = B \cdot t_{Si} / 2 \cdot L$. The total potential can be obtained by substituting both Eq.(2A-19), and Eq.(2A-23) in Eq.(2A-10). We have observed that the model exhibits the expected symmetry of the potential along the GAA MOSFET axis.

2A-3 Threshold voltage derivation

The minimum point at which the potential reaches its minimum value at low V_{ds} is approximately at the middle of the channel. The determination of the minimum

potential is necessary for the threshold voltage calculation. We rewrite Eq.(2A-10) at the minimum potential value as:

$$\phi_{\min}(x, r) = \phi_{1\min}(x) + \phi_{2\min}(x, r)$$
 (2A-26)

where:

$$\phi_{1\min}(x) = \phi_1(x = 0.5) = \phi_{om} \tag{2A-27}$$

and

$$\phi_{2\min}(x,r) = \alpha \cdot \phi_2(x = 0.5, r) \tag{2A-28}$$

where $\alpha (\cong 0.6-0.75)$ is constant and can be calculated from the fact that $d\phi_{min}/dV_{GS}|_{L\to\infty} = 1$ [65].

The threshold voltage is defined as the gate voltage at which the minimum sheet density of carriers, Q_{inv} , reaches a value Q_{TH} adequate for identifying the turn-on condition[65],[46]. The numerical simulation results indicates that $Q_{TH} \approx 1.2 \cdot 10^{12} \ cm^{-2}$ (Appendix 2A-1). The minimum sheet density of the channel carriers Q_{inv} is obtained by integrating their spatial density throughout the entire channel thickness at the channel location where the potential is minimum as:

$$Q_{inv} = \int_{-t_{Si}/2}^{t_{Si}/2} n_i e^{\phi_{min}/V_T} dr = 2 \int_{0}^{t_{Si}/2} n_i e^{\phi_{min}/V_T} dr$$
(2A-29)

One step is sufficient to solve the last integration numerically as:

$$Q_{inv} \approx n_i \cdot t_{si} \cdot e^{[\phi_{om} + \Lambda \cdot (V_{GS} - \phi_{ms} - \phi_{om}) \cdot I_0(\eta)]/V_T}$$
 (2A-30)

where

$$\Lambda = \left(\frac{4}{3}\alpha\right) \left[\frac{C_{si}}{C_{ox}} 2\eta \cdot I_1(\eta) + I_0(\eta) \right]^{-1}$$
(2A-31)

where $e^{\Lambda \cdot I_0(0)/V_T} \approx 0$, and C_{si} is the silicon capacitance per unit channel thickness.

Applying (2A-30) at the threshold voltage condition we find an explicit expression for the threshold voltage as:

$$V_{TH} = \phi_{ms} + \phi_{OM} + \left(V_T \ln \left(\frac{Q_{TH}}{n_i \cdot t_{si}}\right) - \phi_{om}\right) / \left[\Lambda \cdot I_0(\eta)\right]$$
(2A-32)

Therefore, we have obtained a compact threshold voltage model for GAA MOSFETs.

If the channel length is long enough (at $\alpha (\cong 0.6)$), the parameter Λ is saturated at 0.8, and Eq.(2A-32) can be written as:

$$V_{TH} = \phi_{ms} + \left(\frac{5}{4}V_T \ln \left(\frac{Q_{TH}}{n_i \cdot t_{si}}\right) - \frac{\phi_{om}(4I_0(\eta) - 5)}{4}\right) / I_0(\eta)$$
 (2A-33)

From (2A-33) we can observe that, as expected, for long channel devices the threshold voltage does not depend on the channel length.

We want to remark that quantum effects, which can be important for Si film thicknesses smaller than 10 nm, have not been considered in this work; they lead to a reduction of the channel charge density and an increase of the threshold voltage [69]; however, the quantum correction to the threshold voltage is much smaller in lightly doped devices than in highly doped ones [70]. Another effect caused by quantum confinement in thin Si films is a small reduction of the subthreshold swing [71]; however, as the Si film thickness is decreased, the excellent gate control of the channel makes the electron distribution unimportant and therefore, the quantum correction to the subthreshold swing becomes negligible.

2A-4 Threshold Voltage and its sensitivity

A good agreement with the numerical simulation results (for more details about numerical simulation see appendix 2A-1) was obtained for different channel lengths. Fig.2A-3 shows the plot of the calculated values of the threshold voltage versus the silicon film thickness for two channel lengths. Good agreement is obtained with 3-D numerical simulations (using DESSIS-ISE). For L=100 nm the long-channel approximation, Eq(2A-33) has been applied.

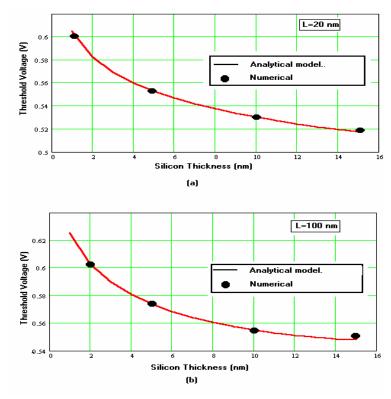


Fig.2A-3 Plots of the threshold voltage versus the Silicon thickness. Comparison between the calculated values of the threshold voltage obtained from a) Eq.(2A-32), and b) Eq.(2A-33), and the values obtained from 3-D numerical simulation results (DESSIS-ISE).

The threshold roll-off, ΔV_{TH} , is defined as the difference between the threshold voltage of a device with a certain channel length and the long-channel threshold voltage (which is independent of the channel length). From Eq.(2A-32), and Eq.(2A-33) we find:

$$\Delta V_{TH} = \left(V_T \ln \left(\frac{Q_{TH}}{n_i \cdot t_{si}}\right) - \phi_{om}\right) \cdot \frac{(1 - 1.25/\Lambda)}{I_0(\eta)}$$
(2A-34)

This roll-off model was compared with 3-D numerical simulation results (obtained with DESSIS-ISE). As shown in Fig. 2A-4, close agreement was observed.

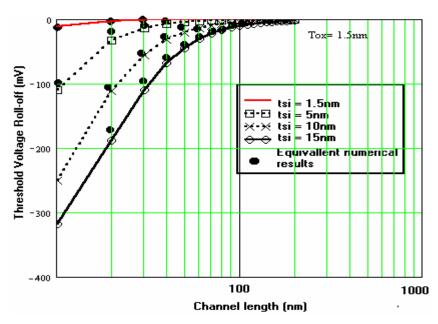


Fig. 2A-4 Plots of the threshold voltage versus the channel length. Solid lines: analytical model. Black circles: 3-D numerical simulation results (DESSIS-ISE).

2A-5 Subthreshold swing model

The point at which the potential reaches to its minimum value can be obtained directly results to be, from (2A-19):

$$x_{\min} = \frac{L}{2} \tag{2A-35}$$

The resulting value of the minimum total potential is, from (2A-10):

$$\phi_{\min} = \phi_{0m} - \cos(2x_m B) \frac{(V_{GS} - \phi_{ms} - \phi_{om})I_0(2\eta \cdot r)}{\frac{C_{Si}}{C_{or}} 2\eta \cdot I_1(\eta) + I_0(\eta)}$$
(2A-36)

Eq.(2A-36) gives the location of the virtual cathode value. The dependence of the virtual cathode value on the biasing values, and the device dimensions are noticed through Eq.(2A-36).

To find an expression for the subthreshold swing, we assume that the subthreshold drain current, I_{ds} , is proportional to the total amount of free electrons diffusing over the virtual cathode [72]:

$$I_{ds} \alpha \int_{0}^{t_{si}/2} n_{i} e^{(\phi_{\min} - \phi_{F})/V_{T}} dr$$
 (2A-37)

The subthreshold swing, S, can be expressed as:

$$S = \frac{\partial V_{GS}}{\partial \log I_D} = \begin{bmatrix} \int_{r=0}^{r_o} n_m(r) \frac{\partial \phi_{\min}}{\partial V_{GS}} dr \\ \int_{r=0}^{r_o} n_m(r) dr \end{bmatrix}^{-1} V_T \ln(10)$$
(2A-38)

where $n_m(r)$ is denoted as:

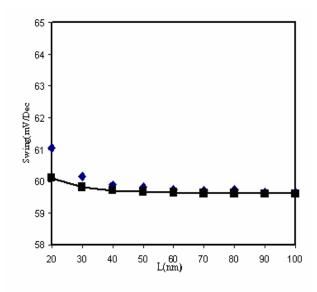
$$n_m(r) = n_i \cdot e^{\phi_{\min}/V_T} \tag{2A-39}$$

Using Eq.(2A-36) in Eq.(2A-38), and taking the value of $n_m(r)$ and $\frac{\partial \phi_{min}}{\partial V_{GS}}(r)$ at

r=t_{Si}/2 (to have an approximate solution of the integral) the final subthreshold swing is obtained as:

$$S = -\frac{2\frac{C_{Si}}{C_{ox}}\eta \cdot I_{1}(\eta) + I_{0}(\eta)}{I_{0}(\eta)\cos(2x_{m}B)}V_{T} \cdot \ln(10)$$
(2A-40)

Therefore, a closed form expression for the subthreshold swing has been introduced in Eq.(2A-40). The minus sign in Eq.(2A-40) will be reversed by the sign of the cosine function to be positive, where B, is closer to π . A good agreement is observed in Fig. 2A-5 compared with the 3-D simulation results for different channel lengths. The model introduced in Eq.(2A-40), produces a maximum relative error of about 0.015 for very short channel lengths.



Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

Fig. 2A-5 The subthreshold swing for Gate All Around MOSFET with t_{si}=5nm, and t_{ox}=1.5nm. Diamond points:3-D numerical simulation results (DESSIS-ISE); lines: analytical model.

(2-A) Part (II): Short Channel Effects (SCEs) In Undoped Cylindrical Gate All Around MOSFET **Including DIBL Effects**

In this section

The model introduced in the Sec.(2.A-1), was not able to calculated the Short Channel Effects SCEs for high drain-source voltage values which limits the model accuracy. In this section, analytical, physically-based, models for the threshold voltage, the subthreshold swing and DIBL of undoped cylindrical Gate All Around (GAA) MOSFETs have been derived based on an analytical solution of the two-dimensional (2-D) Poisson equation (in cylindrical coordinates) including the mobile charge term, by using new techniques that allow to consider the effect of drain-source voltage[80-81].

2A-6 Potential Model Derivation

We shall solve again the Poisson Equation [in Eq. (2A-1)], with complete boundary conditions or,

$$C_{ox}(V_{GS} - \phi_{ms} - \phi(x, r_0)) = \varepsilon_{Si} \frac{\partial \phi(x, r)}{\partial r} \bigg|_{r=r_0}$$
(2A-5)

$$\phi(0,r) = V_{bi} \tag{2A-6}$$

$$\phi(L,r) = V_{bi} + V_{ds} \tag{2A-7}$$

The drain current can be written as,

45

SCEs in undoped multiple gate MOS

$$I_{ds} = q \cdot \mu \cdot n(r, x) \cdot \frac{d\phi_F}{dx} = q \cdot \mu \cdot n_i \cdot e^{[\phi(x, r) - \phi_F]} \frac{d\phi_F}{dx}$$
(2A-41)

or

$$I_{ds} = q \cdot n_{i} \cdot \mu \frac{\int_{0}^{V_{ds}} e^{-\phi_{F}/V_{T}} d\phi_{F}}{\int_{0}^{L} e^{-\phi(x,r)/V_{T}} dx}$$
(2A-42)

where μ is the electron low field mobility, and $r_o=tsi/2$. In subthreshold the quasi-Fermi potential can be considered to have its value at the source end in most of the channel [46]; in fact, this is only the region which significantly contributes to the integral in the denominator on the right-hand side of (2A-9) [68]. Therefore, for practical purposes, in the 2-D Poisson's equation we can use the expression of the electron density with $\phi_F=0$ (value of quasi-Fermi potential at the source)

$$n = n_i e^{\phi(x,r)/V_T} \tag{2A-43}$$

The potential can be written as the sum of two terms: $\phi_o(r)$, which is the solution of the 1D Poisson's equation in the radial direction, and $\phi_I(x,r)$, which is the solution of the remnant 2D differential equation:

$$\phi(x,r) = \phi_0(r) + \phi_1(x,r) \tag{2A-44}$$

Therefore, $\phi_0(x)$ is the solution of:

$$\nabla^2 \phi_0(r) = \frac{q}{\varepsilon_{si}} n \tag{2A-45}$$

where

$$n = n_i e^{\phi_0(r)/V_T}$$
 (2A-46)

The boundary conditions of $\phi_0(r)$ are:

46

SCEs in undoped multiple gate MOS

$$\left. \frac{\partial \phi_0}{\partial r} \right|_{r=0} = 0 \tag{2A-47}$$

and

$$\frac{\varepsilon_{ox}}{t_1} \cdot \left[V_{GS} - \phi_{ms} - \phi_0(r_0) \right] = \varepsilon_{si} \cdot \frac{\partial \phi_0}{\partial r} \bigg|_{r_s}$$
(2A-48)

where from [25][67],

$$t_1 = r_0 \ln(1 + t_{ox} / r_0) \tag{2A-49}$$

 $\phi_1(x,r)$ is the solution of the remnant 2D Poisson's equation:

$$\nabla^2 \phi_1(x, r) = \frac{q}{\varepsilon_{si}} n_i e^{\phi(r, x)/V_T} - \frac{q}{\varepsilon_{si}} n_i e^{\phi_0(r)/V_T}$$
(2A-50)

or

$$\nabla^{2} \phi_{1}(x, r) = \frac{q}{\varepsilon_{si}} n_{i} e^{\phi_{0}(r)/V_{T}} \left[e^{\phi_{1}(r, x)/V_{T}} - 1 \right]$$
(2A-51)

Assuming $\phi_I(r,x)/V_T$ is small, Eq.(2A-51) can be reduced to be a Laplace equation form. Therefore, $\phi_1(x,r)$ can be considered the solution of:

$$\frac{1}{r}\frac{\partial}{\partial r}r\frac{\partial}{\partial r}\phi_1(x,r) + \frac{\partial^2}{\partial x^2}\phi_1(x,r) = 0$$
 (2A-52)

where the boundary conditions of $\phi_1(x,r)$ can be written as:

$$\phi_1(0,r) = V_{bi} - \phi_0(r)$$
 (2A-53)

$$\phi_1(L,r) = V_{ds} + V_{bi} - \phi_0(r) \tag{2A-54}$$

and

$$\frac{\varepsilon_{ox}}{t_1} \cdot \phi_1(r_0, x) = \varepsilon_{si} \cdot \frac{\partial \phi_1(r_0, x)}{\partial r} \bigg|_{r_0}$$
(2A-55)

The solution for the 1-D potential term $\phi_0(r)$ is given by [58][67]:

$$\phi_0(r) = V_T \cdot \ln \left[\frac{32}{\delta} \frac{B_n}{\left(4B_n - r^2\right)^2} \right]$$
 (2A-56)

The solution of (2A-52) with the boundary conditions (2A-53)-(2A-55) is (for details about the solving procedure see Appendix 2A-2):

$$\phi_1(r,x) = \left[C_0 \cdot e^{\lambda \frac{x}{r_0}} + C_1 \cdot e^{-\lambda \frac{x}{r_0}} \right] \cdot J_0(\lambda \cdot r)$$
(2A-57)

where

$$\delta = \frac{q}{\varepsilon_{si} \cdot V_T} n_i \cdot r_0^2 \tag{2A-58}$$

and

$$C_0 = \frac{1}{N^2} \cdot \left[S_1 \cdot (V_{DS} + V_{bi}) - (S_2 + 1) \cdot V_A \right]$$
 (2A-59)

$$C_1 = \frac{1}{N^2} \cdot [S_2 \cdot V_A - S_1 \cdot V_B]$$
 (2A-60)

where S_1 , and S_2 can be considered scaling factors depending on the device dimensions. V_A , and V_B being the biasing effects due to drain and gate-source potentials their values listed below:

$$S_1 = \frac{J_1(\lambda)}{\lambda} \tag{2A-61}$$

$$S_2 = \frac{1 - e^{\lambda \frac{L}{r_0}}}{2 \sinh\left(\lambda \frac{L}{r_0}\right)} \tag{2A-62}$$

$$V_A = J_0 \left(\frac{\lambda}{2}\right) \cdot \left[\frac{\phi_{s0}}{2} + V_T\right] \tag{2A-63}$$

48

SCEs in undoped multiple gate MOS

$$V_{B} = \frac{V_{bi} \left(1 - e^{\lambda \frac{L}{r_{0}}}\right) + V_{ds}}{2 \sinh\left(\lambda \frac{L}{r_{0}}\right)}$$
(2A-64)

And

$$N^{2} = \frac{J_{0}(\lambda)^{2}}{2} \cdot \left[1 + \frac{(C_{r})^{2}}{\lambda^{2}} \right]$$
 (2A-65)

$$C_r = \frac{\varepsilon_{ox} \cdot t_2}{t_1 \cdot \varepsilon_{si}} \tag{2A-66}$$

$$\lambda \frac{J_1(\lambda)}{J_0(\lambda)} = C_r \tag{2A-67}$$

 ϕ_{s0} is the surface potential of long-channel devices (1D surface potential, obtained from (2A-56) using r=r₀), t₂, and t₁ are device radius, and the modified oxide thickness given by[25][67]. J_0 , and J_1 are the zeros of Bessel function type zero, and one respectively. The constant B_n , in Eq.(2A-56) can be calculated from the boundary condition of Eq.(2A-48). The total potential is calculated by using the expressions of (2A-56) and (2A-57) in (2A-44).

A good agreement has been found between the model we have introduced and the classical 3D numerical simulation results for both low, and high drain-source voltage values as shown in Fig.2A-6 (for V_{GS} =0.1V).

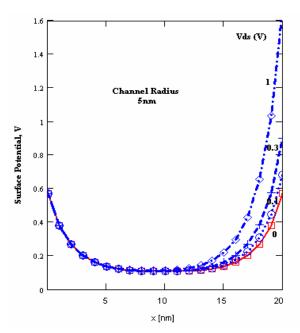


Fig. 2A-6. The surface potential distribution along the channel, for silicon radius is 5nm, and L is 20nm.

2A-7 Virtual Cathode: Value and position

The virtual cathode, or the minimum potential can be calculated from the total potential as:

$$\phi_{\min}(r) = \phi_0(r) + \phi_1(x, r)\Big|_{\min}$$
 (2A-68)

 $\phi_1(x,r)|_{\min}$ is the minimum potential along the longitudinal direction, and can be calculated from

$$\phi_1(x,r)\big|_{\min} = \phi_1(x_{\min},r)$$
 (2A-69)

Where

$$\left. \frac{\partial \phi_1(x,r)}{\partial x} \right|_{x_{\min}} = 0 \tag{2A-70}$$

Using Eq.(2A-70) in Eq.(2A-44) we obtain the following expression of x_{min} ,

$$x_{\min} = \frac{L}{2} - \frac{r_0}{2 \cdot \lambda} \cdot \ln \left[\frac{S_1 \cdot \left[V_{bi} \cdot \left(1 - e^{-L\frac{\lambda}{r_0}} \right) + V_{ds} \right] - \left(1 - e^{-L\frac{\lambda}{r_0}} \right) \cdot V_A}{S_1 \cdot \left[V_{bi} \cdot \left(1 - e^{-L\frac{\lambda}{r_0}} \right) - V_{ds} \cdot e^{-L\frac{\lambda}{R_0}} \right] - \left(1 - e^{-L\frac{\lambda}{r_0}} \right) \cdot V_A} \right]$$
(2A-71)

where the second term of Eq. (2A-71) is the modified term due to drain-source voltage (see Fig. 2A-7).

At zero drain-source voltage

$$x_{\min} = \frac{L}{2} \tag{2A-72}$$

However, at high drain-source voltage value the virtual cathode becomes closer to source end.

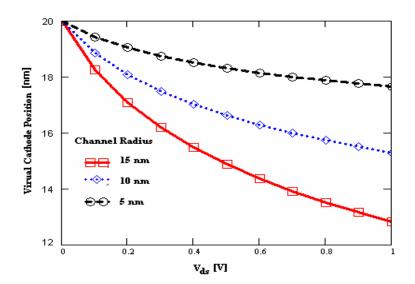


Fig.2A-7 Virtual cathode position vs. Drain-Source Voltage. The channel length is 40nm.

2A-8 Inversion charge and Threshold voltage

Use the same definition for the inversion charge that introduced before in Eq. (2A-29), or

$$Q_{inv} = 2 \int_{0}^{r_0} n_i e^{\phi \left[x_{\min}, \frac{r}{r_0} \right] / V_T} dr$$
 (2A-73)

The integral in (2A-73) can be approximated by its value at $0.5r_0$ [21][46]. After some mathematical manipulations, one obtains:

$$V_{TH} = \phi_{ms} + \frac{1}{1 - S_{gs}} \cdot \left(V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot r_o} \right) - S_{ds} \right)$$
 (2A-74)

 Q_{TH} is the value at which the mobile charge density will reach its threshold value, and found numerically to be $\sim 10^{12} \text{cm}^{-2}$.

In Eq.(2A-74):

$$S_{ds} = \frac{J_0\left(\frac{\lambda}{2}\right)}{N^2} S_1 \cdot \frac{\left[V_{bi} \cdot \left[\sinh\left(\left[L - x_{\min}\right]\frac{\lambda}{r_0}\right) + \sinh\left(x_{\min}\frac{\lambda}{r_0}\right)\right] + V_{ds} \cdot \sinh\left(x_{\min}\frac{\lambda}{r_0}\right)\right]}{\sinh\left(L\frac{\lambda}{r_0}\right)}$$
(2A-75)

$$S_{gs} = \frac{J_0 \left(\frac{\lambda}{2}\right)^2}{2 \cdot N^2} \cdot \left[e^{x_{\min} \frac{\lambda}{r_0}} - 2 \cdot e^{\frac{L \lambda}{2 r_0}} \cdot \frac{\sinh \left(x_{\min} \frac{\lambda}{r_0}\right) \cdot \sinh \left(\frac{L \lambda}{2 r_0}\right)}{\sinh \left(L \frac{\lambda}{r_0}\right)} \right]$$
(2A-76)

Fig.2A-8 shows threshold voltage for different drain- source voltage values. As the radius increases the threshold voltage tends to be independent of it at low V_{ds} . However, due to the DIBL we observe a decrease of the threshold voltage at higher values of radius when V_{ds} is higher enough.

In devices where the channel is long with respect to the channel radius, S_{gs} , and

 S_{ds} are close to zero. Therefore, the long channel threshold voltage can be written as:

$$V_{TH} = \phi_{ms} + \left(V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot r_o}\right)\right)$$
(2A-77)

Eq. (2A-33) will go to Eq. (2A-77) as α goes to 0.75

Fig.2A-9 shows that the short-channel threshold voltage model in Eq. (2A-74), will tend to the expression of Eq. (2A-77) for long channel devices.

Eq.(2A-74), and Eq.(2A-77) are the threshold voltage models for both short, and long channel devices. The threshold voltage roll-off is obtained as the difference between the threshold voltage at a given length, and the long-channel threshold voltage Eq.(2A-77)

$$\Delta V_{TH} = V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot r_o} \right) \left[\frac{1}{1 - S_{gs}} - 1 \right] - S_{ds}$$
(2A-78)

Therefore, we have obtained a complete scalable threshold voltage model for GAA MOSFETs. The threshold voltage roll-off at low drain-source voltage value (10mV), i.e. Eq.(2A-78), is shown in fig. 2A-10. Good agreement is observed for channel lengths down to 30nm.

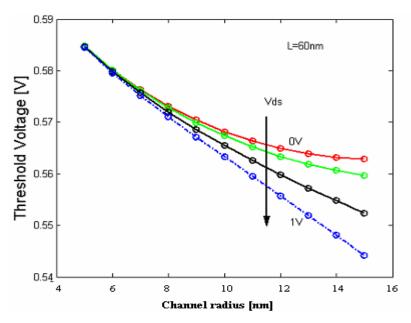


Fig. 2A-8 Threshold voltage vs. channel radius, for different drain-source voltage value. The channel length is 60nm.

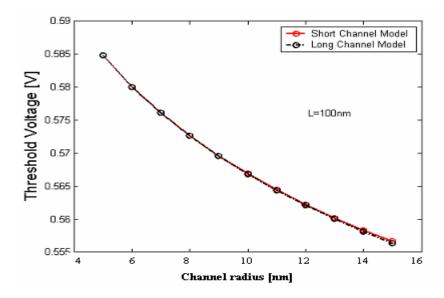
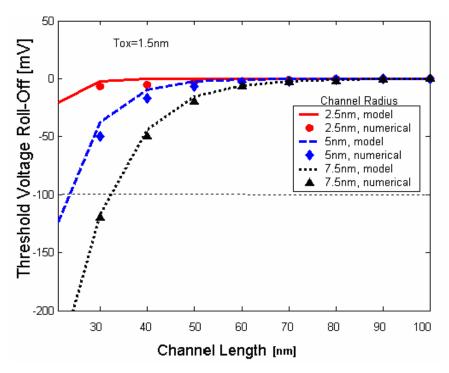


Fig. 2A-9 Threshold voltage calculated using the long-channel model (2A-77) and the general model (2A-74). V_{ds} =10mV



 $\begin{tabular}{ll} \textbf{Fig. 2A-10} Threshold\ Voltage\ Roll-off\ vs.\ channel\ length\ for\ different\ channel\ radius,\ tox=1.5nm, \\ V_{ds}=10mV. \end{tabular}$

The DIBL, is obtained from the difference between the threshold voltage at high drain-source voltage value (e.g., 1V) and the threshold voltage value at low drain-source voltage (0.1V), using (2A-74) (see Fig. 2A-11). The threshold voltage value at low drain-source voltage is:

$$V_{TH0} = \phi_{ms} + \frac{1}{1 - S_{gso}} \cdot \left(V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot r_o} \right) - S_{dso} \right)$$
(2A-79)

where

$$S_{gso} = \frac{J_0 \left(\frac{\lambda}{2}\right)^2}{2 \cdot N^2} \cdot \left[1 + 2 \frac{\sinh\left(\frac{L}{2} \frac{\lambda}{r_0}\right)^2}{\sinh\left(L \frac{\lambda}{r_0}\right)} \right] \cdot e^{-\frac{L}{2} \frac{\lambda}{r_0}}$$
(2A-80)

$$S_{dso} = 2 \frac{J_0\left(\frac{\lambda}{2}\right)}{N^2} \cdot \left[\frac{\sinh\left(\frac{L}{2} \frac{\lambda}{r_0}\right)}{\sinh\left(L \frac{\lambda}{r_0}\right)} \right] \cdot V_{bi}$$
(2A-81)

Finally, the DIBL is obtained as:

$$DIBL = V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot r_o} \right) \left[\frac{1}{1 - S_{gSO}} - \frac{1}{1 - S_{gS}} \right] - \left[\frac{S_{dso}}{1 - S_{gSO}} - \frac{S_{ds}}{1 - S_{gSO}} \right]$$
(2A-82)

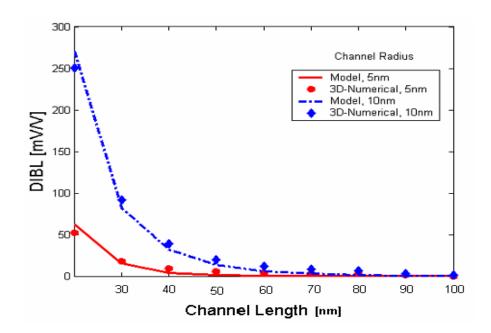


Fig. 2A-11 Drain Induced Barrier Lowering coefficient vs. channel length, for different channel radius, tox=2nm.

2A-9 Subthreshold Swing model

To find an expression for the subthreshold swing, we apply the definition in Eq. (2A-38), or

$$S = \frac{\partial V_{GS}}{\partial \log I_D} = \begin{bmatrix} \int_{r=0}^{r_o} n_m(r) \frac{\partial \phi_{\min}}{\partial V_{GS}} dr \\ \int_{r=0}^{r_o} n_m(r) dr \end{bmatrix}^{-1} V_T \ln(10)$$
(2A-83)

Where $n_m(r)$ is denoted as:

$$n_m(r) = n_i \cdot e^{\phi_{\min}/V_T} \tag{2A-84}$$

The integral in (2A-83) can be approximated by its value at $0.5r_0$. After some mathematical manipulations, one obtain:

$$Swing = \frac{V_T}{1 - S_{gs}} \cdot \ln(10)$$
(2A-85)

Therefore, a closed form expression for the subthreshold swing is obtained (2A-85). In Figs. 2A-12 and 2A-13 a good agreement is observed between our model (2A-85) and 3-D simulation results for different channel lengths, at low and high drain-source voltage, respectively.

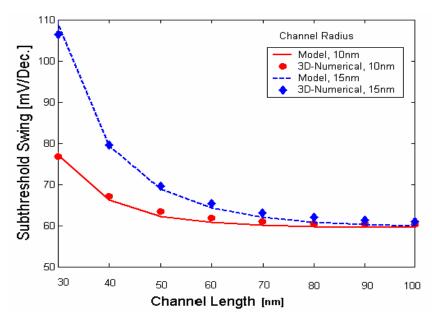


Fig. 2A-12 Subthreshold swing for Gate All Around MOSFET with t_{ox} =2nm, V_{ds} =10mV. Diamond, and Circle points:3-D numerical simulation results (DESSIS-ISE); lines: analytical model.

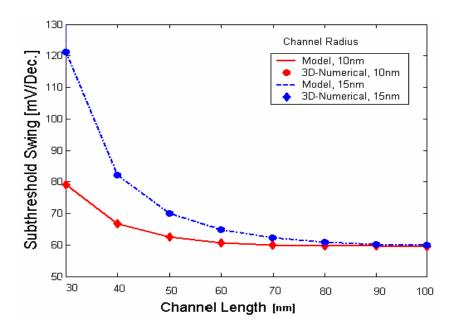


Fig. 2A-13 Subthreshold swing for Gate All Around MOSFET with t_{ox} =2nm, V_{ds} =1V. Diamond, and Circle points:3-D numerical simulation results (DESSIS-ISE); lines: analytical model.

SCEs in undoped multiple gate MOS

Gate MOSFET

(2-B) Short Channel Effects (SCEs) In Undoped Double

In this section

We have developed analytical, physically-based, models for the threshold voltage (including the DIBL effect) and the subthreshold swing of undoped symmetrical Double Gate (DG) MOSFETs [82-83].

2B-1 Introduction

THE double gate architecture is one of the MOSFET structures with the highest potential for the scaling to dimensions below 45 nm [66][25],[93] according to the requirements of the Silicon Roadmap in 2016 [79] and beyond. The downscaling of device dimensions improves the IC performance in digital and RF applications as well as the cost. However, the two-dimensional electrostatic effects become relevant as the channel is aggressively scaled down, and may limit the performance of scaled down MOSFETs, including, of course, DG MOSFETs. When the channel length shrinks down, the electrostatic controllability of the gate over the channel decreases due to the increased charge sharing from source/drain [59].

The main short channel effects, are the threshold voltage roll-off (due to charge sharing), the degradation of the subthreshold swing, and the DIBL (*drain induced barrier lowering*) effect. As a result, the off-state current increases and the on-off current ratio is degraded, and, therefore, the device performance is worsened.

Compact and accurate models of the threshold voltage, DIBL and the

58

SCEs in undoped multiple gate MOS

59

subthreshold swing for DG MOSFETs are needed in order to facilitate and extend the use of these devices in integrated circuits. However, fully 2-D analytical threshold voltage and subthreshold swing models for DG MOSFETs, and in particular for undoped devices, are still missing. Chen et. al. [46] developed a 2-D model for the threshold voltage roll-off of DG undoped devices, but that model did not include DIBL effects. Kranti et al [60], Chen et al. in [46], and Suzuki, et al., [94-95] presented models that accounted for the DIBL effect, but the devices considered were doped and the effect of the mobile charge density was neglected. It has to be remarked that undoped DG MOSFETs show better performances than doped ones, because of their higher mobility. In undoped devices, the effect of the mobile charge density cannot be neglected in the near-threshold regime. It was shown by Francis et al. [96], that even in doped DG MOSFETs, in order to apply standard methods of threshold voltage extraction, volume inversion should be considered when deriving a suitable expression of the threshold voltage. therefore, there is a pressing need to develop an analytical threshold voltage model based on a solution of the 2-D Poisson's equation which includes the carrier concentration term.

The model by Munteanu *et al.* [97] addresses the DIBL effect in a DG MOSFET, but requires iterations to obtain the expression of the electrostatic potential, from which a threshold voltage equation can be derived; on the other hand, this model is only valid for very thin Si films, since it assumes a longitudinal field who does not change along the depth of the film. Besides, it is also based on using an expression of the quasi-Fermi potential below threshold which was derived only for bulk MOSFETs, but which is adapted to DG SOI MOSFETs using fitting parameters, the geometry dependence of them are not clear.

Liang and Taur [45] presented a 2-D analytical solution for the short-channel

SCEs in undoped multiple gate MOS

effects in undoped DG MOSFET; the mobile charge was neglected to solve the 2-D Poisson's equation. This approximation is valid well below threshold (the regime in which the model of [45] the threshold voltage roll-off, DIBL and subthreshold slope are calculated], but near threshold the mobile charge has an effect on the electrostatic potential.

In this section, we present 2-D models for the threshold voltage (including the DIBL effect), and subthreshold swing of a symmetric undoped DG MOSFET including the effect of the mobile charge density. The dependences of channel length, thickness and drain-source voltage are accounted for.

We have used an appropriate definition of the threshold voltage for these devices. In bulk MOSFET, it is usually defined as the gate voltage at which the surface potential is equal to two times the Fermi potential [98]. Nevertheless, this definition is not adequate for DG MOSFETs (in particular for undoped devices), where the inversion and the accumulation take place in the whole film. The threshold voltage can be instead defined as the gate voltage at which the minimum sheet density of carriers, Q_{inv}, reaches a value Q_{TH} that can be identified as the onset of the turn-on condition [46][65].

We observed a very good agreement with 3-D numerical simulations of the threshold voltage and the subthreshold swing for different values of channel lengths and thickness and from low to high drain-source voltage values.

2B-2 Potential Model Derivation

Fig. 2B-1 shows the cross section of the symmetrical DG-MOSFET considered in this work. We have assumed a DG-MOSFET with Si-SiO₂ interface parallel to

60

(100) plane. The channel is undoped (≅10¹⁶cm⁻³), the n⁺ source and drain are highly doped.

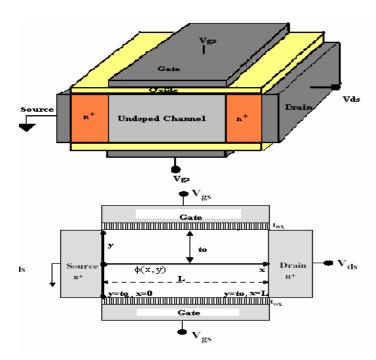


Fig. 2B-1 Symmetrical DG-MOSFET considered in this work, a) 3-D device structure, and b) Cross section.

The channel electrostatics is governed by the Poisson equation. If the device is undoped:

$$\nabla^2 \phi(x, y) = \frac{q}{\varepsilon_{si}} n \tag{2B-1}$$

where ϕ is the electrostatic potential referenced to the Fermi level in the source [25][66], the electron density is given as

$$n = n_i e^{(\phi - \phi_F)/V_T} \tag{2B-2}$$

where n_i is intrinsic electron density in silicon, V_T is the thermal voltage, and ϕ_F

is the non-equilibrium quasi-Fermi level referenced to the Fermi level in the source, satisfying the following boundary conditions (see Fig. 2B-2):

$$\phi_F(0, y) = 0$$
 (2B-3)

$$\phi_F(L, y) = V_{ds} \tag{2B-4}$$

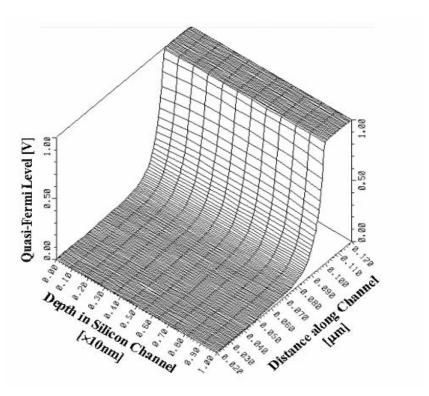


Fig. 2B-2 Quasi Fermi Potential for DG MOSFET.[46] at V_{ds} =1V, mid-gap work function.

 V_{ds} being the drain voltage. The boundary conditions for ϕ are given as:

$$C_{ox}(V_{GS} - \phi_{ms} - \phi(x, y = t_0)) = \varepsilon_{Si} \frac{\partial \phi(x, y)}{\partial y} \bigg|_{y = t_0}$$
(2B-5)

$$\phi(0, y) = V_{bi} \tag{2B-6}$$

63

SCEs in undoped multiple gate MOS

$$\phi(L, y) = V_{bi} + V_{ds} \tag{2B-7}$$

where V_{GS} is the gate voltage, ϕ_{ms} is the gate work function referenced to intrinsic silicon, V_{bi} is the built-in voltage given as (~0.6V), and t_0 is half the Si thickness $t_0=t_{Si}/2$

Assuming drift-diffusion transport, the drain current can be written as:

$$I_D = q \cdot \mu \cdot n(x, y) \cdot \frac{d\phi_F}{dx} = q \cdot \mu \cdot n_i \cdot e^{\left[\phi(x, y) - \phi_F\right]/V_T} \frac{d\phi_F}{dx}$$
(2B-8)

٥r

$$I_{D} = q \cdot n_{i} \cdot \mu \frac{\int_{0}^{V_{ds}} e^{-\phi_{F}/V_{T}} d\phi_{F}}{\int_{0}^{L} e^{-\phi(x,y)/V_{T}} dx}$$
(2B-9)

where μ is the electron low field mobility. In the subthreshold regime the quasi-Fermi potential retains its value at the source end in most of the channel [46]; in fact, this region with a constant value of ϕ_F is the only region which significantly contributes to the integral in the denominator on the right-hand side of (2B-9) [68]. Therefore, for practical purposes, in the 2-D Poisson's equation (2B-1) we can use the expression of the electron density with ϕ_F =0 (value of quasi-Fermi potential at the source, see Fig. 2B-2)

$$n = n_i e^{\phi(x,y)/V_T} \tag{2B-10}$$

In order to find an analytical solution, we apply the superposition principle, and we write the potential $\phi(x,y)$ as the sum of two terms: $\phi_{ID}(y)$, which is the solution of the 1-D Poisson's equation in the direction perpendicular to the channel, and $\phi_{2D}(x,y)$, which is the solution of the residual 2-D differential equation:

64

SCEs in undoped multiple gate MOS

$$\phi(x, y) = \phi_{1D}(y) + \phi_{2D}(x, y) \tag{2B-11}$$

Therefore, $\phi_0(y)$ is the solution of:

$$\nabla^2 \phi_{1D}(y) = \frac{q}{\varepsilon_{si}} n \tag{2B-12}$$

where

$$n = n_i e^{\phi_{\text{ID}}(y)/V_T} \tag{2B-13}$$

The boundary conditions of $\phi_0(y)$ are:

$$\left. \frac{\partial \phi_{1D}}{\partial y} \right|_{y=0} = 0 \tag{2B-14}$$

And

$$\frac{\varepsilon_{ox}}{t_{ox}} \cdot \left[V_{GS} - \phi_{ms} - \phi_{1D} (y = t_0) \right] = -\varepsilon_{si} \cdot \frac{\partial \phi_{1D}}{\partial y} \bigg|_{v=t}$$
(2B-15)

where

$$t_0 = \frac{t_{si}}{2} {2B-16}$$

 $\phi_{2D}(x, y)$ is the solution of the residual 2-D Poisson's Equation:

$$\nabla^2 \phi(x, y) = \frac{q}{\mathcal{E}_{si}} n_i e^{\phi_{1D}(y)/V_T} \left[e^{\phi_{2D}(x, y)/V_T} - 1 \right]$$
 (2B-18)

Assuming ϕ_{2D}/V_T is small Eq.2B-18 can be reduced to be a Laplace equation's. This is a reasonable approximation in well behaved devices, with not too strong short-channel effects. This is equivalent to use the superposition of a 1D solution of the Poisson's equation assuming a 1D distribution of the mobile charge, and a 2D solution of Laplace's equation. Therefore, $\phi_{2D}(x,y)$ can be considered the solution of:

Hamdy Mohamde Abd El Hamid ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

65

SCEs in undoped multiple gate MOS

$$\frac{\partial^2}{\partial x}\phi_{2D}(x,y) + \frac{\partial^2}{\partial y^2}\phi_{2D}(x,y) = 0$$
 (2B-19)

Using (2B-11), the boundary conditions of $\phi_{2D}(x, y)$ can be written as:

$$\phi_{2D}(0, y) = V_{bi} - \phi_{1D}(y) \tag{2B-20}$$

$$\phi_{2D}(L, y) = V_{ds} + V_{bi} - \phi_{1D}(y)$$
(2B-21)

And

$$\frac{\mathcal{E}_{ox}}{t_{ox}} \cdot \left[0 - \phi_{2D}(x, y = t_o) \right] = \mathcal{E}_{si} \cdot \frac{\partial \phi_{2D}(x, y)}{\partial y} \bigg|_{y = t_o}$$
(2B-22)

The solution for the 1-D potential term $\phi_0(y)$ is given by [66]:

$$\phi_{1D}(y) = V_T \cdot \ln \left[\frac{B_n^2}{2 \cdot \delta} \sec^2(B_n \cdot y) \right]$$
(2B-23)

The solution of (2B-19) with the boundary conditions (2B-20)-(2B-22) is (for details about the procedure to obtain it see **Appendix 2B**):

$$\phi_{2D}(x,y) = \left[C_0 \cdot e^{\lambda \frac{x-L}{t_0}} + C_1 \cdot e^{-\lambda \frac{x}{t_0}} \right] \cdot \cos(\lambda \cdot y)$$
(2B-24)

Where

$$\delta = \frac{q}{\varepsilon_{si} \cdot V_T} n_i \cdot t_0^2 \tag{2B-25}$$

And

$$C_0 = S_1 \cdot \left[V_{DS} + V_{bi} \cdot \left(1 - e^{-L\frac{\lambda}{t_o}} \right) \right] - S_2 \cdot \phi_{so}$$

$$(2B-26)$$

$$C_1 = S_1 \cdot \left[V_{bi} \cdot \left(1 - e^{-L\frac{\lambda}{t_o}} \right) - V_{ds} \cdot e^{-L\frac{\lambda}{t_o}} \right] - S_2 \cdot \phi_{so}$$

$$(2B-27)$$

 S_1 , and S_2 depend on the device dimensions, and given by

$$S_{1} = \frac{4 \cdot \sin(\lambda)}{\left[2 \cdot \lambda + \sin(2 \cdot \lambda)\right] \cdot \left[1 - e^{-2L\frac{\lambda}{t_{o}}}\right]}$$
(2B-28)

$$S_{2} = \frac{4 \cdot \lambda \cdot \cos\left(\frac{\lambda}{2}\right) \cdot \left[1 - e^{-L\frac{\lambda}{t_{o}}}\right]}{\left[2 \cdot \lambda + \sin(2 \cdot \lambda)\right] \cdot \left[1 - e^{-2L\frac{\lambda}{t_{o}}}\right]}$$
(2B-29)

$$C_r = \frac{\varepsilon_{ox} \cdot t_o}{t_{ox} \cdot \varepsilon_{si}}$$
 (2B-30)

$$2 \cdot \lambda \tan(\lambda) = C_r \tag{2B-31}$$

 ϕ_{s0} is the surface potential of long-channel devices (1D surface potential, obtained from (2B-23) using $y=t_0$). The constant B_n , in Eq.(2B-23) can be calculated from the boundary condition listed in Eq. (2B-15). The total potential is calculated by using (2B-23) and (2B-24) in Eq. (2B-11).

A good agreement has been obtained between the model we have introduced and the 2D numerical simulation results for low, and high drain-source voltage values, as shown in Fig. 2B-3 (for $V_{GS}=1V$). For a long channel device, the device electrostatic potential follows the 1D potential component as shown in Fig. 2B-3a, whereas as we scaled down the device length, the electrostatic potential follows the 2D potential distributions as shown in (Fig. 2B-3b).

The quantum effects, which become relevant for Si film thickness smaller than 10 nm, have not been considered in this work. They originate a reduction of the channel charge density and an increase of the threshold voltage [69]. Anyway, the quantum correction to the threshold voltage is much smaller in lightly doped devices than in highly doped ones [70]. On the other hand, the small reduction of

the subthreshold swing [71] caused by the quantum confinement in thin Si films becomes negligible in extremenly thin Si films [71].

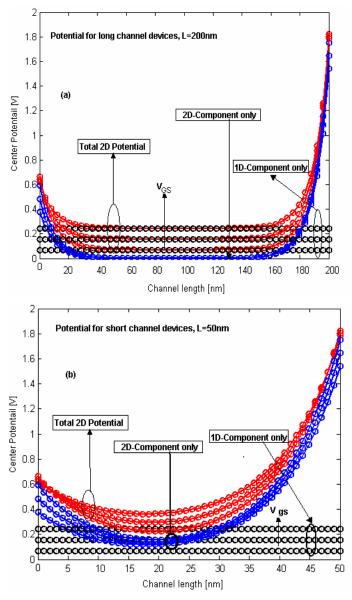


Fig. 2B-3. The center potential distribution along the channel, for a) L=200nm, b)L=50nm, and Vds=1V, mid-gap work function have assumed, $V_{ds}=1V$.

2B-3 Virtual Cathode: Value and position

The minimum potential can be calculated (as defined in Eq. (2A-68)) from the total potential as:

$$\phi_{\min}(x, y) = \phi_{1D}(y) + \phi_{2D}(x, y)\Big|_{\min}$$
 (2B-32)

 $\phi_{2D}(x,y)|_{\min}$ is the minimum potential along the longitudinal direction, and can be obtained from,

$$\phi_{2D}(x,y)|_{\min} = \phi_{2D}(x_{\min},y)$$
 (2B-33)

Where

$$\frac{\partial \phi_{2D}(x,y)}{\partial x}\bigg|_{x} = 0 \tag{2B-34}$$

We obtained the following expression of x_{min} ,

$$x_{\min} = \frac{L}{2} - \frac{t_0}{2 \cdot \lambda} \cdot \ln \left[\frac{\left[V_{bi} \cdot \left(1 - e^{-L\frac{\lambda}{t_0}} \right) + V_{ds} \right] - \lambda \cdot \frac{\cos\left(\frac{\lambda}{2}\right)}{\sin(\lambda)} \left(1 - e^{-L\frac{\lambda}{t_0}} \right) \cdot \phi_{so}}{\left[V_{bi} \cdot \left(1 - e^{-L\frac{\lambda}{t_0}} \right) - V_{ds} \cdot e^{-L\frac{\lambda}{t_0}} \right] - \lambda \cdot \frac{\cos\left(\frac{\lambda}{2}\right)}{\sin(\lambda)} \left(1 - e^{-L\frac{\lambda}{t_0}} \right) \cdot \phi_{so}} \right]$$
(2B-35)

We can see from Eq.2B-35, that at zero drain-source voltage $x_{\min} = 0.5L$. At high drain-source voltage value the virtual cathode becomes closer to source end.

By substituting Eq. (2B-35) into the total potential equation (2B-32), we obtain the virtual cathode value at different Si thickness as shown in Fig. (2B-4), for long channel devices (Fig. 2B-4a), and for short channel devices (Fig. 2B-4b).

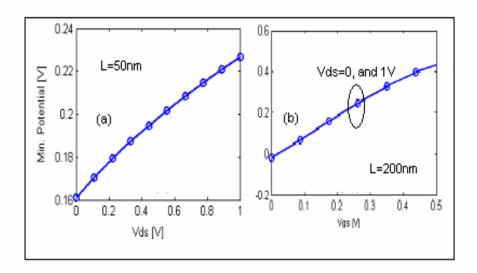


Fig. 2B-4. The minimum potential value, for a) L=200nm, and b)L=50nm

2B-4 Inversion charge and Threshold voltage

The carrier charge sheet density Q_{inv} at the potential minimum is obtained by integrating its spatial density throughout the entire film thickness:

$$Q_{inv} = 2 \int_{0}^{t_0} n_i e^{\phi[x_{\min}, y]/V_T} dy$$
 (2B-36)

The integral in (2B-36) can be approximated by considering the integrand fixed at its value at $0.5t_0$. (See Appendix 2B), since, as shown by Chen *et al.* [46], that is the location of the effective conductive path (validated with numerical simulations). After some mathematical manipulations, we obtain:

$$V_{TH} = \phi_{mS} + \frac{1}{1 - S_{gS}} \cdot \left(V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot t_o} \right) - S_{dS} \right)$$
(2B-37)

70

SCEs in undoped multiple gate MOS

 Q_{TH} is the value at which the inversion charge a threshold value, and found numerically to be ~ 3.10^{10} cm⁻² [46]. In Eq. (2B-37),

$$S_{ds} = 2 \cdot S_1 \cdot \cos\left(\frac{\lambda}{2}\right) \cdot e^{-L\frac{\lambda}{t_0}} \left[V_{ds} \cdot \sinh\left(x_{\min} \frac{\lambda}{t_0}\right) + 2 \cdot V_{bi} \cdot \sinh\left(\frac{L}{2} \frac{\lambda}{t_0}\right) \cdot \cosh\left(\left[x_{\min} - \frac{L}{2}\right] \frac{\lambda}{t_0}\right) \right]$$
 (2B-38)

And,

$$S_{gs} = 2 \cdot S_2 \cdot \cos\left(\frac{\lambda}{2}\right) \cdot e^{-\frac{L \lambda}{2t_0}} \cdot \cosh\left[\left(x_{\min} - \frac{L}{2}\right) \frac{\lambda}{t_0}\right]$$
 (2B-39)

In devices where the channel is long with respect to the channel thickness, S_{gs} is close to zero. Therefore, the long channel threshold voltage can be written as:

$$V_{TH} = \phi_{ms} + \left(V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot t_o}\right) - S_{ds}\right)$$
(2B-40)

The threshold voltage derived in Eq. 2B-37, tends to the theoretical long channel value (2B-40) as the channel length increases. For long enough channels, S_{ds} tends to zero and the threshold voltage expression reduces to the one reported by *Chen et. al.*, [46],

$$V_{TH} = \phi_{ms} + V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot t_o} \right)$$
(2B-41)

Eq.(2B-41), and Eq.(2B-37) constitute the threshold voltage compact models for both short, and long channel devices. The DG-MOSFET threshold voltage roll-off can be written as the difference between the values of threshold voltage calculated using Eq. 2B-41 and Eq. 2B-37,

$$\Delta V_{TH} = V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot t_o} \right) \left[1 - \frac{1}{1 - S_{gS}} \right] - S_{dS}$$
(2B-42)

The threshold voltage roll-off shows a good agreement with the numerical results

published by Frank, et. al., [85], which include the DIBL effect, shown in Fig.(2B-5b).

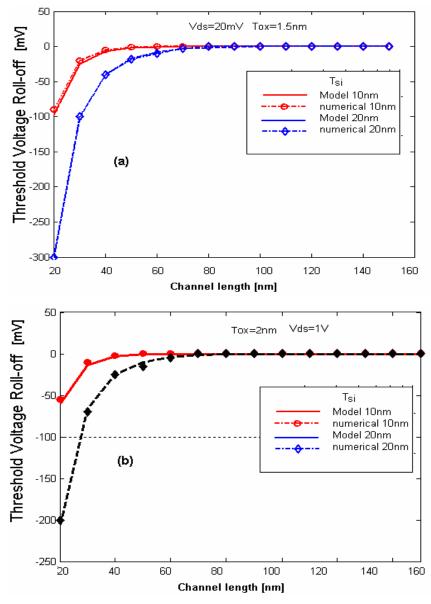


Fig. 2B-5 Threshold Voltage Roll-off vs. channel length, for different channel thickness. a) V_{ds} = 20mV, b) V_{ds} =1V.

The decrease of the threshold voltage with V_{ds} is due to the DIBL effect. The DIBL has to be determined from the difference between the threshold voltage at high drain-source voltage value (e.g., 1V) and the threshold voltage value at low drain-source voltage (0.1V), using (2B-37).

The threshold voltage value at low drain-source voltage is, from (2B-37):

$$V_{TH0} = \phi_{ms} + \frac{1}{1 - S_{gso}} \cdot \left(V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot t_o} \right) - S_{dso} \right)$$
(2B-43)

where

$$S_{gso} = \frac{1 + \cos(\lambda)}{1 + \sin(2 \cdot \lambda) / 2 \cdot \lambda} e^{-2L\frac{\lambda}{t_0}} \cdot \left[\frac{\sinh\left(\frac{L}{2}\frac{\lambda}{t_0}\right)}{\sinh\left(L\frac{\lambda}{t_0}\right)} \right]$$
(2B-44)

and

$$S_{dso} = \frac{\cos\left(\frac{\lambda}{2}\right)/\lambda}{1+\sin(2\cdot\lambda)/2\cdot\lambda} \cdot \left[\frac{\sinh\left(\frac{L}{2}\frac{\lambda}{t_0}\right)}{\sinh\left(L\frac{\lambda}{t_0}\right)}\right] \cdot V_{bi}$$
(2B-45)

The DIBL coefficient can therefore be written as:

$$DIBL = \left\{ V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot t_o} \right) \left[\frac{1}{1 - S_{gso}} - \frac{1}{1 - S_{gs}} \right] - \left[\frac{S_{dso}}{1 - S_{gso}} - \frac{S_{ds}}{1 - S_{gso}} \right] \right\} / \left[V_{ds,high} - V_{ds,low} \right]$$
(2B-46)

As shown in Fig. (2B-6), very good agreement has been obtained with 2-D numerical simulations using DESSIS-ISE for channel lengths down to 30 nm.

This confirms that the approximations done do not significantly hamper the accuracy of the model.

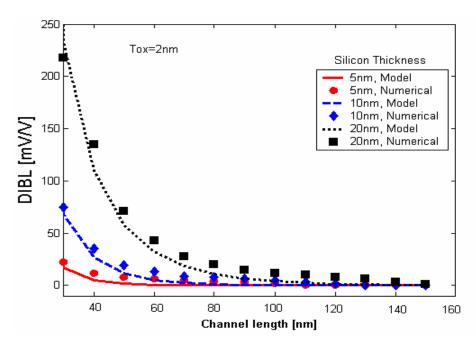


Fig. 2B-6 Drain Induced Barrier Lowering coefficient vs. channel length, for different channel thickness.

2B-5 Subthreshold Swing model

To find an expression for the subthreshold swing, following [72] we assume that the subthreshold drain current, I_D , is proportional to the total amount of the free electrons diffusing over the virtual cathode (see Fig.2B-7):

$$I_D \alpha \int_0^{t_o} n_i e^{(\phi_{\min} - \phi_F)/V_T} dy$$
 (2B-47)

The subthreshold swing, S, can be expressed as:

$$S = \frac{\partial V_{GS}}{\partial \log I_D} = \begin{bmatrix} \int_{y=0}^{t_o} n_m(y) \frac{\partial \phi_{\min}}{\partial V_{GS}} dy \\ \int_{y=0}^{t_o} n_m(y) dr \end{bmatrix}^{-1} V_T \ln(10)$$
(2B-48)

$$n_m(y) = n_i \cdot e^{\phi_{\min}/V_T} \tag{2B-49}$$

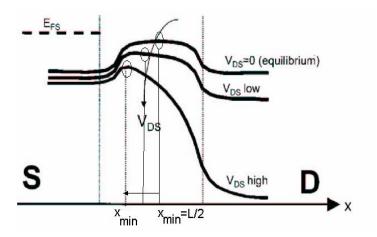


Fig. 2B-7 Virtual cathode position vs. channel length, for different Drain-source, and Gate-source potential .

The integral in (2B-48) can be approximated (See **Appendix 2B**) by considering the integrand fixed at its value at $0.5t_0$; that is the location of the effective conduction path. It was demonstrated that good agreement with numerical simulation results is only possible taking the integrand at the location of the effective conduction path. Taking it at the middle of the film leads to significant differences with numerical simulations (clearly observed in [72]). After some mathematical manipulations, we obtain:

$$Swing = \frac{V_T}{1 - S_{gs}} \cdot \ln(10)$$

(2B-50)

Therefore, a closed form for the subthreshold swing has been introduced in Eq.(2B-50). A good agreement is observed in Fig.2B-8 with the 2-D simulation results for different channel lengths (at V_{ds} =10 mV).

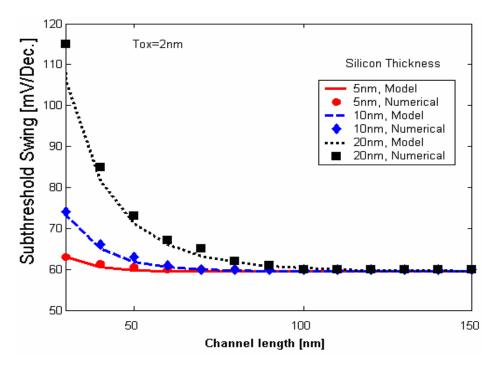


Fig.2B-8 Subthreshold swing for DG MOSFET with t_{ox} =2nm. V_{ds} =10 mV.

ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

76

SCEs in undoped multiple gate MOS

(2-C) A 3-D Analytical Physically-Based Models for Short Channel Effects in Undoped FinFETs

In this section

An analytical, physically-based analysis for undoped FinFET devices in the subthreshold and near threshold regimes has been developed by solving the 3-D Poisson equation, in which the mobile charge term was included. From this analysis, a subthreshold swing model has been developed; this model is also based on a new physically-based analysis of the conduction path. The subthreshold swing model has been verified by comparison with 3-D numerical simulations and measured values; a very good agreement with both 3-D numerical simulation and the experimental results was observed. Also, we have developed analytical models, for threshold voltage, threshold voltage-roll off, and DIBL effects. We have observed from the analysis that the FinFET height has a smaller effect than the FinFET width on the threshold voltage calculations. The threshold voltage calculations are based on extracting a threshold charge from the numerical simulation results of the long channel devices. The models of threshold voltage, Roll-off, DIBL effects have been verified by comparison with 3-D numerical simulations(DESSIS-ISE); a very good agreement with both 3-D numerical simulation has been obtained[99-101].

2C-1 Introduction

As discussed before the double-gate metal-oxide-semiconductor field-effect transistor (DG MOSFET) structure minimizes short channel effects in order to allow a more aggressive device downscaling [102]. Numerical simulations have shown that it can be scalable down to 10-nm gate length [103-104]. However, process complexity can pose a serious technological barrier to the development of

double-gate devices. In 1998, Hisamoto *et al.* introduced the FinFET, demonstrating a not very complex process that yielded n-channel devices with promising performance and scalability [105]. The FinFET uses a single poly-Si layer deposited over a silicon fin patterned to form perfectly aligned gates straddling the fin structure for optimal performance. P-channel FinFETs were subsequently demonstrated using a similar fabrication process and showed excellent and characteristics [106]. Undoped devices are particularly interesting, since they offer higher mobility (because of the decrease of the body scattering effects).

So far very little work has been done on the analytical modeling of FinFET devices, although there have been some works studying the FinFET performance through numerical simulation [107], or studying the device physics from experimental data [108-120]. The reason why so far there is so little work on analytical modeling has probably something to do with the fact that, as the devices dimensions are scaled down, the 3-D electrostatics becomes significant and compact model development becomes a difficult problem to solve.

G. Pei, et. al., [49], presented 3-D subthreshold swing and threshold voltage roll-off models, but they are only valid for doped FinFET devices, i.e. neglecting the mobile charge term (and therefore neglecting volume inversion). However, in undoped devices the mobile charge will affect the electrostatic performance, at least in the near threshold regime. In this work, we introduce an analytical analysis of the 3-D electrostatics for undoped FinFET in the subthreshold and near threshold regimes, and consequently we develop a subthreshold swing model, threshold voltage model, threshold voltage roll-off, and DIBL effects, which have been validated by comparison with both 3-D numerical simulations, and experimental measurements. The devices, fabricated

by the IMEC research group (Leuven, Belgium), have been characterized in the Microelectronics Laboratory, Université catholique de Louvain, Belgium. The fin height is 60nm, with different channel lengths, and different fin widths.

2C-2 Potential Model Derivation

Fig. 2C-1 shows the FinFET structure considered in this work. The channel is practically undoped (≅10¹⁵cm⁻³), the n⁺ source and drain are highly doped, buried oxide thickness thickness of 150nm, oxide thickness 1.5nm, mid-gap work function, and all measurements and calculations have been done at room temperature.

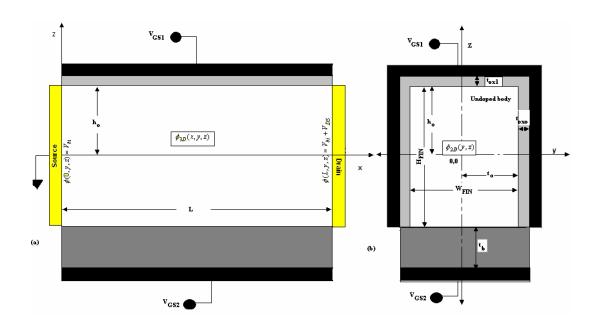


Fig. 2C-1. FinFET Cross section for this work, and also that used in simulator, a) xz-device structure, and b) yz. device structure

As the channel length becomes comparable with the fin height and fin width, the channel electrostatics for the device is governed by the 3-D Poisson's equation, with only the mobile charge term included:

$$\frac{\partial^2 \phi(x, y, z)}{\partial x^2} + \frac{\partial^2 \phi(x, y, z)}{\partial y^2} + \frac{\partial^2 \phi(x, y, z)}{\partial z^2} = \frac{q}{\varepsilon_{si}} n(x, y, z)$$
(2-C1)

The electron density is given as

$$n(x, y, z) = n_i e^{\left[\phi(x, y, z) - \phi_F(x)\right]/V_T}$$
(2-C2)

where n_i is intrinsic electron density in silicon, V_T is the thermal voltage, and ϕ_F is the non-equilibrium quasi- Fermi level referenced to the Fermi level in the source, satisfying the following boundary conditions:

$$\phi_F(0) = 0 \tag{2C-3}$$

$$\phi_F(L) = V_{ds}, \qquad (2C-4)$$

 V_{ds} being the drain-source voltage. Before listing the boundary condition, we need to mention that the model we shall introduce can be applied for: DG MOSFET (if we consider the fin height is very long), Square Gate All Around MOSFET (if we have take into account the bottom gate potential, V_{GS2} see Fig. 2C-1), and finally FinFET (if we ground the bottom gate, and use the same oxide thickness for both the right-left and top gates).

The boundary conditions for ϕ based on the whole alternative device, are given as:

80

SCEs in undoped multiple gate MOS

1) Boundary condition of right gate

$$C_{oxo} \cdot [V_{GS1} - \phi_{ms} - \phi(x, y = t_0, z)] = -\varepsilon_{Si} \frac{\partial \phi(x, y, z)}{\partial y} \bigg|_{y = t_0}$$
(2C-5)

2) Boundary condition of left gate

$$C_{oxo} \cdot \left[V_{GS1} - \phi_{ms} - \phi(x, y = -t_0, z) \right] = \varepsilon_{Si} \frac{\partial \phi(x, y, z)}{\partial y} \bigg|_{y = -t_0}$$
(2C-6)

3) Boundary condition of top gate

$$C_{ox1} \cdot \left[V_{GS1} - \phi_{ms} - \phi(x, y, z = h_o) \right] = -\varepsilon_{Si} \frac{\partial \phi(x, y, z)}{\partial z} \bigg|_{z = h_o}$$
(2C-7)

4) Boundary condition of bottom gate

$$C_{ox2} \cdot \left[V_{GS2} - \phi_{ms} - \phi(x, y, z = -h_o) \right] = \varepsilon_{Si} \frac{\partial \phi(x, y, z)}{\partial z} \bigg|_{z = -h_0}$$
(2C-8)

Notice that we have considered that V_{GS1} is the potential applied on both left/right and top gate. Also, we have considered that the bottom gate biasing (it will be the buried oxide for FinFET as example) is not the same potential as the top gate, V_{GS1} . From the last boundary condition (2C-8) we can say that the device can be identified as a FinFET with and without a back gate biasing, as Square Gate All Around by setting V_{GS1} and V_{GS2} at the same value (if the oxide thickness has the same value everywhere), and finally as a DG MOSFET by removing the top and bottom gate (this can done if considered very high values for the top and bottom gate the oxide thickness). The boundary condition at the source and drain and can be written as,

At the source end

$$\phi(0, y, z) = V_{bi} \tag{2C-9}$$

At the drain end,

$$\phi(L, y, z) = V_{bi} + V_{ds} \tag{2C-10}$$

We should mention here that we have assumed that the Source/Drain to channel junction is abruptly doped, and we have neglected the corner effects.

In the above equations ϕ_{ms} is the gate work function referred to intrinsic silicon, and V_{bi} is the built-in voltage given as (~0.6V, $V_T \cdot ln(N_{S/D}/n_i)$), where Equations (2C-5 to 2C-8) arise from the continuity of the normal component of the displacement vector across interface.

To solve the potential in Eq. (2C-1) using the last boundary conditions we have considered that the potential will be the sum of three potential (the third component included in 2D solution) components as,

$$\phi(x, y, z) = \phi_{2D}(y, z) + \phi_{3D}(x, y, z)$$
(2C-11)

Where $\phi_{2D}(y,z)$ is the 2D potential and is related to 1D potential as,

$$\phi_{2D}(y,z) = \phi_{1D}(y) + \alpha_o(y) \cdot z + \alpha_1(y) \cdot z^2$$
(2C-12)

with boundary conditions,

$$C_{ox1} \cdot \left[V_{GS1} - \phi_{ms} - \phi_{2D}(y, z = h_o) \right] = -\varepsilon_{Si} \frac{\partial \phi_{2D}(y, z)}{\partial z} \bigg|_{z = h_0}$$
(2C-13)

$$C_{ox2} \cdot \left[V_{GS2} - \phi_{ms} - \phi_{2D}(y, z = -h_o) \right] = \varepsilon_{Si} \frac{\partial \phi_{2D}(y, z)}{\partial z} \bigg|_{z = -h_o}$$

$$(2C-14)$$

Assuming drift-diffusion transport, the drain current can be written as:

$$I_{ds} = q \cdot n_i \cdot \mu \frac{\int_{0}^{V_{ds}} e^{-\phi_F/V_T} d\phi_F}{\int_{0}^{L} e^{-\phi(x,y,z)/V_T} dx}$$
(2C-14')

In the subthreshold regime the quasi-Fermi potential retains its value at the source end in most of the channel [46]; in fact, this region with a constant value of ϕ_F is

the only region which significantly contributes to the integral in the denominator on the right-hand side of (2C-14') [68]. Therefore, for practical purposes, in the 3-D Poisson's equation (2C-1) we can use the expression of the electron density with $\phi_F = 0$ (value of the quasi-Fermi potential at the source).

 $\phi_{ID}(y)$ is the solution of,

$$\frac{\partial^2 \phi_{1D}(y)}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i e^{\phi_{1D}(y)/V_T}$$
(2C-15)

with the following boundary conditions,

$$\left. \frac{\partial \phi_{1D}(y)}{\partial y} \right|_{v=0} = 0 \tag{2C-16}$$

And (symmetric boundary condition),

$$C_{oxo} \cdot \left[V_{GS1} - \phi_{ms} - \phi_{1D}(y = t_o) \right] = -\varepsilon_{si} \cdot \frac{\partial \phi_0}{\partial y} \bigg|_{y = t_o}$$
(2C-17)

We found that (see appendix 2B),

$$\phi_{1D}(y) = V_T \cdot \ln \left[\frac{B_n^2}{2 \cdot \delta} \sec^2(B_n \cdot y) \right]$$
(2C-18)

 B_n , δ , α_o , and α_l are indicated in **Appendix 2C.**

 $\phi_{3D}(x,y,z)$ is the solution of the residual 3-D Poisson's Equation:

$$\nabla^{2} \phi_{3D}(x, y, z) = \frac{q}{\varepsilon_{si}} n_{i} e^{\phi_{2D}(x, y)/V_{T}} \left[e^{\phi_{3D}(x, y, z)/V_{T}} - 1 \right]$$
(2C-19)

Assuming $\phi_{3D}N_T$ is small Eq.2C-19 can be reduced to be a Laplace equation's. This is a reasonable approximation in well behaved devices, with not too strong short-channel effects. This is equivalent to use the superposition of a 2D solution of the Poisson's equation assuming a 2D distribution of the mobile charge, and a

3D solution of Laplace's equation. Therefore, $\phi_{3D}(x, y, z)$ can be considered the solution of:

$$\frac{\partial^2 \phi_{3D}(x, y, z)}{\partial x^2} + \frac{\partial^2 \phi_{3D}(x, y, z)}{\partial y^2} + \frac{\partial^2 \phi_{3D}(x, y, z)}{\partial z^2} = 0$$
(2C-20)

with boundary conditions,

$$C_{ox1} \cdot \left[0 - \phi_{3D}(x, y, z = h_o)\right] = -\varepsilon_{Si} \frac{\partial \phi_{3D}(x, y, z)}{\partial z} \bigg|_{z = h_0}$$
(2C-21)

$$C_{ox2} \cdot \left[0 - \phi_{3D}(x, y, z = -h_o)\right] = \varepsilon_{Si} \frac{\partial \phi_{3D}(x, y, z)}{\partial z} \bigg|_{z = -h_o}$$
(2C-22)

$$C_{oxo} \cdot \left[0 - \phi_{3D}(x, y = t_o, z)\right] = -\varepsilon_{si} \cdot \frac{\partial \phi_{3D}(x, y, z)}{\partial y}\bigg|_{y = t_o}$$
(2C-22')

$$\phi_{3D}(0, y, z)|_{Source-end} = V_{bi} - \phi_{2D}(y, z)$$
 (2C-23)

$$\phi_{3D}(L, y, z)\Big|_{Drain-end} = V_{ds} + V_{bi} - \phi_{2D}(y, z)$$
 (2C-24)

After solving the potential for the last components (See Appendix 2C), we obtained that

$$\phi_{3D}(x, y, z) = \cos(\lambda_y \cdot y) \cdot \left\{ \sum_{N=0}^{1} \frac{\Delta P_2}{\Delta R_1} \cos(\lambda_{zN} \cdot z) \cdot \left[V_{ds} \cdot D_1 + V_{bi} \cdot D_o \right] - \left(\frac{S_1}{\Delta R_1} \cos(\lambda_{zN} \cdot z) + \frac{S_o}{\Delta R_o} \cdot \sin(\lambda_{zN} \cdot z) \right) \cdot D_o \right\} (2C-25)$$

$$D_o = \frac{\sinh(\lambda_x \cdot x) - \sinh[\lambda_x \cdot (x - L)]}{\sinh(\lambda_x \cdot L)}$$
(2C-26)

$$D_1 = \frac{\sinh(\lambda_x \cdot x)}{\sinh(\lambda_x \cdot L)}$$
 (2C-27)

Where ΔP_2 , ΔR_o , ΔR_I , S_o , and S_I are scaling factors, and their values have been indicated in **Appendix 2C**. λ_y , λ_z , and λ_x are the eigen values (see **Appendix 2C**), where,

$$\lambda_x = \sqrt{\lambda_z^2 + \lambda_y^2} \tag{2C-28}$$

We need to mention here that we have used the lowest eigen value, for both λ_y , and λ_z . λ_{zo} and λ_{zl} (that appeared in the summation of Eq. (2C-25)) are due to top, and bottom gate boundary conditions.

The total 3-D potential, is obtained by applying Eq. (2C-11) to the potential components (sum of Eq. 2C-12 and 2C-25).

Fig. 2C-2 shows the potential along the device channel, due to Eq. 2C-25, at the top gate and cut line at $y=W_{FIN}/2$ (i.e., at center of the top surface and along the channel), for a drain-source voltage is 1V, and channel length is 50nm. The model have been tested for different channel length in **appendix 2C**.

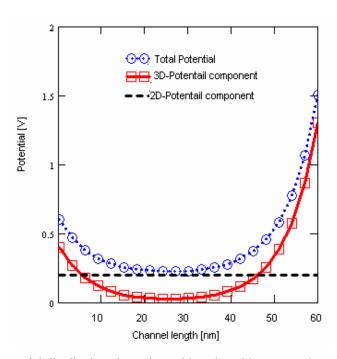


Fig. 2C-2 3-D potential distribution along channel length, with t_{oxo} = t_{ox1} =2nm, and buried oxide thickness 200nm, and V_{GS1} =0.2V, V_{GS2} =0V, and V_{ds} =1V mid-gap work function

2C-3 Subthreshold Swing Model

Considering the potential distribution all over the channel region, the location of the minimum potential in the channel length direction, known as the "virtual cathode," is of great usefulness for the device modeling purpose. This location corresponds to the maximum of an energy barrier, over which free electrons diffuse from the source and then are swept into the drain forming the subthreshold drain current.

By setting,

$$\left. \frac{\partial \phi(x, y, z)}{\partial x} \right|_{x = x_{\min}} = 0 \tag{2C-29}$$

where x_{min} is the location of the virtual cathode, the electrostatic potential at the virtual cathode can found by replacing (x) in the potential equation by its minimum value, where,

$$x_{\min} = \frac{L}{2} - \frac{1}{\lambda_x} \cdot \ln \left[\frac{A' + B' \cdot \tan(\lambda_z \cdot z)}{C' + D' \cdot \tan(\lambda_z \cdot z)} \right]$$
 (2C-30)

As expected, the minimum position will not be dependent on the device width (from the devices symmetry on y direction), but it is dependent on the height position. We found that the effect of the position along the fin height on the virtual cathode value, is very small. The main effects come from the drain-source potential no matter the device dimensions (see **Appendix 2C**).

The subthreshold drain current, I_D , is proportional to the total amount of free electrons diffusing over the virtual cathode, that is,

$$I_{ds} \alpha \int_{y=-t_o}^{t_o} \int_{z=-h_o}^{h_o} n_i \cdot e^{\frac{\phi_{\min}(y,z)}{V_T}} dz dy$$
 (2C-31)

where W_{FIN} , H_{FIN} are the device width and device height. ϕ_F is the difference between the equilibrium Fermi level and non-equilibrium quasi-Fermi level (the quasi-Fermi level referred to the Fermi level, ϕ_F , is assumed to be constant in the channel depth and channel height direction where practically no current flow occurs) caused by the current flow in the channel length direction, the subthreshold swing can be expressed as,

$$S = \frac{\partial V_{GS}}{\partial \log I_{ds}} = \left[\frac{2 \cdot \int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y,z) \frac{\partial \phi_{3D_{-}\min}(y,z)}{\partial V_{GS}} dy dz}}{2 \cdot \int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y,z) dy dz} \right]^{-1} V_T \ln(10)$$
(2C-32)

Where $n_m(y,z)$ is introduced to denote,

$$n_m(y,z) = n_i \cdot e^{\frac{\phi_{3D_{\min}}(y,z)}{V_T}}$$
 (2C-33)

By substituting the virtual cathode value into Eq. (2C-32), the solution of Eq. (2C-32), can be expressed as,

$$S = \left[1 - \sum_{\lambda_{zo,1}} K_1 \cdot \cos(\lambda_y \cdot y_c) \cdot \cos(\lambda_z \cdot z_c) + K_2 \cdot \cos(\lambda_y \cdot y_c) \cdot \sin(\lambda_z \cdot z_c)\right]^{-1} \cdot V_T \cdot \ln(10) \qquad (2C-34)$$

Where K_1 , and K_2 are scaling factors shown in **Appendix 2C**. y_c , and z_c are the conduction paths due to Left/Right Gate, and Top gate respectively.

The exact value for both y_c , and z_c can be calculated from,

$$1 - \cos(\lambda_{y} \cdot y_{c}) \cdot \cos(\lambda_{z} \cdot z_{c}) = \begin{bmatrix} \int_{z=-h_{o}}^{h_{o}} \int_{y=0}^{t_{o}} n_{m}(y,z) \cdot \cos(\lambda_{y} \cdot y) \cdot \cos(\lambda_{z} \cdot z) dy dz \\ \int_{z=-h_{o}}^{h_{o}} \int_{y=0}^{t_{o}} n_{m}(y,z) dy dz \end{bmatrix}^{-1}$$

$$(2C-35)$$

And,

$$\cos(\lambda_{y} \cdot y_{c}) \cdot \sin(\lambda_{z} \cdot z_{c}) = \begin{bmatrix} \int_{z=-h_{o}}^{h_{o}} \int_{y=0}^{t_{o}} n_{m}(y, z) \cdot \cos(\lambda_{y} \cdot y) \cdot \sin(\lambda_{z} \cdot z) dy dz \\ \int_{z=-h_{o}}^{h_{o}} \int_{y=0}^{t_{o}} n_{m}(y, z) dy dz \end{bmatrix}^{-1}$$

$$(2C-36)$$

For high doping (N_C -) values, the dopant induced field is significant, so that the surface potential is much greater than the center potential and the overall conduction is highly confined to surfaces [95]. Consequently, the effective conducting path is found at surfaces subjected to immediate gate control, resulting in an improved S. With decreasing N_C -values, a weakened dopant induced field leads to a flatter shape of potential profile such that the effective conducting path retreats from surfaces into depth, causing weakened gate control and a larger S. Finally, the dopant induced field becomes negligible at low N_A values, and then the potential profile is virtually determined by 3-D effects alone. Consequently, the effective conducting path no longer shifts with N_A , resulting in a constant S value. In undoped (or lightly doped) FinFET devices, the electrostatic potential,

88

being determined by 3-D effects, is greater at the channel center (y=0) [121] than at the surfaces $(y = \pm t_0)$, making the channel center more leaky than anywhere else. However, the difference between the surface and center potentials is quite small because of the 3-D nature of its formation and significantly less than that in heavily doped cases. Due to this relatively even spreading of free electrons, known as volume inversion [122], the overall conduction, y_c , is not confined to the channel center and the effective conducting path should be somewhere in-between surfaces and channel center. However the situation will be a quite different for z_c , because of the asymmetric structure in vertical direction (z-direction), where due the zero potential applied to the buried oxide, the electric field at the fin bottomsurface, which will shift the conduction path to be closer to the top gate surface. Moreover, the quantum effect will affect the conduction path location for both doped and undoped devices; however, we consider here a device with sizes large enough to neglect the quantum confinement.

Mathematically, the integration in y-direction of Eq. (2C-32) can be approximated, due to the device symmetry in y-direction, by its value at $y=t_0/2$; however this cannot be done in z-direction due to the asymmetric device structure. This means that the y_c will be closer to $y=t_o/2$ (i.e., $W_{FIN}/4$). At high drain-source the virtual cathode position will go towards the source end, but this will not prevent the effect of drain-source voltage on the virtual cathode value (i.e., DIBL effect), (see Fig. 2C-1, and potential equation). The increase of drain-source potential will raise the FinFET electric field at the back interface, and the conduction path z_c will shift up more towards the top gate surface. Its is expected that both conduction paths will be strong functions of both device dimensions ratios (i.e. W_{FIN}/H_{FIN}), and devices biasing (i.e., $x_{min}/0.5L$).

Fig. 2C-3 shows the SEM, and TEM images for a one of FinFET device, where its wider as we going towards the top gate, which is more clearly in the schematic diagram in right side of the same figure.

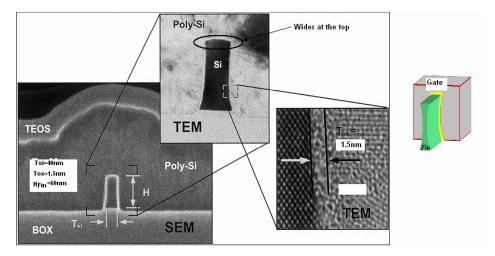


Fig. 2C-3 FinFET SEM , and TEM image used through this work.

A good agreement have been obtained in Fig. 2C-4(a) and (b), at low V_{ds} value, for y_c approximately $t_o/2$, and z_c at approximately at 95% of fin height.

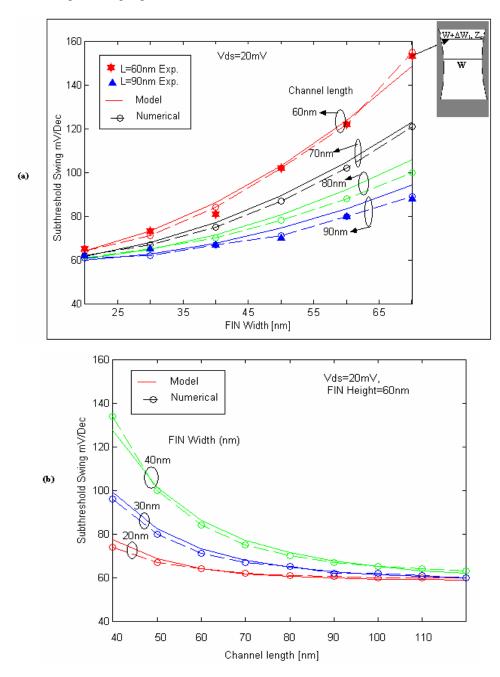


Fig. 2C-4 Subthreshold swing at low drain-source voltage, a) vs. Fin width, and b) vs. Channel length. Solid lines in (a) and (b), are for our model, the dashed circle are the numerical results, and the stars, and triangular in (a) are the experimental results

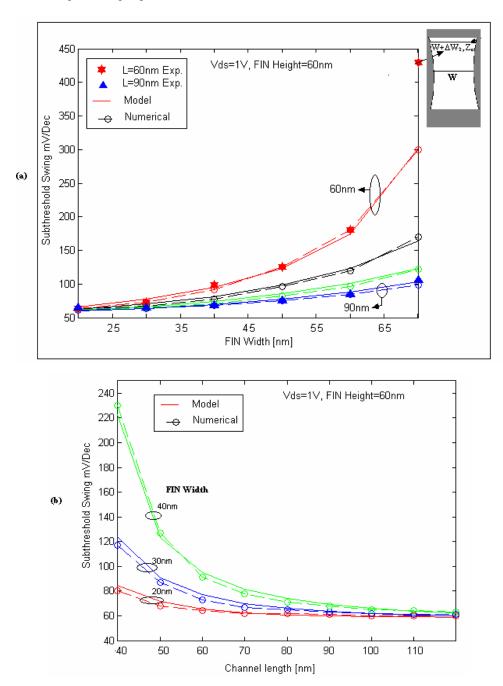


Fig. 2C-5 Subthreshold swing at high drain-source voltage, a) S vs. FIN width, and b) S vs. Channel length. Solid lines in (a) and (b), are for our model, the dashed circle are the numerical results, and the stars, and triangular in (a) are the experimental results

92

At high V_{ds} values, as we have mentioned before, the electric field will increase at the back surface compared to the top gate surface, which will push the conduction path toward the top surface. A good agreement has been obtained in Fig. 2C-5(a) and (b), at high V_{ds} value, for y_c approximately $W_{FIN}/4$ from the center along yaxis, and z_c at approximately at 0.99H_{FIN} from the bottom interface.

The sub-figure shown in Fig. 2C-4(a), (device cross section), shows the actual devices shape. The device width is wider at the top gate than at the center (by ΔW_l). And since the conduction path, " z_c ", at low V_{ds} value is far from the surface, this effect will lead to a negligible value of the effective fin width. However, for high drain-source voltages the conduction path, "z_c" will be pushed up toward the surface at which the fin width becomes wider than the last case (at which $\Delta W_2 > \Delta W_1$), which will introduce a higher subthreshold current and consequently a higher subthreshold swing value, as shown in Fig. 2C-5.a at W_{FIN} =70nm. Fig. 2C-6(a), and (b) show the measured drain current at low and high drain-source voltage for different channel width, at L=90nm.

A good agreement has been obtained for various FinFET widths (at H_{FIN} =60nm) in Fig. 2C-4(b), and Fig. 2C-4(b) against channel length.

After fitting the model with both numerical simulations and experimental data, we found that both y_c and z_c barely change from their original values ($y_c = t_o/2$, and $z_{c}=h_{o}$). Therefore, the model gives acceptable results for all device dimensions, as shown in Fig. 2C-7. In Fig. 2C-7, we have fixed the conduction path value " z_c ", at a value closer to the fin height, and we got a good agreement even if we changed the fin height value, with a slight change of y_c value from its original value as shown in the figure. This change in y_c comes from the effects of the

electric field of the top gate on the right upper and left upper corners as we increase and decrease the Fin height.

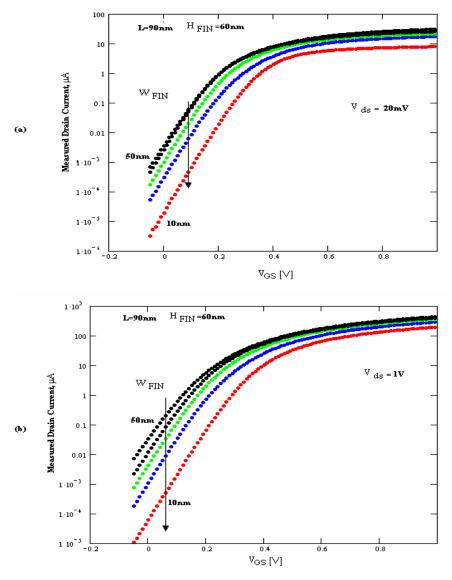


Fig. 2C-6 Measured drain current in logarithmic-scale for a channel length of 90nm, at a)Vds=20mV, and b)1V.

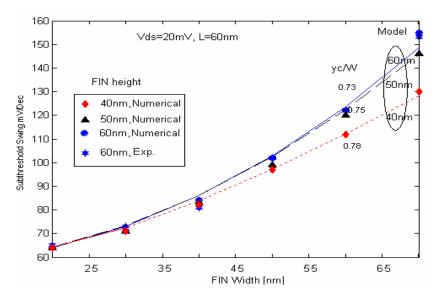


Fig. 2C-7 Subthreshold swing versus Fin height, at channel length=60nm, and $z_c \sim H_{FIN}$. The lines are our model, where the stars for experimental data at 60nm.

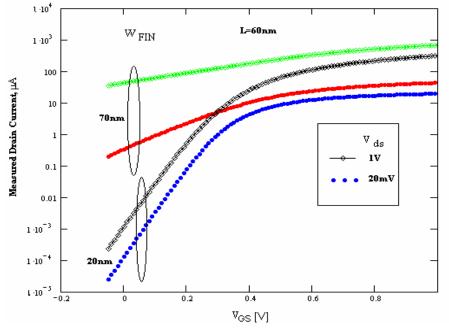


Fig. 2C-8 Measured drain current in Logarithmic-scale, for W_{fin} =20, and 70nm for different drain-source voltage, H_{FIN} =60nm

95

SCEs in undoped multiple gate MOS

Fig. 2C-8 shows the measured drain current (logarithmic) at low and high drain source voltages. At a high drain-voltage, not only the drain current increases for W_{FIN} =70nm when compared to W_{FIN} =20nm, but also the slope increases, because the conduction path at high drain-source voltage will be closer to the surface with a wider width (at which $\Delta W_2 > \Delta W_1$) than the equivalent conduction path at low drain-source voltage value.

2C-4 Threshold Voltage Model

The virtual cathode is considered as a barrier for the electron current and its height is fully controlled by the gate-source voltage at very long channel devices. As the channel length scaled down and high V_{ds} value, the electric field from the drain affects on the virtual cathode value to produce the DIBL effect. The short channel effects are strongly dependent the virtual cathode value. The inversion charge can be calculated as,

$$Q_{inv} = 2 \int_{y=0}^{t_o} \int_{z=-h_o}^{h_o} n_i \cdot e^{\frac{\phi_{\min}(y,z)}{V_T}} dz dy$$
(2C-37)

 $\phi_{min}(y,z)$, is the minimum potential value (virtual cathode), which can be calculated by replacing x by x_{min} in potential equation, Eq. (2C-11), where

$$x_{\min} = \frac{L}{2} - \frac{1}{\lambda_x} \cdot \ln \left[\frac{A + B \cdot \tan(\lambda_z \cdot z)}{C + D \cdot \tan(\lambda_z \cdot z)} \right]$$
 (2C-38)

96

SCEs in undoped multiple gate MOS

$$\begin{split} A &= \frac{\Delta P_2 \cdot \left| V_{ds} + V_{bi} \cdot \left(1 - e^{-\lambda_x \cdot L} \right) \right| - \left(1 - e^{-\lambda_x \cdot L} \right) \cdot S_1}{\Delta R_1 \cdot \left(1 - e^{-2\lambda_x \cdot L} \right)} \\ B &= -\frac{\left(1 - e^{-\lambda_x \cdot L} \right) \cdot S_o}{\Delta R_o \cdot \left(1 - e^{-2\lambda_x \cdot L} \right)} \\ C &= \frac{\Delta P_2}{\Delta R_1} \left[V_{bi} - \frac{\left[V_{ds} + V_{bi} \cdot \left(1 - e^{-\lambda_x \cdot L} \right) \right]}{2 \sinh(\lambda_x \cdot L)} \right] - \frac{S_1}{\Delta R_1} \left[1 - \frac{\left(1 - e^{-\lambda_x \cdot L} \right)}{2 \sinh(\lambda_x \cdot L)} \right], \\ D &= -\frac{S_o}{\Delta R_o} \left[1 - \frac{\left(1 - e^{-\lambda_x \cdot L} \right)}{2 \sinh(\lambda_x \cdot L)} \right] \end{split}$$

The last integral in the equation for Q_{inv} , (2C-37), can be solved by assuming that, in every half of the fin, its main contribution takes place at a location equal to $W_{FIN}/4$; this is the location of the conduction path along the fin width (considering one half of the fin in the y direction) if we consider the FinFET as a Double Gate MOSFET in which the film thickness is equal to the fin width (since it was demonstrated that in DG MOSFETs the conduction path is located at a position equal to $\frac{1}{4}$ of the thickness from the surface, in each half).

However, the device is asymmetric along z-axis (not only the structure but also the biasing is not symmetrical) which will lead to an asymmetric carrier distribution. But we can consider that the result of the integral in Eq. 2C-37, is equal to the value of the integrand at the location of the conduction path over an effective height equal to $(\alpha \ H_{FIN})$, where α (<1) is a correction factor which depends on H_{FIN} , and W_{FIN} and its value is extracted numerically. The inversion charge can be written, in terms of α , as,

$$Q_{inv} = n_i \cdot W_{FIN} \cdot (\alpha \cdot H_{FIN}) \cdot e^{\frac{\phi_{\min}(y_c, z_c)}{V_T}}$$
(2C-39)

 $y_c(\approx W_{FIN}/4)$, and z_c are the conduction paths due to the Left/Right and Top/down gates, respectively. As the inversion charge tends to its threshold value, we can calculate the threshold voltage as,

$$V_{TH} = \phi_{ms} + \frac{1}{1 - S_{gs}} \left[V_T \cdot \ln \left(\frac{Q_o / \alpha}{n_i \cdot W_{FIN} \cdot H_{FIN}} \right) - S_{ds} \right]$$
(2C-40)

 Q_o is threshold charge at certain pair of fin height and fin width. The numerical simulation indicated that there are different threshold charge values based on fin height and fin width and a negligible dependence on device length, contrary to that happens to the threshold charge value for both DG MOSFET, and GAA MOSFET where it was found that there is a unique threshold charge value for both devices.

This indicates the importance of α in the threshold voltage model, which will adapt the model to tend to be DG MOSFET behavior at very long fin height or to be the square GAA MOSFET behavior for a symmetric devices structure. For all device dimensions we can put,

$$V_{TH} = \phi_{ms} + \frac{1}{1 - S_{os}} \left[V_T \cdot \ln \left(\frac{Q_{TH}}{n_i \cdot W_{FIN} \cdot H_{FIN}} \right) - S_{ds} \right]$$
(2C-41)

$$S_{ds} = \sum_{\lambda_{z_0}} \frac{P_2}{R_1} \cdot \cos(\lambda_y \cdot y_c) \cdot \cos(\lambda_z \cdot z_c) \cdot (V_{ds} \cdot D_1 + V_{bi} \cdot D_o) + \frac{V_t}{R_1} \cos\left(\frac{\lambda_y}{2}\right) \cdot \cos(\lambda_z \cdot z_c) \cdot \cos(\lambda_y \cdot y_c)$$
(2C-42)

Where the first term in the last summation accounts for Vds effects on threshold voltage, and second term accounts for the temperature effect. Q_{TH} is threshold charge for the whole device dimensions.

For very long channel devices, both S_{gs} and S_{ds} are going to zero as shown in the Fig. (2C-9).

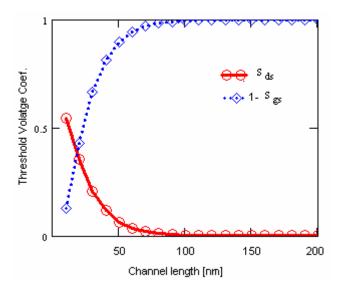


Fig. 2C-9 Threshold Voltage coefficients S_{gs} , and S_{ds} calculations for long channel devices.

The threshold voltage for long channel devices can then be written as,

$$V_{TH} = \phi_{ms} + V_T \cdot \ln \left(\frac{Q_{th}}{n_i \cdot W_{FIN} \cdot H_{FIN}} \right)$$
 (2C-43)

By comparing Eq.(2C-43) with the threshold voltage obtained numerically at a very long channel device, we have obtained the Q_{th} values as shown in Fig.(2C-10). There is a negligible threshold charge dependence on the Fin height, and Fin width as shown Fig.(2C-10). The threshold charge value has found to be (1*10¹⁵/m). Now, we can use this Q_{th} value for all the device dimensions.

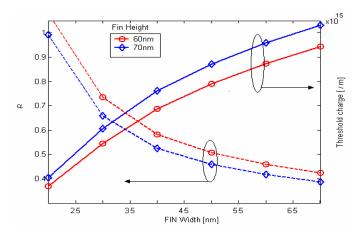


Fig. 2C- 10 Extracted threshold charge value from long threshold voltage model

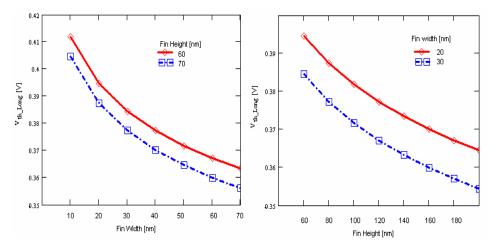


Fig. 2C- 11 long channel threshold voltage vs. a) W $_{\rm fin}$ and b)H $_{\rm fin}$

Fig. 2C-10 shows the comparison between the threshold voltage calculated by model given in Eq.(2C-43), and the numerical simulation results at different Fin heights and different Fin widths. The variation of Q_{TH} value due to the Fin width is higher than variations due to the fin height and consequently affects more the threshold voltage (this because there are two lateral gates that control the

electrostatic inside the film width). For short devices, the model is working well for different Fin widths and for different heights as shown in Fig. 2C-12a, and b.

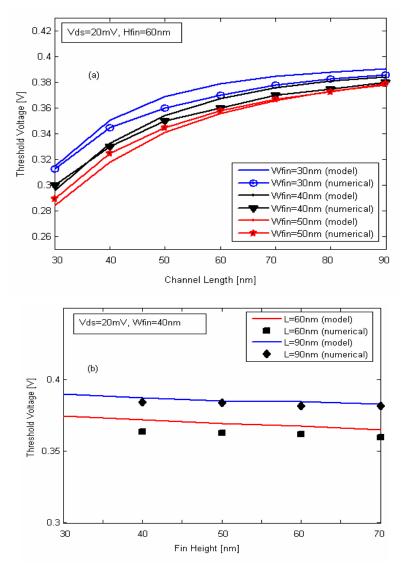


Fig. 2C-12 Threshold voltage for short channel devices for different a) Fin widths, b) Fin heights

The threshold voltage roll-off is an indication of the sensitivity of the short channel effects. It can be calculated by substracting Eq. (2C-43) (threshold voltage for long channel model) from the general model in Eq. (2C-41). A good agreement have been obtained with that obtained numerically for different W_{FIN} , and H_{fin} as shown in Fig. 2C- 13 a, and b.

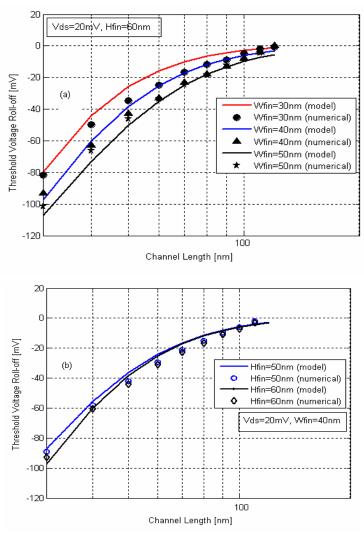


Fig. 2C- 13 Threshold voltage roll-off for different a) Fin widths, and b) Fin heights.

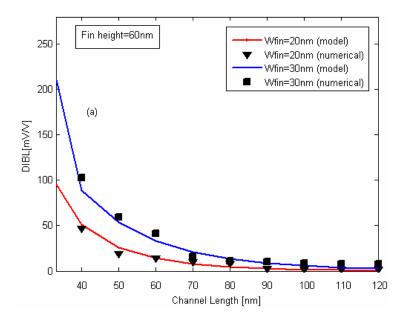
ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

Also, the threshold voltage model given in Eq. (2C-41), is valid for all drainsource voltage values. Therefore the DIBL effect can be calculated in the same manner as DG MOSFET, and GAA MOSFET: by substracting the threshold voltage at high Vds value (e.g., 1V) from a low Vds value (e.g., 20mV). The DIBL effects for different Fin widths are shown in Fig. 2C-14a, and the DIBL effects for different different Fin height are shown in Fig. 2C- 14b.

From the last analysis using our 3-D model we conclude that the Fin height has lower effect on the SCEs than the Fin width, and this is because the SCEs can be improved by controlling the electrostatic potential inside the device, where the Fin width has been surrounding by a two gates leads to a high controllability than the fin height. From our analytical models we have proved that as we increase the number of gates the SCEs also improve, and GAA MOSFET better than both DG MOSFET, and FinFET.

102



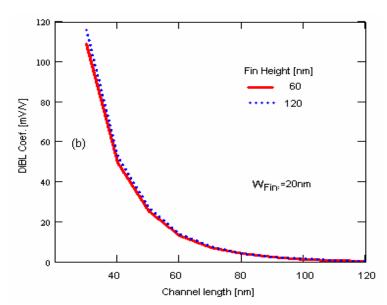


Fig. 2C-14 DIBL vs. channel length for different a) Fin widths, b)For different Fin heights

ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

104

(2D) Scalability limits of Surrounding Gate MOSFETs and Double Gate MOSFETs

In this section

we shall introduce scalability limits comparison between the surrounding gate MOSFET (GAA), and Double Gate MOSFET, the reasons for selecting both devices are to demonstrate that multiple gate devices are better than devices with only one gate and a devices with two gates [123-124].

A small subthreshold swing is required to provide an adequate value of the on-to-off current ratio so that a DG/GAA MOSFET can effectively work as a switch. A small value of the threshold voltage roll-off is an indication of acceptable SCEs. The subthreshold swing of a *long*-channel fully depleted DG/GAA MOSFET has an ideal value, i.e., ~60 mV/dec. To have an acceptable performance, the subthreshold swing has to be close to the ideal value. In this example we have selected an acceptable subthreshold swing value,70mV, and we will obtain the dimensions of the devices that will satisfy this value and also a high drain current, i.e. shorter device. Not only the channel length will be estimated but also the DIBL value which can somehow account for the power supply needed, and the oxide thickness that may be used.

The obtained dimensions for that equivalent subthreshold swing value (i.e., 70mV) of GAA and DG MOSFETs devices are shown in Figs. 2D-(1-2). The device dimensions have been summarized in Tables 2D-1, and 2D-2. The most important conclusion is that the GAA MOSFET can satisfy the same subthreshold swing value as DG MOSFET with a channel length 33% shorter than that given by DG MOSFET with also a lower DIBL value.

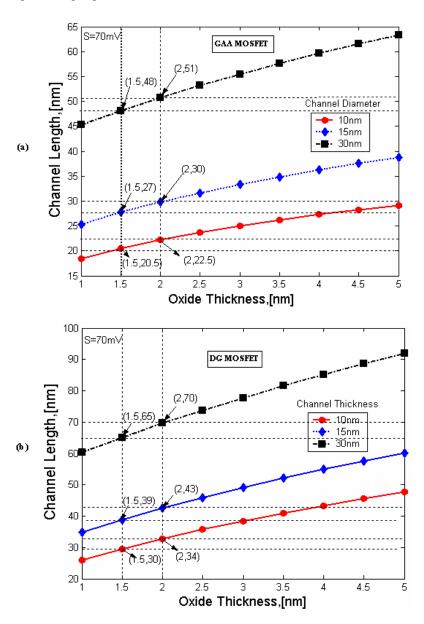


Fig. 2D- 1 Channel length vs. oxide thickness at Vds=0.1V, a) GAA MOSFET, and b) DG MOSFET

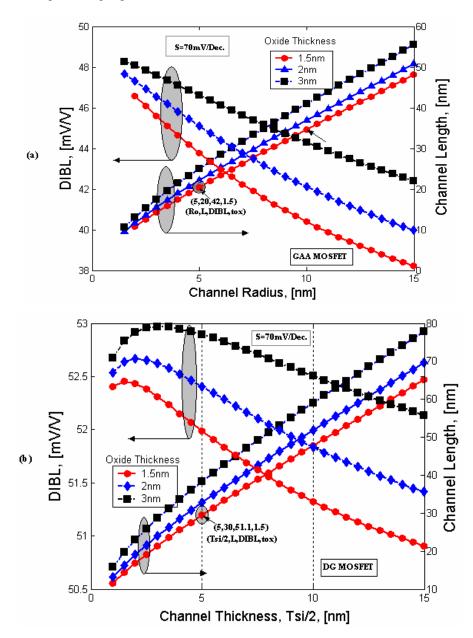


Fig. 2D- 2 DIBL and channel length vs. channel radius/thickness, Vds=0.1V. a) GAA MOSFET, and b) DG MOSFET

107

SCEs in undoped multiple gate MOS

Channel Diameter,	Channel Length,	Oxide Thickness,	DIBL,
[nm]	[nm]	[nm]	[mV/V]
10	20	1.5	42
15	27	1.5	41.6
30	48	1.5	38
10	22.5	2	45
15	30	2	43.5
30	51	2	40

Table 2D-1 GAA MOSFET device characteristics for 70mv

Channel	Channel Length,	Oxide thickness,	DIBL,
Thickness [nm]	[nm]	[nm]	[mV/V]
10	30	1.5	51.1
15	39	1.5	51.75
30	65	1.5	50.8
10	34	2	52.45
15	43	2	52.25
30	70	2	51.45

Table 2D-2 DG MOSFET device characteristics for S=70mV

To obtain a 70mV subthreshold swing, for oxide thickness 1.5nm and low DIBL value, we recommend to use a GAA MOSFET device with a channel length of 20nm, and channel diameter of 10nm which has better characteristics than that

108

SCEs in undoped multiple gate MOS

given by the DG MOSFET characteristics. However, for an oxide thickness below 1.5nm, a shorter device can be obtained but there are non-negligible value of gate tunneling- current. Anyway, as mentioned by *Rahman*, *et. al.* [75] this oxide thickness value (1.5nm) is suitable before the tunneling current is significant.

CHAPTER THREE

Current Transport in Undoped Multiple Gate MOS Devices

In this chapter

We present analytical and continuous DC models for cylindrical undoped surrounding-gate (SGT) MOSFETs, and FinFETs in which the channel current is written as an explicit function of the applied voltages [125]. The model is based on a new unified charge control model developed for this device. The explicit model shows good agreement with the numerical exact solution obtained from the new charge control model, which was previously validated by comparison with 3D numerical simulations. We shall also, explain the ultimate models for DG MOSFET for calculating the DC models.

A compact model, which includes scattering, for the silicon quantum well/wire MOSFET has been introduced [126-127]. The model is based on the Landauer transmission theory and McKelvey's flux theory, and is continuous from below to above threshold and from linear to saturation regions. A good agreement with 2-D numerical simulations (nanoMOS) is obtained with our compact model. The effect of backscattering on both the channel conductance and the average velocity near the source end is studied in this work. For the undoped FinFET devices we have extracted the backscattering coefficient experimentally.

ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

110

(3A) Explicit Continuous Model For Long Channel Undoped Multiple Gate MOSFETs

3A-1 Introduction

In this section, we present explicit continuous DC model for the SGT MOSFET, and FinFET devices. The new model is based on a unified charge control model for a SGT MOSFET, which results from a reformulation of the previous model [128]. The channel current is written in terms of the charge densities at the source and drain ends. Examining, with the new charge control model, the dependences of the channel charge density on the applied voltages in each operating regime, we propose approximate explicit expressions of the channel charge densities in terms of the applied bias, and valid and infinitely continuous through all operating regimes. Therefore, the channel current becomes an explicit function of the bias. Another very important advantage of the new model is the absence of empirical fitting parameters. Therefore, all parameters have a physical meaning.

We have demonstrated that our approximate explicit solution fits very well the numerical exact solution of the charge control model in all operating regimes for GAA MOSFET devices, we used the experimental results to verify our model for the FinFET devices. The resulting explicit model of the channel current shows also a very good agreement with the exact calculation (from the numerical solution of the charge control model) of the channel current. Due to its infinite order of continuity, the new model provides smooth transitions through all operating regimes, which is very desirable in circuit simulation.

3A-2 GAA Model and results

Assuming the gradual channel approximation (GCA), in an undoped (lightly-doped) cylindrical *n*-type SGT-MOSFET (Fig. 3A-1) Poisson's equation takes the following form:

$$\frac{d^2\phi}{dr^2} + \frac{1}{r}\frac{d\phi}{dr} = \frac{kT}{q}\delta e^{\frac{q(\phi - V)}{kT}}$$
(3A-1)

where $\delta = q^2 n_i / kT \varepsilon_{Si}$, being q the electronic charge, $\phi(r)$ the electrostatic potential, and $V(=\phi_F)$ the electron quasi-Fermi potential. It has been assumed that the hole density is negligible compared with the electron density. Equation (3A-1) must satisfy the following boundary conditions:

$$\frac{d\phi}{dr}(r=0) = 0, \qquad \phi(r=R) = \phi_{so}$$
(3A-2)

where ϕ_{so} is the surface potential. The first one is a symmetry condition.

The current mainly flows along the y-direction; therefore, we can assume that V is constant along the r-direction; i.e., V=V(x). Equation (3A-1) can be analytically solved yielding [67]:

$$\phi(\mathbf{r}) = \mathbf{V} + \frac{\mathbf{kT}}{\mathbf{q}} \log \left(\frac{-8\mathbf{B}}{\delta(1 + \mathbf{Br}^2)^2} \right)$$
(3A-3)

B is related to ϕ_{so} through the second boundary condition in (3A-2). The total mobile charge (per unit gate area) can be written as $Q=C_{ox}(V_{GS}-\phi_{ms}-\phi_s)$, where $C_{ox}=\varepsilon_{ox}/(R\ln(1+t_{ox}/R))$. From Gauss's law, the following relation must hold, $R=t_o=T_{si}/2(see\ Fig.\ 3A-1)$:

$$C_{ox}(V_{GS} - \phi_{ms} - \phi_{so}) = Q = \varepsilon_{Si} \frac{d\phi}{dr}\Big|_{r=R}$$
(3A-4)

Substituting (3A-3) into (3A-4) leads to

$$\frac{q(V_{GS} - \phi_{ms} - V)}{kT} - \log\left(\frac{8}{\delta R^2}\right) = \log(1 - \beta) - \log\beta^2 + \eta\left(\frac{1 - \beta}{\beta}\right)$$
(3A-5)

where $\beta = 1 + BR^2$ is a constant (of r) to be determined from (5), and $\eta = 4\varepsilon_{Si}/C_{ox}R$ is a structural parameter. For a given V_{GS} , β can be solved from (3A-5) as a function of V. Note that V varies from the source to the drain, being V=0 at the source end, and $V=V_{ds}$ at the drain end.

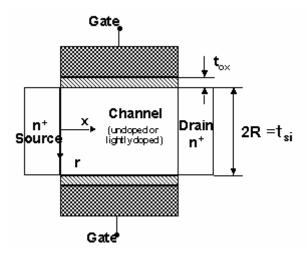


Fig. 3A-1. Cross section of a Surrounding Gate MOSFET

By writing β as a function of Q, we can obtain a charge control model relating the carrier charge density with the bias.

We obtain from (3A-3) that $\frac{d\phi}{dr}\Big|_{r=R} = -\frac{kT}{q} \frac{4BR}{1+BR^2}$; therefore, in terms of β , we

can write
$$\frac{d\phi}{dr}\Big|_{r=R} = 4\frac{kT}{q}\frac{(1-\beta)}{\beta}$$
. Using this expression in Eq. (3A-4),

$$Q = \varepsilon_{Si} \frac{d\phi}{dr}\Big|_{r=R}$$
, we finally can write $Q = Q_0 \frac{1-\beta}{\beta}$, where $Q_0 = \frac{4\varepsilon_{Si}}{R} \frac{kT}{q}$.

Therefore, $\beta = \frac{Q_0}{Q + Q_0}$. Replacing it in (3A-5) we obtain the following charge

control model:

$$\left(V_{GS} - \phi_{ms} - V\right) - \frac{kT}{q} \log\left(\frac{8}{\delta R^2}\right) = \frac{Q}{C_{ox}} + \frac{kT}{q} \log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q} \log\left(\frac{Q + Q_0}{Q_0}\right)$$
(3A-6)

This charge control model, without the third term in the right hand side (RHS), is very similar to the Unified Charge Control Model (UCCM) derived previously for bulk and single-gate fully-depleted SOI MOSFET [129-130]. The third term appears because of the existence of volume accumulation or inversion, although this effect, in the RHS of (3A-6), is also included in the other two terms. Quantum mechanical effects have not been considered in this model; anyway, they are negligible for silicon films thicker than 10 nm (i.e., R>5 nm). For films thinner than 10 nm, quantum confinement should be considered; it leads to a reduction of the channel charge density and an increase of the threshold voltage [67].

The drain current is calculated from:

$$I_{ds} = \mu \frac{2\pi R}{L} \int_{0}^{V_{ds}} Q(V)dV$$
 (3A-7)

We will obtain an expression of I_{ds} in terms of the carrier charge densities. From (3A-6) we obtain:

$$dV = -\frac{dQ}{C_{ox}} + \frac{kT}{q} \left(\frac{dQ}{Q} + \frac{dQ}{Q + Q_0} \right)$$
 (3A-8)

Writing dV as a function of Q and dQ in (3A-7), and integrating between Q_s and Q_d , we obtain:

114

$$I_{ds} = \frac{2\pi R}{L} \mu \left[2 \frac{kT}{q} (Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2C_{ox}} + \frac{kT}{q} Q_0 \log \left[\frac{Q_d + Q_0}{Q_s + Q_0} \right] \right]$$
(3A-9)

Without the third term in RHS, this expression is very similar to the conventional one for bulk or SOI MOSFET.

As in other device models derived from UCCM, the second term in the RHS of (3A-9) dominates in strong inversion (when channel charges are large), and the first term dominates in weak inversion (when channel charges are small). We observed that the third term in RHS is only important near threshold, but cannot neglected in this regime.

To calculate the channel current, we have to solve Eq(3A-6) for $Q=Q_s$ at the source and $Q=Q_d$ at the drain. However, (3A-6) has no exact analytical solution and in principle has to be solved numerically.

Anyway, it is possible to find approximate explicit expressions of Q in the asymptotic limits of subthreshold and above threshold.

We can see that in (3A-6), well above threshold, the two logarithmic terms in RHS are smaller than the first term in RHS, and (3A-6) can be approximated as:

$$\frac{Q}{C_{ox}} = (V_{GS} - \phi_{ms} - V) - \frac{kT}{q} \log \left(\frac{8}{\delta R^2}\right)$$
 (3A-10)

And therefore:

$$Q = C_{ox} \left(V_{GS} - V_0 - V \right) \tag{3A-11}$$

where
$$V_0 = \phi_{ms} + \frac{kT}{q} \log \left(\frac{8}{\delta R^2} \right)$$

On the other hand, we can see that in (3A-6), well below threshold, since $Q \le Q_0$

$$Q = Q_0 \exp\left(\frac{V_{GS} - V_0 - V}{V_{th}}\right) \tag{3A-12}$$

where $V_T = kT/q$

An approximate explicit expression of Q in terms of the bias will, in turn, lead to an explicit model of the channel current. In fact, in previous works explicit solutions of UCCM in bulk and single-gate SOI MOSFETs were proposed and tested [129-131].

An approximate explicit solution of the standard UCCM equation is [131], is:

$$Q = C_{ox} \left(-\frac{2C_{ox}V_{T}^{2}}{Q_{0}} + \sqrt{\left(\frac{2C_{ox}V_{T}^{2}}{Q_{0}}\right)^{2} + 4V_{T}^{2}\log^{2}\left(1 + \exp\left(\frac{V_{GS} - V_{0} - V}{2V_{T}}\right)\right)}\right) (3A-13)$$

This expression tends to (3A-10) and (3A-12) above and below threshold, respectively.

However, we observed that this explicit expression of Q (3A-13) does not work very well above threshold. The modeled Q using (3A-13) is significantly lower than the calculated Q from the numerical solution of (3A-6). The reason of this difference is that the two logarithmic terms in the RHS of (3A-6) increase, although slowly, with V_{GS} above threshold, and they are not negligible. Nevertheless, this effect can be modeled as a correction of V_0 . This logarithmic increase of the threshold voltage with V_{GS} above threshold is also significant in DG SOI MOSFETs [122].

By considering this effect, from (3A-6), we can write the above threshold charge density as:

$$Q = C_{ox} \left(V_{GS} - V_0 - V_T \log \left(\frac{Q'}{Q_0} \right) - V_T \log \left(1 + \frac{Q'}{Q_0} \right) \right)$$
(3A-14)

ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

116

SCEs in undoped multiple gate MOS

where
$$Q' = C_{ox}(V_{GS} - V_0 - V)$$
, is actually a first iteration for Q .

Eq(3A-14) is a much more accurate expression for above threshold than (3A-10). In order to keep a unified expression for Q, we need a unified expression of the threshold voltage. From (3A-12), the threshold voltage is $V_{TH}=V_0$ below threshold, but from (3A-14), above threshold, it is:

$$V_{TH} = V_0 + V_T \log \left(\frac{Q'}{Q_0} \right) + V_T \log \left(1 + \frac{Q'}{Q_0} \right)$$
 (3A-15)

We cannot use Eq.(3A-15) as a unified threshold voltage expression, because the second term in the RHS of (3A-15) would tend to $-\infty$ as we decrease V_{GS} below threshold (since then Q'/Q_0 tends to 0). However, for the same reason, the third term of the RHS tends to 0 as we decrease V_{GS} below threshold, as it should. Note, on the other hand, that well above threshold, $Q'>>Q_0$, and

$$V_{\text{TH}} \approx V_0 + 2V_T \log \left(\frac{Q'}{Q_0} \right)$$
 (3A-16)

A suitable unified expression of the threshold voltage is:

$$V_{TH} = V_0 + 2V_T \log \left(1 + \frac{Q'}{Q_0} \right)$$
 (3A-17)

Below threshold, $Q' \leq Q_0$ and $V_{TH} = V_0$, as it should. Well above threshold,

$$Q >> Q_0$$
 and $V_{TH} \approx V_0 + 2V_T \log \left(\frac{Q}{Q_0}\right)$, as it should.

Our final explicit expression of Q is written as:

$$Q = C_{ox} \left(-\frac{2C_{ox}V_{T}^{2}}{Q_{0}} + \sqrt{\frac{2C_{ox}V_{T}^{2}}{Q_{0}}} \right)^{2} + 4V_{T}^{2}\log^{2}\left(1 + \exp\left(\frac{V_{GS} - V_{TH} + \Delta V_{TH} - V}{2V_{T}}\right)\right)\right)$$
(3A-18)

In (3A-17) V_{TH} is calculated from (3A-17), where Q' is calculated from the unified expression of (3A-13), that ignores the logarithmic corrections of the threshold voltage:

$$Q' = C_{ox} \left(-\frac{2C_{ox}V_T^2}{Q_0} + \sqrt{\left(\frac{2C_{ox}V_T^2}{Q_0}\right)^2 + 4V_T^2 \log^2 \left(1 + \exp\left(\frac{V_{GS} - V_0 - V}{2V_T}\right)\right)} \right) (3A-19)$$

In (3A-18)
$$\Delta V_{TH} = \frac{\frac{2C_{ox}V_T^2}{Q_0}Q'}{Q_0 + Q'}$$
. This term assures the correct behavior of Q

above threshold, since $\Delta V_{TH} \approx \frac{2C_{ox}V_T^2}{Q_0}$ above threshold, and therefore

$$Q \approx C_{ox} \left(-\frac{2C_{ox}V_T^2}{Q_0} + \left(V_{GS} - V_{TH} + \Delta V_{TH} - V\right) \right) \approx C_{ox} \left(V_{GS} - V_{TH} - V\right), \quad \text{as} \quad \text{it}$$

should. Below threshold ΔV_{TH} has no influence since $\Delta V_{TH} \approx \frac{2C_{ox}V_T^2}{Q_0^2}Q^{'} << V_{TH}$.

We can see in the figures 3A-2 and 3A-3 that the expression given by (3A-18) agrees very well with the numerical solution of (3A-5), both below and above threshold, for different values of R. No fitting parameters are used. We assumed a device with channel length L=1 μ m, a silicon film radius R=6.25 nm, a silicon oxide thickness $t_{ox}=1.5$ nm, and a mid-gap gate electrode (gate working function of 4.61 eV).

Therefore, Q_s and Q_d are calculated from (3A-19) using V=0 and $V=V_{ds}$, respectively. The expression of the channel current given in (3A-9) becomes explicit.

We observe in the figures 3A-4 that the new explicit model provides very good agreement with the channel current values obtained using the numerical solution

of (3A-6). The device simulated is the same as for Fig. 3A-2. The fitting is quite good from below to above threshold, and the transitions between the operating regimes are smooth, because of the infinite order of continuity of the model.

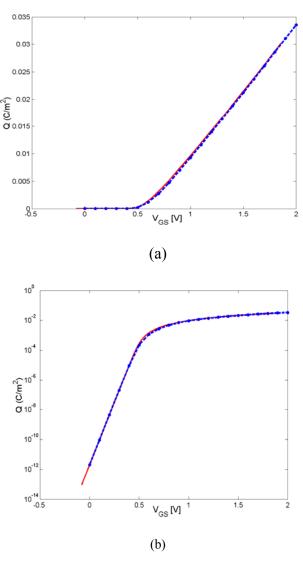


Fig. 3A-2 Channel charge density (per unit area) at the source (*V*=0) in linear (a) and logarithmic scale (b). R=6.25 nm. Dashed line with circles: model using (3A-17). Solid line: Numerical solution of (3A-6).

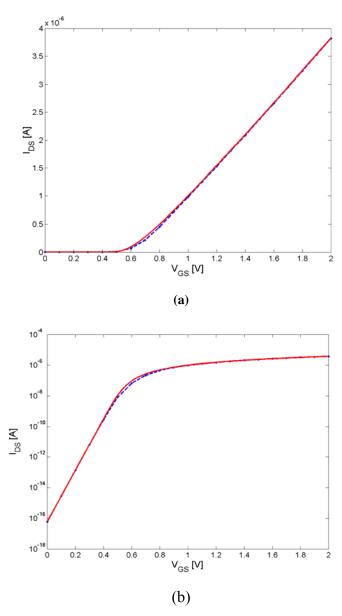


Fig. 3A-3. Transfer characteristic at V_{ds} =0.1 V in linear (a) and logarithmic scale (b). R=6.25 nm. Dashed line with circles: model using (3A-18). Solid line: Model using the numerical solution of (3A-6).

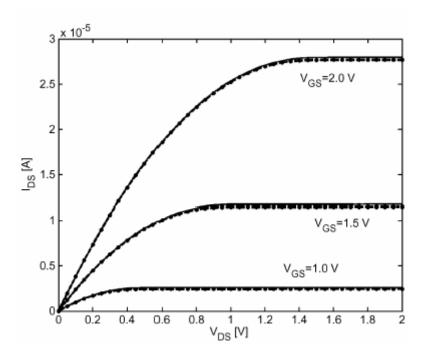


Fig. 3A-4. Output characteristics. R = 6.25 nm. Dashed line with circles: model using (3A-19). Solid line: model using the numerical solution of (3A-6).

3A-3 FinFET long channel model

To find a closed form for the current in the long channel FinFET devices, we shall follow the same procedures as the Gate All Around model that were presented in the last section. From Fig. (3A-5), (see chapter two) the electrostatic potential for the long channel FinFET is following the 2D-potential component in case the Fin height are comparable to the Fin width, however for a very long height the device will follow only the 1D-component.

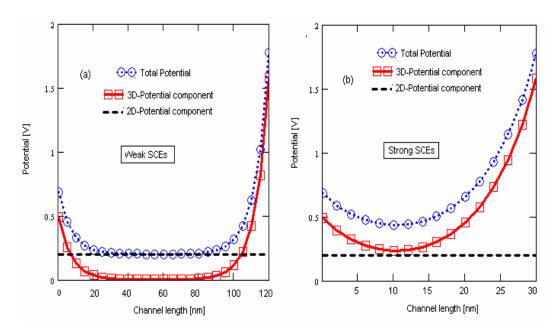


Fig. 3A-5 3D potential components vs. channel length at a) Long channel devices, b) Short channel devices.

Assuming the gradual channel approximation (GCA), in an undoped FinFET, Poisson's equation takes the following form (referring to Fig. 2C-1b):

122

SCEs in undoped multiple gate MOS

$$\frac{\partial^2 \phi_{2D}(y,z)}{\partial y^2} + \frac{\partial^2 \phi_{2D}(y,z)}{\partial z^2} = \frac{q}{\varepsilon_{si}} n(y,z)$$
(3A-20)

$$n(y,z) = n_i e^{[\phi(y,z)-V]/V_T}$$
(3A-21)

We have found (see chapter two, and appendix 2C),

$$\phi_{2D}(y,z) = \phi_{1D}(y) + \alpha_o(y) \cdot z + \alpha_1(y) \cdot z^2$$
(3A-22)

where from chapter two the 1D potential component can written be as,

$$\phi_{1D}(y) = V_T \cdot \ln \left[\frac{B_n^2}{2 \cdot \delta} \sec^2 \left(B_n \cdot y \right) \right] + V$$
(3A-23)

with,

$$\alpha_{1s} = \alpha(y = t_o) = \Delta_{11} \cdot V_{GS1} + \Delta_{22} \cdot V_{GS2} - \Delta_{33} \cdot \phi_{so}$$
(3A-24)

$$\Delta_{11} = 2 \frac{C_{r11} \cdot C_{r22} - 2C_{r11}}{(C_{r11} - 2)(C_{r22} - 2)}$$
(3A-25)

$$\Delta_{22} = 2 \frac{C_{r11} \cdot C_{r22} - 2C_{r22}}{(C_{r11} - 2)(C_{r22} - 2)}$$
(3A-26)

$$\Delta_{33} = 4 \frac{C_{r11} \cdot C_{r22} - C_{r11} - C_{r22}}{(C_{r11} - 2)(C_{r22} - 2)}$$
(3A-27)

the values of C_{r11} , and C_{r22} are $2C_{r1}$,and $2C_{r2}$ respectively, where C_{r1} , and C_{r2} values are given before in chapter two

From Gauss's law, the following relation must hold, (see Fig. 2C-1) along the FinFET height:

$$C_{\text{ox}} \int_{z=-\text{ho}}^{\text{ho}} \left[V_{\text{GS}} - \phi_{ms} - \phi_{2D} \left(y = t_{o}, z \right) \right] dz = Q = \varepsilon_{\text{Si}} \int_{z=-\text{ho}}^{\text{ho}} \frac{\partial \phi_{2D}}{\partial y} \bigg|_{r=t_{o}} dz$$
 (3A-28)

From (3A-22) and (3A-24) into (3A-28), we write

L.H.S:

$$Q = C_{ox} \cdot H_{FIN} \cdot \left[V_{GS} - \phi_{ms} - \left(\phi_{so} + \frac{\alpha_{1s}}{12} \right) \right]$$

$$= C_{ox} \cdot H_{FIN} \cdot \left[\left(1 - \frac{\Delta_{11}}{12} \right) \left(V_{GS1} - \phi_{ms} \right) - \frac{\Delta_{22}}{12} \left(V_{GS2} - \phi_{ms} \right) - \phi_{so} \left(1 - \frac{\Delta_{33}}{12} \right) \right]$$
(3A-

29)

or normalized to H_{FIN},

$$Q_{n} = C_{ox} \cdot \left[\left(1 - \frac{\Delta_{11}}{12} \right) \left(V_{GS1} - \phi_{ms} \right) - \frac{\Delta_{22}}{12} \left(V_{GS2} - \phi_{ms} \right) - \phi_{so} \left(1 - \frac{\Delta_{33}}{12} \right) \right]$$
(3A-30)

R.H.S:

$$Q = \varepsilon_{Si} \int_{z=-ho}^{ho} \frac{\partial \phi_{2D}}{\partial y} \bigg|_{y=t_o} dz = \varepsilon_{Si} \int_{z=-ho}^{ho} E_{so}(z) dz$$
 (3A-31)

$$E_{so}(z) = \frac{\partial \phi_{2D}}{\partial y}\bigg|_{y=t_o} = \left[\frac{\partial \phi_{1D}(y)}{\partial y} + \frac{\partial \alpha_o(y)}{\partial y}z + \frac{\partial \alpha_1(y)}{\partial y}z^2\right]_{y=t_o}$$
(3A-32)

with,

$$\left. \frac{\partial \phi_{1D}(y)}{\partial y} \right|_{y=t_o} = 2V_T \cdot B_n \cdot \tan(B_n \cdot t_o) \tag{3A-33}$$

$$\left. \frac{\partial \alpha_o(y)}{\partial y} \right|_{y=t_o} = 2 \frac{C_{r11} - C_{r22}}{(C_{r11} - 2)(C_{r22} - 2)} \frac{\partial \phi_{1D}(y)}{\partial y} \right|_{y=t_o}$$
(3A-34)

$$\frac{\partial \alpha_1(y)}{\partial y}\bigg|_{y=t_*} = -\Delta_{33} \frac{\partial \phi_{1D}(y)}{\partial y}\bigg|_{y=t_*}$$
(3A-35)

from (3A-32) into (3A-31),

$$Q = \varepsilon_{\text{Si}} \cdot H_{FIN} \cdot \left(1 - \frac{\Delta_{33}}{12} \right) \cdot \frac{\partial \phi_{1D}(y)}{\partial y} \bigg|_{y=t}$$
 (3A-36)

or normalized to H_{FIN}

$$Q_{n} = \varepsilon_{\text{Si}} \cdot \left(1 - \frac{\Delta_{33}}{12}\right) \cdot \frac{\partial \phi_{1D}(y)}{\partial y}\bigg|_{y=t_{o}} = \varepsilon_{\text{Si}} \cdot \left(1 - \frac{\Delta_{33}}{12}\right) \cdot \left(2V_{t} \cdot B_{n} \cdot \tan(B_{n} \cdot t_{o})\right) \quad (3A-37)$$

Where B_n related to V_{GSI} , (given in chapter two).

Set,

$$Q_{n} = \varepsilon_{Si} \cdot \left(1 - \frac{\Delta_{33}}{12}\right) \cdot \left(2V_{T} \cdot \frac{C_{n}}{t_{o}} \cdot \tan(C_{n})\right) = 4C'_{si} \cdot V_{T} \cdot \left(1 - \frac{\Delta_{33}}{12}\right) \cdot C_{n} \cdot \tan(C_{n})$$

$$= Q_{o} \cdot C_{n} \cdot \tan(C_{n})$$
(3A-38)

Where
$$C'_{si} = \frac{\varepsilon_{Si}}{W_{FIN}}$$
, $Q_o = 4C'_{si} \cdot V_T \cdot \left(1 - \frac{\Delta_{33}}{12}\right)$, and $C_n = B_n \cdot t_o$.

And,

$$\frac{Q_n}{O} = C_n \cdot \tan(C_n) \tag{3A-39}$$

From (3A-39) into (3A-23), the surface potential can be written as

$$\begin{split} \phi_{so} &= \phi_{1D}(y)\big|_{y=t_o} = V_T \cdot \ln \left[\frac{B_n^2}{2 \cdot \delta} \sec^2\left(B_n \cdot t_o\right)\right] + V = V_T \cdot \ln \left[\frac{1}{\delta_n} \left(C_n^2 + C_n^2 \tan^2\left(C_n^2\right)\right)\right] + V \\ &= V_T \cdot \ln \left[\frac{1}{\delta_n} \left(C_n^2 + \left(\frac{Q}{Q_o}\right)^2\right)\right] + V \end{split}$$

$$3A-40$$

 C_n related to Q_n/Q_o from Eq. (3A-39). From Eq. (3A-40) into Eq. (3A-30),

$$Q_{n} = C_{ox} \left[\left(1 - \frac{\Delta_{11}}{12} \right) (V_{GS1} - \phi_{ms}) - \frac{\Delta_{22}}{12} (V_{GS2} - \phi_{ms}) - \left(V_{T} \cdot \ln \left[\frac{1}{\delta_{n}} \left(C_{n}^{2} + \left(\frac{Q_{n}}{Q_{o}} \right)^{2} \right) \right] + V \right) \left(1 - \frac{\Delta_{33}}{12} \right) \right]$$

$$= C_{ox}' \cdot \left[\Delta_{44} V_{GS1} - \Delta_{55} V_{GS2} - V_{T} \cdot \ln \left[C_{n}^{2} + \left(\frac{Q_{n}}{Q_{o}} \right)^{2} \right] - V - V_{0} \right] \rightarrow (3A - 41)$$

where
$$C_{ox}' = \left(1 - \frac{\Delta_{33}}{12}\right) C_{ox}$$
, $\Delta_{44} = \frac{\left(1 - \frac{\Delta_{11}}{12}\right)}{\left(1 - \frac{\Delta_{33}}{12}\right)} \approx 1$, and $\Delta_{55} = \frac{\left(\frac{\Delta_{22}}{12}\right)}{\left(1 - \frac{\Delta_{33}}{12}\right)} \approx 0$.

$$V_{0} = V_{T} \cdot \ln \left[\frac{1}{\delta_{n}} \right] = \phi_{ms} \cdot \left(\Delta_{44} - \Delta_{55} \right) + V_{T} \cdot \ln \left[8 \frac{\varepsilon_{si} \cdot V_{T}}{q n_{i} \cdot W_{FIN}^{2}} \right] \approx \phi_{ms} + V_{T} \cdot \ln \left[8 \frac{\varepsilon_{si} \cdot V_{t}}{q n_{i} \cdot W_{FIN}^{2}} \right]$$
 3A-42)

Note that for below threshold voltage $Q_n \le Q_o$

$$0 = \left[\Delta_{44} V_{GS1} - \Delta_{55} V_{GS2} - V_T \cdot \ln \left[C_n^2 \right] - V - V_0 \right]$$
 (3A-43)

From Eq. (3A-39), at $Q_n << Q_o$

$$C_n \cdot \tan(C_n) \approx C_n^2 = \frac{Q_n}{Q_0}$$
(3A-44)

For simplicity, drop *n*-subscript from Q to be

$$Q = Q_0 \exp\left(\frac{\left(\Delta_{44}V_{GS1} - \Delta_{55} \cdot V_{GS2} - V_0 - V\right)}{V_T}\right) \approx Q_0 \exp\left(\frac{\left(V_{GS1} - V_0 - V\right)}{V_T}\right)$$
(3A-45)

For strong inversion: the LHS of Eq. (3A-41), will be larger than both the logarithmic terms in the RHS, or

$$Q = C_{ox}' \cdot \left[\Delta_{44} (V_{GS1}) - \Delta_{55} (V_{GS2}) - V - V_0 \right] \approx C_{ox}' \cdot \left[V_{GS1} - V - V_0 \right]$$
(3A-46)

From Eq. (3A-41), the threshold voltage can written as,

$$V_{TH} = V_T \cdot \ln \left[C_n^2 + \left(\frac{Q}{Q_o} \right)^2 \right] + V_0$$
 (3A-47)

And below the threshold voltage will be,

$$V_{TH} = V_T \cdot \ln \left[\left(\frac{Q}{Q_o} \right)^2 + \left(\frac{Q}{Q_o} \right)^2 \right] + V_0 \approx -\infty$$
 (3A-48)

However for strong inversion $C_n^2 >> (Q_n/Q_o)^2$, and the threshold voltage can be written as,

$$V_{TH} \approx V_T \cdot \ln \left[C_n^2 \right] + V_0 = 2 \cdot V_T \cdot \ln \left[C_n \right] + V_0$$
 (3A-49)

Eq. (3A-47) cannot be used as an explicit model for the threshold voltage, however we can approximate Eq. (3A-47) to be,

$$V_{TH} = 2 \cdot V_T \cdot \ln[1 + C_n] + V_0 \tag{3A-50}$$

Applying Eq. (3A-7), we shall get the same formula like GAA MOSFET by replacing the cylindrical surface with $2H_{FIN}+W_{FIN}$, or,

$$I_{ds} = \frac{(2H_{FIN} + W_{FIN})}{L} \mu \left[2\frac{kT}{q} (Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{2C_{or}} + \frac{kT}{q} Q_0 \log \left[\frac{Q_d + Q_0}{Q_s + Q_0} \right] \right]$$
(3A-51)

$$Q = C_{ox}' \left(-\frac{2C_{ox}'V_{T}^{2}}{Q_{0}} + \sqrt{\frac{2C_{ox}'V_{T}^{2}}{Q_{0}}^{2} + 4V_{T}^{2}\log^{2}\left(1 + exp\left(\frac{V_{GS1} - V_{TH} + \Delta V_{TH} - V}{2V_{T}}\right)\right)}\right)$$
(3A-52)

and,

$$Q' = C_{ox}' \left(-\frac{2C_{ox}'V_T^2}{Q_0} + \sqrt{\frac{2C_{ox}'V_T^2}{Q_0}^2 + 4V_T^2 \log^2 \left(1 + \exp\left(\frac{V_{GS1} - V_0 - V}{2V_T}\right)\right)} \right)$$
(3A-53)

Where, V_0 is calculated from Eq. (3A-42), and V_{TH} from Eq. (3A-50), and ΔV_{TH} as it given in the last section. The differences between the GAA MOSFET model, and this general model, can written as

127

SCEs in undoped multiple gate MOS

- 1) The oxide capacitances for both devices are different..
- 2) The V_0 expression are different for both devices
- 3) The effects of the buried oxide and V_{GS2} are included in the threshold voltage calculations, and charge sheet calculations.
- 4) The device height also is included and taken into account
- 5) Threshold voltage calculations (Eq. (3A-49) have been done self consistently with the charge ratio Q_n/Q_o to find C_n)

We have tested the model by comparing the model as a square GAA MOSFET (i.e. $W_{FIN}=H_{FIN}$, $t_{ox}=t_{box}$, and $V_{GSI}=V_{GS2}$, and effective devices width will be the square area) with cylindrical GAA MOSFET, as shown in Fig. (3A-6a). However there are some difference at high V_{GS} value for cylindrical GAA MOSFET, and it is due to the fact that the oxide capacitance for cylindrical GAA MOSFET is bigger than the square GAA MOSFET, which leads more charge as shown from Eq. (3A-46), in strong inversion.

The threshold voltage correction, ΔV_{TH} , will be zero at low V_{GS1} voltage to produce a threshold voltage at low V_{GS} i.e., V_0 as shown in Fig. (3A-6b), and their values will be corrected at high V_{GS} , due to the approximation done in Eq. (3A-48).

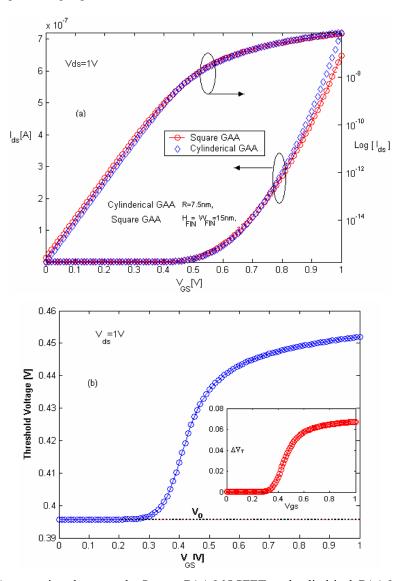


Fig. 3A-6 a) comparison between the Square GAA MOSFET, and cylindrical GAA MOSFET, by selecting R=7.5nm, $H_{FIN}=W_{FIN}=15$ nm, and $t_{ox}=t_b=1.5$ nm, and b) Threshold voltage correction

Fig. 3A-7 (a and b), shows the FinFET Ids- V_{GSI} (at V_{GS2} =0) at low and high V_{ds} value, the model is continuous from below-to-above the threshold voltage and from linear to saturation regime. The device has been simulated for a mobility of

450 cm²/V-sec, channel length L=10 µm, a silicon film width W_{FIN}=25 nm, H_{FIN}=65nm, a silicon oxide thickness $t_{ox}=1.5$ nm, box-oxide thickness $t_{b}=150$ nm and gate working function of 4.5 eV. The FinFET output characteristics were also shown in Fig. 3A-8.

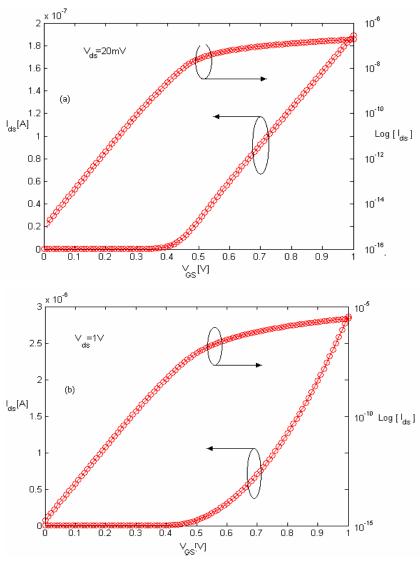


Fig. 3A-7. Transfer characteristic in linear and logarithmic scale at (a) V_{ds} =20mV (b) V_{ds} =1V

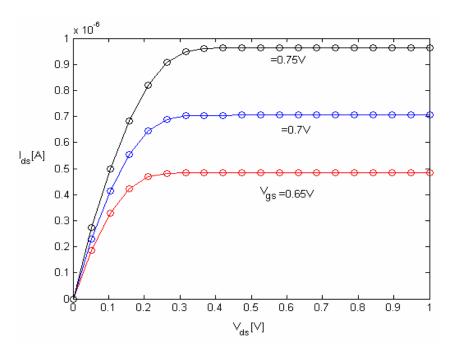


Fig. 3A-8. Output characteristics. at $H_{\text{FIN}}\!\!=\!\!65\text{nm},\,W_{\text{FIN}}\!\!=\!\!25\text{nm},$ and L=10micron

3A-4 DG MOSFET Model

There are a many models for the undoped long channel DG MOSFET devices which have been developed. We shall only mention the charge control model similar to the one developed before for both GAA MOSFET, and FinFET devices in the last sections.

Taur in [93], has introduced a long channel model for the inversion charge of undoped DG MOSFET devices based on a 1-D analytical solution of Poisson equation incorporating only the mobile charge term (referring to Fig. 3A-1, replacing r by y), or

$$\frac{d^2\phi}{dy^2} = \frac{q}{\varepsilon_{si}} n_i \cdot e^{\frac{\phi(y)}{V_T}}$$
 (3A-54)

After solving the last equation along the channel depth, the potential been solved as a function of the surface, ϕ_{so} , and centre potential, ϕ_0 , as

$$q\frac{\phi_{so} - \phi_o}{2KT} = -\ln\left[\cos\left(\sqrt{\frac{q^2}{2\varepsilon_{si}KT}}n_i\right)e^{\frac{\phi_o}{2V_T}}\frac{t_{si}}{2}\right]$$
(3A-55)

and,

$$\varepsilon_{ox} \frac{V_{GS} - \phi_{ms} - \phi_{so}}{t_{ox}} = \sqrt{2\varepsilon_{si} KT n_i \left(e^{\frac{\phi_{os}}{V_T}} - e^{\frac{\phi_0}{V_T}} \right)}$$
(3A-56)

From the last two equations it was able to calculate the charge density as shown in Fig. (3A-9).

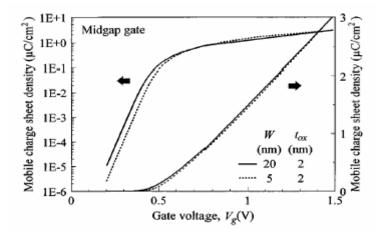


Fig. 3A-9 Sheet density of mobile charge[93]

Malobabic, et. al [132], have extended the Taur model by solving the surface potential in terms of Lambert function, and they found an explicit solution for the inversion charge model with a good agreement with that obtained numerically as shown in Fig. 3A-10 and Fig. 3A-11.

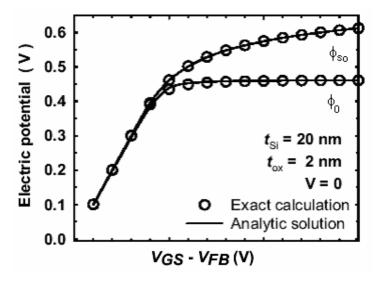


Fig. 3A-10 Potential at the channel surface and channel center

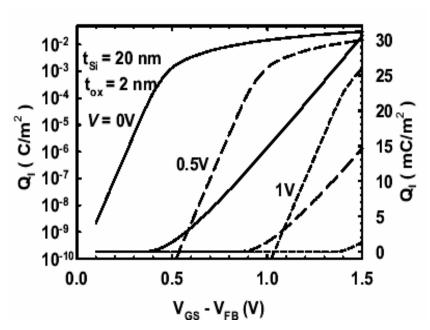


Fig. 3A-11 Carrier charge per unit area induced in the channel

After applying the current model given by He J. et. al., [133] (see Eq. (3A-57)) on his charge model, a good agreement have been obtained for the DC characteristics, as shown in Fig. 3A-12

$$I_{ds} = \frac{W}{L} \mu \left[\frac{Q_s^2 - Q_d^2}{4C_{ox}} + \frac{kT}{q} (Q_s + Q_d) \right]$$
 (3A-58)

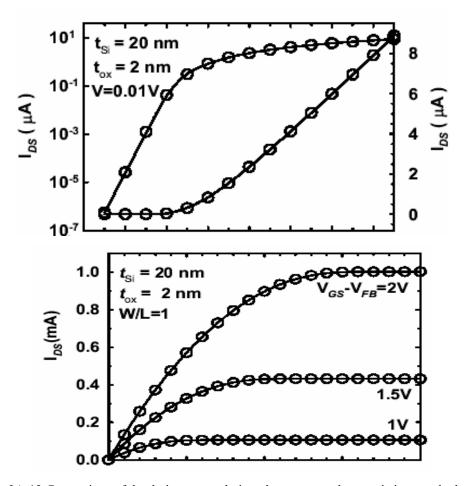


Fig. 3A-12 Comparison of the drain current-drain voltage output characteristics as calculated analytically [132] (continuous line) and from exact numerical calculations (symbols)

From the last sections, we can say that the charge control model has succeeded to develop an accurate current model for the undoped long channel multiple gate MOS devices. Moreover these models can be applied to the devices with short channel if we take consideration the SCEs parameters reported in chapter two. This can be done if we are able to couple the SCEs developed in chapter two with the drain current model.

(3B) Ballistic and Quasi Ballistic Transport in undoped Multiple Gate MOS Devices

3B-1 Introduction

CMOS technology has been proven as one of the most important achievements in modern engineering history. In less than 30 years, it has become the primary engine driving the world economy. The secret to the success is very simple: keep delivering more functionality with fewer resources. Device scaling makes this possible. For decades, progress in device scaling has followed an exponential curve: device density on a microprocessor doubles every three years. This has come to be known as Moore's law[140]. The roadmap projects a device gatelength down to ~30 nm around 2014. This forecast *promises* us another ten years of brightness. Scaling beyond 30 nm, however, can be much more difficult and different. Remember, we are quite close to the fundamental limits of semiconductor physics. How much further down can we go? It is hard to answer. Nevertheless, without doubt, we are facing numerous challenges, both practically and theoretically. Device simulation requires new theory and approaches to help us understand device physics and to design devices at the sub-30nm scale.

For device scaling, we basically try to balance two things: device functionality and device reliability. Both of them have to be maintained at a smaller dimensional size. To accomplish this, we need to suppress any dimension related effects or short channel effects (SCEs) as much as possible. SCEs include threshold voltage (V_{TH}) variations versus channel length, typically V_{TH} rolloff at shorter channel lengths. This effect is usually accompanied by degraded subthreshold swing (S), which causes difficulty in turning off a device. SCEs

ISBN: 978-84-690-8295-9 / D.L: T. 1514-2007

SCEs in undoped multiple gate MOS

also include the drain-induced barrier lowering (DIBL) effect. DIBL results in a drain voltage dependent V_{TH} , which complicates CMOS design at a circuit level. As a transistor scales, reliability concerns become more pronounced. In an ultrathin body multiple gate MOSFETs the SCEs can be minimized as explained in Chapter two.

It should be also noticed that high body doping is not needed here, so the bandto-band tunneling junction leakage is no longer a big concern.

Moreover, the use of ultra-thin bodies will result in reduced metallurgical junction perimeter, therefore low junction capacitance. The bodies are typically lightly doped, giving other advantages: 1) there is barely room for the FBE to come into play, 2) the V_{TH} variation due to dopant fluctuations can be eliminated, 3) closeto-ideal subthreshold swing (60 mV/dec) can be achieved, 4) severe mobility degradation due to ion scattering might be avoided.

Quantum effects (sub-band splitting) can become significant as the confinement of carriers becomes stronger within ultra-thin bodies, translating to sensitivity of V_{TH} to the body thickness. This fundamental physics effect poses an additional difficulty to control V_{TH} in ultra-thin bodes. (It is worthwhile to point out that this sub-band splitting effect will increase the band gap between lowest electron subband and highest hole subband, which may considerably suppress the band-toband tunneling leakage in ultra-thin silicon bodies.)

So, controlling of short-channel effects is more challenging with the progressive scaling of MOSFETs. In an attempt to contribute to this field, we propose a physical compact model of the ballistic DG-MOSFET operation, based on the Landauer transmission theory [141]. This theory has proved to be an excellent framework for describing mesoscopic transport [12-13]. In the Landauer approach, the current through a conductor is expressed in terms of the probability

136

that an electron can transmit through it. The net current of the ballistic MOSFET is obtained by substracting the drain to source transmitted current from the source to drain transmitted current. The electrons injected from the two electrodes see a potential barrier along the transport direction. We will consider a classical potential barrier with a shape governed by the gate and drain voltages. The transmission probabilities for the electrons crossing this barrier is one or zero depending whether the electron energy is above or below the barrier respectively. The use of a classical barrier to model MOSFET operation is a simplification, but it captures the basic mechanism controlling the current. This approach is valid as long as the source to drain tunnelling current does not dominate the total current. More detailed current-voltage characteristics could be obtained considering a quantum potential barrier.

137

3B-2 Ballistic and Quasi Ballistic Transport In DG and GAA MOSFETs

In Refs. [25],[134] a compact model for the nanoscale DG-MOSFET, assuming ballistic transport, has been presented. With this model the maximum expected performances can be obtained. However, backscattering affects the behaviour of multiple Gate MOSFET, even if they are nanoscale. Therefore, backscattering has to be included in a general model. Since the source is highly doped, a built in potential exists between the source end and the channel. This built in potential will be a barrier for the carriers. The carriers with energies less than this barrier value will be reflected towards the injecting reservoirs (source/drain), and the total current will be decreased due to these backward travelling carriers. The backscattering coefficient (r) has a value between zero and one, and is a function of both the critical length, ℓ , and the low field momentum relaxation length λ [28]. In this section, our objective is studying and modelling the backscattering effects on nanoscale DG-MOSFETs, using the flux method originally introduced by McKelvey [135].

Fig. 1 shows the cross section of the symmetrical DG-MOSFET considered in this work. In order to illustrate the behaviour of the compact model we have assumed a DG-MOSFET with gate length of 20 nm and the Si-SiO₂ interface parallel to (100) plane. The top and bottom gate oxide thickness are t_{ox} =1.5 nm, the Si body thickness t_{si} is taken as 1.5 nm. The same gate voltage V_{GS} is applied to both gates. The channel is undoped, the n^+ source and drain are highly doped, 10^{20} cm⁻³. A low field mobility of 120 cm⁻²/V-sec will be assumed in the channel. All calculations have been done at room temperature.

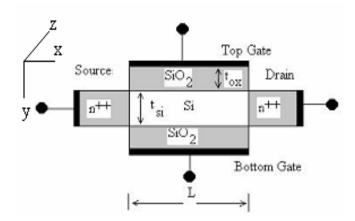


Fig. 3B-1 Cross section of the symmetrical DG-MOSFET considered in this section

Let us start with the current expression for a quantum wire MOSFET, given by [25]

$$I_{ds} = \frac{q}{L} \sum_{v} \sum_{k_{z}, k_{y}, k_{x} > 0} g_{v} (f_{s}(E) - f_{D}(E)) \left(\frac{\hbar k_{x}}{m_{x}^{v}} \right) T(E)$$
(3B-1)

In this equation, L is the channel length, corresponding to the transport direction (x-direction), and $\hbar k_x / m_x^{\nu}$ is the velocity of the electrons as they are injected from the contact with energy E. The two inner sums account for all the wave vectors injected by the electrodes and the outer sum for the three sets of silicon valleys (v=1,2,3) where electrons can lie, each one with a two-fold degeneracy ($g_v=2$); m_x^{ν} is the effective mass for the transport in the x-direction. If we suppose that the silicon-oxide interface orientation is <100>, then $m_x^1 = m_x^2 = m_T$, $m_x^3 = m_L$, where $m_T=0.19m_0$ and $m_L=0.91m_0$, being m_0 the free electron mass. The electron energy is related to k through the parabolic dispersion relation; $f_S(E)$ in Eq. (3B-1) is the

Fermi function for the source contact, which gives the probability that such an electron is injected from the contact; T(E) is the transmission coefficient for the electron; and $f_D(E)=f_S(E+qV_{ds})$ is the Fermi function at the drain contact. The electron energy E can be written as the sum of the component in the transport direction (E_x) and the component in the confining zy-plane (E_n^v) , with the subbindex n denoting discrete subbands (E_n^v) ; E_n^v ; E_n

$$I_{ds} = \frac{q}{\pi \hbar} \sum_{v} \sum_{n} g_{v} \left\{ \int_{E_{x}} (f_{s}(E) - f_{D}(E)) T(E) dE_{x} \right\},$$

$$(3B-2)$$

where we have made use of the parabolic dispersion relation for the E_x component

$$E_x = \frac{\hbar^2 k_x^2}{2m_x^{\vee}} \tag{3B-3}$$

The quantity $q/\pi\hbar$ is the current carried per occupied subband per unit energy, which is about 80 nA/meV. For ballistic transport T(E)=1 for $_{E>E_{n}^{v}}(x_{max})$, where x_{max} identifies the position of the nth-subband maximum energy (or x_{min} for the potential, V). We assume T(E)=0 otherwise. Eq. (3B-2) can be developed obtaining the following result:

$$I_{B} = \frac{qkT}{\pi\hbar} \sum_{v} \sum_{n} g_{v} \ln \left\{ \frac{1 + e^{\frac{E_{FS} - E_{n}^{v}(x_{\text{max}})}{kT}}}{1 + e^{\frac{E_{FD} - E_{n}^{v}(x_{\text{max}})}{kT}}} \right\}$$
(3B-4)

where I_B refers to the current under the ballistic transport hypothesis.

The ballistic off-current and on-current, are shown in Fig. 3B-2a. The I_{ds} - V_{ds} characteristic for a DG MOSFET shown in Fig. 3B-2b.

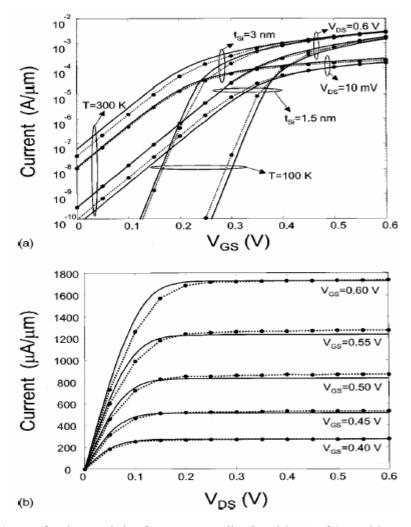


Fig. 3B-2. a) Transfer characteristic of a quantum well DG-MOSFET of 1.5 and 3 nm silicon film thickness working at 100 and 300 K; b) output characteristic at room temperature of the quantum well DG-MOSFET with a silicon film thickness of 1.5 nm. In the dotted line, we plot the nanoMOS simulations; in the solid line, the results from the compact model[25].

Eq. (3B-4) can be rewritten as a simple function of the forward and backward directed fluxes as:

$$I_R = I^+ - I^- = W \ q \ (F^+ - F^-)$$
 (3B-5)

where W, F^+ , and F^- are the channel width, the incident flux from the source, and the incident flux from the drain, respectively. A simple one-flux representation of channel transport in the nanoscale MOSFET is shown in Fig. 3B-3. This flux formulation will be useful for introducing the scattering, as we will explain later. The potential and charge distribution of the intrinsic DG structure has been reported by Taur [93]. The electrostatic analysis was only done in the vertical direction, but it serves to our purposes if we apply the results at the maximum energy point (x_{max}). At this special point, the potential and charge distributions are essentially controlled by the electric field perpendicular to the silicon-oxide interface provided that the short-channel-effects are not dominant. The potential along the vertical direction ($0 \le y \le t_{Si}/2$) is given by [93]

$$\frac{q(\phi(y) - \phi_0)}{2kT} = -\ln\left(\cos\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{Si}kT}}e^{q\phi_0/2kT}y\right)\right)$$
(3B-6)

where $\phi_0 = \phi(y=0)$ is the potential at the center of the silicon film, ε_{Si} is the permittivity of silicon and n_i is the intrinsic carrier density. The surface potential is $\phi_{so} = \phi(y=t_{Si}/2)$; ϕ_{so} is also related to V_{GS} and t_{ox} through the boundary condition at the silicon-oxide interface [93]

$$\varepsilon_{ox} \frac{V_{GS} - \phi_{ms} - \phi_{so}}{t_{ox}} = \varepsilon_{Si} \frac{d\phi}{dy} \bigg|_{y=t_{Si}/2} = Q/2 =$$

$$= \sqrt{2\varepsilon_{Si} kTn_i \left(e^{q\phi_{so}/kT} - e^{q\phi_0/kT} \right)}$$
(3B-7)

Here Q is the sheet density of mobile charge and ϕ_{ms} is the work-function difference between the gate electrode and intrinsic silicon:

$$\phi_{ms} = \phi_m - (\chi_{Si} + E_g / 2q) \tag{3B-8}$$

The GAA MOSFET model can be developed as reported by [25], with the following modifications:

1) the intrinsic carrier concentration which given as,

$$n_{i} = \frac{\sqrt{2kT}}{\pi\hbar} \sum_{v} \sum_{n} g_{v} \sqrt{m_{d}^{v}} \mathcal{J}_{-1/2} \left(\frac{E_{Fi} - E_{n}^{v}}{kT} \right). \tag{3B-9}$$

should divided by $(\pi \cdot t_{si}^2/4)$ instead of the area of the rectangular section $(W \cdot t_{Si})$;

 the separation between the bottom of the conduction band and the bottom of the subbands is given by the theory of the cylindrical quantum potential well or,

$$\Delta E_{n_r,n_\alpha}^v \approx \frac{2\hbar^2}{m_\perp^v t_{\rm Si}^2} \left\{ \left(n_r + \frac{1}{2} |n_\alpha| - \frac{1}{4} \right) \pi \right\}^2, \tag{3B-10}$$

3) the oxide capacitance per unit area for the cylindrical geometry should be used (see Sec. 3A)

where E_g is the gap energy for silicon (1.12 eV). Below the threshold voltage $V_{TH}\approx E_g/2q+\phi_{ms}$, the mobile charge is very small and $\phi_{so}\approx\phi_0\approx V_{GS}-\phi_{ms}$. In this case, the bands move as a whole because ϕ_{so} and ϕ_o closely follow V_{GS} . When the gate voltage is further increased above the threshold voltage, when $\phi_{so}\approx E_g/2q$, the right hand side of (3B-6) and (3B-7) are no longer negligible. Since the angle of the cosine function in (3B-6) cannot exceed $\pi/2$, ϕ_0 saturates to the maximum value

 $(kT/q)\ln(2\pi^2\varepsilon_{s_i}kT/q^2n_it_{s_i}^2)$. On the other hand, ϕ_{so} continues to increase slowly as governed by (3B-7) with the $\exp(q\phi_o/kT)$ term in the square root neglected. From (3B-7), the sheet density of mobile charge can be written as

$$Q = 2C_{ox} \left(V_{GS} - \phi_{mS} - \phi_{so} \right)$$
 (3B-11)

where ϕ_{so} is a function of V_{GS} that can be solved iteratively from (3B-7). The gate electrodes control the mobile charge (Q) at the virtual cathode (x_{max}) . This charge is provided by the source (Q⁺) and drain (Q⁻) reservoirs, by adjusting adequately the separation between E_{FS} and $E_n^v(x_{max})$:

$$Q = \sum_{v} \sum_{n} \left\{ Q^{+}(E_{FS} - E_{n}^{v}(x_{max})) + Q^{-}(E_{FD} - E_{n}^{v}(x_{max})) \right\}$$
(3B-12)

In equilibrium (V_{ds} =0), the k_x -distribution at x_{max} is symmetrical ($+k_x$ and $-k_x$ states are equally populated). When V_{ds} increases, the negative part of the k_x -distribution is progressively reduced because the barrier height for the $-k_x$ states increases with V_{ds} . To maintain Q constant, the Fermi level at the source must be pulled up to inject more forward travelling electrons into the channel to compensate the reduction of the negative flow. Eq. (3B-12) then relates V_{GS} and V_{ds} , with the distance between the Fermi level and the bottom of the energy subbands at the virtual cathode. It can be written in the form

$$Q = \frac{q}{W} \sum_{v} \sum_{n} g_{v} \int_{0}^{\infty} \frac{N_{1D}^{v}(E)}{2} (f_{S}(E) + f_{D}(E)) dE$$
 (3B-13)

Inserting the one-dimensional density of states into (3B-13) and after some algebraic manipulations we arrive to

$$Q = \frac{q\sqrt{2kT}}{2W\pi\hbar} \sum_{v} \sum_{n} g_{v} \sqrt{m_{d}^{v}} \left\{ \mathfrak{I}_{-1/2} \left(\frac{E_{FS} - E_{n}^{v}(x_{\text{max}})}{kT} \right) + \mathfrak{I}_{-1/2} \left(\frac{E_{FD} - E_{n}^{v}(x_{\text{max}})}{kT} \right) \right\}$$
(3B-14)

Or in the fluxes form, Eq. (3B-14) can be rewritten as:

$$Q = \frac{q}{v}(F^+ + F^-) \tag{3B-15}$$

where v is the average velocity of carriers crossing the plane x=0, and the velocities associated with the positive and negative directed fluxes are assumed identical [75].

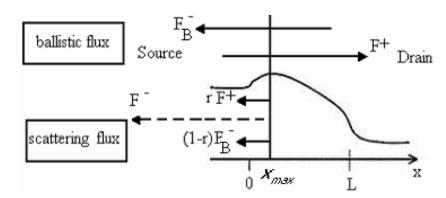


Fig. 3B-3. Simple one flux representation of channel transport in nanoscale MOSFETs.

In the presence of scattering, the negative directed flux (F^-) contains a component (rF^+) due to the backscattering of the positive directed flux injected from the drain and another component $(1-r)F_B^-$ corresponding to the fraction of the flux injected from the drain (F_B^-) that transmits towards the source. This can be clearly seen in Fig. 3B-3. By adding the source and drain related contributions, we find

$$F^{-} = rF^{+} + (1 - r)F_{B}^{-} \tag{3B-16}$$

By substracting the positive and negative directed fluxes, as in Eq. (3B-5), the current including scattering can be calculated as:

$$I = W \ q \ \left\{ F^{+} - rF^{+} - (1 - r)F_{B}^{-} \right\}$$

$$= W \ q \ (1 - r)(F^{+} - F^{-}) = (1 - r)I_{B}$$
(3B-17)

where I_B is the ballistic current given by Eq. (3B-5). The charges provided by the source (Q^+) and drain (Q^-) will also be modified due to the backscattering, to be:

$$Q = \frac{q}{v} \left\{ F^{+} + rF^{+} + (1 - r)F_{B}^{-} \right\} = (1 + r)Q^{+} + (1 - r)Q^{-}$$
(3B-18)

The backscattering coefficient r is related to the critical channel length ℓ and the low field momentum relaxation length λ according to Ref. [28] by means of:

$$r = \frac{\ell}{\ell + \lambda} \tag{3B-19}$$

The critical channel length ℓ is evaluated analytically in [75] as a function of the drain voltage,

$$\ell = L \left(\beta \frac{KT / q}{V_{ds}} \right)^{\alpha} \tag{3B-20}$$

where β is a fitting parameter, which should be greater than 1, and α can be estimated by solving the one dimensional Poisson's equation along the transport direction in two extreme cases: collision free (ballistic) and collision dominated (diffusive) transport in the channel. A single pair of β and α values are used in [75], and also in this work, i.e., β =1.18 and α =0.57.

The critical channel length which was introduced in Eq. (3B-20), is switched to L for V_{ds} </br>
kT/q, leading to discontinuous behavior of the I-V characteristics. In our model, to avoid discontinuities, we use the following interpolation function for the critical channel length (ℓ), which tends to the desired values at low and high drain voltage:

$$\ell' = \frac{\ell}{\left[1 + (\ell/L)^m\right]^{1/m}}$$
 (3B-21)

where m is a fitting parameter (~3). From Eq. (3B-21), at low values of ℓ ($\ell << L$, i.e., $V_{ds} >> kT/q$), $\ell' \approx \ell$ as it should, and at high values of ℓ ($\ell >> L$, i.e., $V_{ds} < kT/q$), $\ell' \approx L$ as it should. The low field momentum relaxation length λ can be obtained from the low field effective channel mobility [75],

$$\lambda = \left(\frac{2\mu}{v_T} \frac{kT}{q}\right) \frac{\{\mathfrak{I}_0(\eta)\}^2}{\mathfrak{I}_{-1}(\eta) \cdot \mathfrak{I}_{1/2}(\eta)}$$
(3B-22)

where η is the difference between the Fermi energy level and the maximum of the barrier and \mathfrak{I}_{-1} denotes the Fermi integral of order -1, which can be numerically computed by Blakemore's method [138]. μ is the low field mobility. The thermal velocity (nondegenerated), v_T , is given by:

$$v_T = \sqrt{\frac{2kT}{m_T \pi}} \tag{3B-23}$$

In Fig. 3B-4, the output characteristics of the DG-MOSFET on the presence of scattering are shown. The solid lines are calculated by Eq. (3B-17), and the symbols are the numerical 2-D NEGF simulations obtained with nanoMOS. Good agreement with nanoMOS numerical simulations has been found. We have observed that about 60% of the ballistic current is scattered, as mentioned in [139], and the reason is that the average velocity at the top of the barrier is well below the thermal injection limit. The cause of the nonsaturation of the current is that the average velocity at the top of the barrier does not saturate to the thermal velocity value, as shown in Fig. 3B-5.

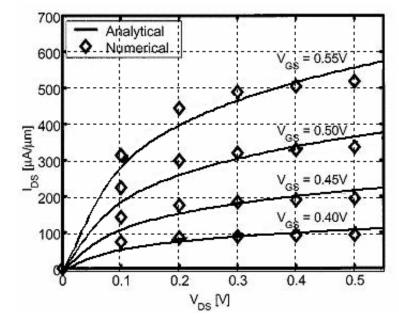


Fig. 3B-4. Comparison of the output characteristics of the modeled DG-MOSFET. The solid line results of our compact model, and the diamonds represents 2D numerical simulation of the same device.

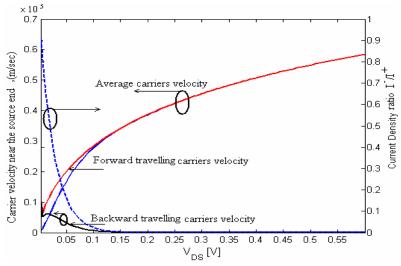


Fig. 3B-5. The bold solid lines are the total average velocity, backward travelling carrier velocity, and forward travelling carrier velocity. The ratio of the negative directed flux (Γ) respect to the positive directed flux (Γ) is also indicated.

Fig. 3B-5. shows the average velocity near the source end and its components (forward and backward travelling components). As the drain voltage, become greater than the thermal voltage, the average velocity will be dominated by the forward travelling carrier velocity, and the contribution of the backward travelling carrier velocity will be negligible. The reason for the vanishing backward travelling carrier velocity is the suppression of the backward directed flux at high drain voltage, as shown in Fig. 3B-5 (right side).

The predicted channel conductance does not tend to zero (see Fig. 3B-6), as in the ballistic case, because of the non-saturating electron velocity near the source end.

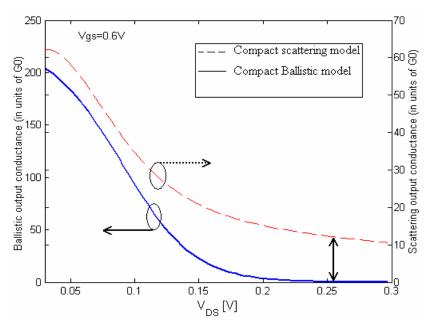


Fig. 3B-6 Channel conductance for the DG-MOSFET. The dotted line is the result from our compact scattering model ($r\neq 0$), and the solid line from the ballistic model (r=0). G_0 is the quantum conductance unit (= $q^2 / \pi \hbar$).

Fig. 3B-7 introduces a comparison between the transfer characteristics (I_{ds} versus V_{GS}) obtained with our proposed model (solid lines), and with the model presented by [75] (dotted lines). The characteristics are plotted for low (V_{ds} =0.05V) and higher (V_{ds} =0.55V) drain bias conditions. We demonstrate that our model can be used to describe both subthreshold and above threshold behavior. A discontinuity was observed in the model of [75] at the transition between below and above threshold, whereas our model does not suffer from this discontinuity.

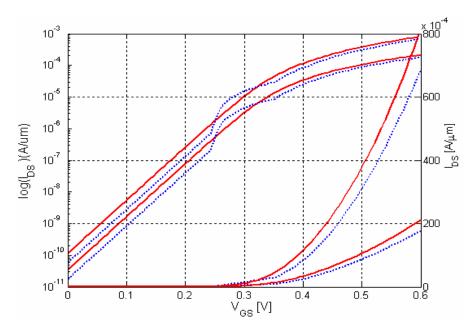


Fig. 3B-7. Comparison of the transfer characteristics between our model (solid lines) and the model presented in [75] (dotted lines). Plots in linear and log scales for low (V_{ds} =0.05V) and higher (V_{ds} =0.55V) drain biases.

3B-3 Quasi Ballistic Transport in undoped FinFET devices

As explained before, FinFET becomes attractive due to its quasi-planar structure, better immunity to SCEs, range of channel lengths, CMOS compatibility, good area efficiency compared to double gate structures and the possibility of using it with strained Si.

The complexity for developing a 3-D model for studying the DC characteristics of the FinFETs makes most of the researchers focusing on the numerical results to explain the devices performance, as done [145-147]. Even the models which developed to study the DC characteristics considered the FinFET as a Double Gate device neglecting the effects of the third gate benefits [148-150], and so on, the backscattering coefficient cannot be analytically developed.

So, we can say, the DC characteristics modeling of doped/undoped FinFET devices is still an open issue.

In this section we are focusing on the quasi ballistic transport of the undoped FinFET devices. We shall extract the backscattering coefficient from the device performance experimentally at different temperatures as it done before for MOSFET devices in [142-144].

From scattering theory in [75], drive current in saturation region can be expressed as,

$$I_{ds_sat} = W \cdot v_{inj} \cdot \left[\frac{1 - r_{sat}}{1 + r_{sat}} \right] \cdot C_{ox} \cdot \left(V_{GS} - V_{T,sat} \right)$$

However this model is valid for the conventional MOSFET, but no matter if we have used it for the FinFET devices, by considering W is the effective device width, i.e., $2H_{fin}+W_{fin}$. v_{ini} , r_{sat} and $V_{TH,sat}$ represent injection velocity,

backscattering ratio, and threshold voltage, respectively. The ratio r_{sat} is a function of the carrier mean free path (as shown in the last section), λ , and KT layer thickness, ℓ . From Eq. 3B-19, we can rewrite the backscattering coefficient as

$$r_{sat} = \frac{1}{1 + \lambda / \ell \Big|_{sat}} \tag{3B-24}$$

The $V_{TH,sat}$ is determined by the maximum transconductance method with the DIBL consideration (Fig. 3B-9).

The temperature-dependent analytic model is employed to extract the ratio using the following analytic expression:

$$\frac{\partial I_{ds_sat}}{\partial T} = I_{ds_sat} \left[\frac{1}{v_{inj}} \frac{\partial v_{inj}}{\partial T} + \frac{1 + r_{sat}}{1 - r_{sat}} \frac{\partial}{\partial T} \left(\frac{1 + r_{sat}}{1 - r_{sat}} \right) + \frac{1}{V_{GS} - V_{TH,sat}} \frac{\partial \left(V_{GS} - V_{TH,sat} \right)}{\partial T} \right]$$

$$= I_{ds_sat} \left[\frac{1}{2T} - \frac{\partial r_{sat}}{\partial T} \left(\frac{1}{1 + r_{sat}} + \frac{1}{1 - r_{sat}} \right) - \frac{\eta}{V_{GS} - V_{TH,sat}} \right]$$

$$= I_{ds_sat} \cdot \alpha$$
(3B-25)

where

$$\frac{\partial r_{sat}}{\partial T} = \left[2r_{sat} \cdot (1 - r_{sat})\right]/T \tag{3B-26}$$

and α can written as,

$$\alpha = \frac{1}{T} \left[\frac{1}{2} - \frac{4}{2 + \frac{\lambda}{\ell}} \right] - \frac{\eta}{V_{GS} - V_{TH,sat}}$$
(3B-27)

where α , η represent the temperature sensitivity of I_{ds-sat} and $V_{TH-sat.}$, i.e., $\alpha = (I_{ds-sat1} - I_{ds-sat2})/[(T_1 - T_2)]$, and $\eta = (V_{TH-sat1} - V_{TH-sat2})/(T_1 - T_2)$.

Experimentally we have increased the temperature from 20 to 125C°, and reported I_{ds} - V_{GS} curve as shown in Fig. 3B-8(a,b), from below to above threshold voltage,

at low and high drain-source voltage values. The $V_{TH,sat}$ is determined by the maximum transconductance curve shown in Fig. 3B-9. The extracted threshold voltage at low V_{ds} value is shown in Fig. 3B-10, From the last curves we calculated both α , and , η , which have been used to calculate the backscattering coefficient ratio λ/ℓ , and the backscattering coefficient r_{sat} , as shown in Fig. 3B-11. The last procedures have been repeated for a FinFET with different channel lengths, at fixed height (60nm), and width (25nm).

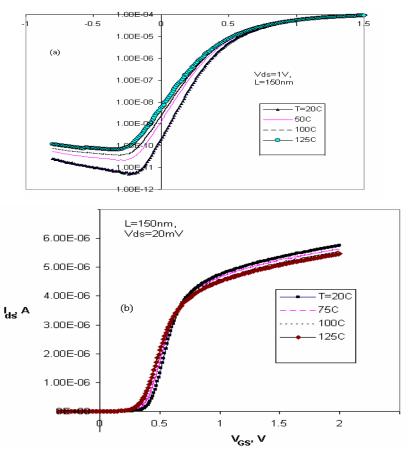


Fig. 3B-8 I_{ds} vs. V_{GS} at a) V_{ds} =1V, and b) V_{ds} =20mV. L=150nm, Hfin=60nm at different temperature values.

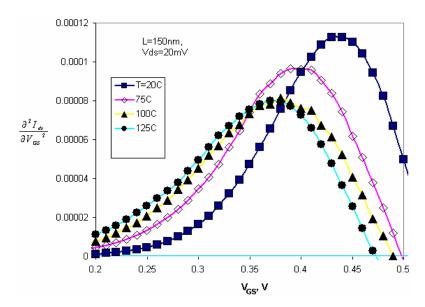


Fig. 3B-9 The second derivative method used for extracting threshold voltage. V_{ds} =20mV. L=150nm, Hfin=60nm at different temperature values.

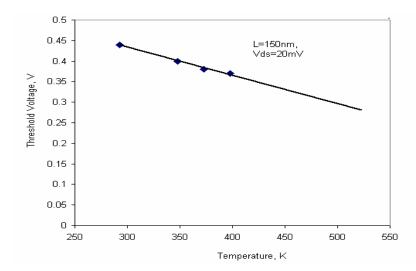


Fig. 3B-10 Extracted threshold voltage vs the temperature, symbols is the extracted values, and solid is the linear fitting approximation. V_{ds} =20mV. L=150nm, Hfin=60nm

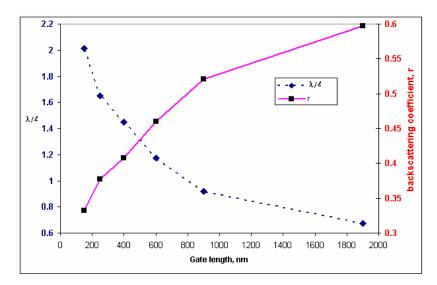


Fig. 3B-11Extracted backscattering coefficient vs. channel lengths. *Hfin=60nm*

We need to mention here that we have taken into account the effect of the series resistance, which extracted from I_{ds} - V_{ds} curves. Now, to account the amount of the scattering current, we set

$$\beta_{sat} = \left(\frac{1 - r_{sat}}{1 + r_{sat}}\right) \tag{3B-28}$$

Then, the total current can be written as,

$$I_{ds_with-scattering} = \beta_{sat} \cdot I_{ds_without-scattering}$$
 (3B-29)

As shown from Fig. 3B-12, we have found that more than 50% of the total current will be scattered due to the backscattering phenomena for channel length below 100nm, which is approximately the same result we have deduced analytically before for the DG MOSFETs, in the last section.

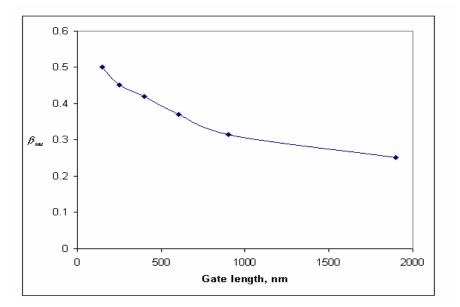


Fig. 3B-12 The backscattering current ratio vs. channel lengths. *Hfin=60nm*

With backscattering phenomena we have lost more than 50% of the total current for the modern devices, which are designed to obtain lengths below 100nm. The future work should try to minimize this ratio. There are many solutions for doing that. This work should focus on increasing the electron mobility by,

- 1) Using a strained Si layer which will increase the electron mobility and so on increasing the total current.
- 2) Using new materials like carbon or Ge which increases the drift current component.
- 3) Using different lattice orientations, and this may need more studying to get the best methods that give a higher mobility.

CHAPTER FOUR

Conclusions and recommendations for the future work

4-1 Summary

In this thesis we have studied the characteristics of the undoped multiple gate MOS devices.

We have introduced compact models for the Short Channel Effects (SCEs) for three multiple gate devices (Surrounding Gate All Around, Double Gate, and FinFET). The compact models for SCEs that are introduced through this thesis are:

- 1) Threshold voltage
- 2) Subthreshold swing
- 3) Threshold Voltage Roll-off
- 4) DIBL

After we have studied the last four SCEs effects we got a complete idea about the three device performances in the case of scaling down their dimensions. The last SCEs effects have been modeled based on solving the Poisson's equation with the mobile charge density. We did not introduce any fitting parameters to develop those models. The device electrostatics has been studied based on the device

158

SCEs in undoped multiple gate MOS

structures as: we consider 2D structures (like Double Gate MOSFETs), and 3D structures (like Gate All Around MOSFETs, and FinFETs). The models have been successfully validated with numerical simulation results and the experimental results that were done at the Microelectronics Laboratory, Université catholique de Louvain, Belgium, for channel lengths down to 30nm.

We have also proved that the devices with multiple gates have better performances than the devices with a single gate using our models. We have compared the performances of Double Gate (DG) and Surrounding Gate (SG) MOSFETs, and we have found that the Surrounding Gate MOS devices can provide the same performances as the Double Gate MOS devices, having a channel length longer by about 33% than the channel length in the Double Gate MOS devices.

Also, we have presented an analytical DC model for undoped multiple gate MOS devices. The model is based on a new unified charge control model developed for those devices, from which we derived a channel current expression in terms of the channel charge densities at the source and drain ends of the channel. The model becomes explicit by using appropriate expressions for the channel charge densities in terms of the applied voltages. The channel charge distribution in the silicon film is adequately accounted for in the charge control model. Good agreement is found between the new explicit model and the numerical exact solution obtained from the charge control model, which, in turn, was previously validated by comparison with 3D numerical simulations. Besides, the channel current expression presents an infinite order of continuity over all operating regimes, which makes the model very promising for circuit simulation.

The backscattering coefficient has also been studied through this thesis. We have studied the backscattering coefficient analytically in the Double Gate MOSFETs, and experimentally in the FinFETs. The analytical model has been introduced based on the McKelvey theory. The current model we have developed, is continuous from below to above threshold and from linear to saturation regions without suffering from discontinuities. A good agreement with 2-D numerical simulations (nanoMOS) was obtained. We have extracted the backscattering coefficient from the device performances experimentally based on the device current dependence with the temperature variations.

4-2 Recommendations for the future work

We have studied the SCEs for devices with channel thickness larger than 10nm, which allows us to exclude the quantum effects in our models. In the future we shall study the SCEs for the undoped multiple gate MOS devices with channel thickness thinner than 10nm, i.e. the quantum effects should be included. To improve the SCEs models that were developed through chapter two to includes the quantum effects, we do not need to start from the beginning. We should only correct the threshold charge values for the three devices[151]. After correcting the threshold charge values we can apply our SCEs models with the new corrected values.

Also in the future, we shall study the DC device characteristics for the devices with shorter lengths. Again, we shall not start from scratch. The basic idea will be to couple the DC model, introduced for the long channel devices in chapter three, with SCEs models that we developed in chapter two.

159

160

SCEs in undoped multiple gate MOS

After we have studied the backscattering coefficient and we have detected that the device lost more than 50% of its total current for the devices with channel lengths below 100nm, we should study the backscattering coeffcient for the devices with new materials like SiGe [152], or carbon. A lot of research has already been done for carbon nanotubes but still there are no suitable compact models for the backscattering for that device. Also, the strained materials are interesting to be used in Si multiple gate devices, such as FinFET. Compact modeling for those devices is still an open issue.

Appendix (2A-1)

Using (2A-8), (2A-10) and (2A-11)in Eq (2A-14), we get:

$$\nabla^{2} \phi_{2}(x, r) = \frac{q}{\varepsilon_{si}} n_{i} e^{\phi_{1}(x)/V_{T}} \left[e^{\phi_{2}(x, r)/V_{T}} - 1 \right]$$
(2a-1)

Making a Taylor series expansion of $e^{\phi_2(x,r)/V_T}$ up to the linear term we obtain (this approximation is valid if $\phi_2(x,r)/V_T$ is small enough):

$$\nabla^{2} \phi_{2}(x, r) = \frac{q}{\varepsilon_{si}} n_{i} e^{\phi_{1}(x)/V_{T}} \left[1 + \phi_{2}(x, r)/V_{T} - 1 \right]$$
(2a-2)

We finally get:

$$\nabla^2 \phi_2(x,r) = \frac{q}{\varepsilon_{si} \cdot V_T} n_i e^{\phi_1(x)/V_T} \phi_2(x,r)$$
 (2a-3)

where $\phi_1(x)$ is given in Eq.(2A-19), by applying the cylindrical gradient to the left hand side term of Eq.(2a-3) as:

$$\frac{1}{r}\frac{\partial}{\partial r}r\frac{\partial}{\partial r}(\phi_2(x,r)) + \frac{\partial^2}{\partial x}\phi_2(x,r) = \frac{q}{\varepsilon_{si} \cdot V_T} \eta_i e^{\phi_1(x)/V_T} \phi_2(x,r)$$
(2a-4)

Assuming that:

$$\phi_2(x,r) = f_1(x) \cdot f_2(r) \tag{2a-5}$$

substituting Eq.(2a-5) into Eq.(2a-4) and rearranging the appropriate function $f_n(x)$ with its derivative, we get:

$$\frac{f_2''}{f_2} + \frac{f_2'}{r \cdot f_2} + \frac{f_1''}{f_1} = \frac{q}{\varepsilon_{si} \cdot V_T} n_i e^{\phi_1(x)/V_T}$$
(2a-6)

Eq.(2a-4) can divided into two equations based on variables separation method to be:

$$\frac{f_1''}{f_1} = \frac{q}{\varepsilon_{si} \cdot V_T} n_i e^{\phi_1(x)/V_T} - \gamma^2$$
 (2a-7)

162

SCEs in undoped multiple gate MOS

and

$$\frac{f_2''}{f_2} + \frac{f_2'}{r \cdot f_2} = \gamma^2 \tag{2a-8}$$

where γ (=2B/L) as given by [92] is the separation factor (i.e. eigen value of Eq.(2a-8)).

Eq.(2a-8) has a general solution of form:

$$f_2(r) = C1 \cdot I_o(\gamma \cdot r) + C2 \cdot K_o(\gamma \cdot r)$$
(2a-9)

where K_0 is the zeroth order modified Bessel function of the second kind. Eq.(2a-9) can be written in terms of a new parameter η as:

$$f_2(r) = C1 \cdot I_0(2\eta \cdot r/t_{Si}) + C2 \cdot K_0(2\eta \cdot r/t_{Si})$$
(2a-10)

Where $\eta = \gamma/2 = B \cdot tsi/2 \cdot L$ and $0 \le r \le t_{Si}/2$. We can analyze the factor η due to the channel length and silicon thickness as:

$$\eta_{\min} \le \eta_{short} \le \eta_{\max}$$
(2a-11)

where η_{short} expresses the value for the short channel devices (<50nm), and η_{long} for long-channel devices. Since $B \approx 3$, and the minimum silicon thickness that can be considered is about 1.5nm (despite it is not practical case but we shall not exclude it to get a wide range model), we obtain η_{min} to be ≈ 0.1 . From the roadmap and the recommendation listed in ITRS report [79], and the fact that, as mentioned in [84-85], $[tsi/L]_{max} = 0.7$ and since the minimum expected channel length is 10nm (in 2014), we obtain that $\eta_{max} \approx 1$. Also, at very long channel lengths $\eta_{min} \rightarrow 0$. Therefore, Eq.(2a-1) can be modified to cover both short and long channel lengths as:

$$0 < \eta < 2 \tag{2a-12}$$

The last introduction about η and its range is important to refine Eq.(2a-10), and also to get an analytical model that may contribute for updating or comparing with that listed in ITRS report.

We will obtain analytical expressions of $f_1(x)$ and $f_2(r)$, from which, using (2a-5), $\phi_2(x)$ will be calculated.

Fig. (2a-1) shows the graphs of the different orders of the first modified Bessel function I_n .

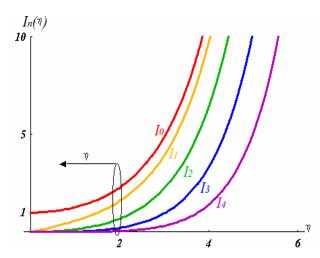


Fig. (2a-1) The first order modified Bessel function

Since the second order modified Bessel function K_0 , is defined as [86-91]:

$$K_{0}(2\eta r) = \begin{bmatrix} \left(\ln \frac{2\eta r}{2} + C \right) I_{O}(2\eta r/t_{Si}) - \frac{2}{1} I_{2}(2\eta r/t_{Si}) - \frac{2}{2} I_{4}(2\eta r/t_{Si}) - \frac{2}{2} I_{4$$

C being approximately 0.6, and for the given range of η , Eq.(2a-10) can be approximated to be:

$$f_2(r) = C1 \cdot I_0(2\eta \cdot r/t_{S_i}) - C2 \cdot \ln(\eta \cdot r/t_{S_i}) \cdot I0(2\eta \cdot r/t_{S_i})$$
(2a-14)

Because of the symmetry of the potential along the channel depth the constants C_1 , and C_2 must be equal and Eq.(2a-14) finally can written as:

$$f_2(r) = I0(2\eta \cdot r) \cdot \left[1 - \ln(\eta \cdot r)\right] \tag{2a-15}$$

The differential equation (2a-7) has an analytical solution for $f_1(x)$ [92]:

$$f_{1}(x) = \begin{cases} 4\sin(\psi \cdot x) - 2\cos(\psi \cdot x) \left[\tan(\frac{\gamma}{2} \cdot x_{m}) + \tan(\frac{\gamma}{2} (x - x_{m})) \right] \\ \tan(\frac{\gamma}{2} \cdot x_{m}) \cdot \tan(\frac{\gamma}{2} (x - x_{m})) \cdot \sin(\psi \cdot x) \end{cases}$$

$$\left\{ \frac{V_{GS} - \phi_{MS} - \phi_{om}}{\frac{C_{SI}}{C_{ox}} 2\eta \cdot I_{1}(\eta) + I_{0}(\eta)} \cdot \frac{\sin(\beta)}{3} \cdot \left[1 - \ln(\eta/2) \right] \right\}$$
(2a-16)

The threshold charge has been calculated numerically. Fig. (2a-2) shows the 3-D numerical values of the inversion charge density (cm⁻²) with log scale for various values of both silicon thickness and channel lengths against the gate-source voltage. From these simulations, the mobile sheet charge density at threshold was estimated to be about $\approx 1.2 \cdot 10^{12} \, cm^{-2}$. At approximately this value its dependence on V_{GS} stops being exponential, which is an indication of the starting of the turn-on condition. DESSIS-ISE software has been used to perform 3-D numerical simulations using the MOSFET structure described in Section 2. The Poisson and electron continuity equations are solved considering the drift-diffusion approach.

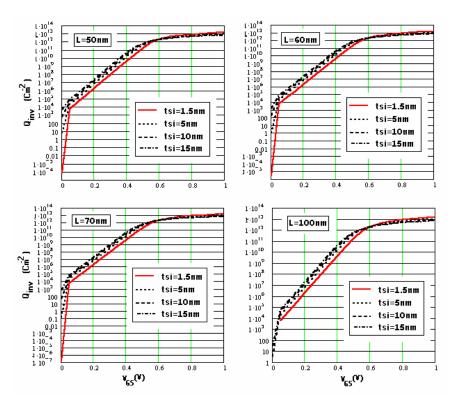


Fig. (2a-2) 3-D numerical simulation results (using DESSIS-ISE)of the mobile charge density (per unit area). We observe that the threshold charge is approximately $1.2 \cdot 10^{12}$ cm⁻²

Appendix (2A-2)

(A) SOLVING (2A-52),

$$\frac{1}{r}\frac{\partial}{\partial r}r\frac{\partial}{\partial r}\phi_1(x,r) + \frac{\partial^2}{\partial x^2}\phi_1(x,r) = 0$$
 Eq. (2A-52)

We use variable separation to find the solution of Eq.(2A-52), i.e,

$$\phi_1(x,r) = G(r) \cdot H(x) \tag{2a-17}$$

From (2a-17) into (2A-52), and re-arranging the equation to be:

$$\frac{G''(r)}{G(r)} + \frac{1}{r} \frac{G'(r)}{G(r)} = -\frac{H''(y)}{H(y)} = -\gamma^2$$
 (2a-18)

where γ is a separation factor, i.e. an eigen value. (2a-18), can written in two parts as:

$$\frac{G''(r)}{G(r)} + \frac{1}{r} \frac{G'(r)}{G(r)} + \gamma^2 = 0$$
 (2a-19)

And

$$\frac{H''(y)}{H(y)} - \gamma^2 = 0 {(2a-20)}$$

Eq. (2a-19) has a general solution in terms of the Bessel functions types J_0 , and K_0 as,

$$G(r) = A \cdot J_0(\gamma \cdot r) + B \cdot K_0(\gamma \cdot r)$$
(2a-21)

And Eq. (2a-20) has a general solution in terms of exponential functions as,

$$H(x) = C \cdot e^{\gamma \cdot x} + D \cdot e^{-\gamma \cdot x}$$
 (2a-22)

We normalize Eq. (2a-21) to channel radius:

$$G(r) = A \cdot J_0(\lambda \cdot r_n) + B \cdot K_0(\lambda \cdot r_n)$$
(2a-23)

where

$$\lambda = \gamma \cdot r_o \tag{2a-24}$$

Substituting Eq. (2a-24) into (2a-22), to obtain

$$H(x) = C \cdot e^{\lambda \frac{x}{r_o}} + D \cdot e^{-\lambda \frac{x}{r_o}}$$
 (2a-25)

Since the Bessel function K_0 is not defined at zero, we can consider that its coefficient is zero(for simplicity). Therefore, the potential can be written as:

$$\phi_1(r,x) = \left[(A \cdot C) \cdot e^{\lambda \frac{x}{r_0}} + (A \cdot D) \cdot e^{-\lambda \frac{x}{r_0}} \right] \cdot J_0(\lambda \cdot r_n)$$
(2a-26)

Or

167

SCEs in undoped multiple gate MOS

$$\phi_1(r,x) = \left[C_0 \cdot e^{\lambda \frac{x}{r_0}} + C_1 \cdot e^{-\lambda \frac{x}{r_0}} \right] \cdot J_0(\lambda \cdot r_n)$$
(2a-27)

From Eq. (2A-53) one obtains:

$$V_{bi} - \phi_0(r) = \sum_{m=1}^{\infty} [C_0 + C_1] \cdot J_0(\lambda_m \cdot r_n)$$
 (2a-28)

And from Eq. (2A-54) one obtains:

$$V_{ds} + V_{bi} - \phi_0(r) = \sum_{m=1}^{\infty} \left[C_0 \cdot e^{\lambda_m \frac{L}{r_0}} + C_1 \cdot e^{-\lambda_m \frac{L}{r_0}} \right] \cdot J_0(\lambda_m \cdot r_n)$$
 (2a-29)

Please notice that, from (2a-28), $V_{bi} - \phi_0(r)$ is the bessel Fourier coefficient of the function $[C_0 + C_1] \cdot J_0(\lambda \cdot r_n)$. $V_{ds} + V_{bi} - \phi_0(r)$ is the Bessel Fourier coefficient of

$$\left[C_0\cdot e^{\lambda\frac{L}{r_0}} + C_1\cdot e^{-\lambda\frac{L}{r_0}}\right] \cdot J_0(\lambda\cdot r_n) \ .$$

Drop subscript m, and n in Eq.2a-28, and Eq.2a-29 by considering,

$$\lambda = \frac{\lambda_m}{r_0} \tag{2a-30}$$

$$[C_0 + C_1] = \int_0^1 \frac{r}{N} \cdot [V_{bi} - \phi_0(r)] \cdot J_0(\lambda \cdot r) dr$$
 (2a-31)

$$\left[C_0 \cdot e^{\lambda \cdot L} + C_1 \cdot e^{-\lambda \cdot L}\right] = \int_0^1 \frac{r}{N} \cdot \left[V_{ds} + V_{bi} - \phi_0(r)\right] \cdot J_0(\lambda \cdot r) dr$$
(2a-32)

To calculate the eigen value, apply (2A-55) to (2a-27), or

$$G'(r_o) + C_r \cdot G(r_o) = 0$$
 (2a-33)

or

$$\lambda \frac{J_1(\lambda)}{J_0(\lambda)} = C_r \tag{2a-33}$$

Eq. (2a-33) is called "Robin Boundary condition" [73], [74], with norm, (i.e. N) is given as,

$$N^{2} = \frac{J_{0}(\lambda)^{2}}{2} \cdot \left[1 + \frac{(C_{r})^{2}}{\lambda^{2}} \right]$$
 (2a-34)

After solving 2a-31, and 2a-32 one obtains the coefficients C_0 , C_1 and hence the complete solution.

As given in the text of the chapter.

(B) THRESHOLD VOLTAGE CALCULATIONS

Use the same definition for the inversion charge as that introduced before in Eq. (2A-29), or

$$Q_{inv} = 2 \int_{0}^{r_0} n_i e^{\phi \left[x_{\min}, \frac{r}{r_0} \right] / V_T} dr$$
 (2a-73)

$$V_T \cdot \ln \left[\frac{Q_{inv}}{2n_i \cdot r_o} \right] = \phi_{\min}(r = r_c)$$
 (2a-74)

where r_c is the weak path or the conduction path, and from the symmetric of the device along the radius Eq. (2a-73) can solved at $r=r_c=0.5$, or

$$V_T \cdot \ln \left[\frac{Q_{inv}}{2n_i \cdot r_o} \right] = \phi_o \Big|_{r=0.5} + S_{ds} - S_{gs} \cdot \phi_{so}$$
(2a-75)

Since the channel is undoped with a negligible electric field across the device radius, we can consider,

$$V_{GS} - \phi_{ms} = \phi_o \Big|_{r=0.5} \approx \phi_{so} \tag{2a-76}$$

At the threshold voltage condition, $Q_{inv} \Rightarrow Q_{TH}$, and since we can write the threshold voltage as,

$$V_{TH} = \phi_{ms} + \frac{1}{1 - S_{gs}} \cdot \left(V_T \ln \left(\frac{Q_{TH}}{2n_i \cdot r_o} \right) - S_{ds} \right)$$
 (2a-77)

(C) SUBTHRESHOLD SWING CALCULATIONS

To find the subthreshold swing model, solve Eq. 2A-83 at the conduction path value, i.e. $r=r_c=0.5$, or

$$S = \frac{\partial V_{GS}}{\partial \log I_D} = \left[\frac{\partial \phi_{\min}(r = r_c)}{\partial V_{GS}}\right]^{-1} V_T \ln(10)$$
 (2a-78)

where,

$$\frac{\partial \phi_{\min}(r = r_c)}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}} \left[\phi_o \Big|_{r=0.5} + S_{ds} - S_{gs} \cdot \phi_{so} \right] \approx \left[1 - S_{gs} \right]$$
(2a-79)

From (2a-79) into (2a-78), we write the subthreshold swing as,

$$S = \frac{\partial V_{GS}}{\partial \log I_D} = \frac{1}{\left[1 - S_{gS}\right]} V_T \ln(10)$$
 (2a-80)

Appendix 2B

(A) SOLVING (2B-12)

$$\nabla^2 \phi_{1D}(y) = \frac{q}{\varepsilon_{si}} n$$
 Eq.(2B-12)

or

$$\frac{d^2\phi_{1D}}{dy^2} = \frac{q}{\varepsilon_{si}} n_i \cdot e^{\frac{\phi_{1D}(y)}{V_T}}$$
(2b-1)

Eq(2b-1) has a general solution of the form

$$\phi_{1D}(y) = V_T \cdot \ln \left[\frac{A}{2 \cdot \alpha} \left[1 + \tan^2 \left(\frac{\sqrt{A}}{2 \cdot V_T} y \right) \right] \right]$$
 (2b-2)

where

$$\alpha = \frac{q}{\varepsilon_{si} \cdot V_T} n_i \tag{2b-3}$$

Introduce a new constant B_n , as (normalized to tsi/2, where the device is symmetric along y-axis)

$$B_n = \frac{\sqrt{A}}{2 \cdot V_T} \cdot \frac{t_{si}}{2} \tag{2b-4}$$

$$\phi_{1D}(y) = V_T \cdot \ln \left[\frac{B_n}{2 \cdot \delta} \left[1 + \tan^2 \left(B_n y \right) \right] \right]$$
(2b-5)

2b-5 satisfies the boundary condition listed in Eq. 2B-14

$$\left. \frac{\partial \phi_{1D}}{\partial y} \right|_{y=0} = 0 \tag{Eq. 2B-14}$$

171

SCEs in undoped multiple gate MOS

2b-5 can be written as:

$$\phi_{1D}(y) = V_T \cdot \ln \left[\frac{B_n}{2 \cdot \delta} \sec^2 \left(B_n y_n \right) \right]$$
(2b-6)

Where B_n , can be calculated from:

$$\frac{\varepsilon_{ox}}{t_{ox}} \cdot \left[V_{GS} - \phi_{ms} - \phi_{1D} \left(y = t_o \right) \right] = -\varepsilon_{si} \cdot \frac{\partial \phi_{1D}}{\partial y} \bigg|_{y = t_o}$$
(2b-7)

(B) SOLVING 2D POTENTIAL DISTRIBUTION

Solving Eq.(2B-19)

$$\frac{\partial^2}{\partial y^2} \phi_{2D}(x, y) + \frac{\partial^2}{\partial x^2} \phi_{2D}(x, y) = 0$$
 (Eq. 2B-19)

Eq. 2B-19 boundary conditions related to the 1-D potential component, can be written as

$$\frac{\varepsilon_{ox}}{t_{ox}} \cdot \left[0 - \phi_{2D}(x, y = t_o) \right] = \varepsilon_{si} \cdot \frac{\partial \phi_{2D}(x, y)}{\partial y} \bigg|_{y = t_o}$$
(2b-8)

$$\frac{\varepsilon_{ox}}{t_{ox}} \cdot \left[0 - \phi_{2D}(x, y = -t_o) \right] = -\varepsilon_{si} \cdot \frac{\partial \phi_{2D}(x, y)}{\partial y} \bigg|_{y = -t_o}$$
(2b-9)

$$\phi_{2D}(0,y) = V_{bi} - \phi_{1D}(y)$$
 (2b-10)

$$\phi_{2D}(L, y) = V_{ds} + V_{bi} - \phi_{1D}(y)$$
(2b-11)

Set,

$$\phi_{2D}(x,y) = G(y) \cdot H(x) \tag{2b-12}$$

From 2b-12 into Eq.(2B-19), and rearrange the equation to be:

$$\frac{G''(y)}{G(y)} = -\frac{H''(x)}{H(x)} = -\gamma^2$$
 (2b-13)

172

SCEs in undoped multiple gate MOS

Where γ is separation factor, i.e. eigen value. Eq.2b-13, can written in two parts as:

$$\frac{G''(y)}{G(y)} + \gamma^2 = 0 {(2b-14)}$$

and

$$\frac{H''(x)}{H(x)} - \gamma^2 = 0 {(2b-15)}$$

Eq.2b-14 has a general as,

$$G(y) = A \cdot Cos(\gamma \cdot y) + B \cdot Sin(\gamma \cdot y)$$
 (2b-16)

And Eq.2b-15 has a general solution in term of exponential functions as,

$$H(x) = \left[C \cdot e^{\gamma \cdot (x - L)} + D \cdot e^{-\gamma \cdot x} \right]$$
 (2b-17)

We normalize Eq.(2b-16) to channel thickness, tsi/2, :

$$G(y) = A \cdot Cos(\lambda \cdot y_n) + B \cdot Sin(\lambda \cdot y_n)$$
(2b-18)

Where

$$\lambda = \gamma \cdot t_o \tag{2b-19}$$

substitute Eq.2b-19 into 2b-17, to obtain

$$H(x) = C \cdot e^{\lambda \frac{x - L}{t_o}} + D \cdot e^{-\lambda \frac{x}{t_o}}$$
(2b-20)

From 2b-16, and 2b-14 into 2b-8, or

$$\phi_{2D}(x, y) = G(y) \cdot H(x) = \left[A \cdot Cos(\lambda \cdot y_n) + B \cdot Sin(\lambda \cdot y_n) \right] \cdot \left[C \cdot e^{\lambda \frac{x - L}{t_o}} + D \cdot e^{-\lambda \frac{x}{t_o}} \right]$$
(2b-21)

drop subscript n from Eq. 2b-21, to be

$$\phi_{2D}(x,y) = \left[A \cdot Cos(\lambda \cdot y) + B \cdot Sin(\lambda \cdot y)\right] \cdot \left[C \cdot e^{\lambda \frac{x-L}{t_o}} + D \cdot e^{-\lambda \frac{x}{t_o}}\right]$$
(2b-22)

To find the constants of Eq. 2b-22, use the boundary conditions in Eq. 2b-8 and Eq. 2b-9, apply the two boundary conditions to 2b-22, or

$$\frac{\varepsilon_{ox}}{t_{ox}} \cdot [0 - G(y = t_o) \cdot H(x)] = \varepsilon_{si} \cdot G'(y = t_o) \cdot H(x)$$
(2b-23)

and

$$\frac{\varepsilon_{ox}}{t_{ox}} \cdot \left[0 - G(y = -t_o) \cdot H(x) \right] = \varepsilon_{si} \cdot G'(y = -t_o) \cdot H(x)$$
(2b-24)

From 2b-17, 2b-18, Chen et. al [78], has proved that the eigen value λ can be,

$$\lambda \Rightarrow \lambda_{\text{even}}$$
, and λ_{odd}

 λ_{odd} has a very small effect on Eq. 2b-22, which leads to a negligible *sin* coeffcient, and the effective value will be only the cosine component based on the even eigen i.e, λ_{even} with (see Fig. 2b-1),

$$\lambda_{even} \tan(\lambda_{even}) = C_r \tag{2b-25}$$

set,

$$\lambda \tan(\lambda) = C_r \tag{2b-26}$$

$$C_r = C_{ox} \frac{t_o}{\varepsilon_{si}}$$
 (2b-27)

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$
 (2b-28)

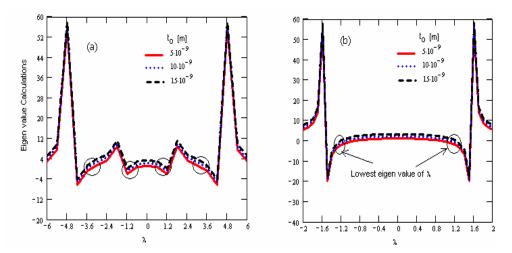


Fig. 2b-1 Eigen value calculations, a) series of eigen values, and b) lowest eigen value

So, we can write,

$$\phi(x,y) = \left[(A \cdot C) \cdot e^{\lambda \frac{x - L}{t_0}} + (A \cdot D) \cdot e^{-\lambda \frac{x}{t_0}} \right] \cdot Cos(\lambda \cdot y_n)$$
(2b-29)

or

$$\phi(x,y) = \left[C_0 \cdot e^{\lambda \frac{x-L}{t_0}} + C_1 \cdot e^{-\lambda \frac{x}{t_0}} \right] \cdot Cos(\lambda \cdot y_n)$$
(2b-30)

we can find C_0 , and C_I , by applying the boundary conditions at the source end, and drain end as (Eq. 2b-10, and Eq. 2b-11),

$$V_{bi} - \phi_{1D}(y) = \sum_{n=1}^{\infty} \left[C_0 \cdot e^{-\lambda \frac{L}{t_0}} + C_1 \right] \cdot Cos(\lambda \cdot y_n)$$

$$(2b-31)$$

$$V_{ds} + V_{bi} - \phi_{1D}(y) = \sum_{n=1}^{\infty} \left[C_0 + C_1 \cdot e^{-\lambda_n \frac{L}{r_0}} \right] \cdot Cos(\lambda \cdot y_n)$$
 (2b-32)

Please notice that from Eq.2b-30 that: $V_{bi} - \phi_0(y)$ is the Fourier coeffcient of

$$\left[C_0 \cdot e^{-\lambda \frac{L}{t_0}} + C_1\right]$$
, i.e., a_n . Where $V_{ds} + V_{bi} - \phi_0(y)$ is the Fourier coeffcient of

$$\left[C_0 + C_1 \cdot e^{-\lambda_n \frac{L}{r_0}}\right] \cdot Cos(\lambda \cdot y_n), \text{ i.e., } a_n. \text{Where,}$$

$$a_n = \int f(y)\cos(\lambda_y \cdot y)dy \tag{2b-33}$$

Applying Eq. 2b-33 to Eq. 2b-31 and Eq. 2b-33 (for more details about solving the fourier coefficient, see appendix 2C, for FinFET), we found C_0 , and C_1 , as,

$$C_0 = S_1 \cdot \left[V_{ds} + V_{bi} \cdot \left(1 - e^{-L\frac{\lambda}{t_o}} \right) \right] - S_2 \cdot \phi_{so}$$
 (2b-34)

$$C_{1} = S_{1} \cdot \left[V_{bi} \cdot \left(1 - e^{-L\frac{\lambda}{t_{o}}} \right) - V_{ds} \cdot e^{-L\frac{\lambda}{t_{o}}} \right] - S_{2} \cdot \phi_{so}$$
 (2b-35)

 S_1 , and S_2 depend on the device dimensions, and given by

$$S_{1} = \frac{4 \cdot \sin(\lambda)}{\left[2 \cdot \lambda + \sin(2 \cdot \lambda)\right] \cdot \left[1 - e^{\frac{-2L\frac{\lambda}{t_{o}}}{t_{o}}}\right]}$$
(2b-36)

$$S_{2} = \frac{4 \cdot \lambda \cdot \cos\left(\frac{\lambda}{2}\right) \cdot \left[1 - e^{-L\frac{\lambda}{t_{o}}}\right]}{\left[2 \cdot \lambda + \sin(2 \cdot \lambda)\right] \cdot \left[1 - e^{-2L\frac{\lambda}{t_{o}}}\right]}$$
(2b-37)

(C) VIRTUAL CATHODE VALUE AND THRESHOLD VOLTAGE

Since the virtual cathode value is the minimum potential value, i.e.:

$$\phi_{\min}(x, y) = \phi_{1D}(y) + \phi_{2D}(x, y)|_{\min}$$
 (2b-38)

where

$$\phi_{2D}(x,y)|_{\min} = \phi_{2D}(x_{\min},y)$$
 (2b-39)

Where x_{min} is the minimum position value and can be expressed as:

$$\left. \frac{\partial \phi_{2D}(x, y)}{\partial x} \right|_{x_{\min}} = 0 \tag{2b-40}$$

We found that

$$x_{\min} = \frac{L}{2} - \frac{t_0}{2 \cdot \lambda} \cdot \ln \left[\frac{C_1}{C_o} \right]$$
(2b-41)

$$x_{\min} = \frac{L}{2} - \frac{t_0}{2 \cdot \lambda} \cdot \ln \left[\frac{\left[V_{bi} \cdot \left(1 - e^{-L\frac{\lambda}{t_0}} \right) + V_{ds} \right] - \lambda \cdot \frac{\cos\left(\frac{\lambda}{2}\right)}{\sin(\lambda)} \left(1 - e^{-L\frac{\lambda}{t_0}} \right) \cdot \phi_{so}}{\left[V_{bi} \cdot \left(1 - e^{-L\frac{\lambda}{t_0}} \right) - V_{ds} \cdot e^{-L\frac{\lambda}{t_0}} \right] - \lambda \cdot \frac{\cos\left(\frac{\lambda}{2}\right)}{\sin(\lambda)} \left(1 - e^{-L\frac{\lambda}{t_0}} \right) \cdot \phi_{so}} \right]$$

$$(2b-42)$$

All the above parameters are defined before (see text).

The virtual cathode position vs. channel length, shown in fig.(2b-2)for different V_{ds} values.

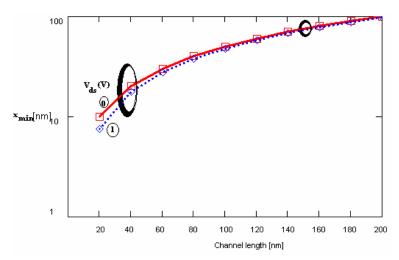


Fig. 2b-2 Virtual cathode position vs. channel length.

Since, the inversion charge can be calculated as,

$$Q_{inv} = 2 \int_{0}^{t_0} n_i e^{\phi[x_{\min}, y]/V_T} dy$$
 (2b-43)

where the last integration can be approximated as,

$$Q_{inv} = 2 \cdot t_o \cdot n_i e^{\phi[x_{\min}, y_c]/V_T}$$
 (2b-44)

where y_c , in Eq.(2b-44) accounting as the conduction path (or weak path), and from the device symmetry, Eq. (2b-43) can be approximated at the value of $y=y_c=t_o/2$ or $t_{si}/4$. This approximation of the conduction path agrees with the natural of the undoped channel, where the potential along the channel thickness is approximately flat which allow us to expected that the weak path can be at any point from center to the surface unlike the doped devices. So we can write Eq. (2b-44), as

$$V_T \cdot \ln \left[\frac{Q_{inv}}{2n_i \cdot t_o} \right] = \phi_{1D} \Big|_{y = y_c = 0.5} + S_{ds} - S_{gs} \cdot \phi_{so}$$
 (2b-45)

$$S_{ds} = 2 \cdot S_1 \cdot \cos\left(\frac{\lambda}{2}\right) \cdot e^{-L\frac{\lambda}{t_0}} \left[V_{ds} \cdot \sinh\left(x_{\min}\frac{\lambda}{t_0}\right) + 2 \cdot V_{bi} \cdot \sinh\left(\frac{L}{2}\frac{\lambda}{t_0}\right) \cdot \cosh\left(\left[x_{\min}-\frac{L}{2}\right]\frac{\lambda}{t_0}\right) \right]$$
(2b-46)

And,

$$S_{gs} = 2 \cdot S_2 \cdot \cos\left(\frac{\lambda}{2}\right) \cdot e^{-\frac{L}{2}\frac{\lambda}{t_0}} \cdot \cosh\left[\left(x_{\min} - \frac{L}{2}\right)\frac{\lambda}{t_0}\right]$$
 (2b-47)

$$\phi_{1D}|_{v=v_{-}=0.5} \approx \phi_{1D}|_{v=1} = \phi_{so}$$
 (2b-48)

or

$$\phi_{1D}|_{y=y_c=0.5} = \left(\frac{V_T \cdot \ln\left[\frac{Q_{inv}}{2n_i \cdot t_o}\right] - S_{ds}}{1 - S_{gs}}\right)$$
 (2b-49)

since the undoped devices leads to a negligible electric field along the devices thickness, or

$$V_{GS} - \phi_{ms} - \phi_{1D}|_{v=0.5} = 0 {(2b-50)}$$

or

$$V_{GS} - \phi_{ms} = \phi_{1D}|_{v=0.5} \tag{2b-51}$$

into Eq.(2b-50),

$$V_{GS} - \phi_{ms} = \phi_{1D}|_{y=0.5} = \left(\frac{V_T \cdot \ln\left[\frac{Q_{inv}}{2n_i \cdot t_o}\right] - S_{ds}}{1 - S_{gs}}\right)$$
(2b-52)

At which the inversion charge reaches to its threshold value we can rewrite Eq.(2b-52), as

$$V_{TH} - \phi_{ms} = \left(\frac{V_T \cdot \ln\left[\frac{Q_{TH}}{2n_i \cdot t_o}\right] - S_{ds}}{1 - S_{gs}}\right)$$

$$(2b-53)$$

or.

$$V_{TH} = \phi_{ms} + \left(\frac{V_T \cdot \ln\left[\frac{Q_{TH}}{2n_i \cdot t_o}\right] - S_{ds}}{1 - S_{gs}}\right)$$

$$(2b-54)$$

At very long channel device both S_{ds} , and S_{gs} goes to zero,

$$V_{TH} = \phi_{ms} + \left(V_T \cdot \ln \left[\frac{Q_{TH}}{2n_i \cdot t_o}\right]\right)$$
 (2b-55)

Eq. 2b-54 and Eq. 2b-55 are accounting as the threshold voltage for both short and long channel DG MOSFET device.

(D) SUBTHRESHOLD SWING

To find an expression for the subthreshold swing, apply

$$S = \frac{\partial V_{GS}}{\partial \log I_D} = \begin{bmatrix} \int_{y=0}^{t_o} n_m(y) \frac{\partial \phi_{\min}}{\partial V_{GS}} dy \\ \int_{y=0}^{t_o} n_m(y) dr \end{bmatrix}^{-1} V_T \ln(10)$$
 (2b-56)

$$S = \frac{\partial V_{GS}}{\partial \log I_D} \approx \left[\frac{n_m (y = y_c) \cdot \frac{\partial \phi_{\min}}{\partial V_{GS}}}{n_m (y = y_c)} \right]^{-1} V_T \ln(10)$$
(2b-57)

$$S \approx \left[\frac{\partial \phi_{\min}}{\partial V_{GS}} \right]^{-1} V_T \ln(10) \tag{2b-58}$$

From Eq. (2b-45), we can write

$$\frac{\partial \phi_{\min}}{\partial V_{GS}} \approx 1 - S_{gs} \tag{2b-59}$$

or,

$$S \approx \frac{1000}{\left[1 - S_{gs}\right]} \cdot V_T \ln(10) \Rightarrow \left[mV / Dec\right]$$
 (2b-60)

Appendix 2-C

3-D Poisson's Equation solving procedures

We define the oxide capacitances as

$$C_{oxo} = \frac{\varepsilon_{ox}}{t_{ox}}$$
 (2c-1)

$$C_{ox1} = \frac{\varepsilon_{ox}}{t_{ox1}}$$
 (2c-2)

$$C_{ox2} = \frac{\varepsilon_{ox}}{t_b} \tag{2c-3}$$

We define the oxide capacitance to Si- capacitances ratio, as

$$C_{ro} = C_{ox1} \frac{t_o}{\varepsilon_{si}} \tag{2c-4}$$

$$C_{r1} = C_{ox1} \frac{h_o}{\varepsilon_{si}}$$
 (2c-5)

$$C_{r2} = C_{ox2} \frac{h_o}{\varepsilon_{si}} \tag{2c-6}$$

$$\Delta = \frac{1 - \frac{2}{C_{r1}}}{1 - \frac{2}{C_{r2}}} \tag{2c-7}$$

$$\Delta 1 = \frac{1 - \frac{1}{C_{r1}}}{1 - \frac{1}{C_{r2}}} \tag{2c-8}$$

(A) THE 1D POTENTIAL SOLUTION (NORMALIZED TO FIN WIDTH)

$$\frac{d^2\phi_{1D}}{dy^2} = \frac{q}{\varepsilon_{si}} n_i \cdot e^{\frac{\phi_{1D}(y)}{V_T}}$$
 (2c-9)

$$\phi_{1D}(y) = V_T \cdot \ln \left[\frac{B_n^2}{2 \cdot \delta} \sec^2 \left(B_n \cdot y \right) \right]$$
(2c-10)

Where B_n , can be calculated from

$$C_{oxo} \cdot \left[V_{GS} - \phi_{ms} - \phi_{1D} \left(y = t_o \right) \right] = \varepsilon_{si} \cdot \frac{\partial \phi_{1D}}{\partial y} \bigg|_{y=1}$$
(2c-11)

$$\delta = \frac{q}{\varepsilon_{si} \cdot V_T} n_i \cdot t_o^2 \tag{2c-12}$$

$$\phi_{2D}(y,z) = \phi_{1D}(y) + \alpha_o(y) \cdot z + \alpha_1(y) \cdot z^2$$
(2c-13)

using the boundary condition in Eq. (2C-13), and Eq. (2C-14), or

$$C_{ox1} \cdot \left[V_{GS1} - \phi_{ms} - \phi_{2D}(y, z = 1) \right] = -\varepsilon_{Si} \frac{\partial \phi_{2D}(y, z)}{\partial z} \bigg|_{z=1}$$
 Eq.(2C-13)

$$C_{ox2} \cdot \left[V_{GS2} - \phi_{ms} - \phi_{2D}(y, z = -1) \right] = \varepsilon_{Si} \frac{\partial \phi_{2D}(y, z)}{\partial z} \bigg|_{z = -1}$$
Eq.(2C-14)

We found that,

$$\alpha_{o}(y) = \frac{\left[\left(V_{GS1} - \phi_{ms} \right) - \phi_{1D}(y) \right] - \Delta \cdot \left(\left(V_{GS2} - \phi_{ms} \right) - \phi_{1D}(y) \right)}{\left(1 - \frac{1}{C_{r1}} \right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}} \right)}$$
(2c-14)

SCEs in undoped multiple gate MOS

$$\alpha_{1}(y) = \frac{\left[\left(V_{GS2} - \phi_{ms} \right) - \phi_{1D}(y) \right] + \alpha_{o}(y) \cdot \left(1 - \frac{1}{C_{r2}} \right)}{\left(1 - \frac{2}{C_{r2}} \right)}$$
(2c-15)

(B) 3-D ELECTROSTATIC POTENTIAL SOLUTION

The 3-D potential component, is harder to obtain than the other two components.

We set,
$$\phi_{3D}(x, y, z) = f(x) \cdot g(y) \cdot h(z)$$
 (2c-16)

from Eq. (2c-16), into Laplace Equation in (20), we get

$$\frac{f(x)''}{f(x)} + \frac{g(y)''}{g(y)} + \frac{h(z)''}{h(z)} = 0$$
 (2c-17)

by using the variable separation method we can separate f(x),g(y), and h(z), as

$$\frac{g(y)''}{g(y)} + \gamma_y^2 = 0 {(2c-18)}$$

$$\frac{h(z)''}{h(z)} + \gamma_z^2 = 0 {(2c-19)}$$

$$\frac{f(x)''}{f(x)} - \lambda_x^2 = 0 {(2c-19)}$$

where γ_x , γ_y , and γ_z are separation variables or eigen values, with

$$\gamma_{v}^{2} + \gamma_{z}^{2} - \gamma_{x}^{2} = 0 \tag{2c-20}$$

and

$$\lambda_x = \sqrt{\gamma_y^2 + \gamma_z^2} \tag{2c-21}$$

The general solution for f(x), g(y) and h(z) found as,

$$g(y) = A_1 \cdot \cos(\gamma_y \cdot y) + B_1 \cdot \sin(\gamma_y \cdot y)$$
 (2c-22)

SCEs in undoped multiple gate MOS

$$f(x) = A_2 \cdot e^{\lambda_x \cdot (L - x)} + B_2 \cdot e^{-\lambda_x \cdot x}$$
(2c-23)

$$h(z) = A_3 \cdot \cos(\gamma_z \cdot z) + B_3 \cdot \sin(\gamma_z \cdot z) \tag{2c-24}$$

Since we have proved before from DG MOSFET analysis that g(y) can written as,

$$g(y) = A_1 \cdot \cos(\gamma_y \cdot y) \tag{2c-25}$$

From Eq.(2c-16) we can write,

$$\phi_{3D}(x,y,z) = \left(A_2 \cdot e^{\lambda_x \cdot (L-x)} + B_2 \cdot e^{-\lambda_x \cdot x}\right) \cdot \left(A_1 \cdot \cos(\gamma_y \cdot y)\right) \cdot \left(A_3 \cdot \cos(\gamma_z \cdot z) + B_3 \cdot \sin(\gamma_z \cdot z)\right) (2c-26)$$

Multiply A_1 in the whole parts, and rename the constants again to be as,

$$\phi_{3D}(x,y,z) = \cos(\gamma_{y} \cdot y) \cdot \left(A \cdot e^{\lambda_{x} \cdot (L-x)} + B \cdot e^{-\lambda_{x} \cdot x}\right) \cdot \left(C \cdot \cos(\gamma_{z} \cdot z) + D \cdot \sin(\gamma_{z} \cdot z)\right) \quad (2c-27)$$

For the 3D-Potential component we have 5-boundary conditions and are related to the main boundary condition, or,

$$C_{ox1} \cdot \left[0 - \phi_{3D}(x, y, z = h_o)\right] = -\varepsilon_{Si} \frac{\partial \phi_{3D}(x, y, z)}{\partial z} \bigg|_{z = h_0}$$
(Eq.21)

$$C_{ox2} \cdot \left[0 - \phi_{3D}(x, y, z = -h_o)\right] = \varepsilon_{Si} \frac{\partial \phi_{3D}(x, y, z)}{\partial z} \bigg|_{z = -h_o}$$
(Eq.22)

$$C_{oxo} \cdot \left[0 - \phi_{3D}(x, y = t_o, z)\right] = -\varepsilon_{si} \cdot \frac{\partial \phi_{3D}(x, y, z)}{\partial y}\bigg|_{y = t_o}$$
(Eq.2C-22')

$$\phi_{3D}(0, y, z)|_{Source-end} = V_{bi} - \phi_{2D}(y, z)$$
(Eq.2C-23)

$$\phi_{3D}(L, y, z)|_{Drain-end} = V_{ds} + V_{bi} - \phi_{2D}(y, z)$$
(Eq.2C-24)

To find the eigen values we should use the boundary conditions in Eqs. (21, 22 and 22'), as

(B.C.1) Top gate Boundary condition: apply Eq.(21) into Eq. (2c-27),

$$[0 - f(x) \cdot g(y) \cdot h(z = h_o)] = -\frac{h_o}{C_{r_1}} \cdot [f(x) \cdot g(y) \cdot h'(z = h_o)]$$
 (2c-28)

$$C_{r1} - h_o \cdot \frac{h'(z)}{h(z)} = 0$$
 (2c-29)

where, from Eq.(2c-27)

$$h(z) = C \cdot \cos(\gamma_z \cdot z) + D \cdot \sin(\gamma_z \cdot z) \tag{2c-30}$$

$$h'(z) = -\lambda_z \cdot C \cdot \cos(\gamma_z \cdot z) + \lambda_z \cdot D \cdot \sin(\gamma_z \cdot z)$$
 (2c-31)

Substitute from Eq.(2c-30) and Eq.(2c-31), into Eq.(2c-29),

$$C_{r1} - \gamma_{zo} \cdot h_o \frac{1 - R \cdot \tan(\gamma_{zo} \cdot h_o)}{R + \tan(\gamma_{zo} \cdot h_o)} = 0$$
(2c-32)

where γ_{zo} is related to the top-gate eigen value

or normalized to h_o ,

$$F_{zo} = C_{r1} - \lambda_{zo} \frac{1 - R \cdot \tan(\lambda_{zo})}{R + \tan(\lambda_{zo})} = 0 \quad , \quad \lambda_{zo} = \gamma_{zo} \cdot h_o$$
 (2c-33)

(B.C.2) Bottom gate Boundary condition(at Buried oxide): apply Eq.(21) into Eq. (2c-27),

$$C_{r2} + \gamma_{z1} \cdot h_o \frac{1 + R \cdot \tan(\gamma_{z1} \cdot h_o)}{R - \tan(\gamma_{z1} \cdot h_o)} = 0$$
 (2c-34)

where γ_{z1} is related to the buttom-gate eigen value

or normalized to h_o ,

$$F_{z1} = C_{r2} + \lambda_{z1} \frac{1 + R \cdot \tan(\lambda_{z1})}{R - \tan(\lambda_{z1})} = 0 , \lambda_{z1} = \gamma_{z1} \cdot h_o$$
 (2c-35)

where,

$$R = \frac{C}{D} = \frac{B \cdot C}{B \cdot D} = \frac{C'}{D'} = \frac{Eq.(C - 57)}{Eq.(C - 58)}$$
 (2c-36)

(B.C.3) Right/Left gate Boundary condition: apply Eq.(22 ') into Eq. (2c-27),

$$C_{oxo} \cdot \left[0 - \phi_{3D}(x, y = t_o, z) \right] = -\varepsilon_{si} \cdot \frac{\partial \phi_{3D}(x, y, z)}{\partial y} \bigg|_{y = t_o}$$

$$(2c-37)$$

$$C_{ro} - \gamma_y \cdot t_o \cdot \tan(\gamma_y \cdot t_o) = 0 \tag{2c-38}$$

normalized to to,

$$F_{yo} = C_{ro} - \lambda_y \cdot \tan(\lambda_y) = 0, \qquad \lambda_y = \gamma_y \cdot t_o$$
 (2c-39)

The eigen values calculations is shown in Fig. 2c-1.

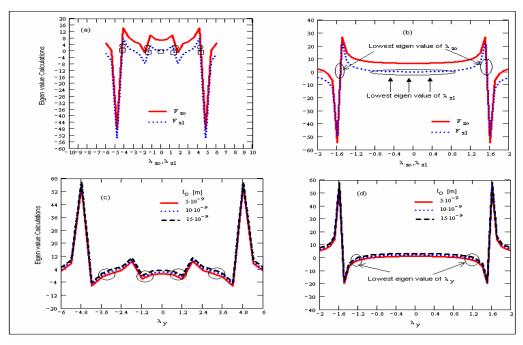


Fig. 2c-1 The eigen values calculation, where the right sides (b, and d) explore the values of the lowest eigen values that were used for calculating the potential, and satisfy Eq. 2C-19.

(B.C.4) Source end Boundary condition: apply Eq.(2C-23) into Eq. (2c-27),

$$V_{bi} - \phi_{2D}(y, z) = \sum_{n = -\infty}^{\infty} \sum_{m = -\infty}^{\infty} \left(A \cdot e^{\lambda_x \cdot (L - 0)} + B \cdot e^{-\lambda_x \cdot 0} \right) \cdot \cos(\lambda_{y, n} \cdot y) \cdot \left(C \cdot \cos(\lambda_{z, m} \cdot z) + D \cdot \sin(\lambda_{z, m} \cdot z) \right) \quad (2c-40)$$

we multiply both sides by $sin(\lambda_z z)$ and integrate over the Fin height,

$$\int_{z} \left[V_{bi} - \phi_{2D}(y, z) \right] sin(\lambda_{z} \cdot z) dz = \int_{z} \sum_{n = -\infty}^{\infty} \sum_{m = -\infty}^{\infty} \left(A \cdot e^{\lambda_{z} \cdot (L - 0)} + B \cdot e^{-\lambda_{x} \cdot 0} \right) \cdot \cos(\lambda_{y, n} \cdot y) \cdot \begin{pmatrix} C \cdot \cos(\lambda_{z, m} \cdot z) \\ + D \cdot \sin(\lambda_{z, m} \cdot z) \end{pmatrix} sin(\lambda_{z, m} \cdot z) dz$$

$$(2c-41)$$

we use the property of two orthogonal sets, i.e.,

$$\int \cos(\lambda_n z) \cdot \cos(\lambda_m z) dz = 0 \dots \Rightarrow n \neq m$$
and
$$\int \cos(\lambda_n z) \cdot \cos(\lambda_m z) dz = \int \cos(\lambda_n z) \cdot \cos(\lambda_n z) dz \dots \Rightarrow n = m$$
(2c-42)

or

$$\int_{z} \left[V_{bi} - \phi_{2D}(y, z) \right] \sin(\lambda_{z} \cdot z) dz = \left[\sum_{n=-\infty}^{\infty} \left(A \cdot D \cdot e^{-\lambda_{x} \cdot L} + B \cdot D \right) \cdot \int_{z} \sin(\lambda_{z} \cdot z)^{2} dz \cdot \cos(\lambda_{y, n} \cdot y) \right] (2c-43)$$

The last equation is equivalent to the Fourier coefficient b_n , for the function $\int_z [V_{bi} - \phi_{2D}(y, z)] \sin(\lambda_z \cdot z) dz$, where b_n is defined as,

$$b_n = \int f(y)\sin(\lambda_y \cdot y)dy \tag{2c-44}$$

From Eq. (2c-43), and Eq. (2c-44),

$$(A \cdot D \cdot e^{-\lambda_x \cdot L} + B \cdot D) \int_z \sin(\lambda_z \cdot z)^2 dz = \int_y \cos(\lambda_{y,n} \cdot y) dy \int_z [V_{bi} - \phi_{2D}(y,z)] \sin(\lambda_z \cdot z) dz$$
 (2c-45)

$$B \cdot D = \frac{\iint \left[V_{bi} - \phi_{2D}(y, z) \right] \sin(\lambda_z \cdot z) \cos(\lambda_{y, n} \cdot y) dz dy}{\int \int \sin(\lambda_z \cdot z)^2 dz} - A \cdot D \cdot e^{-\lambda_x \cdot L}$$
(2c-46)

Again, we multiply Eq.(2c-40) by $cos(\lambda_z z)$ and integrate over the Fin height,

$$\int_{z} \left[V_{bi} - \phi_{2D}(y, z) \right] \cdot \cos(\lambda_{z} \cdot z) dz = \int_{z} \sum_{n = -\infty}^{\infty} \sum_{m = -\infty}^{\infty} \left(A \cdot e^{\lambda_{x} \cdot (L - 0)} + B \cdot e^{-\lambda_{x} \cdot 0} \right) \cdot \cos(\lambda_{y, n} \cdot y) \cdot \begin{pmatrix} C \cdot \cos(\lambda_{z, m} \cdot z) \\ + D \cdot \sin(\lambda_{z, m} \cdot z) \end{pmatrix} \cos(\lambda_{z} \cdot z) dz$$
(2c-47)

or

$$\int_{z} \left[V_{bi} - \phi_{2D}(y, z) \right] \cos \left(\lambda_{z} \cdot z \right) dz = \left[\sum_{n = -\infty}^{\infty} \left(A \cdot C \cdot e^{-\lambda_{z} \cdot L} + B \cdot C \right) \cdot \int_{z} \cos \left(\lambda_{z} \cdot z \right)^{2} dz \cdot \cos \left(\lambda_{y, n} \cdot y \right) \right] (2c-48)$$

The last equation is equivalent to the fourier coefficient a_n , for the function $\int [V_{bi} - \phi_{2D}(y, z)] \cos(\lambda_z \cdot z) dz$, where a_n is defined as,

$$a_n = \int f(y)\cos(\lambda_y \cdot y)dy \tag{2c-49}$$

$$\iint_{z} [V_{bi} - \phi_{2D}(y, z)] \cos(\lambda_{z} \cdot z) \cos(\lambda_{y} \cdot y) dz dy$$

$$B \cdot C = \frac{\int_{z}^{y \cdot z} [V_{bi} - \phi_{2D}(y, z)] \cos(\lambda_{z} \cdot z) \cos(\lambda_{y} \cdot y) dz dy}{\int_{z}^{z} \cos(\lambda_{z} \cdot z)^{2} dz} - A \cdot C \cdot e^{-\lambda_{x} \cdot L}$$
(2c-50)

(B.C.5) Drain end Boundary condition: apply Eq.(24) into Eq. (2c-27),

$$V_{ds} + V_{bi} - \phi_{2D}(y, z) = \sum_{n = -\infty}^{\infty} \sum_{m = -\infty}^{\infty} \left(A + B \cdot e^{-\lambda_x \cdot L} \right) \cdot \cos(\lambda_{y, n} \cdot y) \cdot \left(C \cdot \cos(\lambda_{z, m} \cdot z) + D \cdot \sin(\lambda_{z, m} \cdot z) \right) \quad (2c-51)$$

we multiply the last equation by $sin(\lambda_z z)$ and integrate both sides, and solve for AD,

$$A \cdot D = \frac{\iint \left[V_{ds} + V_{bi} - \phi_{2D}(y, z) \right] \sin(\lambda_z \cdot z) \cos(\lambda_{y,n} \cdot y) dz dy}{\iint \int \sin(\lambda_z \cdot z)^2 dz} - B \cdot D \cdot e^{-\lambda_x \cdot L}$$
(2c-52)

Again we multiply Eq.(2c-51) by $cos(\lambda_z z)$ and solve for AC,

$$A \cdot C = \frac{\iint_{z} V_{ds} + [V_{bi} - \phi_{2D}(y, z)] \cos(\lambda_{z} \cdot z) \cos(\lambda_{y} \cdot y) dz dy}{\int_{z} \cos(\lambda_{z} \cdot z)^{2} dz} - B \cdot C \cdot e^{-\lambda_{x} \cdot L}$$
(2c-53)

we name the variables $\Delta R_o,\,\Delta P_o,\,\Delta R_1,\,\Delta P_1,\,Q_o,$ and Q_1 as,

$$\Delta R_o = \int_z \sin(\lambda_z \cdot z)^2 dz = -\frac{1}{\lambda_z} \cdot \left[\frac{\sin(2\lambda_z)}{2} - \lambda_z \right] \dots \lambda_z \neq 0$$
 (2c-54)

$$\Delta R_1 = \int_z \cos(\lambda_z \cdot z)^2 dz = \frac{1}{\lambda_z} \cdot \left[\frac{\sin(2\lambda_z)}{2} + \lambda_z \right]$$
 (2c-55)

$$\Delta P_o = \int_z \sin(\lambda_z \cdot z) dz \tag{2c-56}$$

$$\Delta P_1 = \int_z \cos(\lambda_z \cdot z) dz \tag{2c-57}$$

$$\Delta P_2 = \Delta P_1 \int_{y} \cos(\lambda_y \cdot y) dy = \frac{4}{\lambda_y \cdot \lambda_z} \sin(\lambda_z) \cdot \sin(\lambda_y)$$
 (2c-58)

Fig . 2c-2, shows the variation of $\Delta R_o, \Delta R_1, \Delta P_1$ and ΔP_2 against eigen values, $\lambda_z.$

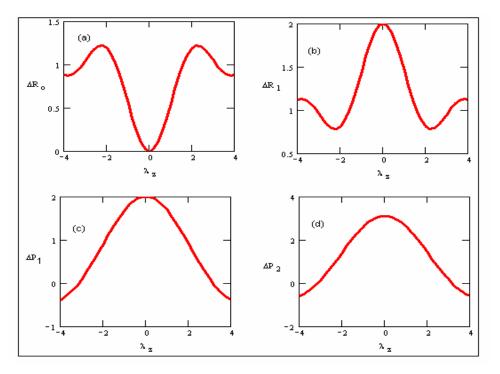


Fig. 2c-2 Potential parametric figure (ΔR_0 , ΔR_1 , ΔP_1 and ΔP_2)

Set,

$$Q_o(y) = \int_z \phi_{2D}(y, z) \sin(\lambda_z \cdot z) dz = -\frac{2 \cdot \alpha_o(y)}{\lambda_z^2} \cdot \left[\sin(\lambda_z) - \lambda_z \cdot \cos(\lambda_z) \right]$$
 (2c-59)

$$Q_{1} = \int_{z} \phi_{2D}(y, z) \cos(\lambda_{z} \cdot z) dz = 2 \cdot \frac{\phi_{1D}(y)}{\lambda_{z}} \left[\sin(\lambda_{z}) + \frac{2 \cdot \alpha_{1}(y)}{\phi_{1D}(y)} \cdot \left[\sin(\lambda_{z}) \left(\frac{1}{2} - \frac{1}{\lambda_{z}^{2}} \right) + \frac{\cos(\lambda_{z})}{\lambda_{z}} \right] \right]$$
(2c-60)

where Q_0 , and Q_1 are two symmetric functions along the y-axis as shown in Fig. 2c-3. We rewrite the equations of AD,AC,BD and BC in terms of the new variables to be as,

$$B \cdot D = \frac{V_{bi} \Delta P_o \int \cos(\lambda_y \cdot y) dy - \int_{y} Q_o(y) \cos(\lambda_y \cdot y) dy}{\Delta R_o} - A \cdot D \cdot e^{-\lambda_x \cdot L}$$
(2c-61)

$$B \cdot C = \frac{V_{bi} \Delta P_1 \int \cos(\lambda_y \cdot y) dy - \int Q_1(y) \cos(\lambda_y \cdot y) dy}{\Delta R_1} - A \cdot C \cdot e^{-\lambda_x \cdot L}$$
(2c-62)

$$(V_{ds} + V_{bi}) \cdot \Delta P_o \int_{y} \cos(\lambda_y \cdot y) dy - \int_{y} Q_o(y) \cos(\lambda_y \cdot y) dy$$

$$A \cdot D = \frac{1}{\Delta R_o} - B \cdot D \cdot e^{-\lambda_x \cdot L}$$
(2c-63)

$$A \cdot C = \frac{(V_{ds} + V_{bi}) \cdot \Delta P_1 \int_{y} \cos(\lambda_y \cdot y) dy - \int_{y} Q_1(y) \cos(\lambda_y \cdot y) dy}{\Delta R_1} - B \cdot C \cdot e^{-\lambda_x \cdot L}$$
(2c-64)

The 3D Potential can then rewritten as,

$$\phi_{3D}(x,y,z) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} \cos(\lambda_{y,n} \cdot y) \cdot \left[\cos(\lambda_{z,m} \cdot z) \cdot \left(AC \cdot e^{\lambda_{x,k} \cdot (L-x)} + BC \cdot e^{-\lambda_{x,k} \cdot x} \right) + \sin(\lambda_{z,m} \cdot z) \cdot \left(AD \cdot e^{\lambda_{x,k} \cdot (L-x)} + BD \cdot e^{-\lambda_{x,k} \cdot x} \right) \right] (2c-65)$$

$$\phi_{3D}(x,y,z) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} \sum_{k=-\infty}^{\infty} \cos(\lambda_{y,n} \cdot y) \cdot \left[\cos(\lambda_{z,m} \cdot z) \cdot \left(A' \cdot e^{\lambda_{x,k} \cdot (L-x)} + C' \cdot e^{-\lambda_{x,k} \cdot x} \right) + \sin(\lambda_{z,m} \cdot z) \cdot \left(B' \cdot e^{\lambda_{x,k} \cdot (L-x)} + D' \cdot e^{-\lambda_{x,k} \cdot x} \right) \right] (2c-66)$$

$$A' = A \cdot C = \frac{\left(V_{ds} + V_{bi} \left[1 - e^{-\lambda_x \cdot L}\right]\right) \cdot \Delta P_2 - S_1 \cdot \left[1 - e^{-\lambda_x \cdot L}\right]}{\Delta R_1 \cdot \left[1 - e^{-2\lambda_x \cdot L}\right]}$$
(2c-67)

$$B' = A \cdot D = \frac{-S_o \cdot \left| 1 - e^{-\lambda_x \cdot L} \right|}{\Delta R_o \cdot \left| 1 - e^{-2\lambda_x \cdot L} \right|}$$
(2c-68)

$$C' = B \cdot C = \frac{V_{bi} \cdot \Delta P_2 - S_1}{\Delta R_1} - A' \cdot e^{-\lambda_x \cdot L}$$
(2c-69)

$$C' = \frac{\Delta P_2}{\Delta R_1} \left[V_{bi} - \frac{\left[V_{ds} + V_{bi} \cdot \left(1 - e^{-\lambda_x \cdot L} \right) \right]}{2 \sinh(\lambda_x \cdot L)} \right] - \frac{S_1}{\Delta R_1} \left[1 - \frac{\left(1 - e^{-\lambda_x \cdot L} \right)}{2 \sinh(\lambda_x \cdot L)} \right]$$

$$(2c-70)$$

$$D' = B \cdot D = \frac{-S_o}{\Delta R_o} - B' \cdot e^{-\lambda_x \cdot L}$$
 (2c-71)

$$D' = -\frac{S_o}{\Delta R_o} \left[1 - \frac{\left(1 - e^{-\lambda_x \cdot L} \right)}{2 \sinh(\lambda_x \cdot L)} \right]$$
 (2c-72)

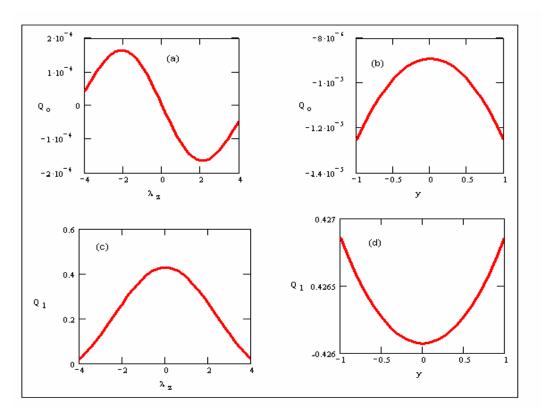


Fig. 2c-3 Qo, and Q1 vs. normalized Fin width, and eigen values

Set,

$$S_o = \int_{y} Q_o \cos(\lambda_y \cdot y) dy$$
 (2c-73)

$$S_1 = \int_{\mathcal{V}} Q_1 \cos(\lambda_y \cdot y) dy \tag{2c-74}$$

Where S_o , and S_1 have not analytical solutions but from the symmetry of both Qo, and Q1 along y-axis as shown in Fig. (2c-3), both S_o , and S_1 can be approximated as,

$$S_o \approx 2Q_o(y = 0.5) \cdot \cos\left(\frac{\lambda_y}{2}\right)$$
 (2c-75)

$$S_o = \frac{4}{\lambda_z^2} \cdot \left[\sin(\lambda_z) - \lambda_z \cdot \cos(\lambda_z) \right] \cdot \cos\left(\frac{\lambda_y}{2}\right) \cdot \alpha_o \Big|_{y=0.5}$$
 (2c-76)

$$S_1 \approx \left[2Q_1(y=0.5) - V_T\right] \cos\left(\frac{\lambda_y}{2}\right) \tag{2c-77}$$

$$S_{1} = \left\{ \frac{4}{\lambda_{z}} \cdot \left[\sin(\lambda_{z}) \cdot \phi_{1D}(y = 0.5) - \alpha_{1}(y = 0.5) \cdot \left(\sin(\lambda_{z}) \cdot \left[\frac{1}{2} - \frac{1}{\lambda_{z}^{2}} \right] + \frac{\cos(\lambda_{z})}{\lambda_{z}} \right) \right] - V_{T} \right\} \cdot \cos\left(\frac{\lambda_{y}}{2} \right) (2c - 78)$$

Where V_T is just an offset. The comparison between exact and the approximated values of S_o , and S_I is shown in Fig.(2c-4).

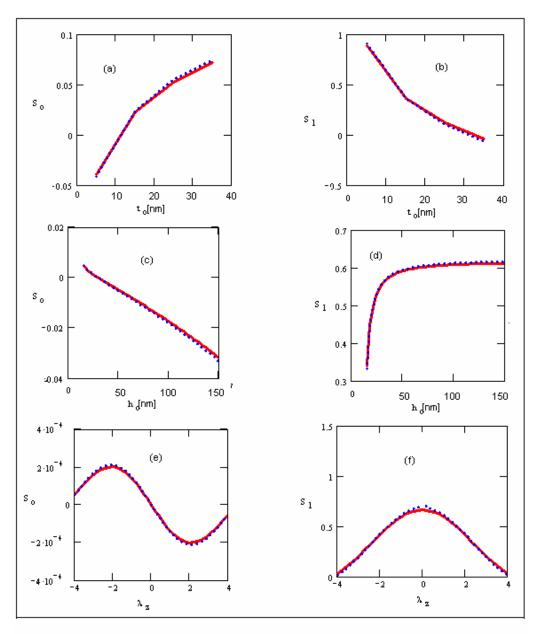


Fig. 2c-4 Comparison between exact values (solid lines), and the approximated values (dotted lines) of So, and S1.

In Eq.(2c-66) replace the exponential function by hyperbolic functions and rearrange the terms again, we got

$$\phi_{3D}(x,y,z) = \cos(\lambda_y \cdot y) \cdot \left\{ \sum_{N=0}^{1} \frac{\Delta P_2}{\Delta R_1} \cos(\lambda_{zN} \cdot z) \cdot \left[V_{ds} \cdot D_1 + V_{bi} \cdot D_o \right] - \left(\frac{S_1}{\Delta R_1} \cos(\lambda_{zN} \cdot z) + \frac{S_o}{\Delta R_o} \cdot \sin(\lambda_{zN} \cdot z) \right) \cdot D_o \right\} (2c-79)$$

The two summing symbols have been removed; we only consider the lowest eigen value, with,

$$D_o = \frac{\sinh(\lambda_x \cdot x) - \sinh[\lambda_x \cdot (x - L)]}{\sinh(\lambda_x \cdot L)}$$
Eq.(2C-26)

$$D_1 = \frac{\sinh(\lambda_x \cdot x)}{\sinh(\lambda_x \cdot L)}$$
 Eq.(2C-27)

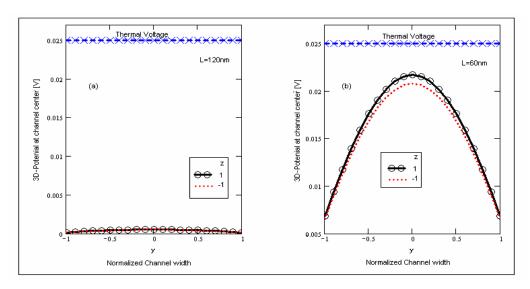


Fig. 2c-5 proves the assumption done in Eq. 19, Hfin=60nm, Wfin=20nm. The potential is drawn at $y=0.75W_{FIN}$, x=0.5L, and $z=H_{FIN}$

Now, the complete 3D potential can be calculated by summing both 3D-potential part (Eq. 2c-66) and 2-D potential part (Eq. 2C-13), as shown in Fig.2c-6 a, and b.

In Fig. 2c-6a the device is quite long and therefore the device electrostatics is governed only by the 2D-part (≅ 1D potential value) where the Short Channel Effects are negiligible. In Fig.2c-6b, the device length is scaled down and therefore the gate losts the full controllability of the channel electrostatic potential, and the drain/source potential are arises the channel potential to increase the SCEs, as shown in Fig.(2c-6b).

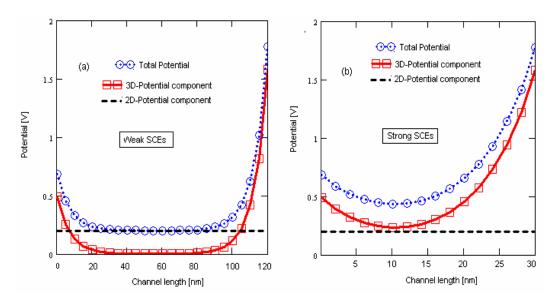


Fig. 2c-6 3D potential components vs. channel length at a) Long channel devices, b) Short channel devices. H_{FIN}=60nm, W_{FIN}=20nm. The potential is drawn at y=0.75W_{FIN}, and z=H_{FIN}

(C) VIRTUAL CATHODE VALUE AND POSITION

The virtual cathode value is the point at which the potential has its minimum value. By finding this point (along the channel length), the virtual cathode expression can be calculated substituting by this value into the general form of the

3D-electrostatic potential. The minimum value will take place at the position at which,

$$\frac{\partial \phi(x, y, z)}{\partial x}\bigg|_{x=x} = 0 \tag{2c-80}$$

Applying the last definition into Eq. 2C-27, we got

$$x_{\min} = \frac{L}{2} - \frac{1}{\lambda_x} \cdot \ln \left[\frac{A' + B' \cdot \tan(\lambda_z \cdot z)}{C' + D' \cdot \tan(\lambda_z \cdot z)} \right]$$
 (2c-81)

where as shown from Fig. 2c-7, the minimum position will not be dependent on the position along y-axis (where it is symmetric), but there is a small dependence on the z-axis position due to the asymmetric device structure (biasing and structure). From Fig. 2c-7, we conclude that there is only one point in the devices which will be the virtual cathode value, (which will accounting as the weak path). The minimum potential can then be written as (see Fig. 2c-8),

$$\phi_{3D_{-\min}}(y,z) = \cos(\lambda_{y} \cdot y) \cdot \left\{ \sum_{N=0}^{1} \frac{\Delta P_{2}}{\Delta R_{1}} \cos(\lambda_{zN} \cdot z) \cdot \left[V_{ds} \cdot D_{1\min} + V_{bi} \cdot D_{o\min} \right] - \left(\frac{S_{1}}{\Delta R_{1}} \cos(\lambda_{zN} \cdot z) + \frac{S_{0}}{\Delta R_{0}} \cdot \sin(\lambda_{zN} \cdot z) + \frac{S_{0}}{\Delta R_{0}} \cdot \sin(\lambda_{zN} \cdot z) \right) \cdot D_{o\min} \right\} + \phi_{2D}(y,z)$$

$$(2c-82)$$

$$D_{o \min} = \frac{\sinh(\lambda_x \cdot x_{\min}) - \sinh[\lambda_x \cdot (x_{\min} - L)]}{\sinh(\lambda_x \cdot L)}$$
(2c-83)

$$D_{1\min} = \frac{\sinh(\lambda_x \cdot x_{\min})}{\sinh(\lambda_x \cdot L)}$$
 (2c-84)

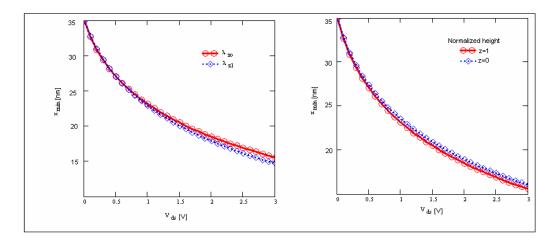


Fig.2c-7 The virtual cathode position vs. drain-source voltage. due to a) the effect of the eigen value, and b) the position from center to the top gate.

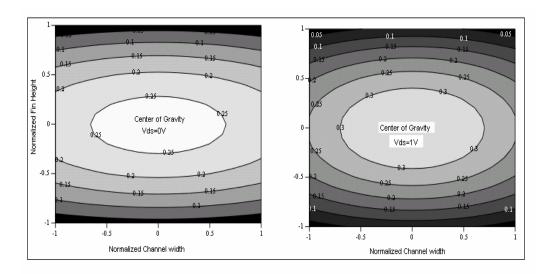


Fig. 2c-8 the contour of virtual cathode at a) Vds=0V, b) Vds=1V, L=60nm, Hfin=60nm, V_{GS1}=0.2V, Wfin=20nm.

(D) SUBTHRESHOLD SWING

From Eq.(2C-31), the subthreshold swing defined as,

SCEs in undoped multiple gate MOS

$$I_D \alpha \int_{y=-t_o}^{t_o} \int_{z=-h_o}^{h_o} n_i \cdot e^{\frac{\phi_{min}(y,z)}{V_i}} dz dy$$
 (Eq.2C-31)

or

$$S = \frac{\partial V_{GS1}}{\partial \log I_D} = \begin{bmatrix} 2 \cdot \int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y, z) \frac{\partial \phi_{3D_{min}}(y, z)}{\partial V_{GS1}} dy dz \\ 2 \cdot \int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y, z) dy dz \end{bmatrix}^{-1}$$
(Eq.2C-32)

However the last integration is the exact expression for the subthreshold swing, and can be calculated at the conduction path,:

$$S = \frac{\partial V_{GS1}}{\partial \log I_D} = \left[\frac{n_m(y_c, z_c) \frac{\partial \phi_{3D_\min}(y_c, z_c)}{\partial V_{GS1}}}{n_m(y_c, z_c)} \right]^{-1} = \left[\frac{\partial \phi_{3D_\min}(y_c, z_c)}{\partial V_{GS1}} \right]^{-1}$$
(2c-85)

By differentiating Eq. (2c-82) respecting to the V_{GS1} , or

$$\frac{\partial \phi_{3D_{\min}}(y_c, z_c)}{\partial V_{GS1}} = \frac{\partial}{\partial V_{GS1}} \left[\cos(\lambda_y \cdot y_c) \left\{ \sum_{N=0}^{1} \frac{\Delta P_2}{\Delta R_1} \cos(\lambda_{zN} \cdot z_c) \cdot \left[V_{ds} \cdot D_{1 \min} + V_{bi} \cdot D_{o \min} \right] - \frac{1}{\Delta R_1} \left[\frac{S_1}{\Delta R_1} \cos(\lambda_{zN} \cdot z_c) + \frac{S_o}{\Delta R_o} \cdot \sin(\lambda_{zN} \cdot z_c) \right] \cdot D_{o \min} \right\} + \phi_{2D}(y_c, z_c) \right] (2c-86)$$

Set,

$$D_{S_o} = \frac{\partial S_o}{\partial V_{GS1}} = \frac{\partial}{\partial V_{GS1}} \cdot \left[\frac{4}{\lambda_z^2} \cdot \left[\sin(\lambda_z) - \lambda_z \cdot \cos(\lambda_z) \right] \cdot \cos\left(\frac{\lambda_y}{2}\right) \cdot \alpha_o \Big|_{y=0.5} \right]$$
(2c-87)

$$D_{-}S_{1} = \frac{\partial S_{1}}{\partial V_{GS1}} = \frac{\partial}{\partial V_{GS1}} \left\{ \frac{4}{\lambda_{z}} \cdot \left[\sin(\lambda_{z}) \cdot \phi_{1D}(y = 0.5) - \alpha_{1}(y = 0.5) \cdot \left(\frac{\sin(\lambda_{z}) \cdot \left[\frac{1}{2} - \frac{1}{\lambda_{z}^{2}} \right]}{\lambda_{z}} \right] \right\} - V_{T} \right\} \cdot \cos\left(\frac{\lambda_{y}}{2} \right) (2c - 88)$$

$$D_{-}\phi_{2D} = \frac{\partial}{\partial V_{GS1}} \left[\phi_{1D}(y_c) + \alpha_o(y_c) \cdot z_c + \alpha_1(y_c) \cdot z_c^2 \right]$$
 (2c-89)

From the symmetry along y-axis, (yc \cong 0.5):

$$\frac{\partial}{\partial V_{GSI}} \phi_{1D}(y_c) = \frac{\partial}{\partial V_{GSI}} \phi_{1D}(y = 0.5)$$
 (2c-90)

$$\frac{\partial}{\partial V_{GS1}} \alpha_o(y_c) = \frac{\partial}{\partial V_{GS1}} \alpha_o(y = 0.5) = \frac{\partial}{\partial V_{GS1}} \frac{\left[\left(V_{GS1} - \phi_{ms} \right) - \phi_{1D}(y_c) \right] - \Delta \cdot \left(\left(V_{GS2} - \phi_{ms} \right) - \phi_{1D}(y_c) \right)}{\left(1 - \frac{1}{C_{r1}} \right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}} \right)}$$
(2c-91)

and,

$$\frac{\partial}{\partial V_{GS1}} \alpha_1(y_c) = \frac{\partial}{\partial V_{GS1}} \alpha_1(y = 0.5) = \frac{\partial}{\partial V_{GS1}} \frac{\left[\left(V_{GS2} - \phi_{ms} \right) - \phi_{1D}(y_c) \right] + \alpha_o(y_c) \cdot \left(1 - \frac{1}{C_{r2}} \right)}{\left(1 - \frac{2}{C_{r2}} \right)}$$
(2c-92)

$$\frac{\partial}{\partial V_{GS1}} \alpha_o(y_c) = \frac{\Delta}{\left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)}$$
(2c-93)

$$\frac{\partial}{\partial V_{GS1}} \alpha_{1}(y_{c}) = \frac{\frac{\partial}{\partial V_{GS}} \alpha_{o}(y_{c}) \cdot \left(1 - \frac{1}{C_{r2}}\right) - 1}{\left(1 - \frac{2}{C_{r2}}\right)} = \frac{-\left(1 - \frac{1}{C_{r1}}\right)}{\left(1 - \frac{2}{C_{r2}}\right) \cdot \left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)}$$
(2c-94)

$$D_{-}\phi_{2D} = \left[1 + \frac{\partial}{\partial V_{GS1}}\alpha_{o}(y_{c}) \cdot z_{c} + \frac{\partial}{\partial V_{GS1}}\alpha_{1}(y_{c}) \cdot z_{c}^{2}\right]$$

$$D_{-}\phi_{2D} = 1 + \frac{\Delta}{\left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)} z_{c} - \frac{\left(1 - \frac{1}{C_{r1}}\right)}{\left(1 - \frac{2}{C_{r2}}\right) \cdot \left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)} z_{c}^{2} \approx 1$$
(2c-95)

The FinFET normally is designed to have a Fin height bigger than the Fin width, and therefore Eq.2c-95, at certain dimensions will tend to be unity (where for a very narrow device cross section, the exact solution in Eq. 2c-95 should not approximated to be unity).

From Eq.(2c-93) and Eq.(2c-94) into Eq.(2c-87), and Eq.(2c-88), we can write D_So, and D_S1 as,

$$D_{-}S_{o} = \frac{4}{\lambda_{z}^{2}} \cdot \left[\sin(\lambda_{z}) - \lambda_{z} \cdot \cos(\lambda_{z})\right] \cdot \cos\left(\frac{\lambda_{y}}{2}\right) \cdot \frac{\Delta}{\left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)}$$
(2c-96)

$$D_{-}S_{1} = \left\{ \frac{4}{\lambda_{z}} \cdot \left[\sin(\lambda_{z}) + \frac{\left(1 - \frac{1}{C_{r1}}\right)}{\left(1 - \frac{2}{C_{r2}}\right) \cdot \left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)} \cdot \left(\frac{\sin(\lambda_{z}) \cdot \left[\frac{1}{2} - \frac{1}{\lambda_{z}^{2}}\right]}{\lambda_{z}} \right] \right\} - V_{t} \right\} \cdot \cos\left(\frac{\lambda_{y}}{2}\right) \quad (2c-97)$$

or

$$D_{-}S_{o} = \frac{1}{\lambda_{z}^{2}} \cdot \left[\sin(\lambda_{z}) - \lambda_{z} \cdot \cos(\lambda_{z})\right] \cdot \cos\left(\frac{\lambda_{y}}{2}\right) \cdot \frac{1}{\left(1 - \frac{1}{C_{r2}}\right)} \frac{\Delta}{\Delta 1 + \Delta}$$
(2c-98)

$$D_{-}S_{1} = \frac{4}{\lambda_{z}} \cdot \left[\sin(\lambda_{z}) + \frac{1}{\left(1 - \frac{2}{C_{r2}}\right)} \frac{\Delta 1}{\Delta 1 + \Delta} \cdot \left[\frac{\sin(\lambda_{z}) \cdot \left[\frac{1}{2} - \frac{1}{\lambda_{z}^{2}}\right]}{+\frac{\cos(\lambda_{z})}{\lambda_{z}}} \right] \right] \cdot \cos\left(\frac{\lambda_{y}}{2}\right)$$

$$(2c-99)$$

Finally we can write,

$$\frac{\partial \phi_{3D_\min}(y_c, z_c)}{\partial V_{GS1}} = 1 - \left[\cos(\lambda_y \cdot y_c) \cdot \left\{ \sum_{N=0}^{1} \left(\frac{D_S_1}{\Delta R_1} \cos(\lambda_{zN} \cdot z_c) + \frac{D_S_o}{\Delta R_o} \cdot \sin(\lambda_{zN} \cdot z_c) \right) \cdot D_{o\min} \right\} \right] (2c-100)$$

Using Eq. (2c-100) into Eq. (2c-85), the subthreshold swing is found as

SCEs in undoped multiple gate MOS

$$S.S = \left\{1 - \left[\cos(\lambda_y \cdot y_c) \cdot \left\{\sum_{N=0}^{1} \left(\frac{D_- S_1}{\Delta R_1} \cos(\lambda_{zN} \cdot z_c) + \frac{D_- S_o}{\Delta R_o} \cdot \sin(\lambda_{zN} \cdot z_c)\right) \cdot D_{o \min}\right\}\right]\right\}^{-1} \quad (2c-101)$$

We set K_1 , and K_2 as,

$$K_1 = \frac{S_o}{\Delta R_o} \frac{D_{o \, \text{min}}}{\phi_{1D} \left(y = 0.5 \right)} \tag{2c-102}$$

$$K_2 = \frac{S_1}{\Delta R_1} \frac{D_{o \min}}{\phi_{1D}(y = 0.5)}$$
 (2c-103)

we can write,

$$S.S = \left[1 - \sum_{\lambda_{\infty,1}} K_1 \cdot \cos(\lambda_y \cdot y_c) \cdot \cos(\lambda_z \cdot z_c) + K_2 \cdot \cos(\lambda_y \cdot y_c) \cdot \sin(\lambda_z \cdot z_c)\right]^{-1} \cdot V_T \cdot \ln(10) \qquad (2c-104)$$

By comparing Eq. (2c-104) with Eq. (32), we can write

$$1 - \cos(\lambda_y \cdot y_c) \cdot \cos(\lambda_z \cdot z_c) = \begin{bmatrix} \int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y, z) \cdot \cos(\lambda_y \cdot y) \cdot \cos(\lambda_z \cdot z) dy dz \\ \int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y, z) dy dz \end{bmatrix}^{-1}$$

$$(2c-105)$$

And,

$$\cos(\lambda_y \cdot y_c) \cdot \sin(\lambda_z \cdot z_c) = \left[\frac{\int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y, z) \cdot \cos(\lambda_y \cdot y) \cdot \sin(\lambda_z \cdot z) dy dz}{\int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y, z) dy dz} \right]^{-1}$$

$$(2c-106)$$

or

SCEs in undoped multiple gate MOS

$$\cos(\lambda_{y} \cdot y_{c}) \cdot \cos(\lambda_{z} \cdot z_{c}) = \begin{bmatrix} \int_{z=-h_{o}}^{h_{o}} \int_{y=0}^{t_{o}} n_{m}(y, z) \cdot \cos(\lambda_{y} \cdot y) \cdot \cos(\lambda_{z} \cdot z) dy dz \\ \int_{z=-h_{o}}^{h_{o}} \int_{y=0}^{t_{o}} n_{m}(y, z) dy dz \end{bmatrix}^{-1}$$

$$(2c-105')$$

And,

$$1 - \cos(\lambda_y \cdot y_c) \cdot \sin(\lambda_z \cdot z_c) = \begin{bmatrix} \int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y, z) \cdot \cos(\lambda_y \cdot y) \cdot \sin(\lambda_z \cdot z) dy dz \\ \int_{z=-h_o}^{h_o} \int_{y=0}^{t_o} n_m(y, z) dy dz \end{bmatrix}^{-1}$$

$$(2c-106')$$

We can write S.S as,

$$S.S = \frac{V_T \cdot \ln(10)}{1 - S_{\sigma s}} \cdot 1000 \Rightarrow \left[mV / Dec \right]$$
(2c-107)

Remember that both K_1 , and K_2 are in units of V/V, $(S_o, \text{ and } S_1 \text{ are in units of } Volt)$. Where,

$$S_{gs} = \sum_{\lambda_{z_{o,1}}} K_1 \cdot \cos(\lambda_y \cdot y_c) \cdot \cos(\lambda_z \cdot z_c) + K_2 \cdot \cos(\lambda_y \cdot y_c) \cdot \sin(\lambda_z \cdot z_c)$$
 (2c-108)

The subthreshold swing has been extracted from I_{ds} - V_{GS} curves experminatly (Fig. 2c-9 show an example for the measured I_{ds} - V_{GS} in logarithmic scale) and numerically, with a good agreement with both as shown from the figures through the chapter.

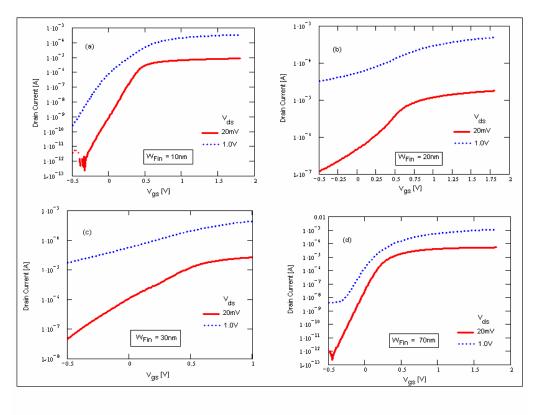


Fig. 2c-9 Measured I_{ds} - V_{GS} in logarithmic scale, Hfin=60nm, and L=40nm

(E) THRESHOLD VOLTAGE CALCULATIONS

The inversion charge can be written as,

$$Q_{inv} = 2 \int_{y=0}^{t_o} \int_{z=-h_o}^{h_o} n_i \cdot e^{\frac{\phi_{\min}(y,z)}{V_T}} dz dy$$
 (2c-109)

From the devices symmetry along the Fin width, the last integration can be approximated as

$$Q_{inv} = (2 \cdot t_o) \cdot (\alpha \cdot H_{FIN}) \cdot n_i \cdot e^{\frac{\phi_{\min}(y_c, z_c)}{V_T}}$$
(2c-110)

$$\phi_{\min}(y_c, z_c) = V_T \ln \left[\frac{Q_{inv}}{(W_{FIN}) \cdot (\alpha \cdot H_{FIN}) \cdot n_i} \right]$$
(2c-111)

Using Eq.(2c-86), into Eq.(2c-111),

$$\cos(\lambda_{y} \cdot y_{c}) \cdot \left\{ \sum_{N=0}^{1} \frac{\Delta P_{2}}{\Delta R_{1}} \cos(\lambda_{zN} \cdot z_{c}) \cdot \left[V_{ds} \cdot D_{1 \min} + V_{bi} \cdot D_{o \min} \right] - \left(\frac{S_{1}}{\Delta R_{1}} \cos(\lambda_{zN} \cdot z_{c}) + \frac{S_{1}}{\Delta R_{1}} \cos(\lambda_{zN} \cdot z_{c}) + \frac{S_{2}}{\Delta R_{0}} \cdot \sin(\lambda_{zN} \cdot z_{c}) \right) \right\} + \phi_{2D}(y_{c}, z_{c}) \left(2\mathbf{c} - 112 \right)$$

$$= V_{T} \ln \left[\frac{Q_{inv}}{(W_{EIN}) \cdot (\alpha \cdot H_{EIN}) \cdot n_{i}} \right]$$

or

$$-\cos(\lambda_{y} \cdot y_{c}) \cdot \sum_{N=0}^{1} \left(\frac{S_{1}}{\Delta R_{1}} \cos(\lambda_{zN} \cdot z_{c}) + \frac{S_{0}}{\Delta R_{0}} \cos(\lambda_{zN} \cdot z_{c}) + \frac{S_{0}}{\Delta R_{0}} \cos(\lambda_{zN} \cdot z_{c}) \right) \cdot D_{0 \min} + \phi_{2D}(y_{c}, z_{c})$$

$$= V_{T} \ln \left[\frac{Q_{inv}}{(W_{EIN}) \cdot (\alpha \cdot H_{EIN}) \cdot n_{i}} \right] - \cos(\lambda_{y} \cdot y_{c}) \cdot \sum_{N=0}^{1} \frac{\Delta P_{2}}{\Delta R_{1}} \cos(\lambda_{zN} \cdot z_{c}) \cdot \left[V_{ds} \cdot D_{1 \min} + V_{bi} \cdot D_{0 \min} \right]$$

$$(2c-113)$$

$$\phi_{2D}(y_{c}, z_{c}) - \cos(\lambda_{y} \cdot y_{c}) \cdot \sum_{N=0}^{1} \left(\frac{S_{1}}{\Delta R_{1}} \cos(\lambda_{zN} \cdot z_{c}) + \frac{S_{o}}{\Delta R_{o}} \cdot \sin(\lambda_{zN} \cdot z_{c}) \right) \cdot D_{o \min}$$

$$= V_{T} \ln \left[\frac{Q_{inv}}{(W_{EIN}) \cdot (\alpha \cdot H_{EIN}) \cdot n_{i}} \right] - S_{ds}$$
(2c-114)

$$S_{ds} = \cos(\lambda_y \cdot y_c) \cdot \sum_{n=0}^{1} \frac{\Delta P_2}{\Delta R_1} \cos(\lambda_{z,n} \cdot z_c) \cdot \left[V_{ds} \cdot D_{1 \min} + V_{bi} \cdot D_{o \min} \right]$$
 (2c-115)

Write,

$$\frac{\phi_{2D}(y_c, z_c)}{\phi_{1D}(y_c)} = \left(1 + \frac{\alpha_o(y_c)}{\phi_{1D}(y_c)} z_c + \frac{\alpha_1(y_c)}{\phi_{1D}(y_c)} z_c^2\right) \\
= 1 + \frac{\Delta \cdot \phi_{1D}(y_c)}{\phi_{1D}(y_c) \cdot \left[\left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)\right]} + \frac{-\phi_{1D}(y_c) + \alpha_o(y_c) \cdot \left(1 - \frac{1}{C_{r2}}\right)}{\left(1 - \frac{2}{C_{r2}}\right) \cdot \phi_{1D}(y_c)} + \delta$$

$$= 1 + \frac{\Delta \cdot \phi_{1D}(y_c)}{\phi_{1D}(y_c) \cdot \left[\left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)\right]} z_c + \frac{-\phi_{1D}(y_c)}{\left(1 - \frac{2}{C_{r2}}\right) \cdot \phi_{1D}(y_c)} + \frac{\Delta \cdot \phi_{1D}(y_c)}{\left[\left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)\right] z_c^2 + \delta} (2c-117)$$

$$= 1 + \frac{\Delta}{\left[\left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)\right]} z_c + \frac{\Delta}{\left[\left(1 - \frac{1}{C_{r2}}\right) \cdot \phi_{1D}(y_c)\right]} z_c + \frac{\Delta}{\left[\left(1 - \frac{1}{C_{r2}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right)\right]} z_c^2 + \delta (2c-118)$$

Where F_1 accounts for the ratio between the top gate oxide to the buried oxide, and written as,

$$F_{1} = \left\{ \frac{1}{\left(1 - \frac{1}{C_{r2}}\right)} \frac{\Delta}{\Delta_{1} + \Delta} \right\} \cdot z_{c} + \left\{ -\frac{1}{\left(1 - \frac{2}{C_{r2}}\right)} + \frac{\Delta}{\left[\Delta_{1} + \Delta\right]} \right\} \cdot z_{c}^{2}$$

$$(2c-119)$$

 δ accounts for the ratio between back gate biasing, V $_{GS2}$ and V $_{GS1},$ and can be written as

$$\delta = \delta_2 - \delta_1 = \left\{ \frac{(V_{GS2} - \phi_{ms})}{\left(1 - \frac{2}{C_{r2}}\right) \cdot \phi_{1D}(y_c)} \cdot \right\} z_c^2 - \left\{ \frac{\Delta \cdot (V_{GS2} - \phi_{ms})}{\phi_{1D}(y_c) \cdot \left[\left(1 - \frac{1}{C_{r1}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right) \right]} \right\} \cdot z_c$$
(2c-120)

Since,

$$S_o = -2 \cdot \frac{2 \cdot \alpha_o(y = 0.5)}{\lambda_z^2} \cdot \left[\sin(\lambda_z) - \lambda_z \cdot \cos(\lambda_z) \right] \cdot \cos\left(\frac{\lambda_y}{2}\right)$$
 (2c-64)

where,

$$\alpha_{o}(y=0.5) = \frac{\left[(V_{GS1} - \phi_{ms}) - \phi_{1D}(y=0.5) \right] - \Delta \cdot ((V_{GS2} - \phi_{ms}) - \phi_{1D}(y=0.5))}{\left(1 - \frac{1}{C_{r1}} \right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}} \right)}$$

$$= \frac{\left[(V_{GS1} - \phi_{ms}) \right] + \phi_{1D}(y=0.5) \cdot (\Delta - 1)}{\left(1 - \frac{1}{C_{r1}} \right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}} \right)} - \delta_{1} \cdot \phi_{1D}(y=0.5)$$

$$= \frac{\Delta}{\left(1 - \frac{1}{C_{r1}} \right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}} \right)} \cdot \phi_{1D}(y=0.5) - \delta_{1} \cdot \phi_{1D}(y=0.5)$$

$$= \frac{\Delta}{\left(1 - \frac{1}{C_{r1}} \right) + \Delta \cdot \left(1 - \frac{1}{C_{r2}} \right)} \cdot \phi_{1D}(y=0.5) - \delta_{1} \cdot \phi_{1D}(y=0.5)$$

Since the device is undoped, the electric field is $\cong 0$, or

$$[(V_{GS1} - \phi_{ms}) - \phi_{1D}(y_c)] \approx 0$$
 (2c-122)

$$S_{o} = \frac{4}{\lambda_{z}^{2}} \cdot \left[sin\left(\lambda_{z}\right) - \lambda_{z} \cdot \cos\left(\lambda_{z}\right) \right] \cdot \cos\left(\frac{\lambda_{y}}{2}\right) \cdot \frac{\Delta}{\left(1 - \frac{1}{C_{r}}\right) + \Delta \cdot \left(1 - \frac{1}{C_{r}}\right)} \cdot \phi_{1D}\left(y = 0.5\right) - \delta_{1} \cdot \phi_{1D}\left(y = 0.5\right) \cdot \left(2c - 123\right)$$

From Eq. (2C-15), we can write

$$\frac{\alpha_{1}(y=0.5)}{\phi_{1D}(y=0.5)} = \frac{1}{\phi_{1D}(y=0.5)} \cdot \frac{\left[\left(V_{GS2} - \phi_{ms}\right) - \phi_{1D}(y=0.5)\right] + \alpha_{o}(y=0.5) \cdot \left(1 - \frac{1}{C_{r2}}\right)}{\left(1 - \frac{2}{C_{r2}}\right)}$$
(2C-15)

$$\frac{\alpha_1(y=0.5)}{\phi_{1D}(y=0.5)} = -\frac{1}{\left(1 - \frac{2}{C_{r2}}\right)} + \frac{\Delta}{\left(1 - \frac{1}{C_{r1}}\right)} + \Delta \cdot \left(1 - \frac{1}{C_{r2}}\right) \cdot \frac{\left(1 - \frac{1}{C_{r2}}\right)}{\left(1 - \frac{2}{C_{r2}}\right)} + \delta'$$
(2c-124)

$$\delta' = \delta_2 - \delta_1 \cdot \frac{\left(1 - \frac{1}{C_{r2}}\right)}{\left(1 - \frac{2}{C_{r2}}\right)} \tag{2c-125}$$

From Eq. (2c-124), and (2c-125) into Eq. (2c-66),

SCEs in undoped multiple gate MOS

$$S_{1} = 2 \cdot 2 \cdot \frac{\phi_{1D}(y = 0.5)}{\lambda_{z}} \left[\sin(\lambda_{z}) + \frac{2 \cdot \alpha_{1}(y = 0.5)}{\phi_{1D}(y = 0.5)} \cdot \left[\sin(\lambda_{z}) \left(\frac{1}{2} - \frac{1}{\lambda_{z}^{2}} \right) + \frac{\cos(\lambda_{z})}{\lambda_{z}} \right] \right] \cdot \cos\left(\frac{\lambda_{y}}{2}\right) - V_{t} \cdot \cos\left(\frac{\lambda_{y}}{2}\right)$$

$$(2c-66)$$

put
$$(V_{gs2} - \phi_{ms}) \approx 0$$

$$S_{1} = 4 \cdot \frac{\phi_{1D}(y = 0.5)}{\lambda_{z}} \left[sin(\lambda_{z}) + 2 \cdot \left\{ \frac{1}{\left(1 - \frac{2}{C_{r2}}\right)} \left(\frac{\Delta}{\left(1 - \frac{1}{C_{r1}}\right)} + \Delta \right) + \delta' \right\} \right] \cdot cos\left(\frac{\lambda_{y}}{2}\right) - V_{t} \cdot cos\left(\frac{\lambda_{y}}{2}\right)$$

$$\cdot \left[sin(\lambda_{z}) \left(\frac{1}{2} - \frac{1}{\lambda_{z}^{2}} \right) + \frac{cos(\lambda_{z})}{\lambda_{z}} \right]$$

$$(2c-126)$$

$$S_{1} = 4 \cdot \frac{\phi_{1D}(y = 0.5)}{\lambda_{z}} \left[\sin(\lambda_{z}) + 2 \cdot \left\{ \frac{1}{\left(1 - \frac{2}{C_{r2}}\right)} \left(\frac{\Delta}{\Delta_{1} + \Delta} - 1\right) + \delta' \right\} \right] \cdot \cos\left(\frac{\lambda_{y}}{2}\right) - V_{T} \cdot \cos\left(\frac{\lambda_{y}}{2}\right)$$

$$\cdot \left[\sin(\lambda_{z}) \left(\frac{1}{2} - \frac{1}{\lambda_{z}^{2}}\right) + \frac{\cos(\lambda_{z})}{\lambda_{z}} \right]$$

$$(2c-127)$$

From (2c-118),(2c-123), and (2c-127), into (2c-114), we got

$$\phi_{1D}\left(y_{c}\right)\left(1+F_{1}+\delta\right)-\cos\left(\lambda_{y}\cdot y_{c}\right)\cdot\sum_{N=0}^{1}\left(\frac{1}{\Delta R_{1}}\cos\left(\lambda_{zN}\cdot z_{c}\right)\cdot\frac{4}{\lambda_{z}}\right]\sin\left(\lambda_{z}\right)+2\cdot\left\{\frac{1}{\left(1-\frac{2}{C_{r_{2}}}\right)}\left(\frac{\Delta}{\Delta_{1}+\Delta}-1\right)+\delta'\right\}\right)\cdot\cos\left(\frac{\lambda_{y}}{2}\right)+\sum_{N=0}^{1}\left(\frac{1}{\Delta R_{0}}\cdot\sin\left(\lambda_{zN}\cdot z_{c}\right)\cdot\frac{4}{\lambda_{z}^{2}}\cdot\left[\sin\left(\lambda_{z}\right)-\lambda_{z}\cdot\cos\left(\lambda_{z}\right)\right]\cdot\cos\left(\frac{\lambda_{y}}{2}\right)\right)\cdot D_{omin}\left(\frac{\Delta}{\left(1-\frac{1}{C_{r_{1}}}\right)+\Delta\cdot\left(1-\frac{1}{C_{r_{2}}}\right)}-\delta_{1}\right]$$

(2c-128)

207

$$S_T = V_T \cos(\lambda_y \cdot y_c) \cos\left(\frac{\lambda_y}{2}\right) \cdot \sum_{N=0}^{1} \cos(\lambda_{zN} \cdot z_c) \cdot D_{o \min}$$
 (2c-129)

$$\phi_{1D}(y_c) \left[1 - S_{gs}' + \delta_3 \right] + S_T = V_T \ln \left[\frac{Q_{inv}}{(W_{EIN}) \cdot (\alpha \cdot H_{EIN}) \cdot n_i} \right] S_{ds}$$
 (2c-130)

$$\phi_{1D}(y_c) = \frac{1}{\left[1 - S_{gs}' + \delta_3\right]} \left(V_T \ln \left[\frac{Q_{inv}}{(W_{FIN}) \cdot (\alpha \cdot H_{FIN}) \cdot n_i}\right] - S_{ds} - S_T\right)$$
(2c-131)

At the value of the threshold charge we can write threshold voltage as,

$$V_{TH} = \phi_{ms} + \frac{1}{\left[1 - S_{gs}' + \delta_3\right]} \left(V_T \ln \left[\frac{Q_{TH}}{(W_{FIN}) \cdot (\alpha \cdot H_{FIN}) \cdot n_i}\right] - S_{ds} - S_T\right)$$
(2c-132)

$$\delta_3 = F_1 + \delta - \delta_c \tag{2c-133}$$

$$\delta_{c} = \cos(\lambda_{y} \cdot y_{c}) \cdot \cos\left(\frac{\lambda_{y}}{2}\right) \cdot \left[\sum_{n=0}^{1} \frac{\delta'}{\Delta R_{1}} \cos(\lambda_{zn} \cdot z_{c}) \cdot \frac{4}{\lambda_{zn}} \left[\sin(\lambda_{zn}) + 2 \cdot \left\{\frac{1}{\left(1 - \frac{2}{C_{r2}}\right)} \left(\frac{\Delta}{\Delta_{1} + \Delta} - 1\right)\right\}\right] + \left[\sin(\lambda_{zn}) \left(\frac{1}{2} - \frac{1}{\lambda_{zn}^{2}}\right) + \frac{\cos(\lambda_{zn})}{\lambda_{zn}}\right] + \left[\sum_{n=0}^{1} \frac{\delta_{1}}{\Delta R_{0}} \cdot \sin(\lambda_{zn} \cdot z_{c}) \cdot \frac{4}{\lambda_{zn}^{2}} \cdot \left[\sin(\lambda_{zn}) - \lambda_{zn} \cdot \cos(\lambda_{zn})\right]\right]$$

As $V_{GS2} \approx \phi_{ms}$, δ_3 will go to zero as shown in Fig. (2c-10),

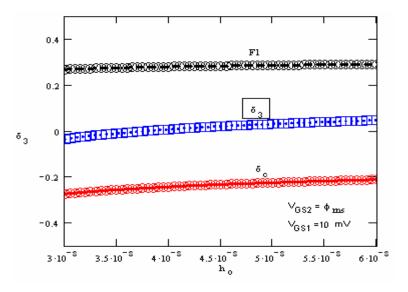


Fig. 2c-10 Demonstration of the value of δ_3

Finally we can write the threshold voltage as,

$$\phi_{1D}(y_c) = \frac{1}{\left[1 - S_{gs}\right]} \left(V_t \ln \left[\frac{Q_{TH}}{(W_{FIN}) \cdot (\alpha \cdot H_{FIN}) \cdot n_i}\right] - S_{ds} - S_T\right)$$
(2c-135)

where,

$$S_{gs}' = \cos(\lambda_{y} \cdot y_{c}) \cdot \cos\left(\frac{\lambda_{y}}{2}\right) \cdot \sum_{n=0}^{1} \left[\frac{\frac{1}{\Delta R_{1}} \cos(\lambda_{zn} \cdot z_{c}) \cdot \frac{4}{\lambda_{zn}}}{\left[\sin(\lambda_{zn}) + 2 \cdot \left\{\frac{1}{\left(1 - \frac{2}{C_{r2}}\right)} \left(\frac{\Delta}{\Delta_{1} + \Delta} - 1\right)\right\}\right] + \left[\sin(\lambda_{zn}) \left(\frac{1}{2} - \frac{1}{\lambda_{zn}^{2}}\right) + \frac{\cos(\lambda_{zn})}{\lambda_{zn}}\right]\right] + \left[\frac{1}{\Delta R_{o}} \cdot \sin(\lambda_{zn} \cdot z_{c}) \cdot \frac{4}{\lambda_{zn}^{2}} \cdot \left[\sin(\lambda_{zn}) - \lambda_{zn} \cdot \cos(\lambda_{zn})\right] \cdot \frac{1}{\left(1 - \frac{1}{C_{r2}}\right)} \cdot \frac{\Delta}{\Delta_{1} + \Delta}\right]$$

$$(2c-136)$$

To get the value for the threshold charge, we have found that both S_{ds} , and S_{gs} at long channel device goes to zero, as shown in Fig.(2c-11). Also there is a negligible difference between S_{gs} , and S_{gs} .

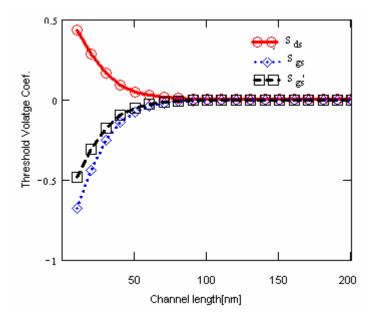


Fig. 2c-11 The long channel threshold voltage parameters

and so on the long channel threshold voltage, can be written as

$$V_{TH} = \phi_{ms} + V_T \cdot \ln \left(\frac{Q_{TH}}{n_i \cdot W_{FIN} \cdot H_{FIN}} \right)$$
 (2c-136)

By substracting the V_{TH} for long channel devices from the general model in Eq.(2c-135), the roll-off can be written as,

$$\Delta V_{\text{TH}} = V_T \cdot \ln \left(\frac{Q_{th}}{n_i \cdot W_{FIN} \cdot H_{FIN}} \right) \cdot \left[\frac{1}{1 - S_{gs}} - 1 \right] - S_{ds}$$
 (2c-137)

The DIBL effect can be calculated using the same manner as for both DG, and GAA MOSFETs, by substracting the V_{TH} at high V_{ds} value from the V_{TH} at low V_{ds} value.

References

- [1] S. B. Park, Y. W. Kim, Y. G. Ko, K. I. Kim, I. K. Kim, H. S. Kang, J. O. Yu, and K. P. Suh, "A 0.25-μm, 600 MHz, 1.5-V, fully depleted SOI CMOS 64-bit microprocessor," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1436–1445, 1999.
- [2] R. Chau, J. Kavalieros, B. Roberds, A. Murthy, B. Doyle, D. Barlage, M. Doczy, and R. Arghavani, "A 50 nm depleted-substrateCMOStransistor (DTS)," in *IEDM Tech. Dig.*, 2001, pp. 621–623.

- [3] T. Ernst, D. Muteanu, S. Cristoloveanu, T. Ouisse, N. Hefyene, S. Horiguchi, Y. Ono, Y. Takahashi, and K. Murase, "Ultimately thin SOI MOSFETs: Special characteristics and mechanisms," in *Proc. IEEE Inte. SOI Conf.*, 1999, pp. 92–93.
- [4] B. Cheng, B. Maiti, S. Samavedam, J. Grant, B. Taylor, P. Tobin, and J. Mmogab, "Metal gates for advanced sub-90 nm SOI CMOS technology," in *Proc. IEEE Int. SOI Conf.*, 2001, pp. 91–92. 354–359, Feb. 2000.
- [5] T. Ernst and S. Cristoloveanu, "Buried oxide fringing capacitance: A new physical model and its implication on SOI device scaling and architecture," in *Proc. IEEE Int. SOI Conf.*, 1999, pp. 38–39.
- [6] J. P. Colinge, X. Baie, V. Bayot, and E. Grivei, "A silicon-on-insulator quantum wire," *Solid-State Electron.*, vol. 39, no. 1, pp. 49–51, 1996.
- [7] X. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y. K. Choi, K. Asano, V. Subramanian, T. J. King, J. Bokor, and C. Hu, "Sub 50 nm FinFET: PMOS," in *IEDM Tech. Dig.*, 1999, pp. 67–70.
- [8] Z. Jiao and C. A. T. Salama, "A fully depleted _-channel SOI nMOSFET," in *Proc. Electrochem. Soc. 2001–3*, 2001, pp. 403–408.
- [9] J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, "Silicon-on-insulator gate-all-around device," in *IEDM Tech.Dig.*, 1990, pp. 595–598.
- [10] D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, "A fully depleted leanchannel transist or (DELTA)-a novel vertical ultra thin SOI MOSFET," in *IEDM Tech. Dig.*, 1989, pp. 833–836.
- [11] F.-L. Yang "25 nm CMOS Omega FETs," in *IEDM Dig.*, 2002, pp. 255–258.

- [12] J. T. Park, J. P. Colinge, and C. H. Diaz, "Pi-gate SOI MOSFET," *IEEE Electron Device Lett.*, vol. 22, pp. 405–406, Aug. 2001.
- [13] H. Takato *et al.*, "Impact of surrounding gate transistor (SGT) for ultrahighdensity LSIs," *IEEE Trans. Electron Devices*, vol. 38, pp. 573–577, Mar. 1991.
- [14] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 18, pp. 74–76, Feb. 1997.
- [15] Christopher P. Auth, and James D. Plummer, "Scaling Theory for Cylindrical, Fully-Depleted, Surrounding-Gate MOSFET's", IEEE ELECTRON DEVICE LETTERS, VOL. 18, NO. 2, FEBRUARY 1997
- [16] W. Xiong, J. W. Park, and J. P. Colinge, "Corner effect in multiple-gate SOI MOSFETs," in *Proc. Int. SOI Conf.*, 2003, pp. 111–113.
- [17] Weize Xiong, Gabriel Gebara, Joyti Zaman, Michael Gostkowski, Billy Nguyen, Greg Smith, David Lewis, C. Rinn Cleavelin, Rick Wise, Shaofeng Yu, Michael Pas, Tsu-Jae King, and J. P. Colinge, "Improvement of FinFET Electrical Characteristics by Hydrogen Annealing", IEEE ELECTRON DEVICE LETTERS, VOL. 25, NO. 8, AUGUST 2004
- [18] Jae Young Song, Woo Young Choi, Ju Hee Park, Jong Duk Lee, and Byung-Gook Park," Optimization of Gate-All-Around (GAA) MOSFETs", IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 5, NO. 3, MAY 2006
- [19] Sharma, A. K., Zaidi, S. H., Lucero, S., Brueck, S. R. J., and Islam, N. E., 2004: "Mobility and Transverse Electric Field Effects in Channel Conduction of Wrap-around-gate Nanowire MOSFETs", *IEE Proc.* Circuits, Devices and Systems, 151

- [20] Benjamín Iñiguez,, Tor A. Fjeldly, Antonio Lázaro, François Danneville, and M. Jamal Deen, "Compact-Modeling Solutions For Nanoscale Double-Gate and Gate-All-Around MOSFETs", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 9, SEPTEMBER 2006.
- [21] S. Xiong, T. J. King and J. Bokor, "A comparison study of symmetric ultrathin body double gate devices with metal source/drain and doped source/drain, " IEEE Trans. On Electron Devices, vol. 52, no. 8, pp. 18591867, August 2005.
- [22] Y. Taur, X. Liang, W. Wang and H. Lu, "A continuous analytic drain current model for double gate MOSFETs," IEEE Electron Device Letters, vol. 25, no. 2, pp. 107-109, February 2004.
- [23] A. Ortiz-Conde, F. J. Garcia-Sanchez and J. Muci, "Rigorous analytic solution for the drain current of undoped symmetric dual gate MOSFETs," Solid-State Electronics 49, 2005
- [24] D. Jimenez, B. Iniguez, J. Sune, L. F. Marsal, J. Pallares, J. Roig and D. Flores, "Continuous analytic current voltage model for surrounding gate MOSFETs," IEEE Electron Device Letters, vol. 251, no. 8, pp. 571-573, August 2004.
- [25] D. Jimenez, J. J. Saenz, B. Iniguez, J. Sune, L. F. Marsal and J. Pallares, "Unified compact model for the ballistic quantum wire and quantum well metal oxide semiconductor field effect transistor," Journal of Applied Physics, vol. 94, no. 2, pp. 1061-1068, July 2003.
- [26] A. Toriumi, M. Iwase, and M. Yoshimi, "On the performance limit for Si MOSFET: Experimental study," *IEEE Trans. Electron Devices*, vol. 35, pp. 999–1003, 1988.

- [27] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *J. Appl. Phys.*, vol. 76, pp. 4879–4890, 1994.
- [28] M. S. Lundstrom, "Elementary scattering theory of the MOSFET," *IEEE Electron Device Lett.*, vol. 18, pp. 361–363, 1997.
- [29] S. Datta, F. Assad, and M. S. Lundstrom, "The Si MOSFET from a transmission viewpoint," *Superlattices and Microstructures*, vol. 23, pp. 771–780, 1998.
- [30] D. Vasileska, D. K. Schroder, and D. K. Ferry, "Scaled silicon MOSFET's: Degradation of the total gate capacitance," *IEEE Trans. Electron Devices*, vol. 44, pp. 584–587, 1997.
- [31] T. Ando, A. B. Fowler, and F. Stern, "Electronic properties of two-dimensional systems," *Rev. Mod. Phys.*, vol. 54, pp. 437–672, 1982.
- [32] M. Lundstrom, *Fundamentals of Carrier Transport*. Reading, MA: Addison-Wesley, 1990.
- [33] Ren Z, Venugopal R, Datta S, Lundstrom M, Jovanovic D, Fossum J. The ballistic nanotransistor: a simulation study. IEDM Tech Digest 2000:715–8.
- [34] Timp G, Bude J, Bourdelle KK, Garno J, Ghetti A, Gossmann H, et al. The ballistic nano-transistor. IEDM Tech Digest 1999:55–8.
- [35] Natori K. "Ballistic metal-oxide-semiconductor field effect transistor", J Appl Phys 1994;76(8):4879–90.
- [36] Assad F, Ren Z, Datta S, Lundstrom M, Bendix P. "Performance limits of silicon MOSFETs", IEDM Tech Digest 1999:547–50.
- [37] Assad F, Ren Z, Vasileska D, Datta S, Lundstrom M. "On the performance limits for Si MOSFETs: a theoretical study", IEEE Trans Electron Dev 2000;47(1):232–40.

- [38] Naveh Y, Likharev KK. "Modeling of 10-nm-scale ballistic MOSFETs", IEEE Electron Dev Lett 2000
- [39] Chang L, Hu C. "MOSFET scaling into the 10 nm regime", Superlattices Microstruct 2000;28(5/6):351–5.
- [40] Lundstrom M, Ren Z. "Essential physics of carrier transport in nanoscale MOSFETs", IEEE Trans Electron Dev 2002
- [41] Lundstrom MS. "Fundamentals of carrier transport", 2nd ed. Cambridge, UK: Cambridge University Press; 2000.
- [42] Ferry DK, Goodnick SM. "Transport in nanostructures", Cambridge University Press; 1997.
- [43] Naveh Y, Likharev KK. "Shrinking limits of silicon MOSFETs: numerical study of 10 nm scale devices", Superlattices Microstruct 2000;27(2/3):111–23.
- [44] Ge L, Fossum J. "Physical compact modeling and analysis of velocity overshoot in extremely scaled CMOS devices and circuits", IEEE Trans Electron Dev 2001;48(9):2074–80.
- [45] X. P. Liang and Y. Taur, A 2-d analytical solution for SCEs in DG MOSFETs, *IEEE Transactions on Electron Devices*, vol. 51, no. 9, pp. 1385-1391, September 2004.
- [46] Q. Chen, E. M. Harrell, II, and J. D. Meindl "A Physical Short-Channel Threshold Voltage Model for Undoped Symmetric Double-Gate MOSFETs," *IEEE Trans. on Electron Devices*, Vol. 50, no. 7, July 2003
- [47] C. P. Auth and J. D. Plummer, "A simple model for threshold voltage of surrounding-gate MOSFET's," *IEEE Trans. Electron Devices*, vol. 45, pp. 2381–2383, Nov. 1998.

- [48] Sang-Hyun Oh, Don Monroe, and J. M. Hergenrother "Analytic Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs ",IEEE ELECTRON DEVICE LETTERS, VOL. 21, NO. 9, SEPTEMBER 2000.
- [49] G. Pei, J. Kedzierski, P. Oldiges, M. Ieong, and E. C.-C. Kan," FinFET Design Considerations Based on 3-D Simulation and Analytical Modeling", *IEEE Trans. on Electron Devices*, vol. 49, no. 8, pp. 1411-1419, August 2002
- [50] Hamdy Abd-Elhamid, Benjamin Iñiguez, David Jiménez, Jaume Roig, Josep Pallarès, and Lluís F. Marsal, "Two-Dimensional Analytical Threshold Voltage Roll-Off and Subthreshold Swing Models For Undoped Cylindrical Gate All Around MOSFET," Solid-State Electronics, vol. 50, no. 5, pp. 805-812, May 2006
- [51] Hamdy Abd-Elhamid, Benjamin Iñiguez, David Jiménez, Jaume Roig, Josep Pallarès, and Lluís F. Marsal "*Threshold voltage, and subthreshold swing for GAA MOSFET*", Euro-SOI, Grenoble, France. 19-21 March, 2006
- [52] Hamdy Abd-Elhamid, Benjamin Iñiguez, David Jiménez, Josep Pallarès, and Lluís F. "Compact Modelling for Surrounding Gate MOSFETs" International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES 2005), Krakow (Poland), June 2005.
- [53] Benjamin Iñiguez, Hamdy Abd-Elhamid, David Jiménez, "Compact Model of Multiple-gate SOI MOSFETs" ES 2005 NSTI Nanotechnology Conference and Trade Show Nanotech 2005 May 8-12, 2005 Anaheim Marriott & Convention Center Anaheim, California, U.S.A, workshop on compact modelling, WCM,.

- [54] C. H. Wann, K. Noda, T. Tanaka, M. Yoshida and C. Hu,"A comparative study of advanced MOSFET concepts," *IEEE Trans. Electron Devices*,vol. 43, no.10, pp. 1742-1753, Oct. 1996.
- [55] H. Takato, K. Sunouchi, N. Okabc, A. Nitayama, K. Hieda, F. Horiguchi, and F. Masuoka,"High performance CMOS surrounding gate transistor (SGT) for ultra high density LSIs", in *IEDM Tech. Dig.*, 1988, pp. 222-225.
- [56] J. T. Park and J. P. Colinge,"Multiple-gate SOI MOSFETs: Device design guidelines", *IEEE Trans. Electron Devices*, vol.49, no. 12, pp. 2222-2229, December, 2002.
- [57] S. –H. Oh, D. Monroe and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs", *IEEE Electron Device Letters*, vol. 21, no. 9, pp. 445–447, September. 2000.
- [58] Benjamin Iñíguez, David Jiménez, Jaume Roig, and Hamdy A. Hamid "Explicit Continous Model for Long-Channel Undoped Surrounding Gate MOSFETs," *IEEE Trans. on Electron Devices*, vol. 52, no. 8, pp. 1868-1872, August 2005.
- [59] H. C. Poon, L. D. Yau, R. L. Johnston, and D. Beecham, "DC model for short-channel IGFETs," in *IEDM Tech. Dig.*, 1974, pp. 156–159.
- [60] Kranti A, Haldar S, Gupta RS An accurate 2D analytical model for short channel thin film fully depleted cylindrical/surrounding gate (CGT/SGT) MOSFET MICROELECTRONICS JOURNAL 32 (2A-4): 305-313 APR 2001
- [61] Kranti A, Haldar S, Gupta RS Analytical model for threshold voltage and I-V characteristics of fully depleted short channel cylindrical/surrounding gate

- MOSFET *MICROELECTRONIC ENGINEERING* 56 (3-4): 241-259 AUG 2001
- [62] H. Lu and Y. Taur, "Physics-based, non charge-sheet compact modeling of Double-Gate MOSFET", Prof. of the Workshop on Compact Modeling (*WCM*), Anaheim, CA (USA), May 2005.
- [63] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, Y. Amimoto, and T. Itoh, "Analytical surface potential expression for thin-film double-gate SOI MOSFETs," *Solid-State Electron.*, vol. 37, no. 2, pp. 327–332, 1994.
- [64] D. J. Frank "Power constrained CMOS scaling Limits", IBM J. RES. & DEV. Vol.. 46 no. 2/3 March/May 2002
- [65] Y. Ma, Z. Li, L. Liu, L. Tian, and Z. Yu, "Effective density-of-states approach to QM correction in MOS structure," *Solid-State Electron.*, vol. 44, pp. 401–407, 2000.
- [66] Y.Yuan Taur, "An analytical solution to a double-gate MOSFET with undoped body," *IEEE Electron Device Lett.*, vol. 21, pp. 245–247, May 2000.
- [67] D. Jiménez, J. Sáenz, B. Iñíguez ,J. Suñé "Modeling of Nanoscale Gate-All-Around MOSFETs" IEEE Electron Device Letters, Vol. 25, no. 5, May 2004
- [68] Tor A. Fjeldly, and Michael Shur "Threshold Voltage Model and subthreshold Regime of Operation of Short-Channel MOSFET's," *IEEE Trans. on Electron Devices*, vol. 40, no.1, pp. 137-145, January 1993.
- [69] L. Ge and J. G. Fossum, "Analytical Modeling of Quantization and Volume Inversion in Thin Si-Film DG MOSFETs," *IEEE Trans. on Electron Devices*, vol. 49, no. 2, pp. 287-294, February 2002.

- [70] G. Chindalore, S. A. Hareland, S. Jallepalli, A. F. Tasch, Jr., C. M. Maziar, V. K. F. Chia, and S. Smith, "Experimental Determination of Threshold Voltage Shifts Due to Quantum Mechanical Effects in MOS Electron and Hole Inversion Layers," *IEEE Electron Device Letters*, vol. 18, no. 5, pp. 206-208, May 1997.
- [71] A. Kumar, Jakub Kedzierski, and Steven E. Laux, "Quantum-Based Simulation Analysis of Scaling in Ultrathin Body Device Structures," *IEEE Trans. on Electron Devices*, vol. 52, No. 4, pp. 614-617, April 2005.
- [72] Q. Chen, B. Agrawal and J. D. Meindl, "A Comprehensive Analytical Subthreshold Swing Model for Double-Gate MOSFETs," *IEEE Trans. on Electron Devices*, vol. 49, no. 6, pp. 1086-1090, June 2002.
- [73] B. Lee "First order system least squares fo ellepitic problems with Robin Boundary conditions", *SIAM Journal on numerical analysis*, vol.37, no.1, pp.70-104, 1999.
- [74] Klaus Kirsten, Spectral functions in mathematics and physics.
- [75] A. Rahman and M. S. Lundstrom, "A Compact Scattering Model for the Nanoscale Double-Gate MOSFET" *IEEE Trans. on Electron Devices*, Vol. 49, No. 3, March 2002 481
- [76] S.-H. Oh, *PhD Thesis*, Stanford University, June 2001
- [77] J. Guo, PhD Thesis, Purdue University, 2002
- [78] Q. Chen, *PhD Thesis*, Georgia Institute of Technology, January 2003
- [79] The International Technology Roadmap for Semiconductors (2001). http://public.itrs.net
- [80] Hamdy Abd-Elhamid, Benjamin Iñiguez, and Jaume Roig" NATO International Advanced Research Workshop "Nanoscaled Semiconductor-

- on-Insulator Structures and Devices" 15-19 October 2006, Sudak, Crimea, Ukraine
- [81] Hamdy Abd-Elhamid, Benjamin Iñiguez, and Jaume Roig, "Analytical Model of the Threshold Voltage and Subthreshold Swing of Undoped Cylindrical Gate All Around Based MOSFETs", IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 54, No.3, March 2007
- [82] Hamdy Abd-Elhamid, Benjamin Iñiguez, and Jaume Roig "Two-Dimensional Analytical Threshold Voltage and Subthreshold Swing Models of Undoped Symmetric Double Gate MOSFETs", IEEE TRANSACTIONS ON ELECTRON DEVICES, accepted
- [83] Hamdy Abd-Elhamid, Benjamin Iñiguez, and Jaume Roig "A 2-D Short Channel Effects Model For Undoped Double Gate MOSFET, Euro-SOI, Leuven, Belgium. 17-19 January, 2007
- [84] F. Asaad, Z. Ren, and S. Daatta, "Performance limits of Silicon MOSFET", *IEEE Trans. on Electron Devices*, Vol. 47, No. 1, pp. 232-240, January 2000.
- [85] D. J. Frank, and R. H. Dennard," Device Scaling Limits of Si MOSFETs and Their Application Dependencies", *Proc. of the IEEE*, Vol. 89, No. 3, March 2001.
- [86]http://www.efunda.com/math/bessel/bessel.cf
- [87]http://mathworld.wolfram.com/ModifiedBesselFunctionoftheFirstKind.html [88]http://www.vibrationdata.com/
- [89] A.Albiol, L. Torres, and E. J. Delp. Audio to the rescue. *OE magazine*, 4(1):17-21, January 2004.
- [90] L.Jodar and J. Sastre. Asymptotic expressions of normalized Laguerre matrix polynomials on bounded intervals. *Utilities Mathematical*, 65:3-31, 2004.

- [91] J. Sastre and L. Jodar. Asymptotics of the modified Bessel and the incomplete gamma matrix functions. *Applied Math. Letters*, 16:815-820, 2003.
- [92] E. Kamke, Differentialgleichungen Losungsmethoden und Losungen, Lepizig, Germany: Akademische Verlagsgesellschaft Becker & Erler Kom.-GEM, 1942.
- [93] Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2861–2869, December. 2001.
- [94] K. Suzuki, Y. Tosaka and T. Sugii, "Analytical threshold voltage model for short-channel Double-Gate SOI MOSFETs," IEEE Trans. On Electron Devices, vol. 43, no. 7, pp. 1166-1168, July 1996.
- [95] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI MOSFET's," *IEEE Trans. on Electron Devices*, vol. 40, no. 12, pp. 2326-2329, Dec. 1993.
- [96] P. Francis, A. Terao, D. Flandre and F. Van de Wiele. "Modeling of Ultrathin Double-Gate nMOS/SOI Transistors", *IEEE Transactions on Electron Devices*, vol.41, no.5, May 1994.
- [97] D. Munteanu, J. L. Autran, X. Loussier X, S. Harrison S, R. Cerutti and T. Skotnicki, *Solid-State Electronics*, vol. 50, no. 4, pp. 680-686, April 2006
- [98] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.
- [99]Hamdy Abd-Elhamid, Benjamin Iñiguez, Jaume Roig" A 3-D Analytical Physically-Based Model for SCEs in Undoped FinFETs," IEEE TRANSACTIONS ON ELECTRON DEVICES, submitted

- [100] Hamdy Abd-Elhamid, Benjamin Iñiguez, Jaume Roig "A 3-D Analytical Physically-Based Model for the Subthreshold Swing in Undoped FinFETs", IEEE TRANSACTIONS ON ELECTRON DEVICES, submitted
- [101] Hamdy Abd-Elhamid, Benjamin Iñiguez, and Jaume Roig "3-D Analytical Models for the Short-Channel Effect Parameters in Undoped FinFET Devices", Tenth International Conference on Modeling and Simulation of Microsystems, workshop on compact modelling, WCM, May 20-24, 2007 Santa Clara Convention Center, California, U.S.A.
- [102] H.-S. P. Wong, D. J. Frank, and P. M. Solomon, "Device design considerations for double-gate, ground-plane, and single-gated ultrC-thin SOI MOSFETs at the 25 nm channel length generation," in *IEDM Tech. Dig.*, 1998, pp. 407–410.
- [103] L. Chang and C. Hu, "MOSFET scaling into the 10 nm regime," in *Nanoelectronics Workshop*, 2000, pp. 351–355.
- [104] L. Chang, S. Tang, T.-J. King, J. Bokor, and C. Hu, "Gate length scaling and threshold voltage control of double-gate MOSFETs," in *IEDM Tech.Dig.*, 2000, pp. 719–722.
- [105] D. Hisamoto, W.-C. Lee, J. Kedzierski, E. Anderson, H. Takeuchi, K. Asano, T.-J. King, J. Bokor, and C. Hu, "A folded-channel MOSFET for deep-sub-tenth micron era," in *IEDM Tech. Dig.*, 1998, pp. 1032–1034.
- [106] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," in *IEDM Tech. Dig.*, 1999, pp. 67–70.

- [107] Seung-Hwan Kim, Jerry G. Fossum, and Vishal P. Trivedi, "Bulk Inversion in FinFETs and Implied Insights on Effective Gate Width", *IEEE Trans. on Electron Devices*, vol. 52, no. 9, pp. 1993-1997, September 2005.
- [108] M. R.Rahman, "Design and Fabrication of Tri-Gated FinFET", 22nd Annual Microelectronic Engineering Conference, May 2004
- [109] D. Hisamoto, et al., "FinFET—A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans.Electron Devices*, vol. 47, pp. 2320-2325, Dec. 2000.
- [110] L. Mathew, et al., "CMOS vertical multiple independent gate field effect transistor-MIGFET" *IEEE Int. SOI Conf.*, 187-189, Oct. 2004.
- [111] D. M. Fried, J. S. Duster, and K. T. Kronegay, "High performance p-type independent-gate FinFETs," *IEEE Electron Device Lett*, pp. 199-201, Apr. 2004.
- [112] E.-J. Yoon, et al., "Sub 30nm multi-bridge-channel MOSFET (MBCFET) with metal gate electrode for ultra high performance application," *IEDM Tech.Dig.*, Dec. 2004, pp. 627-630.
- [113] David M. Fried, Jon S. Duster, and Kevin T. Kornegay," High-Performance P-Type Independent-Gate FinFETs", *IEEE Electron Device Letters*, vol.. 25, no. 4, April 2004
- [114] D. M. Fried, "A sub 40-nm body thickness n-type FinFET," in *Proc.Device Research Conf.*, June 2001, pp. 24–25.
- [115] T. Rudenko, N. Collaert, S. De Gendt, V. Kilchytska, M. Jurczak and D. Flandre, Effective mobility in FinFET structures with HfO2 and SiON gate dielectrics and TaN gate electrode, *Microelectronic Engineering*, vol. 80, no. 386-389, June 2005.

- [116] V. Kilchytska, D. Lederer, N. Collaert, J. P. Raskin and D. Flandre, Accurate effective mobility extraction by split C-V technique in SOI MOSFETs: Suppression of the influence of floating-body effects, *IEEE Electron Device Letters*, vol. 26, no. 10, pp. 749-751, October 2005
- [117] D. Lederer, V. Kilchytska, T. Rudenko, N. Collaert, D. Flandre, A. Dixit, K. De Meyer, and J. P. Raskin, FinFET analogue characterization from DC to 110 GHz, *Solid-State Electronics*, vol. 49, no. 9, pp. 1488-1496, September 2005.
- [118] J. P. Raskin, T. M. Chung, V. Kilchytska V, D. Lederer and D. Flandre, Analog/RF performance of multiple gate SOI devices: Wideband simulations and characterization, *IEEE Trans. on Electron Devices*, vol. 53, no. 5, pp. 1088-1095, May 2006
- [119] B. Yu, "FinFET scaling to 10 nm gate length," in *IEDM Tech. Dig.*, Dec. 2002, pp. 251–254.
- [120] E. Nowak, "A functional FinFET-DGCMOS SRAM cell," in *IEDMTech*. *Dig.*, Dec. 2002, pp. 411–414.
- [121] Y. Tosaka, K. Suzuki, and T. Sugii, "Scaling-parameter-dependent model for subthreshold swing *S* in double-gate SOI MOSFET's," *IEEE Electron Device Letters*, vol. 15, no. 11, pp. 466-468, Nov. 1994.
- [122] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: a new device with greatly enhanced performance," *IEEE Electron Device Letters*, vol. ED-8, pp. 410-412, Sep. 1987.
- [123] Hamdy Abd-Elhamid, Benjamin Iñiguez, and Jaume Roig, "Scalability Limits Of Multiple Gate MOSFET Devices", Solid-State Electronics, in press, April, 2007.

- [124] Hamdy Abd-Elhamid, Benjamin Iñiguez, and Jaume Roig, MOS Modeling and Parameter Extraction Working Group MOS-AK/ESSDERC/ESSCIRC Workshop Compact Modeling for Emerging Technologies, September 2006 Montreux Convention and Exhibition Center "scalability limits of multiple gate MOS devices
- [125] Benjamin Iñiguez et. al., "EXPLICIT CONTINUOUS MODEL FOR LONG CHANNEL UNDOPED SURROUNDING GATE MOSFETS", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 52, NO. 8, AUGUST 2005
- [126] Hamdy Abd-Elhamid, Benjamin Iñiguez, David Jiménez, Josep Pallarès, and Lluís F. Marsal "A simple model of the nanoscale double gate MOSFET based on the flux method" physica status solidi (c) Volume 2, Issue 8, Date: May 2005, Pages: 3086-3089
- [127] Hamdy Abd-Elhamid, Benjamin Iñiguez, David Jiménez, Josep Pallarès, and Lluís F. "Quasi Ballistic Model of double gate MOSFET", First Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits Granada, SPAIN. 19-21 January, 2005
- [128] D. Jiménez, B. Iñiguez, J. Suñé, L. F. Marsal, J. Pallarès, J. Roig, and D. Flores, "Continuous analytic current-voltage model for surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 571–573, Aug. 2004.
- [129] C.-K. Park, C.-Y. Lee, K. Lee, B.-J. Moon, Y. H. Byun, and M. Shur, "A unified current-voltage model for long-channel nMOSFETs," *IEEE Trans. Electron Devices*, vol. 38, pp. 399–406, Feb. 1991.
- [130] M. S. Shur, T. A. Fjeldly, T. Ytterdal, and K. Lee, "Unified MOSFET model," *Solid State Electron.*, vol. 35, no. 12, pp. 1795–1802, Dec. 1992.

- [131] B. Iñíguez, L. F. Ferreira, B. Gentinne, and D. Flandre, "A physically based C -continuous fully-depleted SOI MOSFET model for analog applications," *IEEE Trans. Electron Devices*, vol. 43, no. 4, pp. 568–575, Apr. 1996.
- [132] Slavica Malobabic, Adelmo Ortiz-Conde, and Francisco J. García Sánchez, "Modeling the Undoped-Body Symmetric Dual-Gate MOSFET", Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems, Dominican Republic, Nov.3-5, 2004
- [133] J. He J, X. Xi, C.H. Lin, M. Chan, A. Niknejad, C. Hu, "A non-Charge-Sheet Analytic Theory for Undoped Symmetric Double-Gate MOSFET from the Exact Solution of Poisson's Equation using SSP Approach," *NSTI-Nanotech 2004*, Boston, Massachusetts, vol. 2, pp. 124-127, March 7-11, 2004.
- [134] D. Jiménez et al., *Proc. ESSDERC Conf. 2003*, pp. 187-190.
- [135] J. P. McKelvey et al., *Phys. Rev.*, vol. 123, pp. 51–57, 1961.
- [136] Y. Taur, *Fundamentals of VLSI Devices*, Cambridge University, Cambridge University Press, 1998.
- [137] K. Natori, Ballistic metal-oxide-semiconductor field effect transistor, *J. Appl. Phys.*, 76, pp. 4879-4890, 1994.
- [138] J.S. Blakemore, Solid-State Electronics, vol. 25, pp. 1067, 1982.
- [139] A. Lochtefield and D. Antoniadis, On experimental determination of carrier velocity in deeply scaled NMOS: How close to the thermal limit?,?*IEEE Electron Dev. Lett.*, 22, pp. 95-97, 2001.
- [140] Moor's law]G.E. Moore, "Progress in digital integrated electronics," *IEDM Tech. Digest*, pp. 11-13, 1975.

- [141] R. Landauer, "Conductance determined by transmission: probes and quantised constriction resistance," J. Phys. Condens. Matter, 1, pp. 8099-8109, 1989.
- [142] Hong-Nien Lin, Hung-Wei Chen, Chih-Hsin Ko, Chung-Hu Ge, Horng-Chih Lin,
- Tiao-Yuan Huang, and Wen-Chin Lee, "Channel Backscattering Characteristics of Uniaxially Strained Nanoscale CMOSFETs", IEEE ELECTRON DEVICE LETTERS, VOL. 26, NO. 9, SEPTEMBER 2005
- [143] Ming-Jer Chen, Huan Tsung, Kuo Chaun Huang, Po Nien Chen, Chih Sheng Chang, and Cralos H. Diaz, "Temperature Dependent Channel Backscattering Coefficients in nanoscale MOSFETs", IEDM, 2002
- [144] Kah Wee Ang, Hock Chun Chin, King Jien, Ming Fu Li, Ganesh Samudra, and Yee Chia Ya, "Carrier Backscattering Characteristics of strained N-MOSFET Featuring Silicon Carbon Source/Drain Regions", ESSDERIC, 2006, Swisszerland.
- [145] HASANUR R. KHAN, DRAGICA VASILESKA AND S.S. AHMED, "Modeling of FinFET: 3D MC Simulation Using FMM and Unintentional Doping Effects on Device Operation", Journal of Computational Electronics 3: 337–340, 2004
- [146] T. Poiroux, M. Vinet, O. Faynot, J. Widiez1, J. Lolivier, T. Ernst, B. Previtali, S. Deleonibus," Multiple gate devices: advantages and challenges", Microelectronic Engineering 80 (2005) 378–385
- [147] Seung-Hwan Kim, Jerry G. Fossum, and Vishal P. Trivedi," Bulk Inversion in FinFETs and Implied Insights on Effective Gate Width", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 52, NO. 9, SEPTEMBER 2005

- [148] J. G. Fossum, J.-W. Yang, and V. P. Trivedi, "Suppression of corner effects in triple-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 24, no.12, pp. 745–747, Dec. 2003.
- [149] Zhichao Lu, and Jerry G. Fossum, "Short Channel Effects in Independent Gate FinFET", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 28, NO. 2, FEBRUARY 2007
- [150] Byung Kil Choi, Kyoung Rok Han, Young Min Kim, Youn June Park and Jong Ho Lee, "Threshold Voltage Modeling of Body Tied FinFETs", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 54, NO. 3, MARCH 2007
- [151] Vishal P. Trivedi, and Jerry G. Fossum, "Quantum-Mechanical Effects on the Threshold Voltage of Undoped Double-Gate MOSFETs", IEEE ELECTRON DEVICE LETTERS, VOL. 26, NO. 8, AUGUST 2005
- [152] Vivek Venkataraman, Susheel Nawal, and M. Jagadesh Kumar, "Compact Analytical Threshold Voltage Model of Nanoscale Fully Depleted Strained Si on Silicon Germanium on Insulator (SGOI) MOSFETs", IEEE ELECTRON DEVICE LETTERS, VOL. 54, NO. 3, MARCH 2007