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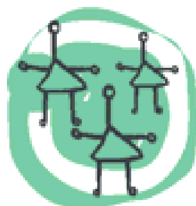
Study and Modeling of Multi-Gate Transistors in the Context of CMOS Technology Scaling



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PH. D. THESIS

Study and Modeling of Multi-Gate Transistors in the Context of CMOS Technology Scaling

FERNEY ALVEIRO CHAVES ROMERO

2012

In Partial Fulfillment of the Requirements of the PhD Program in Electronics Engineering for the Degree of Doctor

Universitat Autònoma de Barcelona

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El Dr. David Jiménez Jiménez, profesor Agregado, y el Dr. Jordi Suñé Tarruella, Catedrático de Universidad, del Departament d'Enginyeria Electrònica de la Universitat Autònoma de Barcelona,

CERTIFICAN

Que la memoria "Study and Modeling of Multi-Gate Transistors in the Context of CMOS Technology Scaling" que presenta Ferney Alveiro Chaves Romero para optar al grado de Doctor en Ingeniería Electrónica, ha sido realizado bajo su dirección.

Bellaterra, marzo de 2012

Dr. David Jiménez Jiménez   Dr. Jordi Suñé Tarruella

Cuando bordeamos un abismo y la noche es tenebrosa,

el jinete sabio suelta las riendas

y se entrega al instinto del caballo.

Armando Palacio Valdés (1853-1938)

Literato español

Agradecimientos

Después de los muchos esfuerzos que he tenido que realizar para llegar a este punto y así ver culminada una etapa más en mi camino por la académica y la investigación, quiero ante todo agradecer a Dios por sostenerme, darme la sabiduría y el aliento necesario cuando más lo he necesitado. Gracias Señor por no permitirme desfallecer.

Agradezco a mis padres Mary y Alberio y a mis hermanos, quienes siempre han creído en mí y de quienes siempre he recibido apoyo incondicional. A mi hijo Sebastian, quien ha sido testigo viviendo conmigo pacientemente este proceso y quien siempre me ha llenado de fuerza para seguir. A mi Jimena hermosa por su apoyo diario, por la fe que ha tenido en mí y por su compañía durante la culminación de este doctorado. Los amo.

Gracias también a mis amigos, los de Barcelona y los de Colombia, por animarme cuando me sentía cansado y por hacer de mi vida fuera de mi casa algo más placentero.

También un agradecimiento especial a David por sus valiosos aportes, enseñanzas, discusiones, paciencia y sobre todo por su amistad. Así mismo a Jordi por su dirección, apoyo y por la amabilidad que siempre me demostró. Gracias a Andrés y a Fran de la Universidad de Granada por los aportes y la colaboración que siempre estuvieron dispuestos a brindarme.

Finalmente debo agradecer el apoyo del Ministerio Español de Ciencia y Tecnología bajo contrato No. TEC2009-09350 (parcialmente financiado por el programa FEDER de la Unión Europea) y a la financiación por parte de la Generalitat de Catalunya con el programa *Distinción de la Generalitat de Catalunya para la promoción de la investigación universitaria*, bajo el proyecto S08811001G *Nanoelectrónica.*

Ferney A. Chaves
Barcelona, marzo 2012

SUMMARY

The scaling of the conventional MOSFETs has led these devices to the nanoscale to increase both the performance and the number of components per chip. In this process, the so-called "Short Channel Effects" have arisen as a limiting factor. To extend the use of the bulk MOSFETs, the most effective ways of suppressing such effects are the reduction of the gate oxide thickness and increasing of the channel doping concentration. When the gate oxide thickness is reduced to a few atomic layers, quantum mechanical tunneling is responsible of a huge increase in the gate leakage current impairing the normal operation of MOSFETs. This has made mandatory the use of high permittivity materials or high-κ as gate dielectrics.

Despite the proposed solutions, reduction of the physical dimensions of the conventional MOSFETs cannot be maintained. To keep the technological trend, new MOSFET structures have been suggested such as ultra-thin body Multi-Gate MOSFETs. In particular, the Double-Gate MOSFETs is considered as a promising MG structure for its several qualities and advantages in scaling.

This thesis focuses on the modeling of Double-Gate MOSFET and, in particular, on the modeling of the gate leakage current critically affecting the power consumption. First we develop a compact quantum model for both the electrostatic potential and the electric charge in symmetric double-gate MOSFET with undoped thin body. Then, this quantum model is used to propose an analytical compact model for the direct tunnelling current with SiO_2 as gate dielectric, firstly, and later assuming a dual layer consisting of a SiO_2 interfacial layer and a high-κ material.
Finally, an accurate method for the calculation of the gate tunnelling current is developed. It is based on Absorbing Boundary Conditions techniques and, more specifically, on the Perfectly Mached Layer (PML) method.

This thesis is motivated by the recommendations given by the "International Technology Roadmap of Semiconductors" (ITRS) about the need for the modeling and simulation of multi-gate semiconductor structures.

RESUM

L'escalat dels transistors MOSFET convencionals ha portat a aquests dispositius a la nanoescala per incrementar tant les seves prestacions com el nombre de components per xip. En aquest process d'escalat, els coneguts "Short Channel Effects" representen una forta limitació. La forma més efectiva de suprimir aquests efectes i així estendre l'ús del MOSFET convencional, és la reducció del gruix de l'òxid de porta i l'augment de la concentració de dopants al canal. Quan el gruix d'òxid de porta es redueix a unes quantes capes atòmiques, apareix l'efecte túnel mecano-quàntic d'electrons, produint un gran augment en el corrent de fuita, perjudicant la normal operació dels MOSFETs. Això ha fet obligatori l'ús de materials d'alta permitivitat o materials high-κ en els dielèctrics de porta.

Tot i les solucions proposades, la reducció de les dimensiones físiques del MOSFET convencional no pot ser mantinguda de forma indefinida i per mantenir la tendència tecnològica s'han suggerit noves estructures com ara MOSFETs multi-porta de cos ultra-prim. En particular, el MOSFET de doble porta és considerat com una estructura multi-porta prometedora per les seves diverses qualitats i avantatges en l'escalat.

Aquesta tesi s'enfoca en la modelització de dispositius MOSFET de doble porta i, en particular, en la modelització del corrent túnel de porta que afecta críticamente al consum de potència del transistor. Primerament desenvolupem un model quàntic compacte tant per al potencial electrostàtic com per a la càrrega elèctrica en el transistor de doble-porta simètric amb cos no dopat. Després, aquest model quàntic s'utilitza per proposar un model analític compacte per al corrent túnel directe amb SiO_2 com dielèctric de porta, primerament, i després amb una doble capa composta de SiO_2 com a capa interfacial i un material "high-κ". Finalment es desenvolupa un mètode precís per calcular el corrent túnel de porta. El mètode es basa en l'aplicació de condicions de frontera absorbents i, més especificament, en el mètode PML.

Aquesta tesi està motivada per les recomanacions fetes pel "International Technology Roadmap of Semiconductors" (ITRS) sobre la necessitat existent de modelatge i simulació d'estructures semiconductores multi-porta.

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CHAPTER 1.

Introduction and Background

1.1 CMOS Technology Scaling

Throughout recent history, silicon-based microelectronics has experienced tremendous growth and performance improvements since the innovative concept of integrated circuit (IC) was invented by J. Kilby in late 1950's [1]. The computational power is enhanced at a tremendous rate with cost reduction, resulting in incredible reduction of cost-per-computation with higher computational performance in data processing and memory functions. In 1965, Gordon Moore made a very famous and important observation: the complexity of ICs approximately doubles every year (Moore later refined the period to two years) [2]. This estimation is the well known "Moore's Law" [3]. Over the past four decades, the scaling of the conventional metal-oxide-semiconductor field-effect transistor (MOSFET) has been accomplished with technology innovations and led the device dimensions well into the nanometer era, allowing a great integration as shown in Figure1-1.

"Scaling" refers to reduction of the lateral geometric dimensions of devices and interconnect. This evolution of process technologies has brought new benefits. However, the performance improvement by scaling the dimension of conventional bulk MOSFET is approaching a limit.

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. As the channel length is reduced (scaling) to increase both the operation speed and the number of component per chip, "Short Channel Effects" (SCEs) arise as hurdles. In particular some different SCEs can be distinguished:

threshold voltage roll-off, subthreshold swing degradation, drain-induced barrier lowering (DIBL), surface scattering, velocity saturation, impact ionization and hot electrons.

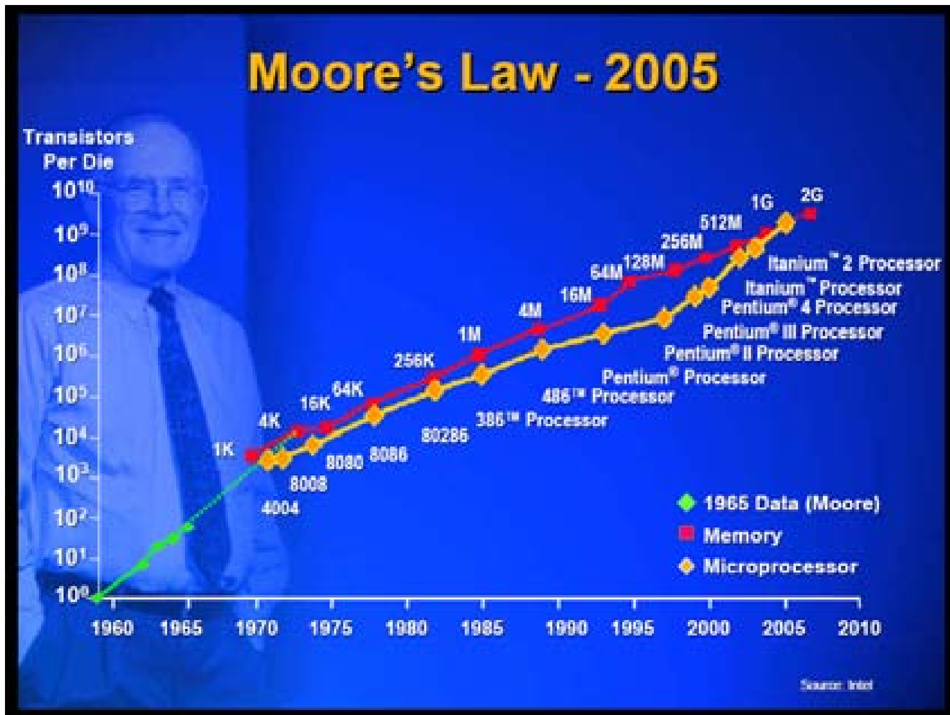


Figure 1-1
Moore's Law has delivered exponential increases in the number of transistors integrated into microprocessors and other leading platform ingredients. [Source: Intel Corporation]

In conventional bulk MOSFET technologies, the most effective ways of suppressing SCE are the reduction of the gate oxide thickness (T_{ox}) and the increase of the channel doping concentration (N_A) [4, 5]. The former is aimed to increase the gate capacitance, thus enhancing the electrostatic control of the gate over the channel. The latter is desired to minimize depletion depths of the source-to-channel and drain-to-channel junctions, preventing the junction electric fields from penetrating too much into the channel and forming an undesired leakage path relatively distant from the gate.

Researchers in [6, 7] have shown that the gate oxide scaling to thicknesses close to a few atomic layers gives rise to quantum mechanical tunneling producing a sharp increase in gate leakage currents. The gate leakage current is the current flowing into the gate of the transistor also called the tunneling current. Other major causes of concern in further reduction of the SiO_2 thickness include increased polysilicon gate depletion and gate dopant penetration into the channel region, which leads to questions regarding dielectric integrity, reliability, and stand-by power consumption. With scaling, gate leakage has increased to undesirable values and will continue to increase at a much higher rate mandating the use of dielectric materials with high electric permittivity or high-κ dielectrics [8]. This allows the actual thickness of the gate dielectric to be increased while still maintaining the same electric field in the channel.

Specifically, the International Technology Roadmap for Semiconductors (ITRS) [9] identifies that for 32nm technology node, gate oxide thickness is nearly to 1nm. The direct tunneling current through the gate oxide of such small thickness may become more of a problem especially in terms of the stand-by power consumption [10]. In addition, abnormal degradation of the drive current has been experimentally observed when the gate oxide thickness is less than 1.3nm [11]. Meanwhile, the channel doping concentration required for SCE control in sub-32 nm bulk MOSFETs is expected to be a few times 10^{18} cm^{-3} and above [12, 13]. These extremely high doping levels will lead to i) severe degradation of the carrier mobility as the impurity scattering becomes dominant, ii) severe threshold voltage variations because of random microscopic fluctuations of dopant atoms both in numbers and in placement [14, 15], and iii) increased junction band-to-band tunneling current [16]. In view of the fundamental nature of both the gate direct tunneling current and random dopant fluctuations, it becomes problematic to scale bulk MOSFETs much deeper into the sub-32 nm technology regime while preserving good immunity to SCEs.

On the other hand, a major portion of semiconductor device production, nowadays, is devoted to digital logic and one key theme is continued scaling of the MOSFETs for leading-edge logic technology in order to maintain historical trends of improved device performance. This scaling is driving the industry toward a number of major technological innovations, including material and process changes such as high-κ gate dielectric, metal gate electrodes, strained silicon channels, etc., and in the near future, new structures such as ultra-thin body fully depleted SOI, multi-gate (MG) MOSFETs (Fig. 1-2), such as FinFETs and alternate high-mobility channel materials [17] are expected to be

incorporated. In particular, the Double-Gate MOSFETs is a promising MG structure for its several qualities and advantages in scaling which will be described in the next section. Besides, Double-Gate (DG) MOSFET actually is the central device studied in this thesis.

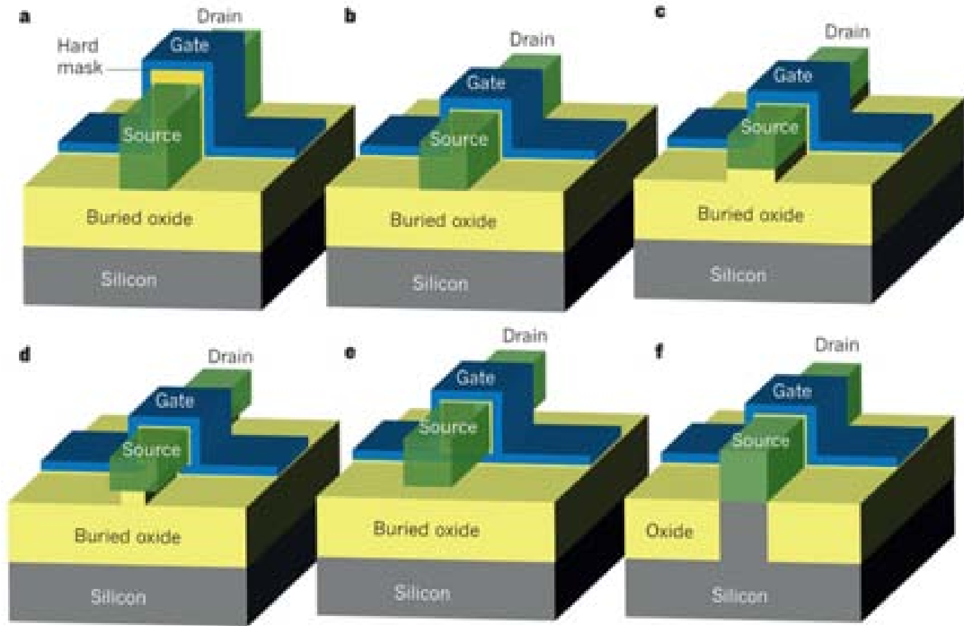


Figure 1-2
The different ways in which the gate electrode can be wrapped around the channel region of a transistor are shown. **a**, A silicon-on-insulator (SOI) fin field-effect transistor (FinFET). The 'hard mask' is a thick dielectric that prevents the formation of an inversion channel at the top of the silicon 'fin'. Gate control is exerted on the channel from the lateral sides of the device. **b**, SOI triple-gate (or tri-gate) MOSFET. Gate control is exerted on the channel from three sides of the device (the top, as well as the left and right sides). **c**, SOI Π-gate MOSFET. Gate control is improved over the tri-gate MOSFET shown in **b** because the electric field from the lateral sides of the gate exerts some control on the bottom side of the channel. **d**, SOI Ω-gate MOSFET. Gate control of the bottom of the channel region is better than in the SOI Π-gate MOSFET. The names Π gate and Ω gate reflect the shape of the gates. **e**, SOI gate-all-around MOSFET. Gate control is exerted on the channel from all four sides of the device. **f**, A bulk tri-gate MOSFET. Gate control is exerted on the channel from three sides of the device (the top, the left and the right). In this case, there is no buried oxide underneath the device. Ref. [17].

Implementation of fully depleted SOI and multi-gate will be challenging. Since such devices will typically have lightly doped channels, the threshold voltage will not be controlled by the channel doping. The problems associated

with high channel doping and stochastic dopant variation in planar bulk MOSFETs will be alleviated, but numerous new challenges are expected. These innovations are expected to be introduced at a rapid pace, and hence understanding, modeling, and implementing them into manufacturing in a timely manner is expected to be a major issue for the industry [9].

For the long-term, when the transistor gate length is projected to scale below 10 nm and body (fin) thicknesses below 5 nm, the impact of quantum confinement effects on such thin devices should be well understood.

The numerical modeling and simulation of semiconductor structures by computer is a useful resource for the study and understanding of several electronic phenomena, of which would otherwise have an incomplete knowledge. In fact, in most cases, the simulated devices are ahead of the current technology. Computer simulation allows, in a fast way, to explore new geometries and sizes that could be manufactured in the future.

Modeling and simulation in semiconductor technology is one of the few enabling methodologies that can reduce development cycle times and cost. One of the topical areas of Modeling and Simulation of the ITRS is the *Device Modeling* which presents as a difficult challenge the nanoscale devices simulation capability: methods, models and algorithms. In particular it is necessary modeling for gate stacks with ultra-thin/high-κ dielectrics for several channel materials with respect to electrical permittivity, built-in charge, influence on workfunction by interface interaction with metals, reliability, carrier transport and tunneling currents. As mentioned before, gate dielectrics have become so thin that tunneling gate current is today an important design factor. Therefore, a comprehensive quantum modeling of the entire gate stack (channel, dielectric and electrode) is needed to represent the behavior of oxides that are only a few atomic layers thick. Since the adoption of high-κ dielectrics and metals, details of tunneling and charge transport in the dielectric, effective dielectric constant of complex dielectric stacks, interfaces states and dipoles, and charge and trap distribution in high-κ materials must be included urgently. Simulations must also be applicable beyond standard planar CMOS.

1.2 Double-Gate MOSFET

DG CMOS offers distinct advantages for scaling to very short gate lengths. Furthermore, adoption of gate dielectrics with permittivity substantially greater than that of SiO_2 (high-κ materials) may be deferred if a DG architecture is employed. Recently, through use of delta devices, now commonly referred to as the FinFET [18], significant advantages in DG device technology and performance have been demonstrated. Fabrication of FinFET is very close to that conventional CMOS process, with only minor disruptions, offering the potential for a rapid deployment to manufacturing. Planar products designs have been converted to FinFET without disruption to the physical area, thereby demonstrating its compatibility with today's planar CMOS design methodology and automation techniques [19].

CMOS technology scaling has traversed many anticipate barriers over the past two decades to rapidly progress from 2μm to sub 100nm rules, as discussed in the article by Chuang et.al. [20]. Two obstacles, namely subthreshold and gate dielectric leakage become the dominant barrier for further CMOS scaling, even for highly leakage-tolerant applications such as microprocessors.

DG MOSFET is composed of a thin silicon body sandwiched between the gate dielectrics and contacts as Figure 1-3 shows. We will consider that the two gates of the DG device are shorted giving rise to numerous advantages, such as greater control of the gate over the channel thereby reducing SCEs [21, 22]. Such SCE limit the minimum channel length at which a FET is electrically well behaved. Unlike bulk MOSFETs which require very high channel doping ($\sim10^{18}/cm^3$ for sub-100nm devices), thin body DG MOSFETs show good short-channel behavior even with undoped silicon as a channel.

As the channel length of a bulk MOSFET is reduced, the drain potential begins to strongly influence the channel potential, leading to an inability to shut off the channel current with the gate. This SCE is mitigated by use of thin gate oxide (to increase the influence of the gate on the channel) and thin depletion depth below the channel to the substrate, to shield the channel from the drain. Gate oxide thickness has been reduced to the point where, at sub-100 nm CMOS, the power drain from gate leakage is comparable to the power used for switching of circuits. Thus, further reduction of the thickness would lead to unreasonable power increases. Alternatively, further decrease of the depletion

region degrades gate influence on the channel and leads to a slower turn on of the channel region.

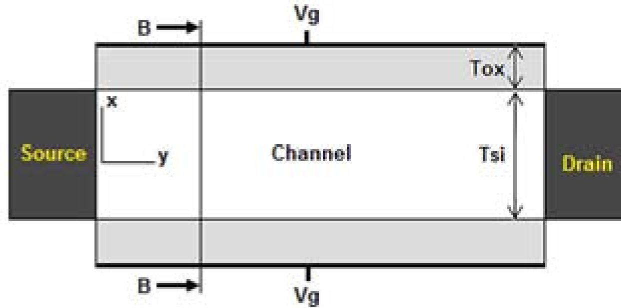


Figure 1-3
Cross section scheme of the symmetrical DG MOSFET considered in this work.

In DGs, the longitudinal electric field generated by the drain is better screened from the source end of the channel due to proximity to the channel of the second gate, resulting in reduced SCE such as the DIBL and improved subthreshold swing (S). Therefore, as CMOS scaling becomes limited by leakage currents, DG offers the opportunity to proceed beyond the performance of single-gate (SG) bulk-silicon. Figure 1-4 shows MEDICI-predicted DIBL and subthreshold swing for bulk silicon and (symmetrical) DG devices as a function of the effective channel length L_{eff}. Both the DIBL and subthreshold swing for the DG device are dramatically improved relative to those of the bulk-silicon counterpart [19].

From a bulk-silicon device design perspective, increased body doping concentration could be employed to reduce DIBL; however, at some point it would also increase the subthreshold swing, thereby requiring higher threshold voltage to keep the subthreshold current adequately low. Similarly, decreasing the body doping concentration could improve the subthreshold swing but degrade DIBL. Hence a compromise is necessary for the bulk-silicon device design. Note that, for a scaled bulk-silicon device, a highly doped channel must be used to control severe SCEs, and lower S for extremely short L_{eff} could not be achieved by use of low channel doping.

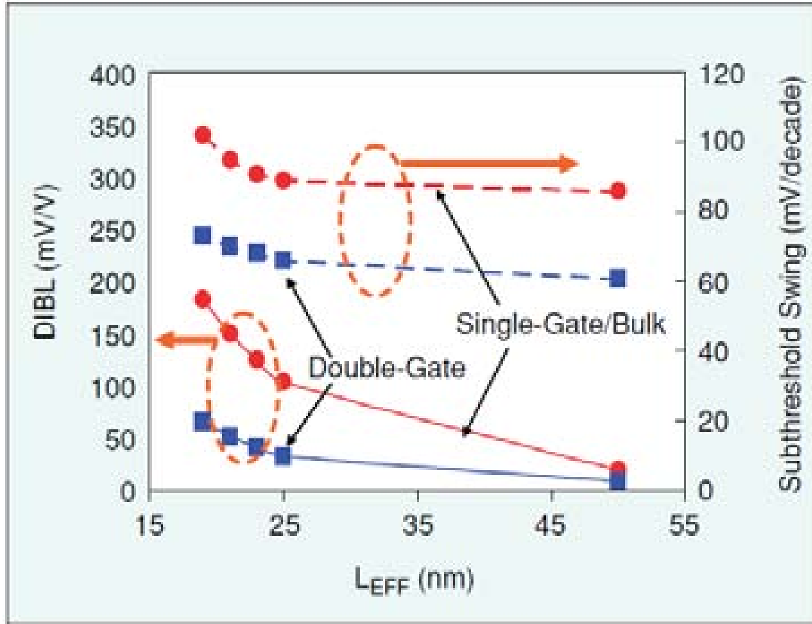


Figure 1-4
MEDICI-predicted DIBL and subthreshold swing versus effective channel length for DG and bulk-silicon nFETs. The DG device is designed with an undoped body and a near-mid-gap gate material [19].

In Figure1-5 simulations of the drain current I_{DS} of DG and SG MOSFETs shows the steeper turn on of the DG, which results from the gate coupling advantage previously discussed. This property enables the use of lower threshold voltage for the DG for a given off-current. As a direct result, higher drive currents at lower power-supply voltages V_{DD} are attainable.

1.3 Thesis Organization

This thesis is organized in the following way: in Chapter 2 a compact quantum model for both the electrostatic potential and electric charge in thin-film symmetric double-gate MOSFET is presented. This is done from a classical model proposed by Taur [23]. That quantum model is used in Chapter 3 to propose an analytical compact model for the gate tunnelling current with silicon dioxide as a gate dielectric, relying on a quadratic approximation to the

conduction band profile and the well-known WKB approximation to the transmission probability. The Chapter 4 is devoted to extend the compact model presented in Chapter 3 to take account a dielectric stack consisting of a SiO_2 interfacial layer and a high permittivity dielectric material (high-κ). Up to this point the electronic states are considered fully bounded, namely, wave function penetration is not allowed into the gate dielectrics. Finally and thinking in future research for applied to other MG transistors such as cylindrical gate or quadruple gate, an accurate method for the calculation of the gate tunnelling in DG MOSFETs is studied and developed in Chapter 5, which is based on Absorbing Boundary Conditions techniques and, more specifically, on the Perfectly Mached Layer (PML) method.

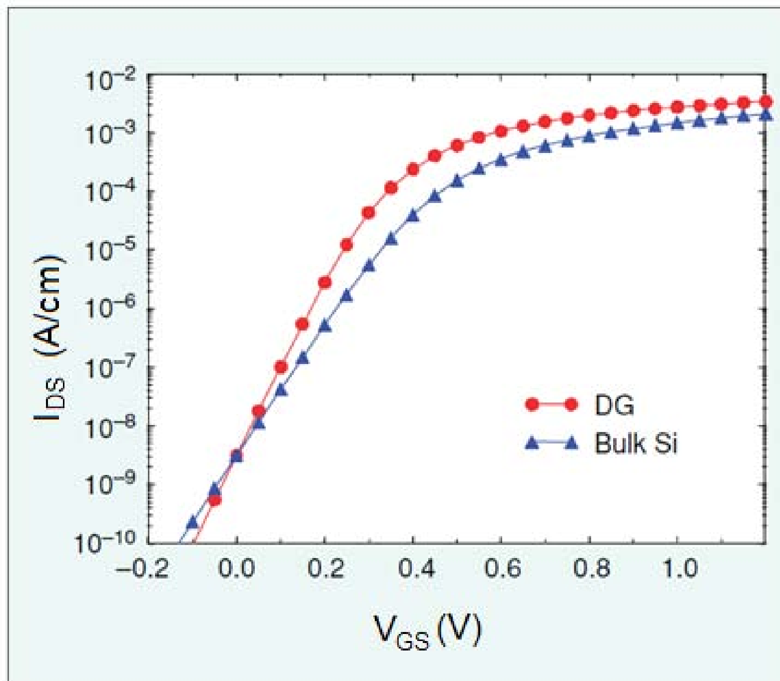


Figure 1-5
Simulation of DG and single-gate FETs, designed for equal subthreshold current density at V_{GS} = 0 V, illustrates the gain in drive current from improved channel control of the DG FET. Both gates contribute to control of the channel potential in subthreshold, while in the bulk case the gate must compete with the influence of the substrate [19].

CHAPTER 2.

Explicit Quantum Potential and Charge Model for Double-gate MOSFETs

2.1 Outline

In this chapter, a compact quantum model for both the electrostatic potential and electric charge in thin-film symmetric double-gate MOSFET with undoped body is presented. As a novelty, both the resulting potential and charge have explicit expressions on bias and geometrical parameters. A comparison has been made between self-consistent numerical solutions of Schrödinger-Poisson equations and our model results with close agreement. Finally, the range of validity of the presented model is discussed.

MULTI-GATE metal-oxide-semiconductor field-effect transistors (MOSFETs), and in particular, DG MOSFETs, are a topic of intense interest in order to improve the performance of complementary metal-oxide-semiconductor (CMOS) devices [24]. Theoretically, DG MOSFETs can be scaled to significantly shorter channel length than bulk MOSFETs for a given oxide thickness [25] keeping a better control of short channel effects (SCE). Because of such advantage, these devices are potential candidates as building blocks for nanoscale circuits in the midterm, thus making the development of computer-aided-design (CAD) compatible models an important issue. When the gate

length is scaled below deep submicron dimensions very large normal electric fields at the Si/SiO_2 interface may appear. Therefore a significant bending of the energy bands at the Si/SiO_2 interface is produced and the potential well becomes narrow enough to quantize the motion of inversion layer carriers in the direction perpendicular to the interface [26]. Due to the quantization, the energy levels are splitted into subbands and the lowest of the allowed energy levels for electrons in the well does not coincide with the bottom of the conduction band. On the other hand, the electron density does not reach its maximum at the Si/SiO_2 interface as semiclassical theory predicts [27, 28], but at some distance inside the semiconductor. Thus, a reliable compact model for DG MOSFETs must take into account quantum effects. Several works have been devoted to model the electrostatic features of DG-MOSFETs, which can be categorized as: i) models relying on a purely classical description [23] and [29-31], which do not treat QM effects, ii) 1D and 2D self-consistent models which numerically solve the coupled Schrödinger and Poisson equations [32-34], ideal for quantitative understanding of the physics behind, but not suitable for compact modeling; iii) models using a perturbation theory -even in strong inversion region-, for which the structural confinement is taken into account, but which are not suitable to deal with the strong field dependence [35, 36]; and iv) models based on a quantum-mechanical variational approach [37], where the potential depends on the inversion charge density, and thus requires the solution of an implicit equation.

In this chapter, we extend the state-of-the-art by proposing a simple model for the electrostatics of undoped DG-MOSFETs, which reproduces the results obtained from accurate self-consistent quantum-mechanical (QM) solutions, showing an explicit dependence with the gate voltage and geometrical parameters, thus making it suitable for compact modeling.

2.2 Classical Potential Model

This section shows the main features of a classical model for the potential and charge of the DG-MOSFET developed by Taur [6]. Figure 2-1 illustrates the geometric parameters such as the silicon thickness T_{si} and SiO_2 dielectric thickness T_{ox} and the schematic band diagrams of the device. Same voltage is applied to the two gates having the same work function. At zero gate voltage V_g, the position of the silicon bands is largely determined by the gate work function.

This is because as long as the thin silicon is lightly-doped and the depletion charge is negligible, the bands remain essentially flat throughout the thickness of the film. Since there is no contact to the silicon body, the energy levels are referenced to the electron quasi-Fermi level or the conduction band of the n+ source–drain (not shown), represented by the long dotted line in Figure 2-1. As the gate voltage increases toward the threshold voltage in Figure 2-1b, mobile charge or electron density becomes appreciable and the conduction band of the silicon body moves toward the conduction band of the source-drain. The silicon bands will just float to the position dictated by the gate work function.

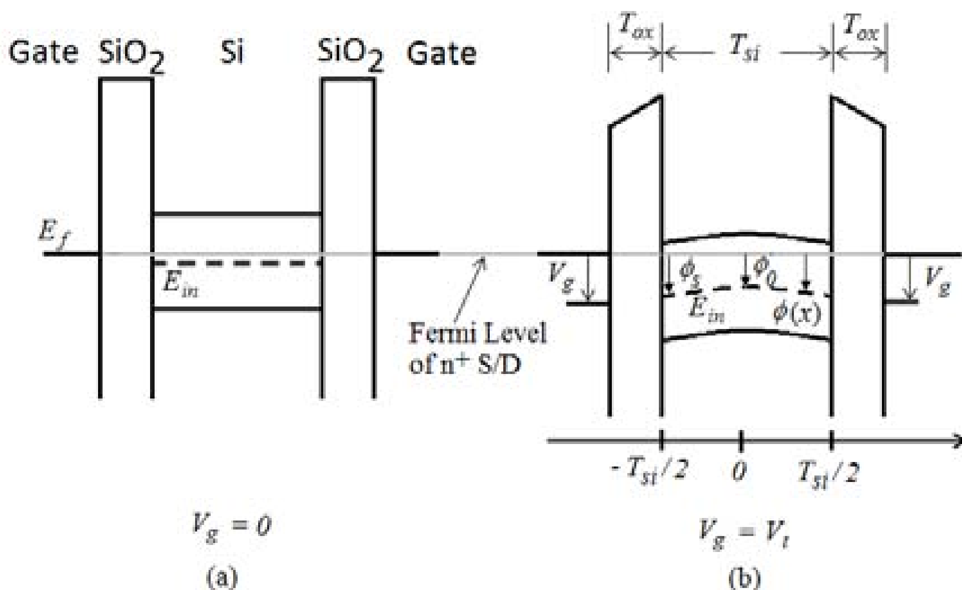


Figure 2-1
Schematic band diagrams of a symmetric, undoped double-gate nMOSFET. At zero gate voltage (a), the silicon bands are flat for the gate work function (slightly toward n than the midgap work function) shown in the example. Near the threshold voltage (b), the conduction band of the silicon body at the surface is bent to near the conduction band of the n source-drain (long dotted line).

By defining the coordinates and potential as in Figure 2-1, one can write Poisson's equation for the silicon region with only the mobile charge (electron) density as

$$\frac{d^2\phi}{dx^2} = \frac{q}{\epsilon_{si}} n_i e^{\phi/V_T} \tag{2.1}$$

where q is the electronic charge, ϵ_{si} is the permittivity of the silicon, n_i is the intrinsic carrier density, $V_T = k_B T/q$ is the thermal voltage with the Boltzmann's constant k_B and the absolute temperature T. Here, we consider an nMOSFET with $\phi/V_T \gg 1$ so that the hole density is negligible.

Using the symmetry boundary condition $d\phi/dx|_{x=0} = 0$ and integrating (2.1) twice, the electrostatic potential can be expressed as

$$\phi(x) = \phi_0 - 2V_T ln\left[cos\left(\sqrt{\frac{qn_i}{2\epsilon_{si}V_T}}e^{\phi_0/2V_T}x\right)\right] \tag{2.2}$$

valid for the entire range $-T_{si}/2 \leq x \leq T_{si}/2$ and where all the potentials are referenced to the source Fermi level. Here, $\phi_0 \equiv \phi(x = 0)$ is the potential at the center of the silicon film, to be solved later as a function of V_g.

The surface potential $\phi_s \equiv \phi(x = T_{si}/2)$ is then given by

$$\phi_s = \phi_0 - 2V_T ln\left[cos\left(\sqrt{\frac{qn_i}{2\epsilon_{si}V_T}}e^{\phi_0/2V_T}\frac{T_{si}}{2}\right)\right] \tag{2.3}$$

and it is also related to V_g and T_{ox} through the boundary condition at the Si/SiO_2 interface:

$$V_g - \Delta\varphi - \phi_s = \frac{\epsilon_{si}}{\epsilon_{ox}}T_{ox}\frac{d\phi}{dx}\bigg|_{x=\frac{T_{si}}{2}} = \frac{T_{ox}}{\epsilon_{ox}}\sqrt{2\epsilon_{si}kTn_i(e^{\phi_s/V_T} - e^{\phi_0/V_T})} \tag{2.4}$$

Here $\Delta\varphi$ is the work function difference between the gate electrode and intrinsic silicon. Given V_g, Eqs. (2.3) and (2.4) are coupled equations that can be solved for ϕ_s and ϕ_0.

The sheet density of mobile charge can be obtained from the Gauss's law and $Q_{ch} = 2\epsilon_{si}(d\phi/dx)_{x=t_{si}/2}$ (the factor of two arises from the two surfaces).

Although this is a simple physics-based model for DG, it requires numerical calculations, Newton-Raphson type, to solve the highly nonlinear Eq. (2.4). On the other hand, quantum corrections should arise when very thin Si-film is considered. For instance, Figure 2-2 shows, for two different geometries, the

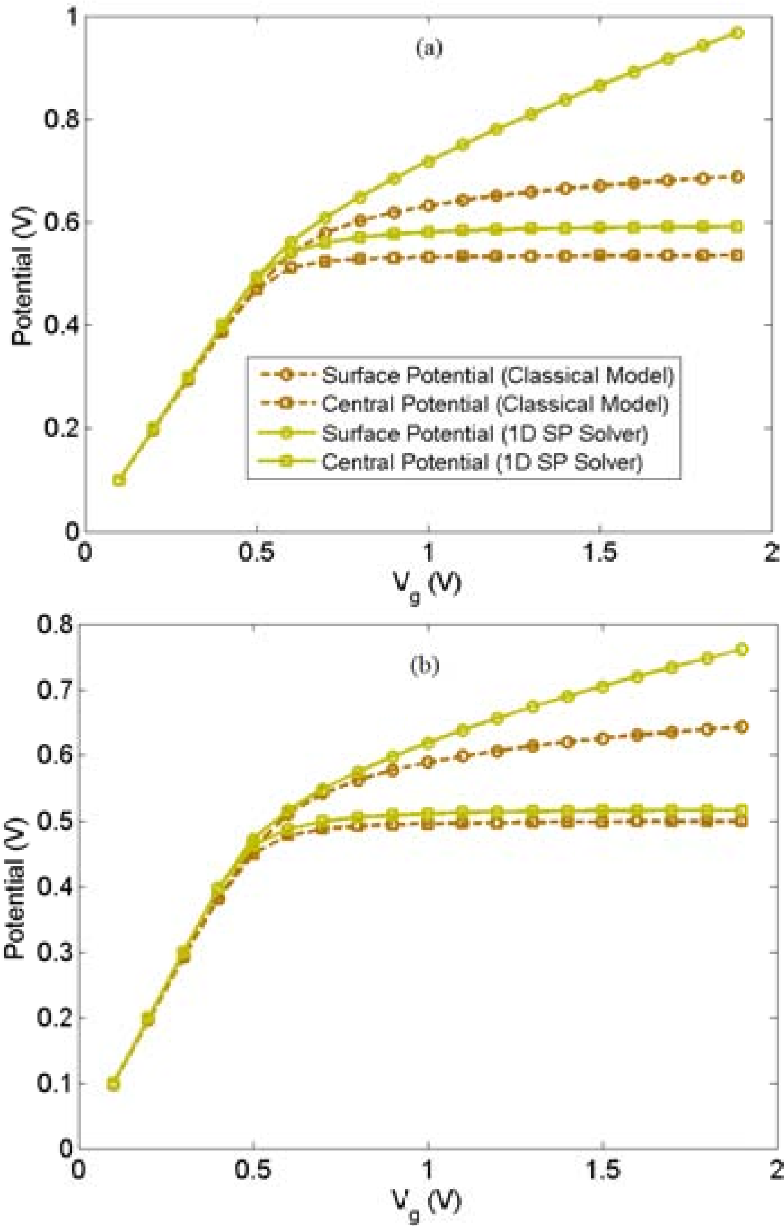


Figure 2-2
Comparison between classical [6] and quantum [38] models of the potentials in DG MOSFETs for (a) $T_{si} = 5$nm, $T_{ox} = 1$nm; (b) $T_{si} = 10$nm, $T_{ox} = 3$nm.

differences between the potentials (surface and central) when these are calculated using the classical model described in this section and when those are calculate by means of a self-consistent 1D Schrödinger-Poisson (SP) solver [38]. Also, Figure 2-3 shows those differences to the mobile charge density Q_{ch} as a function of V_g. Clearly, the differences correspond to the quantization or discretization of electronic states and to the decreasing of the density of states (DOS). In next section we propose a simple compact model for the potentials and charge which takes into account the quantum effects present in DG MOSFETs.

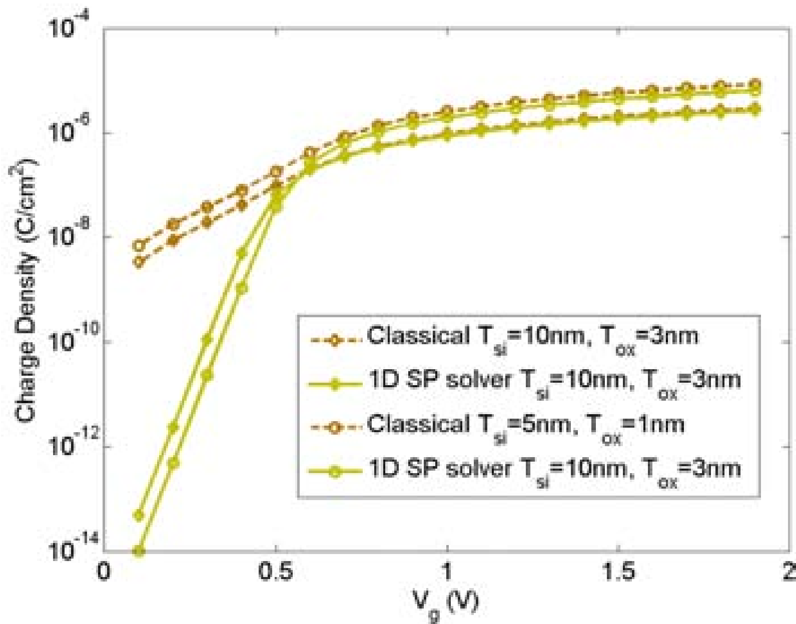


Figure 2-3
Comparison between classical [6] and quantum [38] models of mobile charge density in DG MOSFETs.

2.3 Quantum Potential Model

Our model takes the classical potential described in previous section as a starting point. The potential given by Eq. (2.2) is obtained by solving the Poisson equation (Eq. (2.1)) in the silicon region with only the classical mobile charge (electrons) density.

Since the angle of the cosine function in Eq. (2.2) cannot exceed $\pi/2$, the central potential ϕ_0 is pinned to an upper bound of $\phi_{0max} = V_T ln\left(\frac{2\pi^2 V_T \varepsilon_{si}}{T_{si}^2 q n_i}\right)$ which gives the saturation values of ϕ_0 in Figure 2-2 and it is the maximum value that the central potential reaches by increasing the gate voltage. Using this saturation value for ϕ_0, the classical potential ϕ of the Eq. (2.2) can be rewritten as follow without loss of generality [23]:

$$\phi(x) = \phi_0 - 2V_T ln\left[cos\left(\frac{\pi}{T_{si}} e^{(\phi_0 - \phi_{0max})/2V_T} x\right)\right] \quad (2.5)$$

Now, in order to correct the classical potential we must add QM effects, relevant at the nanoscale. We will do it introducing two additional parameters ξ and γ together with a ϕ_{0max} modified parameter in Eq. (2.6) to allow the fitting of the self-consistent QM numerical solution:

$$\phi(x) = \phi_0 - \frac{2V_T}{\gamma} ln\left[cos\left(\frac{\pi\xi}{T_{si}} e^{(\phi_0 - \phi_{0max})/2V_T} x\right)\right] \quad (2.6)$$

We can justify the introduction of two parameters because quantum effects modify both the charge density and its spatial distribution. The main idea and the simplicity of our model are based on finding compact expressions for the parameters ϕ_{0max}, ϕ_0, γ and ξ, as we will show.

2.3.1 Maximum central potential ϕ_{0max}:

For the QM case, the maximum central potential is larger than in the classical case due to the decrease of the charge density. Figure 2-4 shows the dependence of the maximum central potential with the silicon thickness T_{si} for $T_{ox} = 1, 2$ and 3 nm, which were obtained from simulations using a 1D self-consistent simulator [38]. Based on these simulations, a semi-empirical formula can be obtained with a goodness of fit statistics given by R = 1, using a square of correlation (R-square) metrics:

$$\phi_{0max} = (aT_{si} + b)/(T_{si} + c), \quad (2.7)$$

with the values $a = 0.4555\ (0.4535, 0.4574)$ V, $b = 0.1755\ (0.1156, 0.2358)$nm-V and $c = -0.8525\ (-0.9366, -0.7683)$ nm, where the numbers inside the parenthesis correspond to the confidence bounds. Note that T_{ox} does

not explicitly appear in Eq. (2.7) because ϕ_{0max} exhibits a very weak dependence on T_{ox} for T_{si}≥ 4nm.

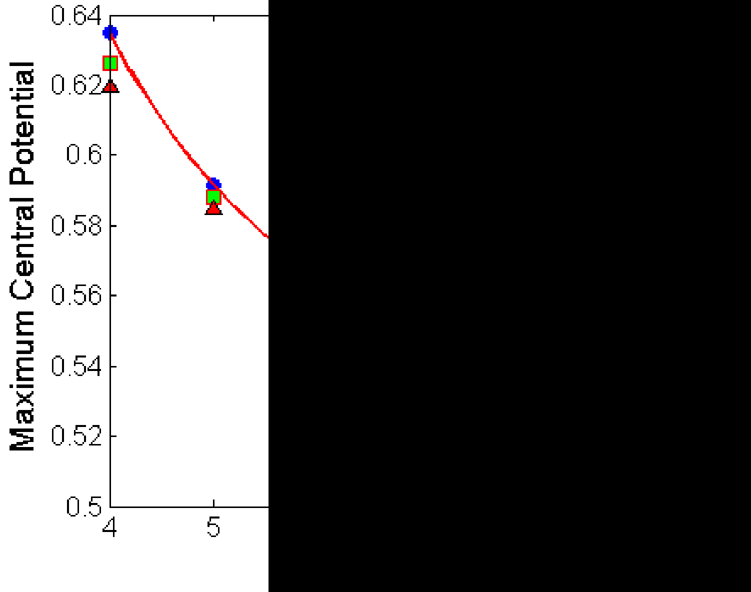


Figure 2-4
Maximum central potentials for $T_{ox} = 1, 2$ and 3 nm versus the silicon thickness T_{si}. Data are taken from 1D self-consistent simulator. Solid line corresponds to Eq. (2.7).

The sensitivity of final results respect to small variations on ϕ_{0max} is shown in the Figure 2-12.

2.3.2 The central potential ϕ_0

The Central potential is calculated using the approach of Ortiz [39], which to portray the behavior of ϕ_0 as a function of gate voltage uses the following smoothing function, similar to one previously used to model drain saturation voltage [40]:

$$\phi_0 = U - \sqrt{U^2 - (V_g - V_{fb})\phi_{0max}} \quad (2.8)$$

$$U = \frac{1}{2}\left[\left(V_g - V_{fb}\right) + (1 + r)\phi_{0max}\right] \quad (2.9)$$

Here V_g is the voltage applied to both gates, V_{fb} is the flat band voltage and r is a smoothing parameter weakly dependent on T_{ox} and T_{si}, which may be also determined from [39]

$$r = (AT_{ox} + B)(C/T_{si} + D) \tag{2.10}$$

where the constants $A = 0.0267$ nm^{-1}, $B = 0.0270$, $C = 0.4526$ nm and $D = 0.0650$ are appropriate values for oxide thicknesses below 5nm and film channel thicker than 4nm.

2.3.3 The γ parameter

We have mentioned that the charge density and potential profile are modified by the QM effects. We can model the change on the potential profile by means of the γ parameter, which is also obtained from the analysis of 1D self-consistent simulation, and is nicely modeled by the expression:

$$\gamma = \left[\frac{k}{(T_{si}+a_o)^2} + l\right] * G(T_{si}, T_{ox}) \tag{2.11}$$

$$G(T_{si}, T_{ox}) = \left(1 + exp\left(\frac{f(T_{ox}) - T_{si}}{a_1}\right)\right)^{-1} + G_0, \tag{2.12}$$

with

$$f(T_{ox}) = (f_1 + f_2)/2 + |f_1 - f_2|/2, \tag{2.13}$$

$$f_2 = 2T_{ox} + f_2^0 \tag{2.14}$$

where the combination $k = -5.9$ nm^2 , $a_0 = 0.078$ nm, $l = 0.23$, $a_1 = 0.1$ nm, $G_0 = 10^{-4}$, $f_1 = 5.5$ nm, $f_2^0 = 1.5\ nm$ yields pretty nice results. Factor G depends strongly on the ratio $2T_{ox}/T_{si}$ which is closed related to the structural parameter m defined as $m = 2\epsilon_{si}T_{ox}/\epsilon_{ox}T_{si}$. For values of T_{si} where the two inverted channels of the DG do not overlap, the γ parameter has two different regimes closely related to m. If $T_{si}/2T_{ox} \gtrsim 1$ then $\gamma \cong k/(T_{si} + a_o)^2 + l$, otherwise $\gamma \cong G_0$. When the two inverted channels overlap, i.e for values of $T_{si} \lesssim$ 5nm and $\forall\ T_{ox}$, $\gamma \cong G_0$, reflecting a greater effect of structural parameter on the electrostatics of the DG.

2.3.4 The ξ parameter

The ξ parameter must be obtained after applying the boundary condition at the Si/SiO_2 interface:

$$V_g = V_{fb} + \phi_s + \frac{\epsilon_{si}}{\epsilon_{ox}} T_{ox} \frac{d\phi}{dx}\bigg|_{x=T_{si}/2}, \tag{2.15}$$

where $\phi_s = \phi(x = T_{si}/2)$ corresponds to the surface potential. By using Eq. (2.6), introducing the change of variable $\beta = \xi \frac{\pi}{2} e^{(\phi_0 - \phi_{0max})/2V_T}$, and after a simple algebraic manipulation, Eq. (2.15) can be written as:

$$f(\beta) = ln\,(cos\,(\beta)) - m\beta\, tan\,(\beta) + F = 0. \tag{2.16}$$

Here m is the structural parameter, and $F = \gamma/2V_T * (V_g - V_{fb} - \phi_0)$. Given a gate voltage V_g, Eq. (2.16) cannot be analytically solved for β, and numerical or table look-up methods are required. To overcome this limitation, we can adopt a three step-method to find out β in a closed and accurate manner (see Appendix A for details) [41]. Finally, substitution of the explicit expressions for ϕ_0, ϕ_{omax}, γ and ξ into Eq. (2.6) provide a compact model for the electrostatic potential and charge including QM effects.

2.4 Quantum Charge Model

An analytic and continuous expression of the quantum electric charge associated with the gate is desirable in circuit simulation to know, for example, the gate tunneling current or capacitance to compute the AC and transient behavior.

Due to the confinement of electron motion normal to the Si/SiO_2 interface, the conduction band within the transistor channel is split in several subbands, each of which is associated with the corresponding energy eigenvalue. The channel charge per unit area may be expressed as

$$Q_{ch} = q \sum_{i=1,2} \sum_j N_i log\,[1 + e^{(E_f - E_{ij})/kT}] \tag{2.17}$$

where i and j are subscripts for valleys and subbands respectively, N_i is the density of states in the subband at energy E_{ij} . For silicon <100> cristal orientation, two groups of conduction subbands, with degeneracy factor $g_1 = 2$ and $g_2 = 4$, corresponding to the six distinct ellipsoidal constant energy surfaces, are considered for the computation of the density of states:

$$N_i = \frac{g_i m_{di}^* kT}{\pi \hbar^2} \tag{2.18}$$

where $m_{d1}^* = m_t, m_{d2}^* = \sqrt{m_l m_t}$ are the density-of-states effective masses for the low and high energy valleys respectively with $m_l = 0.92m_0$ and $m_t = 0.19m_0$ corresponding to the longitudinal and transversal masses.

It is difficult to find an analytic expression for the subband energies E_{ij} for all possible gate voltages. To circumvent this problem we can take advantage of the asymptotic behavior of $Q(V_g)$. Specifically, for $V_g \lesssim V_{th}$ (where V_{th} refers to the threshold voltage), the electronic states in a box-like potential well with an infinite barrier height are a very good approximation. On the other hand, for $V_g \gtrsim V_{th}$, Eq. (2.15) provides a simple relation, through the oxide voltage, between the channel charge and surface potential. Hence, we can write the following expressions accounting for the asymptotic behavior at low and high gate voltages, respectively:

$$Q^{<} = q \sum_{i=1,2} \sum_j N_i log\left[1 + e^{(E_f - E_{ij}^0)/kT}\right] \quad \text{for} \quad V_g \lesssim V_{th} \tag{2.19}$$

and

$$Q^{>} = \frac{2\epsilon_{ox}}{T_{ox}}\left(V_g - V_{fb} - \phi_s\right) \quad \text{for} \quad V_g \gtrsim V_{th} \tag{2.20}$$

where $E_{ij}^0 = \frac{\hbar^2}{2m_{zi}}\left(\frac{j\pi}{T_{si}}\right)^2 + \frac{E_g}{2} - q\phi_s$.

The factor two in Eq. (2.20) takes into account the contribution to the charge from the two gates, and m_{zi} refers to the confinement mass for valley i^{th}, so $m_{z1} = m_l, m_{z2} = m_t$.

Similarly to one previous model used to calculate the drain saturation voltage [40], based on a hyperbolic smoothing function with asymptotic

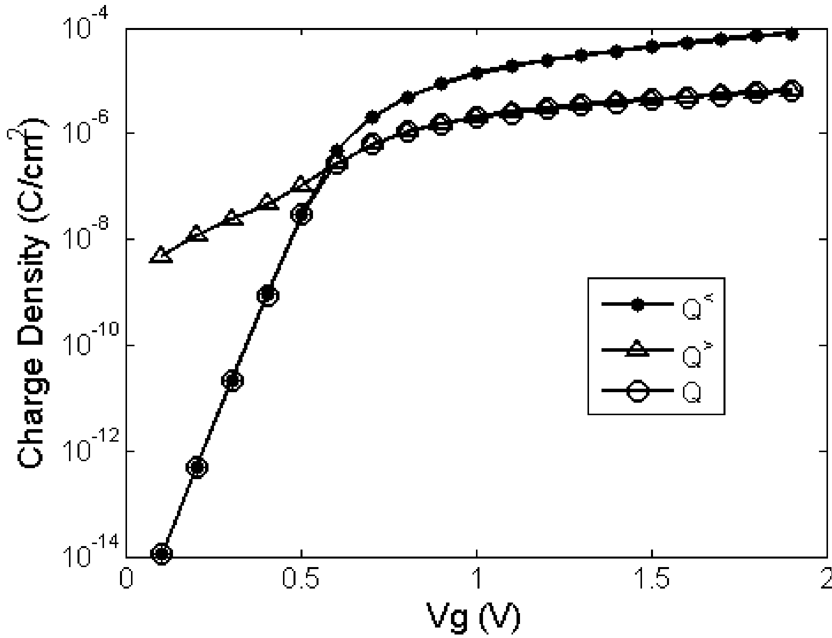


Figure 2-5
Charge density for T_{si} = 5nm and T_{ox} = 1nm. Solid lines are data from 1D simulator and symbols corresponds to our model data.

behavior to $Q^{<}$ and $Q^{>}$, the charge density can be composed using the expression

$$Q = Q_m - \sqrt{{Q_m}^2 - Q^{<}Q^{>}}, \tag{2.21}$$

with $Q_m = 0.5(Q^{>} + \mu Q^{<})$, and $\mu = 1.01$ being a smoothing parameter that controls the distance of the hyperbola from its asymptotes. Figure 2-5 shows the behavior of Q, $Q^{<}$ and $Q^{>}$ as a function of the gate voltage and the Figure 2-6 shows the difference between the classical and quantum solutions of the charge density for comparison purposes.

Using the mentioned procedure, the charge per unit area can be expressed in a compact and explicit form in terms of known variables.

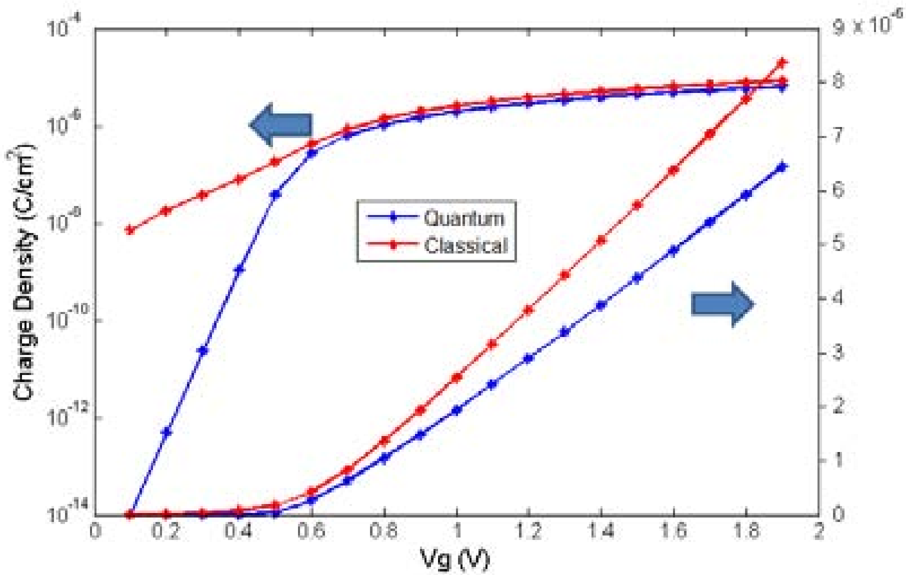


Figure 2-6
Quantum and classical charge density for $T_{si} = 5$nm and $T_{ox} = 1$nm.

2.5 Results

The model was validated by an extensive comparison with quantum numerical simulations from a 1D Poisson-Schrödinger solver [38]. Specifically, we have simulated the surface potentials, central potentials and charge density in the silicon channel as a function of V_g. Additionally, the silicon conduction band profiles along the perpendicular direction to the interface Si/SiO_2 have been computed for comparison.

Figure 2-7 shows an example of the surface and central potential as a function of V_g with different geometries. The results show that the output of our model is in close agreement with the self-consistent solution with a relative error less than 5 % in any case.

Typical silicon conduction band profiles are shown in Figure 2-8a and Figure 2-8b, respectively, for several gate voltages. Note that bands are essentially flat in the subthreshold region, just up to $V_g \sim 0.4$ V identified as the threshold voltage. For $V_g \gtrsim 0.4$ V, the surface potential increases linearly, and the central potential slightly downshifts until saturation is reached at $V_g \sim 1$V, identified as the onset of screening effects. Limitations of our model arise when

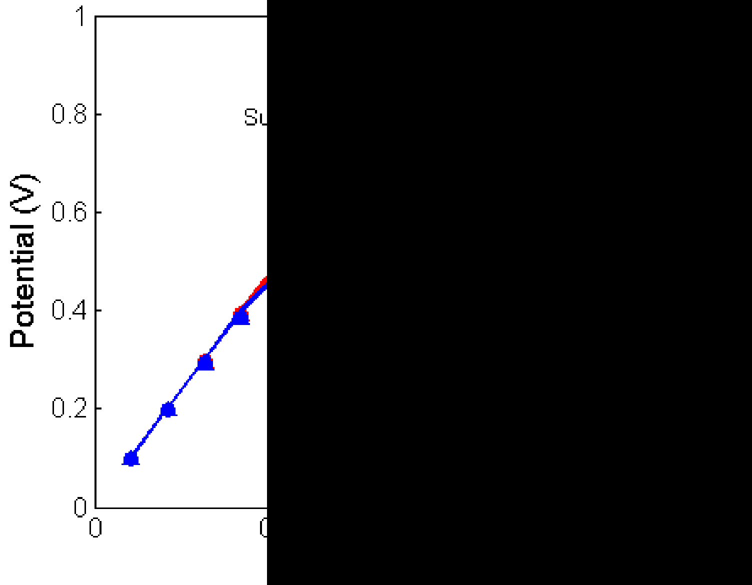


Figure 2-7
Electrostatic potentials at the center of the channel and the surface versus the gate voltage V_g. Geometrical parameters used here are T_{si} = 5nm, T_{ox} = 1nm and T_{si} = 9nm, T_{ox} = 3nm. The flat band voltage is assumed to be $V_{fb} = 0$ V. Solid lines correspond to 1D simulations and symbols to our model data.

very thin films are considered. To illustrate this point, Figure 2-9 shows the behavior of the central potential as a function of V_g for DG-MOSFETs with different silicon films. For $T_{si} \gtrsim$ 4nm, the central potential shows a saturated like behavior above the threshold voltage, indicative of the gate field shielding due to the formation of inverted channels on both surfaces. However, for $T_{si} \lesssim$ 4nm and super-threshold operation, the central potential is no longer constant but grows almost linearly ($d\phi_0/dV_g > 0$), as can be observed from QM self-consistent results, suggesting the suppression of the two separated inverted channels in favor of volume inversion operation, where the gate field is now allowed to penetrate into the silicon film thus taking the control of the central potential.

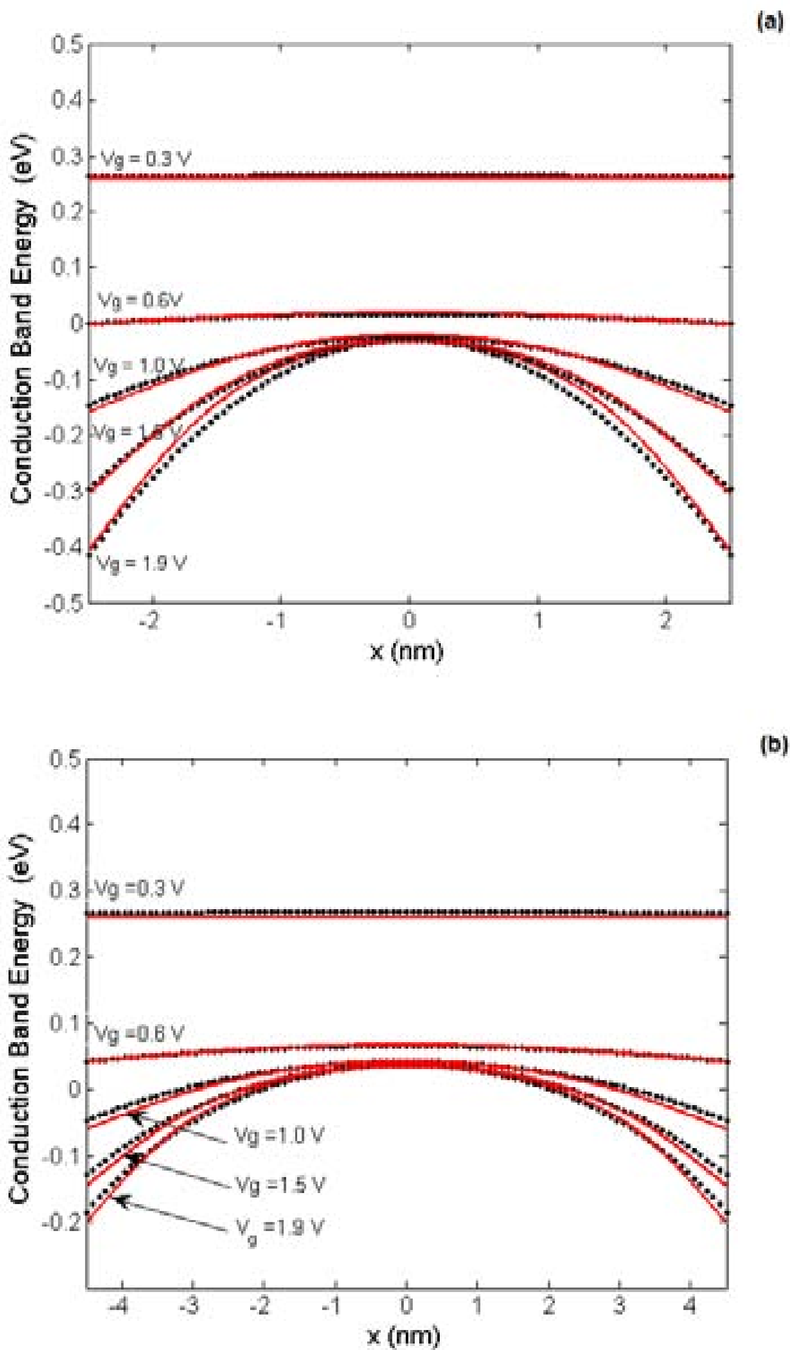


Figure 2-8

Silicon conduction band profiles for (a) $T_{si} = 5$nm, $T_{ox} = 1$nm and (b) $T_{si} = 9$nm, $T_{ox} = 3$nm. Solid lines are data from 1D simulator and symbols corresponds to our model data.

Although we have found that for $T_{si} \lesssim$ 4nm the T_{ox} dependence of ϕ_{0max} start to be important and our model fails in this range (see Figure 2-4 and Figure 2-9), it works very well in scales where the effective mass approximation for nanoscale system is reasonable and the simulated results are correct. This is, the parabolic approximation may be not sufficient for nanoscale systems with atomic scale variations and tight-binding band-structure calculation or empirical pseudo potentials may be necessary [42, 43]. To highlight the importance of introducing a quantum model for the electrostatics on thin DG-MOSFETs, the reader should remember Figure 2-2 where the surface and central potentials are calculated from our model and compared with the classical model from Taur [23]. Note that the difference $\phi_s - \phi_0$, above the threshold voltage, as given by the quantum model is significantly larger than the classical result, which should be taken into account, for instance, when tunneling gate current needs to be calculated.

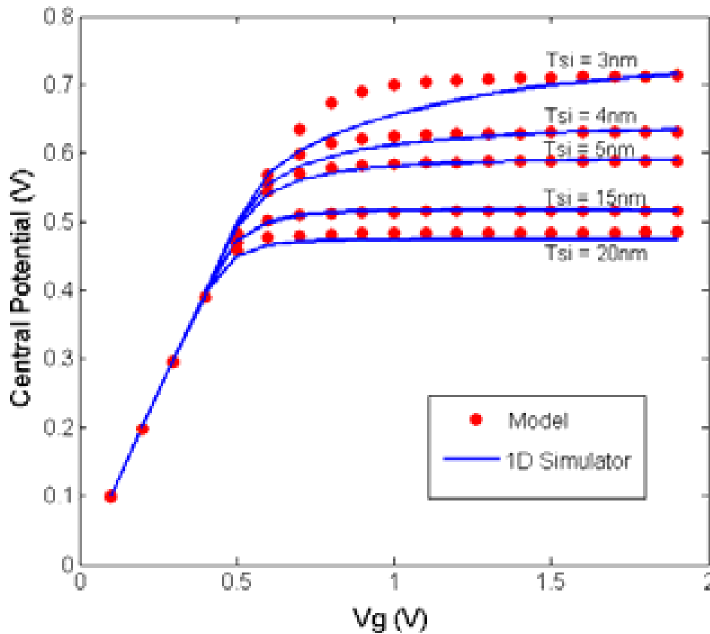


Figure 2-9
Electrostatic potentials at the center of the channel versus the gate voltage V_g for T_{si} = 2,3,4 and 5 nm. Solid lines correspond to the simulations and symbols to our model data.

Figure 2-10 shows a comparison between our charge model presented in Section 2.4 and 1D simulation data for different geometries as a function of the gate voltage. It continuously covers all the operation regions with unique

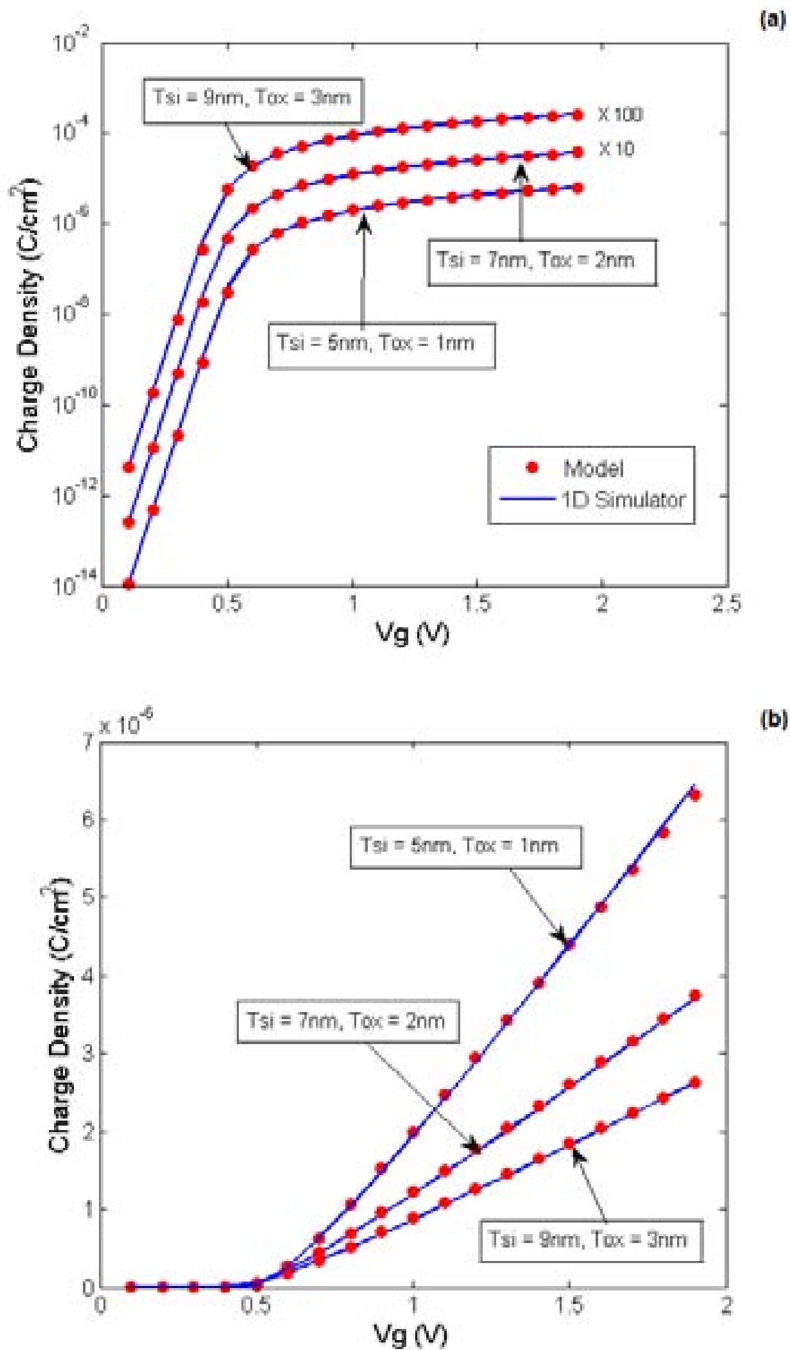


Figure 2-10

Charge density versus gate voltage for several geometries and flat band voltage $V_{fb} = 0$ V. (a) Logarithmic scale and (b) linear scale. Solid lines correspond to 1D simulations and symbols to our model data. Some curves in (a) have been shifted upwards for the sake of clarity.

analytic expressions. A close agreement, in both subthreshold and superthreshold regions, proves the correct behavior of our model. Importantly, the gate capacitance, defined as $C_g = dQ/dV_g$ is well captured by our model (Figure 2-11). That is a key parameter when AC and transient simulations are required.

Finally, Figure 2-12 shows, for different geometries, the sensitivity of physical variables ϕ_0, ϕ_s and Q to small variations of ϕ_{0max} and γ parameters included in Eq. (2.6), around the values of ϕ_{0max}^* and γ^* calculated from Eqs. (2.7) and (2.11), respectively. The sensitivity is quantified using the R-Square factor. The inset shows similar results but, in this case, the sensitivity analysis refers to the γ parameter. Note the ξ parameter in Eq. (2.6) has not been analyzed because is a function of γ and ϕ_{0max} through Eq. (2.16). The R-Square factor appears to be not very sensitive to small variation of ϕ_{0max} and γ parameters included in Eq. (2.6).

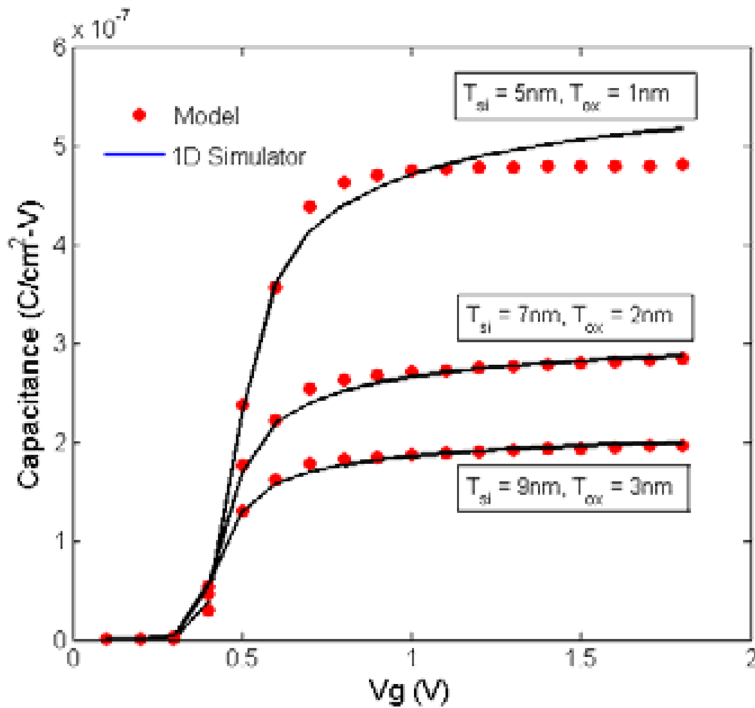


Figure 2-11
Gate capacitance versus gate voltage for several geometries and flat band voltage $V_{fb} = 0$ V. Solid lines correspond to 1D simulations and symbols to our model data.

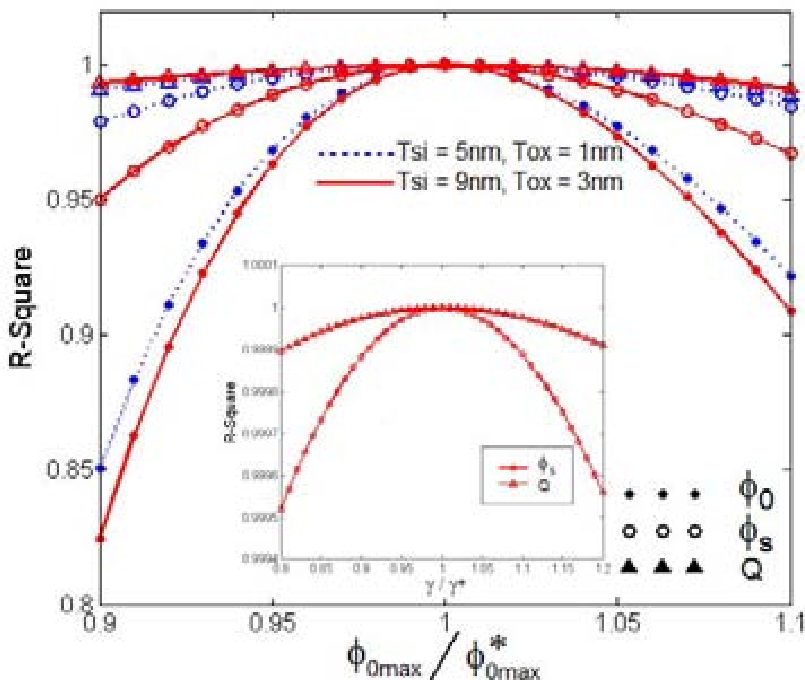


Figure 2-12
R-Square factor analysis of ϕ_0, ϕ_s and Q as a function of ϕ_{0max} relative to ϕ^*_{0max}. The inset shows the R-Square factor of ϕ_s and Q as a function of γ relative to γ^*.

2.6 Summary

A simple model for the quantum electrostatic potential and charge of the undoped long channel DG-MOSFET for thin silicon films has been developed and assessed. Additionally our model accurately reproduces the gate capacitance. The model presented here, based on the previously developed classical model [23], accounts for the Si-film thickness, oxide thickness and gate voltage dependences. Our model gives a closed form for the potential and charge (it does not need any iteration) and the results are in close agreement with self-consistent solutions.

We must emphasize that this model works very well within the range of validity of the used approximations. That is, for $T_{si} \gtrsim 4$nm, $T_{ox} \leq 5$nm, sub- and superthreshold regions. Although Ge's model [37] describes the quantum potential profile in a wider range of silicon thickness, their approach is not

useful to obtain the distribution of voltage through the MOS structure because the potential is referenced to the surface potential; i.e. $\phi_s = 0$ for all V_g. That is, our model is able to calculate, completely, the dependence on ϕ_s, ϕ_0 and Q as a function of the gate voltage. The presented compact model can be interpreted as the core of more advanced models including, for instance, short-channel effects, non-equilibrium effects and tunneling effects.

Next chapter will address the development of an explicit model for the direct tunneling current in DG structures, using SiO_2 as gate dielectric material. Such a model makes extensive use of the electrostatic model presented in this chapter.

CHAPTER 3.

Explicit Model for the Gate Tunneling Current in Double-Gate MOSFETs

3.1 Outline

In this chapter, an explicit compact quantum model for the gate tunneling current in double-gate (DG) MOSFET is presented. Specifically, an explicit closed-form expression is proposed, useful for the fast evaluation of the gate leakage in the context of electrical circuit simulators. A benchmarking test against 1D self-consistent numerical solution of Schrödinger-Poisson (SP) equations has been performed to demonstrate the accuracy of the model.

Like conventional transistors, the scaling rule of DG-MOSFETs for controlling SCE dictates a reduction of the equivalent oxide thickness together with the channel length. The increasing gate leakage has to be taken into account due to its importance in determining the standby power.

Researchers have proposed some models for calculating the gate current in DG-MOSFETs however, due to the difficulty of solving the coupled SP equations, certain models have being proposed based on semi-empirical

dependent electric field expressions [44, 45], or purely numerical [46, 32], or considering only the ground state derived from a triangular approximation for the electronic confinement [47]. It is therefore valuable to have a compact model of the gate leakage current for DG-MOSFETs simply calling an explicit closed-form expression embedding the dependence on bias and both geometrical and electrical parameters.

In this work, we further extend the state-of-the-art by proposing a simple model for the electron conduction band (ECB) direct tunneling current of undoped DG-MOSFET, which is the dominant mechanism contributing to the gate leakage [48]. Our results are compared with those obtained from accurate self-consistent quantum-mechanical (QM) solutions resulting in excellent agreement for both moderate and strong inversion regimes, thus making it suitable for compact modeling.

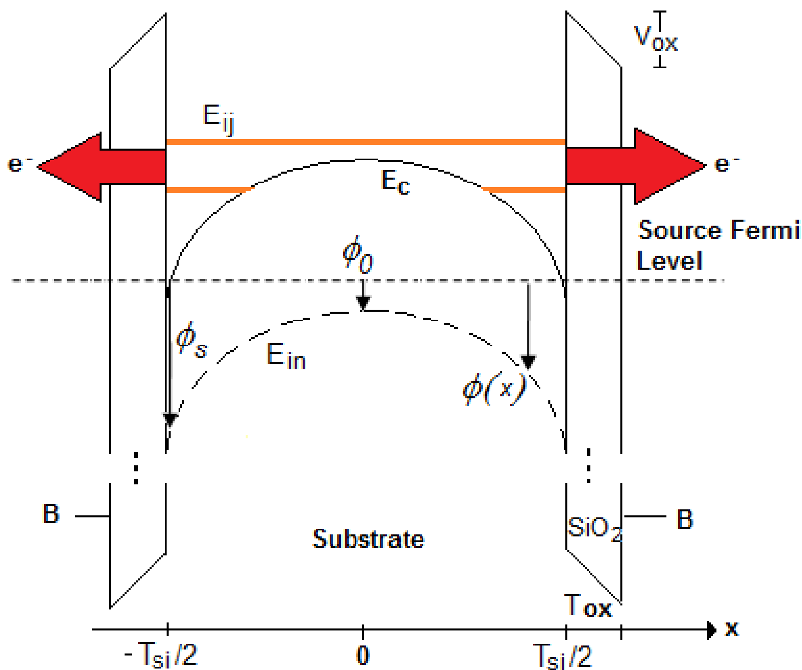


Figure 3-1
Energy-band diagram along a perpendicular cut to the channel, where the direct gate tunneling flow is marked with thick arrows.

3.2 Model Development

In this section, modeling of quantum mechanical effects in an undoped silicon layer, considered as the active layer of the transistor, and subsequent direct tunneling current for a symmetric DG geometry are presented. Figure 3-1 shows a representative energy-band diagram along a vertical cut, where E_c represents the silicon conduction band edge, E_{in} is the intrinsic Fermi energy, and V_{ox} is the potential drop at the gate oxide. Also represented are the surface potential ϕ_s and the central potential ϕ_0, both referred to the Fermi level at the source. Also shown in Figure 3-1 are some of the quantized electron energy subbands and the direct gate tunneling flow of electrons from the Si substrate towards the metal gate.

Because of structural and/or electrostatic confinement in nanoscale DG-MOSFETs, quantization of the carrier energy in the Si layer is a relevant effect to be considered, generally, for any operation regime. Quantum effects result in a spatially wider carrier density as compared to the classical prediction. A common approach to tackle quantum effects consists of solving the coupled SP equations in a fully self-consistent manner. This method is accurate, but time consuming.

What we propose here is an efficient method in terms of computational time. Simplification of the complexity is possible using a quadratic approximation for the electron conduction band in the active layer as a perturbation to the box-like potential well created by the SiO_2/Si/SiO_2 structure. Our model starts from the 1D classical modified potential to include quantum effects described in Chapter 2 and published in Ref. [49]. As demonstrated in Figure 2-7, both the surface and central potentials are well reproduced as compared with self-consistent SP simulations, where, to remember, the surface potential takes the form

$$\phi_s = \phi_0 - \frac{2kT}{q\gamma} ln\left[cos\left(\frac{\pi\xi}{2} e^{q(\phi_0-\phi_{0max})/2kT}\right)\right] \qquad (3.1)$$

where the meaning of parameters ϕ_{0max}, ϕ_0, ξ and γ were previously discussed. It is worth noting that these quantities can be explicitly computed and numerical calculations are not required.

Figure 3-2
Scheme of the transit time for electrons moving through the perpendicular direction to the channel. Also shown are the quantities defined in Eq. (3.7).

Next, for simplicity, we assume a parabolic shape for the 1D electrostatic potential across the channel nicely fitting both ϕ_s and ϕ_0

$$\phi(x) = \phi_0 + 4(\phi_s - \phi_0)x^2/T_{si}^2 \tag{3.2}$$

Using the 2D density of states (DOS) and Fermi-Dirac statistic, the channel charge per unit area contributed per subband can be expressed as

$$N_{ij} = q\left(\frac{kT}{\pi\hbar^2}\right) g_i m_{di}^* \ln[1 + e^{(E_f - E_{ij})/kT}] \tag{3.3}$$

Based on perturbation methods [50], the energy level E_{ij} (referred to the minimum of the conduction band at the surface E_{cs}) could be split into:

$$E_{ij} = E_{ij}^0 + E_{ij}^1 \tag{3.4}$$

where

$$E_{ij}^0 = \frac{\hbar^2}{2m_{zi}}\left(\frac{j\pi}{T_{si}}\right)^2 \tag{3.5}$$

corresponds to the eigenvalues of the non-perturbed Hamiltonian (box-like potential well with infinite barriers) and

$$E_{ij}^{1} = \int_{-T_{si}/2}^{T_{si}/2} \psi_j^0(x)\tilde{E}_c(x)\psi_j^{0^*}(x)dx = 2\Delta E_{\text{os}}\left(\frac{1}{(j\pi)^2} + \frac{1}{3}\right) \quad (3.6)$$

is the correction of the eigenvalues due to the perturbed Hamiltonian (quadratic potential approximation given by Eq. (3.2)). The eigenfunction $\psi_j^0(x)$ corresponds to the wave function coming from the non-perturbed Hamiltonian and is equal to $\sqrt{2/T_{si}}\sin(j\pi/T_{si}(x + T_{si}/2))$. Note that $\psi_j^{0^*}$ refers to the complex conjugate and is equal to ψ_j^0. For expressing Eq. (3.6), we have used the following conventions (see Figure 3-2):

$E_c(x) = E_g/2 - q\phi(x)$	Conduction band relative to the Fermi level at the source electrode.
$E_{cs} = E_c\left(\frac{\pm T_{si}}{2}\right)$	Conduction band at the Si/SiO_2 interface.
$E_{co} = E_c(0)$	Conduction band at the center of Si layer.
$\Delta E_{\text{os}} = E_{co} - E_{cs}$	Difference between the center and surface potential.
$\tilde{E}_c(x) = E_c(x) - E_{cs}$	Conduction band relative to E_{cs}

$$= \Delta E_{\text{os}}(1 - 4x^2/T_{si}^2) \quad (3.7)$$

As we are interested in a simple expression for direct tunneling current at both low and high supply voltage regimes, we chose a modified WKB method to calculate the electron transmission probability [51]. Within the mass effective approximation, transmission probability of electrons with energy E_{ij} can be written in the form:

$$P_{ij} = P_{WKB} \cdot P_R, \quad (3.8)$$

where $P_{WKB} = \exp\left(-2\int_0^{T_{ox}} k_{ox,ij}(x')dx'\right)$ is the usual WKB tunneling probability [52], valid for smoothly varying potentials. Here a change of coordinate has been made such that $x' = x - T_{si}/2$. The term P_R is a correction accounting for reflections due to potential discontinuities [51]. The momentum

entering in the integral can be calculated by using a Franz-type dispersion relation for the gate oxide [53], namely

$$\frac{\hbar^2 k_{ox,ij}^2}{2m_{ox}} = \eta_{ij} = E_{ox,ij}\left(1 - \frac{E_{ox,ij}}{E_{g,ox}}\right) \tag{3.9}$$

$$v_{ox,ij} = \frac{1}{\eta_{ij}^{'}}\sqrt{\frac{2\eta_{ij}}{m_{ox}}}, \tag{3.10}$$

where m_{ox} is the electron effective mass within the SiO_2 oxide, $E_{g,ox}$ is the oxide band gap ≈ 9 eV for SiO_2, $v_{ox,ij}$ refers to the group velocity of electrons in the oxide, and $\eta_{ij}^{'}$ is defined as $\frac{d\eta_{ij}}{dE_{ox,ij}}$. On the other hand $E_{ox,ij}(x')$ is the magnitude of the electron energy relative to the oxide conduction band edge given by $\Phi_B - E_{ij} - qV_{ox}x'/T_{ox}$, where Φ_B is the discontinuity between the Si and SiO_2 conduction bands (~ 3.15 eV), and V_{ox} is the oxide voltage drop equal to $Q\frac{T_{ox}}{2\epsilon_{ox}}$, where the factor 2 in the denominator comes from the half of the total charge (Q) that is controlled by each gate.

To go ahead both P_{WKB} and P_R for electrons with energy E_{ij} can be expressed, respectively, as

$$P_{WKB} = exp\left[\frac{E_g T_{ox}\sqrt{2m_{ox}}}{4\hbar q V_{ox}}\left(2\eta_{ij}^{'}\sqrt{\eta_{ij}} + \sqrt{E_g}\sin^{-1}\eta_{ij}^{'}\right)\Big|_{E_{ox,ij}(x'=T_{ox})}^{E_{ox,ij}(x'=0)}\right] \tag{3.11}$$

$$P_R = \frac{4v_{Si,ij}(E)v_{ox,ij}\left(E_{ox,ij}|_{x'=0}\right)}{v_{si,ij}^2(E)+v_{ox,ij}^2\left(E_{ox,ij}|_{x'=0}\right)}\,\frac{4v_{Si,ij}(E+qV_{ox})v_{ox,ij}\left(E_{ox,ij}|_{x'=T_{ox}}\right)}{v_{si,ij}^2(E+qV_{ox})+v_{ox,ij}^2\left(E_{ox,ij}|_{x'=T_{ox}}\right)} \tag{3.12}$$

where $v_{Si,ij}$ is the perpendicular (normal to the interface) component of electron group velocity. Both P_R and P_{WKB} are quantities depending on the transversal m_t and longitudinal m_l electron effective masses. The group velocity for electrons in the substrate is computed as

$$v_{Si,ij} = \sqrt{\frac{2E_{ij}}{m_{zi}}} \tag{3.13}$$

In addition to the eigenvalues and transmission probabilities, the “lifetime” T_{ij} of the electrons in the i,j^{th} electronic state flowing toward the gates from the silicon layer is needed to calculate the leakage current. A useful model for this parameter comes from [32]:

$$\frac{1}{T_{ij}} = \frac{P_{ij}}{\tau_{ij}}\left[(1 - P_b) + \frac{1}{2}P_b^2\right] \tag{3.14}$$

where τ_{ij} is the classical transit time of an electron between Si/SiO_2 interface and the classical turning point $x_{t,ij}$, P_{ij} is the transmission probability of Eq. (3.8) and P_b is the tunneling probability through the conduction band. Note that the time elapsed for tunneling through the barrier in the silicon region has been neglected in Eq. (3.14).

The transit time is defined as the integral of the inverse of the group velocity $\tau_{ij} = 2\int_{x_{t,ij}}^{T_{si}/2} v^{-1}(x)dx$, which could be analytically calculated yielding

$$\tau_{ij} = 2\int_{x_{t,ij}}^{T_{si}/2} \sqrt{\frac{m_{zi}}{2(E_{ij} - \tilde{E}_c(x))}}\,dx = T_{si}\sqrt{\frac{m_{zi}}{2\Delta E_{os}}}\ln\left(\frac{\sqrt{\Delta E_{os}} + \sqrt{E_{ij}}}{\sqrt{|E_{ij} - \Delta E_{os}|}}\right) \tag{3.15}$$

This expression is valid for both $E_{ij} \leq \Delta E_{os}$ and $E_{ij} > \Delta E_{os}$ cases. A physical interpretation of the transit time is sketched in Figure 3-2.

The tunneling probability P_b for electrons with energies between E_{co} and E_{cs} to cross the conduction band can be calculated with the help of a simplified WKB approximation in the form

$$P_b = exp\left\{-2\int_{-x_{t,ij}}^{x_{t,ij}} \sqrt{\frac{2m_{zi}}{\hbar^2}\left[E_{ij} - \tilde{E}_c(x)\right]}\,dx\right\} \tag{3.16}$$

Inserting Eqs. (3.4) to (3.7) into Eq. (3.16) and, after some manipulations, P_b could be written as a simple closed-form expression

$$P_b = exp\left(-\sqrt{\frac{m_{zi}\pi^2 T_{si}^2}{2\hbar^2 \Delta E_{os}}}(\Delta E_{os} - E_{ij})\right) \text{ for } E_{cs} < E < E_{c0} \quad (3.17)$$

It is worth noting that $\frac{1}{T_{ij}} \sim P_{ij}/(2\tau_{ij})$ for energy levels such as $E_{ij} > \Delta E_{os}$, for which $P_b = 1$. Conversely, for energies deep in the potential well formed by the electrostatic confinement, then $P_b \sim 0$ and $\frac{1}{T_{ij}} \sim P_{ij}/\tau_{ij}$ similar to the case of a very thick semiconductor, which is equivalent to bulk diodes connected by the common substrate.

The proposed semi-classical model for the electron lifetime given by Eq. (3.14) yields similar results as compared with the half-with of the resonant state method [54, 55] as well as the method of quasi-bounded states with absorbing boundary conditions [56, 57]. However is computationally more efficient.

Finally, combining the results from Eqs. (3.3), (3.8), (3.14) and (3.17), we can readily obtain the total gate direct tunneling current density by adding the contribution of every subband:

$$J = \sum_{ij} N_{ij}/T_{ij} = \sum_{ij} J_{ij} \quad (3.18)$$

3.3 Results

The model described in this chapter considers as fundamental quantities E_{ij}, N_{ij}, and T_{ij}. In this section we check the accuracy of these quantities and therefore of the proposed compact model. To illustrate the model outcome we only consider the first three states, which contribute the most to the gate direct tunneling current. We also have assumed a flat band voltage V_{fb} equal to zero, corresponding to a midgap gate. The results below show that the model output is in close agreement with the self-consistent solution in all operation regions and for wide range of silicon layer and gate oxide thicknesses, representative of the design window for nanoscale DG-MOSFETs.

The behavior of the ground state energy E_{11}, E_{12} and E_{21} as a function of the gate voltage is shown in Figure 3-3a. As expected, the energy states increase as T_{si} is reduced due to the structural confinement. Below the threshold voltage,

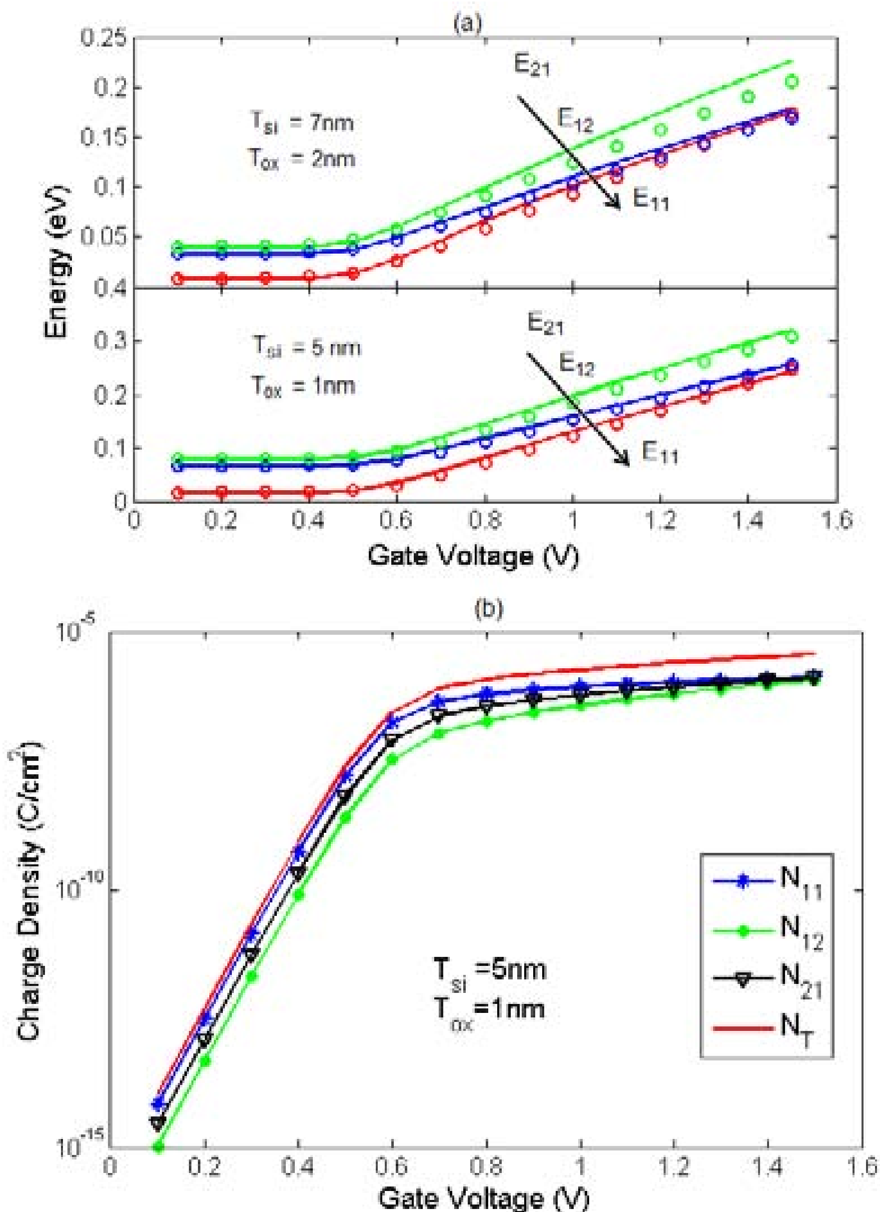


Figure 3-3
(a) Subband energies versus gate voltage for different geometries; (b) Charge densities of the three first states and total charge density (N_T);

the band bending is negligible, and the band diagram looks like a square potential well. Beyond the threshold voltage, the electric field strength induces an electrostatic confinement of carriers, resulting in a semi-quadratic potential

well. Figure 3-3b represents the total charge density and the charge densities $N_{11,}$ N_{12} and N_{21} as a function of the gate voltage. Here, we see that the E_{21} level contributes significantly to the charge density because its degeneracy and density of states effective mass, despite having a higher energy than the other two levels (see Figure 3-3a).

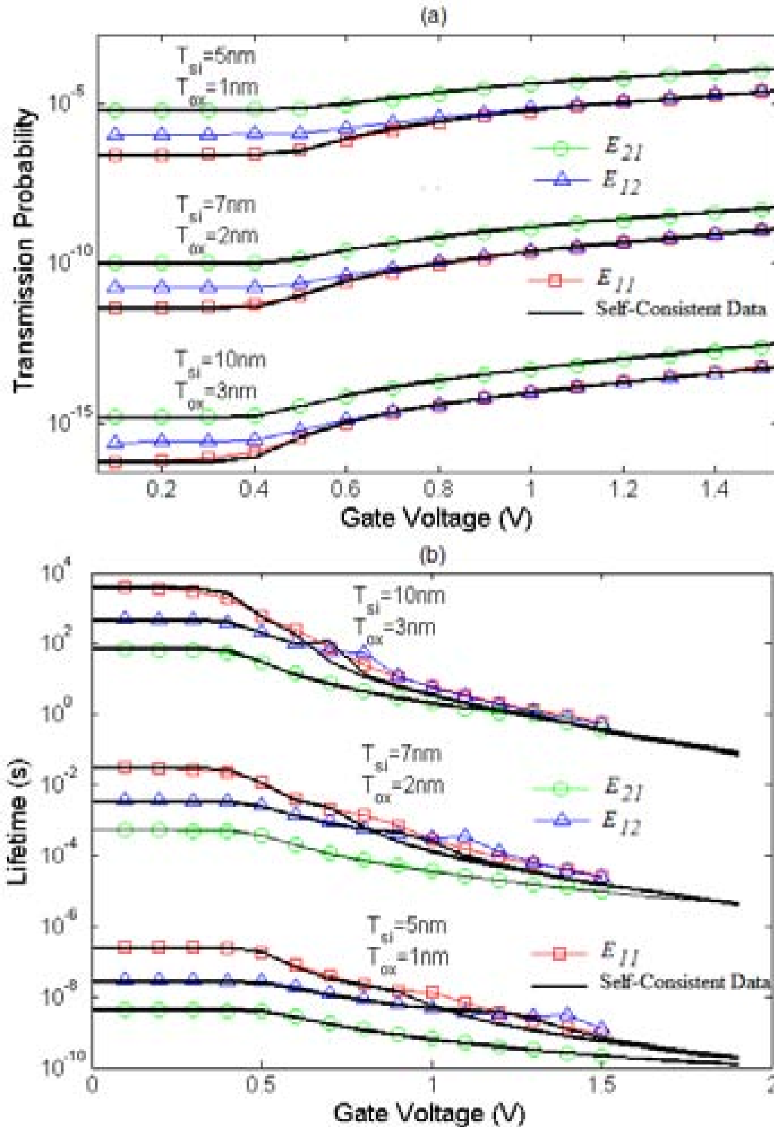


Figure 3-4

(a) Transmission probability of the E_{ij} state through the oxide barrier; (b) Electron lifetime of the E_{ij} state.

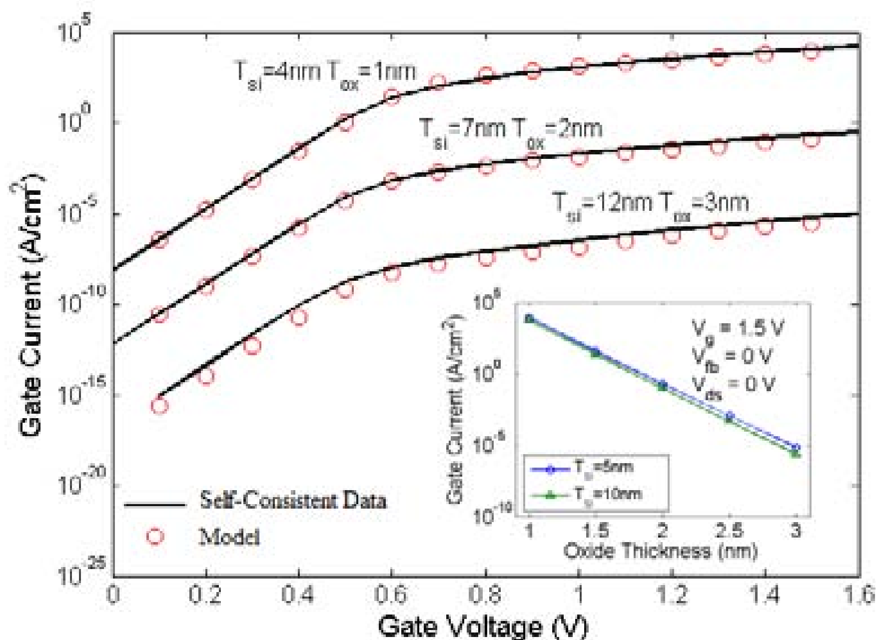


Figure 3-5
Gate current density where the inset shows the gate current density as a function of the oxide thickness. Symbols: model; Solid lines: SP simulations.

Figure 3-4a and Figure 3-4b show the transmission probability P_{ij} and lifetime T_{ij}, respectively. Here, we can appreciate the strong dependence of the tunneling with the oxide thickness (see also the inset of Figure 3-5). In general, the transmission probability increases and the lifetime is reduced with the gate voltage as a result of the electric confinement in the inversion layer. However this effect is smaller when the body is thinner because the confining electric field is reduced [58].

Combining the fundamental quantities, following Eq. (3.18), we have finally calculated the gate current density for several geometries. The result is shown in Figure 3-5 and the inset shows the expected exponential character of the tunneling current with the thickness of the barrier oxide.

In absence of experimental data in the literature (to our knowledge), our results are comparable with those reported in works where the self-consistent simulations take into account the electronic wave function penetration in the metal gate [46, 58].

3.4 Summary

An explicit compact model of the gate direct tunneling current for the symmetric undoped DG-MOSFET has been developed and assessed. Specifically the model was checked via comparison with self-consistent SP simulations. Our model is accurate within the range of validity of the used approximations. That is, for $T_{si} \gtrsim 4nm$ and $T_{ox} \leq 5nm$. All the quantities taking part in the model are explicit closed-form expressions that permit to calculate the dependence of the gate direct tunneling current as a function of the gate voltage.

This model makes possible the fast evaluation of the gate leakage in aggressive scaled DG-MOSFETs and could be incorporated into a general compact model as a building block of electrical circuit simulators.

Although the present model for the direct tunneling works for silicon dioxide as gate dielectric material, when the SiO_2 thickness is scaled roughly to 1nm very large gate current density is observed. Figure 3-5 shows that the gate current density exceeds 1A/cm^2 for gate voltage values larger than 0.5 V, which are too high for low power applications [9]. The introduction of high-κ dielectric materials as gate insulators is a key solution to solve the gate tunneling leakage current issue because for a given equivalent oxide thickness (EOT) the leakage is much smaller for high-κ than for oxi-nitride gate dielectric. Next chapter proposes an extension of the model presented in this chapter, where dual layer stacks including high-κ insulators are considered in the calculation of the direct tunneling current.

CHAPTER 4.

Explicit Model for Direct Tunneling Current in Double-Gate MOSFETs Through a Dielectric Stack

4.1 Outline

In this chapter an extension to the model presented in the previously chapter is presented. In this case, an explicit compact quantum model for the direct tunneling current through dual layer SiO_2/high-κ dielectrics in Double Gate structures is proposed. Specifically, an explicit closed-form expression is proposed, useful to study the impact of dielectric constants and band offsets in determining the gate leakage, allowing to identify materials to construct these devices, and useful for the fast evaluation of the gate leakage in the context of electrical circuit simulators. A comparison with self-consistent numerical solution of Schrödinger-Poisson (SP) equations has been performed to demonstrate the accuracy of the model. Finally, a benchmarking test for different gate stacks have been proposed searching to fulfill the gate tunneling limits as projected by the ITRS.

Similar to the conventional transistors, the scaling rule of DG-MOSFETs dictates a reduction of the oxide thickness together with the channel length, causing a large increase of the gate leakage current [9]. This is critical in determining power dissipation of circuits, especially those used in low-power electronic systems such as cell phones, lap-tops etc. Similarly to the bulk MOSFET, a way to overcome this limitation is to use high-κ materials deposited over a thin SiO_2 layer to form the gate insulator.

To calculate the gate leakage current in DG-MOSFETs it would strictly be necessary to solve the coupled Schrödinger-Poisson (SP) equations in a fully self-consistent manner considering a quasi-bound system. This method is accurate, but time consuming. Researchers have proposed some analytical models for calculating the gate current in DG-MOSFETs including high-κ dielectrics. However those models have being proposed based on semi-empirical dependent electric field expressions [44, 59] and do not consider the quantization of the energy levels. On the other hand there are some purely numerical models solving the SP equations self-consistently [32, 46] not useful for a fast evaluation of device performances in circuits simulators. It is therefore valuable to have a compact model of the gate tunneling current for DG-MOSFETs with dielectrics including high-κ materials, simply calling an explicit closed-form expression that takes into account relevant quantum effects. Such models are essential to understand the scaling limits of DG-MOSFETs.

We introduce a compact model of the direct tunneling current mechanism of symmetric undoped DG-MOSFETs considering a SiO_2/high-κ hetero-structure as gate oxide based on the previous model of the Chapter 3 where only SiO_2 dielectric was used and reported in Ref. [60].

Direct tunneling is known to be the dominant contribution to the gate leakage current [61]. Our results are compared with those obtained from accurate self-consistent quantum-mechanical (QM) solutions, resulting in excellent agreement for both moderate and strong inversion regimes. Both accuracy and simplicity of the model makes it suitable for circuit simulators.

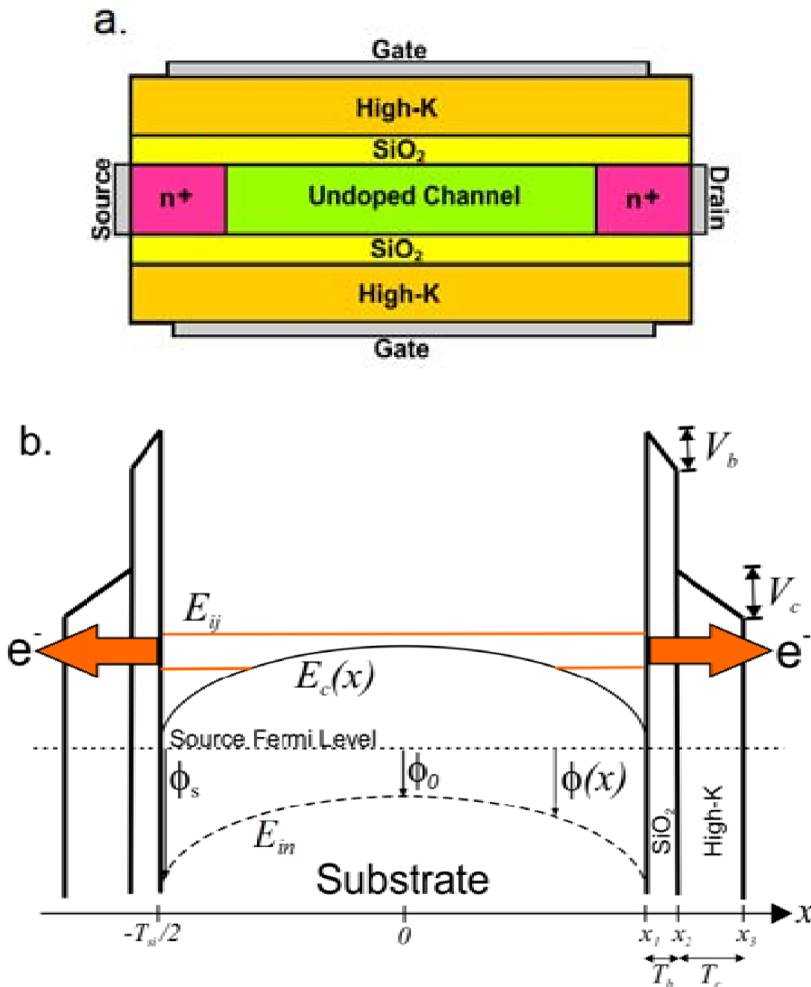


Figure 4-1
Schemes of (a) DG-MOSFET structure and (b) the energy-band diagram across the channel.

4.2 Model Development

To model the direct tunneling current of a symmetric DG-MOS capacitor (Figure4-1a) we have assumed fully bound states, meaning that the electron wave function does not penetrate through the gate oxide. Fig. 1b shows an energy-band diagram considering volume inversion, where E_c represents the silicon conduction band edge, E_{in} is the intrinsic Fermi energy, and V_b and V_c are the potential drops at the SiO_2 and high-κ dielectrics, respectively. Again, the surface and central potentials ϕ_s and ϕ_0 are both referred to the Fermi level at

the source. The electron direct gate tunneling current goes from the Si substrate to the metal gate passing through the dielectric stacks.

In this chapter we propose a suitable method in terms of computational time. Again, it relies on a quadratic approximation for the electron conduction band in the silicon layer acting as a perturbation to the box-like potential well created by the high-κ/SiO_2/Si/SiO_2/high-κ structure (see Figure 4-1b). Our model starts from a 1D classical potential expression, modified to include QM effects [49], which was proposed for a DG structure using SiO_2 as gate dielectric with thickness T_{ox} and potential drop V_{ox}. It can be easily adapted to our purposes, only replacing T_{ox} by the Equivalent Oxide Thickness $EOT = T_b + \frac{3.9}{\kappa} * T_c$, and V_{ox} would be now the sum of the potential drops in each layer V_b and V_c, so $V_{ox} = V_b + V_c$. The κ term is the high-κ material dielectric constant. By making those changes the full model described in Chapter 2 and published under Ref. [49] can be used to calculate the band profile. As shown in Figure 4-2, where the DG with SiO_2/HfO_2 as dielectric stack is considered, both the surface and central potentials are well replicated as compared with self-consistent SP simulations, where the surface potential takes the form

$$\phi_s = \phi_0 - \frac{2kT}{q\gamma} ln\left[cos\left(\frac{\pi\xi}{2} e^{q(\phi_0 - \phi_{0max})/2kT}\right)\right] \tag{4.1}$$

It is worth remembering that ϕ_{0max}, ϕ_0 , ξ and γ can be explicitly computed and iterative numerical calculations are not required.

Next, we assume a parabolic shape for the 1D electrostatic potential across the channel nicely fitting both ϕ_s and ϕ_0

$$\phi(x) = \phi_0 + 4(\phi_s - \phi_0)x^2/T_{si}^2 \tag{4.2}$$

Using the 2D density of states (DOS) and Fermi-Dirac statistic, the channel charge per unit area contributed per sub-band can be expressed as

$$N_{ij} = \frac{qkT}{\pi\hbar^2} g_i m_{di}^* \ln\left[1 + e^{(E_f - E_{ij})/kT}\right] \tag{4.3}$$

where g_i and m_{di}^* are the degeneracy and the DOS effective mass of the *i*th valley respectively, and E_{ij} is the energy level of the *j*th sub-band in the *i*th valley, referred to the minimum of the conduction band at the surface E_{cs}.

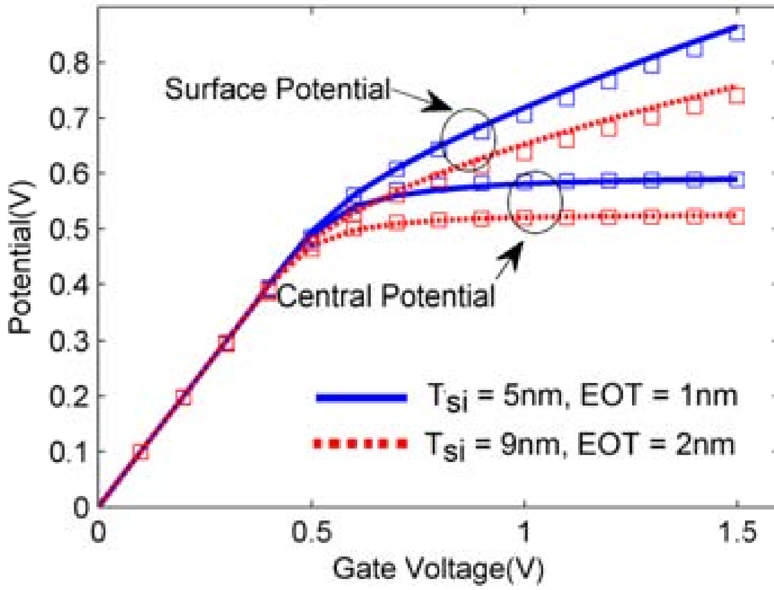


Figure 4-2
Surface and central potentials of a DG-MOS capacitor considering a SiO_2/HfO_2 gate stack, where SiO_2 has a physical thickness T_b = 0.7nm. Lines correspond to 1D SP self-consistent simulation and symbols correspond to the model.

Based on perturbation methods [50], the energy level E_{ij} could be split into:

$$E_{ij} = E_{ij}^0 + E_{ij}^1 \tag{4.4}$$

where

$$E_{ij}^0 = \frac{\hbar^2}{2m_{zi}}\left(\frac{j\pi}{T_{si}}\right)^2 \tag{4.5}$$

corresponds to the eigenvalues of the non-perturbed Hamiltonian (box-like potential well with infinite barriers) and

$$E_{ij}^1 = \int_{-T_{si}/2}^{T_{si}/2} \psi_j^0(x)\tilde{E}_c(x)\psi_j^{0^*}(x)dx = 2\Delta E_{\text{os}}\left(\frac{1}{(j\pi)^2} + \frac{1}{3}\right) \tag{4.6}$$

is the correction of the perturbed Hamiltonian (quadratic potential approximation given by Eq. (4.2)). The eigenfunctions $\psi_j^0(x) = \psi_j^{0^*} = \sqrt{2/T_{si}}\sin(j\pi/T_{si}(x + T_{si}/2))$ correspond to the wave function coming from the non-perturbed Hamiltonian. We have used the same convention of Eq. (3.7) to express Eq. (4.6) (see Figure 4-3).

To calculate the direct tunneling current we chose a modified WKB method to compute the electron transmission probability through the dielectric stack [62]. Within the mass effective approximation, transmission probability of electrons with energy E_{ij} can be written in the form:

$$P_{ij} = P_0 \exp\left[-2S_b - 2S_c\right], \quad (4.7)$$

where

$$S_b = \int_{x_1}^{x_2} \kappa_b(x)dx \quad \text{and} \quad S_c = \int_{x_2}^{x_3} \kappa_c(x)dx \quad (4.8)$$

are the usual WKB tunneling probabilities, valid for smoothly varying potentials. Here, we have defined $x_1 = \frac{T_{si}}{2}, x_2 = \frac{T_{si}}{2} + T_b$ and $x_3 = \frac{T_{si}}{2} + T_b + T_c$. The P_o term is a correction accounting for reflections due to potential discontinuities in the dual layer barrier [62]:

$$P_0 = \frac{64 v_a v_{b0} v_{b1} v_{c0} v_{c1} v_d}{[v_a{}^2 + v_{b0}{}^2](v_{b1} + v_{c0})^2 [v_{c1}{}^2 + v_d{}^2]} \quad (4.9)$$

where *a*, *b*, *c* and *d* regions are shown in Figure 4-3. For simplification, the electron wave functions in the *a* (silicon) and *d* (metal) regions can be expressed as travelling planes waves allowing a simple expression for the electron group velocity, so $v_a = \sqrt{2E_{ij}/m_{zi}}$ and $v_d = \sqrt{2(E_{ij} + E_{cs} + qV_g)/m_0}$ where V_g is the gate voltage and m_0 is the free electron mass. The imaginary part κ of the wave vector in the barrier region entering in Eq. (4.8) and the corresponding group velocity can be calculated by using a Franz-type dispersion relation for each oxide layer $n = b, c$ [63], namely

$$\frac{\hbar^2 k_n^2}{2m_n} = \eta_n = E_{ox,n}\left(1 - \frac{E_{ox,n}}{E_{g,n}}\right) \quad (4.10)$$

$$v_n = \frac{1}{\eta_n'}\sqrt{\frac{2\eta_n}{m_n}} \quad (4.11)$$

where $E_{g,n}$ is the oxide band gap in the *n*-layer, η_n' is defined as $\frac{d\eta_n}{dE_{ox,n}}$ and $E_{ox,n}(x) = \Phi_n - E_{ij} - qV_n(x - h_n)/T_n$ is the magnitude of the electron energy relative to the oxide conduction band edge in the *n*-layer. In this case $h_b = x_1$ and $h_c = x_2$. Also Φ_n and V_n represent the discontinuity between Si and the *n*-

conduction band and the voltage drop at the n-layer respectively. The latter can be expressed in terms of the total voltage drop V_T in the double layer as:

$$V_n = \frac{\frac{T_n}{\epsilon_n}}{\frac{T_b}{\epsilon_b}+\frac{T_c}{\epsilon_c}} V_T = \frac{\frac{T_n}{\epsilon_n}}{\frac{T_b}{\epsilon_b}+\frac{T_c}{\epsilon_c}} \left(V_g - V_{fb} - \phi_s\right), \quad n = b, c \qquad (4.12)$$

where V_{fb} is the flat band voltage.

Considering expressions (4.10) and (4.11), the integrals in (4.8) can be carried out to yield the following analytical solution

$$S_n = \frac{E_{g,n} T_n \sqrt{2m_n}}{4\hbar q V_n} \left(2\eta_n' \sqrt{\eta_n} + \sqrt{E_{g,n}} \sin^{-1}\eta_n'\right)\Bigg|_{E_{ox,n}(x_n+T_n)}^{E_{ox,n}(x_n)} \qquad (4.13)$$

In addition to the eigenvalues and transmission probabilities, the “lifetime” T_{ij} of the electrons in the i,jth electronic state flowing toward the gates from the silicon layer is needed to calculate the leakage current. A useful model for this parameter comes from [32]:

$$\frac{1}{T_{ij}} = \frac{P_{ij}}{\tau_{ij}}\left[(1 - P_b) + \frac{1}{2}P_b^2\right] \qquad (4.14)$$

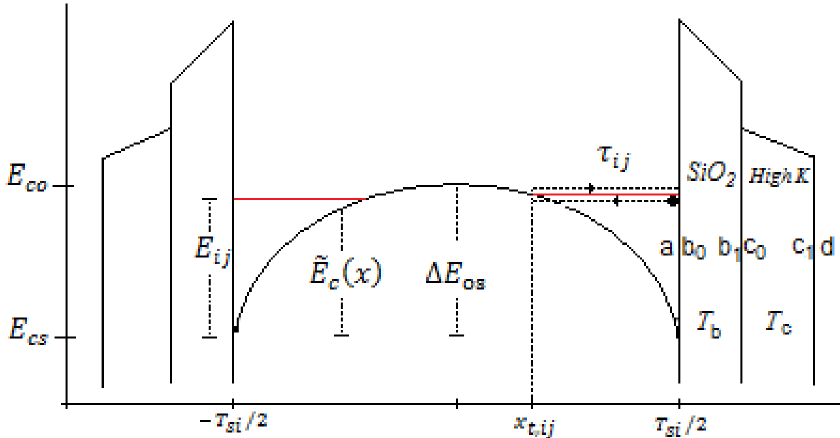


Figure 4-3
Scheme of the transit time for electrons moving perpendiculary to the channel. Also shown are a, b, c and d regions discussed in the text.

where τ_{ij} is the classical transit time of an electron between Si/SiO_2 interface and the classical turning point $x_{t,ij}$ and P_b is the tunneling probability through the conduction band.

Taking the usual definition of the transit time as the integral of the group velocity inverse, namely $\tau_{ij} = 2\int_{x_{t,ij}}^{T_{si}/2} v^{-1}(x)dx$, it can be analytically calculated to yield

$$\tau_{ij} = 2\int_{x_{t,ij}}^{T_{si}/2} \sqrt{\frac{m_{zi}}{2(E_{ij} - \tilde{E}_c(x))}}dx = T_{si}\sqrt{\frac{m_{zi}}{2\Delta E_{\mathrm{os}}}}\ln\left(\frac{\sqrt{\Delta E_{\mathrm{os}}} + \sqrt{E_{ij}}}{\sqrt{\left|E_{ij} - \Delta E_{\mathrm{os}}\right|}}\right) \tag{4.15}$$

This expression is valid for both $E_{ij} \leq \Delta E_{\mathrm{os}}$ and $E_{ij} > \Delta E_{\mathrm{os}}$ cases. A physical interpretation of the transit time is sketched in Figure 4-3.

The tunneling probability P_b for electrons with energies between E_{co} and E_{cs} to cross the conduction band can be calculated with the help of a simplified WKB approximation in the form

$$P_b = exp\left\{-2\int_{-x_{t,ij}}^{x_{t,ij}} \sqrt{\frac{2m_{zi}}{\hbar^2}\left[E_{ij} - \tilde{E}_c(x)\right]}\,dx\right\} \tag{4.16}$$

After some manipulations, P_b could be written as a simple closed-form expression

$$P_b = exp\left(-\sqrt{\frac{m_{zi}\pi^2 T_{si}^2}{2\hbar^2\Delta E_{\mathrm{os}}}}(\Delta E_{\mathrm{os}} - E_{ij})\right) \quad \text{for} \quad E_{cs} < E < E_{co} \tag{4.17}$$

It is worth noting that $\frac{1}{T_{ij}} \sim P_{ij}/(2\tau_{ij})$ for energy levels such as $E_{ij} > \Delta E_{\mathrm{os}}$, for which $P_b = 1$. Conversely, for energies deep in the potential well formed by the electrostatic confinement, then $P_b \sim 0$ and $\frac{1}{T_{ij}} \sim P_{ij}/\tau_{ij}$ similar to the case of a very thick semiconductor.

Finally, combining the results from Eqs. (4.3), (4.7), (4.14) and (4.17), we can readily obtain the total gate direct tunneling current density by adding the contribution of every sub-band:

$$J = \sum_{ij} J_{ij} = \sum_{ij} N_{ij}/T_{ij} \tag{4.18}$$

where, again, N_{ij} (Eq. (4.3)) and T_{ij} (Eq. (4.14)) are the channel charge per unit area and the electron lifetime in the i*th* valley and j*th* sub-band, respectively.

4.3 Results

To calculate the gate current density we have identified E_{ij}, N_{ij}, and P_{ij} as fundamental quantities. In this section we check the accuracy of these quantities and therefore of the proposed compact model. To illustrate the model outcome we only consider the first three states, which contribute the most to the gate direct tunneling current. We also have assumed a flat band voltage V_{fb} equal to zero, corresponding to a midgap gate. The results below show that the model output is in close agreement with the 1D self-consistent SP solution in all operation regions and for wide range of silicon layer and equivalent oxide thicknesses EOT, representative of the design window for nanoscale DG-MOSFETs according to the ITRS document [9].

The location of the energy states E_{11}, E_{12} and E_{21} as a function of the gate voltage is shown in Fig. 4a. In this figure and hereafter solid lines represent self-consistent SP data and symbols are the results of our model. As expected, the energy states values increase as T_{si} is reduced due to the structural confinement. Below the threshold voltage, the band bending is negligible, and the band diagram looks like a square potential well. Beyond the threshold voltage, the electric field strength induces an electrostatic confinement of carriers, resulting in a semi-quadratic potential well. Fig. 4b represents the total charge density and the charge densities $N_{11,}$ N_{12} and N_{21} as a function of the gate voltage for a DG capacitor with 5nm silicon thickness and EOT = 1nm. Here, we see that the E_{21} level contributes significantly to the charge density because its degeneracy and density of states effective mass, despite having a higher energy than the other two levels (see Figure 4-4a). Although we considered only the three states in our model the comparison with numerical results are in very good agreement.

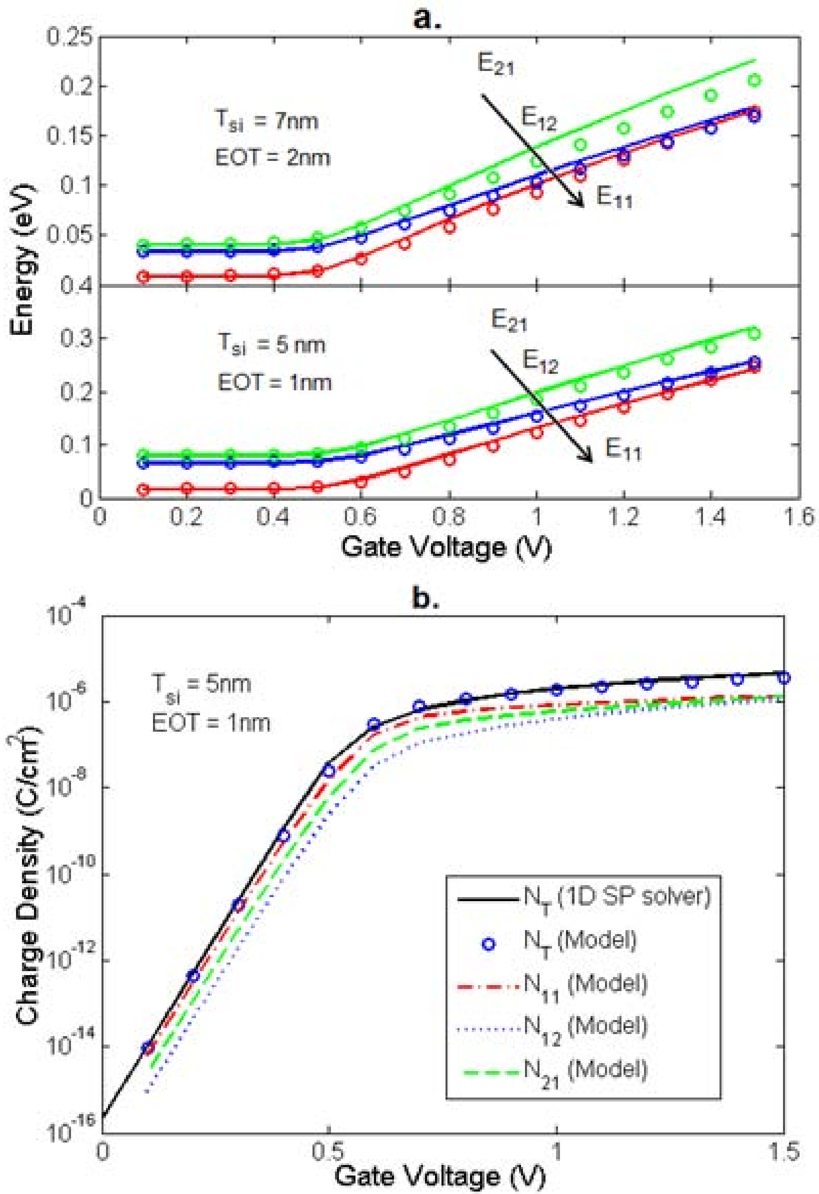


Figure 4-4
(a) Sub-band energies versus gate voltage as calculated from the model (symbols) and 1D self-consistent SP simulator (solid lines); (b) Charge densities of the first states and total charge density (N_T);

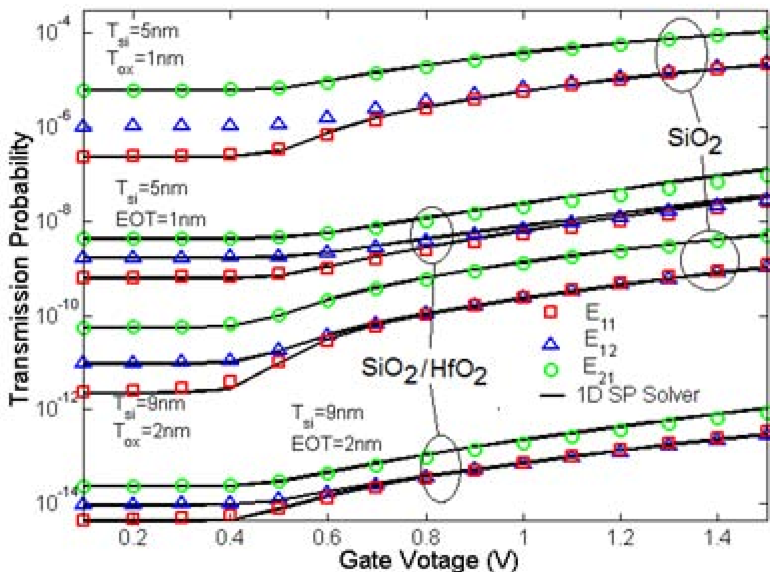


Figure 4-5
Transmission probability of the E_{ij} state through a single-layer of SiO_2 and a SiO_2/HfO_2 dual layer gate oxide.

Figure 4-5 shows the transmission probability P_{ij} as a function of the gate voltage considering as a first case a single layer of SiO_2 as gate oxide and a second case consisting of a SiO_2/HfO_2 dual layer. Here, we can appreciate the strong dependence of the tunneling with the EOT value and its difference with the single-layer SiO_2 case at the same EOT. In general, the transmission probability increases with the gate voltage as a result of the electric confinement in the inversion layer. However this effect is smaller when the body is thinner because the confining electric field is reduced.

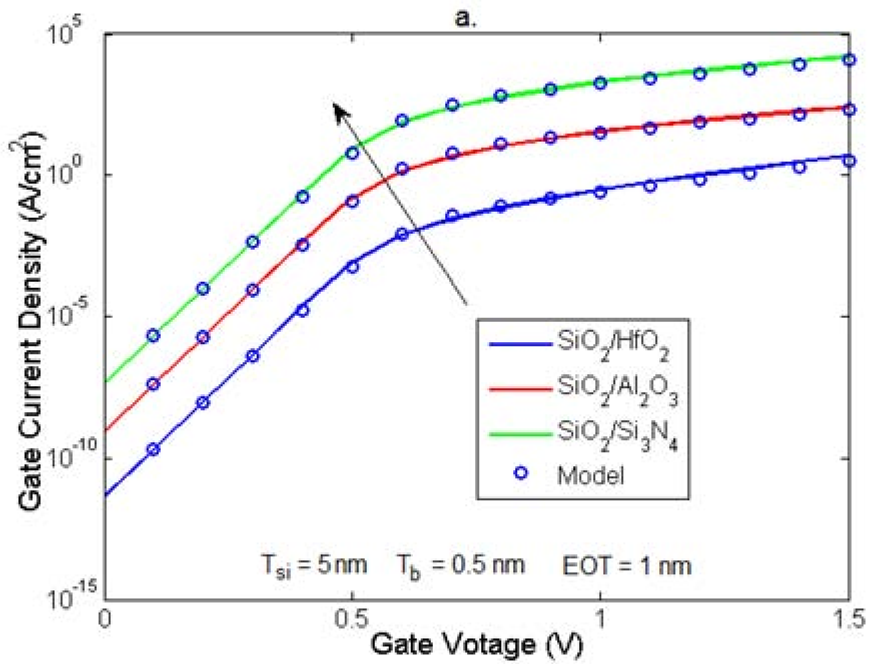
The direct tunneling current density for different dual layer combinations of SiO_2/high-κ materials as a function of the gate voltage has been plotted in Figure 4-6a,b. These results have been obtained using the material related parameters given in Table 4-1. We can see that the SiO_2/HfO_2 combination exhibits the smaller tunneling current. Here the physical thickness of the high-κ layer plays a dominant role, since for the same EOT a higher dielectric constant (25 for HfO2) means a thicker layer, therefore a lower gate current.

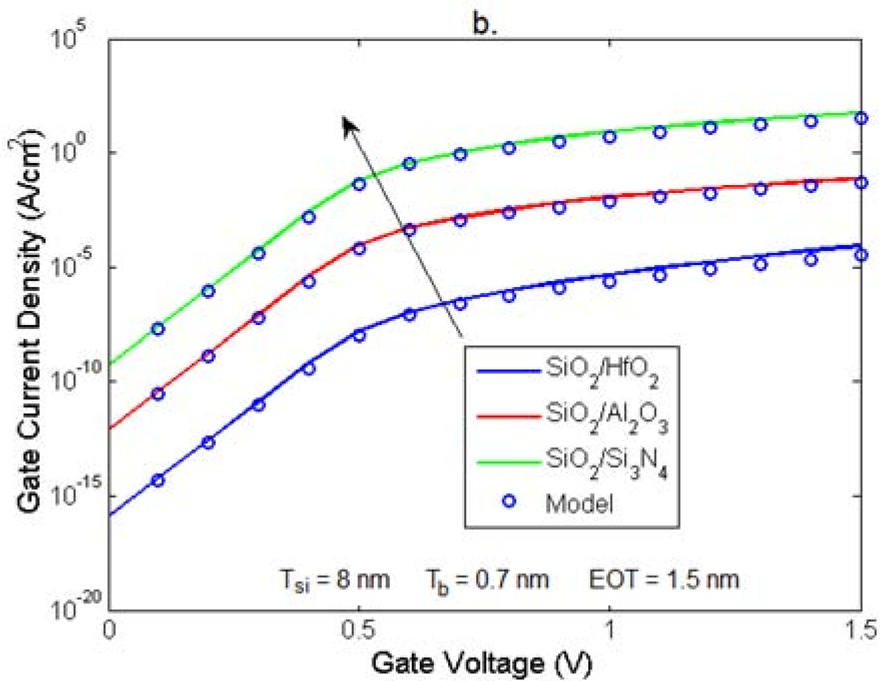
Table 4-1
Parameters for calculation of the direct tunneling gate leakage current considering different high-κ materials.

High-κ	Φ_c (eV)	K	$E_{g,c}$ (eV)	m_n/m_0
Si_3N_4	2.0	7.0	5.3	0.3
ZrO_2	1.4	25	5.8	0.2
Al_2O_3	2.8	9	8.8	0.3
Ta_2O_5	1.1	25	4.4	0.25
HfO_2	1.5	25	5.75	0.18
SiO_2	3.15	3.9	9	0.5

Next we deal with the dependence of the gate leakage current on the thickness of interfacial SiO_2 layer for the SiO_2/HfO_2 hetero-structure keeping constant the EOT. As shown in Figure 4-6c the leakage current can be considerably reduced by keeping the SiO_2 layer as thin as technologically possible.

In these types of structures four gate tunneling mechanisms could occur, depending on the location of the specific energy level respect to the conduction band of the dual-layer insulator: (a) direct tunneling in both SiO_2 and high-κ dielectrics (Figure 4-7a); (b) direct tunneling in SiO_2 oxide and Fowler-Nordheim tunneling in the high-κ dielectric (Figure 4-7b); (c) direct tunneling through the interfacial oxide (Figure 4-7c); (d) Fowler- Nordheim tunneling through the interfacial layer (Figure 4-7d). However, given the fact that the most of the inversion charge is embedded in the first two or three states (Figure 4-4b), it is easy to verify that for gate voltages and materials considered in this work, the dominant tunneling mechanism is the direct tunneling in both layers (Figure 4-7a), for which the condition $\Phi_c - qV_c > E_{ij}$ must be fulfilled. For instance, using values for HfO_2 (lower Φ_c) from Table 1 with $V_g \sim 1.5\,V$ and $T_b \sim 1nm$, $T_c \sim 4nm$, then $\Phi_c - qV_c \sim 1.2V$ and $E_{ij} < 0.4V$ (Figure 4-4a).


a.
10^{5}
10^{0}
10^{-5}
10^{-10}
10^{-15}
Gate Current Density (A/cm^2)
0
0.5
1
1.5
Gate Votage (V)
SiO_2/HfO_2
SiO_2/Al_2O_3
SiO_2/Si_3N_4
Model
T_{si} = 5 nm T_b = 0.5 nm EOT = 1 nm


b.
10^{5}
10^{0}
10^{-5}
10^{-10}
10^{-15}
10^{-20}
Gate Current Density (A/cm^2)
0
0.5
1
1.5
Gate Voltage (V)
SiO_2/HfO_2
SiO_2/Al_2O_3
SiO_2/Si_3N_4
Model
T_{si} = 8 nm T_b = 0.7 nm EOT = 1.5 nm

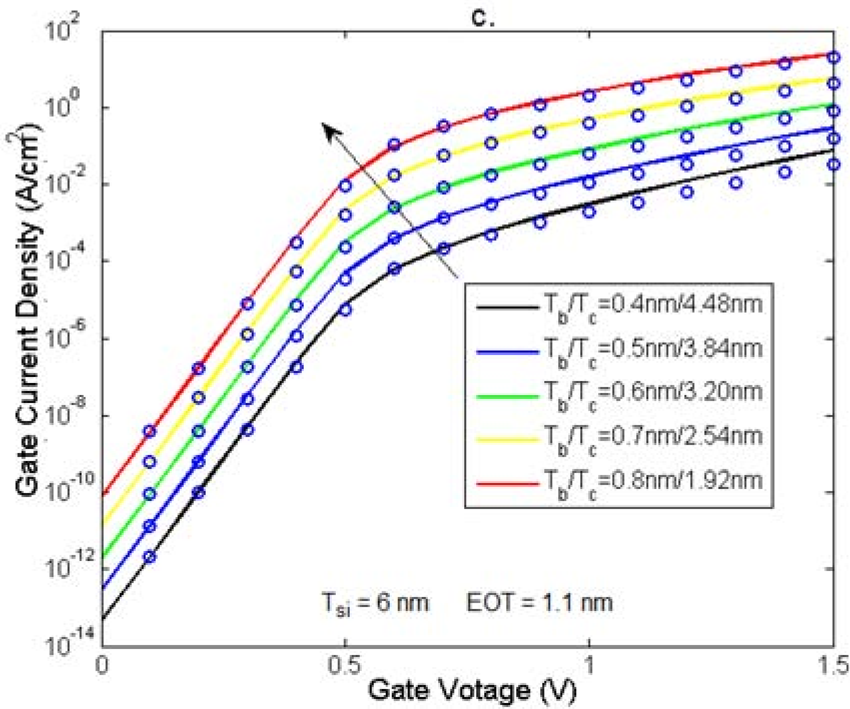


Figure 4-6
(a,b) Direct tunneling gate current density as a function of the gate voltage for different high-κ materials with: (a) $EOT = 1$ nm, $T_b = 0.5$ nm and $T_{si} = 5$ nm; (b) $EOT = 1.5$ nm, $T_b = 0.7$ nm and $T_{si} = 8$ nm. (c) Direct tunneling gate current density as a function of the gate voltage for HfO_2 as high-κ dielectric with $EOT = 1.1$ nm and $T_{si} = 6$ nm.

According to the ITRS 2009 edition, in future technologies the use DG-MOSFETs could start in 2015 with EOT around 1.1nm requiring a maximum gate leakage current density (J_{limit}) of 0.19 A/cm^2 at $V_g = V_{dd} = 1\,V$ for low standby power applications [9]. Figure 4-8 shows the gate current density given by our model, for different high-κ materials, as a function of the SiO_2 layer thickness (T_b) setting EOT = 1.1nm, $V_g = 1V$ and using the parameters given in Table 4-2. In general, the gate current limit could be satisfied in dependence of the SiO_2 layer thickness. For stacks with high-κ material such as Ta_2O_5, HfO_2 and ZrO_2 thickness of SiO_2 roughly lower than 0.7 nm could be needed. On the other hand, materials with lower dielectric constant (K) such as Si_3N_4 and Al_2O_3 could not satisfy the gate current limit requirement. The negative slope exhibited by the Si_3N_4 means that the dominant dielectric in this double layer is the silicon dioxide.

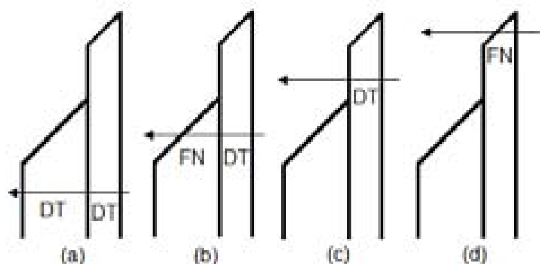


Figure 4-7
Various gate tunneling processes. (a) DT-DT (b) DT-FN (c) DT (d) FN.

4.4 Summary

The gate leakage current is of major concern for nanoscale device operation. For both single-gate and DG-MOSFETs the solution to this problem is to use high-κ dielectrics in gate oxides. In this work the direct tunneling current (dominant process in determining the gate leakage current) through interfacial SiO_2 and high-κ gate stacks have been analytically modeled for symmetric undoped DG-MOSFETs through both layers. It is clear from Figure 4-6a,b that the gate current is reduced for SiO_2/HfO_2 dual layer structure as compared to other SiO_2/high-κ combinations having the same EOT. The tunneling in SiO_2/HfO_2 structure decreases about five orders of magnitude as compared with pure SiO_2 films of the same EOT. For the same EOT a reduced thickness of interfacial layer is beneficial to keep the gate leakage current under control.

The model was checked via comparison with self-consistent SP simulations. All the quantities taking part in the model are explicit closed-form expressions that permit to calculate the dependence of the gate direct tunneling current as a function of the voltage. Because a simple 1D formulation for the electrostatic has been considered in our work, the model can be applied within the validity of the long-channel hypothesis [6]. The presented model makes possible the fast evaluation of the gate leakage current in aggressive scaled DG-MOSFET, being useful in order to find guidelines for the search of an appropriate high-κ dielectric material according to the projections of the ITRS and could be incorporated into general compact model as a building block of future electrical circuit simulators.

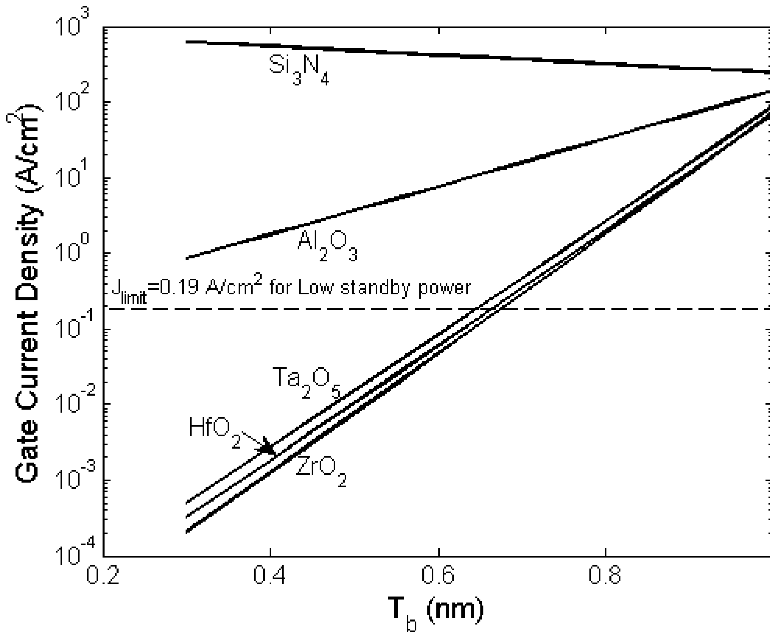


Figure 4-8

Direct tunneling current as a function of the silicon dioxide thickness for several high-κ dielectric materials compared with the maximum gate leakage current density established by the ITRS 2009 edition at EOT = 1nm and $V_g = 1V$.

On the other hand, as mentioned in the introduction of this work, the evolution of the CMOS technology toward the use of Multiple-gate transistors in nanoscale makes mandatory studies on non planar structures such as triple gate, pi-gate, omega-gate, quadruple-gate and surrounding gate. These researches should include accurately the 1D or 2D nature of those devices and particularly to propose models that take into account the electronic wave functions penetration in the gate electrode (metal) to the calculation of the gate tunneling currents. The next chapter describes a numerical model for the description of the gate leakage current of the DG MOSFET based on the Schrödinger-Poisson coupled equations solution, where the electronic wave functions are allowed to penetrate into the metal gate (quasi bound states). For this purpose, the Perfectly Matched Layer (PML) method is embedded in each iteration of the SP solver. The PML method has been adopted because the feasibility to adapt it to devices with non planar geometries.

CHAPTER 5.

Accurate Calculation of Gate Tunneling Current in Double-Gate and Single-Gate SOI MOSFETs Through Gate Dielectric Stacks

5.1 Outline

In this chapter, an accurate description of tunneling in Ultra Thin body Double-Gate and Single-Gate MOSFETs devices through layers of high-κ (HK) dielectrics, which relies on the precise determination of quasi-bound states, is developed. For this purpose the Perfectly Matched Layer method (PML) is embedded in each iteration of a 1D Schrödinger-Poisson solver by introducing a complex coordinate stretching which allows applying artificial absorbing layers in the boundaries.

Similarly to the bulk MOSFET, a way to overcome the limitation imposed by the leakage current is the use of HK materials over a thin SiO_2 interfacial

layer (IL) to form the dual layer gate insulator, keeping a good control of the short-channel effects (SCE) [17]. The IL is either created unintentionally during processing or intentionally deposited to improve the interface quality with the silicon. However, to fully profit from the advantages of HK materials in MOS capacitors with dual layer, the reduction in this IL thickness, at constant EOT (increase of the physical HK thicknees), is desirable [64, 65]. From this point of view two factors favor the scaled toward zero of the IL thickness in the dielectric stacks (DS): the reduction of the direct tunneling current and the improvement of the breakdown-related reliability. Strictly, scaled MG MOSFETs behave as open boundary systems where the electron wave function penetrates the DS and propagates to the metal without reflections. This effect is expected to be highlighted when the IL thickness tends to zero because usually the conduction-band offset or barrier height is inversely proportional to the dielectric constant κ [66]. Therefore in MG MOSFETs the electron states are quasi-bound states (QBS) characterized by complex eigenvalues with the real part corresponding to the energy state and the imaginary part related to the lifetime of the carriers [67].

Hence, accurate models should capture quantum mechanical effects such as discrete QBS and its tunneling to the metal gate through a DS in MG MOS structures. Section 5.2 of this work addresses some lifetime based models used for the calculation of the gate tunneling current, highlighting their validity and applicability. These models are (1) the close boundary based method, (2) the transverse resonant method (TRM) and (3) the method used in this chapter, based on absorbing boundary conditions known as the Perfectly Matched Layer (PML) method. Section 5.3 shows and discusses results of the PML applied to Ultrathin Body Double-Gate (UTBDG) and Ultra Thin Body Single-Gate (UTBSG) with DS consisting of IL/HK, where the IL is assumed to be SiO_2 (see Figure 5-1). Section 5.4 concludes this chapter.

5.2 Models For Gate Tunneling Calculation

The transmission coefficient is a well defined quantity for continuous tridimensional states, where the traveling carriers impact the potential barrier and result in a reflected and transmitted plane wave. However, this concept is not properly defined for localized carrier states. When the silicon body dimensions reach the nanoscale in MG MOSFETs, carriers remain in discrete energy levels and a continuous of energies cannot be considered anymore. It is the same effect that occurs in the inversion layer of a bulk MOSFET forcing a

2D nature of the carriers. Therefore, as Figure 5-2(b) shows, due to the finite barrier height in the DS and to the decreasing of the EOT, the carriers are able to leave these states by tunneling to the gate metal after some time. These states are called, in the presence of leakage current, quasi-bound states (QBS). The average time that a carrier stays in the QBS is called the carrier lifetime in the state. The lifetime concept in a QBS replaces the transmission coefficient of traveling states.

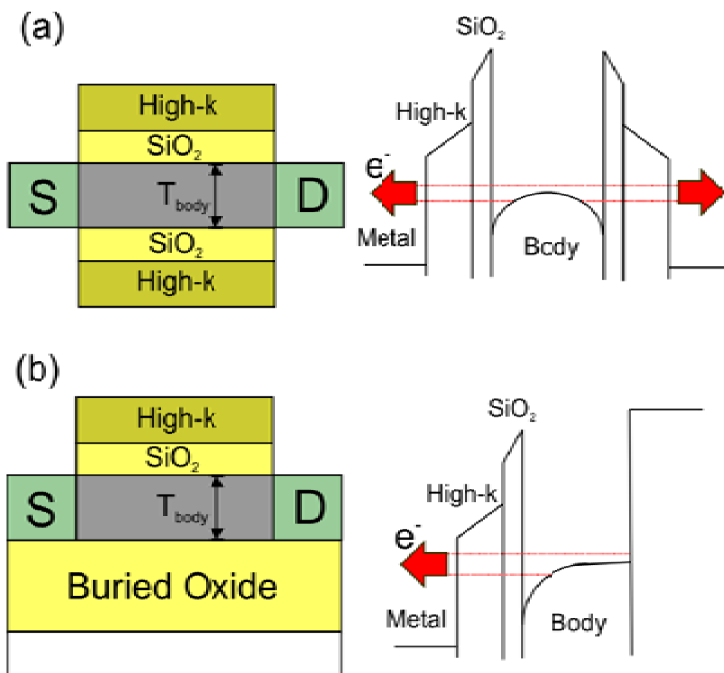


Figure 5-1
(a) Double-Gate (UTBDG) and (b) Single-Gate (UTBSG) MOSFET cross-sections and energy band diagrams. The channel is assumed to be undoped for UTBDG and UTBSG devices.

Indeed, coupling between 2D states at the channel and 3D states in the metal gate through a finite thin gate stack, results in an energy broadening of subbands (Figure 5-2(b)). The energy broadening is inversely proportional to the lifetime of carriers in each subband. The transparency of the barrier is directly reflected in the energy broadening and lifetime concepts. The transparency of a barrier is connected to the height and thickness of that barrier. For a relatively transparent barrier, low or thin, the energy broadening is high and the lifetime is short. In others words, the carriers leave the QBS through a tunnel process with a rather

fast rate and the structure behaves as an open boundary system. On the contrary, for a thick or high barrier, the lifetime is long and energy broadening is negligible, which means that the carriers stay longer on QBS and the tunneling rate is low. In this latter case we can say that QBS transform into bound states and the structure behaves as a closed boundary system.

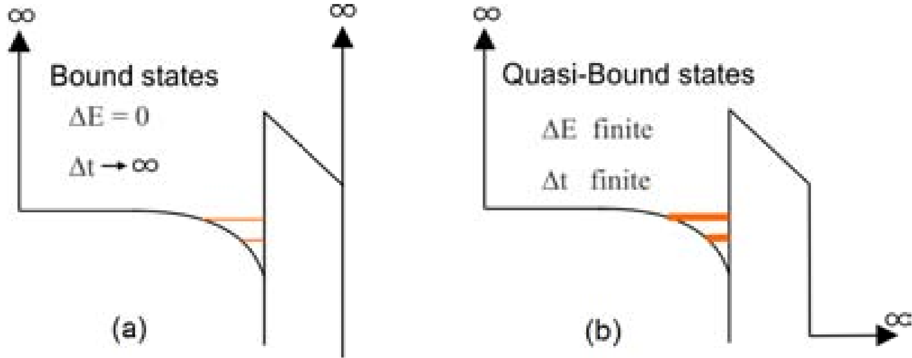


Figure 5-2
(a) Bound (closed boundary) and (b) quasi-bound (open boundary) states in the channel layer of an UTBSG MOS.

5.2.1 Closed boundary based method

Some authors propose to solve the Schrödinger equation applying closed boundary conditions which force the wave function to vanish at either the substrate/dielectric or dielectric/metal interface. Solving the Schrödinger equation with closed boundary conditions leads to discrete bound states with sharp energies $E_{i,j}$, but at the same time this implies that no current could be carried by these states due to vanishing wave functions. The QBS and lifetime concepts explain this paradox and describe the real nature of the 2D carriers. In a quasi-classical approximation, impact frequencies of carriers on the barrier and transmission coefficient are used for the calculation of carrier's lifetime [51, 60, 68]. Here, the lifetime of the carriers located at the jth subband of the ith valley with energy $E_{i,j}$, is defined as

$$\frac{1}{\tau_{i,j}} = T\left(E_{i,j}\right) f\left(E_{i,j}\right) \tag{5.1}$$

where $f\left(E_{i,j}\right)$ and $T\left(E_{i,j}\right)$ are the impact frequency of carriers and transmission coefficient of the barrier, respectively (see Figure 5-3).

The impact frequency of the carrier indicates how many times a carrier hits the barrier per unit time and transmission coefficient is the ratio of successful impacts to the total number of impacts. The impact frequency is related to the kinetic energy and location length of carriers on each subband and can be expressed as follows [68]:

$$\frac{1}{f(E_{i,j})} = 2\int_{x_{t,ij}}^{T_{si}/2} v_{i,j}^{-1}(x)dx = \int_{x_{t,ij}}^{T_{si}/2} \sqrt{2m_{i,j}/\left(E_{i,j} - E_c(x)\right)}\,dx \quad (5.2)$$

where v_{ij} is the group velocity of carriers in the subband, $x_{t,ij}$ refers to the classical turning points of carriers, E_c is the substrate conduction band, T_{si} the substrate thickness and $m_{i,j}$ is the effective mass. The transmission coefficient of a DS barrier takes the form

$$T_{ij} = P_0 \exp\left[-2S_{IL} - 2S_{hk}\right] \quad (5.3)$$

where

$$S_{IL} = \int_{x_1}^{x_2} \kappa_{IL}(x)dx \quad \text{and} \quad S_{hk} = \int_{x_2}^{x_3} \kappa_{hk}(x)dx \quad (5.4)$$

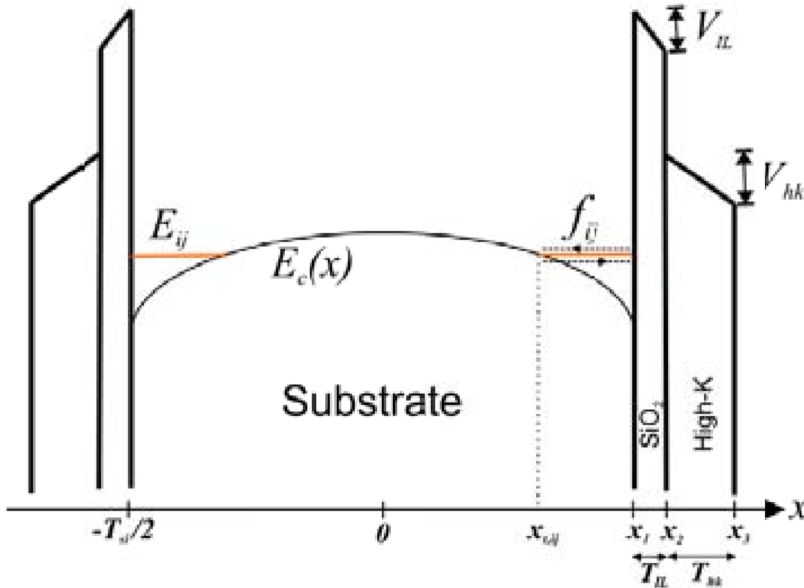


Figure 5-3
Scheme of the conduction band of an UTBDG. Also the impact frequency f_{ij} and classical turning points $x_{t,ij}$ are showed.

are the usual WKB tunneling probabilities. The P_o is a correction term accounting for reflections due to potential discontinuities in the DS barrier [62]. The WKB approximation is widely used for the calculation of the transmission probability. Transfer matrix methods as well as expressions in terms of Airy functions are also applied to the calculation of the transmission probability. However, the aforementioned transmission probability is well defined for 3D states assuming plane waves for incident, reflected and transmitted wave functions, but its application for 2D states is questionable.

Finally, using a close boundary based method, the gate current density of every bound-state can be calculated as $J_{ij} = N_{i,j}(E_{ij})/\tau_{i,j}(E_{ij})$ where $N_{i,j}$ is the channel charge per unit area of every subband, and calculated solving the Schrödinger-Poisson (SP) coupled equations. Although this is a fast computational method it can result in inaccuracies depending on the correction term of Eq. (5.3) and the dispersion relations used to evaluate Eq. (5.4).

5.2.2 Transverse resonant method

A direct calculation of the lifetime without using the transmission coefficient concept was suggested by Lo *et al.* [10], based on the close analogy between the confined electrons in a varying potential and electromagnetic waves in a waveguide with varying refractive index. This analogy allows the utilization of the transverse resonant method (TRM) [69], commonly used for finding the eigenvalues of inhomogeneously filled waveguides and dielectric resonators. To apply this method the structure is divided into intervals of width *d* of a 1D grid along the direction perpendicular to the substrate/dielectric interface. The TRM defines the intrinsic impedance $\eta_l = m_l/k_l$, where m_i is the carrier effective mass and k_l is the wave number, and the terminal impedances of each interval $\overleftarrow{Z}_l$ and $\vec{Z}_l$, where the arrows indicate the impedance looking to the left or right. Considering an interval in the silicon layer and applying the transmission-line transformations as shown in Eq. (5.5) repeatedly, $\overleftarrow{Z}_l$ and $\vec{Z}_l$ could be expressed in terms of $\overleftarrow{Z}_1, \overleftarrow{Z}_2, \dots, \overleftarrow{Z}_{l-1}$ and $\vec{Z}_{l+1}, \dots, \vec{Z}_{N-2}, \vec{Z}_{N-1}$ respectively.

$$\overleftarrow{Z}_m = \eta_m \frac{\overleftarrow{Z}_{m-1} - j\eta_m \tan(k_m d_m)}{\eta_m - j\,\overleftarrow{Z}_{m-1}\tan(k_m d_m)} \qquad m = 2,3,\dots,l.$$

$$\vec{Z}_m = \eta_{m+1} \frac{\vec{Z}_{m+1} - j\eta_{m+1} \tan(k_{m+1} d_{m+1})}{\eta_{m+1} - j\,\vec{Z}_{m+11} \tan(k_{m+1} d_{m+1})} \qquad m = N-2, N-3, \ldots, l. \tag{5.5}$$

Under resonant conditions the terminal impedances to the left and right should satisfy $\overleftarrow{Z}_l + \vec{Z}_l = 0$. This condition would be satisfied with a complex energy $\varepsilon = E - j\Gamma$, whose imaginary part Γ is related to the energy broadening of leaky QBS. This information allows the carrier's lifetime on each subband to be determined as follows:

$$\tau = \frac{\hbar}{2\Gamma} \tag{5.6}$$

Some authors [10, 70] use a SP solver with closed boundary conditions to generate the potential profile and then the TRM to find the complex energies and to calculate the gate tunneling current. This procedure may result in inaccuracies especially with the aggressive scaling of the EOT in MG devices. On the other hand, in order to calculate the complex energy with the resonant conditions, complicated nonlinear equations must be solved, requiring the use of iterative methods hindering the application of the TRM on non-planar MG MOSFETs, such as the SOI FinFETs, SOI Tri-Gate, SOI Pi-Gate, SOI gate-all-around or bulk Tri-Gate [17].

5.2.3 Perfectly Matched Layer Method

In the present work a method based on absorbing boundary conditions for Schrödinger's equation, which is often used in electromagnetic waves with unbounded domains, has been applied to determine the energy levels and the lifetime broadening of QBS in UTBDG and UTBSG MOSFETs with HK materials as gate dielectrics. It is known as the Perfectly Matched Layer (PML) method [71]. In contrast to the TRM, here all the QBS are calculated in one step and no iteration procedures are needed. In addition, the PML method can be extended to 2D and even 3D regions with different geometries [72] making it suitable for non- planar MG MOSFETs. This technique accounts for the wave function penetration into the metal gate, thus allowing a more accurate estimation of the electrostatic potential, quasi-bound states, charge and carrier lifetime [67].

The PML method is based in the addition of non-physical absorbing layers at the boundary of the simulating regions of interest [73] (see Figure 5-4). An absorbing boundary layer is a layer of a simulated artificial absorbing material that is placed adjacent to the edges of the grid. When a wave penetrates the absorbing layer, it is attenuated by the absorption and decays exponentially. The problem with this approach is that, whenever there are transitions from one material to another, waves generally reflect, and the transition from non-

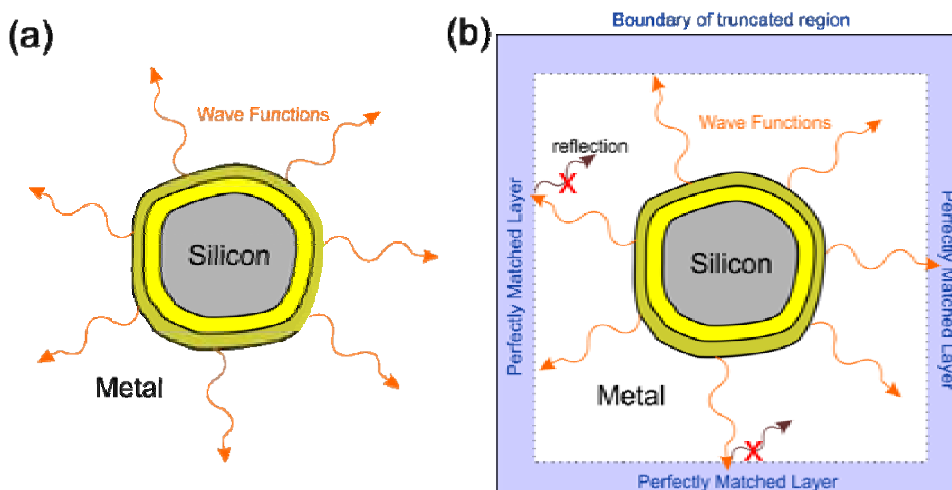


Figure 5-4
(a) Schematic of a typical leakage current problem, in which there is some finite region of interest (silicon + DS), from where some electron wave functions escape to the metal. (b) The same problem where the space has been truncated to a finite computational region. An absorbing layer is placed adjacent to the edges of the computational region –a perfect absorbing layer would absorb outgoing waves without reflections from the edge of the absorber.

absorbing to absorbing material is not an exception so, instead of having reflections from the grid boundary, now there are reflections from the absorber boundary. However, Berenger [73] showed that a special absorbing medium could be constructed so that waves do *not* reflect at the interface: a *perfectly matched layer*, or PML. Although PML was originally derived for electromagnetism (Maxwell's equations), the same ideas are immediately applicable to electron wave functions (Schrödinger's equation). The QBS (eigenstates of the open system) are determined by the eigenvalues of the non-Hermitian Hamiltonian of the system which admits complex eigenvalues $\varepsilon = E - j\Gamma$. The QBS lifetimes are related to the imaginary parts of the

eigenvalues as $\tau = \hbar/2\Gamma$. To implement the PML-absorber regions, complex stretched coordinates $\tilde{x}$ are defined by a stretching factor s_x for the coordinate x:

$$\tilde{x} = \int_0^x s_x(x')dx' \tag{5.7}$$

resulting in

$$\frac{\partial}{\partial \tilde{x}} = \frac{1}{s_x(x)} \frac{\partial}{\partial x} \tag{5.8}$$

In particular, the stretching function $s_x(x)$ can be defined, with good result [67], as:

$$s_x(x) = \begin{cases} 1 + (\alpha + j\beta)x^2 & \text{for the PML region} \\ 1 & \text{for the physical region} \end{cases} \tag{5.9}$$

where x is a normalized variable, being $x = 0$ at the interface between the physical and the PML regions and $x = 1$ at the end of the PML region, and parameters α and β are explained below. Because of the integral form Eq. (5.7) the coordinate gradually is transformed and so the wave functions decay to zero (Figure 5-5).

Assuming a constant potential within the PML region, the wave function can be written as a plane wave $\psi(x) = \psi_0 \exp(j\tilde{k}_x x)$ with the wavevector $\tilde{k}_x = k_x/s_x$. Considering two points in the PML region x_1 and $x_2 = x_1 + dx$ the wavevector at the point x_2 can be approximated as

$$k_x(x_2) \approx \frac{s_x(x_2)}{s_x(x_1)} k_x(x_1) = 1 + (\alpha + j\beta)dx \tag{5.10}$$

Therefore, the parameter α scales the phase velocity of the plane wave, while β acts as a damping parameter. Since this damping coefficient is greater than zero in the absorbing region, the envelope of the wave function decay to zero, as can be seen in Figure 5-5. These parameters, as well as the thickness of the absorbing layer can be varied over a wide range with virtually no influence on the results, as long as there are no reflections at the boundaries. However, to achieve this goal, the complex stretching function and its first derivative have to be continuous.

5.3 Gate Tunneling Current using the PML method

Due to the confinement of electrons in planar structures such as those considered in Figure 5-1, quantum mechanical tunneling has significant effects on their electric characteristics. The main mechanism for tunneling of electrons through the DS is represented by QBS. In this section the numerical estimation of the gate tunneling current is obtained for devices considered in Figure 5-1. Physical parameters defining the structures are T_{si}, T_{ox} (when the SiO_2 is the only gate dielectric) and T_{IL}, T_{hk} (for dual layer gate dielectrics). A workfunction

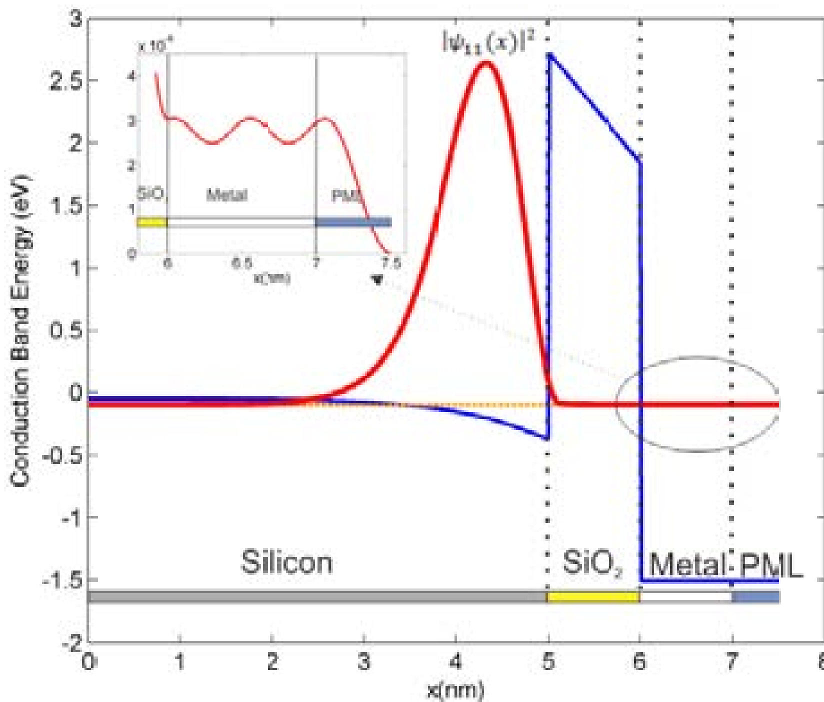


Figure 5-5
Ground state squared wave function (red solid line) and electron conduction band (blue solid line) of an UTBSG MOSFET along the whole simulation domain. The inset shows the oscillations of the wave function in the metal and its decay in the PML region.

difference between the silicon body and the gate metal producing a flatband voltage $V_{fb} = -0.31$ eV has been assumed. Note that we have considered an undoped body. We first solve the 1D SP equations self-consistently, where

electron wave function is allowed to penetrate to the gate metal through the DS (see Figure 5-5) via the implementation of the PML method in each iteration. Similarly to Ref. [67], in Eq. (5.9) $\alpha = 1$ and $\beta = 1.4$ have been assumed, with good results. From this solution, we obtain the potential profile, the complex eigenvalues $\varepsilon_{ij} = E_{ij} - j\Gamma_{ij}$ and the eigenstates ψ_{ij} (complex wave functions) of the ij^{th} state. The effective-mass Schrödinger equation, Eq. (5.11), is solved in the silicon, gate dielectric(s), metal and PML regions whereas the Poisson equation (Eq. (5.12)) is solved in the silicon and gate dielectric(s) regions:

$$\left[-\frac{\hbar}{2}\frac{1}{s_x(x)}\frac{d}{dx}\frac{1}{m_{zi}(x)}\frac{1}{s_x(x)}\frac{d}{dx} + V(x) - \varepsilon_{ij}\right]\psi_{ij}(x) = 0 \qquad (5.11)$$

and

$$\frac{d}{dx}\left[\epsilon(x)\frac{d}{dx}\right]\phi(x) = \frac{q}{\epsilon_0}\left[n(x) - p(x) + N_A^- - N_D^+\right], \qquad (5.12)$$

where s_x is the stretching function as given in Eq. (5.9), m_i is the electron effective mass in the ith valley, V is the potential energy, and N_A^- and N_D^+ are the ionized acceptor and donor concentration, respectively, assumed to be zero for the undoped devices examined in this work. The potential energy $V(x)$ in Eq. (5.11) is related to the electrostatic potential $\phi(x)$ in Eq. (5.12) as $V(x) = -q\phi(x) + \Delta E_c(x)$, where $\Delta E_c(x)$ is the energy barrier difference produced by the band offset between silicon and every dielectric layer. The wave function $\psi_{ij}(x)$ in Eq. (5.11) and the electron density $n(x)$ in Eq. (5.12) are related by

$$n(x) = \left(\frac{kT}{\pi\hbar^2}\right)\sum_{ij} g_i m_{di}^* \ \ln\left[1 + e^{(E_f - E_{ij})/kT}\right]\left|\psi_{ij}(x)\right|^2 \qquad (5.13)$$

where g_i and m_{di}^* are the degeneracy and the DOS effective mass of the ith valley respectively (Table 5-1). For [100] silicon $m_l = 0.92m_0$ and $m_t = 0.19m_0$, where m_0 is the free electron mass [67]. Also, the values used in our numerical calculations related to the dielectric regions are taken from Ref. [66] and summarized in Table 5-2.

Table 5-1
Parameters for [100] silicon.

i^{th} valley	g_i	m_{di}^*	m_i
1	2	m_t	m_l
2	4	$\sqrt{m_t m_l}$	m_t

Table 5-2
Parameters for calculation of the direct tunneling gate leakage current considering different high-κ materials.

High-κ	ΔE_c (eV)	$K = \epsilon/\epsilon_0$	m_{zi}/m_0
SiO_2	3.15	3.9	0.45
Si_3N_4	2.0	7.0	0.5
Y_2O_3	2.3	15	0.25
HfO_2	1.5	25	0.18

Then, the total tunneling current density can be obtained by adding currents due to each energy level according to

$$J = \sum_{ij} J_{ij} = q\left(\frac{kT}{\pi\hbar^2}\right)\sum_{ij}\frac{g_i m_{di}^*}{\tau_{i,j}(E_{ij}(m_i))}\ln[1 + e^{(E_f - E_{ij})/kT}] \quad (5.14)$$

Next, the simulator developed in this work is compared against the measurement and simulation results from [58]. The device under test is an UTBSG MOSFET with several SiO_2 thicknesses T_{ox} and no HK dielectric layer has been included. Figure 5-6 shows that the gate current density values closely follows the results from Ref. [58] where the simulations were made with the TRM described in Section 5.3 and experimental data are reported.

Figure 5-7 illustrates, for an UTBSG MOSFET, the energy difference for the ground state E_{11} considering open or closed boundary conditions as a function of the gate voltage V_g. Even for SiO_2 thicknesses T_{ox} values as thin as 0.3 nm, without a HK dielectric, that difference is just in the order of 10 meV for gate voltages as high as 2V. Important differences could arise, however, when low barrier height insulators are considered. This is illustrated in Figure 5-8 showing the effect of the wave function penetration in the metal for the ground state over four different dielectric materials (Hypothetical SiO_2 where the barrier height is virtually changed, HfO_2, Y_2O_3 and Si_3N_4). In all cases the IL is absent. Hypothetical SiO_2 means a dielectric with SiO_2 properties, except the band offset energy, which is arbitrarily modified to display the E_{11} decreasing effect. The results show that the difference in energy could be as high as 100meV for the HfO_2 case, which has the lower barrier height of oxides considered in this analysis. Differences much smaller than 10meV are expected when an IL is included.

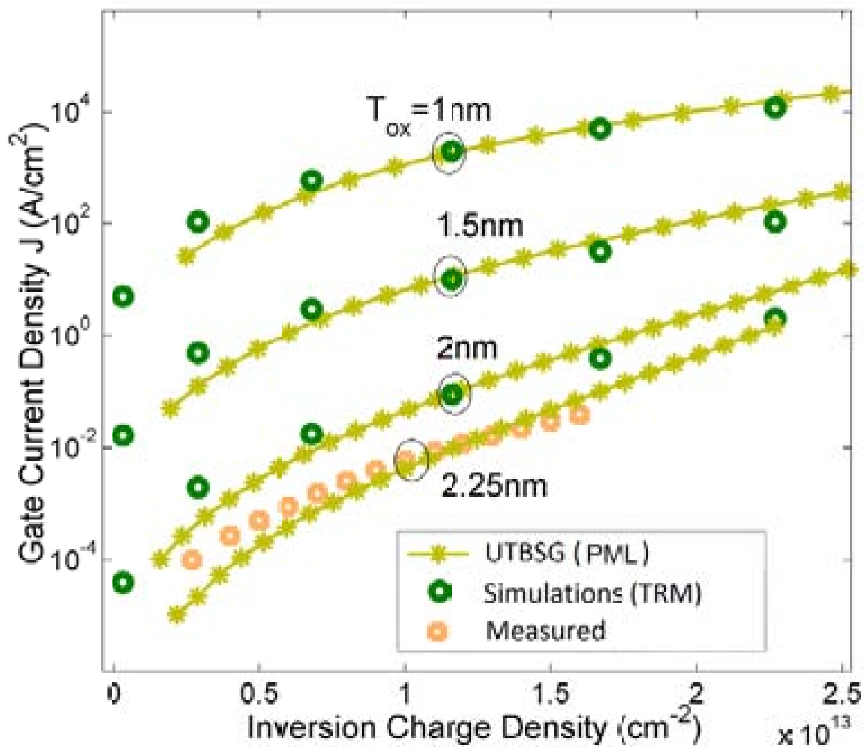


Figure 5-6
Comparison of our results (PML method) with those of Ref. [58], where TRM based simulations and experimental data were reported. Here we used $T_{si} = 10\text{nm}$.

A comparison of the gate current between an UTBSG and an UTBDG as a function of the channel charge density for several SiO_2 thicknesses (without HK dielectric) is shown in Figure 5-9, revealing that for the same charge density the gate current in the UTBSG is larger than in the UTBDG. For UTBSG and UTBDG MOSFETs, the gate current is reduced respect to the bulk MOSFET, due to the smaller vertical electric field near the bottom of the inversion layer, as discussed in Ref. [58]. This reduces the electrical confinement, which lowers the QBS energy, thus resulting in smaller tunneling probability and an increased lifetime of each QBS. Only the SiO_2 faces the problem of very large gate current densities ($J \gtrsim 1\text{A/cm}^2$). For this reason, alternative HK dielectrics have been considered to overcome the large increase of the gate leakage current accompanying the scaling.

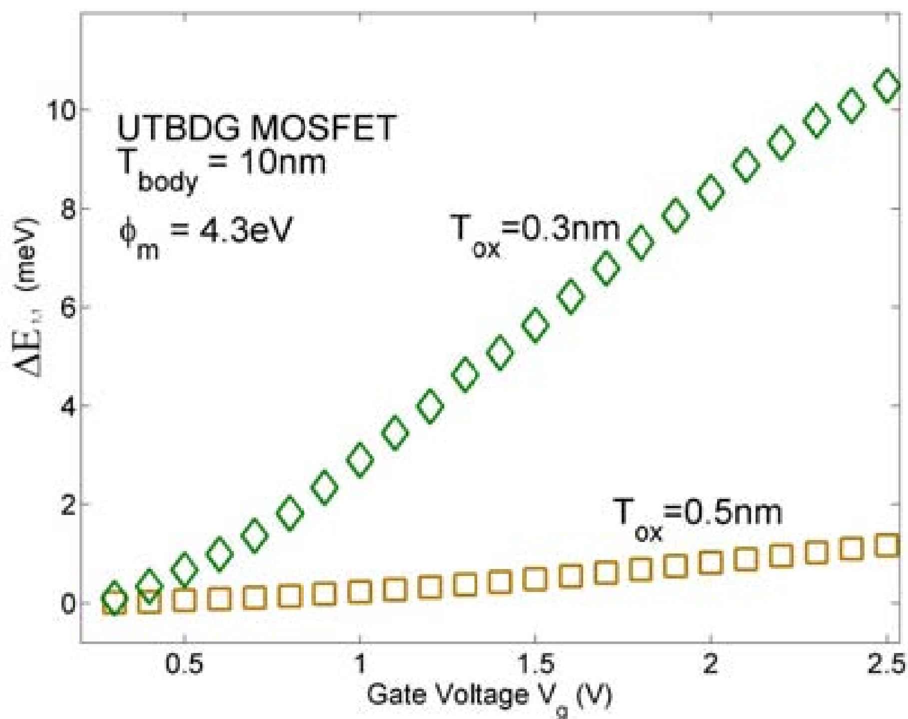


Figure 5-7
Energy difference ΔE_{11} of the ground state with and without considering the wave function penetration in the metal gate through a SiO_2 layer as a function of the gate voltage V_g.

Next, we have performed simulations of the gate current for both UTBSG and UTBDG devices (see Figure 5-10). Different gate DS using HK materials from Table 5-2 have been considered. We found again that the gate current in UTBSG devices is larger than in the UTBDG for the same charge density.

In structures with DS consisting of dual layer (IL+HK), given a gate voltage value, four gate tunneling mechanisms could appear, depending on the location of the specific energy level respect to the conduction band of insulators: (a) direct tunneling in both IL and HK (DT-DT); (b) direct tunneling in the IL and Fowler-Nordheim tunneling in the HK (DT-FN); (c) direct tunneling through the IL (DT) and (d) Fowler-Nordheim tunneling through the IL (FN). For the materials and voltage range considered in this work only mechanisms (a) and (b) are relevant (see Figure 5-11).

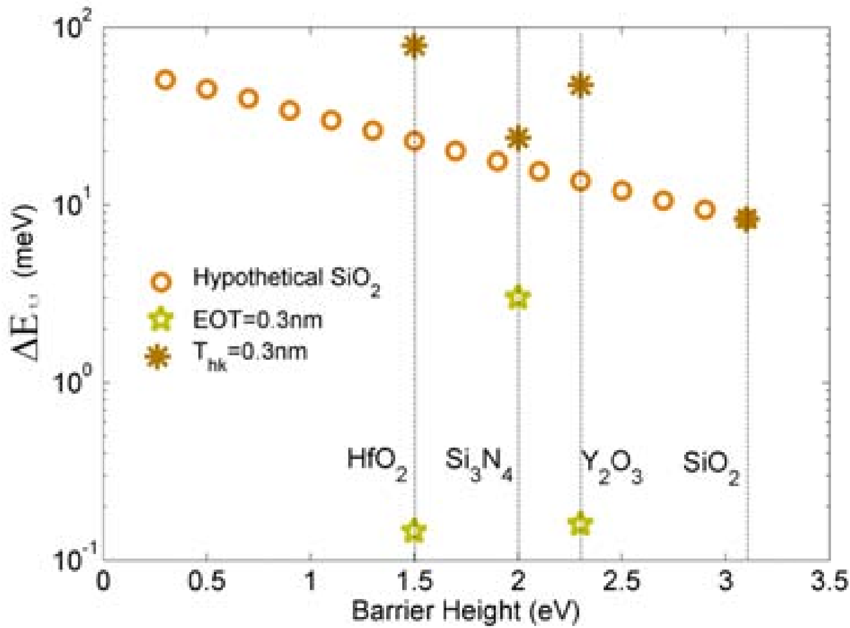


Figure 5-8
Energy difference ΔE_{11} of the ground state with and without considering the wave function penetration in the metal gate as a function of the barrier height. No IL has been considered (only one gate dielectric) and $\mathrm{EOT} = (3.9/\kappa)T_{hk}$.

From Figure 5-10 we can see that the SiO_2/HfO_2 and SiO_2/Y_2O_3 combinations prevent the gate leakage as compared to other material combinations. For V_g values smaller than roughly 1V, the HfO_2 reduces more strongly the gate current than the Y_2O_3. This is because for EOT = 1nm the HfO_2 thickness is 3.2nm while the Y_2O_3 thickness is 1.92nm. Besides, in both cases the QBS that contain most of the charge (lowest energy levels) experience a potential so high that can be considered infinite (Figure 5-11(a)). However, when $V_g \gtrsim 1\,V$, for the SiO_2/HfO_2 case, the gate tunneling suffers a huge increase because the lowest QBS start to feel a finite potential and the HK barrier height becomes a relevant parameter (see Figure 5-10(b) and Figure 5-11(b)). This condition is given when the charge density is approximately 10^{13} cm^{-2} in UTBSG and $2*10^{13}$ cm^{-2} in UTBDG. Then, when the gate voltage increases up to ~2V, any of the QBS tunnels through the SiO_2/HfO_2 via DT-DT mechanism (Figure 5-11(d)). On the contrary, for the SiO_2/Y_2O_3 system the lowest QBSs tunnel via DT-DT due to the larger HK barrier height (Figure 5-11(c)). We can conclude that not only the physical thickness of the HK layer plays an important role, but also the barrier height is crucial in determining the

gate tunneling current. Notice that for the same EOT a higher dielectric constant (25 for HfO_2) means a thicker layer and therefore a lower gate current. Other tunneling effects via either DT or FN mechanism could appear whenever the body is made very thin (energy levels go up) or the gate voltage is high enough.

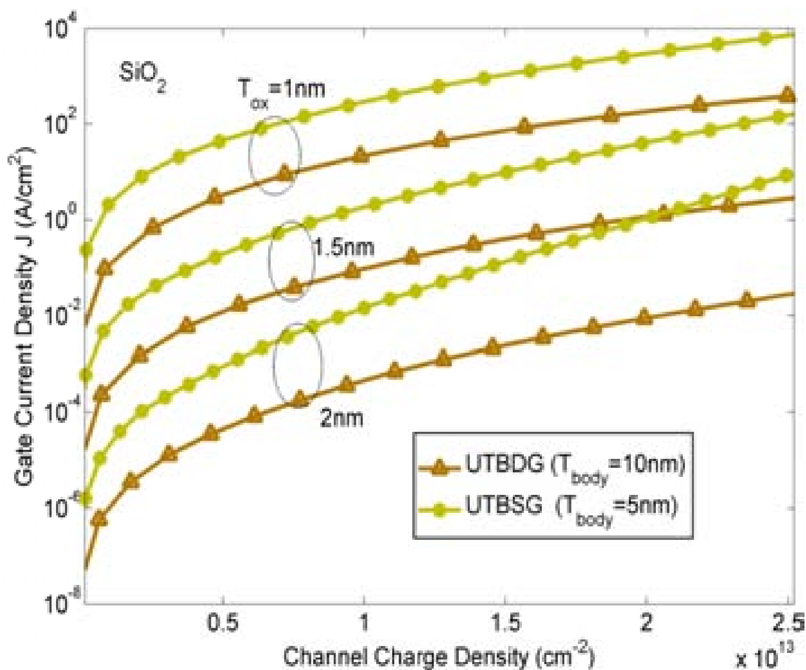


Figure 5-9
Gate current density in both UTDSG and UTBDG MOS structures through a SiO_2 layer as a function of the channel charge density.

Nevertheless, according to the ITRS 2009 edition [9] future technologies using MG as the Double-Gate MOSFETs could start to be in production by 2015 with EOT around 1.1 nm, requiring a maximum gate leakage current density ($J_{g,limit}$) of 0.19 A/cm^2 at $V_g = V_{dd} = 1\,V$ for low standby power applications. Figure 5-12 shows the gate current density predicted by our calculations, for different HK materials, as a function of the IL thickness setting EOT = 1.1nm, $V_g = 1V$ and using the parameters given in Table 5-2. In general, the gate current limit could be satisfied depending on the IL thickness. For DS with HK materials such as Y_2O_3 and HfO_2, IL thicknesses roughly lower than 0.7nm could be needed. On the other hand, materials with lower dielectric constants such as Si_3N_4 could not satisfy the gate current limit requirement.

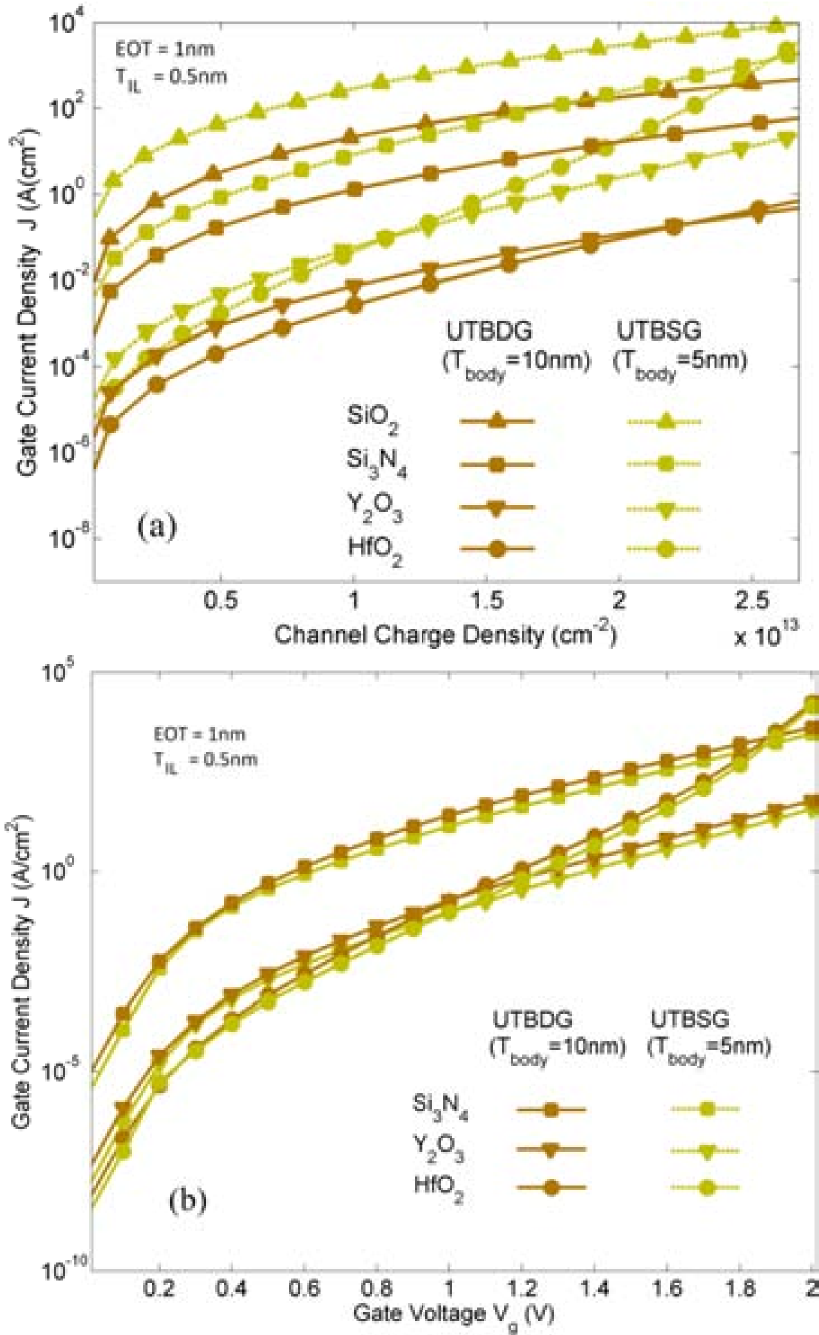


Figure 5-10
Gate current in both UTBSG and UTBDG MOS structures through several DS as a function of: (a) the channel charge density; (b) the gate voltage.

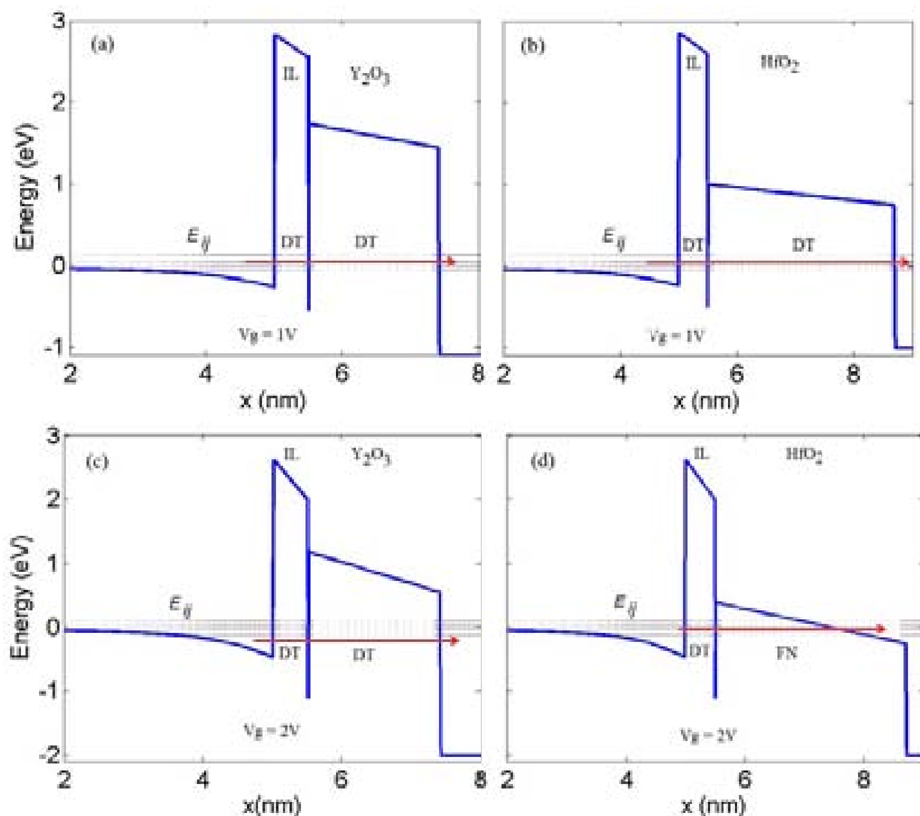


Figure 5-11
Various gate tunneling mechanisms through a DS in UTBSG MOS and location of the lowest energy levels respect to the conduction band.

5.4 Summary

Multi-gate MOSFETs in combination with high-κ materials as gate dielectrics have been investigated as a successors of the single-gate MOSFET for the next technology nodes. Three different models for the calculation of the gate tunneling current have been presented and benchmarked, including some discussion about the eventual application of these models to non-planar SOI MOSFETs. The PML method is explained and developed allowing an accurate calculation of the gate tunneling current in UTBSG and UTBDG MOSFETs with dual layer gate dielectrics. We have found that the introduction of the PML method is recommended to accurately capture the eigenergies of QBS in low barrier height materials. Remarkably, a close agreement between our simulations and experimental results for UTBDG MOSFETs reported in the literature has

been obtained. Finally, we found that HK materials, such as Y_2O_3 and HfO_2, in combination with an IL with thickness roughly lower than 0.7 nm could be needed to satisfy the gate current limit projected by the ITRS 2009.

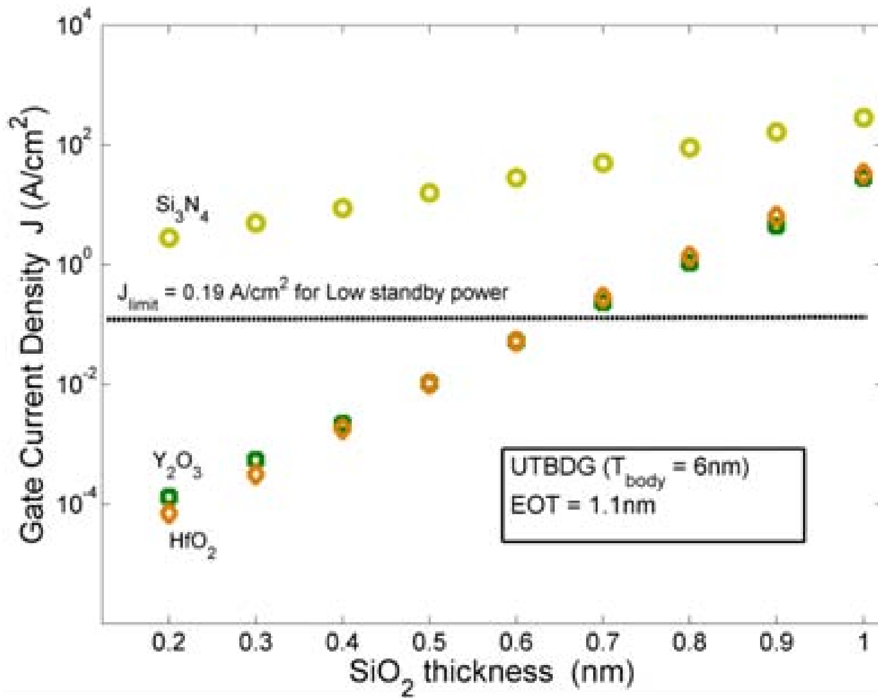


Figure 5-12
Direct tunneling current in UTBDG MOS as a function of the IL thickness for several HK materials compared with the maximum gate leakage current density projected by the ITRS at EOT = 1.1 nm and $V_g = 1V$.

APPENDIX A

Analytical Solution for ξ Parameter

In this Appendix, we describe a three step method to solve Eq. (2.16) in analytic way.

Before presenting a method for the solution in more detail, it is convenient to make the following replacement $\beta = arctan\,(z)$. Thus, the Eq. (2.16) changes and the problem can be redefined as finding out z from

$$f(z; m, F) = \frac{1}{2} ln(1 + z^2) + m\,z\,\arctan(z) - F = 0 \qquad \text{(A1)}$$

1. Compose a continuous starting function as the initial approximation.

The first step gives a rough estimation of the surface potential as an explicit continuous function of gate voltage, quasi-Fermi potential, etc. It is the most important step and the determinant factor of the method. The function should not be too complicated but must be close enough to the exact implicit solution. The feasibility of this general method lies on whether we can find a proper starting function. If the implicit equation can be largely simplified in the region well above or below threshold, the asymptotic limits can be easily obtained. Using an appropriate smoothing function to join two asymptotic behaviors, we may achieve an ideal initial approximation.

The starting function (z_1) can be obtained from the asymptotic behavior of z

$$z = \sqrt{\frac{F}{m}} \quad (\text{as } z \to 0); \quad z = \frac{2F}{\pi m} \quad (\text{as } z \to \infty) \tag{A2}$$

and using the following smoothing function to connect them:

$$z_1 = \sqrt{\frac{8}{\pi^2 m^2}\left(1 + \sqrt{\frac{F}{m}}\right) + \left(\frac{2F}{\pi m}\right)^2} - \frac{8}{\pi^2 m^2} \tag{A3}$$

2. Modify the starting function with a high-order correction.

The starting function is just a crude estimation and is far from accurate. To achieve accuracy, a third-order correction is used in [41] to modify the starting function. Although the third-order correction in [41] is described in a concrete manner and applicable to the specific equation, it is easy to reorganize to satisfy our purposes. Assume that we are going to solve the implicit equation $f(z; m, F) = 0$, where z is to be solved, and m and F are independent variables. Initially z is approximated by $z_1(m, F)$.

The f function can be expanded into Taylor series to the third order near z_1 to yield:

$$f(z; m, F) \approx f_0 + f_1 h + f_2 h^2 + f_3 h^3 = 0 \tag{A4}$$

where $f_n = \frac{1}{n!}\frac{\partial^n f}{\partial z^n}\Big|_{z=z1}$ for $n = 0,1,2,3$ and $h = z - z_1$.

The cubic equation has exact solutions. However, considering that h a small quantity, the solution should be approximately simplified into a rational form for the purpose of efficiency. It is well known that arithmetic operations are much faster that the square root and cubic root. Following the steps in [74], we can obtain a possible rational solution for (A4) and it can be expressed as:

$$h_1 = -\frac{f_0}{f_1}\left[1 + \frac{f_0 f_2}{2{f_1}^2} + \frac{{f_0}^2\left(3{f_2}^2 - f_1 f_3\right)}{6{f_1}^4}\right] \tag{A5}$$

Because the third order results in accurate calculations we do not attempt to work at higher orders. Hence, a first solution to Eq. (A1) is $z_2 = z_1 + h_1$.

3. Make another correction to improve accuracy.

Although a rough estimation evolves into an accurate one through the last step, another correction may be needed to further improve the accuracy to reach a prescribed accuracy. Then we apply one more step, which is similar to the last one.

To refine previous solution (z_2) we apply the outlined procedure yielding $z_3 = z_2 + h_2$, where h_2 corresponds to the second correction and in this case $g_n = \frac{1}{n!}\frac{\partial^n f}{\partial z^n}\Big|_{z=z2}$.

$$h_2 = -\frac{g_0}{g_1}\left[1 + \frac{g_0 g_2}{2{g_1}^2} + \frac{{g_0}^2\left(3{g_2}^2 - g_1 g_3\right)}{6{g_1}^4}\right] \quad \text{(A6)}$$

Finally, the above procedure provides an explicit expression for β^* (and ξ^*), which is an approximate solution of Eq. (2.16):

$$\xi^* = \beta^* \frac{2}{\pi} e^{-q(\phi_0 - \phi_{0max})/2kT} \quad \text{(A7)}$$

where

$$\beta^* = \arctan(z_1 + h_1 + h_2) \quad \text{(A8)}$$

APPENDIX B

Predictor-Corrector Algorithm to Solve SP Equations with PML

In this Appendix a fast and robust iterative method for obtaining self-consistent solution to the coupled system of the Schrödinger's and Poisson's equation, considering the metal oxide semiconductor structure as an open system, is presented. The iterative method is based on a previous work developed by A. Trellakis [75, 76] that uses a predictor-corrector procedure for the solution of the coupled system of differential equations. As a novelty, the Perfectly Matched Layer (PML) method is embedded in each iteration to permit the penetration of the electronic wave functions into the metal electrode and thus to obtain electron lifetime information relevant in the calculation of the gate tunneling current. It should be noted that both the predictor-corrector technique as well as the PML method have been adopted in this work by their efficiency and stability, together with the ability to tackle two-dimensional quantum structures.

1. Physical Model

The physical model used for the description of quasi bound states (QBS) in the perpendicular direction to the channel of a DG structure consists of a nonlinear Poisson equation for the electrostatic potential ϕ

$$\nabla[\epsilon\nabla\phi] = -\rho[\phi] = -q[-n[\phi] + p[\phi] + N_D^+[\phi] - N_A^-[\phi]] \tag{B1}$$

coupled with an eigenvalue problem for Schrödinger's equation,

$$\hat{H}\psi_n \equiv -\frac{\hbar}{2}\frac{1}{\sigma}\nabla\left[\frac{1}{m^*}\frac{1}{\sigma}\nabla\psi_n\right] + (V_h - q\phi)\psi_n = E_n\psi_n \tag{B2}$$

where ϵ is the dielectric constant, q is the unit electric charge, m^* the effective electron mass, ρ the total charge density, n and p electron and hole concentrations, N_D^+ and N_A^- ionized doner and acceptor concentrations, $\hat{H}$ the Hamiltonian operator, ψ_n the wave function belonging to the energy level E_n, V_h the hetero-junction step potential and finally σ the complex stretching function. On the other hand, for device applications the most interesting quantity is the quantum electron density,

$$n_q = N_q \sum_n |\psi_n|^2 \mathcal{F}_k\left(\frac{E_f - E_n}{kT}\right) \tag{B3}$$

where T denotes the temperature, k the Boltzmann's constant, E_f the Fermi level and $\mathcal{F}_k$ is the complete Fermi-Dirac integrals of order k. These integrals are usually defined as

$$\mathcal{F}_k(x) = \frac{1}{\Gamma(k+1)}\int_0^\infty \frac{t^k dt}{e^{t-x}+1}, \quad k > -1 \tag{B4}$$

and they have the interesting property

$$\frac{d}{dx}\mathcal{F}_k(x) = \mathcal{F}_{k-1}(x) \tag{B5}$$

which allows an analytical continuation to any $k \leq -1$. In this work we consider a DG MOS structure, which is characterized by 1D confinement of carriers. Then $k = 0$ and we can write accordingly,

$$N_\mathrm{q} = \frac{kTm_{dn}^*}{\pi\hbar^2} \tag{B6}$$

$$\mathcal{F}_0(x) = \ln[1 + e^x] \tag{B7}$$

2. Approximation of the Quantum Electron Density

The electrostatic potential enters the quantum electron density $n_\mathrm{q}[\phi]$ through the energy levels $E_n[\phi]$ and complex wave functions $\psi_n[\phi]$:

$$n_\mathrm{q}[\phi] = N_\mathrm{q} \sum_n |\psi_n[\phi]|^2 \mathcal{F}_k\left(\frac{E_f - E_n[\phi]}{kT}\right) \tag{B8}$$

A perturbation,

$$\phi \rightarrow \phi + \delta\phi \tag{B9}$$

is introduced modifying both the Hamiltonian of the Schrödinger's equation, namely:

$$\hat{H} \rightarrow \hat{H} - q\delta\hat{\phi}, \tag{B10}$$

and the quantum electron density $n_\mathrm{q}[\phi]$ given as

$$n_\mathrm{q}[\phi] \rightarrow n_\mathrm{q}[\phi + \delta\phi] = n_\mathrm{q}[\phi] + \delta n_\mathrm{q}[\phi, \delta\phi] \tag{B11}$$

Using the derivative property (Eq. B5) of Fermi-Dirac integrals then δn_q can be written as

$$\begin{aligned}\delta n_\mathrm{q}[\phi, \delta\phi] = &-\frac{N_\mathrm{q}}{kT}\sum_n \psi_n^2[\phi]\,\mathcal{F}_{k-1}\left(\frac{E_f - E_n[\phi]}{kT}\right)\delta E_n[\phi, \delta\phi] \\ &+ 2N_\mathrm{q}\sum_n \psi_n[\phi]\delta\psi_n[\phi, \delta\phi]\mathcal{F}_k\left(\frac{E_f - E_n[\phi]}{kT}\right).\end{aligned} \tag{B12}$$

Utilizing first order perturbation theory we can calculate both $\delta E_n[\phi, \delta\phi]$ and $\delta\psi_n[\phi, \delta\phi]$ assuming that ψ_n is nondegenerate,

$$\delta E_n[\phi, \delta\phi] = -q\langle\psi_n|\delta\hat{\phi}|\psi_n\rangle,$$

$$\delta\psi_n[\phi, \delta\phi] = -q\sum_{j\neq n}\psi_j[\phi]\frac{\langle\psi_j|\delta\hat{\phi}|\psi_n\rangle}{E_n[\phi]-E_j[\phi]}, \tag{B13}$$

where we have introduced these expressions back into $\delta n_{\mathrm{q}}[\phi, \delta\phi]$:

$$\begin{aligned}&\delta n_{\mathrm{q}}[\phi, \delta\phi]\\ &= \frac{qN_{\mathrm{q}}}{kT}\sum_n \psi_n^2[\phi]\,\mathcal{F}_{k-1}\left(\frac{E_f - E_n[\phi]}{kT}\right)\langle\psi_n|\delta\hat{\phi}|\psi_n\rangle\\ &- 2qN_{\mathrm{q}}\sum_n\sum_{j\neq n}\psi_n[\phi]\psi_j[\phi]\frac{\langle\psi_j|\delta\hat{\phi}|\psi_n\rangle}{E_n[\phi]-E_j[\phi]}\mathcal{F}_k\left(\frac{E_f - E_n[\phi]}{kT}\right).\end{aligned} \tag{B14}$$

The sum as well as the scalar product in the second term is symmetric in *j* and *n*. Using this property it is possible to symmetrize the above expression as

$$\begin{aligned}\delta n_{\mathrm{q}}[\phi, \delta\phi] &= \frac{qN_{\mathrm{q}}}{kT}\sum_n \psi_n^2[\phi]\,\mathcal{F}_{k-1}\left(\frac{E_f - E_n[\phi]}{kT}\right)\langle\psi_n|\delta\hat{\phi}|\psi_n\rangle\\ &- qN_{\mathrm{q}}\sum_n\sum_{j\neq n}\psi_n[\phi]\psi_j[\phi]\langle\psi_j|\delta\hat{\phi}|\psi_n\rangle\\ &\times\frac{\mathcal{F}_k\left(\frac{E_f - E_n[\phi]}{kT}\right) - \mathcal{F}_k\left(\frac{E_f - E_j[\phi]}{kT}\right)}{E_n[\phi]-E_j[\phi]}.\end{aligned} \tag{B15}$$

The double sum in the above formula is rather undesirable for numerical purpose. Besides, (B15) is only valid for nondegenerate levels E_n and it is difficult to generalize for accidental degeneracies as is possible in systems with two quantization directions. Seeking to improve (Eq. B15), while retaining as much of its accuracy as possible, Trellakis has proposed to approximate the differential quotient by a derivative:

$$\frac{\mathcal{F}_k\left(\frac{E_f - E_n[\phi]}{kT}\right) - \mathcal{F}_k\left(\frac{E_f - E_j[\phi]}{kT}\right)}{E_n[\phi]-E_j[\phi]} \approx -\frac{1}{kT}\mathcal{F}_{k-1}\left(\frac{E_f - E_n[\phi]}{kT}\right). \tag{B16}$$

Inserting (B16) into δn_{q}, the following approximation for $\delta\widetilde{n_{\mathrm{q}}}$ can be written, namely:

$$\begin{aligned}&\delta\widetilde{n_{\mathrm{q}}}[\phi,\delta\phi]\\&=\frac{qN_{\mathrm{q}}}{kT}\sum_{n}\psi_n^2[\phi]\,\mathcal{F}_{k-1}\left(\frac{E_f-E_n[\phi]}{kT}\right)\langle\psi_n|\delta\hat{\phi}|\psi_n\rangle\\&+\frac{qN_{\mathrm{q}}}{kT}\sum_{n}\psi_n[\phi]\mathcal{F}_{k-1}\left(\frac{E_f-E_n[\phi]}{kT}\right)\sum_{j\neq n}\psi_j[\phi]\langle\psi_j|\delta\hat{\phi}|\psi_n\rangle.\end{aligned} \tag{B17}$$

Next, we will take into account the completeness and orthonormality of the wave functions ψ_n in the Hilbert space, that is

$$\sum_{j\neq n}\psi_j[\phi]\langle\psi_j|\delta\hat{\phi}|\psi_n\rangle=\delta\phi\psi_n[\phi]-\psi_n[\phi]\langle\psi_n|\delta\hat{\phi}|\psi_n\rangle. \tag{B18}$$

Substituting this formula into (B17) all the terms containing scalar products cancel to yield the following expression:

$$\delta\widetilde{n_{\mathrm{q}}}[\phi,\delta\phi]=N_{\mathrm{q}}\sum_{n}\psi_n^2[\phi]\,\mathcal{F}_{k-1}\left(\frac{E_f-E_n[\phi]}{kT}\right)\frac{q\delta\phi}{kT} \tag{B19}$$

An approximation $\widetilde{n_{\mathrm{q}}}(\phi)$ for $n_{\mathrm{q}}(\phi)$ itself can be obtained from the following relationship

$$\widetilde{n_{\mathrm{q}}}[\phi,\delta\phi]=\widetilde{n_{\mathrm{q}}}[\phi]+\delta\widetilde{n_{\mathrm{q}}}[\phi,\delta\phi], \tag{B20}$$

and applying the derivative property of Fermi-Dirac integrals (B5), the following final result arises:

$$\widetilde{n_{\mathrm{q}}}[\phi,\delta\phi]=N_{\mathrm{q}}\sum_n\psi_n^2[\phi]\,\mathcal{F}_k\left(\frac{E_f-E_n[\phi]+q\delta\phi}{kT}\right) \tag{B21}$$

Comparing this formula to the original quantum electron density (B8), we can observe that the only change corresponds to a modified set of energy levels E_n due to the change in the electrostatic potential, namely

$$E_n[\phi] \to E_n[\phi] - q\delta\phi. \tag{B22}$$

3. Schrödinger-Poisson Solution Using a Predictor-Corrector Approach

Now, it is possible to detail how to solve the system of coupled partial differential equations using a predictor-corrector approach. The main feature here is the solution of a nonlinear Poisson equation,

$$\nabla[\epsilon\nabla\phi] = q\left[\widetilde{n_{\mathrm{q}}}[\phi] - p[\phi] - N_D^+[\phi] + N_A^-[\phi]\right], \tag{B23}$$

where the potential independent quantum electron density n_{q} is replaced by the potential dependent predictor,

$$\widetilde{n_{\mathrm{q}}}[\phi] = N_{\mathrm{q}} \sum_n \psi_n^{(k)2}\, \mathcal{F}_k\left(\frac{E_f - E_n^{(k)} + q\left(\phi - \phi^{(k)}\right)}{kT}\right), \tag{B24}$$

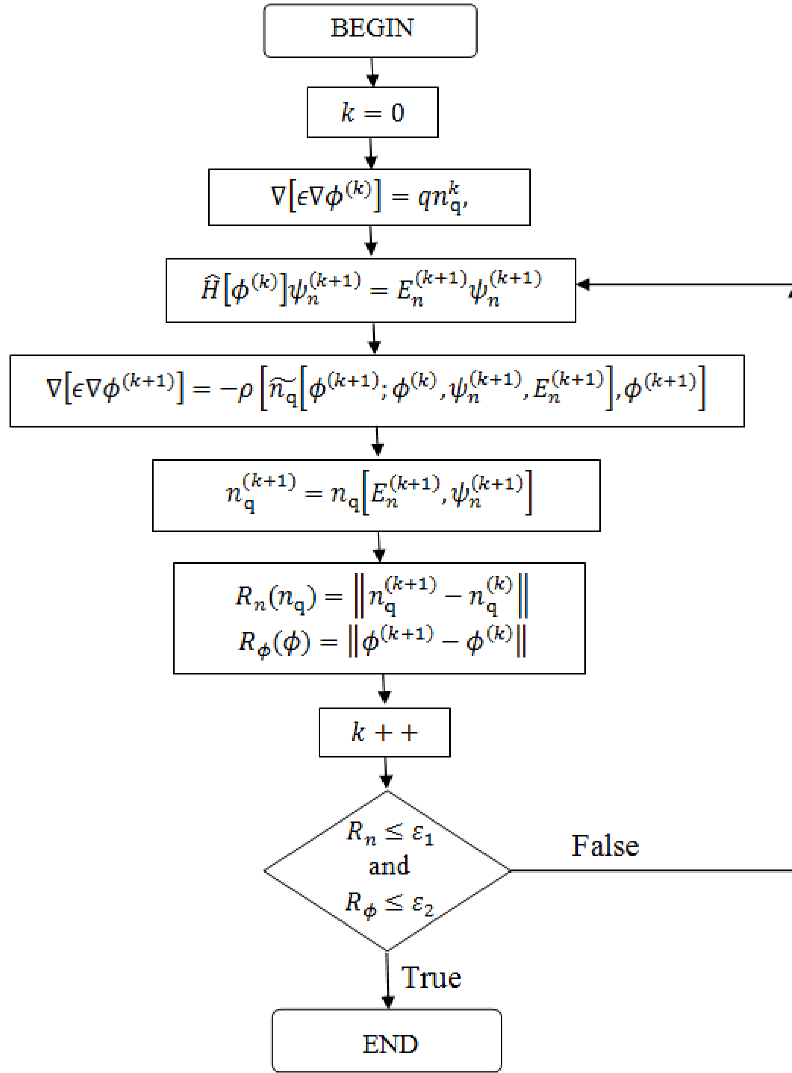
where superscript (k) denote quantities obtained in the previous outer iteration step. The electrostatic potential $\phi^{(k+1)}$ obtained from Poisson's equation (B23) is the one used within the Schrödinger's equation (corrector),

$$-\frac{\hbar}{2}\frac{1}{\sigma}\nabla\left[\frac{1}{m^*}\frac{1}{\sigma}\nabla\psi_n^{(k+1)}\right] + \left(V_h - q\phi^{(k+1)}\right)\psi_n^{(k+1)} = E_n^{(k+1)}\psi_n^{(k+1)}, \tag{B25}$$

to calculate a corrected update of n_{q}, namely

$$n_{\mathrm{q}}^{(k+1)} = N_{\mathrm{q}} \textstyle\sum_n \psi_n^{(k+1)2}\, \mathcal{F}_k\left(\frac{E_f - E_n^{(k+1)}}{kT}\right). \tag{B26}$$

The above algorithm is summarized as follows:


BEGIN
$k = 0$
$\nabla[\epsilon\nabla\phi^{(k)}] = qn_q^k,$
$\hat{H}[\phi^{(k)}]\psi_n^{(k+1)} = E_n^{(k+1)}\psi_n^{(k+1)}$
$\nabla[\epsilon\nabla\phi^{(k+1)}] = -\rho\left[\widetilde{n_q}\left[\phi^{(k+1)}; \phi^{(k)}, \psi_n^{(k+1)}, E_n^{(k+1)}\right], \phi^{(k+1)}\right]$
$n_q^{(k+1)} = n_q\left[E_n^{(k+1)}, \psi_n^{(k+1)}\right]$
$R_n(n_q) = \left\|n_q^{(k+1)} - n_q^{(k)}\right\|$
$R_\phi(\phi) = \left\|\phi^{(k+1)} - \phi^{(k)}\right\|$
$k++$
$R_n \le \varepsilon_1$
and
$R_\phi \le \varepsilon_2$
False
True
END

CONCLUSIONS

The main contributions of this thesis are in the field of compact and numerical modeling of the gate tunneling in Double-Gate MOSFETs in the scaling context of CMOS technology and can be summarized in the following items:

1. A simple compact quantum model for the electrostatic potential, electric charge and gate capacitance in thin-film symmetric DG MOSFET with undoped body has been developed and assessed. As a novelty, this model presents closed explicit expressions on bias and geometrical parameters avoiding numerical iterations. The results are in close agreement with self-consistent solutions [P1].

2. An explicit compact quantum model for the gate tunneling current in DG MOSFET with SiO_2 as gate dielectric has been developed and assessed. Specifically, an explicit closed-form expression is proposed, useful for the fast evaluation of the gate leakage in the context of electrical circuit simulators [P2].

3. An extension to the model for the gate tunneling current in DG MOSFET with SiO_2 as gate dielectric has been developed. Specifically, an explicit compact quantum model for the direct tunneling current through dual layer SiO_2/high-κ dielectrics is proposed. The explicit closed-form expression of this model is useful to study the impact of dielectric constants and band offsets in determining the gate leakage and useful for the fast evaluation of the gate leakage in the context of electrical circuit simulators [P3].

4. A numerical accurate description of tunneling in Double-Gate and Single-Gate MOSFETs devices through layers of high-κ (HK) dielectrics, which relies on the precise determination of quasi-bound states and their penetration in the gate metal, has been developed. For this purpose the Perfectly Matched Layer method (PML) is embedded in each iteration of a 1D Schrödinger-Poisson solver [P4].

5. Our numerical modeling by adopting the PML method can be extended to 2D and even 3D regions with different geometries making it suitable for non- planar MG MOSFETs such as the SOI FinFETs, SOI Tri-Gate, SOI Pi-Gate, SOI gate-all-around or bulk Tri-Gate.

Thesis Publications

[P1] **F. Chaves, D. Jiménez and J. Suñé,** *Explicit Quantum Potential and Charge Model for Double-Gate MOSFETs.* Solid State Electronics, Vol. 54, pp. 530-535, May (2010).

[P2] **F. Chaves, D. Jiménez and J. Suñé,** *Explicit Model for the Gate Tunneling in Double-Gate MOSFETs.* Solid State Electron., Vol. 68, pp. 93-97, Jun. (2011).

[P3] **F. Chaves, D. Jiménez and J. Suñé,** *Explicit Model for Direct Tunneling in Double-Gate MOSFETs Through a Dielectric Stack.* Submitted to Solid State Electron., Dic. (2011).

[P4] **F. Chaves, D. Jiménez, F. García Ruiz, Andrés Godoy and J. Suñé,** *Accurate Calculation of the Gate Tunneling Current in Double-Gate and Single-Gate MOSFETs Through Gate Dielectric Stack.* Submitted to IEEE Trans. Electron Devices, Feb. (2012).

Other Publications

[P5] **O. Moldovan, F. Chaves, D. Jiménez, J-P Raskin, B. Iñiguez**, *Accurate prediction of the volume inversion impact on undoped Double Gate MOSFET capacitances,* International Journal of Numerical Modelling: Electronic Networks, Devices and Fields. Vol. 23, pp 447-457, Jun. (2010).

[P6] **O. Moldovan, F. Chaves, D. Jiménez, and B. Iñiguez**. *Compact Charge and Capacitance Modelling of Undoped Ultra-thin Body (SOI) MOSFET's.* Solid State Electronics, Vol. 52, Pages 1867-1871 Selected Papers from the EUROSOI '08 Conference. Dec. (2008).

[P7] **G. Rius, A. Verdaguer, F. Chaves, I. Martín, P. Godignon, E. Lora-Tamayo, D. Jimenez and F. Perez-Murano.** *Characterization at the nanometer scale of local electron beam irradiation of CNT based devices.* Microelectronic Engineering, Vol. 85, pp. 1413-1416, (2008).

[P8] **O. Moldovan, D. Jiménez, J. Roig Guitart, F. Chaves, and B. Iñiguez.** *Explicit Analytical Charge and Capacitance Models of Undoped Double-Gate MOSFETs.* IEEE Trans. Electron Devices, Vol. 54, pp. 1718, (2007).

[P9] **D. Jiménez, X. Cartoixà, E. Miranda, J. Suñè, F. Chaves and S. Roche.** *A simple drain current model for Schottky-barrier carbon nanotube field effect transistors.* Nanotechnology, Vol. 18, pp. 025201, (2007).

[P10] **D. Jiménez, X. Cartoixá, E. Miranda, J. Suñé, F. Chaves, S. Roche**. *A drain current model for Schottky-barrier CNT-FETs.* J. Comput. Electron. Vol. 5, pp. 361-364 (2006).

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